THE DATASHEET OF

BQ25040DQCT

1.1A, Single-Input, Single Cell Li-Ion Battery Charger With 50mA LDO and 2.3A Production Test Support

FEATURES

- 30V Input Rating, with Overvoltage Protection (OVP)
- Input Voltage Dynamic Power Management Feature
- 50mA Integrated Low Dropout Linear Regulator (LDO)
- 1% Charge Voltage Regulation Accuracy
- 10% Charge Current Accuracy
- Single-Input Interface Selects USB 100mA, 500mA or User-Programmable Maximum Input Current Limit
- 4.2V at 2.3A Production Test Mode
- Thermal Regulation and Thermal Shutdown Protection for Output Current Control
- Soft-Start Feature to Reduce Inrush Current
- Status Indication – Power Good and Charging/Done
- Available in Small 2mm × 3mm DFN-10 Package

APPLICATIONS

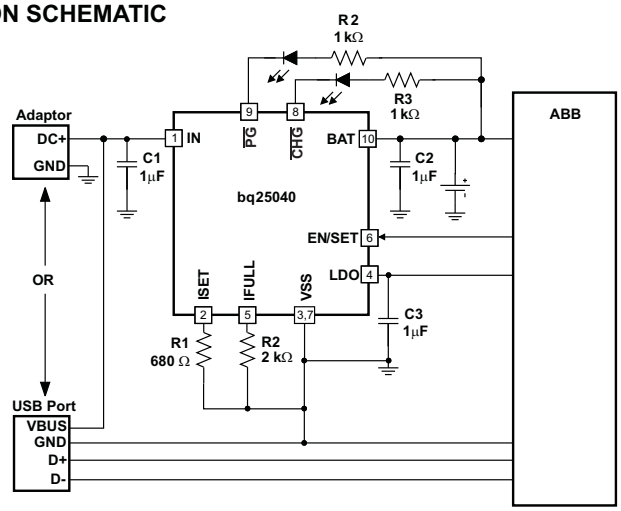
- Mobile Phones
- Smart Phones
- Portable Media Players
- Portable Navigation Devices
- Low-Power Handheld Devices

DESCRIPTION

The bq25040 is an integrated Li-ion linear battery charger targeted at space-limited portable applications. It operates from either a USB port or AC adapter and charges a single cell Li-Ion battery with up to 1.1A of charge current.

The bq25040 has a single power output that charges the battery. A system load can be placed in parallel with the battery. The charge current is programmed using the ISET and EN/SET inputs. The input current limit is programmable to USB100, USB500 or a user programmed current limit up to 1.1A. Additionally, a 4.9V ±3% 50mA LDO is integrated into the IC for supplying low power external circuitry. The single-input interface (EN/SET) is used to select the charge current and to place the bq25040 into Production Test Mode. In Production Test Mode, the bq25040 operates as a linear regulator without a battery connected, where the output is regulated at 4.2V and supplies up to 2.3A to calibrate GSM transceivers.

APPLICATION SCHEMATIC



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

The battery is charged in three phases: conditioning, constant current and constant voltage. In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded.

The charger power stage and charge current sense functions are fully integrated. The charger function has accuracy current and voltage regulation loops, charge status display, and charge termination.

ORDERING INFORMATION

PART NUMBER (1)	$V_{BAT(REG)}$	V_{OVP}	V_{LDO}	MARKING
bq25040DQCR	4.2V	6.9V	4.9V	OAB
bq25040DQCT	4.2V	6.9V	4.9V	OAB

(1) The DQC package is available in the following options:
R - taped and reeled in quantities of 3,000 devices per reel.
T - taped and reeled in quantities of 250 devices per reel.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input voltage	IN (with respect to VSS)	–0.3 to 30	V
	EN/SET, ISET, IFULL (with respect to VSS)	–0.3 to 7	V
Output voltage	BAT, $\overline{CHG}$, $\overline{PG}$ (with respect to VSS)	–0.3 to 7	V
	LDO (with respect to VSS)	-0.3 to 7(2)	V
Input current (Continuous)	IN	1.5	A
Input current (Pulsed)	IN, 20% duty cycle with 10 ms period	2.5	A
Output current (Continuous)	BAT	1.5	A
Output current (Pulsed)	BAT, 20% duty cycle with 10 ms period	2.5	A
Output current (Continuous)	LDO	100	mA
Output sink current	$\overline{CHG}$, $\overline{PG}$	15	mA
Junction temperature, T_J		–40 to 150	°C
Storage temperature, T_{stg}		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) If V_{LDO} is greater than V_{IN}, current must be limited to less than 100mA or damage may occur.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JA}$	$R_{\theta JC}$
10 Pin 2mm × 3mm SON	58.7 °C/W	3.9 °C/W

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. The pad is connected to the ground plane by a 2x3 via matrix.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNITS
V_{IN}	IN voltage range	4.35	26	V
	IN operating voltage range	4.35 (1)	6.7	
I_{IN}	Input current, IN pin (charging)		1.1	A
$I_{IN(PTM)}$	Input current PTM, IN pin, 20% duty cycle with 10ms period		2.3	A
I_O	Output current in charge mode, BAT pin (charging)		1.1	A
$I_{O(PTM)}$	Output current in PTM, BAT pin, 20% duty cycle with 10 ms period		2.3	A
T_J	Junction Temperature	0	125	°C
R_{ISET}	Fast-charge current programming resistor	475	5360	Ω
R_{IFULL}	Charge Done threshold	1	10	kΩ

(1) Operation with V_{IN} < 5V may result in reduced performance due to dropout operation for LDO and/or charger.

ELECTRICAL CHARACTERISTICS

Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
V_{UVLO}	Undervoltage lock-out	V_{IN}: 0V → 4V	3.15	3.30	3.45	V
$V_{HYS(UVLO)}$	Hysteresis on UVLO	V_{IN}: 4V → 0V	190	240	290	mV
$V_{IN(PG)}$	Input Power Good detection threshold $V_{IN(PG)}$ above V_{BAT}	(Input power good if $V_{IN} > V_{BAT} + V_{IN(PG)}$) V_{BAT} = 3.6V, V_{IN}: 3.5V → 4V	30	75	150	mV
$V_{HYS(INPG)}$	Hysteresis on $V_{IN(PG)}$	V_{BAT} = 3.6V, V_{IN}: 4V → 3.5V	18	32	54	mV
$t_{DGL(NO-IN)}$	Delay time, input power loss to charger turn-off	Time measured from V_{IN}: 5V → 2.5V, 1µs fall-time		32		ms
V_{OVP}	Input overvoltage protection threshold	V_{IN}: 5V → 7V	6.7	6.9	7.1	V
$V_{HYS(OVP)}$	Hysteresis on OVP	V_{IN}: 7V → 5V		100		mV
$t_{BLK(OVP)}$	Input overvoltage blanking time			115		µs
$t_{REC(OVP)}$	Input overvoltage recovery time	Time measured from V_{IN}: 11V → 5V 1µs fall-time to $\overline{CHG}$ = LO, V_{BAT} = 3.5V		500		µs
$V_{IN(DPM)}$	Input DPM threshold	VIN Falling, I_{CHRG} reduced to 90%, USB100 or USB500 Mode	4.38	4.43	4.48	V
I_{IN}	USB100 mode input current limit	USB100 programmed by EN/SET, R_{ISET} > 1.1kΩ , V_{BAT} = 3.5V	90	95	100	mA
	USB500 mode input current Limit	USB500 programmed by EN/SET, R_{ISET} > 1.1kΩ , V_{BAT} = 3.5V	380	395	415	
ISET SHORT CIRCUIT TEST						
R_{ISET}	Continuous Monitor	R_{ISET}= 500Ω → 200Ω, IC latches off after $t_{DGL(SHORT)}$	320		460	Ω
$t_{DGL(SHORT)}$	Deglitch time transition from ISET to IC latched off			1.5		ms
I_{LIM}	Current limit with ISET shorted	V_{ISET} = 0V, IC latches off after $t_{DGL(SHORT)}$	1.7	2.0	2.2	A
QUIESCENT CURRENT						
$I_{BAT(PDWN)}$	Battery current into BAT	V_{IN} = 0 V			1	µA
$I_{IN(STDBY)}$	Standby current into IN pin	$V_{IN} \le V_{OVP}$			150	µA
		V_{IN} = 10V			350	
I_{CC}	Active supply current, IN pin	V_{IN} = 6V, no load on BAT pin, $V_{BAT} > V_{BAT(REG)}$, IC enabled			3	mA
BATTERY CHARGER FAST-CHARGE						
$V_{BAT(REG)}$	Battery charge voltage		4.16	4.20	4.24	V
I_{CHRG}	Programmed Output “fast charge” current range	$V_{BAT(REG)} > V_{BAT} > V_{LOWV}$, V_{IN} = 5V, R_{ISET} = 475Ω to 5.36kΩ, User Programmable set by EN/SET	100		1100	mA
$V_{DO(IN-BAT)}$	$V_{IN} - V_{BAT}$	V_{IN} = 4.1V and I_{BAT} = 1A		280	512	mV
I_{CHRG}	Output “fast charge” formula	$V_{BAT(REG)} > V_{BAT} > V_{LOWV}$, V_{IN} = 5 V, User Programmable set by EN/SET		K_{ISET}/R_{ISET}		A

ELECTRICAL CHARACTERISTICS (continued)

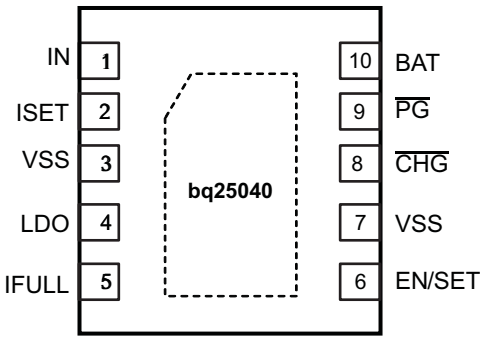
Over junction temperature range 0°C ≤ T_J ≤ 125°C and recommended supply voltage (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
K_{ISET}	Fast charge current factor		480	530	580	AΩ
PRE-CHARGE AND CHARGE DONE						
I_{PRECHG}	Pre-charge current	$V_{BAT} < V_{LOWV}$, V_{IN} = 5V, I_{CHRG} = 250mA to 1100mA	17	20	22	$\%I_{CHG}$
		$V_{BAT} < V_{LOWV}$, V_{IN} = 5V, I_{CHRG} = 100 mA to 249 mA	16	20	27	
V_{LOWV}	Pre-charge to fast-charge transition threshold		2.4	2.5	2.6	V
$t_{DGL1(LOWV)}$	Deglitch time on pre-charge to fast-charge transition			50		µs
$t_{DGL2(LOWV)}$	Deglitch time on fast-charge to pre-charge transition			25		ms
I_{IFULL}	Reference current to IFULL programming resistor		70	75	80	µA
$I_{IFULL\%}$	Charge done current formula	$I_{IFULL\%}$ = 0% to 50% of I_{CHRG}		R_{IFULL}/K_{IFULL}		%
K_{IFULL}	Charge done current factor	V_{IN} = 5V, $I_{CHGDONE}$ = 25mA to 600mA	180	200	220	Ω/%
LDO						
V_{LDO}	LDO Output voltage	$V_{LDO} + V_{DO(LDO)} \le V_{IN} \le V_{OVP}$, I_{LDO} = 0mA to 50mA	4.75	4.90	5.05	V
$I_{LDO(MAX)}$	LDO output current limit	V_{LDO} = 0V	65	125	185	mA
$V_{DO(LDO)}$	LDO Dropout voltage	V_{IN} = 4.5V, I_{LDO} = 50mA		150	300	mV
PRODUCTION TEST MODE						
$V_{BAT(PTM)}$	Production Test Mode BAT Output Voltage	V_{IN} = 5.5V, I_{BAT} = 2A for 4ms pulse	4.116	4.20	4.284	V
$I_{LIM(PTM)}$	Production Test Mode Maximum BAT output current		2.3			A
THERMAL REGULATION						
$T_{J(REG)}$	Temperature regulation limit	T_J Rising		125		°C
$T_{J(OFF)}$	Thermal shutdown temperature	T_J Rising		155		°C
$T_{J(OFF-HYS)}$	Thermal shutdown hysteresis	T_J Falling		20		°C
EN/SET INTERFACE						
$t_{EN/SET(Latch)}$	EN/SET latch timer	Timer to lock pulse count	1.5			ms
$t_{EN/SET(OFF)}$	EN/SET latch timer	Timer to turn off charge current	1.5			ms
$t_{HI(MIN)}$	High duration on EN/SET		100		700	µs
$t_{LO(MIN)}$	Low time duration on EN/SET		100		700	µs
LOGIC LEVELS ON EN/SET						
V_{IL}	Logic LOW input voltage		0		0.4	V
V_{IH}	Logic HIGH input voltage		1.4		6.0	V
$R_{PULLDOWN}$	EN/SET pulldown resistor	See Note (1)		260		kΩ
LOGIC LEVELS ON $\overline{CHG}$ and $\overline{PG}$						
V_{OL}	Output LOW voltage	I_{SINK} = 5mA			0.425	V
I_{IH}	Leakage current	$V_{\overline{CHG}} = V_{\overline{PG}}$ = 5V			1	µA

(1) No specified low without an external pulldown.

PIN CONFIGURATION

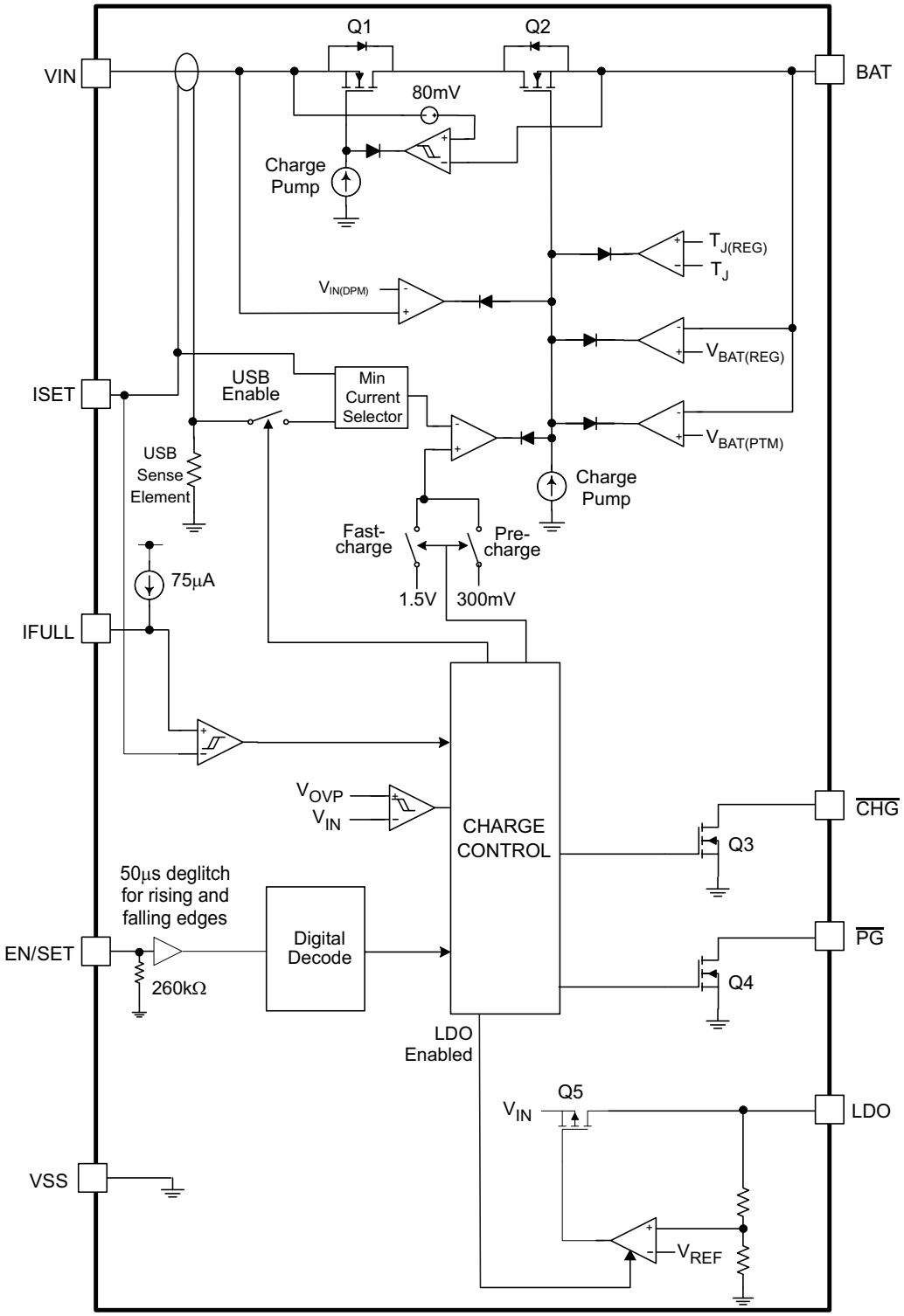
10-Pin 2mm × 3mm DFN
(TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
IN	1	I	Input power supply. IN is connected to the external dc supply (ac adapter or USB port). Bypass IN to VSS with at least a 1µF ceramic capacitor.
ISET	2	I	Current programming input. Connect a resistor from ISET to VSS to program the fast-charge current when the user programmable mode is selected by EN/SET. If the current limit set by ISET is lower than the USB500 limit, the current is limited by the ISET setting even in USB500 mode. The resistor range is between 475Ω and 5.36kΩ to set the current between 100 mA and 1.1 A.
VSS	3, 7	–	Ground terminal. Connect to the thermal pad and the ground plane of the circuit.
LDO	4	O	LDO output. LDO is regulated to 4.9V and drives up to 50mA. Bypass LDO to VSS with at least a 1µF ceramic capacitor. LDO is enabled when VIN is above the UVLO and less than V_{OVP}. The LDO current is not limited by the input current limit.
IFULL	5	I	Charge done current programming input. Connect a resistor from IFULL to VSS to program the charge done threshold. The $\overline{CHG}$ output goes high-impedance when I_{BAT} falls to the charge done threshold. The charge done threshold is programmable from 5% to 50% of the fast charge current programmed at ISET.
EN/SET	6	I	One-wire Interface Input. Drive EN/SET with pulses to enable/disable the device and select different modes. See Table 1 for the data map. EN/SET is pulled to VSS with an internal ~260kΩ resistor.
$\overline{CHG}$	8	O	Charge done indicator open-drain output. $\overline{CHG}$ is pulled low while the device is charging the battery. $\overline{CHG}$ goes high impedance when the battery is fully charged and does not indicate subsequent recharge cycles. $\overline{CHG}$ is high impedance during fault conditions.
$\overline{PG}$	9	O	Power good open-drain output. $\overline{PG}$ is an open-drain output that pulls to VSS when the input power is above the battery voltage by 80mV and below the OVP threshold. $\overline{PG}$ is high impedance when outside this range.
BAT	10	O	Battery connection output. Connect the battery and the system input to BAT. Bypass BAT to VSS with at least a 1µF ceramic capacitor. If no battery is installed, the capacitance on the BAT line must be at least 40µF. In Production Test Mode, BAT regulates to 4.2V and supplies up to 2.3A.
Thermal PAD	Pad	-	There is an internal electrical connection between the exposed thermal pad and the VSS pin of the device. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

BLOCK DIAGRAM



TYPICAL APPLICATION CIRCUITS

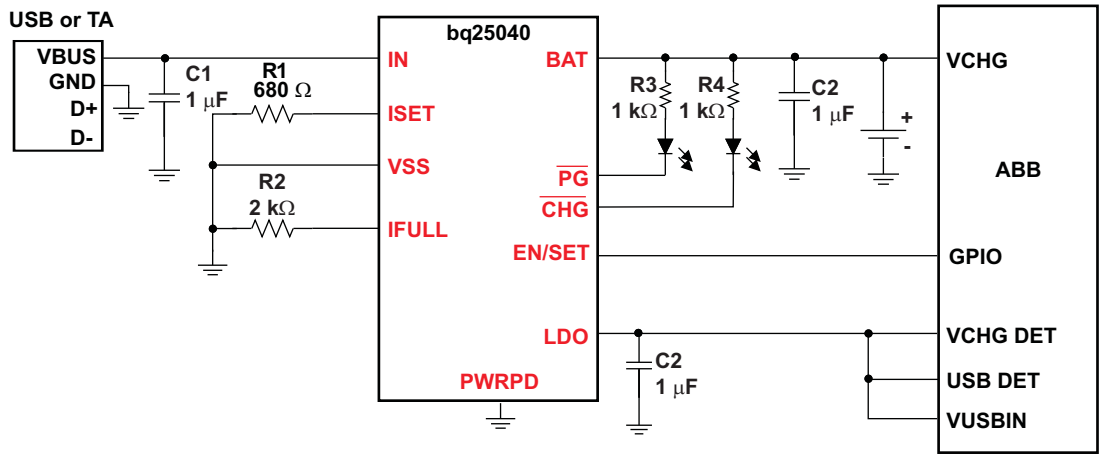


Figure 1. Typical Application Circuit With Battery Always Installed, I_{CHRG} = 780mA, $I_{CHGDONE}$ = 78mA

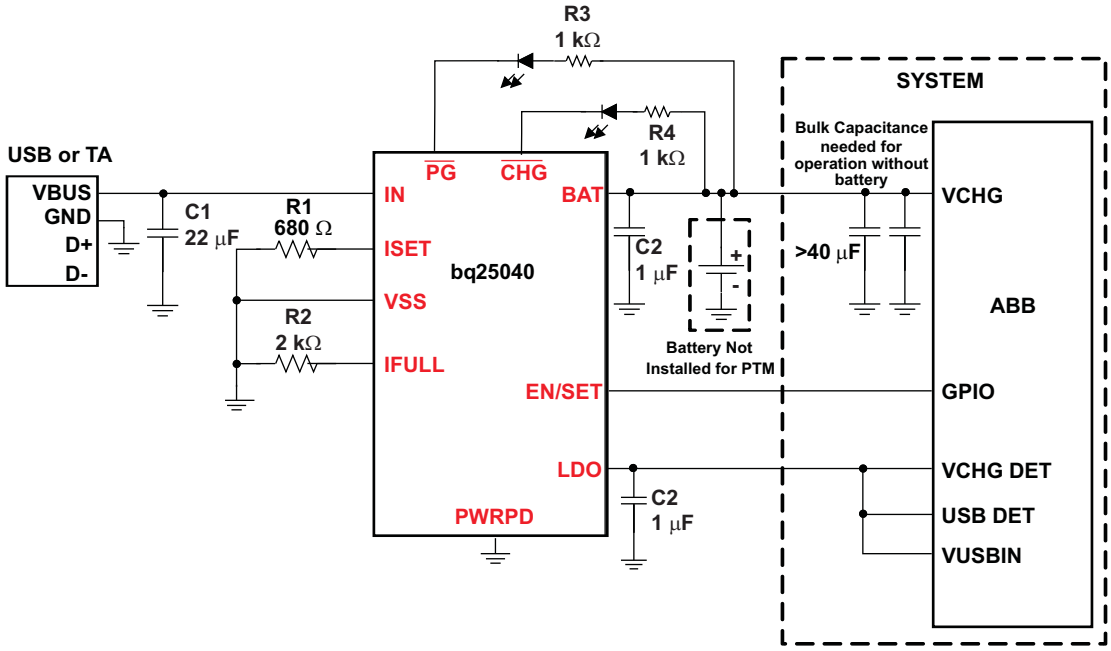


Figure 2. Typical Application Circuit for PTM or With No Battery Installed, I_{CHRG} = 780mA, $I_{CHGDONE}$ = 39mA

TYPICAL CHARACTERISTICS

USB500 Mode, Circuit of Figure 2, T_A = 25°C

Adapter Plugin With Battery Connected Showing Startup With PG, CHG, LDO
$V_{EN/SET}$ = 0V

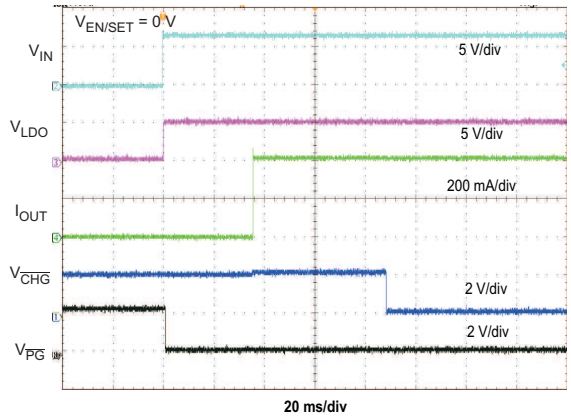


Figure 3.

Charger Enable Using EN/SET

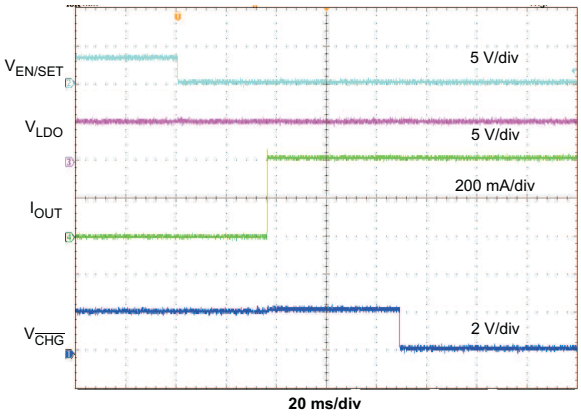


Figure 4.

Charger Disable Using EN/SET

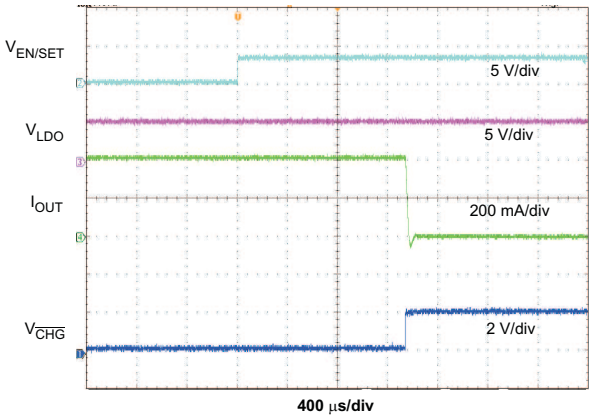


Figure 5.

PTM Load Transient
ROUT = 100Ω to 2.3Ω
Circuit of Figure 2

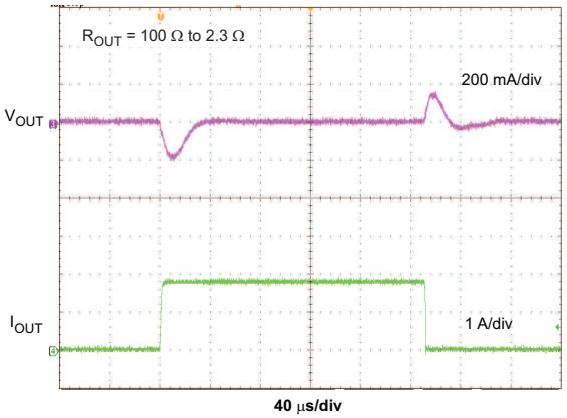


Figure 6.

USB500 to ISET Mode Transition Using EN/SET

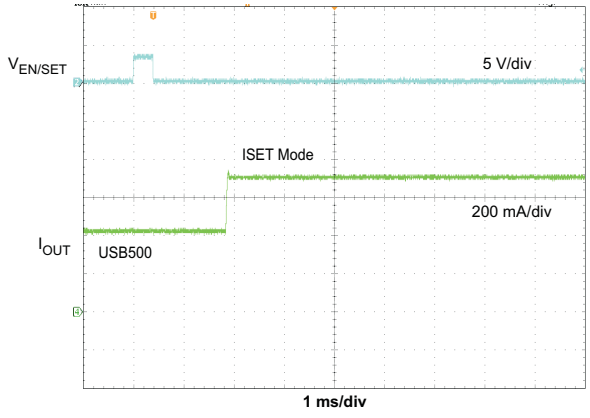


Figure 7.

USB500 to USB100 Mode Transition Using EN/SET

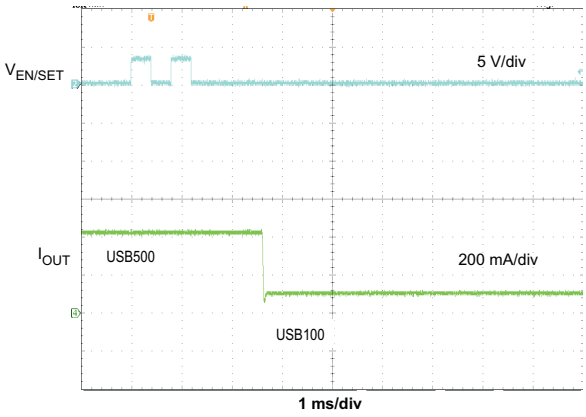


Figure 8.

TYPICAL CHARACTERISTICS (continued)

USB500 Mode, Circuit of Figure 2, T_A = 25°C

UB500 to PTM Transition
Using EN/SET
R_{OUT}=8.4Ω, No battery connected

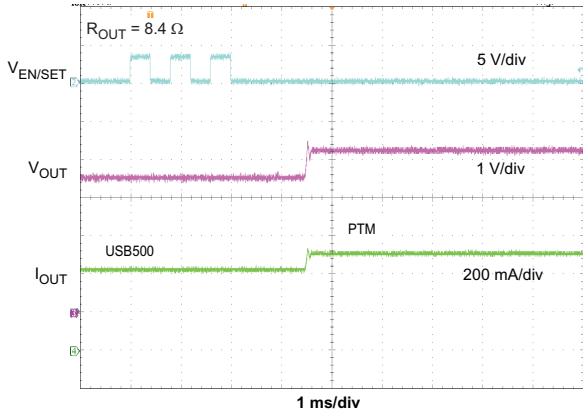


Figure 9.

LDO Load Transient
R_{LDO} = 1kΩ to 100Ω

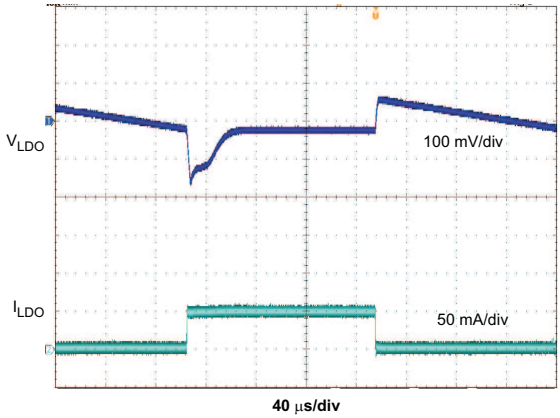


Figure 10.

Complete Charge Cycle

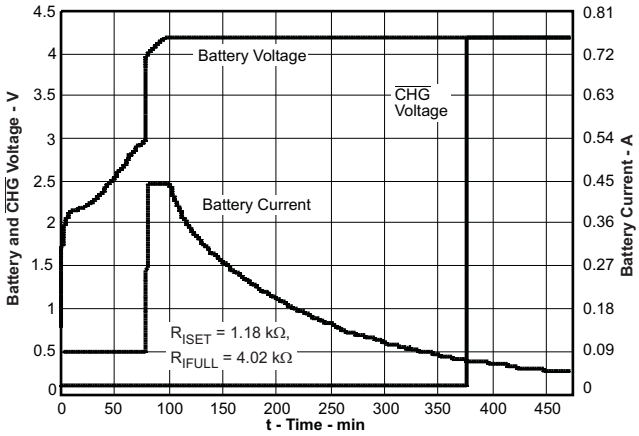


Figure 11.

OVP Fault
V_{IN} = 5V to 12V

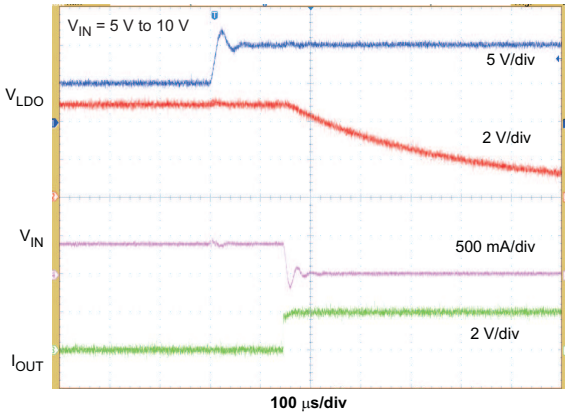


Figure 12.

Thermal Regulation

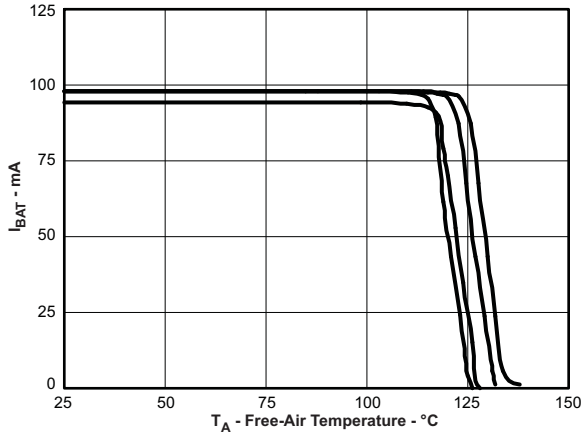


Figure 13.

Dropout Voltage
vs
Temperature

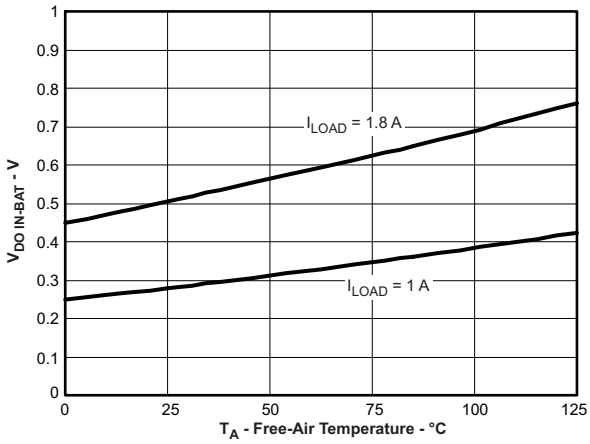


Figure 14.

TYPICAL CHARACTERISTICS (continued)

USB500 Mode, Circuit of Figure 2, T_A = 25°C

Output Regulation Voltage vs Temperature IC in PTM or CV Regulation

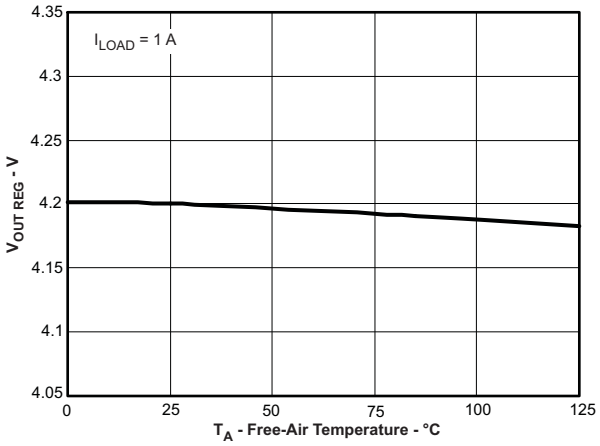


Figure 15.

Output Regulation Voltage vs Input Voltage IC in PTM or CV Regulation

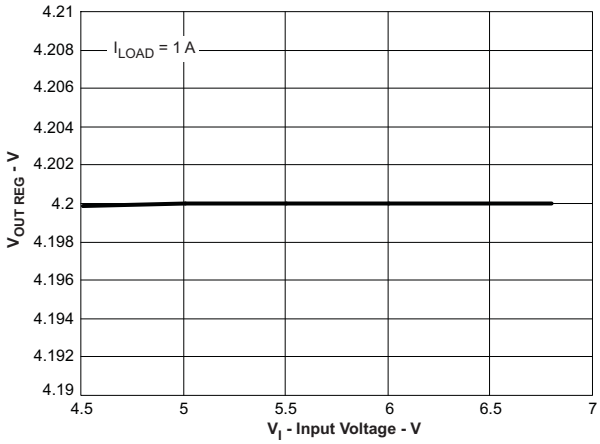


Figure 16.

Overvoltage Protection Threshold vs Temperature

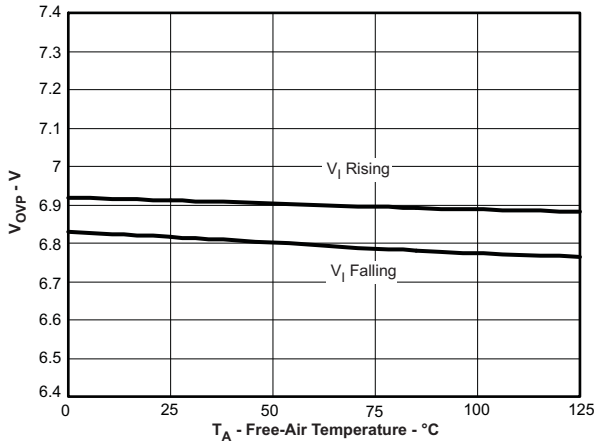


Figure 17.

Fastcharge Current vs Input voltage (USB100, USB500, ISET)

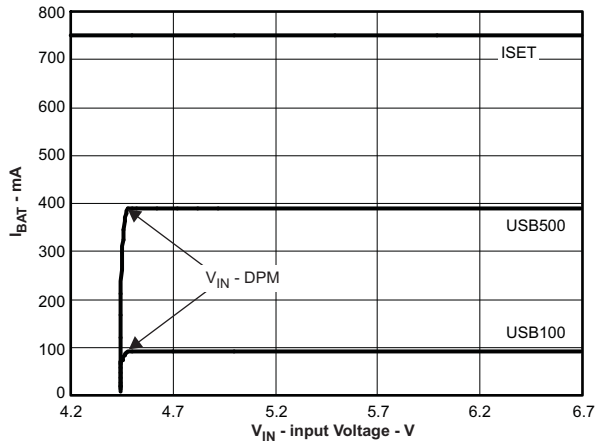


Figure 18.

TYPICAL CHARACTERISTICS (continued)

USB500 Mode, Circuit of Figure 2, T_A = 25°C

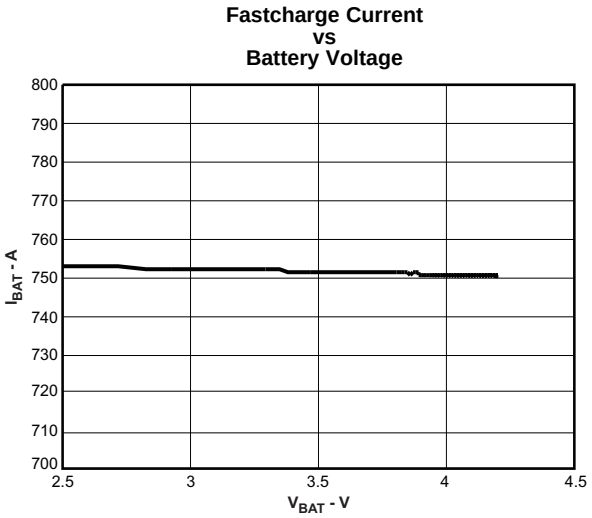


Figure 19.

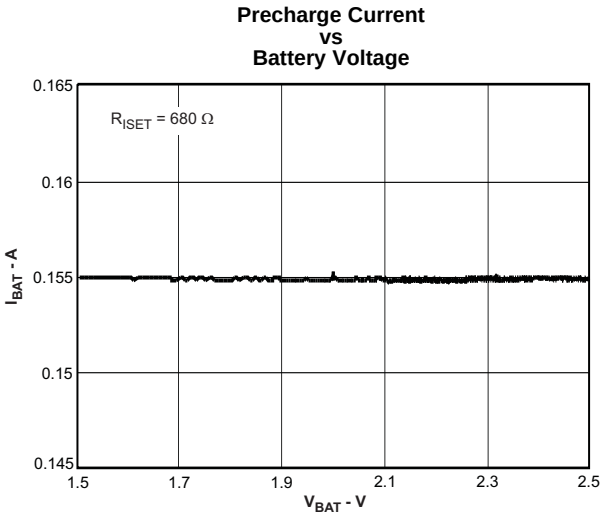


Figure 20.

DETAILED FUNCTIONAL DESCRIPTION

The bq25040 has a single power output that charges a single cell Li-Ion battery from a USB or AC Adapter source. A system load can be placed in parallel with the battery. The charge current is programmed using the ISET and EN/SET inputs. The charge current is programmable to USB100, USB500 or a user programmed charge current up to 1.1A. A Production Test mode is available that supplies up to 2.3A at 4.2V. Additionally, a 4.9V, 50mA linear regulator (LDO) is integrated into the IC for supplying low power external circuitry. The charger power stage and charge current sense functions are fully integrated. The charger function has high accuracy current and voltage regulation loops, charge status display, and charge termination.

Battery Charge Control (BAT)

Charging begins when a battery with a voltage less than V_{RCH} is installed, a valid input source is connected and the EN/SET input is low. A valid input source is defined as V_{IN} greater than V_{BAT} + 80mV and less than V_{OVP}. Additionally, V_{IN} must be above the UVLO. The battery is charged in three phases: conditioning precharge, constant current fast charge (current regulation) and constant voltage tapering (voltage regulation). In all charge phases, an internal control loop monitors the IC junction temperature and reduces the charge current if an internal temperature threshold is exceeded. Figure 21 shows a typical charge profile.

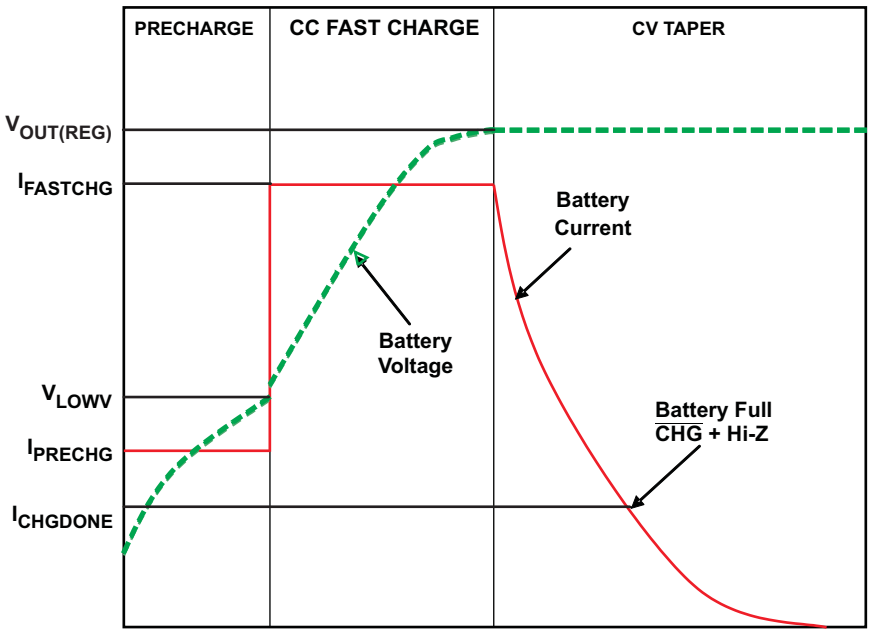


Figure 21. Typical Charge Cycle

When the battery is first installed, the device enters precharge mode. While V_{BAT} is less than V_{LOWV}, the bq25040 remains in precharge mode where the current limit is set to 20% of the current limit programmed at ISET. Once V_{BAT} exceeds V_{LOWV}, the bq25040 enters fast charge mode where the current limit is set by the EN/SET input (USB100, USB500, or ISET. See the *Input Current Limit* section for details). After the battery is charged up to the $V_{BAT(REG)}$, the device enters voltage regulation. V_{BAT} is regulated to $V_{BAT(REG)}$ as the charge current is reduced. Once I_{BAT} decreases to the termination current threshold set by IFULL, the $\overline{CHG}$ output goes high impedance but charging continues. Figure 21 graphically illustrates a typical charge cycle. The bq25040 does not contain charge safety timers, so all safety timers must be done by the host processor.

Single Input Interface (EN/SET)

EN/SET is used to enable/disable the device as well as select the input current limit and Production Test mode. EN/SET is pulled low to enable the device. After the 50µs deglitch expires, the IC enters the 32ms WAIT state. EN/SET may be used to program the current limit during this time. Once t_{WAIT} expires, the IC starts up. If no command is sent to EN/SET during t_{WAIT}, the IC starts up in USB500 mode.

Programming the different modes is done by pulsing the EN/SET input. See Table 1 for a map of the different modes. A valid high pulse is between 100µs and 700µs. The time between pulses must be between 100µs and 700µs to be properly read. Once EN/SET is held low for 1.5ms, the number of pulses is passed to the control logic and decoded and then the mode changes. If during the pulse counting, more than 3 pulses occur, the USB100 mode is immediately selected on the fourth pulse, and the 1.5ms timer does not have to expire. See Figure 22 for a flow diagram of the EN/SET interface.

Once a mode has been programmed once, further pulses on EN/SET are ignored until power is toggled, or the device is disabled and then enabled.

Table 1. Pulse Counting Map for EN/SET Interface

NO. OF PULSES	MODE CONTROL	VALUE
0	Current Limit	USB500 Mode (default for startup)
1	Current Limit	ISET Programmed
2	Current Limit	USB100 Mode
3	Production Test Mode	Enabled
≥ 4	Current Limit	USB100 Mode

If, at any time, the EN/SET input is held high for more than 1.5ms, the IC is disabled. When disabled, charging is suspended and the bq25040 input quiescent current is reduced.

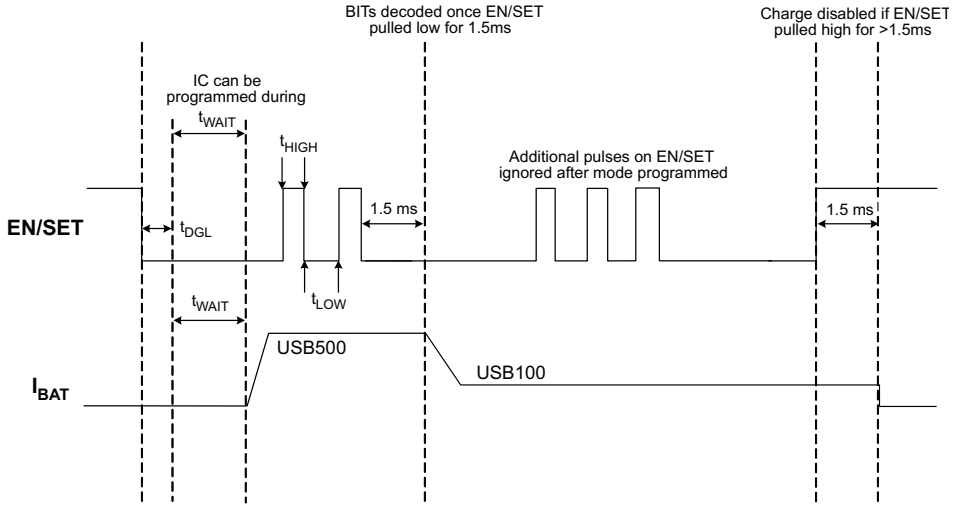


Figure 22. EN/SET Timing Diagram

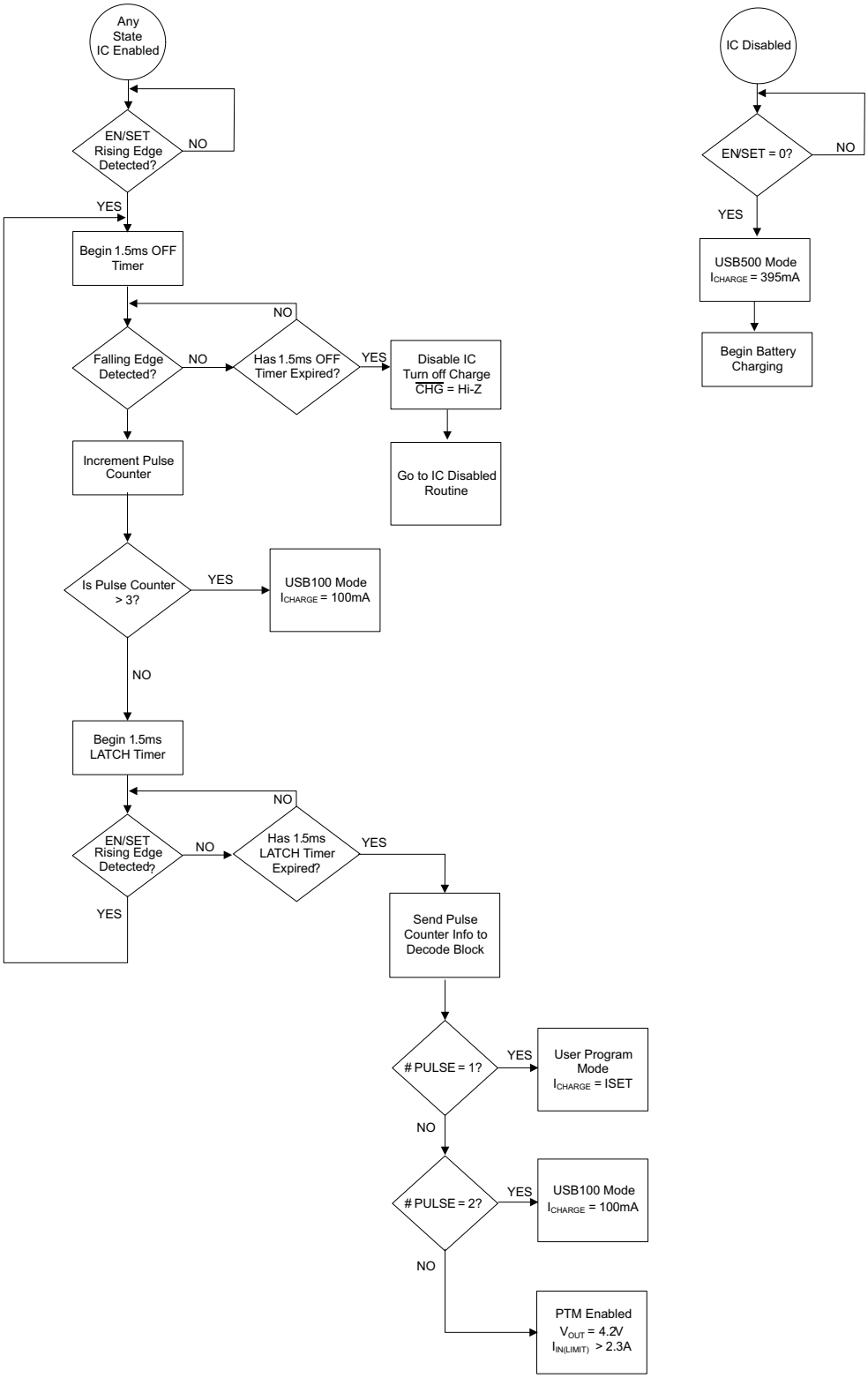


Figure 23. EN/SET State Diagram

Input Current Limit (ISET, EN/SET)

The fast charge current is programmed using the EN/SET and ISET inputs. The EN/SET input allows the user to select USB100 mode, USB500 mode, or the user programmable current set by ISET. The user programmable current is set by connecting a resistor from ISET to VSS. The value of the resistor is determined by:

$$R_{ISET} = \frac{K_{ISET}}{I_{CHG}} \quad (1)$$

The fast charge current (I_{CHG}) must be programmed between 100mA and 1.1A. If the current at ISET is programmed to be less than the USB500 current limit, the current will be limited to the ISET current limit threshold when USB500 mode is selected. Additionally, the precharge current is always 20% of the current programmed by ISET, not 20% of the mode selected by EN/SET. However, if USB100 mode is selected, the precharge current may be restricted to the USB100 limit.

Charge Done Threshold (IFULL)

The charge done threshold is programmed using the IFULL input. The user programmable charge done threshold is set by connecting a resistor from IFULL to VSS. The value of the resistor is determined by:

$$R_{IFULL} = IFULL\% \times K_{IFULL} \quad (2)$$

The charge done threshold (IFULL%) is defined as a percentage of the fast charge current programmed at ISET. IFULL% must be programmed between 5% and 50%. The $\overline{CHG}$ output goes high once I_{BAT} falls below the threshold set by IFULL signaling to the microprocessor that the battery is fully charged and the charge cycle should be terminated, but charging continues until disabled by the EN/SET input.

Production Test Mode (PTM)

The EN/SET interface input for the bq25040 allows the user to select the Production Test mode (PTM). In PTM, BAT is regulated to 4.2V and supplies up to 2.3A for powering external loads with no battery installed. This allows the user to supply loads with no battery connected as in production tests. The IC will not handle continuous dc current of 2.3A. When using currents greater than 1.5A in PTM, the user must limit the duty cycle at the maximum current to 20% with a maximum period of 10ms. In PTM, thermal regulation is disabled; however, thermal shutdown is still active.

Undervoltage Lockout

The bq25040 remains in power down mode when the input voltage is below the undervoltage lockout threshold (UVLO). During this mode, the control input (EN/SET) is ignored. The charge FET connected between IN and BAT is off and the status outputs ($\overline{CE}$ and $\overline{PG}$) are high impedance. Once the input voltage rises above UVLO, the internal circuitry is turned on and the normal operating procedures are followed.

Input Overvoltage Protection

The bq25040 contains an input overvoltage protection circuit that disables the LDO output and charging when the input voltage rises above V_{OVP}. This prevents damage from faulty adapters. The OVP circuitry contains a 115µs deglitch that prevents ringing on the input from line transients from tripping the OVP circuitry falsely. If an adapter with an output greater than V_{OVP} is plugged in, the IC completes soft-start power up and then shuts down if the voltage remains above V_{OVP} after 115µs. The LDO remains off and charging remains disabled until the input voltage falls below V_{OVP}.

Input DPM Mode (V_{IN}-DPM)

The bq25040 uses the V_{IN}-DPM mode for operation from current-limited USB ports. When in USB100 or USB500 mode, V_{IN}-DPM is enabled, the input voltage is monitored. If V_{IN} falls to V_{IN}-DPM, the input current limit is reduced to prevent the input voltage from falling further. This prevents the bq25040 from crashing poorly designed or incorrectly configured USB sources. Figure 24 shows the V_{IN}-DPM behavior to a current limited source. In this figure, the input source has a 250mA current limit and the device is configured with the 395mA current limit (USB500 mode).

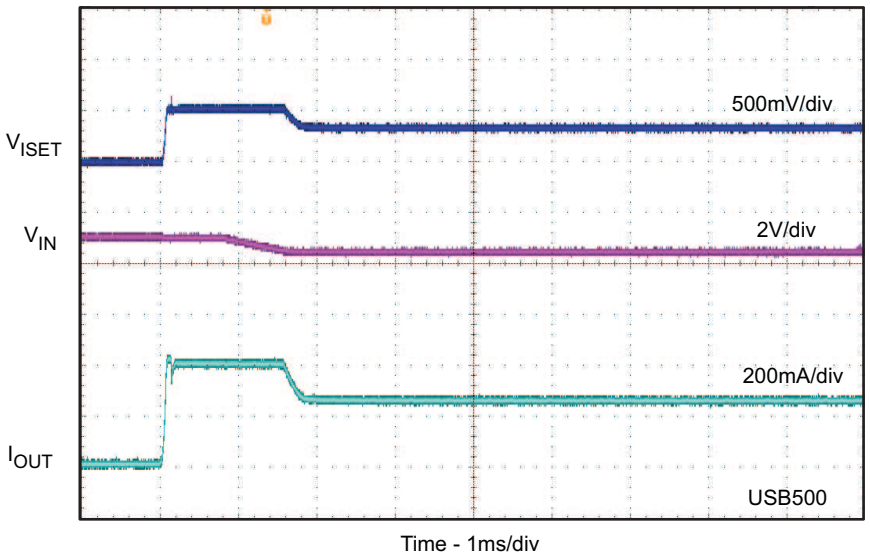


Figure 24. V_{IN}-DPM Protects from Crashing Poor Input Sources

50 mA LDO (LDO)

The LDO output of the bq25040 is a low dropout linear regulator (LDO) that supplies up to 50mA while regulating to V_{LDO}. The LDO is active whenever the input voltage is between UVLO and V_{OVP}. It is not affected by the EN/SET input. The LDO output is used to power circuitry such as USB transceivers in dead battery conditions. This allows the user to operate the product immediately after plugging the adapter in, instead of waiting for the battery to charge to useable levels. Note that the LDO current is not monitored by the input current limit. The LDO current is limited separately and is in addition to the input current limit.

Charge Done Indicator ($\overline{CHG}$)

The bq25040 contains an open drain $\overline{CHG}$ output that indicates when a charge cycle is complete. When charging a battery in precharge, fastcharge or CV mode, the $\overline{CHG}$ output is pulled to VSS. Once the BAT output reaches regulation and the charge current falls below the termination threshold, $\overline{CHG}$ goes high impedance to signal the battery is fully charged. The $\overline{CHG}$ output remains high during subsequent battery refresh charges. Connect $\overline{CHG}$ to the required logic level voltage through a 1kΩ to 100kΩ resistor to use the signal with a microprocessor. Additionally, $\overline{CHG}$ may be used to drive an LED for a visual charging status signal. $I_{\overline{CHG}}$ must be below 15mA.

$\overline{CHG}$ may be pulled up to any voltage rail less than the maximum rating on the $\overline{CHG}$ output. Many LED applications choose to pull up $\overline{CHG}$ to the battery voltage. This is acceptable; however, note that at low battery conditions, the LED may appear dim. Another option is to pull up $\overline{CHG}$ to the LDO output. This is also acceptable; however, note that the LDO current is not limited by the input current limit and the additional current may cause the bq25040 input current to exceed the maximum USB100 specification.

Power Good ($\overline{PG}$)

The bq25040 contains a $\overline{PG}$ signal that indicates when a valid input source is connected. The $\overline{PG}$ output goes low when an input source between (V_{BAT} + 80mV) and V_{OVP} is connected. Additionally, the input source must be greater than the UVLO voltage threshold. See Table 2 for the nominal $\overline{PG}$ deglitches under different conditions.

Table 2.

CONDITION	$\overline{PG}$ DEGLITCH (MEASURED FROM EVENT TO $\overline{PG}$ HIGH OR LOW)	
	bq25040 ENABLED (EN/SET low)	bq25040 DISABLED (EN/SET high)
Entering OVP (V_{IN} = 5.5V→10V)	100 µs	0
Leaving OVP (V_{IN} = 10V→5.5V)	450 µs	500 µs
Entering SLEEP (V_{IN} = 5.5V→3.6V)	32 ms	0
Leaving SLEEP(V_{IN} = 3.6V→5.5V)	500 µs	500 µs
Entering UVLO (V_{IN} = 5.5V→2.5V)	0	0
Leaving UVLO (V_{IN} = 2.5V→5.5V)	230 µs	230 µs

$\overline{PG}$ may be pulled up to any voltage rail less than the maximum rating on the $\overline{PG}$ output. Many LED applications choose to pull up $\overline{PG}$ to the battery voltage. This is acceptable, however note that at low battery conditions, the LED may appear dim. Another option is to pull up $\overline{PG}$ to the LDO output. This is also acceptable, however note that the LDO current is not limited by the input current limit and the additional current may cause the bq25040 input current to exceed the maximum USB100 specification.

Thermal Regulation and Thermal Shutdown

The bq25040 contain a thermal regulation loop that monitors the die temperature continuously. If the temperature exceeds $T_{J(REG)}$, the device automatically reduces the charging current to prevent the die temperature from increasing further. The LDO current is not modified by thermal regulation. If the die temperature continues to rise despite the operation of the thermal loop, and increases to $T_{J(OFF)}$, the IC is turned off. Once the device die temperature cools by $T_{J(OFF-HYS)}$, the device turns on and returns to thermal regulation. Continuous over-temperature conditions result in the pulsing of the load current. If the junction temperature of the device exceeds $T_{J(OFF)}$, the charge FET is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} - T_{J(OFF-HYS)}$.

Note that these features monitor the die temperature of the bq25040. This is not synonymous with ambient temperature. Self heating exists due to the power dissipated in the IC because of the linear nature of the battery charging algorithm. Battery NTC monitoring must be done by the host processor.

APPLICATION INFORMATION

Selection of Input/Output Capacitors

In most applications, all that is needed is a high-frequency decoupling capacitor on the input power pin. For normal charging applications, a 1µF ceramic capacitor, placed in close proximity to the IN pin and GND pad works best. For Production Test mode applications, where the current is up to 2.3A, a 22µF input capacitor is required. In some applications, depending on the power supply characteristics and cable length, it may be necessary to increase the input filter capacitor to avoid exceeding the OVP voltage threshold during adapter hot plug events where the ringing exceeds the deglitch time.

The charger in the bq25040 requires a capacitor from BAT to GND for loop stability. Connect a 1µF ceramic capacitor from BAT to GND close to the pins for best results. For Production Test mode applications up to 2.3A, a 40µF capacitor from BAT to GND is required. More output capacitance may be required to minimize the output droop during large load transients.

The LDO also requires an output capacitor for loop stability. Connect at least a 1µF ceramic capacitor from LDO to GND close to the pins. For improved transient response, this capacitor may be increased.

b25040 Charger Design Example

The following sections provide an example for determining the component values for use with the bq25040.

Requirements

Refer to Figure 1 for Schematics of the Design Example.

- Supply voltage = 5V
- Fast charge current of approximately 780 mA; ISET - pin 2
- Full Current Threshold = 10% of Fast Charge; IFULL – pin 5

Calculations

Program the Fast Charge Current (ISET)

$R_{ISET} = K_{ISET} / I_{CHG}$

K_{ISET} = 530AΩ from the electrical characteristics table.

R_{ISET} = 530AΩ/0.78A = 679Ω

Select the closest standard value, which for this case is 680Ω. Connect this resistor between ISET (pin 2) and VSS.

Program the Charge Done Current (IFULL)

$R_{IFULL} = K_{IFULL} \times I_{IFULL\%}$

K_{IFULL} = 200Ω/%.

R_{IFULL} = 200Ω/% × 10% = 2kΩ.

Connect this resistor between IFULL (pin 5) and VSS.

Status Indicators ($\overline{CHG}$ and $\overline{PG}$)

The STAT pins ($\overline{PG}$ and $\overline{CHG}$) are open drain FETs (internal), if used, should be pulled up via a resistor and possibly a LED to a power source. If monitored by a host, the host V_{CC} source should be used. The $\overline{PG}$ and $\overline{CHG}$ are 7V devices. If used as a LED indicator, the BAT, LDO or IN could be used.

If the IN pin is used a 6.2V zener should be used to clamp the voltage if there is a possibility that the input voltage could exceed 7V. If the BAT pin is used, as the battery voltage changes the intensity of the LED will change. The brightness is greatly decreased for a battery voltage less than 3V. The LDO may be the best source to power the LEDs from since it is a regulated source for high input voltages.

Thermal Considerations

The bq25040 is packaged in a thermally enhanced SON package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\vartheta_{JA} = \frac{T_J - T_A}{P_D} \quad (3)$$

Where:

T_J = chip junction temperature
T_A = ambient temperature
P_D = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

The device power dissipation, P_D, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation when a battery pack is being charged:

$$P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$$

Due to the charge profile of Li-Ion batteries the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. See the charging profile. If the board thermal design is not adequate the programmed fast charge rate current may not be achieved under maximum input voltage and minimum battery voltage, as the thermal loop can be active, effectively reducing the charge current to avoid excessive IC junction temperature

PCB Layout Considerations

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from IN to GND (thermal pad) and the output filter capacitors from OUT to GND (thermal pad) should be placed as close as possible to the bq25040, with short trace runs to both IN, OUT and GND (thermal pad).
- All low-current GND connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The high current charge paths into IN pin and from the OUT pin must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bq25040 is packaged in a thermally enhanced QFN package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB); this thermal pad is also the main ground connection for the device. Connect the thermal pad to the PCB ground connection. Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (SLUA271).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ25040DQCR	ACTIVE	WSON	DQC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAB	Samples
BQ25040DQCT	ACTIVE	WSON	DQC	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OAB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

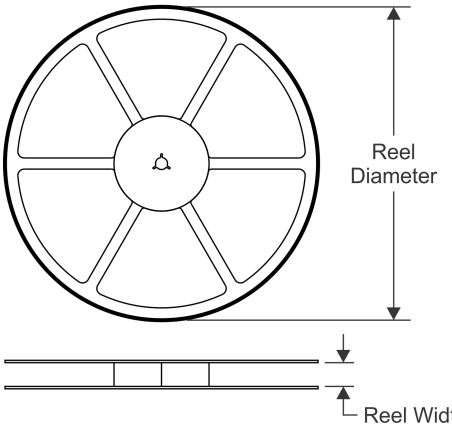
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

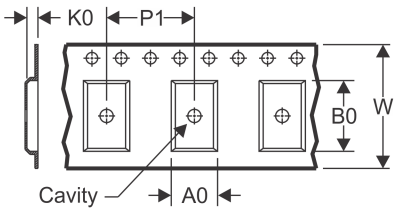
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

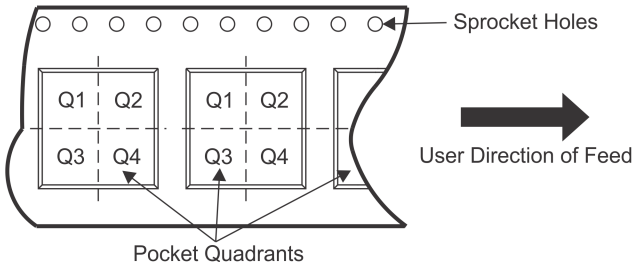


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

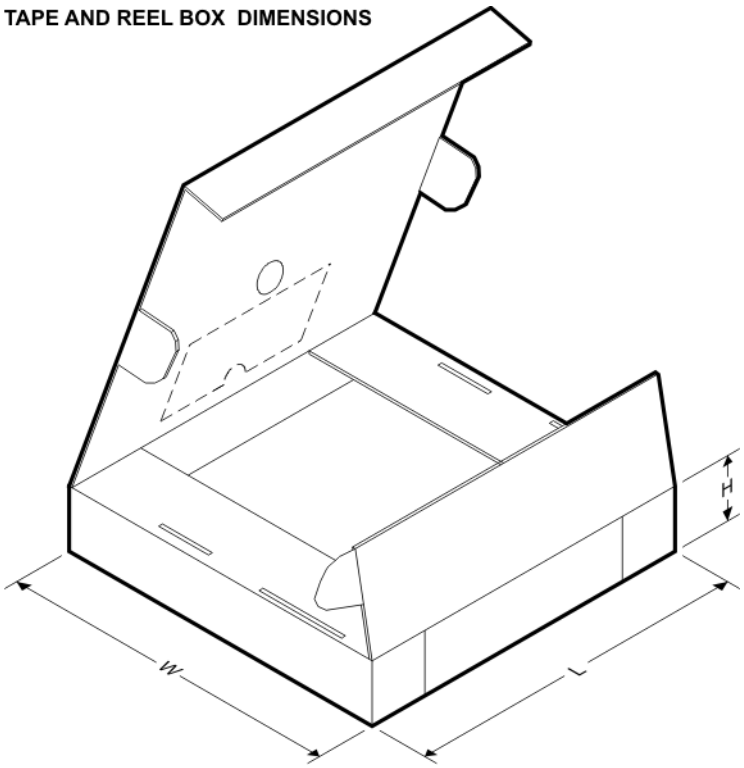
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25040DQCR	WSON	DQC	10	3000	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1
BQ25040DQCT	WSON	DQC	10	250	180.0	8.4	2.25	3.25	1.05	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



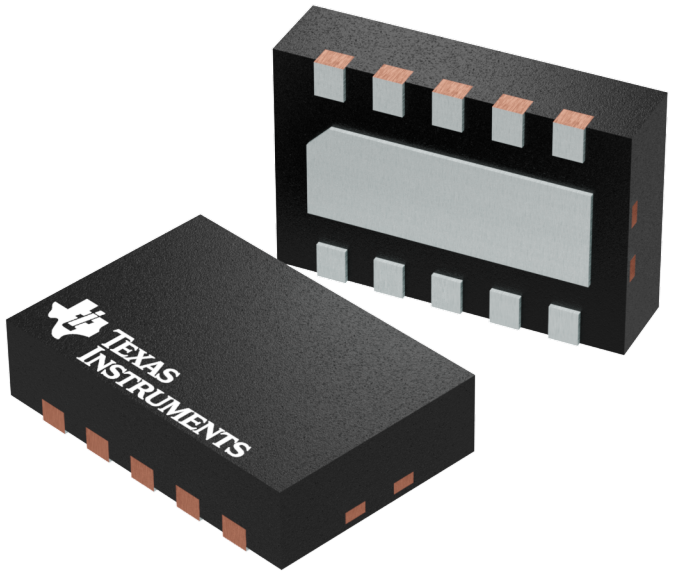
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25040DQCR	WSON	DQC	10	3000	210.0	185.0	35.0
BQ25040DQCT	WSON	DQC	10	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

DQC 10 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

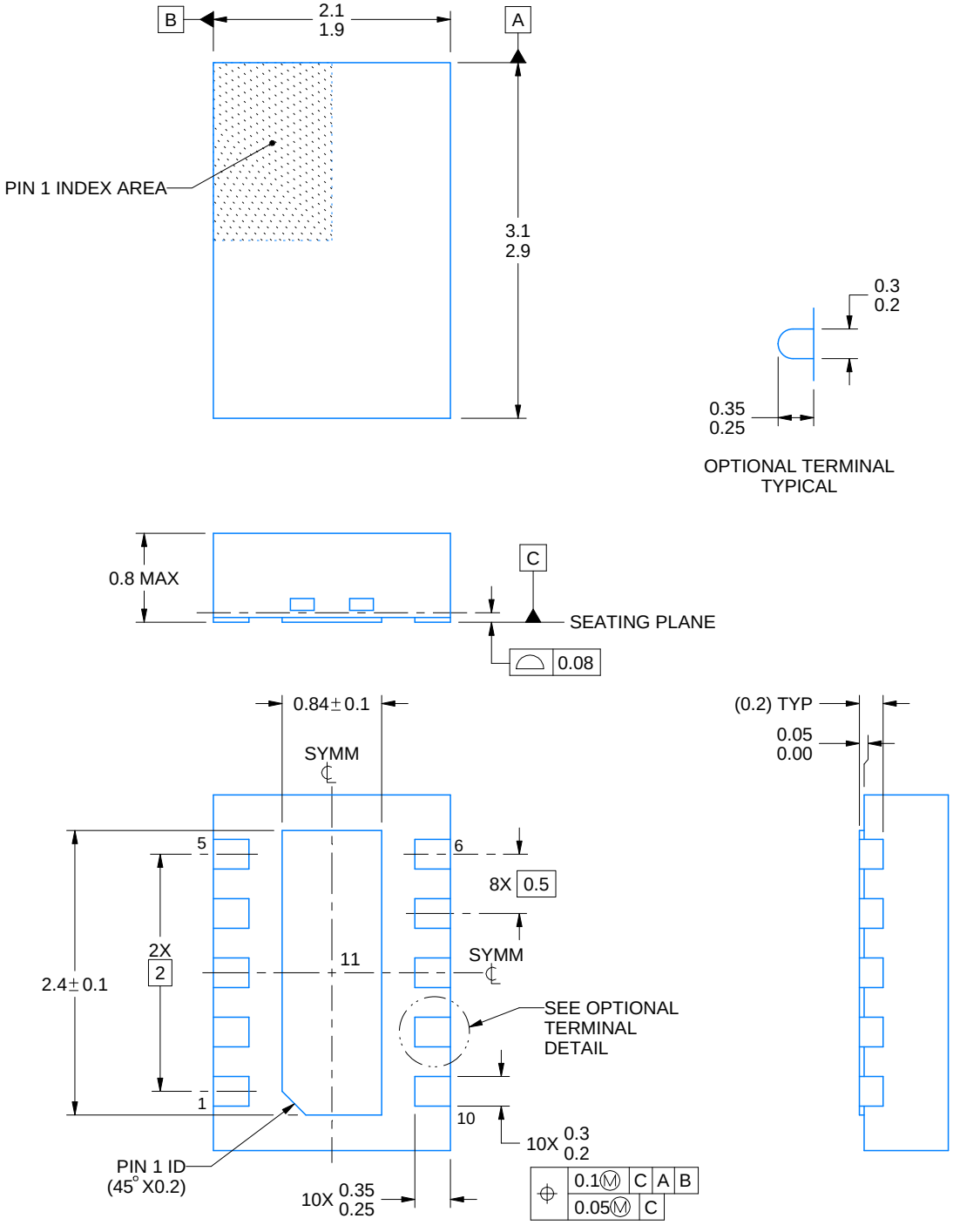
4209674/B

PACKAGE OUTLINE

DQC0010A

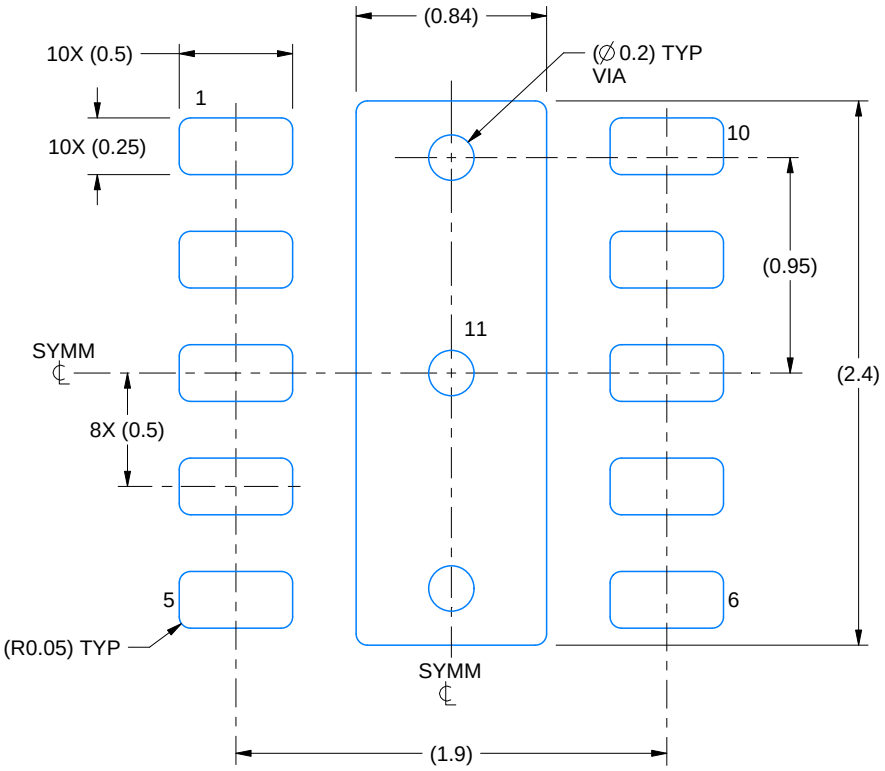
WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD

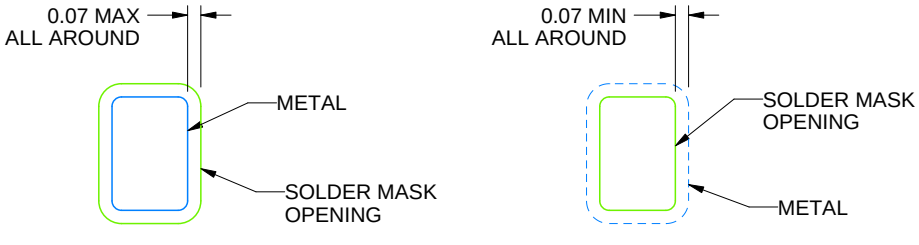


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 30X



SOLDER MASK DETAILS

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NOTES: (continued)

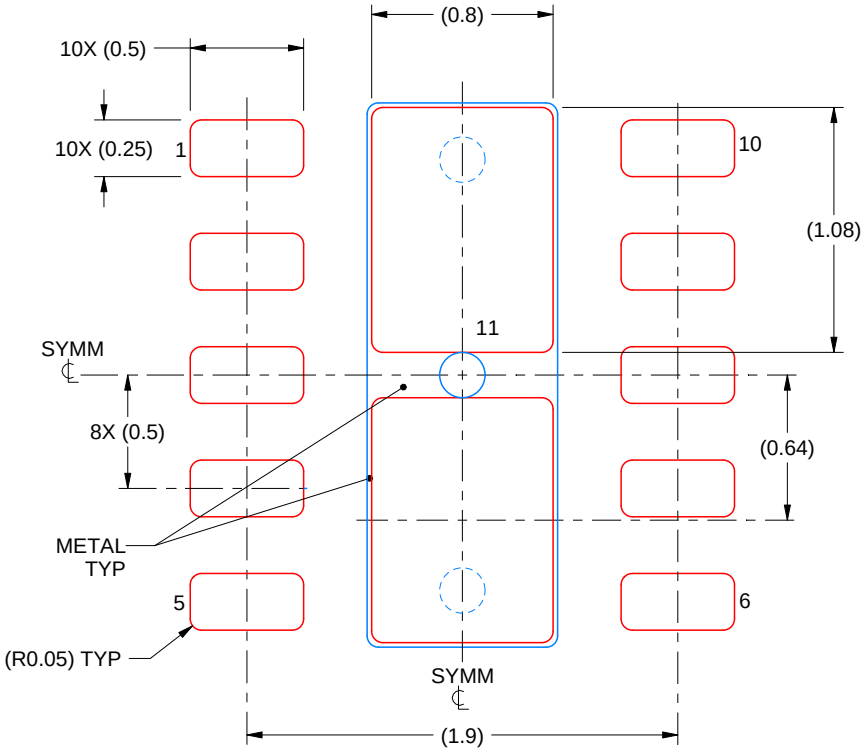
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DQC0010A

WSON - 0.8mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 11:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE: 30X

4218281/B 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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