



**THE DATASHEET OF
AT49BV001AN-55VU**



Features

- Single Supply for Read and Write: 2.7 to 3.6V
- Fast Read Access Time – 55 ns
- Internal Program Control and Timer
- Sector Architecture
 - One 16K Bytes Boot Block with Programming Lockout
 - Two 8K Bytes Parameter Blocks
 - Two Main Memory Blocks (32K Bytes, 64K Bytes)
- Fast Erase Cycle Time – 3 Seconds
- Byte-by-Byte Programming – 30 μ s/Byte Typical
- Hardware Data Protection
- $\overline{\text{DATA}}$ Polling for End of Program Detection
- Low Power Dissipation
 - 15 mA Active Current
 - 50 μ A CMOS Standby Current
- Typical 10,000 Write Cycles
- Green (Pb/Halide-free) Packaging Option

1. Description

The AT49BV001A(N)(T) is a 2.7-volt-only in-system reprogrammable Flash Memory. Its 1 megabit of memory is organized as 131,072 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the device offers access times to 55 ns with power dissipation of just 54 mW over the industrial temperature range.

When the device is deselected, the CMOS standby current is less than 50 μ A. For the AT49BV001AN(T), pin 1 for the PLCC package and pin 9 for the TSOP package are no connect pins. To allow for simple in-system reprogrammability, the AT49BV001A(N)(T) does not require high input voltages for programming. Five-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM; it has standard $\overline{\text{CE}}$, $\overline{\text{OE}}$, and $\overline{\text{WE}}$ inputs to avoid bus contention. Reprogramming the AT49BV001A(N)(T) is performed by erasing a block of data and then programming on a byte by byte basis. The byte programming time is a fast 30 μ s. The end of a program cycle can be optionally detected by the $\overline{\text{DATA}}$ polling feature. Once the end of a byte program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

The device is erased by executing the erase command sequence; the device internally controls the erase operations. There are two 8K byte parameter block sections, two main memory blocks, and one boot block.

The device has the capability to protect the data in the boot block; this feature is enabled by a command sequence. The 16K-byte boot block section includes a reprogramming lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is protected from being reprogrammed.

In the AT49BV001AN(T), once the boot block programming lockout feature is enabled, the contents of the boot block are permanent and cannot be changed. In the AT49BV001A(T), once the boot block programming lockout feature is enabled, the contents of the boot block cannot be changed with input voltage levels of 5.5 volts or less.



**1-megabit
(128K x 8)
Single 2.7-volt
Battery-Voltage
Flash Memory**

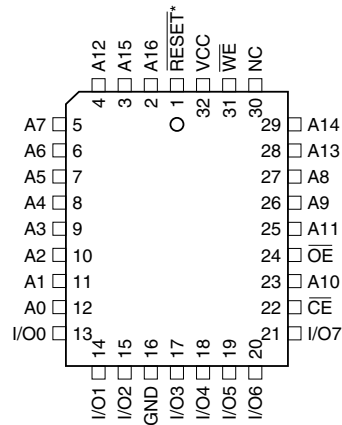
**AT49BV001A
AT49BV001AN
AT49BV001AT
AT49BV001ANT**



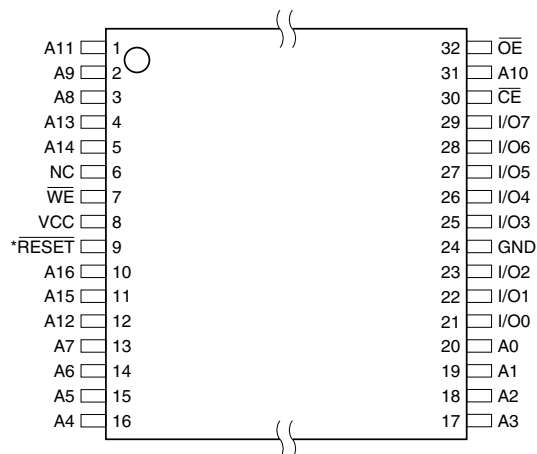
2. Pin Configurations

| Pin Name | Function |
|--------------------|---------------------|
| A0 - A16 | Addresses |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |
| \overline{WE} | Write Enable |
| \overline{RESET} | RESET |
| I/O0 - I/O7 | Data Inputs/Outputs |
| NC | No Connect |

2.1 32-lead PLCC Top View

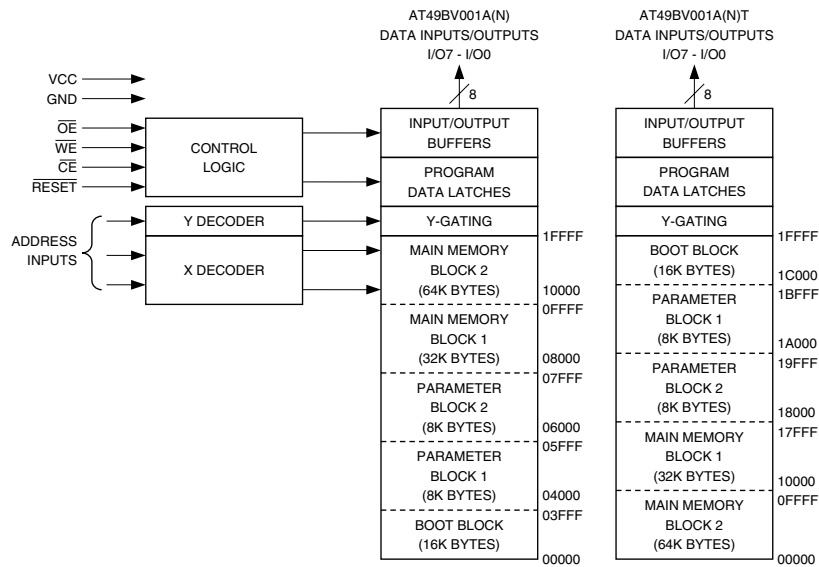


2.2 32-lead VSOP (8 x 14 mm) or 32-lead TSOP, Type 1 (8 x 20 mm) Top View



Note: *This pin is a NC on the AT49BV001AN(T).

3. Block Diagram



4. Device Operation

4.1 Read

The AT49BV001A(N)(T) is accessed like an EPROM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state whenever \overline{CE} or \overline{OE} is high. This dual-line control gives designers flexibility in preventing bus contention.

4.2 Command Sequences

When the device is first powered on it will be reset to the read or standby mode depending upon the state of the control line inputs. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the “Command Definition Table” on page 6. The command sequences are written by applying a low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high. The address is latched on the falling edge of \overline{CE} or \overline{WE} (except for the sixth cycle of the Sector Erase command), whichever occurs last. The data is latched by the first rising edge of \overline{CE} or \overline{WE} . Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

4.3 Reset

A \overline{RESET} input pin is provided to ease some system applications. When \overline{RESET} is at a logic high level, the device is in its standard operating mode. A low level on the \overline{RESET} input halts the present device operation and puts the outputs of the device in a high impedance state. If the \overline{RESET} pin makes a high to low transition during a program or erase operation, the operation may not be successfully completed and the operation will have to be repeated after a high level is applied to the \overline{RESET} pin. When a high level is reasserted on the \overline{RESET} pin, the device returns to the read or standby mode, depending upon the state of the control inputs. By applying a $12V \pm 0.5V$ input signal to the \overline{RESET} pin, the boot block array can be reprogrammed even if the boot block lockout feature has been enabled (see “Boot Block Programming Lockout” on page 4). The RESET feature is not available on the AT49BV001AN(T).

4.4 Erasure

Before a byte can be reprogrammed, the main memory blocks or parameter blocks which contains the byte must be erased. The erased state of the memory bits is a logical “1”. The entire device can be erased at one time by using a 6-byte software code. The software chip erase code consists of 6-byte load commands to specific address locations with a specific data pattern (please refer to the Chip Erase Cycle Waveforms).

After the software chip erase has been initiated, the device will internally time the erase operation so that no external clocks are required. The maximum time needed to erase the whole chip is t_{EC} . If the boot block lockout feature has been enabled, the data in the boot sector will not be erased.

4.4.1 Chip Erase

If the boot block lockout has been enabled, the Chip Erase function will erase Parameter Block 1, Parameter Block 2, Main Memory Block 1 - 2, but not the boot block. If the Boot Block Lockout has not been enabled, the Chip Erase function will erase the entire chip. After the full chip erase the device will return back to read mode. Any command during chip erase will be ignored.

4.4.2 Sector Erase

As an alternative to a full chip erase, the device is organized into sectors that can be individually erased. There are two 8K-byte parameter block sections and two main memory blocks. The 8K-byte parameter block sections and the two main memory blocks can be independently erased and reprogrammed. The Sector Erase command is a six bus cycle operation. The sector address is latched on the rising \overline{WE} edge of the sixth cycle and the 30H data input command is also latched at the rising edge of \overline{WE} . The sector erase starts after the rising edge of \overline{WE} of the sixth cycle. The erase operation is internally controlled; it will automatically time to completion.

4.5 Byte Programming

Once the memory array is erased, the device is programmed (to a logical “0”) on a byte-by-byte basis. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is accomplished via the internal device command register and is a 4 bus cycle operation (please refer to the “[Command Definition Table](#)” on page 6). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of \overline{WE} or \overline{CE} , whichever occurs last, and the data latched on the rising edge of \overline{WE} or \overline{CE} , whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The \overline{DATA} polling feature may also be used to indicate the end of a program cycle.

4.6 Boot Block Programming Lockout

The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 16K bytes. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block’s usage as a write protected region is optional to the user. The address range of the boot block is 00000 to 03FFF for the AT49BV001A(N) while the address range of the boot block is 1C000 to 1FFFF for the AT49BV001A(N)T.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed with input voltage of 5.5V or less. Data in the main memory block can still be changed through the regular programming method. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the [“Command Definition Table” on page 6](#).

4.6.1 Boot Block Lockout Detection

A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry and Exit sections) a read from address location 00002H will show if programming the boot block is locked out for the AT49BV001A(N), and a read from address location 1C002H will show if programming the boot block is locked out for the AT49BV001A(N)T. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification code should be used to return to standard operation.

4.6.2 Boot Block Programming Lockout Override

The user can override the boot block programming lockout by taking the $\overline{\text{RESET}}$ pin to 12 volts during the entire chip erase, sector erase or byte programming operation. When the $\overline{\text{RESET}}$ pin is brought back to TTL levels the boot block programming lockout feature is again active. This feature is not available on the AT49BV001AN(T).

4.7 Product Identification

The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see [“Operating Modes” on page 7](#) (for hardware operation) or Software Product Identification. The manufacturer and device code is the same for both modes.

4.8 $\overline{\text{DATA}}$ Polling

The AT49BV001A(N)(T) features $\overline{\text{DATA}}$ polling to indicate the end of a program cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{DATA}}$ polling may begin at any time during the program cycle.

4.9 Toggle Bit

In addition to $\overline{\text{DATA}}$ polling the AT49BV001A(N)(T) provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

4.10 Hardware Data Protection

Hardware features protect against inadvertent programs to the AT49BV001A(N)(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (c) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.



5. Command Definition Table

| Command Sequence | Bus Cycles | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | | 4th Bus Cycle | | 5th Bus Cycle | | 6th Bus Cycle | |
|-----------------------------------|------------|---------------|------------------|--------------------|------|---------------|------|---------------|-----------------|---------------|------|-------------------|------|
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read | 1 | Addr | D _{OUT} | | | | | | | | | | |
| Chip Erase | 6 | 555 | AA | AAA ⁽²⁾ | 55 | 555 | 80 | 555 | AA | AAA | 55 | 555 | 10 |
| Sector Erase | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | SA ⁽⁵⁾ | 30 |
| Byte Program | 4 | 555 | AA | AAA | 55 | 555 | A0 | Addr | D _{IN} | | | | |
| Boot Block Lockout ⁽³⁾ | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | 555 | 40 |
| Product ID Entry | 3 | 555 | AA | AAA | 55 | 555 | 90 | | | | | | |
| Product ID Exit ⁽⁴⁾ | 3 | 555 | AA | AAA | 55 | 555 | F0 | | | | | | |
| Product ID Exit ⁽⁴⁾ | 1 | XXXX | F0 | | | | | | | | | | |

- Notes:
- The DATA FORMAT in each bus cycle is as follows: I/O7 - I/O0 (Hex). The address format in each bus cycle is as follows: A11 - A0 (Hex); A11 - A16 (don't care).
 - Since A11 is don't care, AAA can be replaced with 2AA.
 - The 16K byte boot sector has the address range 00000H to 03FFFH for the AT49BV001A(N) and 1C000H to 1FFFFH for the AT49BV001A(N)T
 - Either one of the Product ID Exit commands can be used.
 - SA = sector addresses:
 For the AT49BV001A(N):
 SA = 00000 to 03FFF for BOOT BLOCK
 SA = 04000 to 05FFF for PARAMETER BLOCK 1
 SA = 06000 to 07FFF for PARAMETER BLOCK 2
 SA = 08000 to FFFF for MAIN MEMORY ARRAY BLOCK 1
 SA = 10000 to 1FFFF for MAIN MEMORY ARRAY BLOCK 2

 For the AT49BV001A(N)T:
 SA = 1C000 to 1FFFF for BOOT BLOCK
 SA = 1A000 to 1BFFF for PARAMETER BLOCK 1
 SA = 18000 to 19FFF for PARAMETER BLOCK 2
 SA = 10000 to 17FFF for MAIN MEMORY ARRAY BLOCK 1
 SA = 00000 to 0FFFF for MAIN MEMORY ARRAY BLOCK 2

6. Absolute Maximum Ratings

| | |
|---|---------------------------------|
| Temperature Under Bias..... | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| All Input Voltages (including NC Pins) with Respect to Ground | -0.6V to +6.25V |
| All Output Voltages with Respect to Ground | -0.6V to V _{CC} + 0.6V |
| Voltage on \overline{OE} with Respect to Ground | -0.6V to +13.5V |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7. DC and AC Operating Range

| | | AT49BV001A(N)(T)-55 |
|------------------------------|------|---------------------|
| Operating Temperature (Case) | Ind. | -40°C - 85°C |
| V _{CC} Power Supply | | 2.7V - 3.6V |

8. Operating Modes

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | $\overline{RESET}^{(6)}$ | Ai | I/O |
|------------------------------|-----------------|------------------|-----------------|--------------------------|--|----------------------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | V _{IH} | Ai | D _{OUT} |
| Program/Erase ⁽²⁾ | V _{IL} | V _{IH} | V _{IL} | V _{IH} | Ai | D _{IN} |
| Standby/Write Inhibit | V _{IH} | X ⁽¹⁾ | X | V _{IH} | X | High Z |
| Program Inhibit | X | X | V _{IH} | V _{IH} | | |
| Program Inhibit | X | V _{IL} | X | V _{IH} | | |
| Output Disable | X | V _{IH} | X | V _{IH} | | High Z |
| Reset | X | X | X | V _{IL} | X | High Z |
| Product Identification | | | | | | |
| Hardware | V _{IL} | V _{IL} | V _{IH} | | A1 - A16 = V _{IL} , A9 = V _H , ⁽³⁾ A0 = V _{IL} | Manufacturer Code ⁽⁴⁾ |
| | | | | | A1 - A16 = V _{IL} , A9 = V _H , ⁽³⁾ A0 = V _{IH} | Device Code ⁽⁴⁾ |
| Software ⁽⁵⁾ | | | | | A0 = V _{IL} , A1 - A16 = V _{IL} | Manufacturer Code ⁽⁴⁾ |
| | | | | | A0 = V _{IH} , A1 - A16 = V _{IL} | Device Code ⁽⁴⁾ |

- Notes:
- X can be V_{IL} or V_{IH}.
 - Refer to AC Programming Waveforms.
 - V_H = 12.0V ± 0.5V.
 - Manufacturer Code: 1FH, Device Code: 05H – AT49BV001A(N), 04H – AT49BV001A(N)T.
 - See details under Software Product Identification Entry/Exit.
 - This pin is not available on the AT49BV001AN(T).

9. DC Characteristics

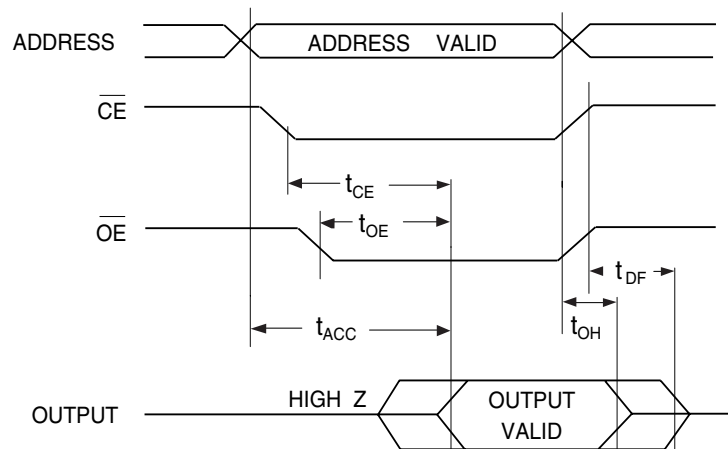
| Symbol | Parameter | Condition | Min | Max | Units |
|--------------------------------|--------------------------------------|--|-----|------|-------|
| I _{LI} | Input Load Current | V _{IN} = 0V to V _{CC} | | 10 | μA |
| I _{LO} | Output Leakage Current | V _{I/O} = 0V to V _{CC} | | 10 | μA |
| I _{SB1} | V _{CC} Standby Current CMOS | $\overline{CE} = V_{CC} - 0.3V$ to V _{CC} | | 50 | μA |
| I _{SB2} | V _{CC} Standby Current TTL | $\overline{CE} = 2.0V$ to V _{CC} | | 1 | mA |
| I _{CC} ⁽¹⁾ | V _{CC} Active Current | f = 5 MHz; I _{OUT} = 0 mA | | 15 | mA |
| V _{IL} | Input Low Voltage | | | 0.6 | V |
| V _{IH} | Input High Voltage | | 2.0 | | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1 mA | | 0.45 | V |
| V _{OH} | Output High Voltage | I _{OH} = -400 μA | 2.4 | | V |

- Note: 1. In the erase mode, I_{CC} is 50 mA.

10. AC Read Characteristics

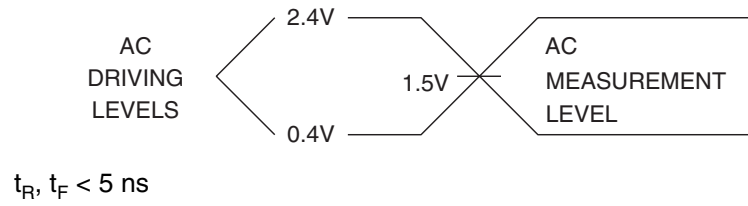
| Symbol | Parameter | AT49BV001A(N)(T)-55 | | Units |
|-------------------|---|---------------------|-----|-------|
| | | Min | Max | |
| t_{ACC} | Address to Output Delay | | 55 | ns |
| $t_{CE}^{(1)}$ | \overline{CE} to Output Delay | | 55 | ns |
| $t_{OE}^{(2)}$ | \overline{OE} to Output Delay | 0 | 30 | ns |
| $t_{DF}^{(3)(4)}$ | \overline{CE} or \overline{OE} to Output Float | 0 | 25 | ns |
| t_{OH} | Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first | 0 | | ns |

11. AC Read Waveforms ⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾

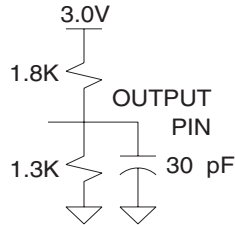


- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} whichever occurs first (CL = 5 pF).
 - This parameter is characterized and is not 100% tested.

12. Input Test Waveform and Measurement Level



13. Output Load Test



14. Pin Capacitance

$f = 1 \text{ MHz}, T = 25^\circ\text{C}^{(1)}$

| Symbol | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 4 | 6 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 8 | 12 | pF | $V_{OUT} = 0V$ |

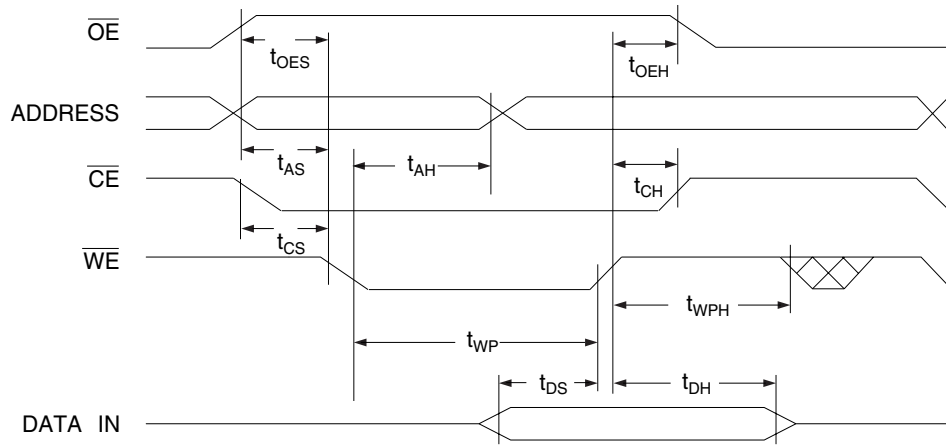
Note: 1. This parameter is characterized and is not 100% tested.

15. AC Byte Load Characteristics

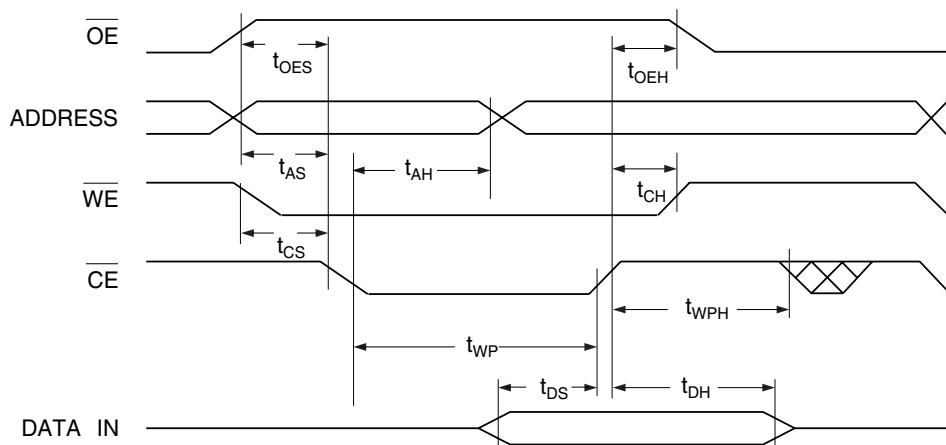
| Symbol | Parameter | Min | Max | Units |
|-------------------|--|-----|-----|-------|
| t_{AS}, t_{OES} | Address, \overline{OE} Set-up Time | 0 | | ns |
| t_{AH} | Address Hold Time | 40 | | ns |
| t_{CS} | Chip Select Set-up Time | 0 | | ns |
| t_{CH} | Chip Select Hold Time | 0 | | ns |
| t_{WP} | Write Pulse Width (\overline{WE} or \overline{CE}) | 30 | | ns |
| t_{DS} | Data Set-up Time | 40 | | ns |
| t_{DH}, t_{OEH} | Data, \overline{OE} Hold Time | 0 | | ns |
| t_{WPH} | Write Pulse Width High | 30 | | ns |

16. AC Byte Load Waveforms

16.1 \overline{WE} Controlled



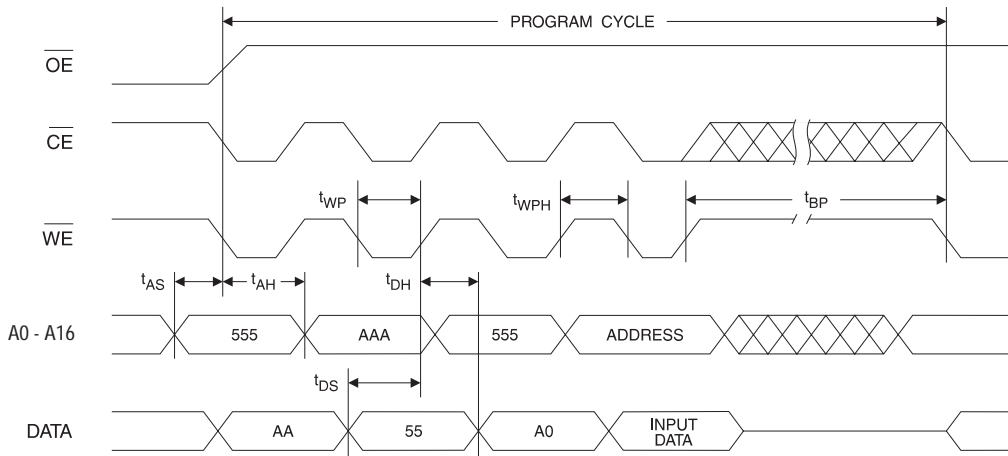
16.2 \overline{CE} Controlled



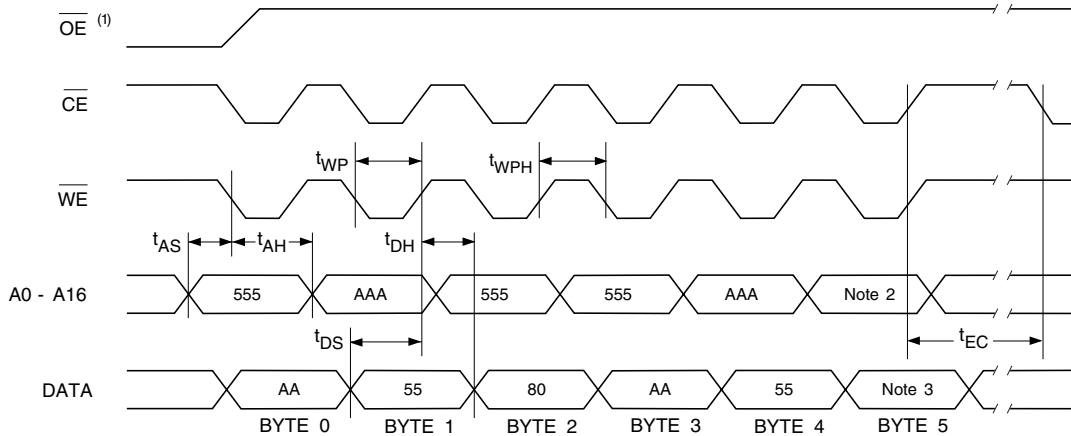
17. Program Cycle Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|------------------------|-----|-----|-----|---------|
| t_{BP} | Byte Programming Time | | 30 | 50 | μ s |
| t_{AS} | Address Set-up Time | 0 | | | ns |
| t_{AH} | Address Hold Time | 40 | | | ns |
| t_{DS} | Data Set-up Time | 40 | | | ns |
| t_{DH} | Data Hold Time | 0 | | | ns |
| t_{WP} | Write Pulse Width | 30 | | | ns |
| t_{WPH} | Write Pulse Width High | 30 | | | ns |
| t_{EC} | Erase Cycle Time | | 3 | 5 | seconds |

18. Program Cycle Waveforms



19. Sector or Chip Erase Cycle Waveforms



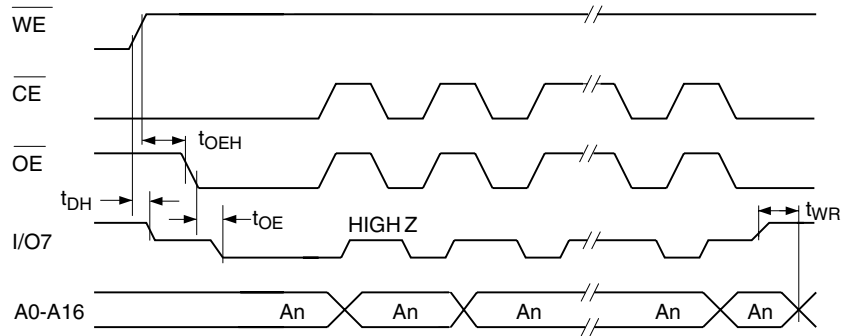
- Notes:
- \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.
 - For chip erase, the address should be 555. For sector erase, the address depends on what sector is to be erased. (See note 4 under "Command Definition Table" on page 6.)
 - For chip erase, the data should be 10H, and for sector erase, the data should be 30H.

20. Data Polling Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|--|-----|-----|-----|-------|
| t_{DH} | Data Hold Time | 10 | | | ns |
| $t_{OE\overline{H}}$ | \overline{OE} Hold Time | 10 | | | ns |
| t_{OE} | \overline{OE} to Output Delay ⁽²⁾ | | | | ns |
| t_{WR} | Write Recovery Time | 0 | | | ns |

Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 8.

21. Data Polling Waveforms

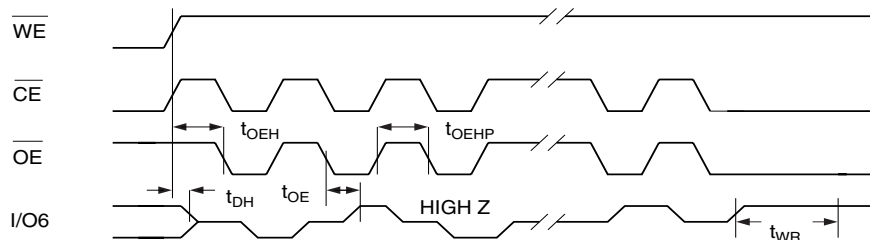


22. Toggle Bit Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|--|-----|-----|-----|-------|
| t_{DH} | Data Hold Time | 10 | | | ns |
| $t_{OE\overline{H}}$ | \overline{OE} Hold Time | 10 | | | ns |
| t_{OE} | \overline{OE} to Output Delay ⁽²⁾ | | | | ns |
| t_{OEHP} | \overline{OE} High Pulse | 50 | | | ns |
| t_{WR} | Write Recovery Time | 0 | | | ns |

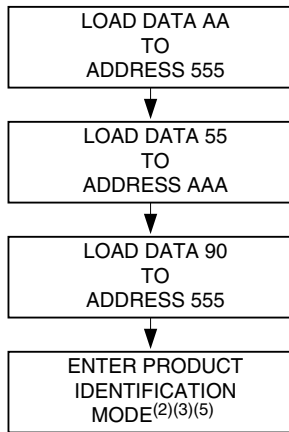
Notes: 1. These parameters are characterized and not 100% tested.
2. See t_{OE} spec in "AC Read Characteristics" on page 8s.

23. Toggle Bit Waveforms⁽¹⁾⁽²⁾⁽³⁾

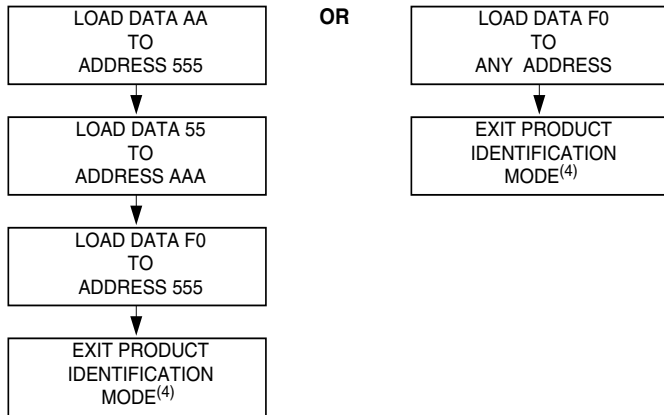


Notes: 1. Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit.
The t_{OEHP} specification must be met by the toggling input(s).
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

24. Software Product Identification Entry⁽¹⁾

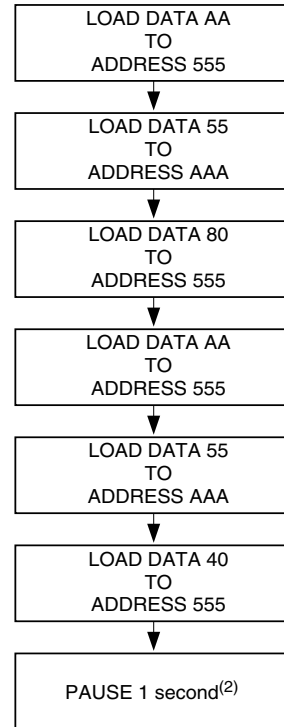


25. Software Product Identification Exit⁽¹⁾



- Notes:
1. Data Format: I/O7 - I/O0 (Hex);
Address Format: A14 - A0 (Hex).
 2. A1 - A16 = V_{IL} .
Manufacture Code is read for A0 = V_{IL} ;
Device Code is read for A0 = V_{IH} .
Additional Device Code is read for address 0003H
 3. The device does not remain in identification mode if powered down.
 4. The device returns to standard operation mode.
 5. Manufacturer Code: 1FH
Device Code: 05H – AT49BV001A(N)
04H – AT49BV001A(N)T
Additional Device Code: 0FH – AT49BV001A(N)(T)

26. Boot Block Lockout Feature Enable Algorithm⁽¹⁾



- Notes:
1. Data Format: I/O7 - I/O0 (Hex);
Address Format: A14 - A0 (Hex).
 2. Boot block lockout feature enabled.

27. Ordering Information

27.1 Standard Package

| t_{ACC} (ns) | I_{CC} (mA) | | Ordering Code | Package | Operation Range |
|-------------------|---------------|---------|-------------------|---------|------------------------------|
| | Active | Standby | | | |
| 55 | 15 | 0.05 | AT49BV001A-55JI | 32J | Industrial (-40° to 85°C) |
| | | | AT49BV001A-55TI | 32T | |
| | | | AT49BV001A-55VI | 32V | |
| | | | AT49BV001AN-55JI | 32J | Industrial (-40° to 85°C) |
| | | | AT49BV001AN-55TI | 32T | |
| | | | AT49BV001AN-55VI | 32V | |
| | | | AT49BV001AT-55JI | 32J | Industrial (-40° to 85°C) |
| | | | AT49BV001AT-55TI | 32T | |
| | | | AT49BV001AT-55VI | 32V | |
| | | | AT49BV001ANT-55JI | 32J | Industrial (-40° to 85°C) |
| | | | AT49BV001ANT-55TI | 32T | |
| | | | AT49BV001ANT-55VI | 32V | |

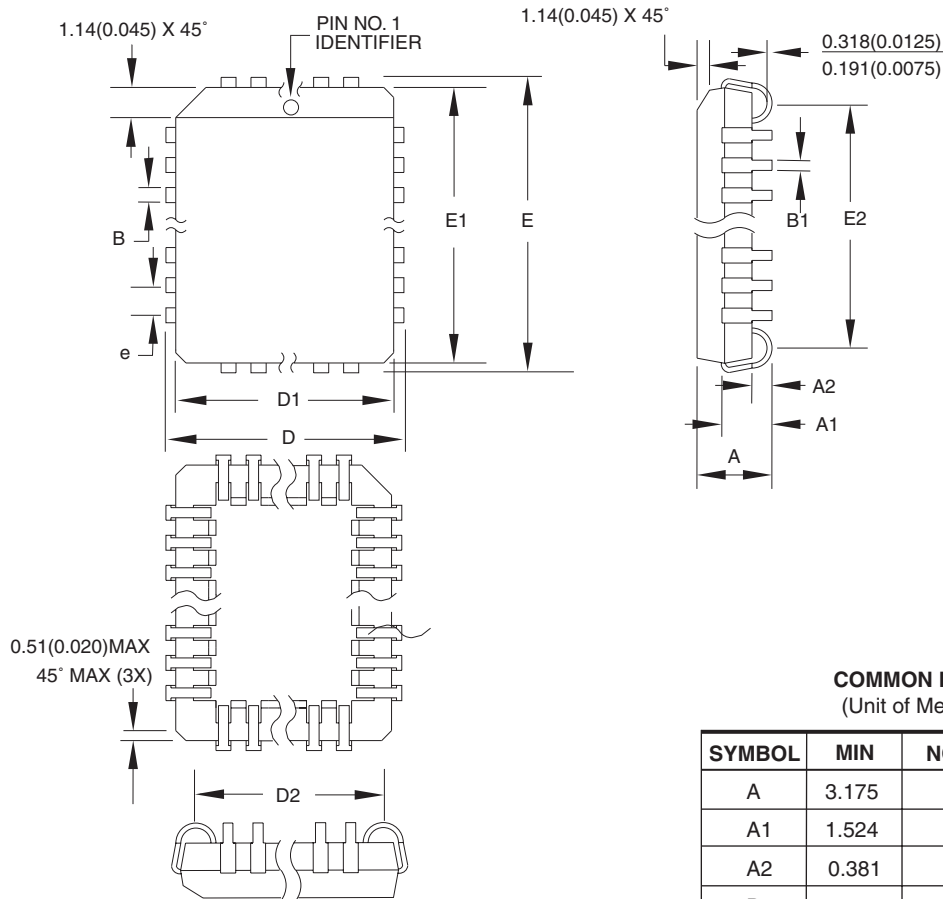
27.2 Green Package Option (Pb/Halide-free)

| t_{ACC} (ns) | I_{CC} (mA) | | Ordering Code | Package | Operation Range |
|-------------------|---------------|---------|-------------------|---------|------------------------------|
| | Active | Standby | | | |
| 55 | 15 | 0.05 | AT49BV001AN-55TU | 32T | Industrial (-40° to 85°C) |
| | | | AT49BV001AN-55VU | 32V | |
| | | | AT49BV001ANT-55JU | 32J | Industrial (-40° to 85°C) |
| | | | AT49BV001ANT-55TU | 32T | |
| | | | AT49BV001ANT-55VU | 32V | |

| Package Type | |
|--------------|--|
| 32J | 32-Lead, Plastic, J-Leaded Chip Carrier Package (PLCC) |
| 32T | 32-Lead, Thin Small Outline Package (TSOP) |
| 32V | 32-Lead, Thin Small Outline Package (VSOP) (8 x 14 mm) |

28. Packaging Information

28.1 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | 3.175 | - | 3.556 | |
| A1 | 1.524 | - | 2.413 | |
| A2 | 0.381 | - | - | |
| D | 12.319 | - | 12.573 | |
| D1 | 11.354 | - | 11.506 | Note 2 |
| D2 | 9.906 | - | 10.922 | |
| E | 14.859 | - | 15.113 | |
| E1 | 13.894 | - | 14.046 | Note 2 |
| E2 | 12.471 | - | 13.487 | |
| B | 0.660 | - | 0.813 | |
| B1 | 0.330 | - | 0.533 | |
| e | 1.270 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32J, 32-lead, Plastic J-leaded Chip Carrier (PLCC)

DRAWING NO.

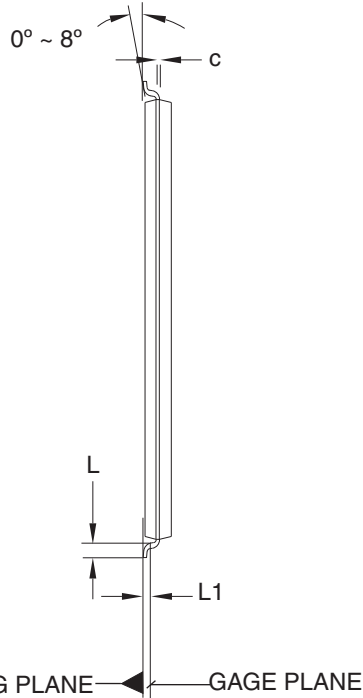
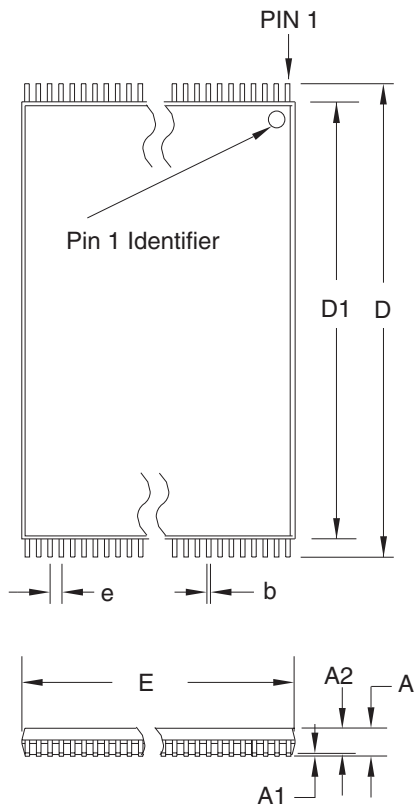
32J

REV.

B



28.2 32T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------------|-------|-------|--------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 19.80 | 20.00 | 20.20 | |
| D1 | 18.30 | 18.40 | 18.50 | Note 2 |
| E | 7.90 | 8.00 | 8.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.50 BASIC | | | |

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation BD.
 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
 3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32T, 32-lead (8 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)

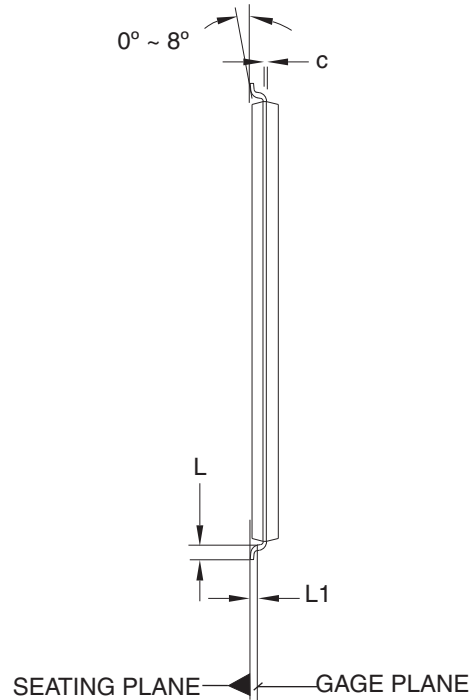
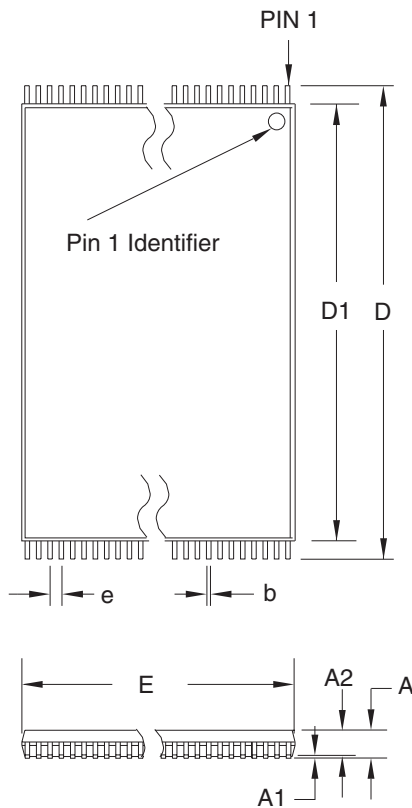
DRAWING NO.

32T

REV.

B

28.3 32V – VSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------------|-------|-------|--------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 13.80 | 14.00 | 14.20 | |
| D1 | 12.30 | 12.40 | 12.50 | Note 2 |
| E | 7.90 | 8.00 | 8.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.50 BASIC | | | |

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation BA.
 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
 3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

32V, 32-lead (8 x 14 mm Package) Plastic Thin Small Outline Package, Type I (VSOP)

DRAWING NO.

32V

REV.

B





Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenalux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/ High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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