THE DATASHEET OF

AT45DB642-TI

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64-megabit 2.7-volt Only Dual-interface DataFlash®

AT45DB642

Features

- Single 2.7V - 3.6V Supply
- Dual-interface Architecture
  - Dedicated Serial Interface (SPI Modes 0 and 3 Compatible)
  - Dedicated Parallel I/O Interface (Optional Use)
- Page Program Operation
  - Single Cycle Reprogram (Erase and Program)
  - 8192 Pages (1056 Bytes/Page) Main Memory
- Supports Page and Block Erase Operations
- Two 1056-byte SRAM Data Buffers – Allows Receiving of Data while Reprogramming the Flash Array
- Continuous Read Capability through Entire Array
  - Ideal for Code Shadowing Applications
- Low-power Dissipation
  - 4 mA Active Read Current Typical
  - 2 µA CMOS Standby Current Typical
- 20 MHz Maximum Clock Frequency – Serial Interface
- 5 MHz Maximum Clock Frequency – Parallel Interface
- Hardware Data Protection
- Commercial and Industrial Temperature Ranges

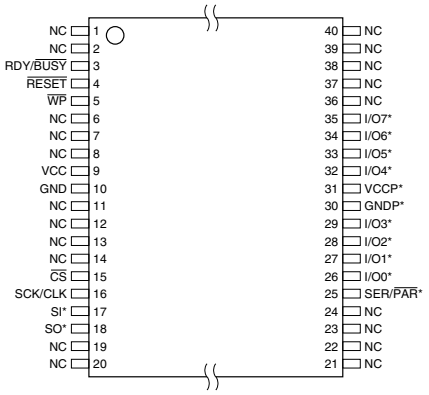
Description

The AT45DB642 is a 2.7-volt only, dual-interface Flash memory ideally suited for a wide variety of digital voice-, image-, program code- and data-storage applications. The dual-interface of the AT45DB642 allows a dedicated serial interface to be connected to a DSP and a dedicated parallel interface to be connected to a microcontroller or vice versa.

Pin Configurations

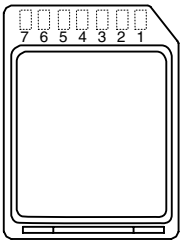
Pin Name	Function
$\overline{CS}$	Chip Select
SCK/CLK	Serial Clock/Clock
SI	Serial Input
SO	Serial Output
I/O7 - I/O0	Parallel Input/Output
$\overline{WP}$	Hardware Page Write Protect Pin
$\overline{RESET}$	Chip Reset
RDY/$\overline{BUSY}$	Ready/Busy
SER/$\overline{PAR}$	Serial/Parallel Interface Control

TSOP Top View
Type 1



Note: *Optional Use – See pin description text for connection information.

DataFlash Card(1)



Note: 1. See AT45DCB008 Datasheet.

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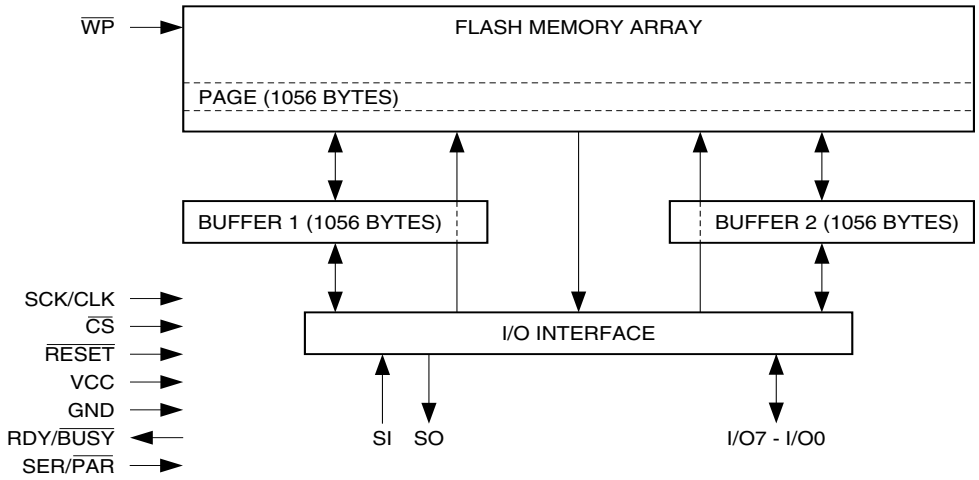
However, the use of either interface is purely optional. Its 69,206,016 bits of memory are organized as 8192 pages of 1056 bytes each. In addition to the main memory, the AT45DB642 also contains two SRAM data buffers of 1056 bytes each. The buffers allow receiving of data while a page in the main memory is being reprogrammed, as well as reading or writing a continuous data stream. EEPROM emulation (bit or byte alterability) is easily handled with a self-contained three step Read-Modify-Write operation. Unlike conventional Flash memories that are accessed randomly with multiple address lines and a parallel interface, the DataFlash® uses either a serial interface or a parallel interface to sequentially access its data. The simple sequential access facilitates hardware layout, increases system reliability, minimizes switching noise, and reduces package size and active pin count. DataFlash supports SPI mode 0 and mode 3. The device is optimized for use in many commercial and industrial applications where high-density, low-pin count, low-voltage, and low-power are essential. The device operates at clock frequencies up to 20 MHz with a typical active read current consumption of 4 mA.

To allow for simple in-system reprogrammability, the AT45DB642 does not require high input voltages for programming. The device operates from a single power supply, 2.7V to 3.6V, for both the program and read operations. The AT45DB642 is enabled through the chip select pin ($\overline{CS}$) and accessed via a three-wire interface consisting of the Serial Input (SI), Serial Output (SO), and the Serial Clock (SCK), or a parallel interface consisting of the parallel input/output pins (I/O7 - I/O0) and the clock pin (CLK). The SCK and CLK pins are shared and provide the same clocking input to the DataFlash.

All programming cycles are self-timed, and no separate erase cycle is required before programming.

When the device is shipped from Atmel, the most significant page of the memory array may not be erased. In other words, the contents of the last page may not be filled with FFH.

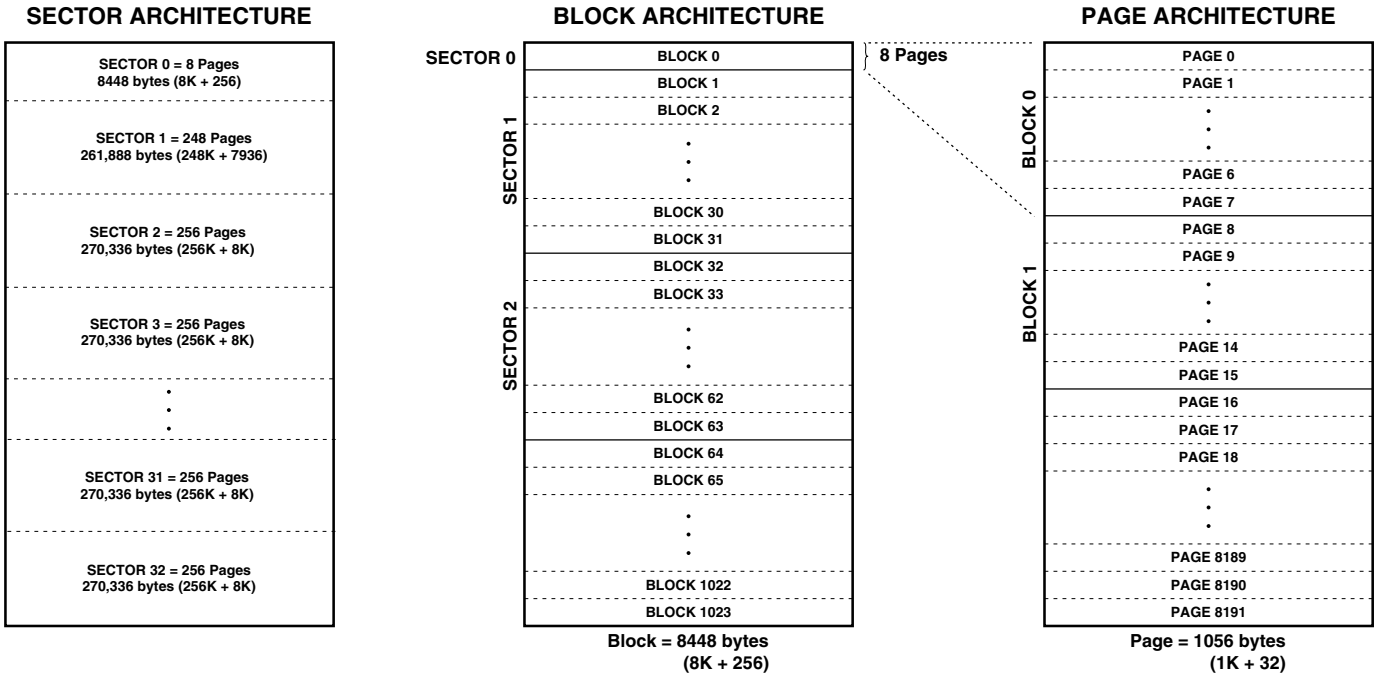
Block Diagram



Memory Array

To provide optimal flexibility, the memory array of the AT45DB642 is divided into three levels of granularity comprising of sectors, blocks and pages. The “Memory Architecture Diagram” illustrates the breakdown of each level and details the number of pages per sector and block. All program operations to the DataFlash occur on a page-by-page basis; however, the optional erase operations can be performed at the block or page level.

Memory Architecture Diagram



Device Operation

The device operation is controlled by instructions from the host processor. The list of instructions and their associated opcodes are contained in Tables 1 through 4. A valid instruction starts with the falling edge of $\overline{CS}$ followed by the appropriate 8-bit opcode and the desired buffer or main memory address location. While the $\overline{CS}$ pin is low, toggling the SCK/CLK pin controls the loading of the opcode and the desired buffer or main memory address location through either the SI (serial input) pin or the parallel input pins (I/O7 - I/O0). All instructions, addresses, and data are transferred with the most significant bit (MSB) first.

Buffer addressing is referenced in the datasheet using the terminology BFA10 - BFA0 to denote the 11 address bits required to designate a byte address within a buffer. Main memory addressing is referenced using the terminology PA12 - PA0 and BA10 - BA0, where PA12 - PA0 denotes the 13 address bits required to designate a page address and BA10 - BA0 denotes the 11 address bits required to designate a byte address within the page.

Read Commands

By specifying the appropriate opcode, data can be read from the main memory or from either one of the two SRAM data buffers. The DataFlash supports two categories of read modes in relation to the SCK/CLK signal. The differences between the modes are in respect to the inactive state of the SCK/CLK signal as well as which clock cycle data will begin to be output. The two categories, which are comprised of four modes total, are defined as Inactive Clock Polarity Low or Inactive Clock Polarity High and SPI Mode 0 or SPI Mode 3. A separate opcode (refer to Table 1 for a complete list) is used to select which category will be used for reading. Please refer to the “Detailed Bit-level Read Timing” diagrams in this datasheet for details on the clock cycle sequences for each mode.

CONTINUOUS ARRAY READ: By supplying an initial starting address for the main memory array, the Continuous Array Read command can be utilized to sequentially read a continuous stream of data from the device by simply providing a clock signal; no additional addressing information or control signals need to be provided. The DataFlash incorporates an internal address counter that will automatically increment on every clock cycle, allowing one continuous read operation without the need of additional address sequences. To perform a continuous read, an opcode of 68H or E8H must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence) and a series of don't care bytes (four don't care bytes if using the serial interface or 60 don't care bytes if using the parallel interface). The first 13 bits (PA12 - PA0) of the 24-bit (three byte) address sequence specify which page of the main memory array to read, and the last 11 bits (BA10 - BA0) of the 24-bit address sequence specify the starting byte address within the page. The four or 60 don't care bytes that follow the three address bytes are needed to initialize the read operation. Following the don't care bytes, additional clock pulses on the SCK/CLK pin will result in data being output on either the SO (serial output) pin or the parallel output pins (I/O7-I/O0).

The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. When the end of a page in main memory is reached during a Continuous Array Read, the device will continue reading at the beginning of the next page with no delays incurred during the page boundary crossover (the crossover from the end of one page to the beginning of the next page). When the last bit (or byte if using the parallel interface mode) in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. As with crossing over page boundaries, no delays will be incurred when wrapping around from the end of the array to the beginning of the array.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins (SO or I/O7-I/O0). The maximum SCK/CLK frequency allowable for the Continuous Array Read is defined by the f_{CAR} specification. The Continuous Array Read bypasses both data buffers and leaves the contents of the buffers unchanged.

BURST ARRAY READ WITH SYNCHRONOUS DELAY: The Burst Array Read with Synchronous Delay functions very similarly to the Continuous Array Read operation but allows much higher read throughputs by utilizing faster clock frequencies. It incorporates a synchronous delay (through the use of don't care clock cycles) when crossing over page boundaries. To perform a Burst Array Read with Synchronous Delay, an opcode of 69H or E9H must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence) and a series of don't care bytes (four don't care bytes if using the serial interface or 60 don't care bytes if using the parallel interface). The first 13 bits (PA12-PA0) of the 24-bit (three byte) address sequence specify which page of the main memory array to read, and the last 11 bits (BA10-BA0) of the 24-bit address sequence specify the starting byte address within the page. The don't care bytes that follow the three address bytes are needed to initialize the read operation. Following the don't care bytes, additional clock pulses on the SCK/CLK pin will result in data being output on either the SO pin or the I/O7-I/O0 pins.

As with the Continuous Array Read, the $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don't care bytes, and the reading of data. During a Burst Array Read with Synchronous Delay, when the end of a page in main memory is reached (the last bit or the last byte of the page has been clocked out), the system must send an additional 32 don't care clock cycles before the first bit (or byte if using the parallel interface mode) of the next page can be read out. These 32 don't care clock cycles are necessary to allow the device enough time to cross over the burst read boundary (the crossover from the end of one page to the beginning of the next page). By utilizing the 32 don't care clock cycles, the system does not need to delay the SCK/CLK signal to the device which allows synchronous operation when reading multiple pages of the memory array. Please see the detailed read timing waveforms for illustrations (beginning on page 21) on which clock cycle data will actually begin to be output.

When the last bit (or byte in the parallel interface mode) in the main memory array has been read, the device will continue reading back at the beginning of the first page of memory. The transition from the last bit (or byte when using the parallel interface) of the array back to the beginning of the array is also considered a burst read boundary. Therefore, the system must send 32 don't care clock cycles before the first bit (or byte if using the parallel interface mode) of the memory array can be read.

A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins (SO or I/O7-I/O0). The maximum SCK/CLK frequency allowable for the Burst Array Read with Synchronous Delay is defined by the f_{BARSD} specification. The Burst Array Read with Synchronous Delay bypasses both data buffers and leaves the contents of the buffers unchanged.

MAIN MEMORY PAGE READ: A main memory page read allows the user to read data directly from any one of the 8192 pages in the main memory, bypassing both of the data buffers and leaving the contents of the buffers unchanged. To start a page read, an opcode of 52H or D2H must be clocked into the device followed by three address bytes (which comprise the 24-bit page and byte address sequence) and a series of don’t care bytes (four don’t care bytes if using the serial interface or 60 don’t care bytes if the using parallel interface). The first 13 bits (PA12 - PA0) of the 24-bit (three-byte) address sequence specify the page in main memory to be read, and the last 11 bits (BA10 - BA0) of the 24-bit address sequence specify the starting byte address within that page. The four or 60 don’t care bytes that follow the three address bytes are sent to initialize the read operation. Following the don’t care bytes, additional pulses on SCK/CLK result in data being output on either the SO (serial output) pin or the parallel output pins (I/O7 - I/O0). The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don’t care bytes, and the reading of data. When the end of a page in main memory is reached, the device will continue reading back at the beginning of the same page. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins (SO or I/O7 - I/O0).

BUFFER READ: Data can be read from either one of the two buffers, using different opcodes to specify which buffer to read from. An opcode of 54H or D4H is used to read data from buffer 1, and an opcode of 56H or D6H is used to read data from buffer 2. To perform a buffer read, the opcode must be clocked into the device followed by three address bytes comprised of 13 don’t care bits and 11 buffer address bits (BFA10 - BFA0). Following the three address bytes, an additional don’t care byte must be clocked in to initialize the read operation. Since the buffer size is 1056 bytes, 11 buffer address bits are required to specify the first byte of data to be read from the buffer. The $\overline{CS}$ pin must remain low during the loading of the opcode, the address bytes, the don’t care bytes, and the reading of data. When the end of a buffer is reached, the device will continue reading back at the beginning of the buffer. A low-to-high transition on the $\overline{CS}$ pin will terminate the read operation and tri-state the output pins (SO or I/O7 - I/O0).

STATUS REGISTER READ: The status register can be used to determine the device's ready/busy status, the result of a Main Memory Page to Buffer Compare operation, or the device density. To read the status register, an opcode of 57H or D7H must be loaded into the device. After the opcode is clocked in, the 1-byte status register will be clocked out on the output pins (SO or I/O7 - I/O0), starting with the next clock cycle. When using the serial interface, the data in the status register, starting with the MSB (bit 7), will be clocked out on the SO pin during the next eight clock cycles.

The five most-significant bits of the status register will contain device information, while the remaining three least-significant bits are reserved for future use and will have undefined values. After the one byte of the status register has been clocked out, the sequence will repeat itself (as long as $\overline{CS}$ remains low and SCK/CLK is being toggled). The data in the status register is constantly updated, so each repeating sequence will output new data.

Ready/busy status is indicated using bit 7 of the status register. If bit 7 is a 1, then the device is not busy and is ready to accept the next command. If bit 7 is a 0, then the device is in a busy state. The user can continuously poll bit 7 of the status register by stopping SCK/CLK at a low level once bit 7 has been output on the SO or I/O7 pin. The status of bit 7 will continue to be output on the SO or I/O7 pin, and once the device is no longer busy, the state of the SO or I/O7 pin will change from 0 to 1. There are eight operations that can cause the device to be in a busy state: Main Memory Page to Buffer Transfer, Main Memory Page to Buffer Compare, Buffer to Main Memory Page Program with Built-in Erase, Buffer to Main Memory Page Program without Built-in Erase, Page Erase, Block Erase, Main Memory Page Program, and Auto Page Rewrite.

The result of the most recent Main Memory Page to Buffer Compare operation is indicated using bit 6 of the status register. If bit 6 is a 0, then the data in the main memory page matches the data in the buffer. If bit 6 is a 1, then at least one bit of the data in the main memory page does not match the data in the buffer.

The device density is indicated using bits 5, 4, 3 and 2 of the status register. For the AT45DB642, the four bits are logical "1"s. The decimal value of these four binary bits does not equate to the device density; the four bits represent a combinational code relating to differing densities of DataFlash devices, allowing a total of sixteen different density configurations.

Status Register Format

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RDY/$\overline{BUSY}$	COMP	1	1	1	1	X	X

Program and Erase Commands

BUFFER WRITE: Data can be clocked in from the input pins (SI or I/O7 - I/O0) into either buffer 1 or buffer 2. To load data into either buffer, a 1-byte opcode, 84H for buffer 1 or 87H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 13 don't care bits and 11 buffer address bits (BFA10 - BFA0). The 11 buffer address bits specify the first byte in the buffer to be written. After the last address byte has been clocked into the device, data can then be clocked in on subsequent clock cycles. If the end of the data buffer is reached, the device will wrap around back to the beginning of the buffer. Data will continue to be loaded into the buffer until a low-to-high transition is detected on the $\overline{CS}$ pin.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITH BUILT-IN ERASE: Data written into either buffer 1 or buffer 2 can be programmed into the main memory. A 1-byte opcode, 83H for buffer 1 or 86H for buffer 2, must be clocked into the device followed by three address bytes consisting of 13 page address bits (PA12 - PA0) that specify the page in the main memory to be written and 11 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first erase the selected page in main memory (the erased state is a logical 1) and then program the data stored in the buffer into the specified page in main memory. Both the erase and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

BUFFER TO MAIN MEMORY PAGE PROGRAM WITHOUT BUILT-IN ERASE: A previously-erased page within main memory can be programmed with the contents of either buffer 1 or buffer 2. A 1-byte opcode, 88H for buffer 1 or 89H for buffer 2, must be clocked into the device followed by three address bytes consisting of 13 page address bits (PA12 - PA0) that specify the page in the main memory to be written and 11 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will program the data stored in the buffer into the specified page in the main memory. It is necessary that the page in main memory that is being programmed has been previously erased using one of the optional erase commands (Page Erase or Block Erase). The programming of the page is internally self-timed and should take place in a maximum time of t_P. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

Successive page programming operations, without doing a page erase, are not recommended. In other words, changing bytes within a page from a "1" to a "0" during multiple page programming operations without erasing that page is not recommended.

PAGE ERASE: The optional Page Erase command can be used to individually erase any page in the main memory array allowing the Buffer to Main Memory Page Program without Built-in Erase command to be utilized at a later time. To perform a page erase, an opcode of 81H must be loaded into the device, followed by three address bytes comprised of 13 page address bits (PA12 - PA0) and 11 don't care bits. The 13 page address bits are used to specify which page of the memory array is to be erased. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected page (the erased state is a logical 1). The erase operation is internally self-timed and should take place in a maximum time of t_{PE}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

BLOCK ERASE: A block of eight pages can be erased at one time allowing the Buffer to Main Memory Page Program without Built-in Erase command to be utilized to reduce programming times when writing large amounts of data to the device. To perform a block erase, an opcode of 50H must be loaded into the device, followed by three address bytes comprised of 10 page address bits (PA12 -PA3) and 14 don't care bits. The 10 page address bits are used to specify which block of eight pages is to be erased. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will erase the selected block of eight pages. The erase operation is internally self-timed and should take place in a maximum time of t_{BE}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

Block Erase Addressing

PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	Block
0	0	0	0	0	0	0	0	0	0	X	X	X	0
0	0	0	0	0	0	0	0	0	1	X	X	X	1
0	0	0	0	0	0	0	0	1	0	X	X	X	2
0	0	0	0	0	0	0	0	1	1	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	0	0	X	X	X	1020
1	1	1	1	1	1	1	1	0	1	X	X	X	1021
1	1	1	1	1	1	1	1	1	0	X	X	X	1022
1	1	1	1	1	1	1	1	1	1	X	X	X	1023

MAIN MEMORY PAGE PROGRAM THROUGH BUFFER: This operation is a combination of the Buffer Write and Buffer to Main Memory Page Program with Built-in Erase operations. Data is first clocked into buffer 1 or buffer 2 from the input pins (SI or I/O7 - I/O0) and then programmed into a specified page in the main memory. A 1-byte opcode, 82H for buffer 1 or 85H for buffer 2, must first be clocked into the device, followed by three address bytes. The address bytes are comprised of 13 page address bits (PA12 - PA0) that select the page in the main memory where data is to be written, and 11 buffer address bits (BFA10 - BFA0) that select the first byte in the buffer to be written. After all address bytes are clocked in, the part will take data from the input pins and store it in the specified data buffer. If the end of the buffer is reached, the device will wrap around back to the beginning of the buffer. When there is a low-to-high transition on the $\overline{CS}$ pin, the part will first erase the selected page in main memory to all 1s and then program the data stored in the buffer into that memory page. Both the erase and the programming of the page are internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

Additional Commands

MAIN MEMORY PAGE TO BUFFER TRANSFER: A page of data can be transferred from the main memory to either buffer 1 or buffer 2. To start the operation, a 1-byte opcode, 53H for buffer 1 and 55H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 13 page address bits (PA12 - PA0), which specify the page in main memory that is to be transferred, and 11 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK/CLK pin to load the opcode and the address bytes from the input pins (SI or I/O7 - I/O0). The transfer of the page of data from the main memory to the buffer will begin when the $\overline{CS}$ pin transitions from a low to a high state. During the transfer of a page of data (t_{XFR}), the status register can be read or the RDY/$\overline{BUSY}$ can be monitored to determine whether the transfer has been completed.

MAIN MEMORY PAGE TO BUFFER COMPARE: A page of data in main memory can be compared to the data in buffer 1 or buffer 2. To initiate the operation, a 1-byte opcode, 60H for buffer 1 and 61H for buffer 2, must be clocked into the device, followed by three address bytes consisting of 13 page address bits (PA12 - PA0) that specify the page in the main memory that is to be compared to the buffer, and 11 don't care bits. The $\overline{CS}$ pin must be low while toggling the SCK/CLK pin to load the opcode and the address bytes from the input pins (SI or I/O7 - I/O0). On the low-to-high transition of the $\overline{CS}$ pin, the 1056 bytes in the selected main memory page will be compared with the 1056 bytes in buffer 1 or buffer 2. During this time (t_{XFR}), the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy. On completion of the compare operation, bit 6 of the status register is updated with the result of the compare.

AUTO PAGE REWRITE: This mode is only needed if multiple bytes within a page or multiple pages of data are modified in a random fashion. This mode is a combination of two operations: Main Memory Page to Buffer Transfer and Buffer to Main Memory Page Program with Built-in Erase. A page of data is first transferred from the main memory to buffer 1 or buffer 2, and then the same data (from buffer 1 or buffer 2) is programmed back into its original page of main memory. To start the rewrite operation, a 1-byte opcode, 58H for buffer 1 or 59H for buffer 2, must be clocked into the device, followed by three address bytes comprised of 13 page address bits (PA12 - PA0) that specify the page in main memory to be rewritten and 11 don't care bits. When a low-to-high transition occurs on the $\overline{CS}$ pin, the part will first transfer data from the page in main memory to a buffer and then program the data from the buffer back into same page of main memory. The operation is internally self-timed and should take place in a maximum time of t_{EP}. During this time, the status register and the RDY/$\overline{BUSY}$ pin will indicate that the part is busy.

If a sector is programmed or reprogrammed sequentially page by page, then the programming algorithm shown in Figure 1 (page 33) is recommended. Otherwise, if multiple bytes in a page or several pages are programmed randomly in a sector, then the programming algorithm shown in Figure 2 (page 34) is recommended. Each page within a sector must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations in that sector.

Operation Mode Summary

The modes described can be separated into two groups – modes that make use of the Flash memory array (Group A) and modes that do not make use of the Flash memory array (Group B).

Group A modes consist of:

1. Main Memory Page to Buffer 1 (or 2) Transfer
2. Main Memory Page to Buffer 1 (or 2) Compare
3. Buffer 1 (or 2) to Main Memory Page Program with Built-in Erase
4. Buffer 1 (or 2) to Main Memory Page Program without Built-in Erase
5. Page Erase
6. Block Erase
7. Main Memory Page Program through Buffer
8. Auto Page Rewrite
9. Group B modes consist of:
10. Buffer 1 (or 2) Read
11. Buffer 1 (or 2) Write
12. Status Register Read

If a Group A mode is in progress (not fully completed), then another mode in Group A should not be started. However, during this time in which a Group A mode is in progress, modes in Group B can be started.

This gives the DataFlash the ability to virtually accommodate a continuous data stream. While data is being programmed into main memory from buffer 1, data can be loaded into buffer 2 (or vice versa). See application note AN-4 ("Using Atmel's Serial DataFlash") for more details.

Pin Descriptions

SERIAL/PARALLEL INTERFACE CONTROL (SER/$\overline{\text{PAR}}$): The DataFlash may be configured to utilize either its serial port or parallel port through the use of the serial/parallel control pin (SER/$\overline{\text{PAR}}$). The Dual Interface offers more flexibility in a system design with both the serial and parallel modes offered on the same device. When the SER/$\overline{\text{PAR}}$ pin is held high, the serial port (SI and SO) of the DataFlash will be used for all data transfers, and the parallel port (I/O7 - I/O0) will be in a high impedance state. Any data presented on the parallel port while SER/$\overline{\text{PAR}}$ is held high will be ignored. When the SER/$\overline{\text{PAR}}$ is held low, the parallel port will be used for all data transfers, and the SO pin of the serial port will be in a high impedance state. While SER/$\overline{\text{PAR}}$ is low, any data presented on the SI pin will be ignored. Switching between the serial port and parallel port can be done at anytime provided the following conditions are met: 1) $\overline{\text{CS}}$ should be held high during the switching between the two modes. 2) T_{SPH} (SER/$\overline{\text{PAR}}$ hold time) and T_{SPS} (SER/$\overline{\text{PAR}}$ Setup time) requirements should be followed.

Having both a serial port and a parallel port on the DataFlash allows the device to reside on two buses that can be connected to different processors. The advantage of switching between the serial and parallel port is that while an internally self-timed operation such as an erase or program operation is started with either port, a simultaneous operation such as a buffer read or buffer write can be started utilizing the other port.

The SER/$\overline{\text{PAR}}$ pin is internally pulled high; therefore, if the parallel port is never to be used, then connection of the SER/$\overline{\text{PAR}}$ pin is not necessary. In addition, if the SER/$\overline{\text{PAR}}$ pin is not connected or if the SER/$\overline{\text{PAR}}$ pin is always driven high externally, then the parallel input/output pins (I/O7-I/O0), the VCCP pin, and the GNDP pin should be treated as "don't connects."

SERIAL INPUT (SI): The SI pin is an input-only pin and is used to shift data serially into the device. The SI pin is used for all data input, including opcodes and address sequences. If the SER/$\overline{\text{PAR}}$ pin is always driven low, then the SI pin should be a "don't connect".

SERIAL OUTPUT (SO): The SO pin is an output-only pin and is used to shift data serially out from the device. If the SER/$\overline{\text{PAR}}$ pin is always driven low, then the SO pin should be a "don't connect".

PARALLEL INPUT/OUTPUT (I/O7-I/O0): The I/O7-I/O0 pins are bidirectional and used to clock data into and out of the device. The I/O7-I/O0 pins are used for all data input, including opcodes and address sequences. The use of these pins is optional, and the pins should be treated as "don't connects" if the SER/$\overline{\text{PAR}}$ pin is not connected or if the SER/$\overline{\text{PAR}}$ pin is always driven high externally.

SERIAL CLOCK/CLOCK (SCK/CLK): The SCK/CLK pin is an input-only pin and is used to control the flow of data to and from the DataFlash. Data is always clocked into the device on the rising edge of SCK/CLK and clocked out of the device on the falling edge of SCK/CLK.

CHIP SELECT ($\overline{\text{CS}}$): The DataFlash is selected when the $\overline{\text{CS}}$ pin is low. When the device is not selected, data will not be accepted on the input pins (SI or I/O7-I/O0), and the output pins (SO or I/O7-I/O0) will remain in a high impedance state. A high-to-low transition on the $\overline{\text{CS}}$ pin is required to start an operation, and a low-to-high transition on the $\overline{\text{CS}}$ pin is required to end an operation.

HARDWARE PAGE WRITE PROTECT: If the $\overline{\text{WP}}$ pin is held low, the first 256 pages (sectors 0 and 1) of the main memory cannot be reprogrammed. The only way to reprogram the first 256 pages is to first drive the protect pin high and then use the program commands previously mentioned. The $\overline{\text{WP}}$ pin is internally pulled high; therefore, in low pin count applications, connection of the $\overline{\text{WP}}$ pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the $\overline{\text{WP}}$ pin be driven high externally whenever possible.

RESET: A low state on the reset pin (RESET) will terminate the operation in progress and reset the internal state machine to an idle state. The device will remain in the reset condition as long as a low level is present on the RESET pin. Normal operation can resume once the RESET pin is brought back to a high level.

The device incorporates an internal power-on reset circuit, so there are no restrictions on the RESET pin during power-on sequences. The RESET pin is also internally pulled high; therefore, in low pin count applications, connection of the RESET pin is not necessary if this pin and feature will not be utilized. However, it is recommended that the RESET pin be driven high externally whenever possible.

READY/BUSY: This open drain output pin will be driven low when the device is busy in an internally self-timed operation. This pin, which is normally in a high state (through an external pull-up resistor), will be pulled low during programming/erase operations, compare operations, and page-to-buffer transfers.

The busy status indicates that the Flash memory array and one of the buffers cannot be accessed; read and write operations to the other buffer can still be performed.

PARALLEL PORT SUPPLY VOLTAGE (VCCP AND GNDP): The VCCP and GNDP pins are used to supply power for the parallel input/output pins (I/O7-I/O0). The VCCP and GNDP pins need to be used if the parallel port is to be utilized; however, these pins should be treated as "don't connects" if the SER/PAR pin is not connected or if the SER/PAR pin is always driven high externally.

Power-on/Reset State

When power is first applied to the device, or when recovering from a reset condition, the device will default to SPI Mode 3 or Inactive Clock Polarity High. In addition, the output pins (SO or I/O7 - I/O0) will be in a high impedance state, and a high-to-low transition on the CS pin will be required to start a valid instruction. The SPI mode or the clock polarity mode will be automatically selected on every falling edge of CS by sampling the inactive Clock State.

System Considerations

The SPI interface is controlled by the serial clock SCK, serial input SI and chip select CS pins. The sequential 8-bit parallel interface is controlled by the clock CLK, 8 I/Os and chip select CS pins. These signals must rise and fall monotonically and be free from noise. Excessive noise or ringing on these pins can be misinterpreted as multiple edges and cause improper operation of the device. The PC board traces must be kept to a minimum distance or appropriately terminated to ensure proper operation. If necessary, decoupling capacitors can be added on these pins to provide filtering against noise glitches.

As system complexity continues to increase, voltage regulation is becoming more important. A key element of any voltage regulation scheme is its current sourcing capability. Like all Flash memories, the peak current for DataFlash occur during the programming and erase operation. The regulator needs to supply this peak current requirement. An under specified regulator can cause current starvation. Besides increasing system noise, current starvation during programming or erase can lead to improper operation and possible data corruption.

Table 1. Read Commands

Command	SCK/CLK Mode	Opcode
Continuous Array Read	Inactive Clock Polarity Low or High	68H
	SPI Mode 0 or 3	E8H
Burst Array Read with Synchronous Delay	Inactive Clock Polarity Low or High	69H
	SPI Mode 0 or 3	E9H
Main Memory Page Read	Inactive Clock Polarity Low or High	52H
	SPI Mode 0 or 3	D2H
Buffer 1 Read	Inactive Clock Polarity Low or High	54H
	SPI Mode 0 or 3	D4H
Buffer 2 Read	Inactive Clock Polarity Low or High	56H
	SPI Mode 0 or 3	D6H
Status Register Read	Inactive Clock Polarity Low or High	57H
	SPI Mode 0 or 3	D7H

Table 2. Program and Erase Commands

Command	SCK/CLK Mode	Opcode
Buffer 1 Write	Any	84H
Buffer 2 Write	Any	87H
Buffer 1 to Main Memory Page Program with Built-in Erase	Any	83H
Buffer 2 to Main Memory Page Program with Built-in Erase	Any	86H
Buffer 1 to Main Memory Page Program without Built-in Erase	Any	88H
Buffer 2 to Main Memory Page Program without Built-in Erase	Any	89H
Page Erase	Any	81H
Block Erase	Any	50H
Main Memory Page Program Through Buffer 1	Any	82H
Main Memory Page Program Through Buffer 2	Any	85H

Table 3. Additional Commands

Command	SCK/CLK Mode	Opcode
Main Memory Page to Buffer 1 Transfer	Any	53H
Main Memory Page to Buffer 2 Transfer	Any	55H
Main Memory Page to Buffer 1 Compare	Any	60H
Main Memory Page to Buffer 2 Compare	Any	61H
Auto Page Rewrite Through Buffer 1	Any	58H
Auto Page Rewrite Through Buffer 2	Any	59H

Note: In Tables 2 and 3, an SCK/CLK mode designation of “Any” denotes any one of the four modes of operation (Inactive Clock Polarity Low, Inactive Clock Polarity High, SPI Mode 0, or SPI Mode 3).

Table 4. Detailed Bit-level Addressing Sequence

Opcode	Opcode	Address Byte								Address Byte								Address Byte								Additional Don't Care Bytes Required
		PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0	BA10	BA9	BA8	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0	
50H	0 1 0 1 0 0 0 0	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	x	x	x	N/A
52H	0 1 0 1 0 0 1 0	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	B	4 or 60 Bytes*
53H	0 1 0 1 0 0 1 1	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
54H	0 1 0 1 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	1 Byte
55H	0 1 0 1 0 1 0 1	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
56H	0 1 0 1 0 1 1 0	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	1 Byte
57H	0 1 0 1 0 1 1 1	N/A								N/A								N/A								N/A
58H	0 1 0 1 1 0 0 0	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
59H	0 1 0 1 1 0 0 1	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
60H	0 1 1 0 0 0 0 0	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
61H	0 1 1 0 0 0 0 1	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
68H	0 1 1 0 1 0 0 0	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	B	4 or 60 Bytes*
69H	0 1 1 0 1 0 0 1	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	B	4 or 60 Bytes*
81H	1 0 0 0 0 0 0 1	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
82H	1 0 0 0 0 0 1 0	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	B	N/A
83H	1 0 0 0 0 0 1 1	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
84H	1 0 0 0 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	N/A
85H	1 0 0 0 0 1 0 1	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	B	N/A
86H	1 0 0 0 0 1 1 0	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
87H	1 0 0 0 0 1 1 1	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	N/A
88H	1 0 0 0 1 0 0 0	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
89H	1 0 0 0 1 0 0 1	P	P	P	P	P	P	P	P	P	P	P	P	P	x	x	x	x	x	x	x	x	x	x	x	N/A
D2H	1 1 0 1 0 0 1 0	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	B	4 or 60 Bytes*
D4H	1 1 0 1 0 1 0 0	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	1 Byte
D6H	1 1 0 1 0 1 1 0	x	x	x	x	x	x	x	x	x	x	x	x	x	B	B	B	B	B	B	B	B	B	B	B	1 Byte
D7H	1 1 0 1 0 1 1 1	N/A								N/A								N/A								N/A
E8H	1 1 1 0 1 0 0 0	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	B	4 or 60 Bytes*
E9H	1 1 1 0 1 0 0 1	P	P	P	P	P	P	P	P	P	P	P	P	P	B	B	B	B	B	B	B	B	B	B	B	4 or 60 Bytes*

Note: P = Page Address Bit
B = Byte/Buffer Address Bit
x = Don't Care
* 4 Bytes for Serial Interface
60 Bytes for Parallel Interface

Absolute Maximum Ratings*

Temperature under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including NC Pins)
with Respect to Ground .....-0.6V to +6.25V

All Output Voltages
with Respect to Ground .....-0.6V to V_{CC} + 0.6V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC and AC Operating Range

		AT45DB642
Operating Temperature (Case)	Com.	0°C to 70°C
	Ind.	-40°C to 85°C
V_{CC} Power Supply(1)		2.7V to 3.6V

Note: 1. After power is applied and V_{CC} is at the minimum specified datasheet value, the system should wait 20 ms before an operational mode is started.

DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{SB}	Standby Current	$\overline{CS}$, $\overline{RESET}$, $\overline{WP}$ = V_{IH}, all inputs at CMOS levels		2	10	µA
I_{CC1}(1)	Active Current, Read Operation, Serial Interface	f = 20 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		4	10	mA
I_{CC2}(2)	Active Current, Read Operation, Parallel Interface	f = 5 MHz; I_{OUT} = 0 mA; V_{CC} = 3.6V		8	15	mA
I_{CC3}	Active Current, Program Operation, Page Program	V_{CC} = 3.6V		20	35	mA
I_{CC4}	Active Current, Program Operation, Fast Page Program	V_{CC} = 3.6V		30	50	mA
I_{CC5}	Active Current, Erase Operation, Page	V_{CC} = 3.6V		20	35	mA
I_{CC6}	Active Current, Erase Operation, Block	V_{CC} = 3.6V		20	35	mA
I_{LI}	Input Load Current	V_{IN} = CMOS levels			1	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = CMOS levels			1	µA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA; V_{CC} = 2.7V			0.4	V
V_{OH}	Output High Voltage	I_{OH} = -100 µA	V_{CC} - 0.2V			V

Notes: 1. I_{CC1} during a buffer read is 20 mA maximum.
2. I_{CC2} during a buffer read is 25 mA maximum.

AC Characteristics – Serial/Parallel Interface

Symbol	Parameter	Min	Max	Units
t_{SPH}	SER/$\overline{PAR}$ Hold Time	100		ns
t_{SPS}	SER/$\overline{PAR}$ Setup Time	100		ns

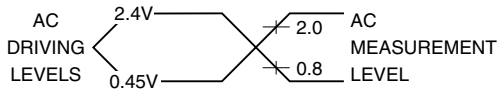
AC Characteristics – Serial Interface

Symbol	Parameter	Min	Max	Units
f_{SCK}	SCK Frequency		20	MHz
f_{CAR}	SCK Frequency for Continuous Array Read		15	MHz
f_{BARSD}	SCK Frequency for Burst Array Read with Synchronous Delay		20	MHz
t_{WH}	SCK High Time	22		ns
t_{WL}	SCK Low Time	22		ns
t_{CS}	Minimum $\overline{CS}$ High Time	250		ns
t_{CSS}	$\overline{CS}$ Setup Time	250		ns
t_{CSH}	$\overline{CS}$ Hold Time	250		ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low		150	ns
t_{SU}	Data In Setup Time	5		ns
t_{H}	Data In Hold Time	10		ns
t_{HO}	Output Hold Time	0		ns
t_{DIS}	Output Disable Time		18	ns
t_{V}	Output Valid		20	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		700	µs
t_{EP}	Page Erase and Programming Time		20	ms
t_{P}	Page Programming Time		14	ms
t_{PE}	Page Erase Time		8	ms
t_{BE}	Block Erase Time		12	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10		µs
t_{REC}	$\overline{RESET}$ Recovery Time		1	µs

AC Characteristics – Parallel Interface

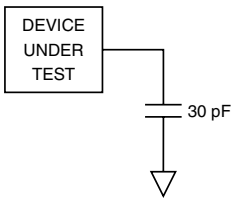
Symbol	Parameter	Min	Max	Units
f_{SCK1}	CLK Frequency		5	MHz
f_{CAR1}	CLK Frequency for Continuous Array Read		3	MHz
f_{BARSD1}	CLK Frequency for Burst Array Read with Synchronous Delay		5	MHz
t_{WH}	CLK High Time	80		ns
t_{WL}	CLK Low Time	80		ns
t_{CS}	Minimum $\overline{CS}$ High Time	250		ns
t_{CSS}	$\overline{CS}$ Setup Time	250		ns
t_{CSH}	$\overline{CS}$ Hold Time	250		ns
t_{CSB}	$\overline{CS}$ High to RDY/$\overline{BUSY}$ Low		150	ns
t_{SU}	Data In Setup Time	75		ns
t_H	Data In Hold Time	25		ns
t_{HO}	Output Hold Time	0		ns
t_{DIS}	Output Disable Time		55	ns
t_V	Output Valid		70	ns
t_{XFR}	Page to Buffer Transfer/Compare Time		700	µs
t_{EP}	Page Erase and Programming Time		20	ms
t_P	Page Programming Time		14	ms
t_{PE}	Page Erase Time		8	ms
t_{BE}	Block Erase Time		12	ms
t_{RST}	$\overline{RESET}$ Pulse Width	10		µs
t_{REC}	$\overline{RESET}$ Recovery Time		1	µs

Test Waveforms and Measurement Levels



tR, tF < 3 ns (10% to 90%)

Output Test Load

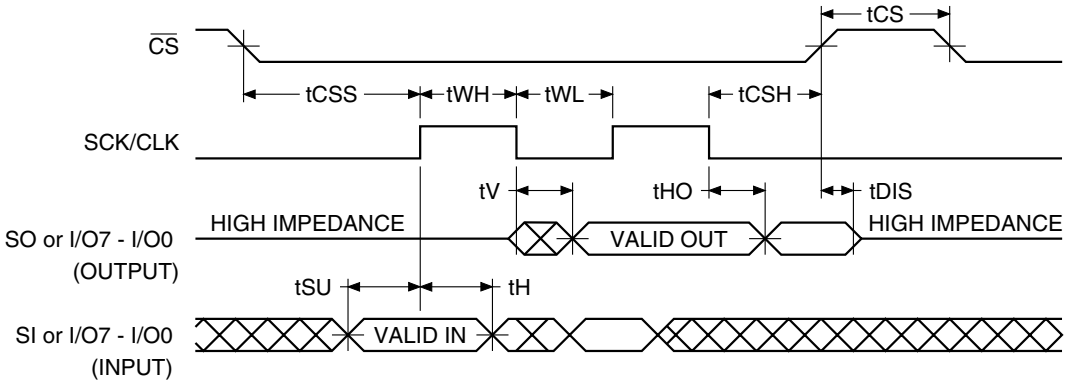


AC Waveforms

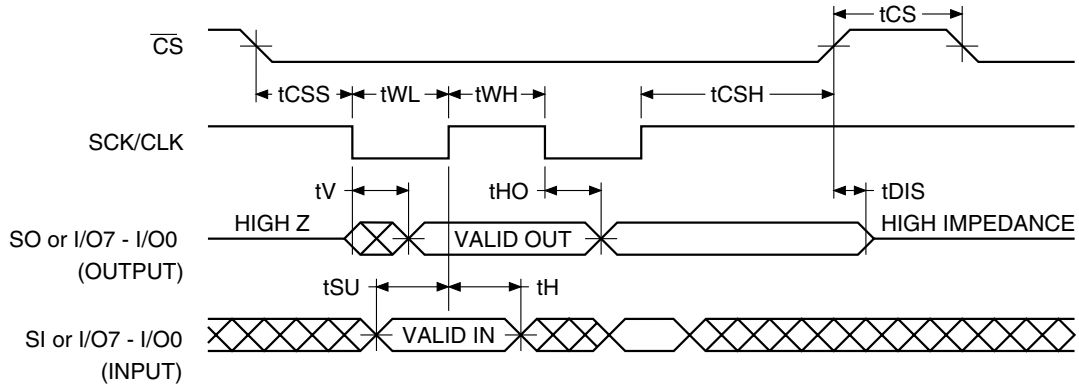
Two different timing diagrams are shown below. Waveform 1 shows the SCK/CLK signal being low when $\overline{CS}$ makes a high-to-low transition, and Waveform 2 shows the SCK/CLK signal being high when $\overline{CS}$ makes a high-to-low transition. Both waveforms show valid timing diagrams. The setup and hold times for the input signals (SI or I/O7-I/O0) are referenced to the low-to-high transition on the SCK/CLK signal.

Waveform 1 shows timing that is also compatible with SPI Mode 0, and Waveform 2 shows timing that is compatible with SPI Mode 3.

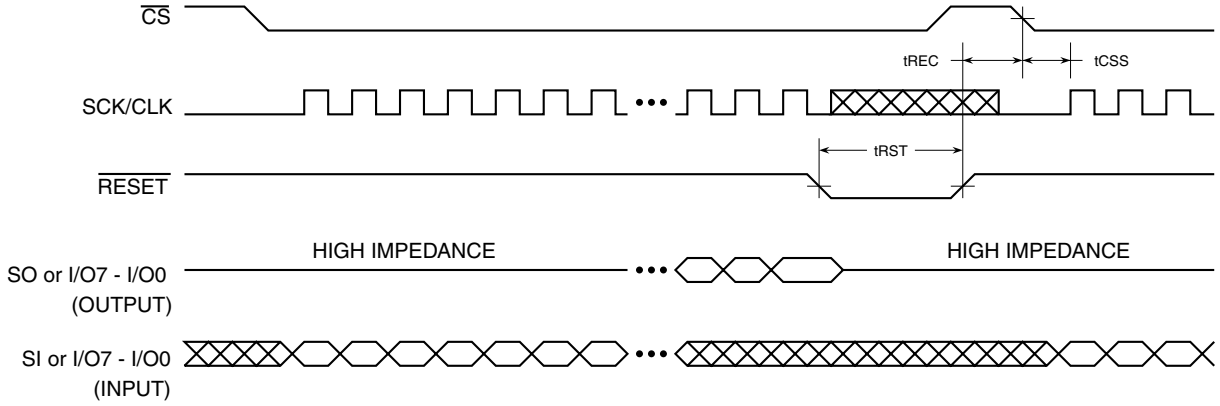
Waveform 1 – Inactive Clock Polarity Low and SPI Mode 0



Waveform 2 – Inactive Clock Polarity High and SPI Mode 3

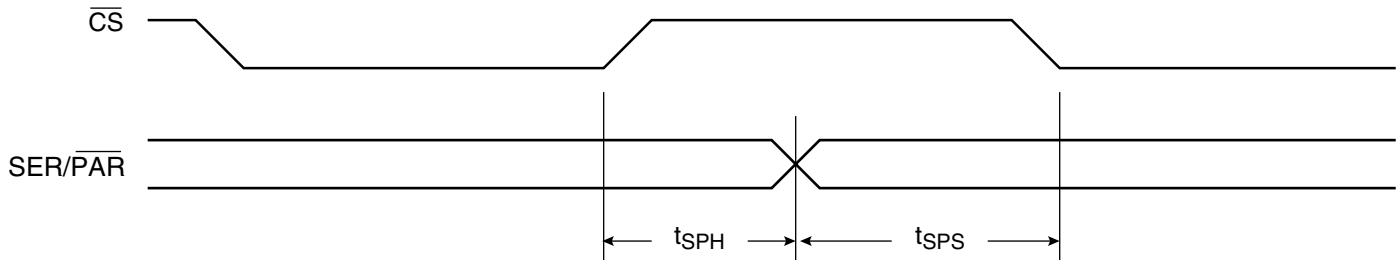


Reset Timing (Inactive Clock Polarity Low Shown)

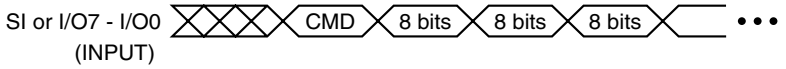


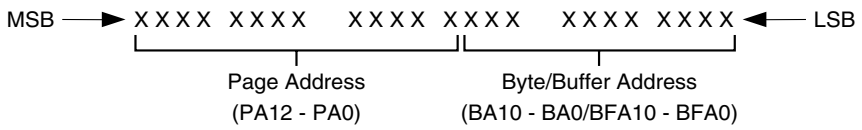
Note: The $\overline{CS}$ signal should be in the high state before the $\overline{RESET}$ signal is deasserted.

Serial/Parallel Interface Timing



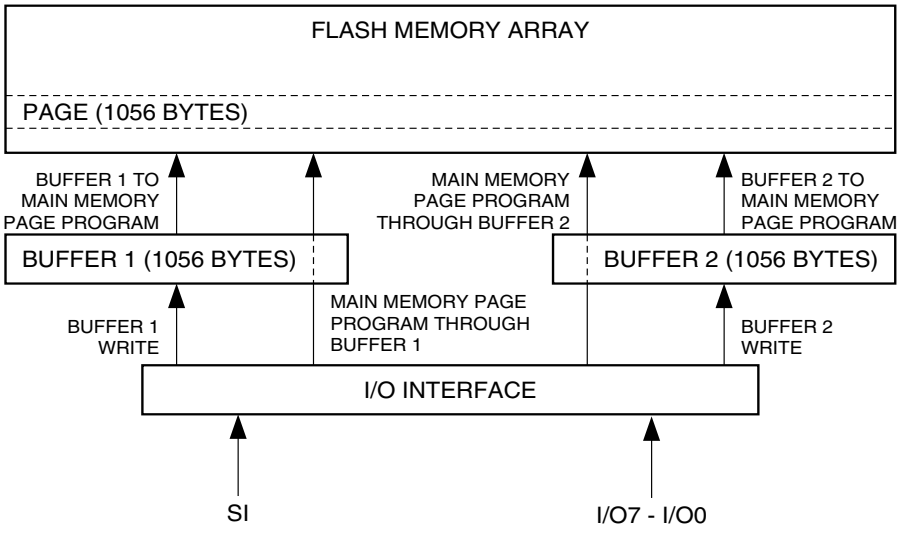
Command Sequence for Read/Write Operations (Except Status Register Read)



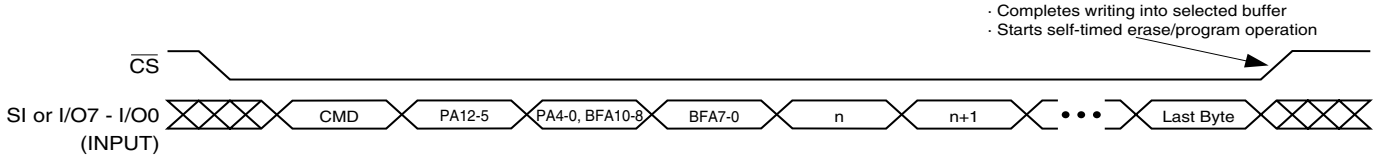


Write Operations

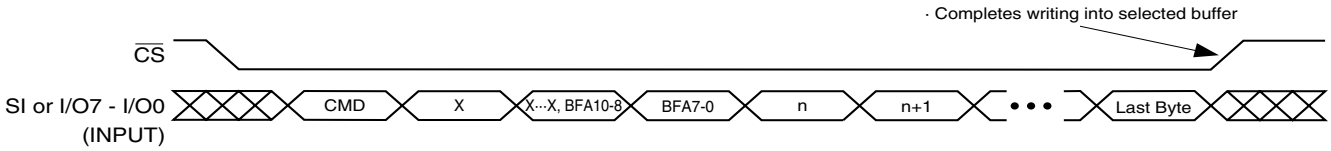
The following block diagram and waveforms illustrate the various write sequences available.



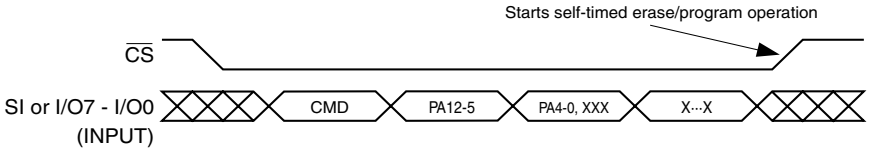
Main Memory Page Program through Buffers



Buffer Write



Buffer to Main Memory Page Program (Data from Buffer Programmed into Flash Page)

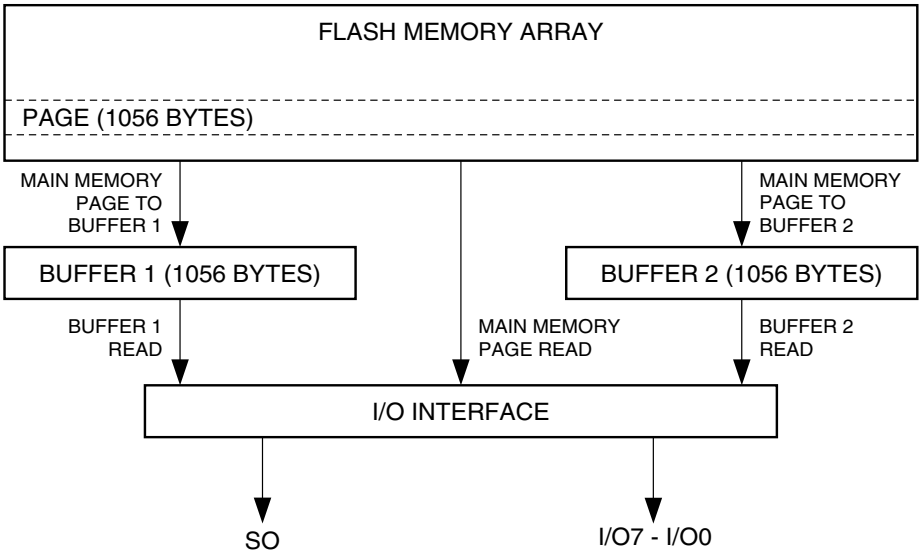


Each transition represents 8 bits

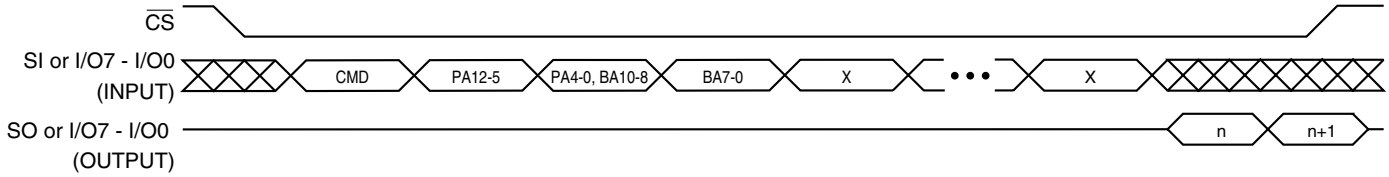
n = 1st byte read
n+1 = 2nd byte read

Read Operations

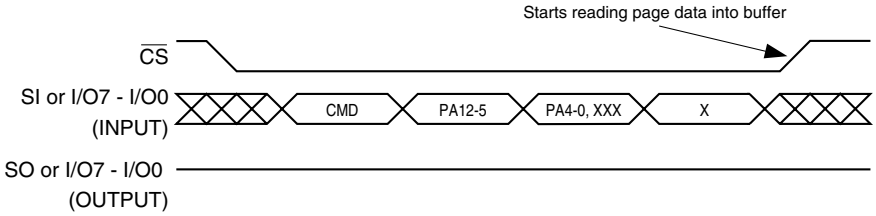
The following block diagram and waveforms illustrate the various read sequences available.



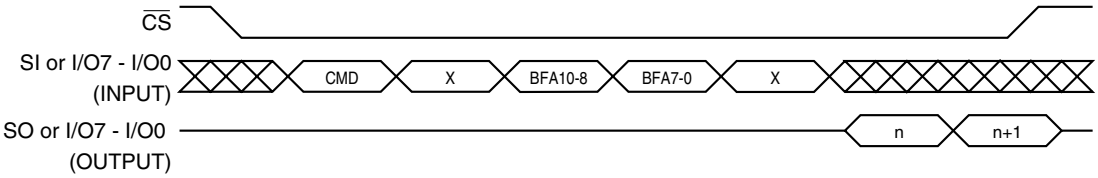
Main Memory Page Read



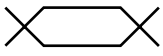
Main Memory Page to Buffer Transfer (Data from Flash Page Read into Buffer)



Buffer Read



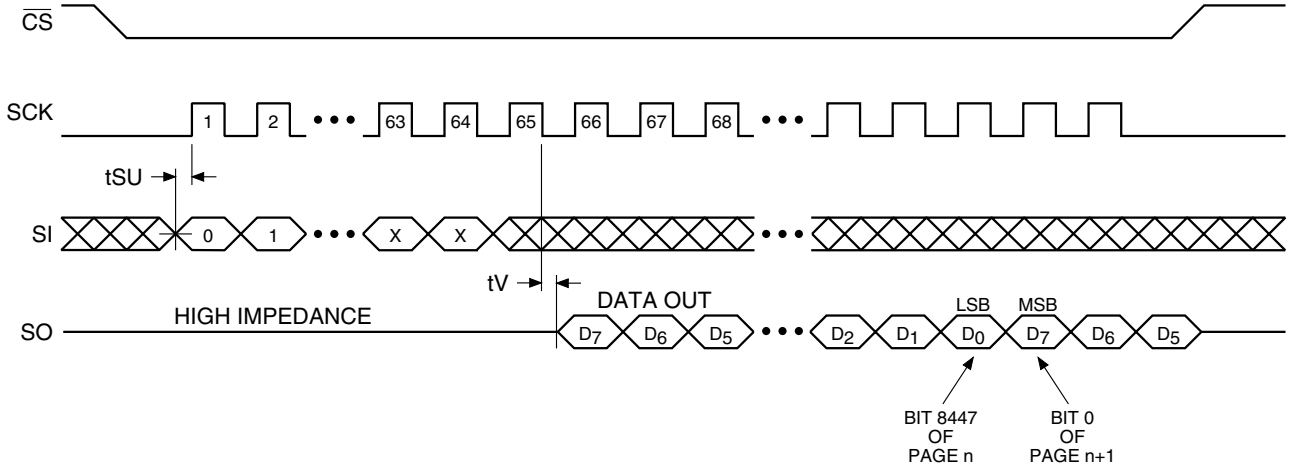
Each transition represents 8 bits



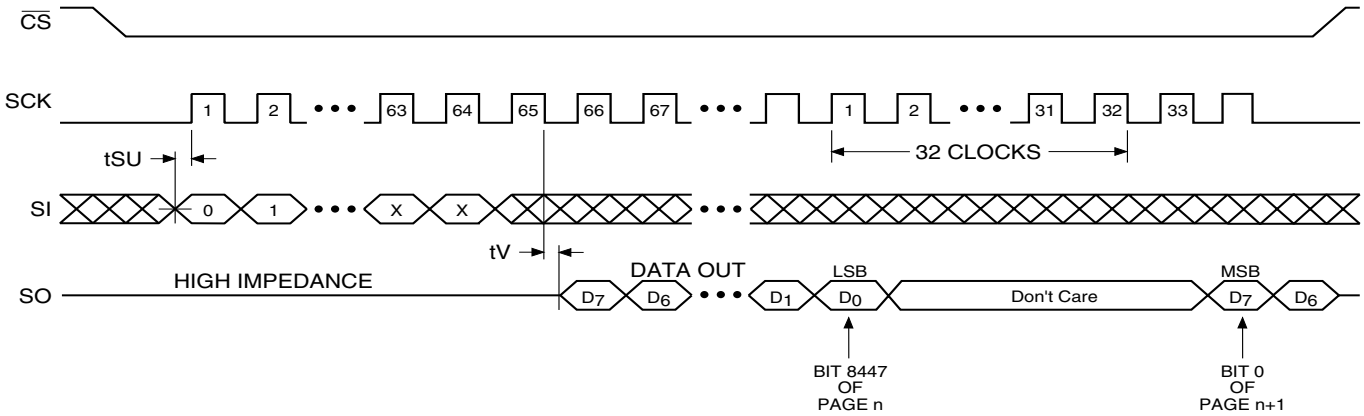
n = 1st byte read
n+1 = 2nd byte read

Detailed Bit-level Read Timing – Inactive Clock Polarity Low

Continuous Array Read (Opcode: 68H)

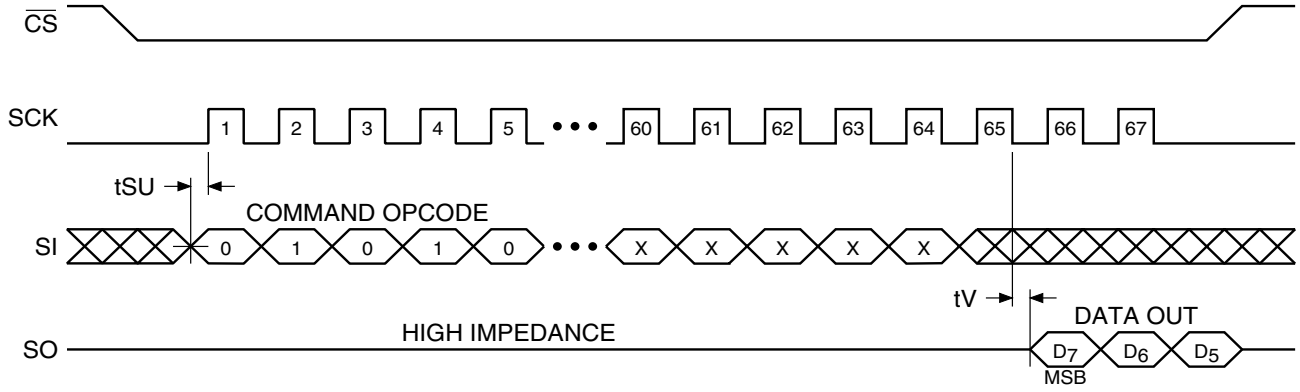


Burst Array Read with Synchronous Delay (Opcode: 69H)

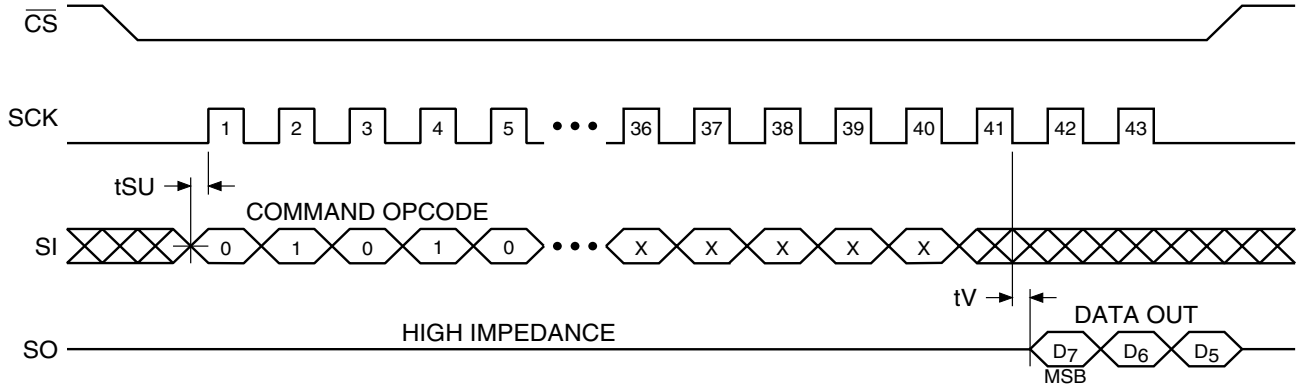


Detailed Bit-level Read Timing – Inactive Clock Polarity Low (Continued)

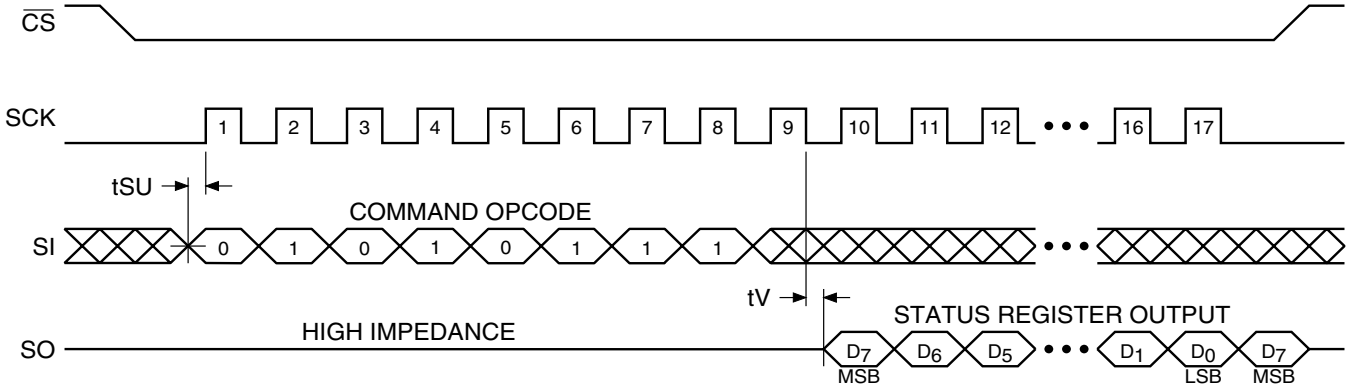
Main Memory Page Read (Opcode: 52H)



Buffer Read (Opcode: 54H or 56H)

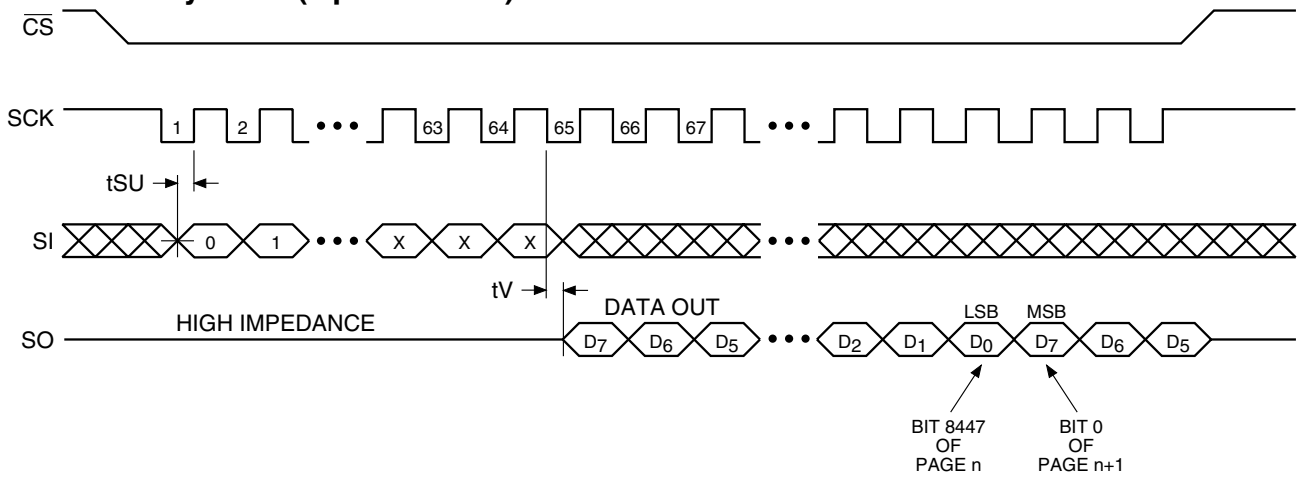


Status Register Read (Opcode: 57H)

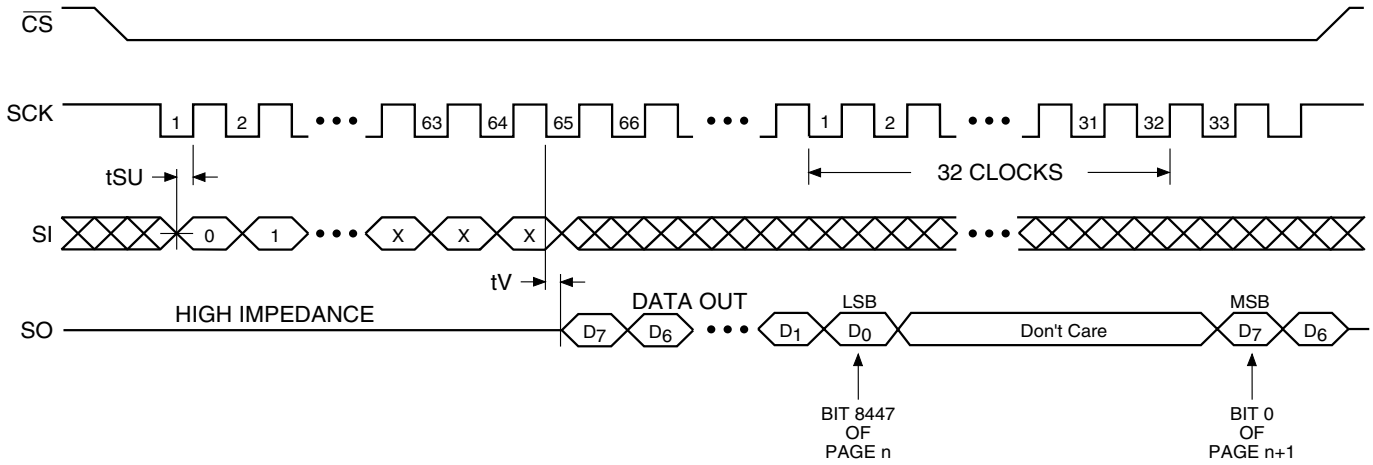


Detailed Bit-level Read Timing – Inactive Clock Polarity High

Continuous Array Read (Opcode: 68H)

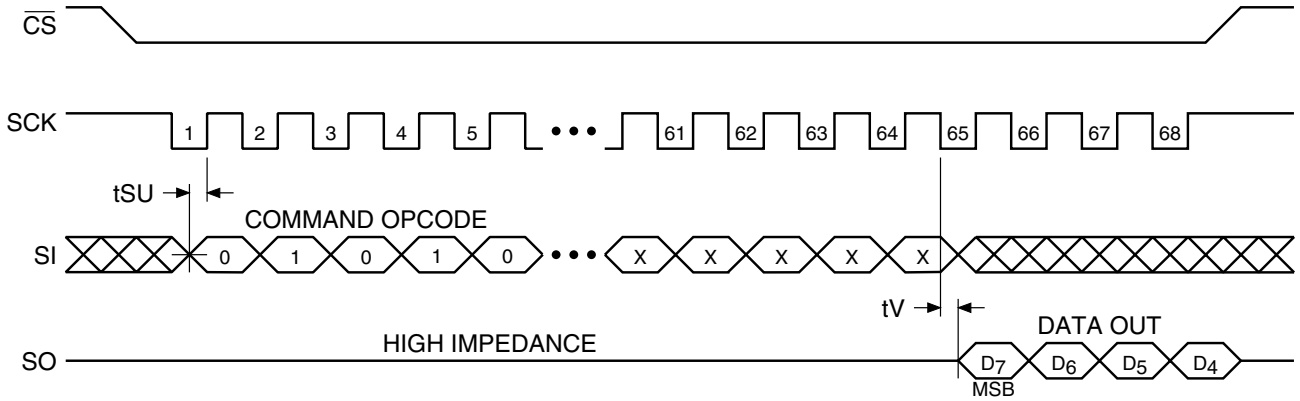


Burst Array Read with Synchronous Delay (Opcode: 69H)

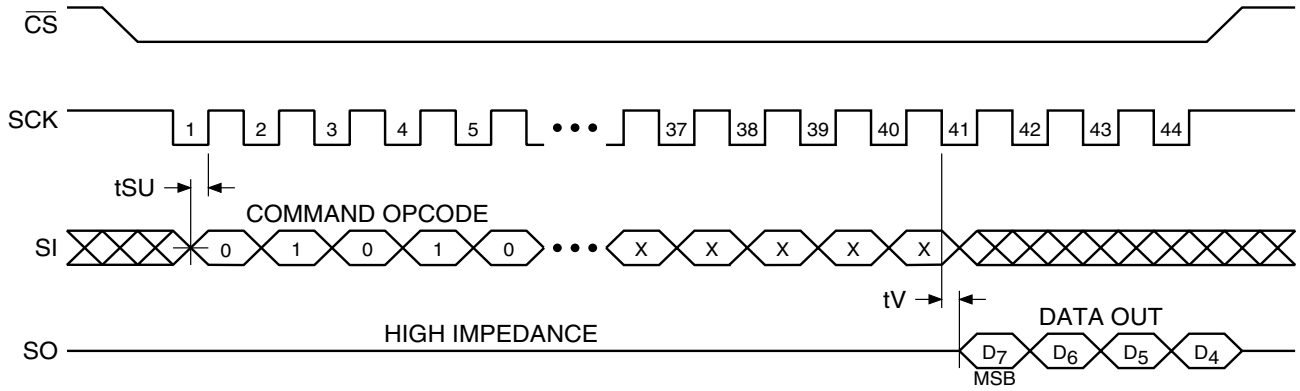


Detailed Bit-level Read Timing – Inactive Clock Polarity High (Continued)

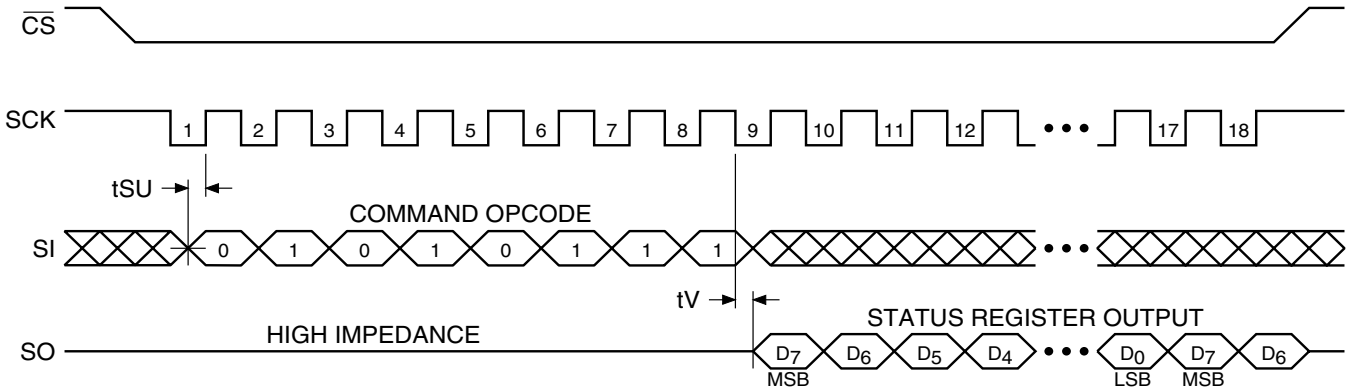
Main Memory Page Read (Opcode: 52H)



Buffer Read (Opcode: 54H or 56H)

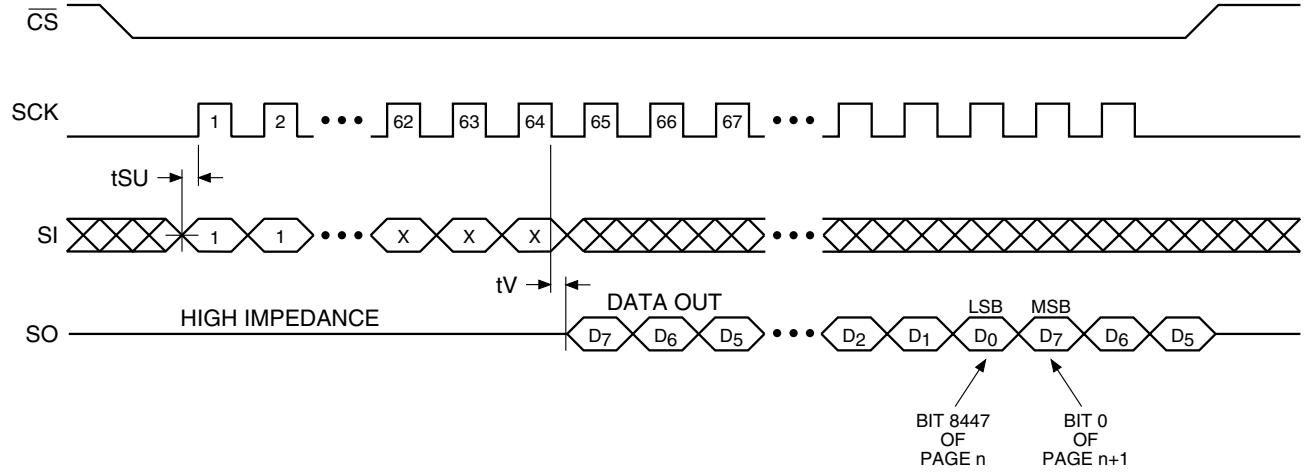


Status Register Read (Opcode: 57H)

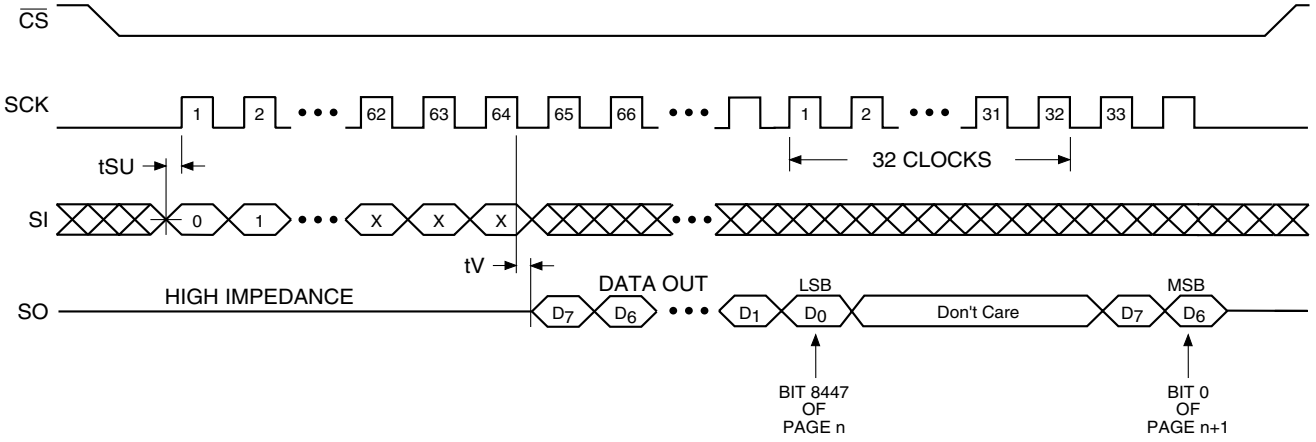


Detailed Bit-level Read Timing – SPI Mode 0

Continuous Array Read (Opcode: E8H)

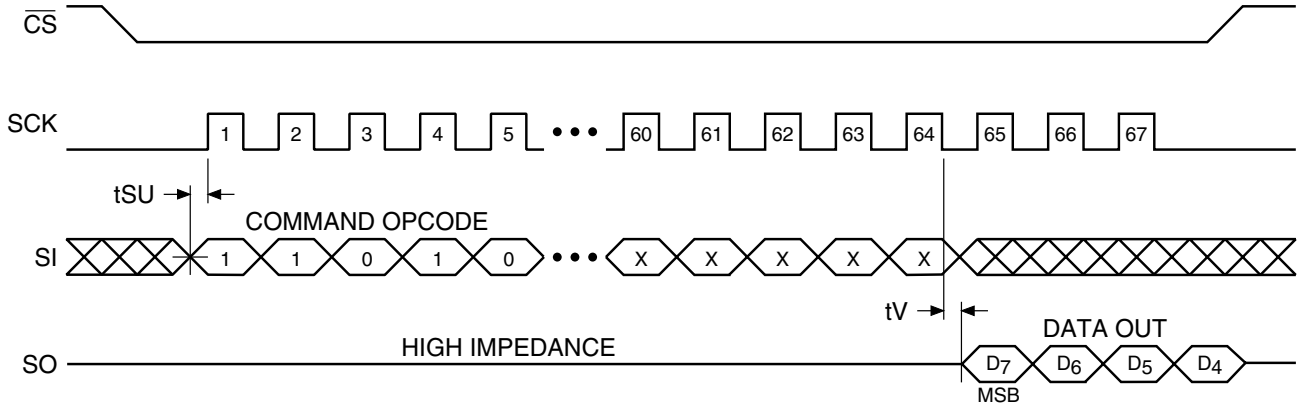


Burst Array Read with Synchronous Delay (Opcode: E9H)

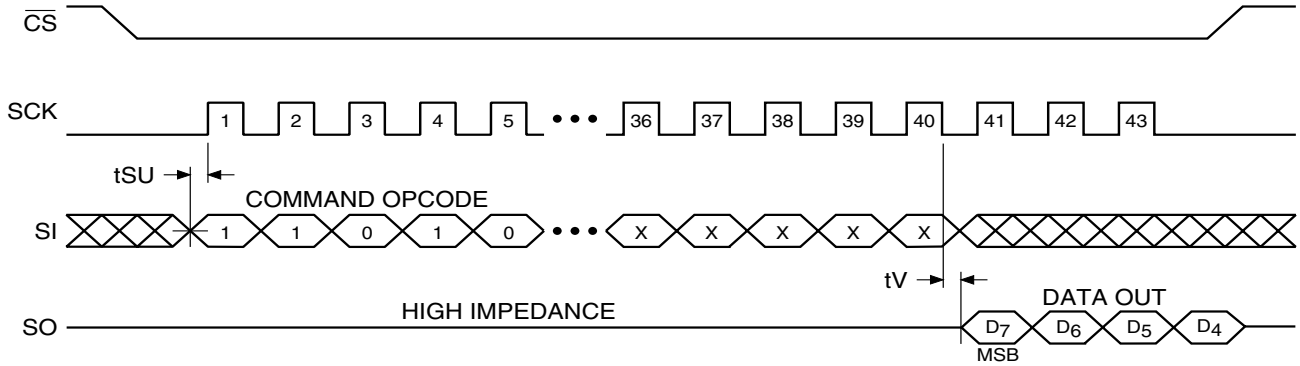


Detailed Bit-level Read Timing – SPI Mode 0 (Continued)

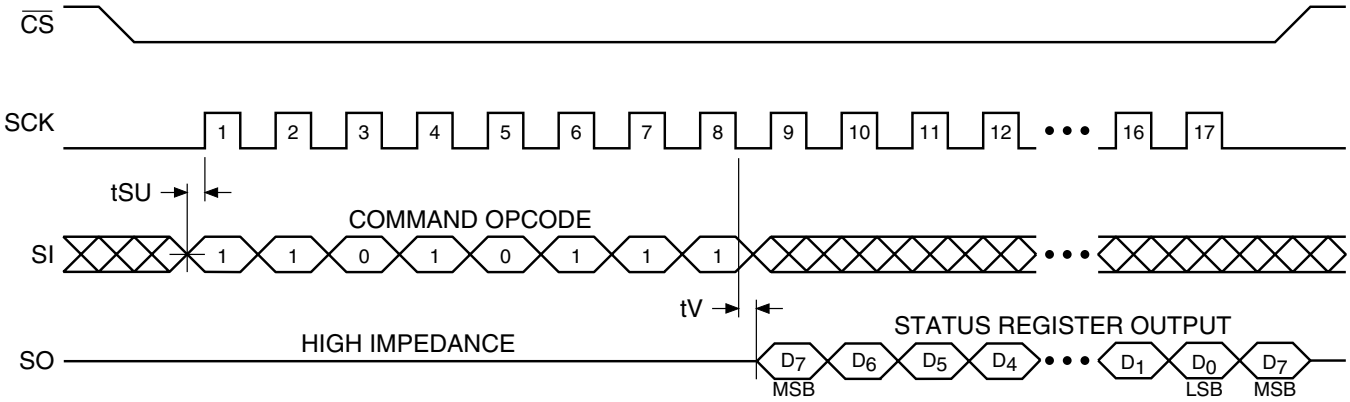
Main Memory Page Read (Opcode: D2H)



Buffer Read (Opcode: D4H or D6H)

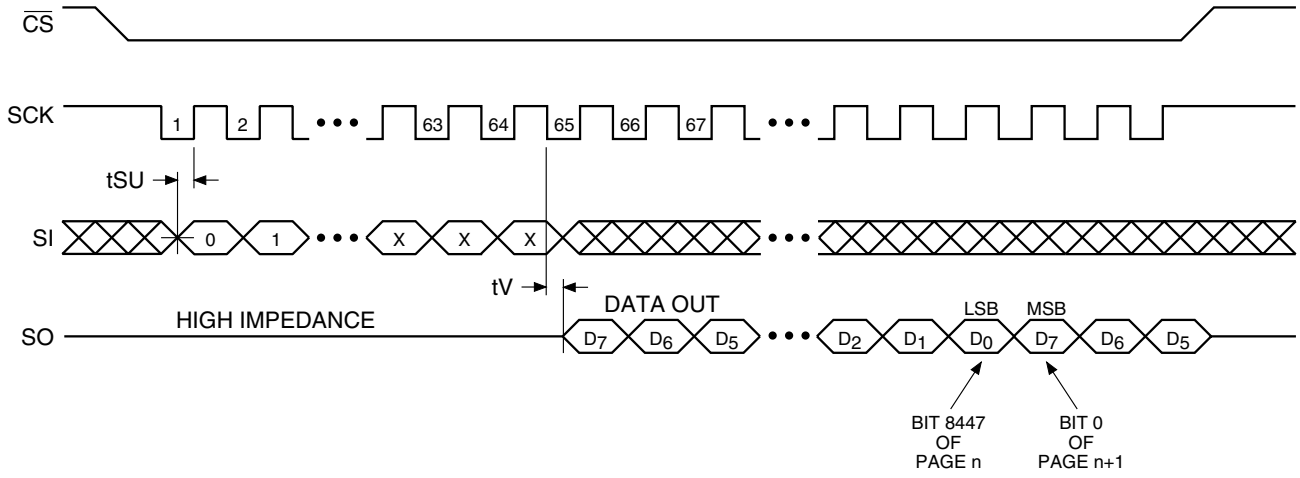


Status Register Read (Opcode: D7H)

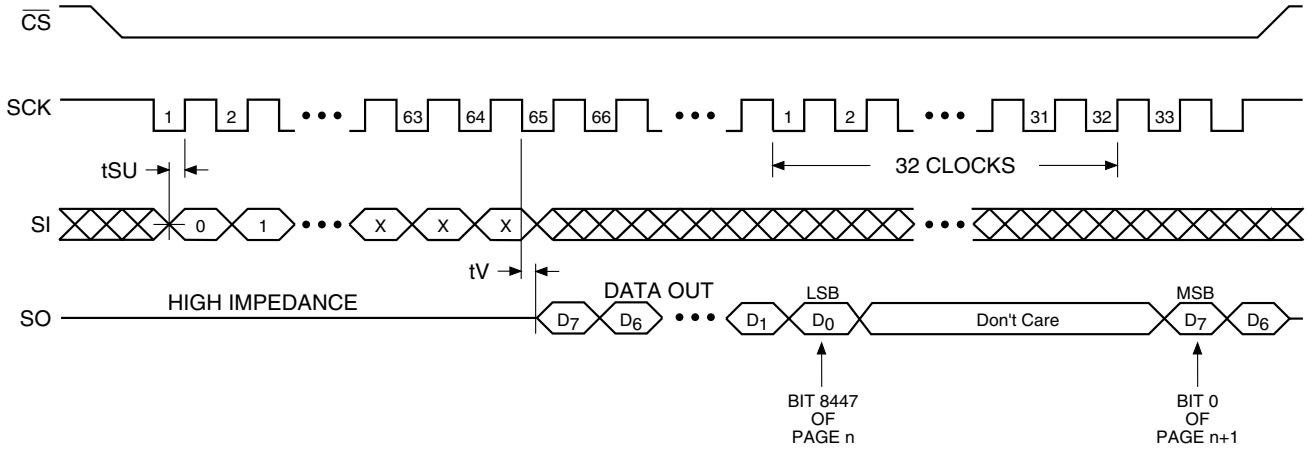


Detailed Bit-level Read Timing – SPI Mode 3

Continuous Array Read (Opcode: E8H)

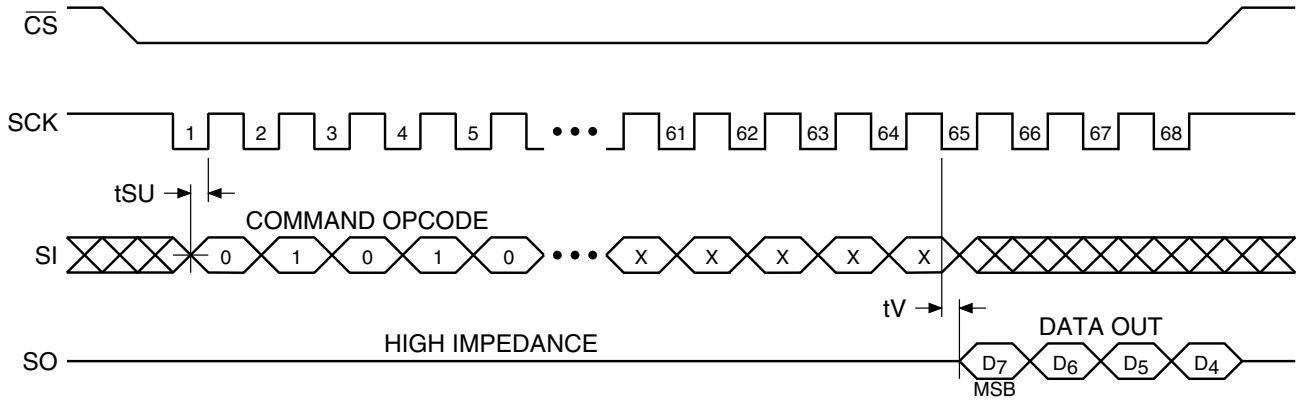


Burst Array Read with Synchronous Delay (Opcode: E9H)

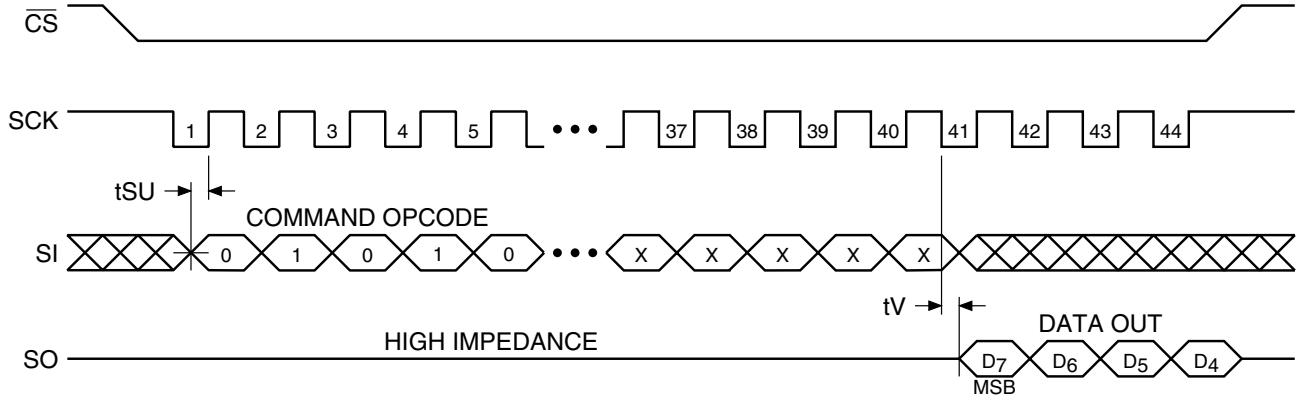


Detailed Bit-level Read Timing – SPI Mode 3 (Continued)

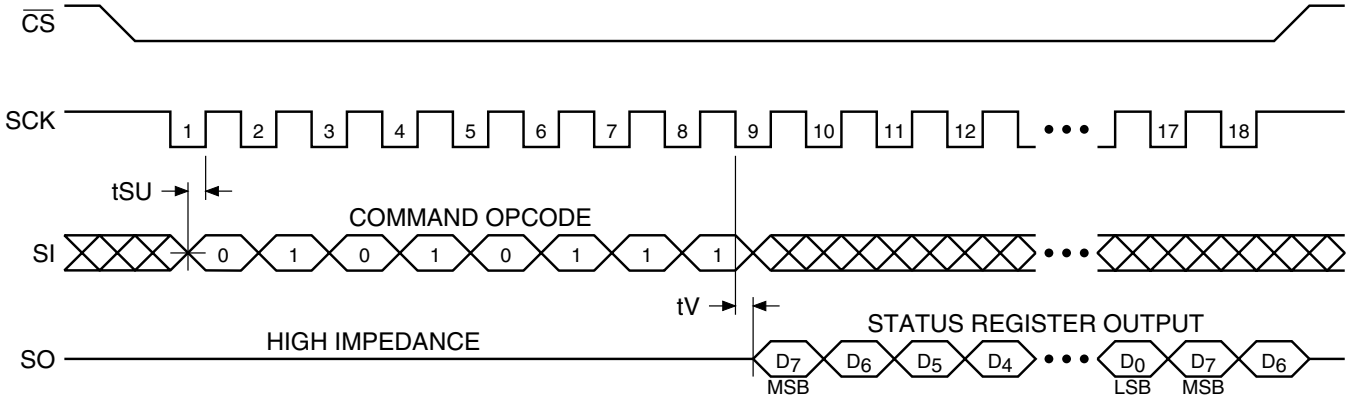
Main Memory Page Read (Opcode: D2H)



Buffer Read (Opcode: D4H or D6H)

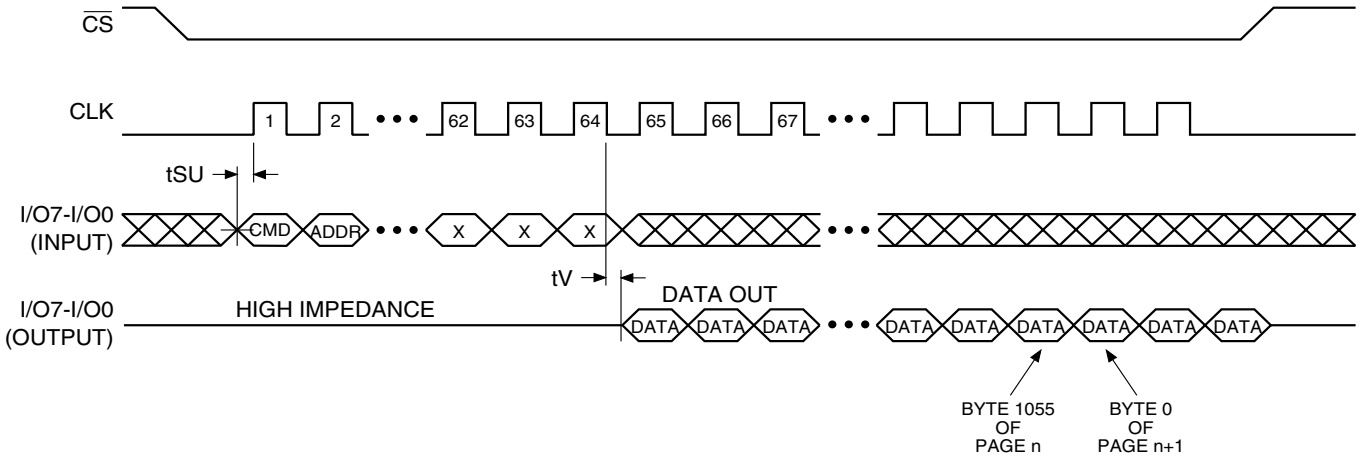


Status Register Read (Opcode: D7H)

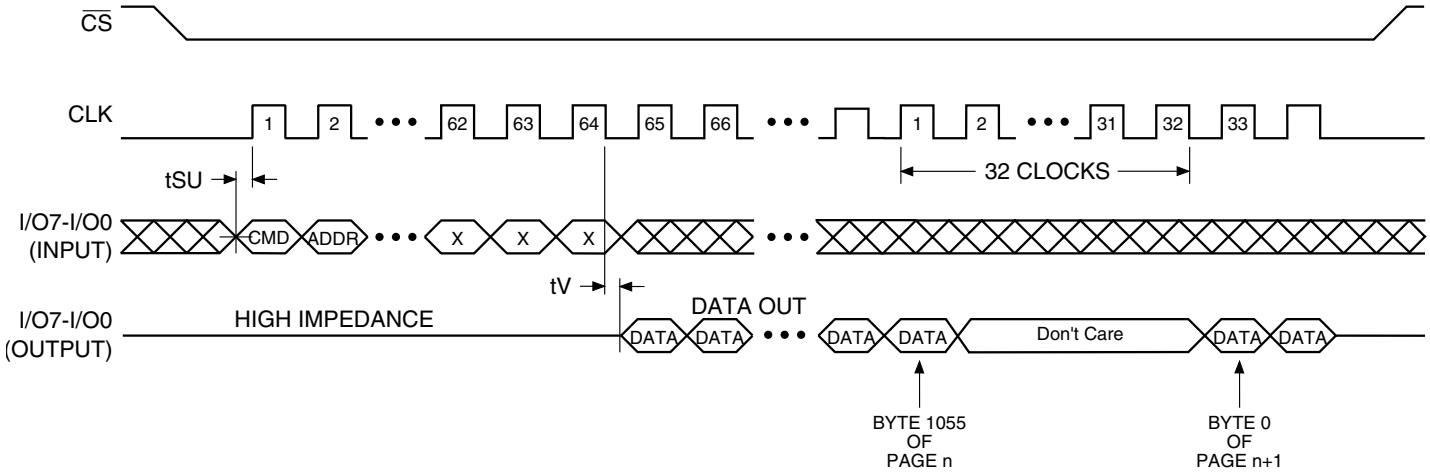


Detailed Parallel Read Timing – SPI Mode 0

Continuous Array Read (Opcode: E8H)

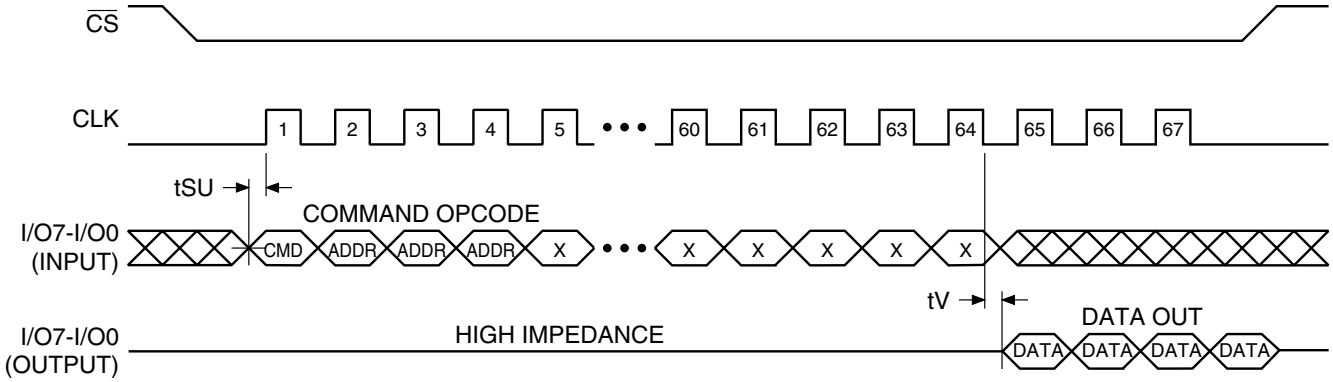


Burst Array Read with Synchronous Delay (Opcode: E9H)

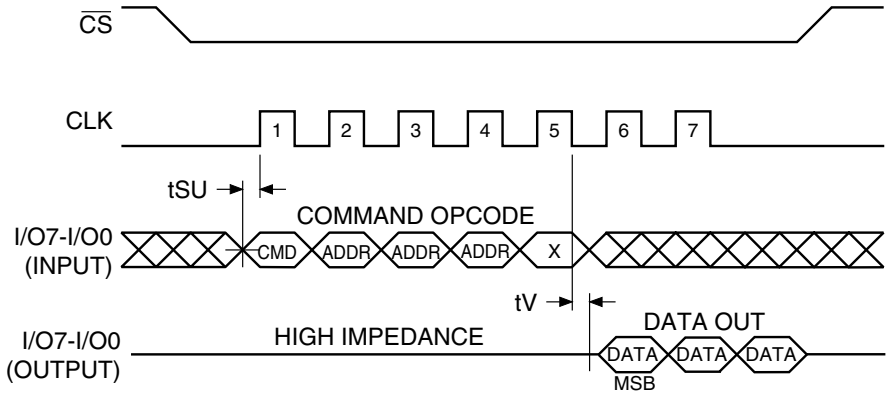


Detailed Parallel Timing – SPI Mode 0 (Continued)

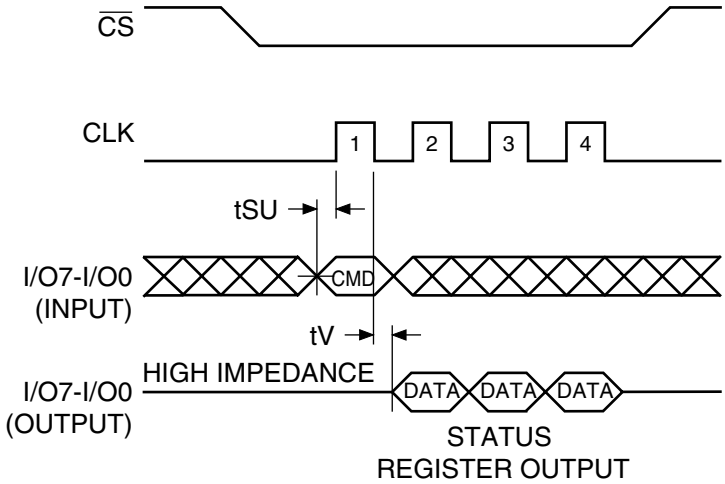
Main Memory Page Read (Opcode: D2H)



Buffer Read (Opcode: D4H or D6H)

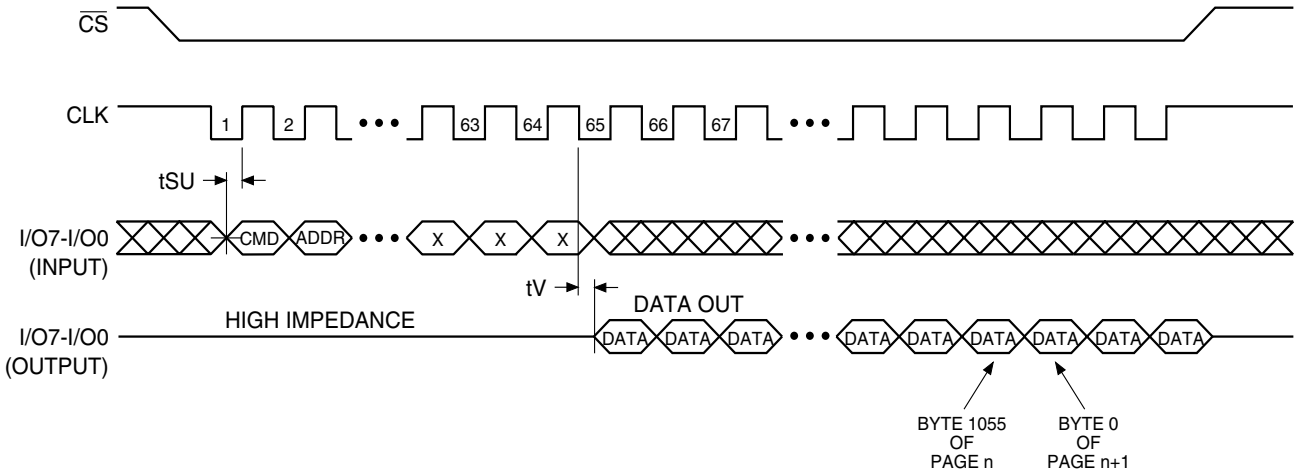


Status Register Read (Opcode: D7H)

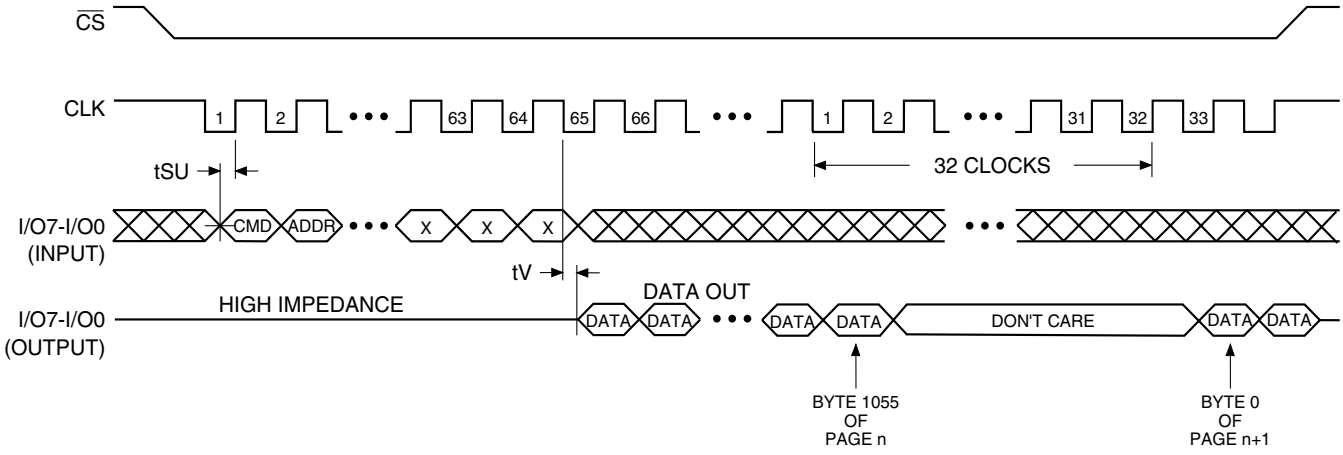


Detailed Parallel Read Timing – SPI Mode 3

Continuous Array Read (Opcode: E8H)

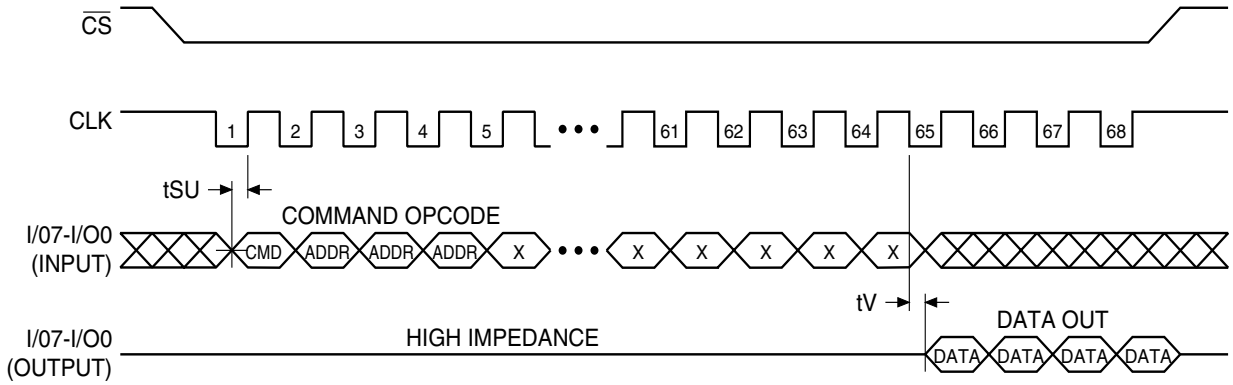


Burst Array Read with Synchronous Delay (Opcode: E9H)

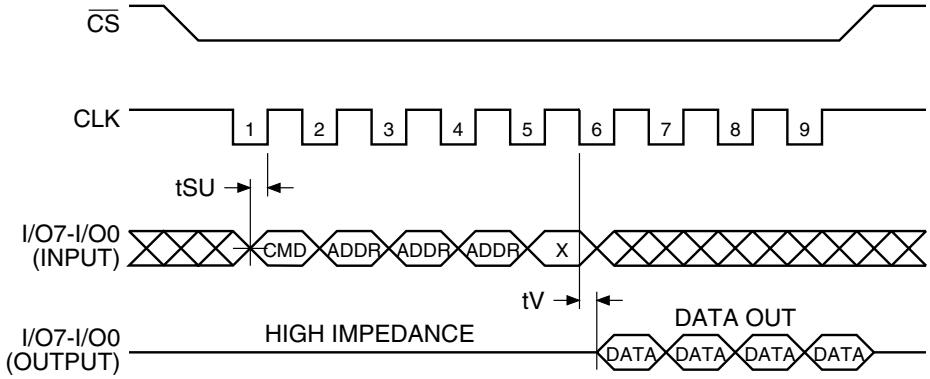


Detailed Parallel Read Timing – SPI Mode 3 (Continued)

Main Memory Page Read (Opcode: D2H)



Buffer Read (Opcode: D4H or D6H)



Status Register Read (Opcode: D7H)

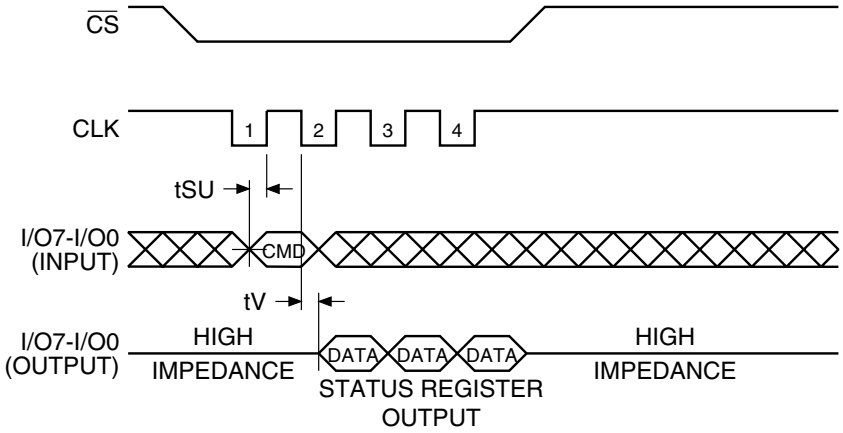
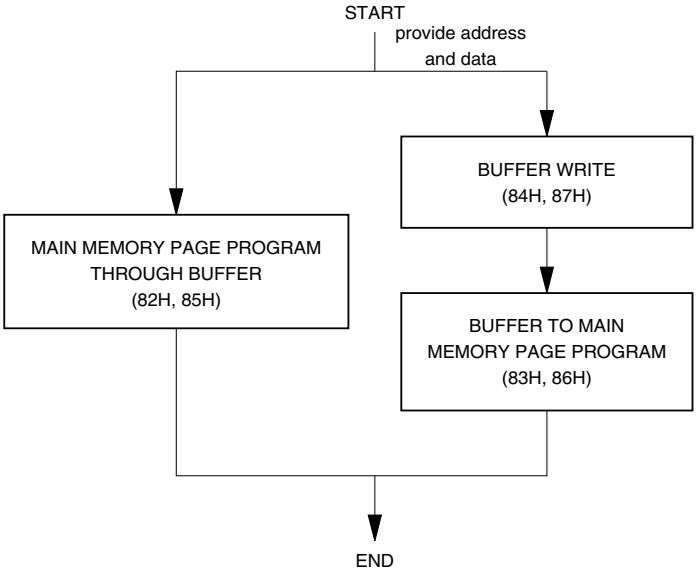
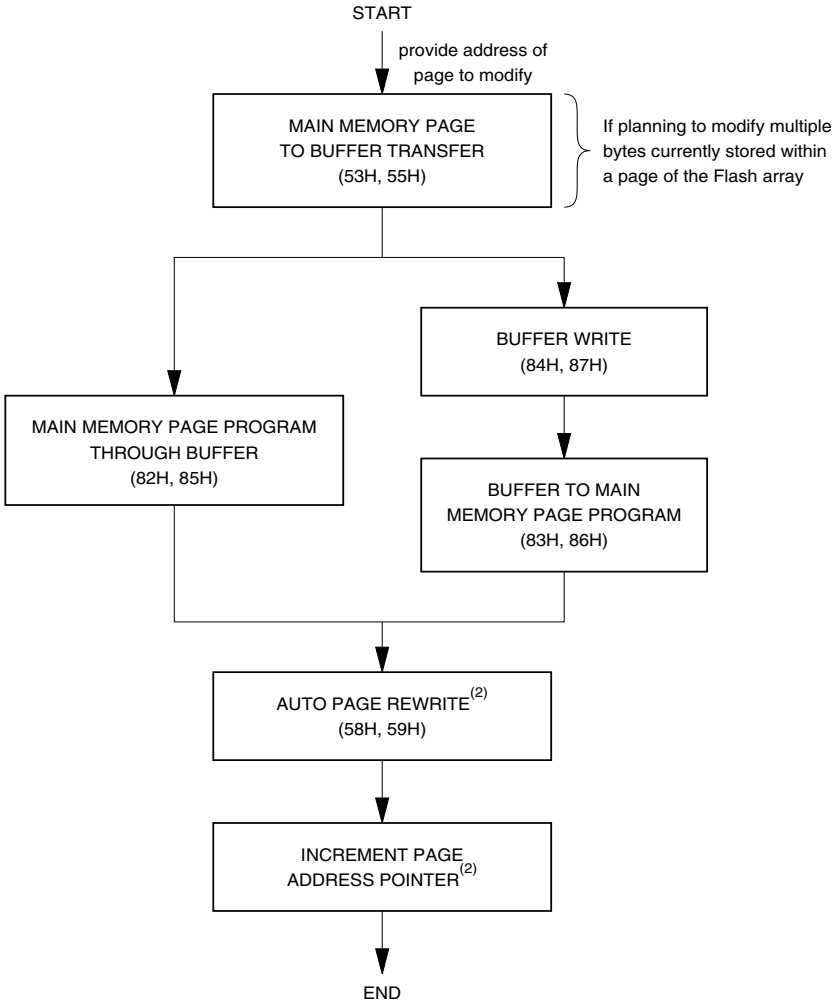


Figure 1. Algorithm for Programming or Reprogramming of the Entire Array Sequentially



Notes:
1. This type of algorithm is used for applications in which the entire array is programmed sequentially, filling the array page-by-page.
2. A page can be written using either a Main Memory Page Program operation or a Buffer Write operation followed by a Buffer to Main Memory Page Program operation.
3. The algorithm above shows the programming of a single page. The algorithm will be repeated sequentially for each page within the entire array.

Figure 2. Algorithm for Randomly Modifying Data



Notes: 1. To preserve data integrity, each page of a DataFlash sector must be updated/rewritten at least once within every 10,000 cumulative page erase/program operations.
2. A Page Address Pointer must be maintained to indicate which page is to be rewritten. The Auto Page Rewrite command must use the address specified by the Page Address Pointer.
3. Other algorithms can be used to rewrite portions of the Flash array. Low-power applications may choose to wait until 10,000 cumulative page erase/program operations have accumulated before rewriting all pages of the sector. See application note AN-4 (“Using Atmel’s Serial DataFlash”) for more details.

Sector Addressing

PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2 - PA0	Sector
0	0	0	0	0	0	0	0	0	0	X	0
0	0	0	0	0	X	X	X	X	X	X	1
0	0	0	0	1	X	X	X	X	X	X	2
0	0	0	1	0	X	X	X	X	X	X	3
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•	•
1	1	1	0	0	X	X	X	X	X	X	29
1	1	1	0	1	X	X	X	X	X	X	30
1	1	1	1	0	X	X	X	X	X	X	31
1	1	1	1	1	X	X	X	X	X	X	32

Ordering Information

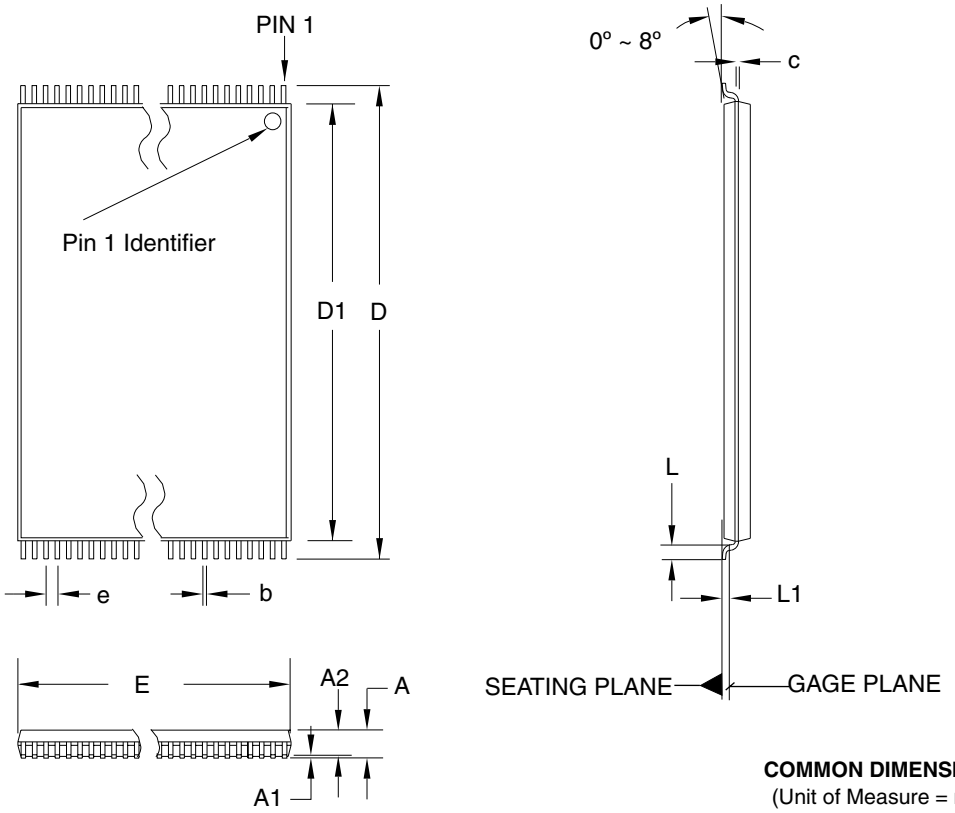
f_{SCK} (MHz)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
20[1]	10[1]	0.01	AT45DB642-TC	40T	Commercial (0°C to 70°C)
20[1]	10[1]	0.01	AT45DB642-TI	40T	Industrial (-40°C to 85°C)

Note: 1. Serial Interface

Package Type	
40T	40-lead, Plastic Thin Small Outline Package (TSOP)

Packaging Information

40T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	19.80	20.00	20.20	
D1	18.30	18.40	18.50	Note 2
E	9.90	10.00	10.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.50 BASIC			

Notes:
1. This package conforms to JEDEC reference MO-142, Variation CD.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

10/18/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40T**, 40-lead (10 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)	40T	B

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