THE DATASHEET OF

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AS3722

Multi-Phase DCDC Controller PMIC

General Description

The AS3722 is a compact System PMU supporting up to 20 high current rails.

The device offers advanced power management functions. All necessary ICs and peripherals in a battery powered mobile device are supplied by the AS3722. It features 4 DCDC buck converters as well as 11 low noise LDOs. The different regulated supply voltages are programmable via the serial control interface. 3-4MHz operation with 0.47uH coils is reducing cost and PCB space.

AS3722 further features 3 DCDC buck controller which are ideal to support processor currents ranging from 5A up to 32A depending on the used power stages. The multi-phase topology operating on 3MHz ensures fast load transient responses and reduces the footprint for external components.

The single supply voltage may vary from 2.7V to 5.5V.

Ordering Information and *Content Guide* appear at end of datasheet.

Key Benefits & Features

The benefits and features of AS3722, Multi-Phase DCDC Controller PMIC are listed below:

Figure 1:
Added Value of Using AS3722

Benefits	Features
• Compact design due to small coils for IO and memory voltage generation	• 4 DCDC step down regulators (3-4MHz) • Output (0.6V-3.35V; 1x5A, 1x2A, 2x1.5A)
• High current generation with external power stages to minimize PMIC power dissipation	• 3 DCDC step down controller • DVM (0.6V-1.5V; 1x6A, 1x12A, 1x24A)

• Multiple independent voltage rails for general purpose IO supplies	• 11 universal LDOs
	  • 9x universal IO range(0.8-3.3V; 0.3A)
	  • 1x low output range (0.6-1.5V; 0.3A)
	  • 1x extended input range (0.8-1.2V; 0.3A)

• Ultra low-power oscillator and no external caps needed	• RTC
	  • 1µA total power consumption
	  • Programmable alarm
	  • Auto wake-up, repeating alarms
	  • 32kHz output to peripherals

Benefits	Features

• Safe supervision in HW which works also without a processor	• Supervisor with interrupt generation and selectable warning levels
	  • Automatic battery monitoring
	  • Automatic temperature monitoring
	  • Automatic over-current monitoring
	  • Power supply supervision for DCDC

• Flexible multi-purpose IOs for general control tasks	• General Purpose IOs
	  • ADC input
	  • Wake-up/stand-by input
	  • PWM input/output
	  • Low battery and power good status

• Enables the processor to check the actual system state in detail	• ADC with internal and external sources
• Flexible and fast adaptation to different processors/applications	• OTP programmable Boot and Power-down sequence
• Power saving control according to the processor needs	• Stand-by function with programmable sequence and voltages

• Self-contained start-up and control for single and multi-cell battery applications. Safety shutdown feature	• Control Interface
	  • I2C/SPI control lines with watchdog
	  • ONKEY with 4/8s emergency shut-down
	  • POR with RESET I/O
	  • 5V pre-regulator enable

• Dedicated packages for specific applications. Optimization for PCB cost or size	• Package
	  • 124-pin CTBGA (8x8mm), 0.5mm pitch
	  • 108-pin WL-CSP (4.8x3.6mm), 0.4mm pitch

Applications

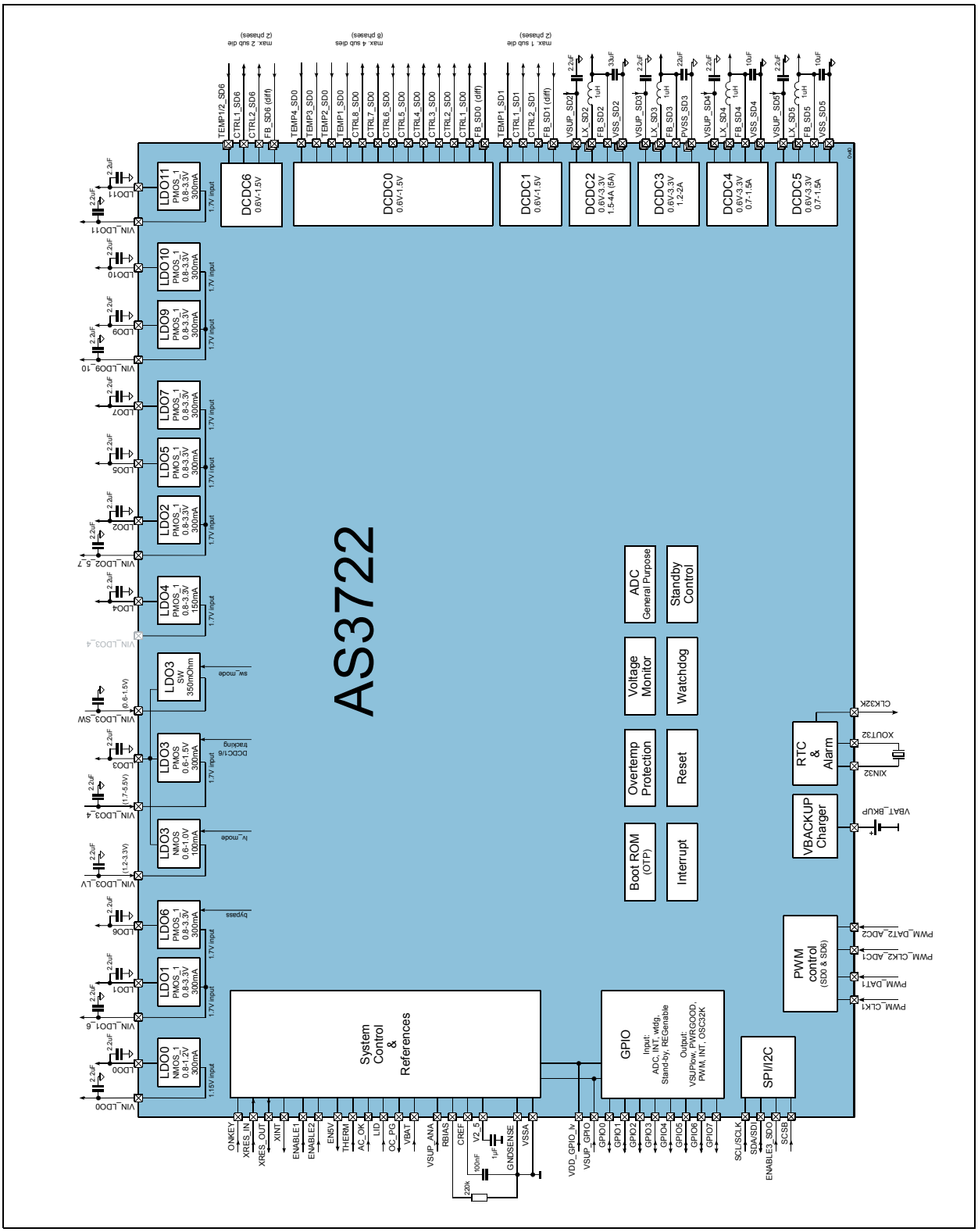
The device is suitable for:

- Mobile Phones
- Tablet PCs
- NetBooks
- Portable Media Players
- Portable Navigation Devices
- Mobile Internet Devices

Block Diagram

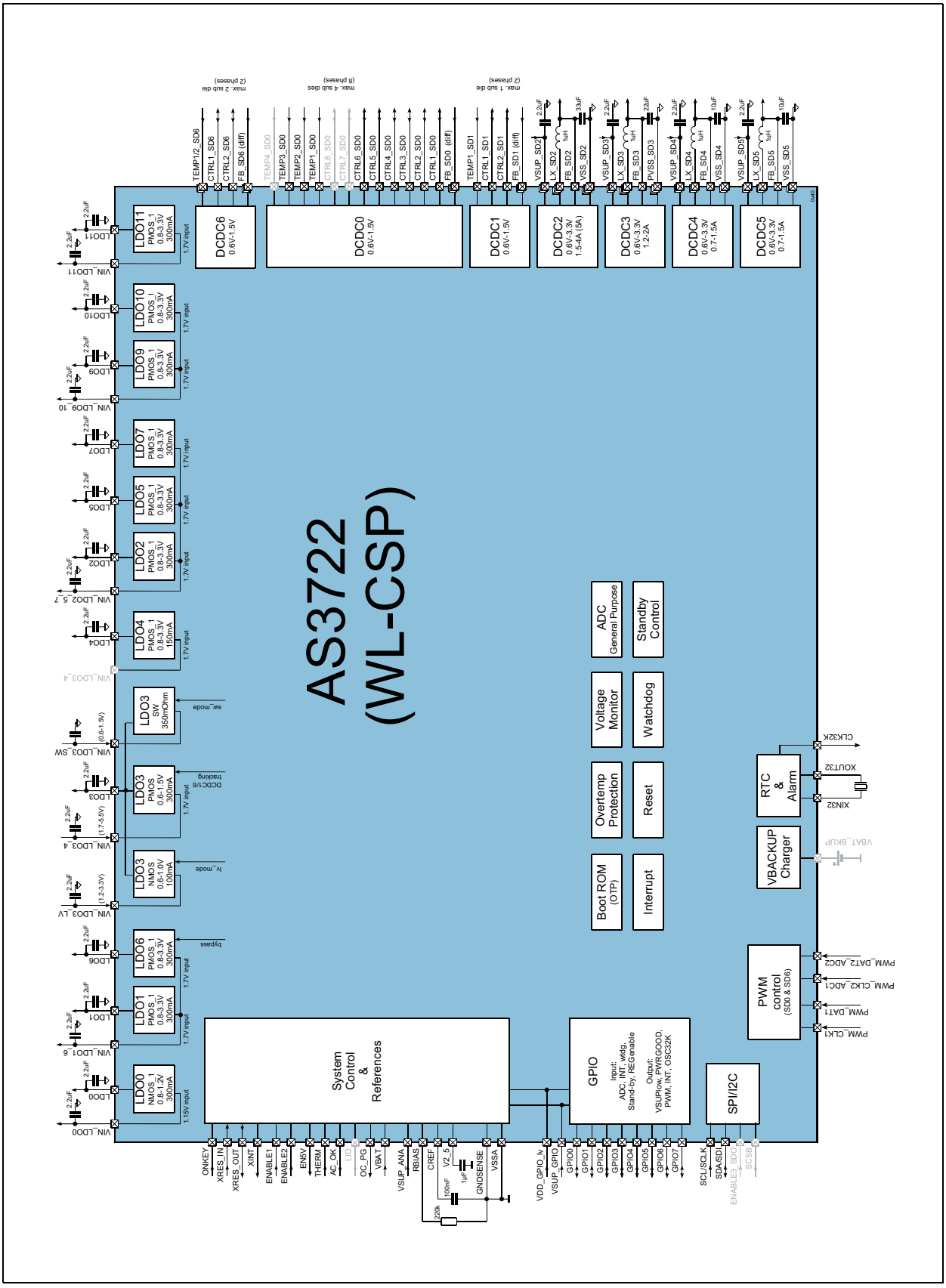
The functional blocks of this device are shown below:

Figure 2:
AS3722 Block Diagram (CTBGA)



Block Diagram: Shows the main function blocks of the AS3722 including basic external components.

Figure 3:
AS3722 Block Diagram (WL-CSP)



Block Diagram: Shows the main function blocks of the AS3722 in WL-CSP package.

Pin Assignment

Figure 4:
Pin Assignment (CTBGA124)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSSA	LDO4	VIN_ LDO3_ 4	VIN_ LDO3_ SW	LDO9	VIN_ LDO9_ 10	LDO6	VIN_ LDO1_ 6	LDO2	LDO5	LDO7	VIN_ LDO2_ 5_7	LDO0	VSSA
B	VIN_ LDO11		GPIO4	GPIO6	LDO11	VIN_ LDO3_ LV	LDO3	LDO10	LDO1	ONKEY	PWM_ CLK2_ ADC1	PWM_ DAT2_ ADC2		VIN_ LDO0
C	XINT	GPIO5											CTRL1 _SD6	CTRL2 _SD6
D	CLK 32K	GPIO7			GPIO2	GPIO0	LID	THERM	PWM_ CLK1	PWM_ DAT1			CTRL1 _SD1	CTRL2 _SD1
E	OC_PG	ENABLE 3_SDO		GPIO3							ENABL E2		CTRL1 _SD0	CTRL2 _SD0
F	VSS_ GPIO	VDD_ GPIO_ LV		SDA_ SDI			VSSA	ENABL E1			FB_ SD6_P		CTRL3 _SD0	CTRL4 _SD0
G	XIN32K	XOUT 32K		SCL_ SCLK		GPIO1			FB_ SD1_P		FB_ SD6_N		CTRL5 _SD0	CTRL6 _SD0
H	VSUP_ ANA	V2_5		VBAT_ BKUP		SCSB			FB_ SD1_N		FB_ SD0_P		CTRL7 _SD0	CTRL8 _SD0
J	FB_SD 5	RBIAS		CREF			VSSA	XRES_ IN			FB_ SD0_N		TEMP2 _SD0	TEMP 1_SD0
K	FB_SD 2	FB_SD 3		GND SENSE							TEMP4 _SD0		TEMP3 _SD0	TEMP _SD1
L	VSUP_ SD3	VSUP_ SD3			XRES_ OUT	EN5V	VBAT	AC_OK	VSUP_ GPIO	FB_SD 4			TEMP2 _SD6	TEMP 1_SD6
M	LX_ SD3	LX_ SD3											VSS_ SD4	VSS_ SD4
N	LX_ SD3		VSS_ SD3	VSS_ SD2	LX_ SD2	VSUP_ SD2	LX_ SD2	VSS_ SD2	VSS_ SD5	LX_ SD5	VSUP_ SD5	VSUP_ SD4		LX_ SD4
P	VSSA	VSS_ SD3	VSS_ SD3	VSS_ SD2	LX_ SD2	VSUP_ SD2	LX_ SD2	VSS_ SD2	VSS_ SD5	LX_ SD5	VSUP_ SD5	VSUP_ SD4	LX_ SD4	VSSA

Pin Assignment: Shows the top view pin assignment of the AS3722 in the CTBGA124.

Figure 5:
Ball Assignment (WL-CSP108)

	1	2	3	4	5	6	7	8	9	10	11	12
A	PWM_ DAT2_ ADC1	ONKEY	LDO7	LDO5	LDO6	LDO1	LDO9	LDO3	LDO4	GPIO0	GPIO5	XINT
B	PWM_ CLK2_ ADC1	THERM	VIN_LDO 0	VIN_LDO 2_5_7	LDO2	VIN_LDO 1_6	VIN_LDO 9_10	VIN_LDO 3_SW	VIN_LDO 11	GPIO4	CLK32K	GPIO7
C	CTRL1_ SD6	ENABLE 1	XRES_IN	LDO0	PWM_ DAT1	PWM_ CLK1	VIN_LDO 3_LV	LDO11	GPIO3	VSUP_ GPIO	OC_PG	SCL_ SCLK
D	CTRL2_ SD6	CTRL1_ SD1	ENABLE2	AC_OK	CTRL2_ SD1	LDO10	VIN_LDO 3_4	GPIO2	VBAT	VDD_ GPIO_LV	SDA_SDI	V2_5
E	CTRL5_ SD0	CTRL2_ SD0	CTRL1_ SD0	CTRL3_ SD0	CTRL4_ SD0	VSSA	GPIO1	EN5V	XOUT 32K	XIN32K	CREF	VSUP_ ANA
F	TEMP2_ SD0	CTRL6_ SD0	VSUP_ GPIO	TEMP1_ SD0	TEMP3_ SD0	FB_SD0_ P	GPIO6	XRES_ OUT	VSSA	FB_SD5	RBIAS	FB_SD2
G	FB_SD6 _N	FB_SD6 _P	TEMP_ SD1	FB_SD1_ P	FB_SD1 _N	VSSA	VSSA	LX_SD2	LX_SD2	FB_SD3	VSS_ SD3	VSS_ SD3
H	TEMP1_ SD6	FB_SD4	FB_SD0_ N	VSUP_ SD4_5	LX_SD5	VSS_ SD5	VSS_ SD2	VSUP_ SD2	LX_SD2	VSS_ SD2	LX_SD3	VSUP_ SD3
J	TEMP2_ SD6	VSS_ SD4	LX_SD4	VSUP_ SD4_5	LX_SD5	VSS_ SD5	VSS_ SD2	VSUP_ SD2	LX_SD2	VSS_ SD2	LX_SD3	VSUP_ SD3

Ball Assignment: Shows the top view pin assignment of the AS3722 in the WL-CSP108.

Pin Description

Figure 6:
Pin Description

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
F4	D11	SDA_SDI	DI	SPI digital input in SPI mode; Data IO in I2C mode.	VSUP	Open
G4	C12	SCL_SCLK	DI	SPI clock input in SPI mode; SCK input in I2C mode.	VSUP	Open
E2		ENABLE3_SDO	DIO	SPI digital output in SPI mode	VSUP	Define level
H6		SCSB	DI	SPI chip-select in SPI mode; connect to VSS in I2C mode.	VSUP	VSS
B14	B3	VIN_LDO0	S	Supply pad for LDOs	5.5V	Mandatory
A8	B6	VIN_LDO1_6	S	Supply pad for LDOs	5.5V	Mandatory
A6	B7	VIN_LDO9_10	S	Supply pad for LDOs	5.5V	Mandatory
A3	D7	VIN_LDO3_4	S	Supply pad for LDOs	5.5V	Mandatory
A12	B4	VIN_LDO2_5_7	S	Supply pad for LDOs	5.5V	Mandatory
A4	B8	VIN_LDO3_SW	S	Supply pad for LDO3 switch function	3.6V	Mandatory
B1	B9	VIN_LDO11	S	Supply pad for LDOs	5.5V	Mandatory
A13	C4	LDO0	AO	Output voltage of LDO - NMOS_0.6	VIN_LDO0	Open
B9	A6	LDO1	AO	Output voltage of LDO - PMOS_1	VIN_LDO1_6	Open
A9	B5	LDO2	AO	Output voltage of LDO - PMOS_1	VIN_LDO2_5_7	Open
B6	C7	VIN_LDO3_LV	S	Supply pad for LDO3 NMOS function	3.6V	Open
A2	A9	LDO4	AO	Output voltage of LDO - PMOS_0.6	VIN_LDO3_4	Open
A10	A4	LDO5	AO	Output voltage of LDO - PMOS_0.6	VIN_LDO2_5_7	Open
A7	A5	LDO6	AO	Output voltage of LDO - PMOS_0.6	VIN_LDO1_6	Open
A11	A3	LDO7	AO	Output voltage of LDO - PMOS_0.6	VIN_LDO2_5_7	Open

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
B7	A8	LDO3	AO	Output voltage of LDO - PMOS_1	VIN_LDO8	Open
A5	A7	LDO9	AO	Output voltage of LDO - PMOS_1	VIN_LDO9_10	Open
B8	D6	LDO10	AO	Output voltage of LDO - PMOS_1	VIN_LDO9_10	Open
B5	C8	LDO11	AO	Output voltage of LDO - PMOS_1	VIN_LDO11	Open
B10	A2	ONKEY	DI	Input pin to startup (no pullup/pull down)	5.5V	Define level
F8	C2	ENABLE1	DI	Input pin for transition into and out of deep-sleep mode	VSUP	Define level
E11	D3	ENABLE2	DI	Input pin for control of DCDC0	VSUP	Define level
D8	B2	THERM	DI	Input pin for thermal event	5.5V	Define level
J8	C3	XRES_IN	DI	Input pin for reset during active and stand-by state	VSUP	Define level
L5	F8	XRES_OUT	DO	Push pull to VDD_GPIO_lv	VSUP	Open
L8	D4	AC_OK	DI	Pin to indicate, that the AC adaptor is present	5.5V	Define level
D7		LID	DI	Input pin to indicates LID status of Device	5.5V	Define level
C1	A12	XINT	DO	Push-Pull or open drain output for interrupt detection	VSUP	Open
L9	C10, F3	VSUP_GPIO	S	Supply pin for GPIOs (connect to other VSUP pins)	5.5V	Mandatory
F2	D10	VDD_GPIO_lv	S	Supply pin for GPIOs (connect to typical 1.8V or 3.3)	VSUP	Mandatory
F1		VSS_GPIO	AIO	Analog GND input	-	Mandatory
D6	A10	GPIO0	DIO	General purpose input/output pin	VSUP	Open
G6	E7	GPIO1	DIO	General purpose input/output pin	VSUP	Open

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
D5	D8	GPIO2	DIO	General purpose input/output pin	VSUP	Open
E4	C9	GPIO3	DIO	General purpose input/output pin	VSUP	Open
B3	B10	GPIO4	DIO	General purpose input/output pin	VSUP	Open
C2	A11	GPIO5	DIO	General purpose input/output pin	VSUP	Open
B4	F7	GPIO6	DIO	General purpose input/output pin	VSUP	Open
D2	B12	GPIO7	DIO	General purpose input/output pin	VSUP	Open
H2	D12	V2_5	AO	Output voltage of low power LDO V2_5	3.6V	Mandatory
J4	E11	CREF	AIO	Bypass capacitor for the internal voltage reference; connect 100nF	V2_5	Mandatory
J2	F11	RBIAS	AIO	External resistor; always connect a resistor of 220kΩ (±1%) to VSSA	V2_5	Mandatory
H4		VBAT_BKUP	AIO	Backup battery input	3.6V	Open
A1	G7	VSSA	AIO	Analog GND input	-	Mandatory
A14	G6	VSSA	AIO	Analog GND input	-	Mandatory
J7	E6	VSSA	AIO	Analog GND input	-	Mandatory
P1	F9	VSSA	AIO	Analog GND input	-	Mandatory
P14		VSSA	AIO	Analog GND input	-	Mandatory
F7		VSSA	AIO	Analog GND input	-	Mandatory
D1	B11	CLK32K	DO	32kHz clk output push/pull to VDD_GPIO_lv	VSUP	Open
G1	E10	XIN32K	AIO	Connect to 32kHz crystal oscillator	V2_5	Open
G2	E9	XOUT32K	AIO	Connect to 32kHz crystal oscillator	V2_5	Open
K4		GNDSENSE	AIO	Analog sense GND input (connect to VSSA on WL-CSP)	-	Mandatory

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
E1	C11	OC_PG	DO	Digital Output open drain to indicate over-current/ power_good	VSUP	Open
H1	E12	VSUP_ANA	S	System supply voltage input (connect to other VSUP pins)	5.5V	Mandatory
N6	H8	VSUP_SD2	S	System supply voltage input of Stepdown2 (connect to other VSUP pins)	5.5V	Mandatory
P6	J8	VSUP_SD2	S	System supply voltage input of Stepdown2 (connect to other VSUP pins)	5.5V	Mandatory
N5	G8	LX_SD2	AIO	LX node of Stepdown2	VSUP	Open
N7	G9	LX_SD2	AIO	LX node of Stepdown2	VSUP	Open
P5	H9	LX_SD2	AIO	LX node of Stepdown2	VSUP	Open
P7	J9	LX_SD2	AIO	LX node of Stepdown2	VSUP	Open
N4	H7	VSS_SD2	AIO	Power GND pin of Stepdown2	-	Mandatory
N8	J7	VSS_SD2	AIO	Power GND pin of Stepdown2	-	Mandatory
P4	H10	VSS_SD2	AIO	Power GND pin of Stepdown2	-	Mandatory
P8	J10	VSS_SD2	AIO	Power GND pin of Stepdown2	-	Mandatory
K1	F12	FB_SD2	AIO	Analog Feedback pin of SD2	3.6V	Open
L1	H12	VSUP_SD3	S	System supply voltage input of Stepdown3 (connect to other VSUP pins)	5.5V	Mandatory
L2	J12	VSUP_SD3	S	System supply voltage input of Stepdown3 (connect to other VSUP pins)	5.5V	Mandatory
M1	H11	LX_SD3	AIO	LX node of Stepdown3	VSUP	Open
M2	J11	LX_SD3	AIO	LX node of Stepdown3	VSUP	Open
N1		LX_SD3	AIO	LX node of Stepdown3	VSUP	Open

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
N3	G11	VSS_SD3	AIO	Power GND pin of Stepdown3	-	Mandatory
P2	G12	VSS_SD3	AIO	Power GND pin of Stepdown3	-	Mandatory
P3		VSS_SD3	AIO	Power GND pin of Stepdown3	-	Mandatory
K2	G10	FB_SD3	AIO	Analog Feedback pin of SD3	3.6V	Open
N12	H4	VSUP_SD4	S	System supply voltage input of Stepdown4 (connect to other VSUP pins)	5.5V	Mandatory
P12	J4	VSUP_SD4	S	System supply voltage input of Stepdown4 (connect to other VSUP pins)	5.5V	Mandatory
L10	H2	FB_SD4	AIO	Analog Feedback pin of SD4	3.6V	Open
N14	J3	LX_SD4	AIO	LX node of Stepdown4	VSUP	Open
P13		LX_SD4	AIO	LX node of Stepdown4	VSUP	Open
M13	J2	VSS_SD4	AIO	Power GND pin of Stepdown4	-	Mandatory
M14		VSS_SD4	AIO	Power GND pin of Stepdown4	-	Mandatory
N11	H4	VSUP_SD5	S	System supply voltage input of Stepdown5 (connect to other VSUP pins)	5.5V	Mandatory
P11	J4	VSUP_SD5	S	System supply voltage input of Stepdown5 (connect to other VSUP pins)	5.5V	Mandatory
J1	F10	FB_SD5	AIO	Analog Feedback pin of SD5	3.6V	Open
N10	H5	LX_SD5	AIO	LX node of Stepdown5	VSUP	Open
P10	J5	LX_SD5	AIO	LX node of Stepdown5	VSUP	Open
P9	H6	VSS_SD5	AIO	Power GND pin of Stepdown5	-	Mandatory
N9	J6	VSS_SD5	AIO	Power GND pin of Stepdown5	-	Mandatory
H11	F6	FB_SD0_P	AIO	Positive Feedback of SD0	3.6V	Open

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
J11	H3	FB_SD0_N	AIO	Negative Feedback of SD0	3.6V	Open
E13	E3	CTRL1_SD0	AIO	Bidirectional control pin of SD0, phase 1	VSUP	Open
E14	E2	CTRL2_SD0	AIO	Bidirectional control pin of SD0, phase 2	VSUP	Open
F13	E4	CTRL3_SD0	AIO	Bidirectional control pin of SD0, phase 3	VSUP	Open
F14	E5	CTRL4_SD0	AIO	Bidirectional control pin of SD0, phase 4	VSUP	Open
G13	E1	CTRL5_SD0	AIO	Bidirectional control pin of SD0, phase 5	VSUP	Open
G14	F2	CTRL6_SD0	AIO	Bidirectional control pin of SD0, phase 6	VSUP	Open
H13		CTRL7_SD0	AIO	Bidirectional control pin of SD0, phase 7	VSUP	Open
H14		CTRL8_SD0	AIO	Bidirectional control pin of SD0, phase 8	VSUP	Open
J14	F4	TEMP1_SD0	AIO	Temperature control pin of subdie1 for SD0	VSUP	Open
J13	F1	TEMP2_SD0	AIO	Temperature control pin of subdie2 for SD0	VSUP	Open
K13	F5	TEMP3_SD0	AIO	Temperature control pin of subdie3 for SD0	VSUP	Open
K11		TEMP4_SD0	AIO	Temperature control pin of subdie4 for SD0	VSUP	Open
G9	G4	FB_SD1_P	AIO	Positive Feedback of SD1	3.6V	Open
H9	G5	FB_SD1_N	AIO	Negative Feedback of SD1	3.6V	Open
D13	D2	CTRL1_SD1	AIO	Bidirectional control pin of SD1, phase 1	VSUP	Open
D14	D5	CTRL2_SD1	AIO	Bidirectional control pin of SD1, phase 2	VSUP	Open

Pin Number		Pin Name	I/O	Description	Maximum Voltage	If Not Used
CTBGA	WL-CSP					
K14	G3	TEMP_SD1	AIO	Temperature control pin of subdie1 for SD1	VSUP	Open
F11	G2	FB_SD6_P	AIO	Positive Feedback of SD6	3.6V	Open
G11	G1	FB_SD6_N	AIO	Negative Feedback of SD6	3.6V	Open
C13	C1	CTRL1_SD6	AIO	Bidirectional control pin of SD6, phase 1	VSUP	Open
C14	D1	CTRL2_SD6	AIO	Bidirectional control pin of SD6, phase 2	VSUP	Open
L14	H1	TEMP1_SD6	AIO	Temperature control pin of subdie1 for SD6	VSUP	Open
L13	J1	TEMP2_SD6	AIO	Temperature control pin of subdie2 for SD6	VSUP	Open
D9	C6	PWM_CLK1	DI	PWM input pin for DVM control of SD0	VSUP	Define level
D10	C5	PWM_DAT1	DI	PWM input pin for DVM control of SD0	VSUP	Define level
B11	B1	PWM_CLK2_ ADC1	DI	PWM input pin for DVM control of SD6 or ADC input pin	VSUP	Define level
B12	A1	PWM_DAT2_ ADC2	DI	PWM input pin for DVM control of SD6 or ADC input pin	VSUP	Define level
L7	D9	VBAT	S	High Voltage Supply pin for RTC, and voltage detection	30V	Connect to VSUP
L6	E8	EN5V	DO	Enable pin for external 5V HV stepdown to supply VSUP rails	V2_5	Open

Pin Description: This table shows the pin description for the CTBGA as well as the WL-CSP package including information of the I/O type, protection and handling if the function block is not used.

Absolute Maximum Ratings

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Electrical Characteristics is not implied. Exposure to absolute maximum rating conditions for periods may affect device reliability.

Figure 7:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
	Supply Voltage to Ground 30V pins	-0.5	32	V	Applicable for pin VBAT
	Supply Voltage to Ground 5V pins	-0.5	7.0	V	Applicable for pins VSUP_SDx, VSUP_ANA, ONKEY, VSUP_GPIO, VIN_LDOx, LDO6 (switch mode), THERM, AC_OK, LID
	5V pins with protection to VSUP	-0.5	VSUP_x	V	Applicable for pins SCL_SCLK, SDA_SDI, SCSB, SDO, XINT, VDD_GPIO_LV, GPIOx, CLK32K, OC_PG, LX_SDx, CTRLx, XRES_IN/OUT, ENABLEx, PWMx
	Supply Voltage to Ground 3V pins	-0.5	5.0	V	Applicable for pins V2_5, VBAT_BKUP, VIN_LDO3_LV/SW
	3V pins with protection to VIN_LDOx	-0.5	5.0 or VIN_LDOx	V	Applicable for pins LDOx
	3V pins with protection to VSUP	-0.5	5.0 or VSUP_x	V	Applicable for pins TEMPx, FB_SDx
	3V pins with protection to V2_5	-0.5	V2_5	V	Applicable for pins CREF, RBIAS, XIN32K, XOUT32K, EN5V
	Voltage Difference between Ground Terminals	-0.3	0.3	V	Applicable for pins VSSx, VSSA, GNDSENSE
I_{SCR}	Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC JESD78

Symbol	Parameter	Min	Max	Units	Comments
Continuous Power Dissipation (T_A = 70°C)					
P_T	Continuous power dissipation		1.4	W	P_T[(1)] for CTBGA124 package (R_{THJA} ~ 38K/W)
P_T	Continuous power dissipation		1.3	W	P_T[(1)] for WL-CSP108 package (R_{THJA} ~ 40K/W)
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	±1.5		kV	Norm: JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
T_A	Operating Temperature	-40	85	°C	
T_J	Junction Temperature		125	°C	
T_{STRG}	Storage Temperature Range	-55	125	°C	
T_{BODY}	Package Body Temperature		260	°C	Norm IPC/JEDEC J-STD-020[(2)]
RH_{NC}	Relative Humidity non-condensing	5	85	%	
MSL	Moisture Sensitivity Level	3			for CTBGA, represents a max. floor life time of 168h
		1			for WL-CSP, represents an unlimited max. floor life time
Bump Temperature (CTBGA Soldering)					
T_{PEAK}	Soldering Profile	235	245	°C	Peak Temperature
t_{WELL}		30	45	s	Well Time above 217°C

Note(s) and/or Footnote(s):

1. Depending on actual PCB layout and PCB used
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices"

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 8:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT	Battery Voltage		2.5	3.6	30	V
VSUPx	Supply Voltage		2.5	3.6	5.5	V
VBAT_BKUP	Backup-Battery Voltage		2.5	3	3.6	V
VDD_GPIO_lv	Alternative GPIO Supply Voltage		1.7	1.8	3.6	V
VINLDO0	Supply Voltage for LDO0		1.15	3.6	5.5	V
VINLDO1-11	Supply Voltage for LDO1 to LDO11		1.7	3.6	5.5	V
VINLDO3_LV	Supply Voltage for LDO3 NMOS		1.2		3.6V	V
VINLDO3_SW	Supply Voltage for LDO3 switch		0.6		1.5V	V
V2_5	Voltage on Pin V2_5		2.4	2.5	2.6	V
$I_{quiescent}$	Quiescent current	@ VSUPx = 3.8V, no regulator enabled only V2_5 on, digital part, bias and references running		310		µA
I_{low_power1}	Low Power current	as above but, low_power=1		265		µA
I_{low_power2}	Low Power current	As above, but low_power=1; clk_div=1		160		µA
I_{power_off}	Power-Off current	All regulators off V2_5 on		10		µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Digital Input Pin Characteristics						
V_{IL}	Low Level input voltage	ONKEY, XRES_IN	–0.3		0.4	V
V_{IH}	High Level input	XRES_IN, ENABLEx	1.4		V_{VSUP_GPIO}	V
V_{IH_noprot}	High Level input	ONKEY, THERM, AC_OK, LID	1.4		5.5V	V
Digital Output Pin Characteristics						
V_{OL}	XRES_OUT Low-Level Output Voltage	XRES_OUT; XINT, OC_PG at 2.0mA			0.2 x $V_{VDD_GPIO_lv}$	V
V_{OH}	XRES_OUT High-Level Output Voltage	XRES_OUT; XINT (if on push pull mode), OC_PG, SDO at -1.0mA	0.8 x $V_{VDD_GPIO_lv}$			V
V_{OL_EN5V}	Low-Level Output Voltage	EN_5V at 0.1mA			0.2 x V_{V2_5}	V
V_{OH_EN5V}	High-Level Output Voltage	EN_5V at -0.1mA	0.8 x V_{V2_5}			V
$I_{LEAKAGE}$	Leakage current	high impedance			10	µA
R_{PULLUP}	Internal pull-up to VDD_GPIO_lv	XINT=2V, VDD_GPIO_LV=3V (XINT in open-drain mode)	33		91	kΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GPIO Pin Characteristics						
V_{IL}	Low level input voltage	digital input	-0.3		0.4	V
V_{IH}	High level input voltage	digital input	1.4		$V_{VDD_GPIO_lv}$ or V_{VSUP_GPIO}	V
V_{OL}	Low level output voltage	GPIO, I_{OL}=+2mA; digital output			0.2 x $V_{VDD_GPIO_lv}$ or V_{VSUP_GPIO}	V
V_{OH}	High level output voltage	GPIO, I_{OH}=–1mA; digital push-pull output	0.8 x$V_{VDD_GPIO_lv}$ or V_{VSUP_GPIO}		$V_{VDD_GPIO_lv}$ or V_{VSUP_GPIO}	V
$I_{LEAKAGE}$	Leakage current	high impedance			10	µA
$R_{pull-up}$	Pull-up resistance	if enabled; VSUP_GPIO=3.6V		300		kΩ
$R_{pull-down}$	Pull-down resistance	if enabled; VSUP_GPIO=3.6V		300		kΩ
R_{NMOS}	NMOS resistance	VSUP_GPIO>=3.3V			50	Ω

Electrical Characteristics: VSUPx=+2.7V...+5.5V, TA = -40ºC...85ºC. Typical values are at VSUPx=+3.6V, TA= 25ºC, unless otherwise specified.

Typical Operating Characteristics

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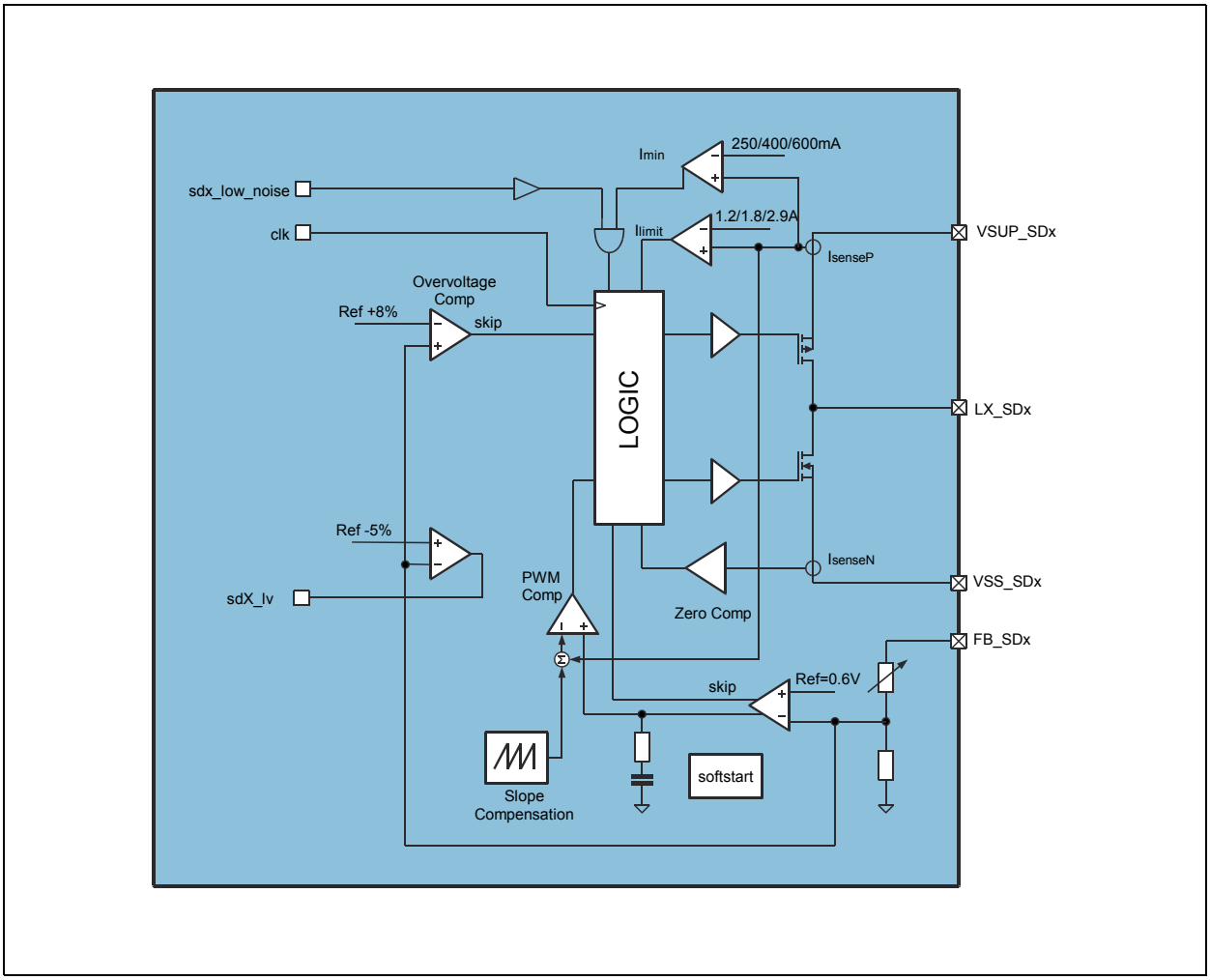
Detailed Descriptions-Power Management Functions

DCDC Step-Down Converter

Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 1.5A (SD4, SD5), 2A (SD3) and 5A for SD2, with an output capacitor of only 8-27µF. The implemented current limitation protects the DCDC and the coil during overload condition.

Figure 9:
Step Down DC/DC Converter Block Diagram



DCDC Step Down Converter Block Diagram: Shows the internal structure of the DCDC bucks.

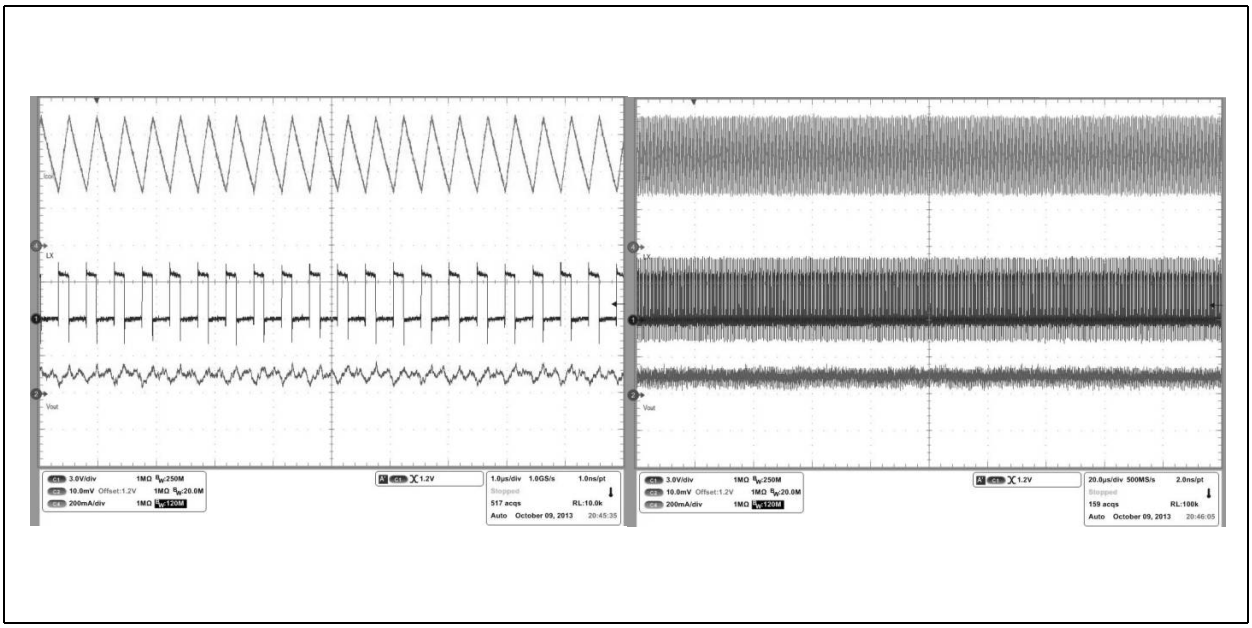
Mode Settings

Low Ripple, Low Noise Operation

Bit settings: *sdX_low_noise*=1

In this mode there is no minimum coil current necessary before switching off the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode.

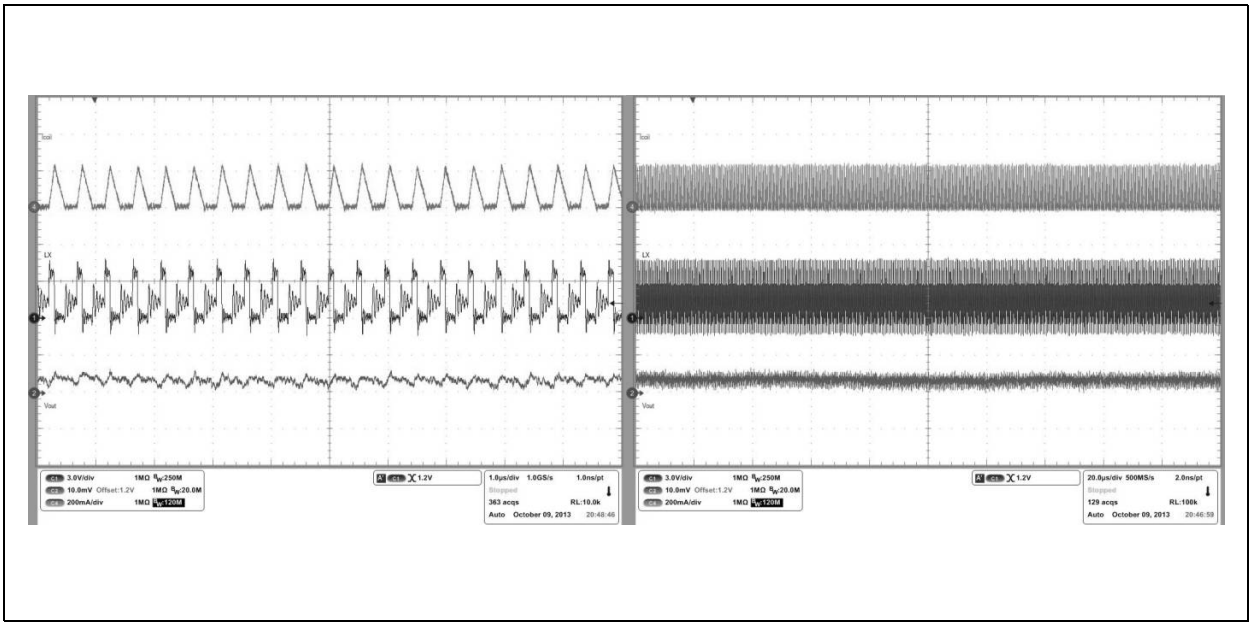
Figure 10:
DC/DC Buck Continuous Mode



DC/DC Buck Continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 500mA.

When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to tmin_on to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

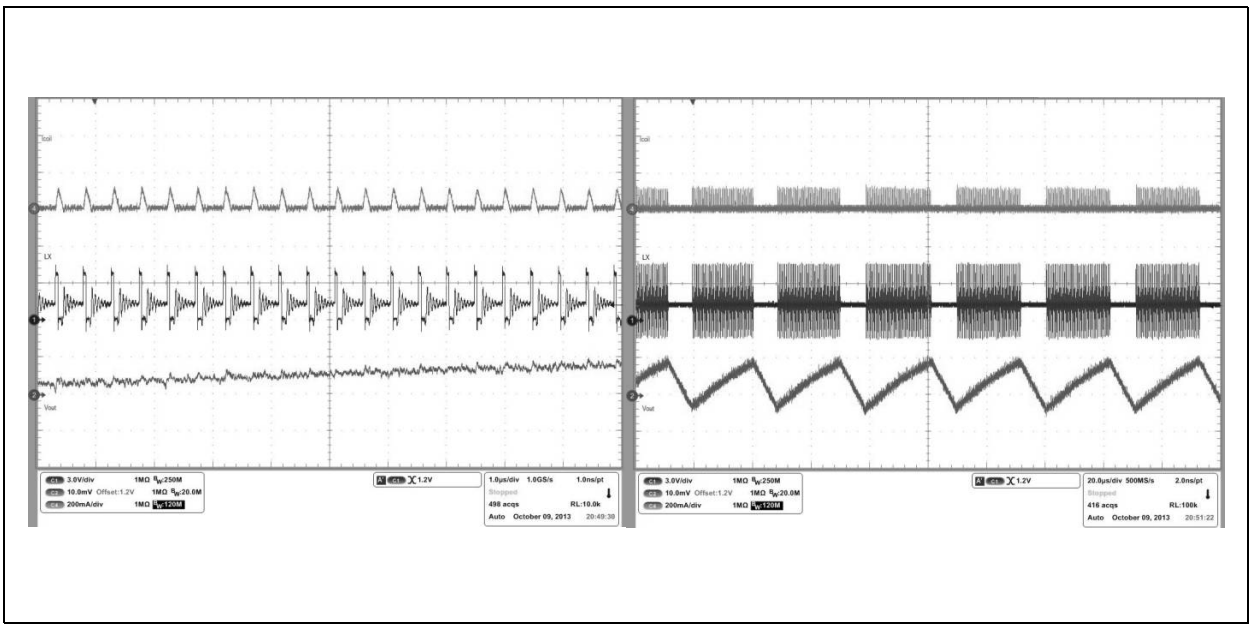
Figure 11:
DC/DC Buck Dis-Continuous Mode



DC/DC Buck Dis-Continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 60mA.

Only in the case the load current gets so small that less than the minimum on-time of the PMOS would be needed to keep the loop in regulation the regulator will enter power save operation and skip pulses during this time. The crossover point is about ~1% of the DCDC current limit.

Figure 12:
DC/DC Buck Dis-Continuous & Low Power Mode



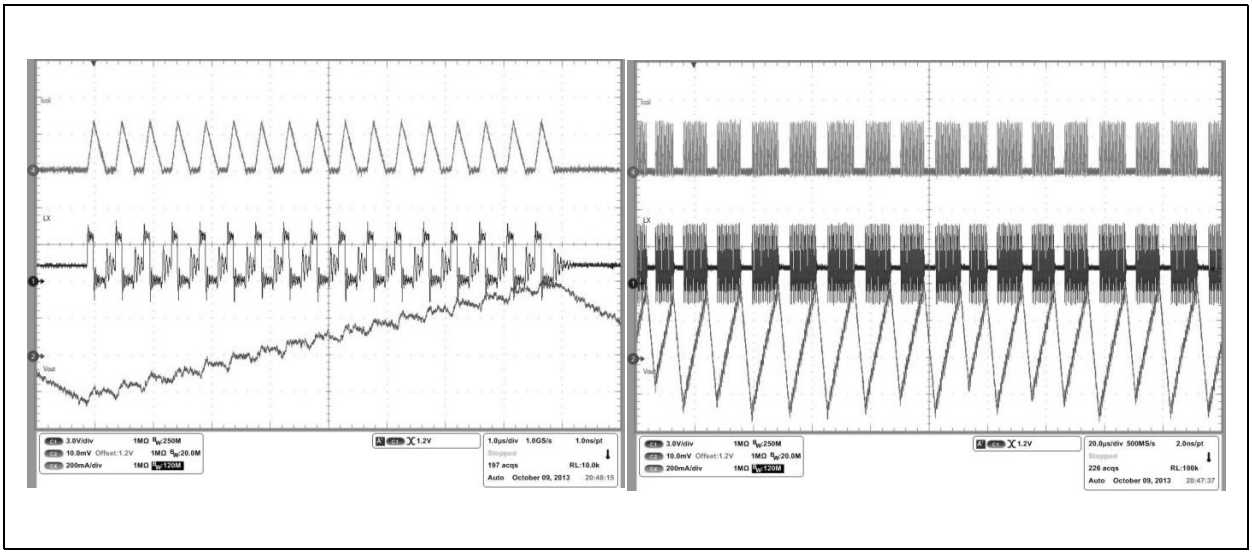
DC/DC Buck Dis-Continuous & Low Power Mode: Shows the DC/DC switching waveforms of for SD5 at about 10mA.High efficiency operation (default setting):

Bit settings: *sdX_low_noise*=0

In this mode there is a minimum coil current necessary before switching off the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to higher output currents.

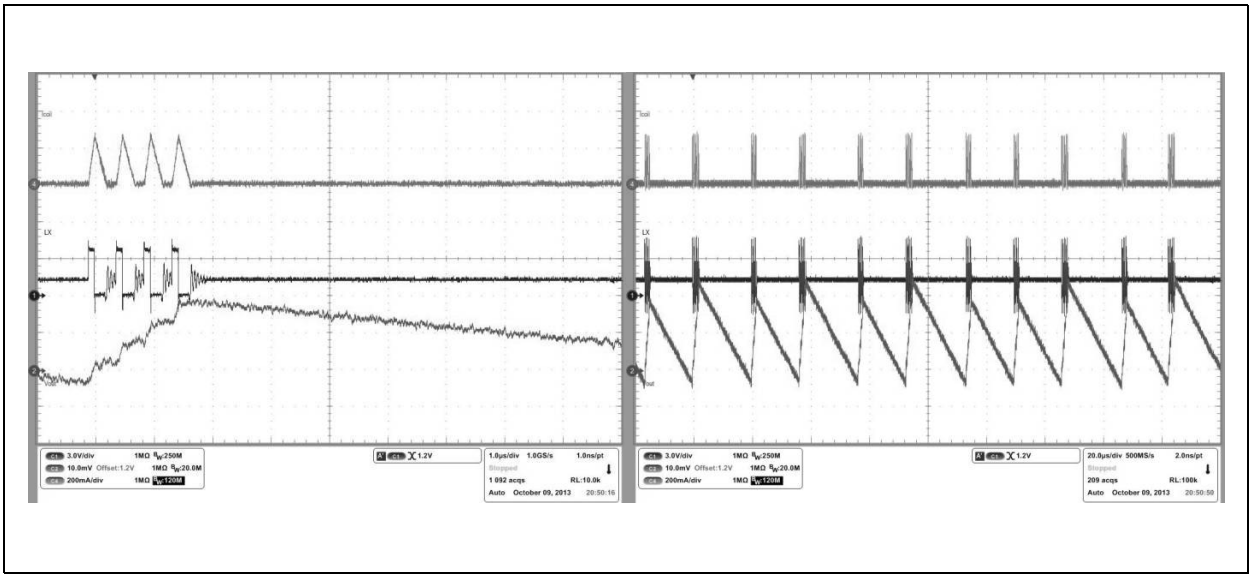
The crossover point to power save operation is already reached at reasonable high output currents (~10% of the DCDC current limit).

Figure 13:
DC/DC Buck Dis-Continuous Mode & High Efficiency 1/2



DC/DC Buck Dis-Continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 60mA with the low_noise bit deactivated.

Figure 14:
DC/DC Buck Dis-Continuous Mode & High Efficiency 2/2



DC/DC Buck Dis-Continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 10mA with the low_noise bit deactivated.

It's possible to switch between these two modes during operation.

Power Save Operation (Automatically Controlled)

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/under-shoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a bigger output capacitor to guarantee the stability of the regulator. The mode is enabled by setting *sdX_fast* =1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency for SD2, SD3, SD4 and SD5 can be set to 3 or 4MHz. This mode is selected by setting *sdX_freq* to the appropriate value.

100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

Step-Down Converter Configuration Modes

The step down dc/dc converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit *sd3_slave*, *sd4_slave* and *sd5_slave* (the default is set by the Boot-OTP). It's not allowed to set *sd3_slave* and *sd4_slave* at the same time.

Figure 15:
DC/DC Buck Converter Normal Operation

DC/DC Buck Normal Operation: Shows the internal DC/DC buck converters in normal operation independent from each other; no slave mode set

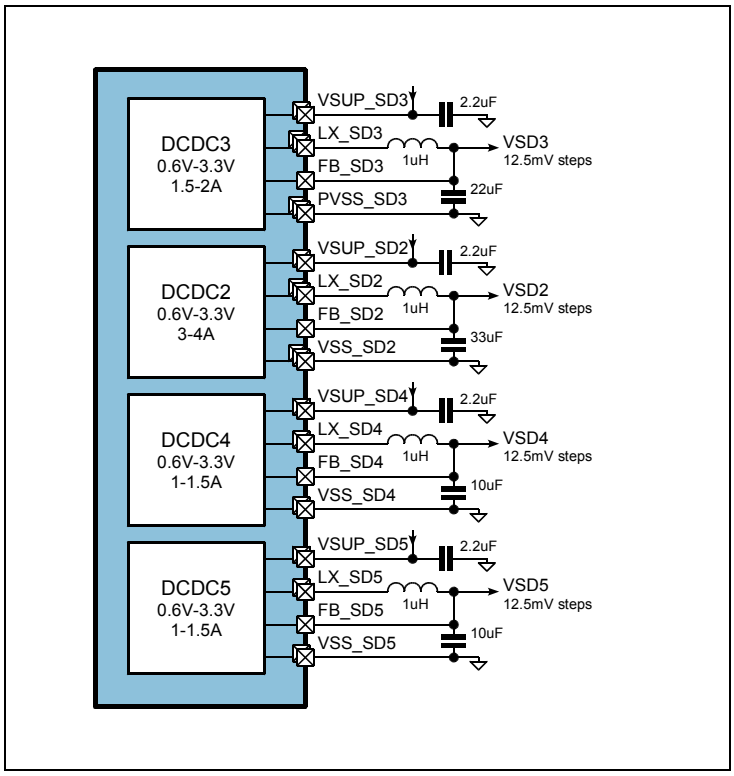


Figure 16:
DC/DC Buck Converter SD4+SD5 (2-3A) Mode

DC/DC Buck Slave Operation: Shows the internal DC/DC buck converters with SD5 operating as slave of SD4 to increase the output current. (*sd5_slave* = 1)

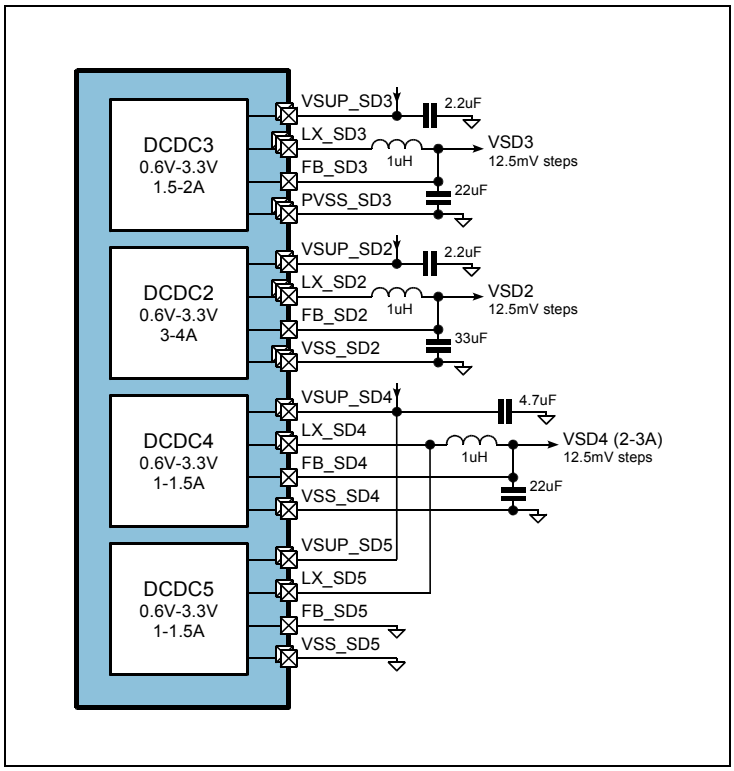


Figure 17:
DC/DC Buck Converter SD2+SD4 (4-5.5A) Mode

DC/DC Buck Slave Operation: Shows the internal DC/DC buck converters with SD4 operating as slave of SD2 to increase the output current.
(*sd4_slave* = 1)

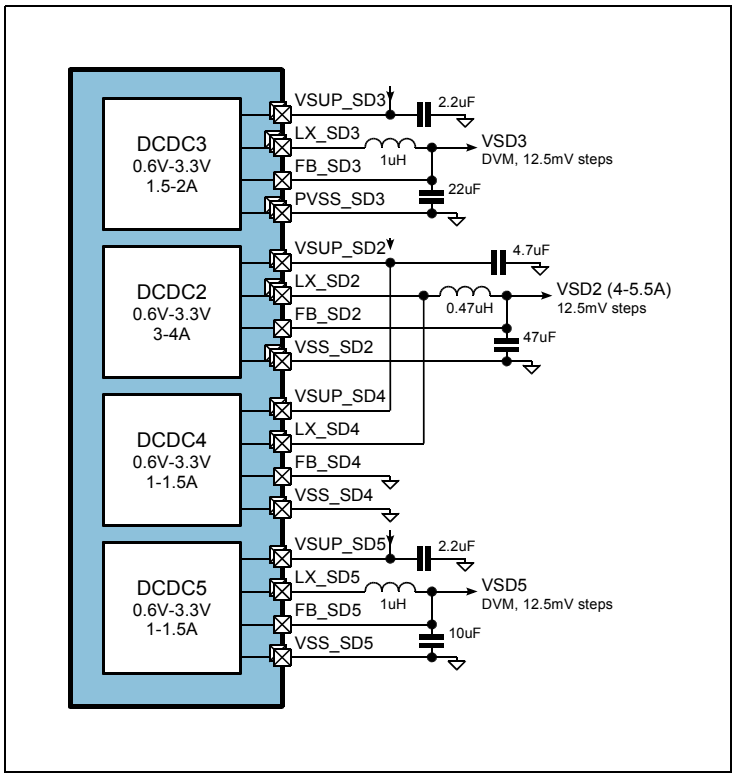
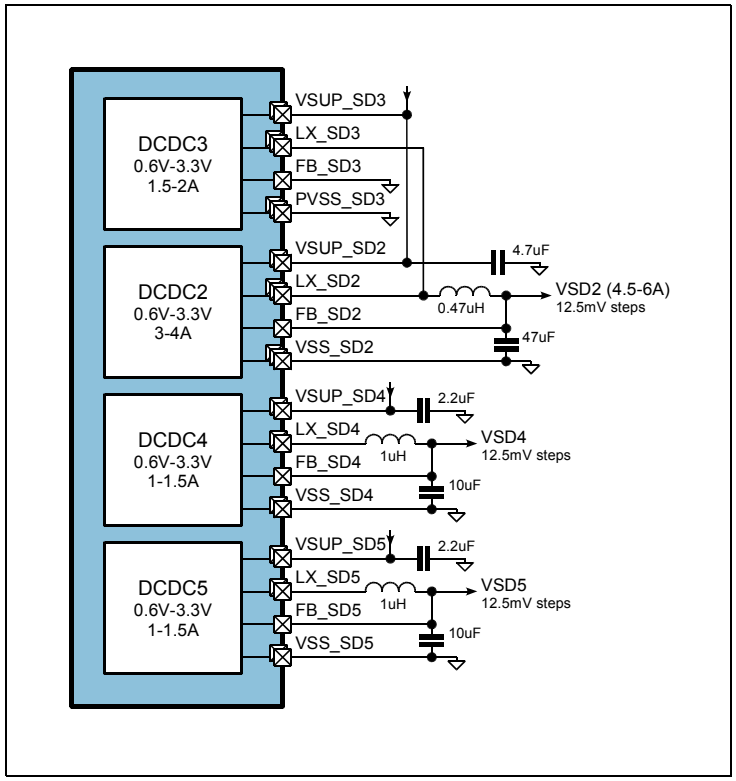


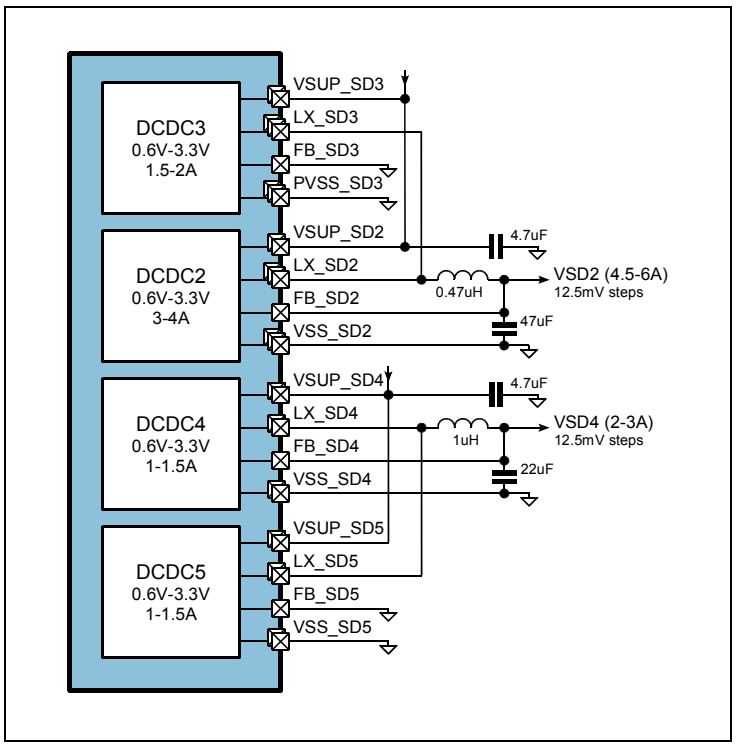
Figure 18:
DC/DC Buck Converter SD2+SD3 (4.5-6A) Mode

DC/DC Buck Slave Operation: Shows the internal DC/DC buck converters with SD3 operating as slave of SD2 to increase the output current.
(*sd3_slave* = 1)



DC/DC Buck Slave Operation: Shows the internal DC/DC buck converters with SD3 operating as slave of SD2 and SD5 operating as a slave from SD4 to increase the output current.
(*sd3_slave* = 1 & *sd5_slave*=1)

Figure 19:
DC/DC Buck Converter SD2+SD3 & SD4+SD5 Mode



Parameter

Figure 20:
DC/DC Buck Converter Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage	Pin VSUP_SDx	2.7		5.5	V
V_{OUT}	Regulated output voltage		0.6125		3.35	V
V_{OUT_tol}	Output voltage tolerance	min. 30mV	-3		+3	%
I_{LOAD_SD2}	Load current SD2	VSD2 ≤1.8V	0		5	A
		VSD2 >1.8V	0		3	A
I_{LOAD_SD3}	Load current SD3	VSD3 ≤1.8V	0		2	A
		VSD3 >1.8V	0		1.5	A
I_{LOAD_SD45}	Load current SD4,5	VSD4/5 ≤1.8V	0		1.5	A
		VSD4/5 >1.8V	0		1	A
I_{LIMIT}	Current limit	SD2 (sd2_hicurr=1)		6		A
		SD3		2.5		A

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		SD4, SD5		1.8		A
R_{PSW}	P-Switch ON resistance incl. bonds, substrate, etc	SD2; VSUP_SDx=3.0V		78	100	mΩ
		SD3; VSUP_SDx=3.0V		156	200	mΩ
		SD4, SD5; VSUP_SDx=3.0V		225	300	mΩ
R_{NSW}	N-Switch ON resistance incl. bonds, substrate, etc	SD2; VSUP_SDx=3.0V		50	70	mΩ
		SD3; VSUP_SDx=3.0V		100	130	mΩ
		SD4, SD5; VSUP_SDx=3.0V		140	190	mΩ
f_{SW}	Switching frequency	sdX_frequ=1; fclk_int =4MHz		4		MHz
		sdX_frequ=0; fclk_int =4MHz		3		MHz
ηeff	Efficiency	see figures below				%
I_{VDD}	Current consumption	Operating current without load		60		µA
R_{DIS}	discharge resistance	SD2 off; Vout=1V		90		Ω
		SD3/4/5 off; Vout=1V		160		Ω

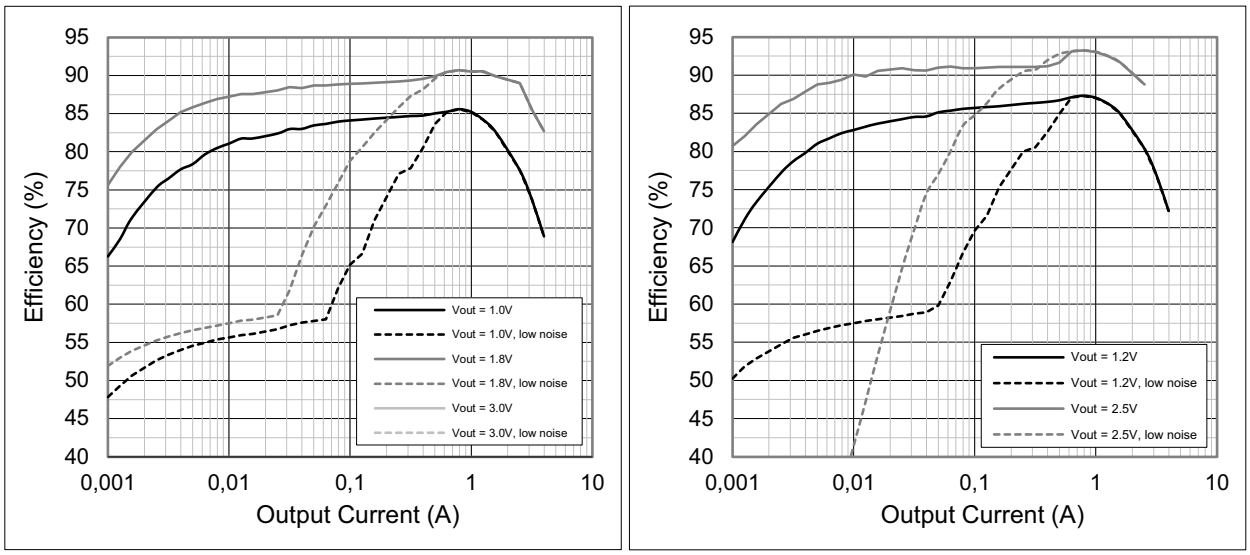
DC/DC Buck Converter Parameter: Shows the key electrical parameter of the internal DC/DC buck converters

Figure 21:
DC/DC Buck Converter External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{FB_SD2}	Output capacitor	Ceramic X5R or X7R	27			µF
	Output capacitor, sd2_fast=1	Ceramic X5R or X7R	54			µF
C_{FB_SD3}	Output capacitor	Ceramic X5R or X7R	12			µF
	Output capacitor, sd3_fast=1	Ceramic X5R or X7R	27			µF
C_{FB_SD4-5}	Output capacitor	Ceramic X5R or X7R	8			µF
	Output capacitor sd4_fast=1 or sd5_fast=1	Ceramic X5R or X7R	18			µF
C_{VSUP_SD2}	Input capacitor	Ceramic X5R or X7R	7			µF
C_{VSUP_SD3}	Input capacitor	Ceramic X5R or X7R	3.5			µF
C_{VSUP_SD4-5}	Input capacitor	Ceramic X5R or X7R	2.2			µF
$L_{SD2-SD5}$	Inductor		0.5	1		µH
$L_{SD2-SD3}$	Inductor	V_{OUT}<=1.8V	0.3	0.47		µH

DC/DC Buck Converter External Components: Shows the external component parameter of the internal DC/DC buck converters

Figure 22:
DC/DC Buck SD2 Efficiency vs. Output Current



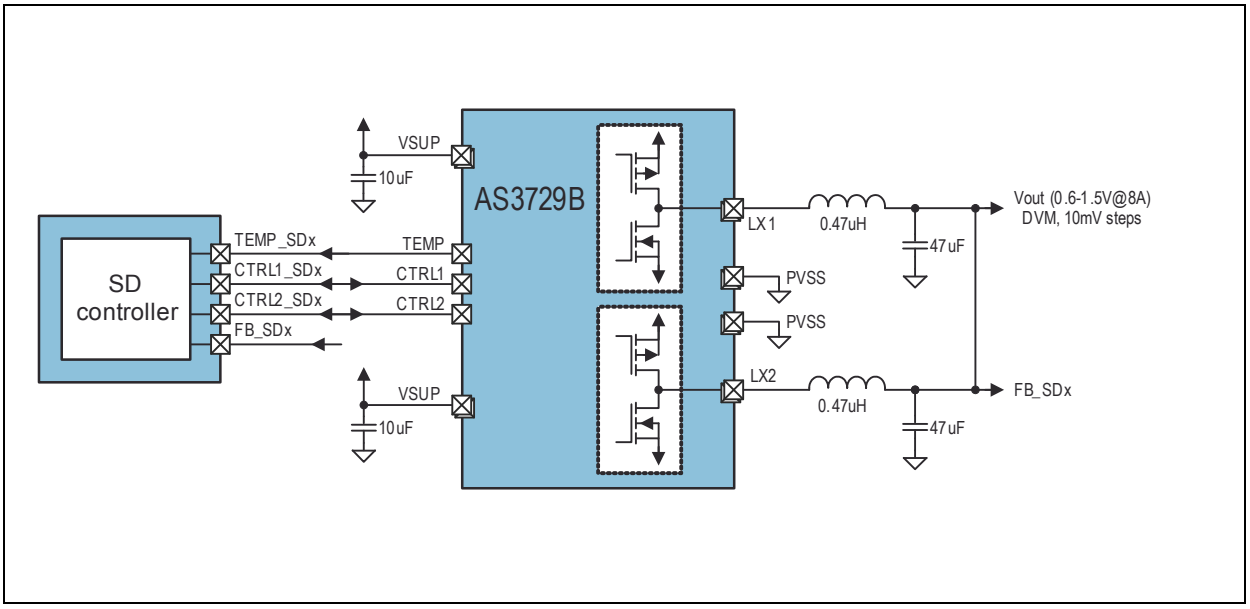
DC/DC Buck SD2 Efficiency: Shows efficiency of the internal SD2 buck converter @ 1.0V, 1,2V, 1.8V, 2,5V& 3.0V with VSUP=3.8V, 3MHz operation and T_A=25°C

DCDC Step-Down Controller

Description

The Step-Down controller SD1 and SD6 are dual phase controller using an external power-stage incorporating 2 phases to achieve higher output currents. The maximum output current when using the AS3729 power stage is 6A (peak) with having 3A (peak) per phase. When using the AS3729B power stage, the current can be up to 4A (peak) per phase. This allows the use of low profile coils without compromising on performance.

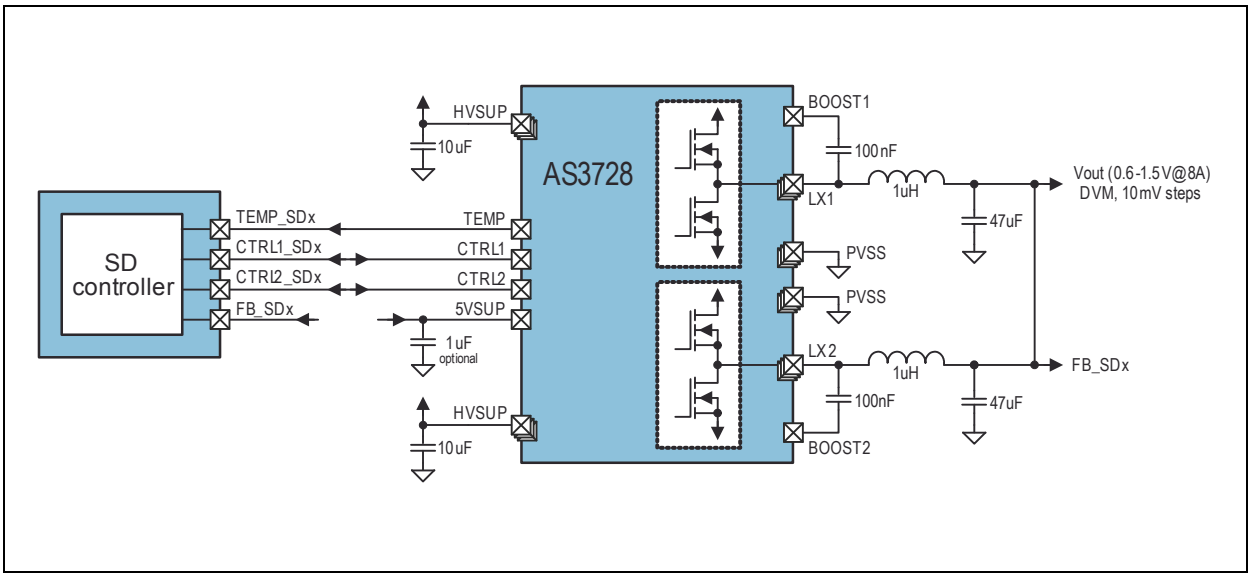
Figure 23:
SD1 DC/DC Buck Controller 8A Peak Block Diagram



SD1 DC/DC Buck Controller: Shows basic connection of the SD1 controller to the external power stage (AS3729B) for 8Apeak output current.

When using the AS3728 power stage a dual phase controller can support up to 8A (4A per phase). The AS3728 is a HV power stage being capable of operating from input voltage up to 14V for multi-cell designs.

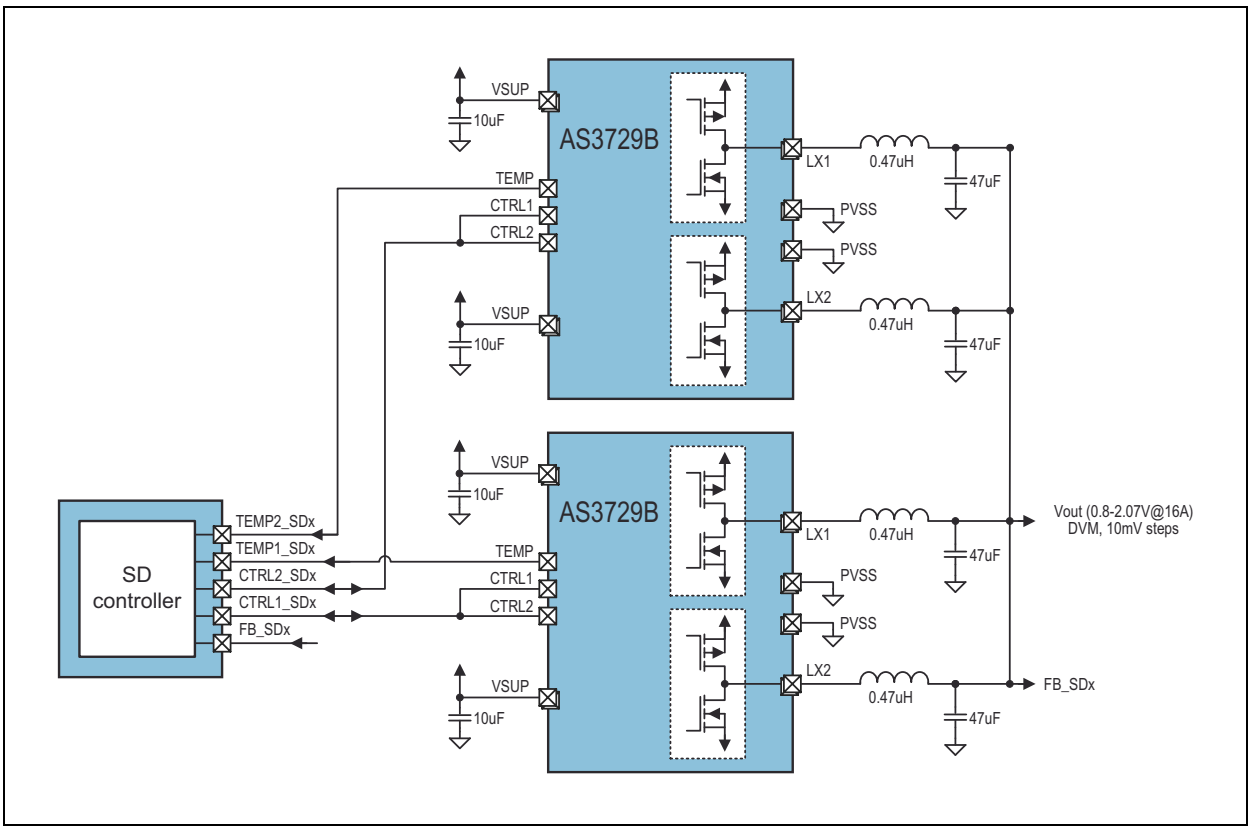
Figure 24:
SD1 DC/DC Buck Controller 8A Block Diagram



SD1 DC/DC Buck Controller: Shows basic connection of the SD1 controller to the external power stage (AS3728) for 8A output current.

Step-Down controller SD6 can be used in a special mode using 2 phases with 2 power stages which provides up to 12Arms but requires coils capable of supporting 6Arms each.

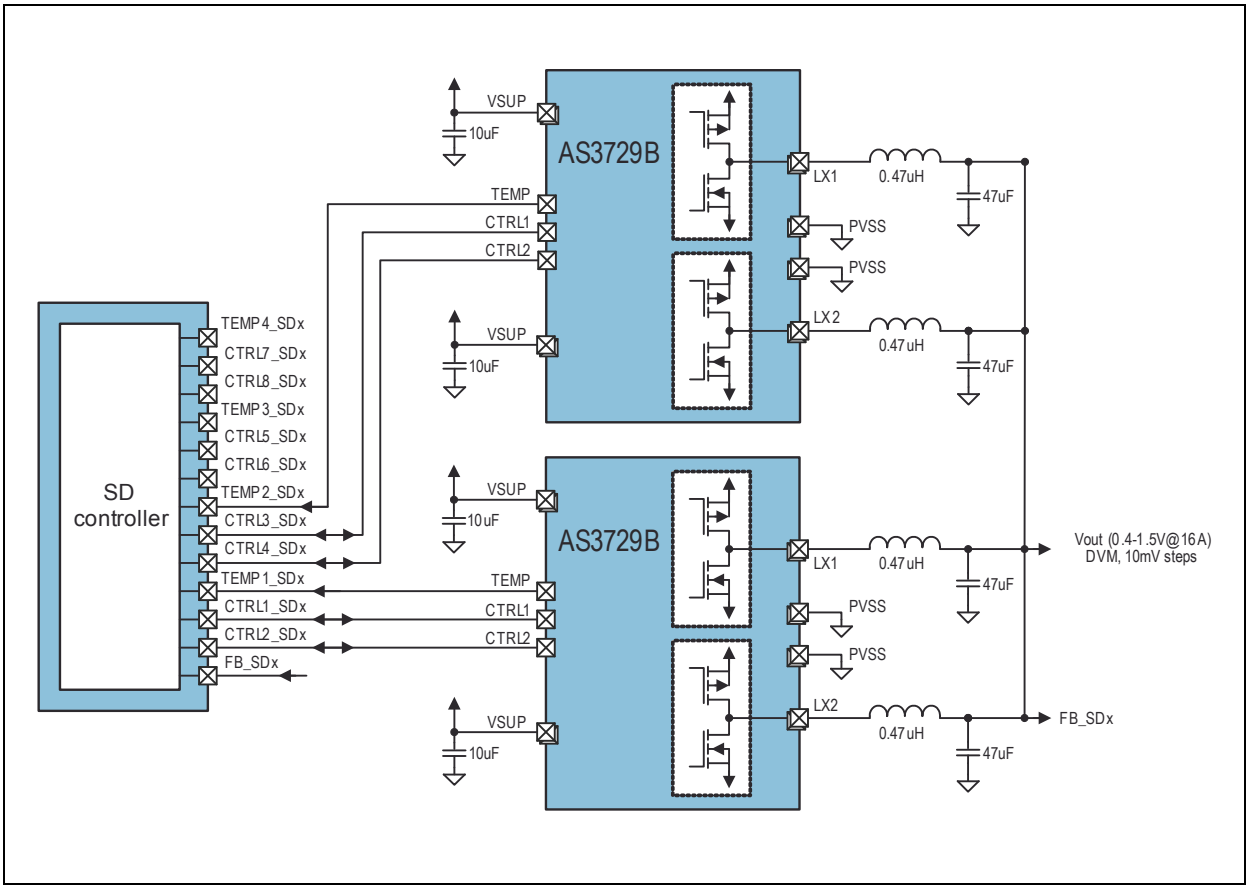
Figure 25:
SD6 DC/DC Buck Controller 16A Block Diagram



SD6 DC/DC Buck Controller: Shows basic connection of the SD6 controller to two external power stages (AS3729B) for 16A output current.

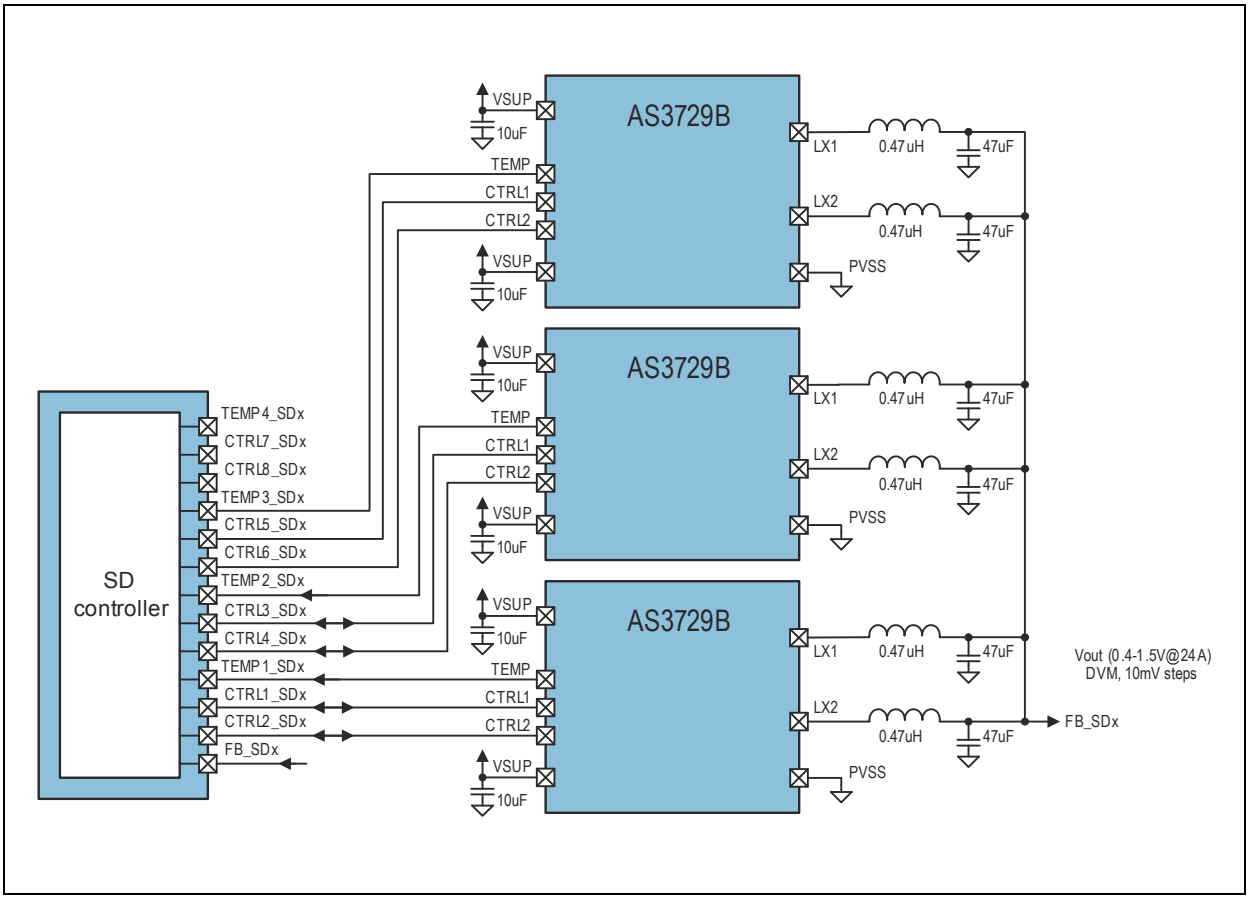
The Step-Down controller SD0 is a multi-phase controller which can use up to 4 power stages (8 phases) with a maximum output current of 20Arms. The output current is easily scalable by varying the number of phases and power-stages from 2.5Arms to 20Arms.

Figure 26:
SD0 DC/DC Buck Controller 16A Block Diagram



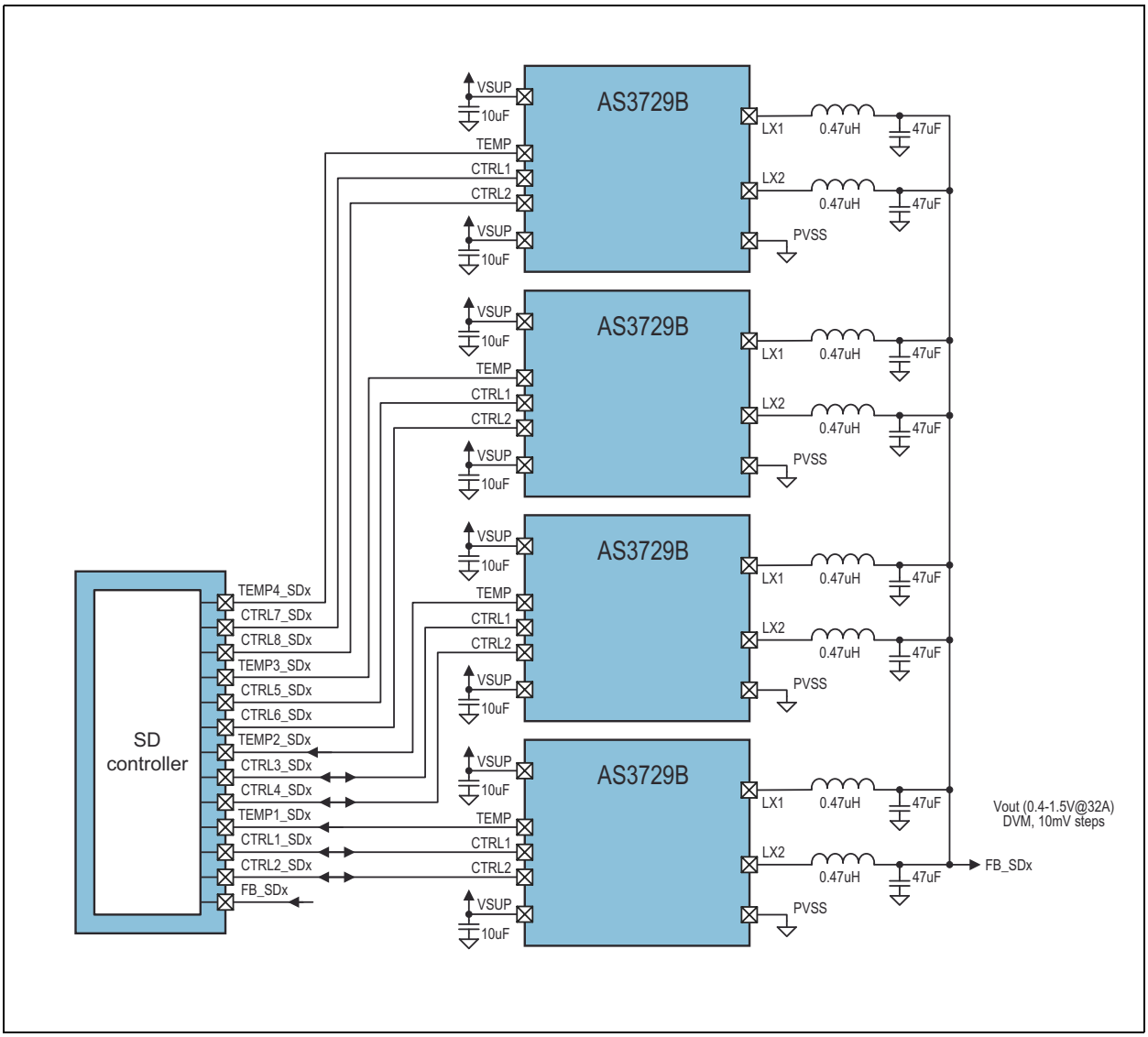
SD0 DC/DC Buck Controller: Shows basic connection of the SD0 controller to two external power stages (AS3729B) for 16A output current.

Figure 27:
SD0 DC/DC Buck Controller 24A Block Diagram



SD0 DC/DC Buck Controller: Shows basic connection of the SD0 controller to three external power stages (AS3729B) for 24A output current.

Figure 28:
SD0 DC/DC Buck Controller 32A Block Diagram



SD0 DC/DC Buck Controller: Shows basic connection of the SD0 controller to four external power stages (AS3729B) for 32A output current.

Mode Settings

Low Ripple, Low Noise Operation

Bit settings: *sdX_low_noise*=1

In this mode there is no minimum coil current necessary before switching off the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to tmin_on to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

Only in the case the load current gets so small that less than the minimum on-time of the PMOS would be needed to keep the loop in regulation the regulator will enter low power mode operation. The crossover point is about ~1% of the DCDC current limit.

High Efficiency Operation (Default Setting)

Bit settings: *sdX_low_noise*=0

In this mode there is a minimum coil current necessary before switching off the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to a higher output current.

The crossover point to low power mode is already reached at reasonable high output currents (~10% of the DCDC current limit).

It's possible to switch between these two modes during operation.

Low Power Operation (sdX_low_power=1)

In this mode the controller is only running on a single phase. Only one output stage of the external power stage is used to reduce the power consumption for e.g. a stand-by mode operation.

Power Save Operation (Automatically Controlled)

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/under-shoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

Force PWM Mode Operation

Even in the case the load current gets so small that less than the minimum on-time of the PMOS would be needed to keep the loop in regulation the regulator will still stay on the fixed switching frequency without entering low power mode. To guarantee a stable output voltage also negative coil currents are possible. This mode guarantees the lowest possible ripple and a fixed frequency over all load conditions for powering noise sensitive RF circuits, but is compromising on the efficiency. The mode is enabled by setting *sdX_force_pwm* =1.

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a bigger output capacitor to guarantee the stability of the regulator. The mode is enabled by setting *sdX_fast* =1.

100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

DVS (Dynamic Voltage Setting)

For a quick change of output voltage a dedicated PWM interface can be used for SD0 and SD6. Please refer to PWM Control Interface chapter for more details.

DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down controllers, but only for one at a time. (see *dvm_time_SDx* description)

Automatic Phase Shedding

SD0, SD1 and SD6 allow automatic phase shedding which can be enabled with *sdX_phsw_on*. For SD0 a minimum number of phases for this automatic phase shedding can be defined with *sd0_nph_min*.

Parameter

Figure 29:
DC/DC Buck Controller Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage	Pin VSUP_SDx	2.5		5.5	V
V_{OUT}	Regulated output voltage		0.61		1.5	V
V_{OUT_tol}	Output voltage tolerance	min. 20mV	-2		+2	%
f_{SW}	Switching frequency	fclk_int = 4MHz		2.7	3	MHz

DC/DC Buck Controller Parameter: Shows the key electrical parameter of the DC/DC buck controller

Figure 30:
DC/DC Buck Controller External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External Components 6A						
AS3729	# power stages		1			
C_{FB}	Output capacitor	Ceramic X5R or X7R, high performance	40	47		µF
		Ceramic X5R or X7R, cost optimized	20	22		µF
C_{VSUP_SDx}	Input capacitor	Ceramic X5R or X7R	6	10		µF
L_{SDx}	Inductor	4A rated, 3MHz operation, low Ron	0.3	0.47		µH
External Components 8A (HV)						
AS3728	# power stages		1			
C_{FB}	Output Capacitor	Ceramic X5R or X7R / 6.3V high performance	64	82		µF
		Ceramic X5R or X7R / 6.3V cost optimized	32	47		µF
C_{HVSUP}	HV Input Capacitor	Ceramic X5R or X7R / 25V	10	22		µF
C_{BOOST}	Boost Capacitor	Ceramic X5R or X7R / 6.3V		100		nF
C_{5VSUP}	5V Supply Capacitor	Ceramic X5R or X7R / 6.3V		1		µF
L	Inductor	5A rated, 1MHz operation, low R_{ON}	0.5	1		µH

DC/DC Buck Controller External Components: Shows the external component parameter of the DC/DC buck controllers

Figure 31:
SD0 Efficiency vs. Output Current Combined Mode

DC/DC Buck SD0 Efficiency: Shows efficiency of the SD0 buck controller with VSUP=3.7V, 1.35MHz operation, T_A=25°C and Coilcraft XAL5030-601MEB coil.

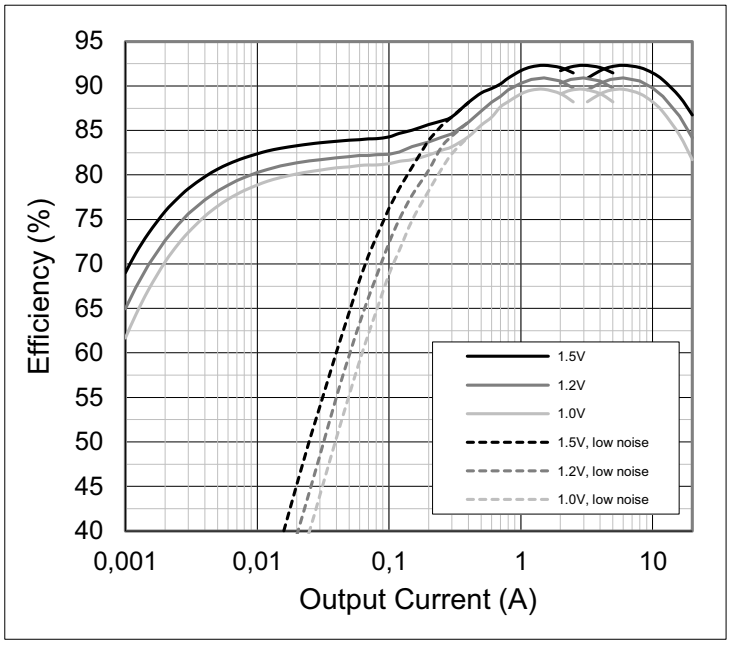


Figure 32:
SD1 3.7V Eff vs. Iout Mode and Coil Comparison 1/2

DC/DC Buck SD1 Efficiency: Shows efficiency of the SD1 buck controller in dual and combined mode @ 1.2V with VSUP=3.7V, 1.35MHz operation, T_A=25°C and TDK TFM coils.

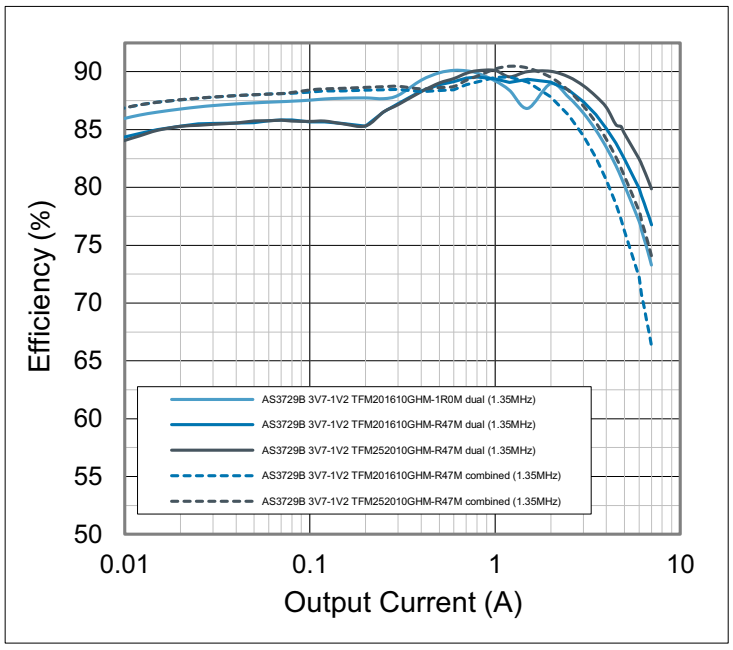


Figure 33:
SD1 3.7V Eff vs. Iout Mode and Coil Comparison 2/2

DC/DC Buck SD1 Efficiency: Shows efficiency of the SD1 buck controller in dual and combined mode @ 1.2V with VSUP=3.7V, 1.35MHz operation, T_A=25°C and Toko DEF coils.

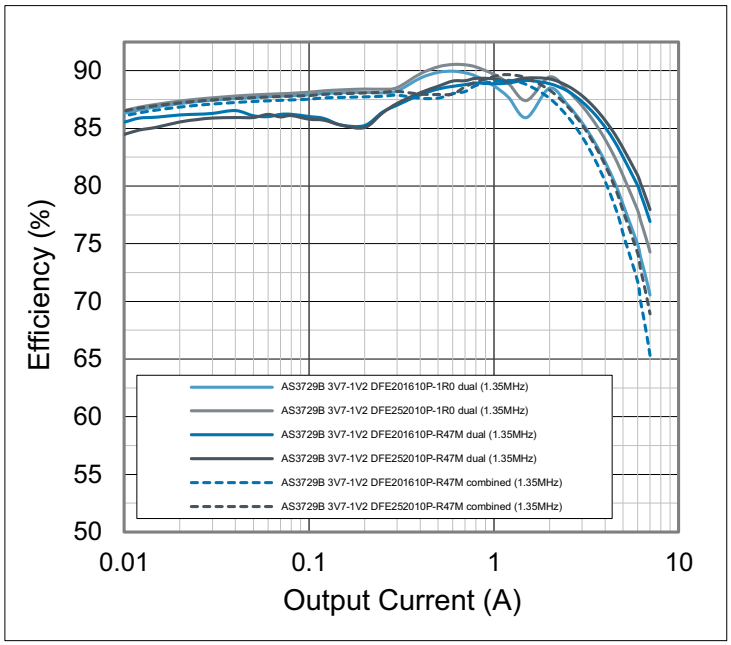


Figure 34:
DC/DC Buck SD0 Load Transient Fast Mode

DC/DC Buck SD0 Load Transient: Shows the response of the SD0 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=1, C_{OUT}=88uF and T_A=25°C

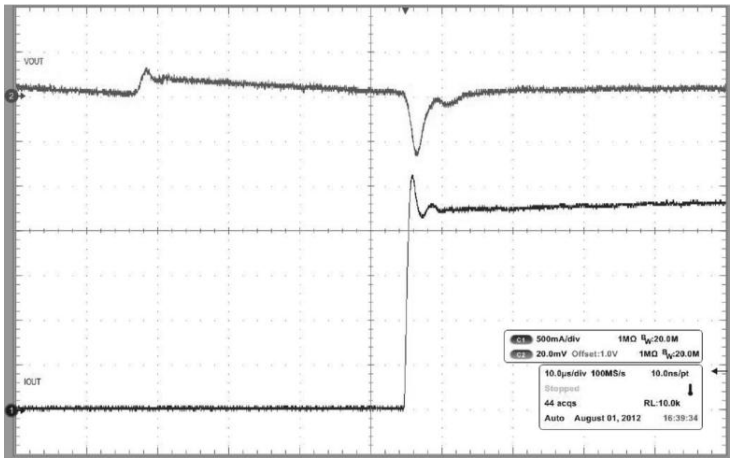


Figure 35:
DC/DC Buck SD0 Low Noise Load Transient Fast Mode

DC/DC Buck SD0 Low Noise Load Transient: Shows the response of the SD0 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=1, C_{OUT}=88uF, low_noise=1 and T_A=25°C

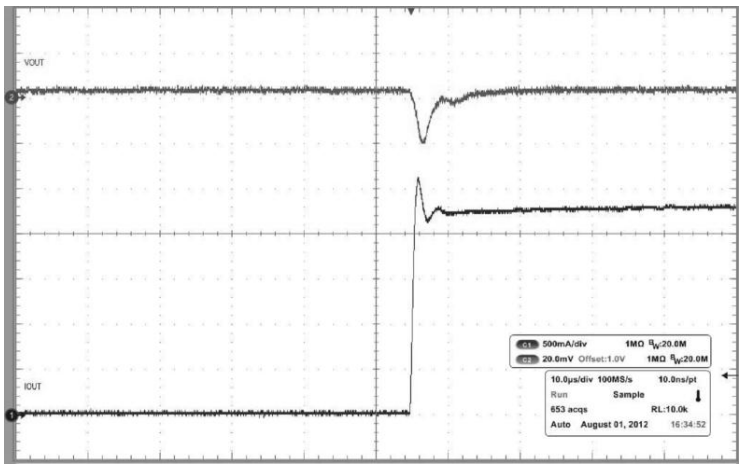


Figure 36:
DC/DC Buck SD0 Load Transient

DC/DC Buck SD0 Load Transient: Shows the response of the SD0 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=0, C_{OUT}=44uF and T_A=25°C

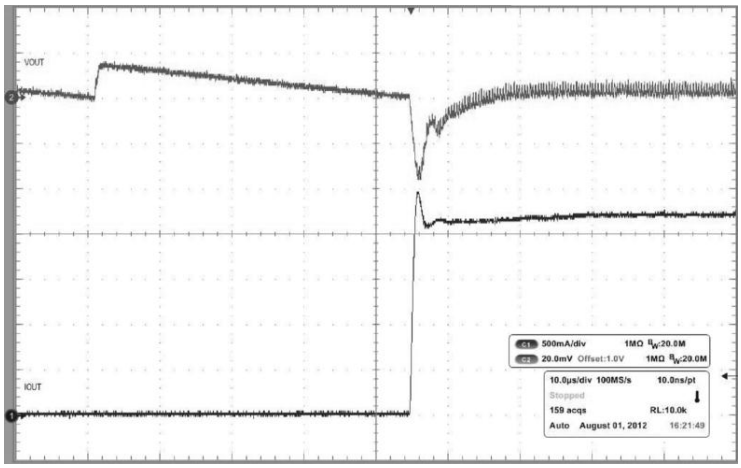
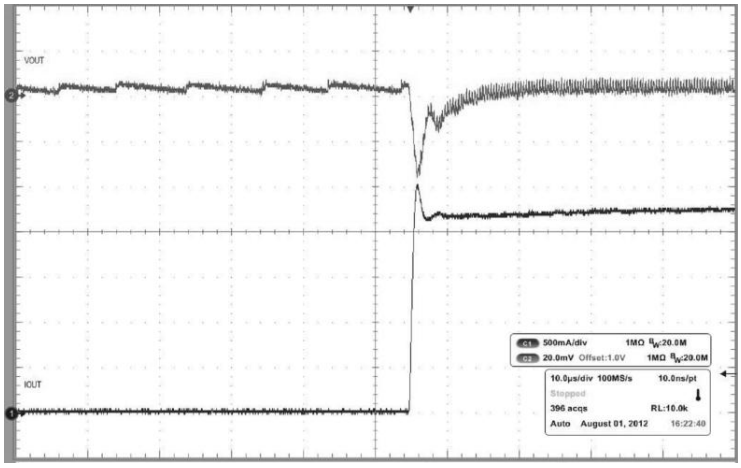


Figure 37:
DC/DC Buck SD0 Low Noise Load Transient

DC/DC Buck SD0 Low Noise Load Transient: Shows the response of the SD0 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=0, C_{OUT}=44uF, low_noise=1 and T_A=25°C



LDO Regulators

Description

11 universal IO range LDOs offer a wide input (1.7V to 5.5V) as well as a wide output (0.8 to 3.3V) voltage range to be used for general purpose peripheral supply. LDO3 is intended to be used for tracking the output voltage of SD1 or SD6, step-size and range are matching those of SD1 and SD6.

The extended input range LDO (LDO0) can work down to 1.15V on the input side, to be used as a post regulator after a DCDC with low output voltage (e.g. 1.2V). Up to 300mA possible output currents are offered with good noise and regulation performance and very low quiescent current even suitable for stand-by power supply.

Figure 38:
Universal IO LDO Block Diagram

Universal IO LDO Block Diagram:
Shows the internal structure of the PMOS linear regulators.

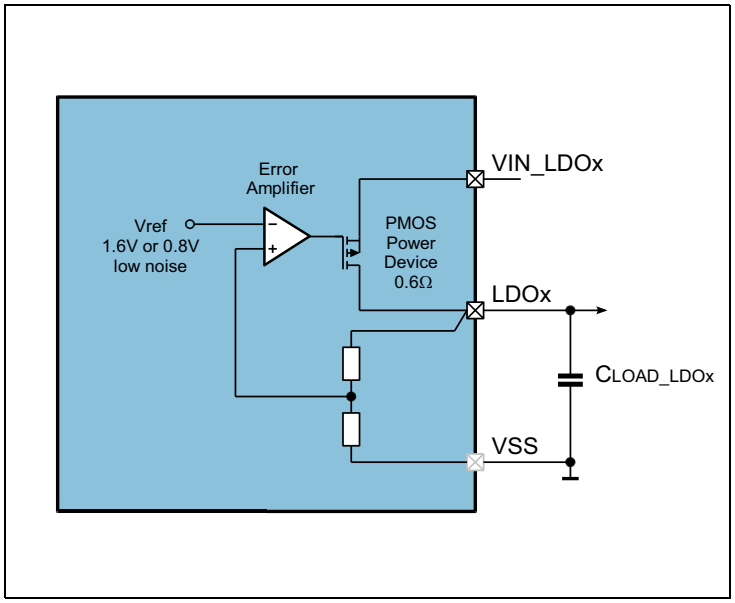


Figure 39:
Extended Input Range LDO Block Diagram

Extended Input Range LDO Block Diagram: Shows the internal structure of the NMOS linear regulator.

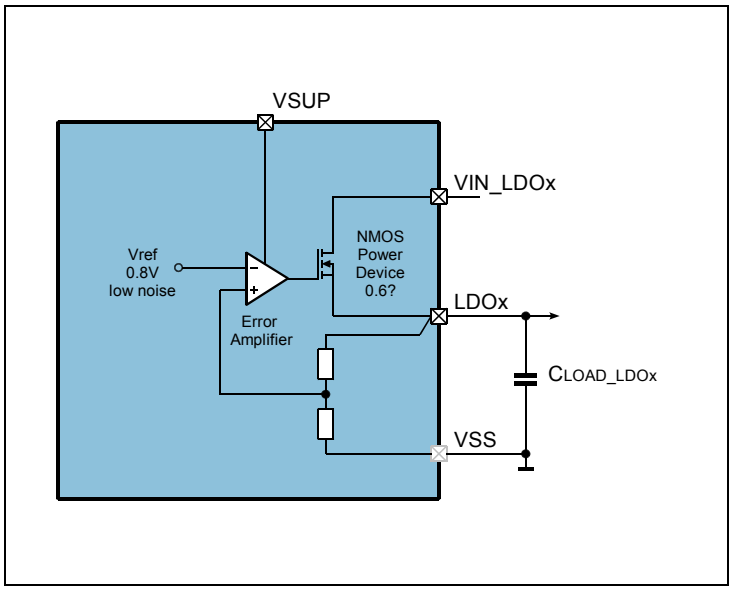
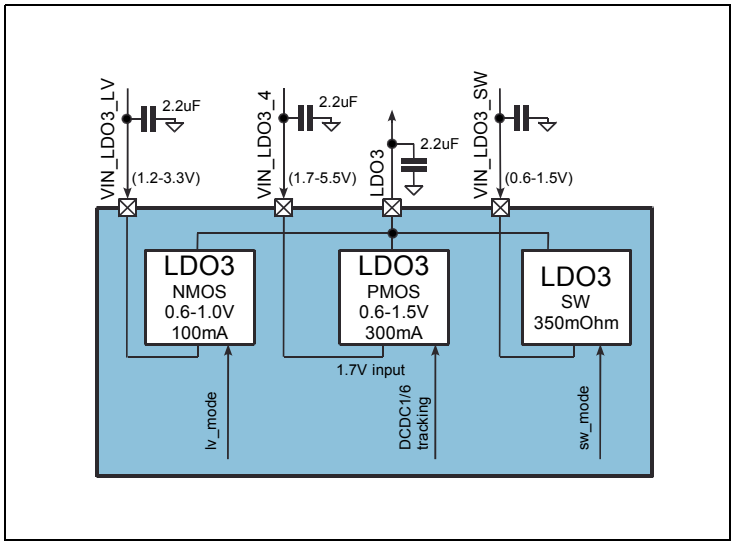


Figure 40:
Tracking LDO3 Block Diagram

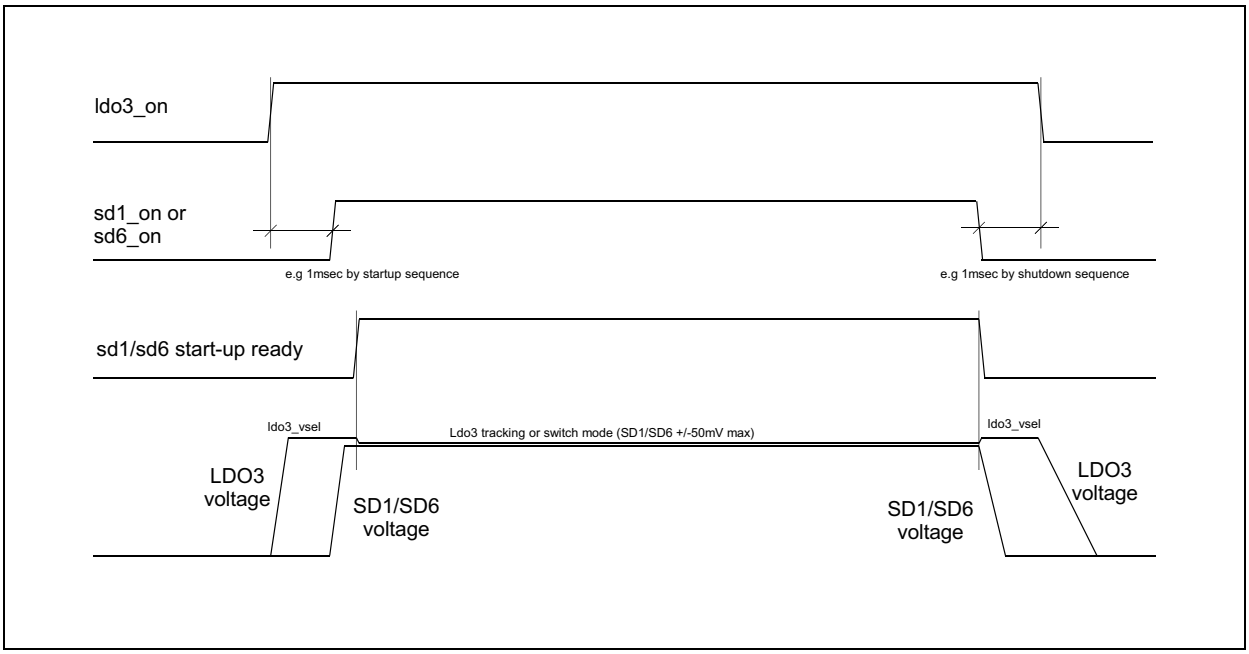
Tracking LDO3 Block Diagram: Shows the internal structure of the LDO3 linear regulator consisting of a PMOS and a NMOS LDO as well as a switch.



LDO3 can operate in three different modes (*ldo3_mode*). As normal PMOS LDO for high intput votlages operating from VIN_LDO3_4, as NMOS LDO on lower input voltages (<1.7V) from VIN_LDO3_LV or as switch between VIN_LDO3_SW and LDO3.

LDO3 has a special tracking function to follow SD1 or SD6 (selectable in OTP) output voltage as long as the DCDC is enabled, if it is disabled the LDO operates in normal PMOS mode. With *ldo3_vtrack_tr* an offset can be programmed for the PMOS tracking to compensate voltage drops along the supply lines.

Figure 41:
Tracking LDO3 Timing Diagram



Tracking LDO3 Timing Diagram: Shows the LDO3 output voltage in tracking mode.

Parameter

Figure 42:
LDO Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OUT_LDO0}	Output voltage	Iout<150mA; 10mV steps	0.825		1.25	V
V_{OUT_LDO3}	Output voltage	Iout<150mA; 10mV steps	0.62		1.5	V
$V_{OUT_LDO1,2,4-11}$	Output voltage	Iout<150mA; 25mV steps	0.825		3.3	V
V_{OUT_tol}	Output voltage tolerance	min. 40mV	-3		3	%
I_{OUT_L}	Output current (1)	ldoX_ilimit = 0 (150mA)	0		150	mA
I_{LIMIT_L}	Current limit (1)			300		mA
I_{OUT_H}	Output current (1)	ldoX_ilimit = 1 (300mA)	0		300	mA
I_{LIMIT_H}	Current limit (1)			500		mA
I_{OUT_NMOS3}	Output current (1)	LDO3 NMOS	0		100	mA
R_{ON}	On resistance	LDO0-11		0.6		Ω
		LDO3 SW			350	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		LDO3 SW; VSUP>=3.3V, VOUT=1.0V0-11			250	mΩ
P_{SRR}	Power supply rejection ratio	f=1kHz	60			dB
		f=100kHz	30			
I_{OFF}	Shut down current			100		nA
I_{VDD}	Supply current	without load		30	43	µA
t_{START}	Startup time	low current used during start-up			500	µs
$V_{LineReg}$	Line regulation	Static		0.07		%/V
		Transient; Slope: tr=15µs; delta 1V		20		mV
$V_{LoadReg}$	Load regulation	Static		0.014		%/mA
		Transient; Slope: tr=15µs; 1mA->300mA		30		mV
R_{DIS}	discharge resistance	LDO1-11 off; Vout=1V		720		Ω
		LDO0 off; Vout=1V		360		Ω

LDO Parameter: Shows the key electrical parameter of the linear regulators

Note(s) and/or Footnote(s):

1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested

Figure 43:
LDO External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT_LDO0}	Output capacitor	Ceramic X5R or X7R	1			µF
$C_{OUT_LDO1-11}$	Output capacitor	Ceramic X5R or X7R	0.7			µF
$C_{VIN_LDO0-11}$	Input capacitor	Ceramic X5R or X7R	1			µF

LDO External Components: Shows the external component parameter of the linear regulators

Low Power LDO V2_5 Regulator

Description

The low power LDO V2_5 is needed to supply the chip core (analog and digital) of the device. It is designed to get the lowest possible power consumption, and still offering reasonable regulation characteristics. The regulator has three supply inputs selecting automatically the higher one. This gives the possibility to supply the chip core either with the VBAT, VSUP or VBAT_BKUP depending on the conditions. Bulk switch comparators are used to avoid any parasitic current flow. To ensure high PSRR and stability, a low-ESR ceramic capacitor of min. 0.7µF must be connected to the output.

Parameter

Figure 44:
Low Power LDO Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Supply voltage rage	See VBAT, VSUP and VBAT_BKUP				
R_{ON}	On resistance	Guaranteed per design		50		Ω
I_{OFF}	Shut down current			100		nA
I_{VDD}	Supply current	Guaranteed per design, consider chip internal load for measurements.		3		µA
t_{START}	Startup time			200		µs
I_{OUT}	Output current	VSUP>3.0V or VBAT>5.7V in power_off mode			3	mA
V_{OUT}	Output voltage		2.4	2.5	2.6	V

Low Power LDO Parameter: Shows the key electrical parameter of the low power V2_5 linear regulator

Figure 45:
Low Power LDO External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{V2_5}	Output capacitor	Ceramic X5R or X7R	0.7			µF

Low Power LDO External Components: Shows the external component parameter of the low power V2_5 linear regulator

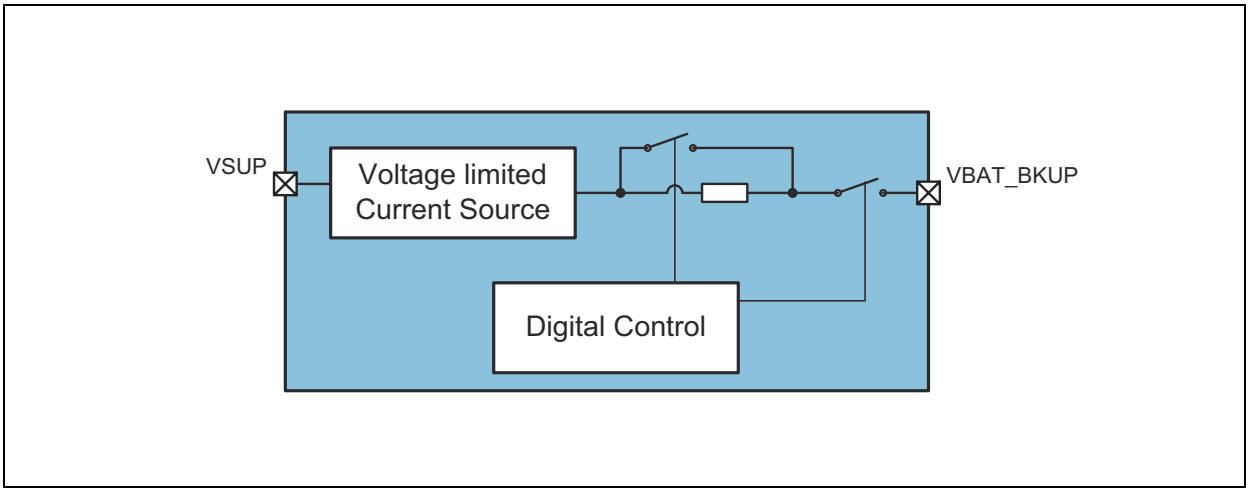
Backup Battery Charger

Description

The backup battery charger operates as a programmable voltage limited current source with a selectable output resistor. It is enabled by setting BBCMode in the Backup Battery Charger register to a value other than '00'b and offers the following features:

- Backup battery presence detection
- Selectable output resistor (R_{BBCOUT}) to reduce the current at higher voltages
- Programmable charge current I_{BBC}
- Programmable maximum charging voltage V_{BBC}
- Reverse current protection turns off backup battery charger automatically if $V_{SUP}<V_{VBAT_BKUP}$; as soon as V_{SUP} exceeds V_{VBAT_BKUP} charging is started again automatically
- Charging is stopped automatically as soon as the backup battery is fully charged; if the voltage on pin V_{BAT_BKUP} drops charging is started again automatically
- In case the main supply voltage V_{SUP} or V_{BAT} is larger than V_{BAT_BKUP} charging of the backup battery is possible in state "Off" as well; the device will check V_{VBAT_BKUP} every minute to determine if charging is required.

Figure 46:
Backup Battery Charger Block Diagram



Backup Battery Charger Block Diagram: Shows the internal structure of the charger for the backup battery.

Parameter

Figure 47:
Backup-Battery Charger Parameter

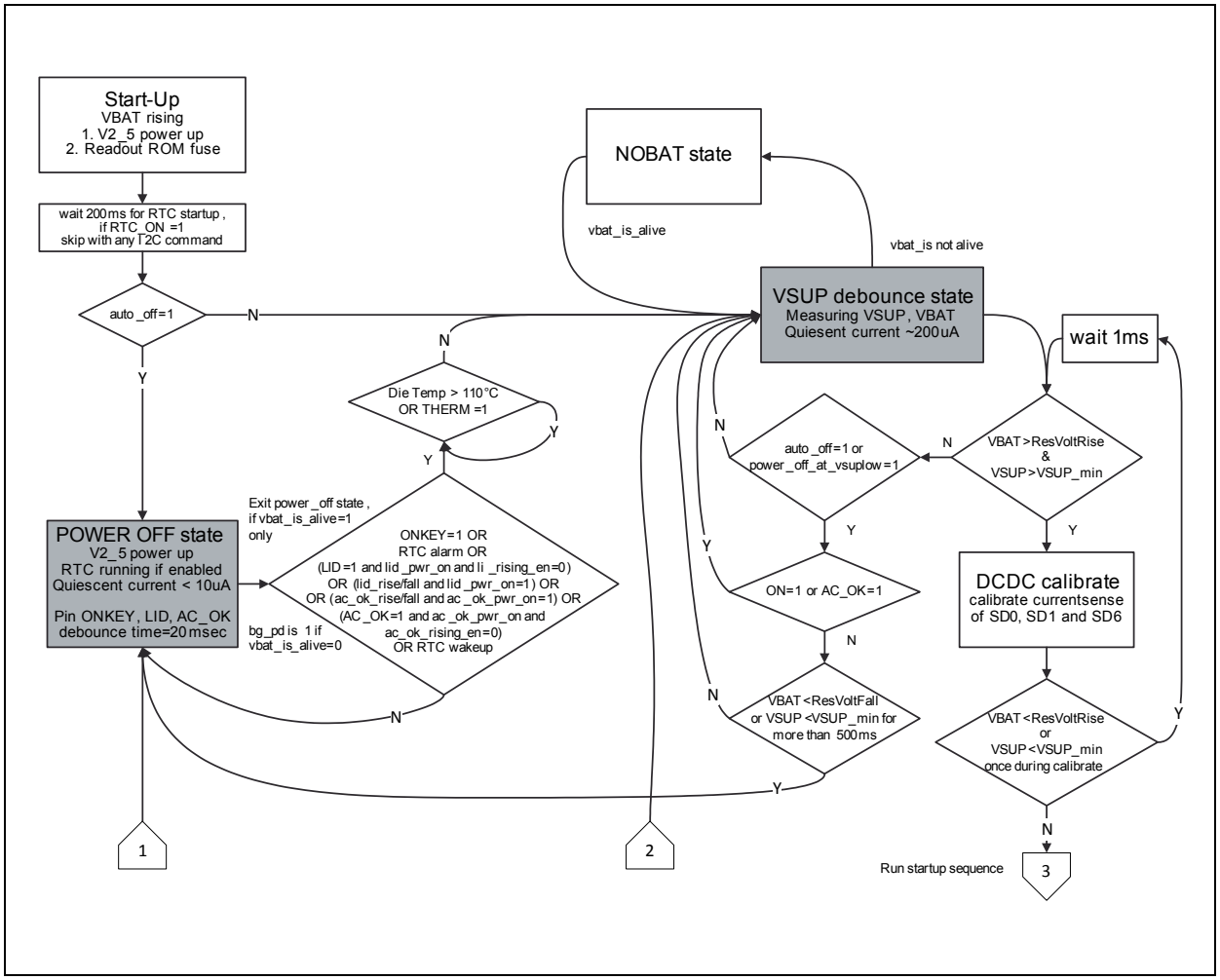
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{SUP}	Supply voltage range	BBCVolt='0'	3.0		5.5	V
		BBCVolt='1'	3.3		5.5	
V_{BBC}	Maximum charging voltage	BBCVolt='0'	2.4	2.5	2.6	V
		BBCVolt='1'	2.9	3.0	3.1	
I_{BBC}	Charge current	Value is set by BBCCur in the Backup Battery Charger register	-30%	BBCCur	+30%	A
V_{DELTA}	Delta voltage for resistive mode	BBCResOff='0'	160	220	300	mV
I_{VSUP}	Supply current	BBCResOff='0'			20	µA
		BBCResOff='1'				
		BBCPwrSave='1'; backup battery full.				

Backup-Battery Charger Parameter: Shows the key electrical parameter of the charger for the backup battery

Detailed Descriptions-System Functions

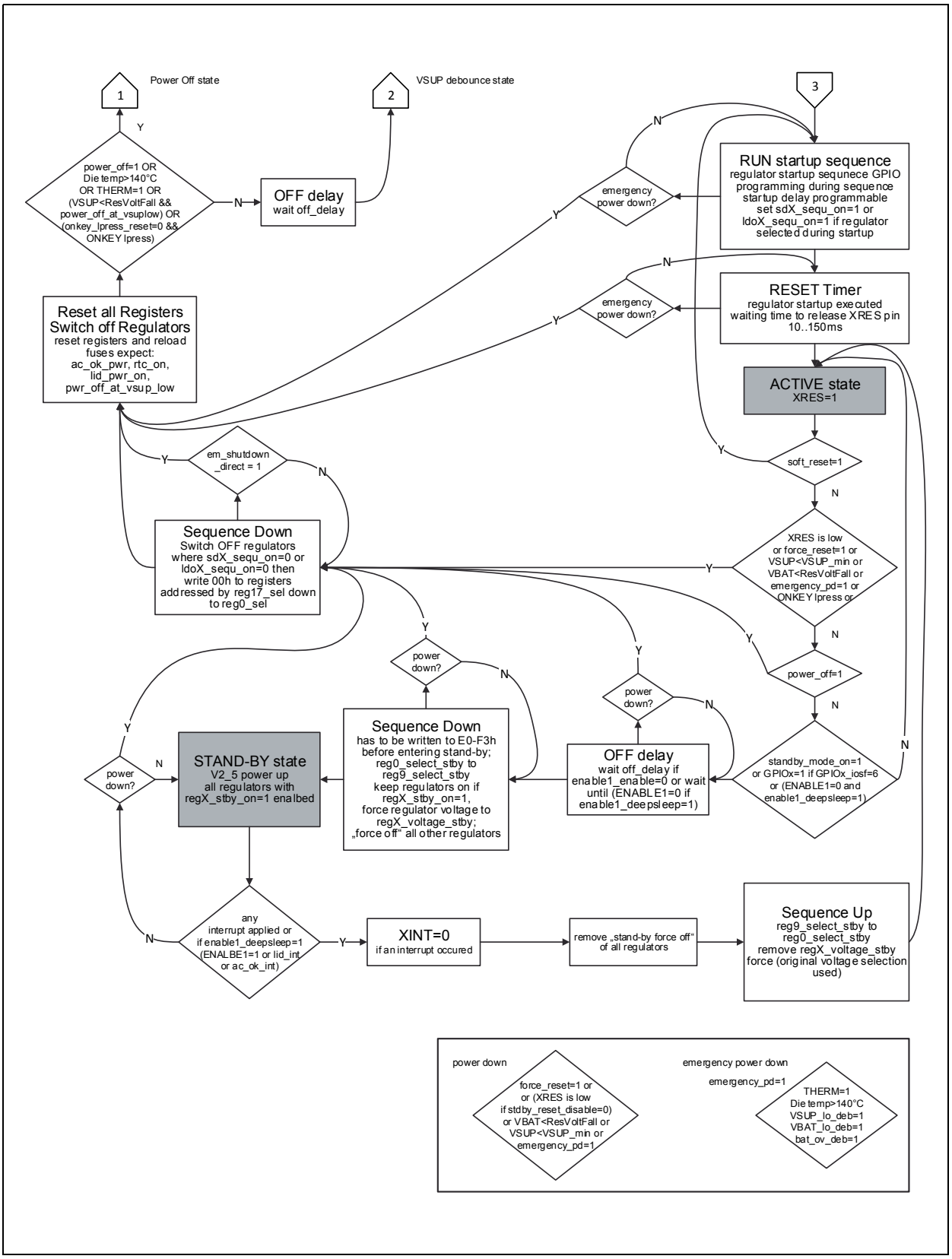
Start-Up

Figure 48:
Start-Up Flow Chart 1/2



Start-Up Flow Chart 1/2: Shows the main state transitions during start-up

Figure 49:
Start-Up Flow Chart 2/2



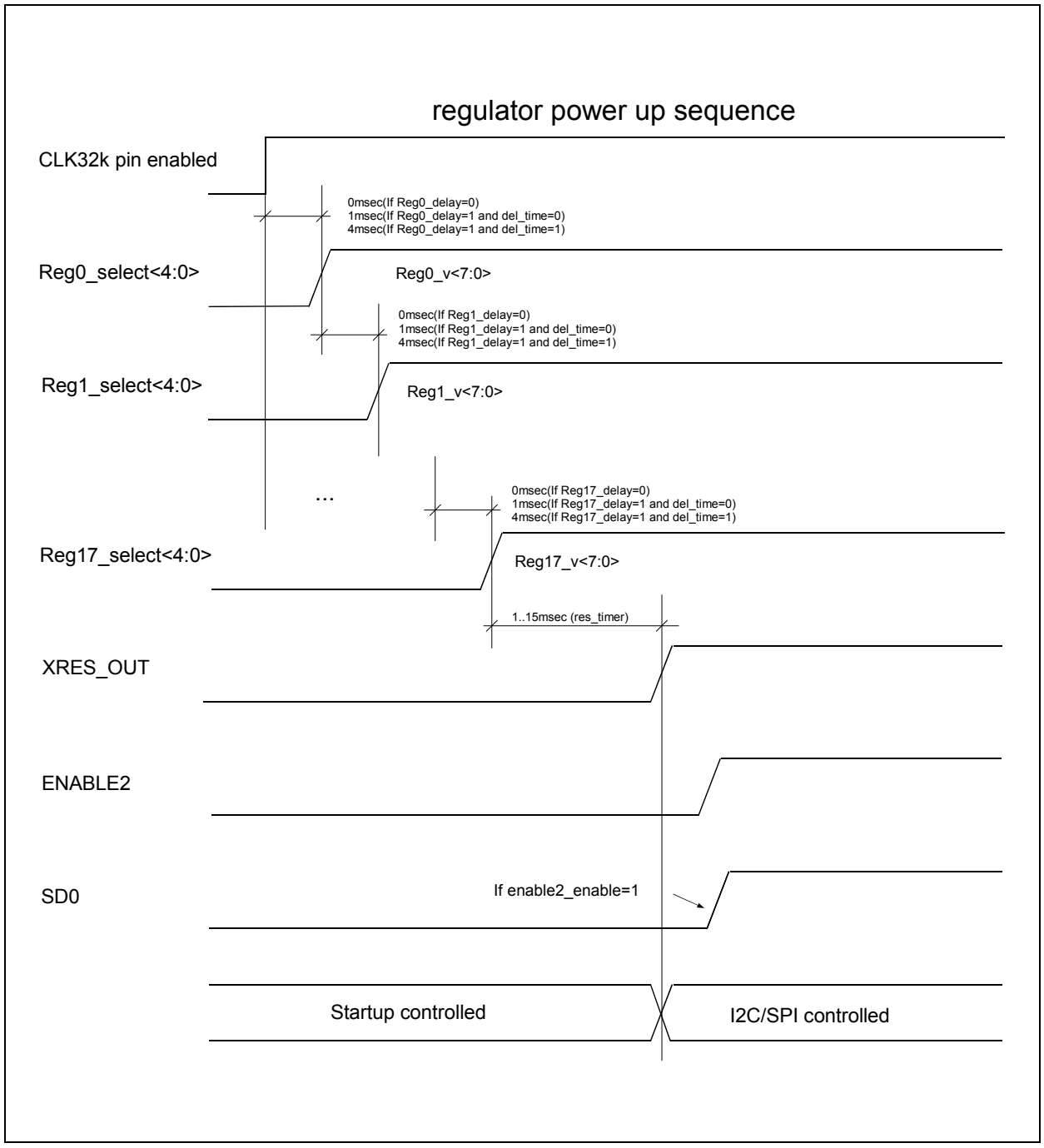
Start-Up Flow Chart 2/2: Shows the main state transitions during operation and stand-by

Normal Start-Up

The following gives a brief description on a start-up from scratch (battery insertion). More details can be found in the start-up flow charts.

- Powering up V2_5 (wait till it's above V_{POR})
- The external capacitor on CREF is charged to 1.6V.
- Check if VBAT is above ResVoltRise and VSUP above VSUP_min
- Configuration of DCDC controller (number of phases) and SD2/SD3/SD4/SD5 (combined mode or separated) is automatically detected during start-up detection phase.
- Current-sense calibration of SD0/SD1 and SD6 is performed
- Startup State machine reads out the internal Boot-OTP. The start-up sequence of Step-Down Converter, LDO's and GPIOs are controlled by the Boot-OTP.
- Reset-Timer is set by the Boot-OTP
- The reset is released when the Reset Timer expires (external pin XRES_OUT)

Figure 50:
Regulator Power-Up Sequence



Regulator Power-Up Sequence: Shows timing relationships of the regulators and corresponding control signals during power-up

Start-Up Reasons

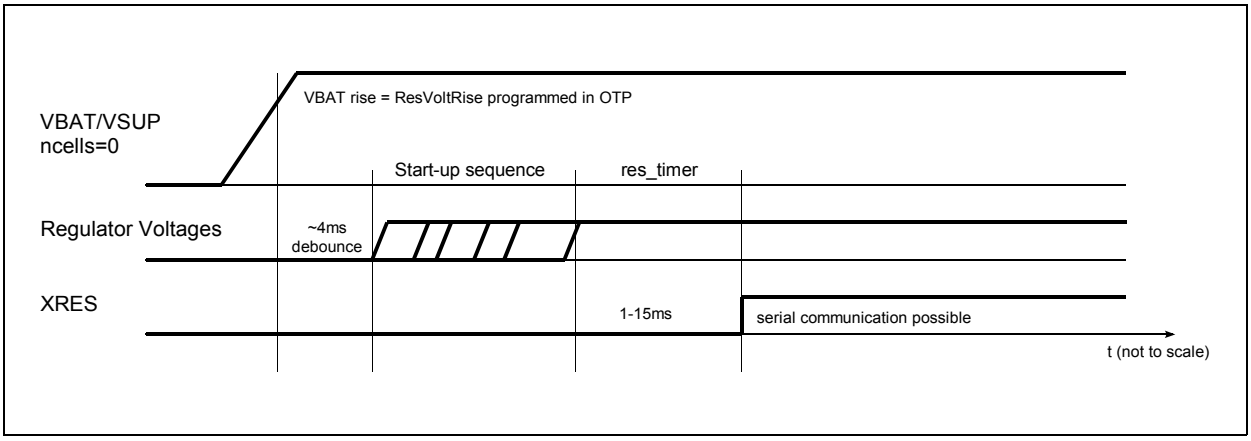
A Start-up can be activated from 8 different sources:

- VPOR has been reached (VSUP/VBAT rising from scratch)
- ONKEY has been pulled high in power_off mode
- AC_OK has been pulled high in power_off mode
- LID has been pulled high in power_off mode
- RTC wake_up has been detected in power_off mode
- Reset cycle
- Soft Reset cycle
- ResVoltRise was reached

Start-Up From Multiple Batteries

If the system is powered by a single battery the start-up looks like below.

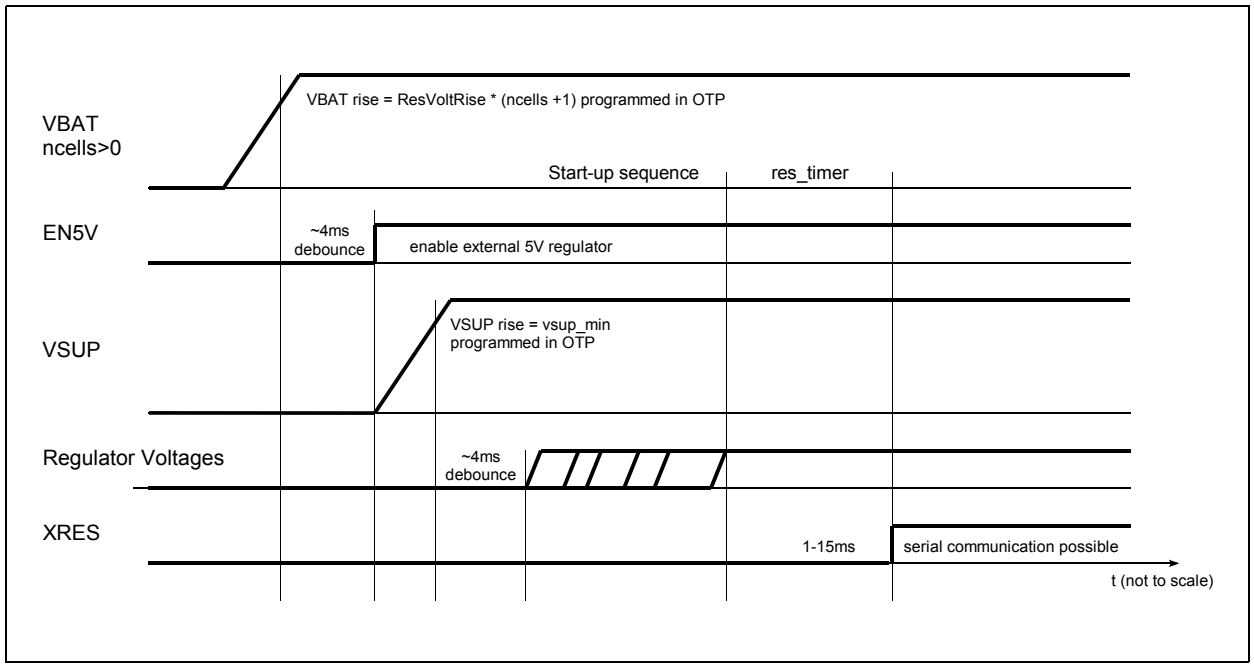
Figure 51:
Start-Up From Single Cell Batteries



Start-Up From Single Cell Batteries: Shows basic start-up from a single cell battery (VBAT and VSUP tied together)

For multi cell batteries or supplies greater 5V, the system needs a 5V pre-regulator to power the AS3722. The AS3722 is monitoring the battery voltage (VBAT) and controls the enable signal (EN5V) for the external 5V pre-regulator for generating a 5V system supply (VSUP).

Figure 52:
Start-Up From Multi Cell Batteries



Start-Up From Multi Cell Batteries: Shows basic start-up from a multi cell battery including a 5V pre-regulator

Reset

Description

XRES_IN and XRES_OUT are low active pins. An external pull-up to the periphery supply has to be added to XRES_IN. XRES_OUT is a push/pull output to VDD_GPIO_lv.

During each reset cycle the following states are controlled by the AS3722:

- Power-down sequence of the regulators
- Pin XRES_OUT is forced to GND
- All registers are set to their default values after power-on, except the reset control- and status-registers.
- Normal startup with programmable power-on sequence and regulator voltages (see chapter Start-up)
- Reset is active until the programmable reset timer expires (set by register bits *res_timer<2:0>*)

Reset Reasons

Reset can be activated from 10 different sources:

- VPOR has been reached (VSUP/VBAT rising from scratch)
- VSUP low or VBAT low, *ResVoltFall* (2.5V) has been reached
- Software forced reset by *force_reset* (soft or hard)
- Software forced Power off mode by *power_off*
- ONKEY long press has been detected
- External triggered through the pin XRES_IN
- External triggered through the pin THERM
- Over-temperature T140 (die, SD0, SD1 or SD6)
- Watchdog
- VSUP overvoltage reached
- Transition to standby_mode

Voltage Detection

There are two types of voltage dependent resets: V_{POR} and $V_{RESRISE}$. V_{POR} monitors the voltage on V2_5 and $V_{RESRISE}$ monitors the voltage on VBAT/VSUP. The linear regulator for V2_5 is always on and uses the voltage VBAT/VSUP as its source.

The pin XRES_OUT is only released if V2_5 is above V_{POR}, VBAT is above *ResVoltRise* and VSUP is above *vsup_min*.

$V_{RESFALL}$ is only accepted if the reset condition is longer than $V_{RESMASK}$. This guard time is used to avoid a complete reset of the system in case of short drops of VBAT.

Figure 53:
VSUP Supervision

SupResEn	power_off_at_vsuplow	auto_off	Behavior if VSUP<ResVoltFall
0	x	x	LowBat interrupt is generated
1	0	0	Reset cycle is initiated, PMIC will move to “VSUP debonce” state and start-up if VSUP>ResVoltRise
1	0	1	Reset cycle is initiated, PMIC will move to “VSUP debonce” state and try to start-up if VSUP>ResVoltRise, if not it will go to the “Power off” state
1	1	x	Reset cycle is initiated, PMIC will move to “Power off” state

VSUP Supervision: Describes the behavior of the PMIC when VSUP drops below ResVoltFall depending on OTP bit settings.

Power Off

To put the chip into ultralow power mode, write '1' into *power_off*. The chip stays in power off mode until he gets a wakeup signal from either the ONKEY, LID or the AC_OK pin or from the RTC. For more details see the start-up flowchart (see Start-up Flow Chart). The bit *power_off* is automatically cleared by this reset cycle. During *power_off* state all circuits are shut-off except the Low Power LDO (V2_5) and the RTC oscillator (if enabled). Thus the current consumption of AS3722 is reduced to less than 10µA. The digital part is supplied by V2_5, all other circuits are turned off in this mode, including references and oscillator. Except the reset control registers all other registers are set to their default value after power-on.

Software Forced Reset

Writing '1' into the register bit *force_reset* immediately starts a reset cycle. The bit *force_reset* is automatically cleared by this reset.

External Triggered Reset

If the pin XRES_IN is pulled from high to low by an external source (e.g. microprocessor or button) a reset cycle is started as well.

Over-Temperature Reset

The reset cycle can be started by over-temperature conditions. (see chapter Supervisor)

Watchdog Reset

If the watchdog is armed (register bit *wtdg_on* = 1 and *wtdg_res_on*= 1) and the timer expires it causes a reset. (see chapter Watchdog).

Long ONKEY Press

When applying a high level on the ONKEY input pin for 2s/4s/8s (depending on *on_shutdown_delay*) a power_off is initiated. With the bit *onkey_lpress_reset* = 1 the chip will generate a reset cycle. This is thought as a safety feature when the SW hangs up and no watchdog is used.

Powering down of the regulators can be done immediately or according to the power-off sequence depending on the *em_shutdown_direct* OTP bit.

Figure 54:
ONKEY Longpress Behavior

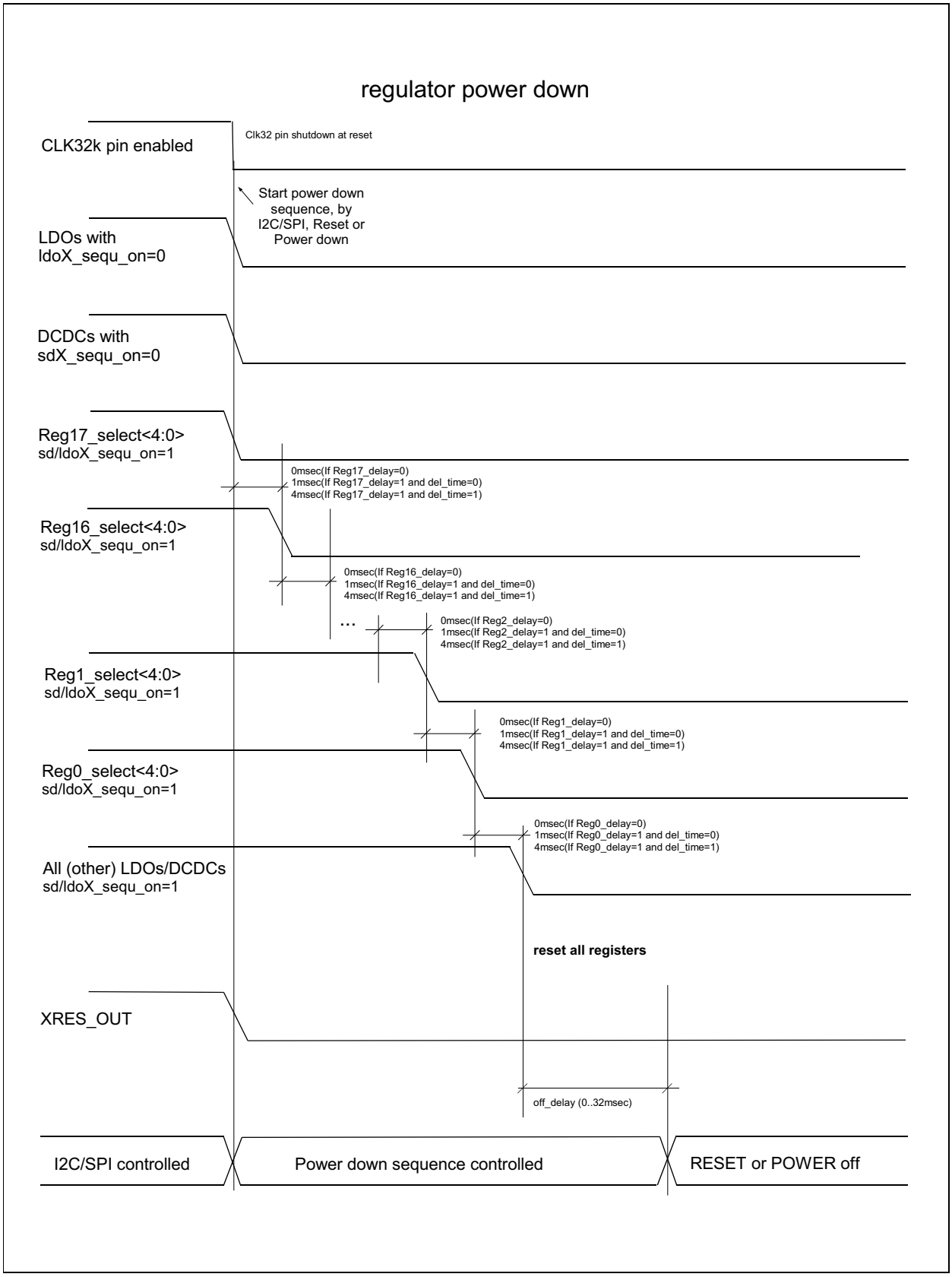
onkey_lpress_reset	onkey_shutdown_delay	Longpress Behavior
0	00	long press feature disabled
0	01	power_off after 2s long press delay
0	10	power_off after 4s long press delay
0	11	power_off after 8s long press delay
1	00	long press feature disabled
1	01	reset_cycle after 2s long press delay
1	10	reset_cycle after 4s long press delay
1	11	reset_cycle after 8s long press delay

ONKEY Longpress Behavior: Shows the selectable options for behaving on a long pressReset and Power-Off Sequence

The regulator power-down sequence is inverted to the power-up sequence programmed in the OTP. It can be slightly modified by setting or clearing the *sdX_sequ_on* and *ldoX_sequ_on* bits. The bit is set automatically for all the regulators defined in the OTP start-up sequence.

- Regulators which have the corresponding sequ_on bit cleared will be shut down before the power-down sequence starts.
- Regulators which have the bit set and are in the power-up sequence of the OTP will shut down in an inverted order.
- Regulators which have the bit set and are not part of the power-up sequence will shut down after the sequence has been completed

Figure 55:
Regulator Power-Down Sequence



Regulator Power-Down Sequence: Shows timing relationships of the regulators and corresponding control signals during power-down

Parameter

Figure 56:
Reset levels

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Overall power on reset	Monitor voltage on V2_5; power on reset for all internal functions	1.5	2.0	2.3	V
$V_{RESRISE}$	Reset level for VSUP/VBAT rising	Monitor voltage on VBAT; rising level		ResVoltRise(1)		V
		Monitor voltage on VSUP; rising level		vsup_min		V
$V_{RESFALL}$	Reset level for VSUP/VBAT falling	Monitor voltage on VSUP/VBAT; falling level		2.5		V
		if SupResEn=1		ResVoltFall or vsup_min		V
$V_{RESMASK}$	Mask time for VRESFALL. Duration for VBAT<ResVoltFall or VSUP<vsup_min until a reset cycle is started(2)	FastResEn = 0		4		ms
		FastResEn = 1		4		µs

Reset Levels: Shows the electrical parameter of the voltage supervisors controlling start-up and reset cycles.

Note(s) and/or Footnote(s):

1. It's recommended to set the ResVoltRise level 200mV above the ResVoltFall level to have a hysteresis.
2. XRES signal is de-bounced with the specified mask time for rising- and falling slope of VBAT.

Stand-By

Description

Stand-by allows shutting down a part or the complete system. Stand-by can be terminated by every possible interrupt or ENABLE1of the PMU. The interrupt has to be before going to stand-by.

Figure 57:
Stand-By

State	Description
Enter via ENABLE1	To enter stand-by mode the following settings have to be done: • Enable just these IRQ sources which should lead to leave stand-by mode. • Make sure that IRQ is inactive (IRQ flags get cleared by register reading) • Enable ENABLE1 (enable1_deepsleep=1) • Set *regX_select_stby* to define the sequence for going into stand-by for up to 10 regulators • Set *regX_voltage_stby* if another voltage is needing during stand-by • Define which regulators should be kept powered during stand-by (*sdX_stby_on* and *ldoX_stby_on*) • Define the delay between the regulators when going into stand-by (*regX_delay_stdby* and *delay_time_stby*) • Activate ENABLE1 (pull LOW)
Enter via GPIO	To enter stand-by mode the following settings have to be done: • Enable just these IRQ sources which should lead to leave stand-by mode. • Make sure that IRQ is inactive (IRQ flags get cleared by register reading) • Set the GPIO to input (*gpioX_mode* = 0) • Set the GPIO for stand-by control (*gpioX_iosf* = 5) • Set *regX_select_stby* to define the sequence for going into stand-by for up to 10 regulators • Set *regX_voltage_stby* if another voltage is needing during stand-by • Define the regulators to be controlled by a specific GPIO (*gpio_ctrl_sdX* and *gpio_ctrl_ldoX*) • Define which regulators should be kept powered during stand-by (*sdX_stby_on* and *ldoX_stby_on*) • Define the delay between the regulators when going into stand-by (*regX_delay_stdby* and *delay_time_stby*) • Set the delay for going into stand-by after GPIO activation (*off_delay)* • Activate the selected GPIO (set to HIGH)
Enter via SW	To enter stand-by mode the following settings have to be done: • Enable just these IRQ sources which should lead to leave stand-by mode. • Make sure that IRQ is inactive (IRQ flags get cleared by register reading) • Set *regX_select_stby* and *regX_voltage_stby* if another voltage is needing during stand-by for up to 10 regulators • Define which regulators should be kept powered during stand-by (*sdX_stby_on* and *ldoX_stby_on*) • Set the delay for going into stand-by after the SW command *(off_delay*) • set *standby_mode_on* to 1
Stand-by	V2_5 chip supply is kept ON All other regulators are switched OFF dependent on the bits *sdX_stby_on* and *ldoX_stby_on* XRES_OUT goes active (can be disabled with *stdby_reset_disable*) and pwr_good goes inactive

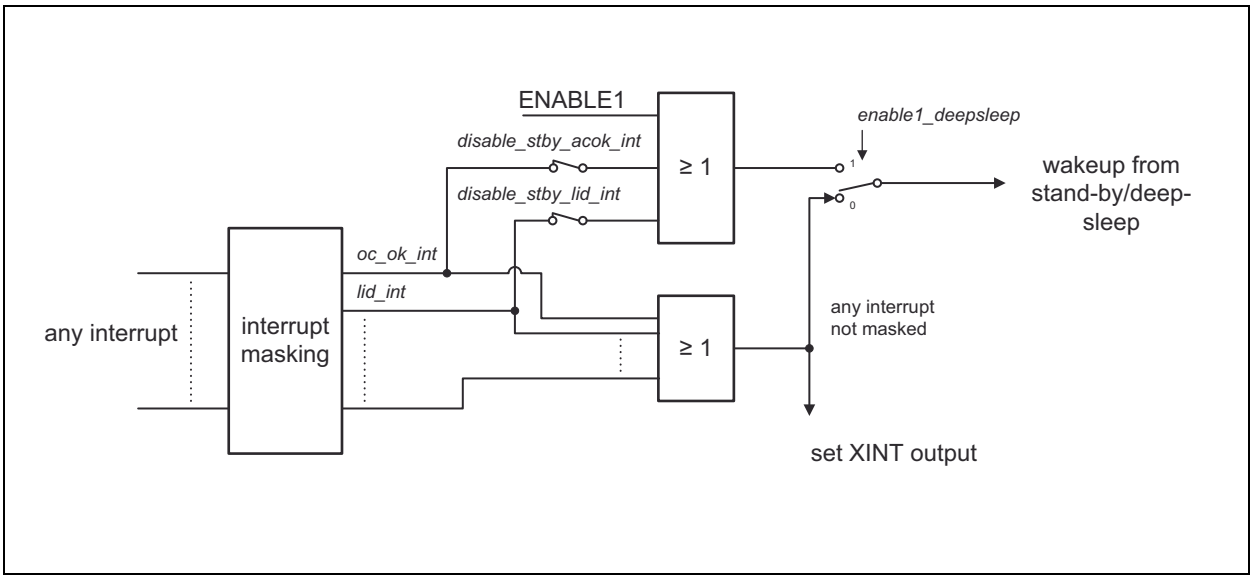
State	Description
Leave	The chip will come out of stand-by with any IRQ activation (it's not possible to leave with the same GPIO you entered stand-by) If enable1_deepsleep=1 the chip will come out of stand-by with ENABLE1 going HIGH or the LID or AC_OK interrupt. Start-Up sequence is provided defined by regX_select_stby, regX_delay_stdby and delay_time_stby

Stand-By: Shows different options to enter and leave the stand-by state.

Stand-By Sequence

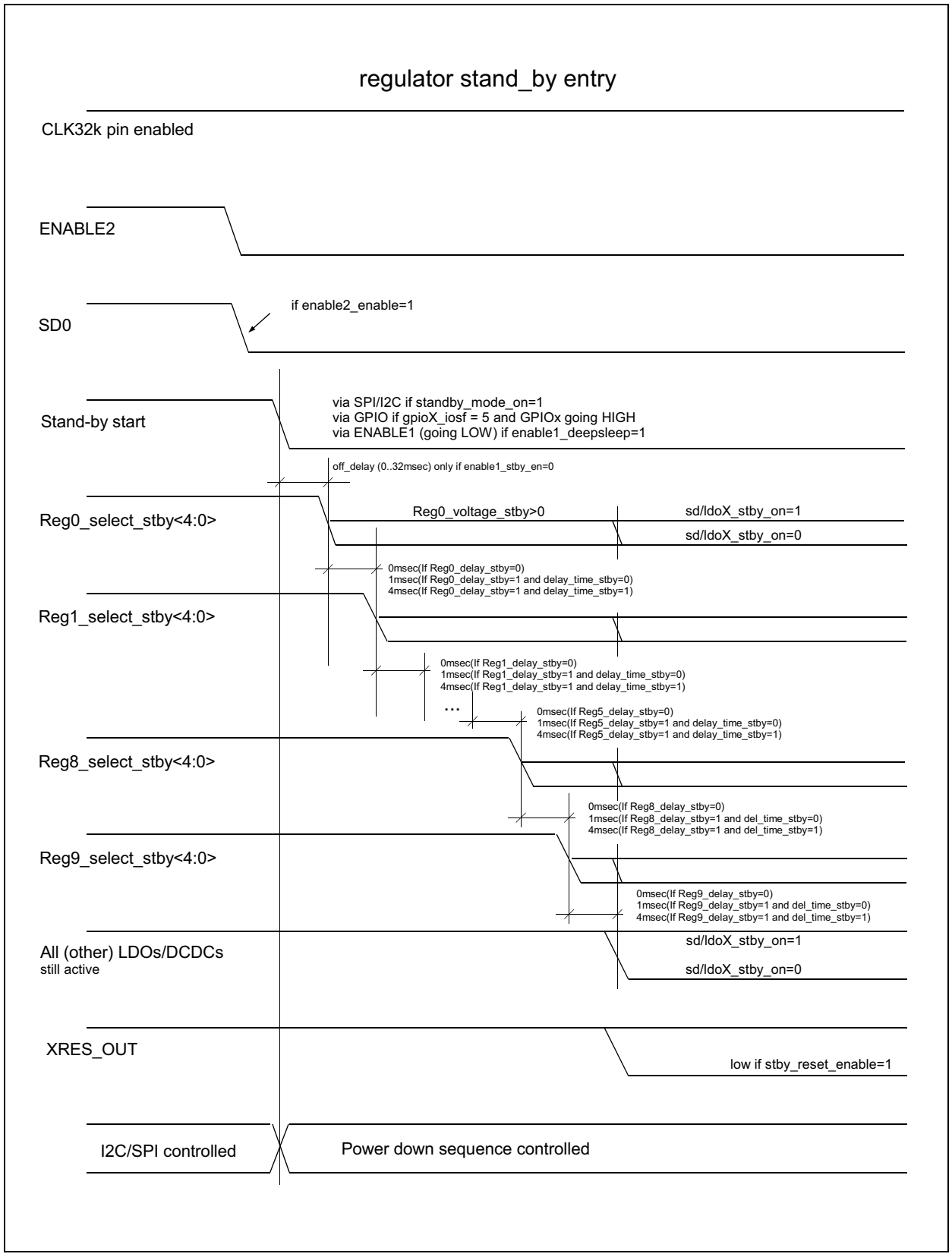
- Regulators which have the *sdX/ldoX_stby_on* bit set will stay active during stand-by
- Regulators which have the *sdX/ldoX_stby_on* bit set and are part of the sequence (*regX_select_stby*) with a *regX_voltage_stby*>0 will change to the defined voltage in the sequence and stay on this voltage during stand_by
- Regulators which are part of the sequence (*regX_select_stby*) with a *regX_voltage_stby*=0 will be turned off in the sequence.
- Regulators which have the *sdX/ldoX_stby_on* bit cleared and are part of the sequence (*regX_select_stby*) with a *regX_voltage_stby*>0 will change to the defined voltage in the sequence and be turned off at the end of the sequence
- Regulators which have the *sdX/ldoX_stby_on* bit cleared and are not part of the sequence will be turned off at the end of the sequence

Figure 58:
Stand-By Leave



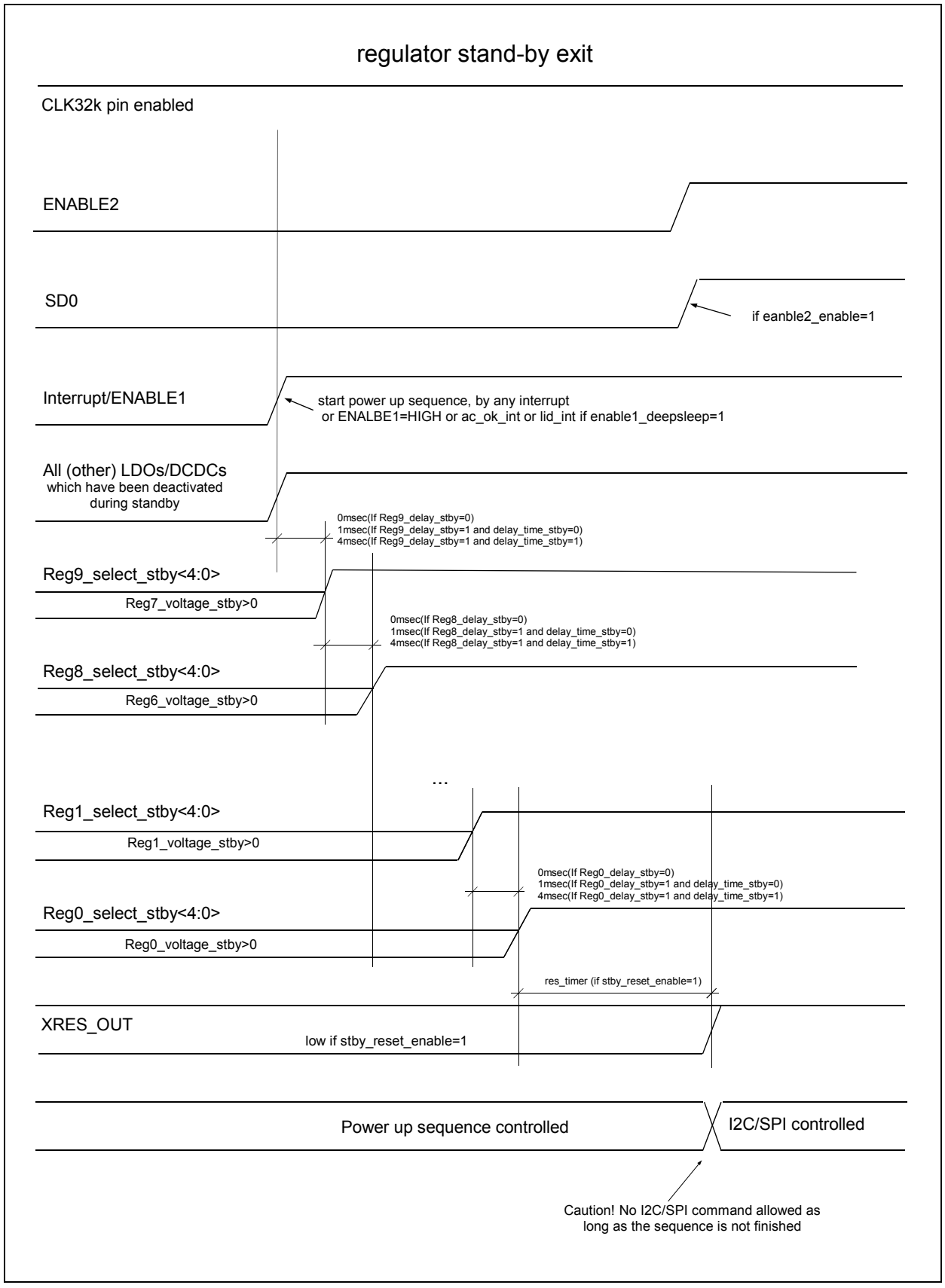
Stand-By Leave: Describes the possibilities of the PMIC to leave the stand-by state

Figure 59:
Regulator Stand-By Entry Sequence



Regulator Stand-By Entry Sequence: Shows timing relationships of the regulators and corresponding control signals during entering stand-by mode

Figure 60:
Regulator Stand-By Exit Sequence



Regulator Stand-By Exit Sequence: Shows timing relationships of the regulators and corresponding control signals during exiting stand-by mode

Internal References

Description

The internal reference is power by the V2_5 always on LDO. It uses an external capacitor and resistor for filtering and current setting. In power_off mode the V2_5 stays alive but the reference will be disabled.

Low Power Mode

Use bit *low_power_on* to activate the Low Power Mode. In this mode the on-chip voltage reference and the temperature supervision comparators are operating in pulsed mode. This reduces the quiescent current of the AS3722 by 45uA (typ.). Because of the pulsed function some specifications are not fulfilled in this mode (e.g. increased noise), but still the full functionality is available.

For disabling the Low Power Mode *low_power_on* has to be cleared via the serial interface.

Parameter

Figure 61:
Reference Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEXT}	Reference Voltage	Low noise trimmed voltage reference – connected to Pad CREF; **do not load**	1.58	1.6	1.62	V
f_{CLK}	Accuracy of Internal reference clock	Adjustable by serial interface register clk_int	-12	f_{CLK}	+12	%

Reference Parameter: Shows the key electrical parameter of the on-chip reference

Figure 62:
Reference External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{EXT}	External filter capacitor	Ceramic low-ESR capacitor between CREF and VSS	-10%	100	+10%	nF
R_{BIAS}	External bias current set resistor	Bias Current set resistor between RBIAS and VSS	-1%	220	+1%	kΩ

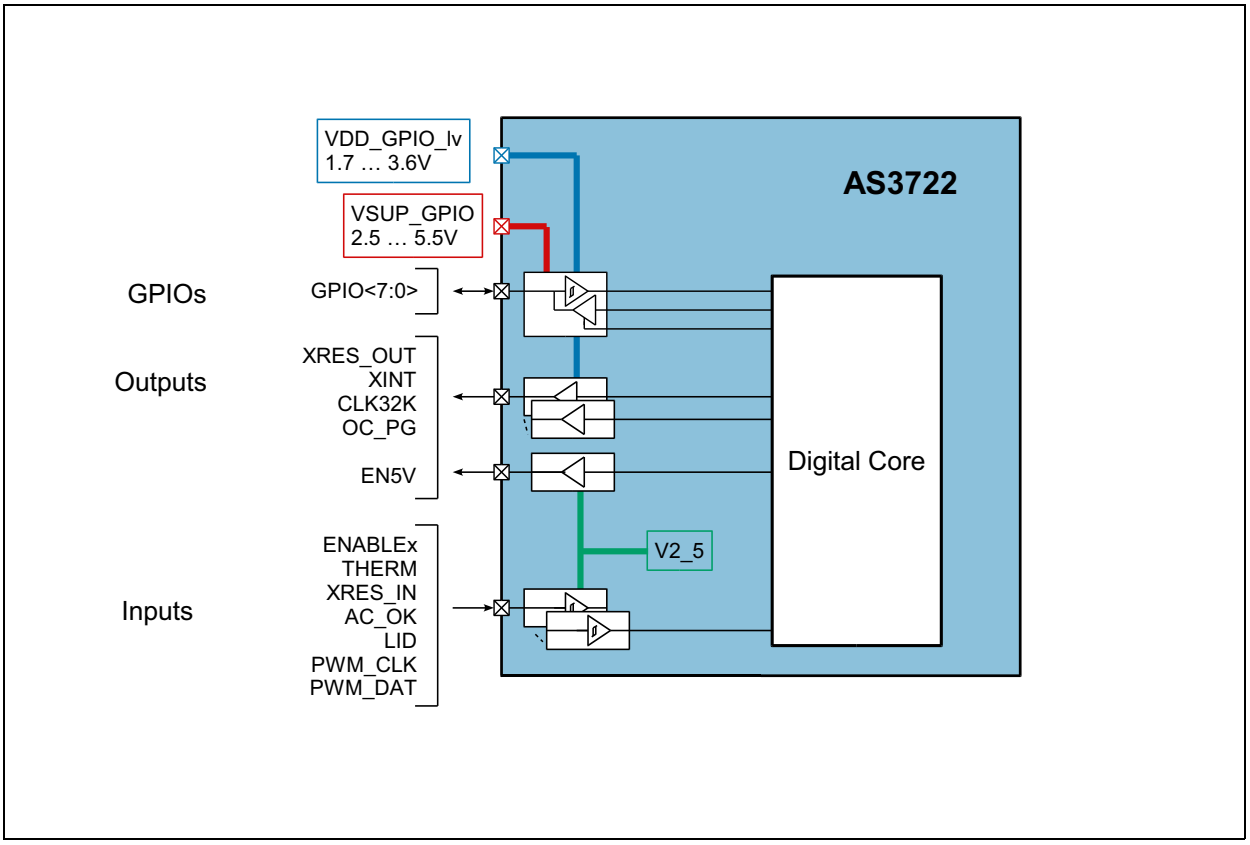
Reference External Components: Shows the external component parameter of the on-chip reference

Digital IO Supply Concept

Description

GPIOs can be switched between VSUP_GPIO and VDD_GPIO_lv supply for the output function. All other digital outputs are supplied with VDD_GPIO_lv.

Figure 63:
Digital IO Supply Concept



Digital IO Supply Concept: Shows the supply concept for digital inputs and outputs.

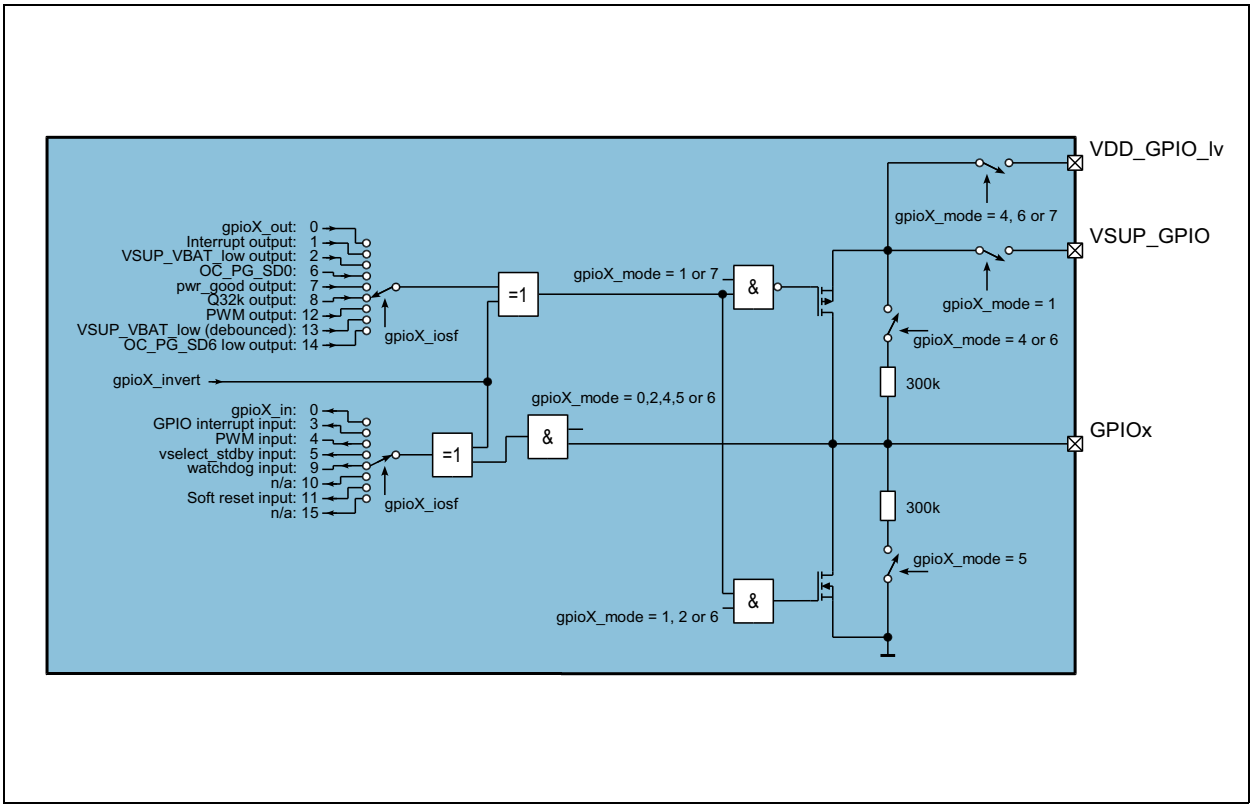
GPIO Pins

Description

The device contains 8 GPIO pins. Each of the pins can be configured as digital input, digital input (with pull-up or pull-down), ADC input (tri-state), push-pull output (selectable lower or higher GPIO supply), or open drain output (with or without pull-up). When configured as output the output source can be a register bit, or the PWM generator.

The polarity of the input and output signals can be inverted with the corresponding *gpioX_invert* bit, all further descriptions refer to normal (non-inverted) mode.

Figure 64:
GPIO Block Diagram



GPIO Block Diagram: Shows the internal structure of the IO pads

IO Functions

Normal IO Operation

If set to input, the logic level of the signal present at the GPIOx pin can be read from *gpioX_in*. If the output mode is chosen, *gpioX_out* specifies the logic level of the GPIOx pin.

This mode is also used for the on/off control of the DCDC and LDOs. The selection which regulator is controlled by which GPIO, is done with the *gpio_ctrl_sdX or gpio_ctrl_ldoX* bits. The *gpioX_mode* should be set to input.

Interrupt Output

GPIOx pin logic state is derived from the interrupt signal INT. Whenever an interrupt is present, the GPIOx pin is pulled high. The *gpioX_mode* should be set to output.

VSUP_VBAT_Low Output (not de-bounced)

GPIOx pin will go high if VSUP falls below *vsup_min* or VBAT falls below *ResVoltFa*ll and *SupResEn* = 0. The gpioX_mode should be set to output.

GPIO Interrupt Input

A falling or rising edge will set the *gpio_int* bit. The *gpioX_mode* should be set to input.

PWM Input

With this input the PWM signal of the internal PWM generator can be over-ruled. This input is then used to drive the PWM output function of a GPIO if selected. The *gpioX_mode* should be set to input.

Voltage_sdtby + Restart Input

As long as the GPIOx pin is high the DCDC/LDOs operate with the normal register settings. If the GPIOx pin goes low the settings will change to the ones stored in *regX_voltage_stby*. In addition the chip is set into stand-by mode. *regX_select_stby* defines the order of the regulators for going into stand_by. All other regulators not defined in *sdX_stby_on* or *ldoX_stdby_on* will be put into stand_by simultaneously at the end of the sequence.

Pulling GPIOx pin high will wake-up the chip. The sequence is reversed to going into stand_by.

Delays for the sequence can be set with *regX_stby_delay* and *delay_time_stby*.

The *gpioX_mode* should be set to input.

OC_PG_SD0 Output

Please see section OC_PG pin function description in chapter OC_PG (Output Pins) for a detailed description.

PWRGOOD Output

This signal will go high at the end of the start-up sequence. This can be used as a second reset signal to the processor to e.g. start oscillators. The *gpioX_mode* should be set to output.

Q32k Output

When selected the GPIOx will provide the 32kHz RTC crystal frequency. If the oscillator is not enabled or not assembled an internal RC oscillator based clock will be used for the output. The *gpioX_mode* should be set to output.

Watchdog Input

When pulling the GPIO high the watchdog will be triggered to avoid a reset cycle initiated by the watchdog. The *gpioX_mode* should be set to input.

Soft-Reset Input

This will perform a start-up sequence to reset all voltage registers. The *gpioX_mode* should be set to input.

PWM Output

The GPIO block includes an internal programmable PWM generator (can be connected to any of the GPIO outputs). Its timing is defined by *pwm_h_time*, *pwm_l_time* and *pwm_div*. The *gpioX_mode* should be set to output.

Vsup_vbat_low Output (de-bounced)

GPIOx pin will go high if VSUP falls below *vsup_min* or VBAT falls below *ResVoltFall* and *SupResEn* = 0. The *gpioX_mode* should be set to output.

OC_PG_SD6 Output

GPIOx pin will go high if DCDC6 is disabled. GPIOx pin will be low during start-up of DCDC6.

After start-up of DCDC6 the GPIOx pin will be high as long DCDC6 is not in a low voltage or overcurrent operation. The inputs may be masked with *pg_powergood_sd6_mask and pg_ovcurr_sd6_mask*. There is no 90us black-out time like for DCDC0. The *gpioX_mode* should be set to output.

ADC_reference Output

By setting *adc_buf_on* the buffered 1.6V ADC reference is available on GPIO7. The *gpio7_mode* should be set to "3" (tristate) *gpio7_iosf* should be set to "0" (normal).

Dedicated IO Pins

Input Pins

ENABLE1/CORE_PWRREQ

As long as the ENABLE1 pin is high the DCDC/LDOs operate with the normal register settings. If the ENABLE1 pin goes low the settings will change to the ones stored in *regX_voltage_stby*. In addition the chip is set into stand-by mode. *regX_select_stby* defines the order of the regulators for going into stand_by. All other regulators not defined in *sdX_stby_on* or *ldoX_stdby_on* will be put into stand_by simultaneously at the end of the sequence.

Pulling ENABLE1 pin high will wake-up the chip. The sequence is reversed to going into stand_by.

Delays for the sequence can be set with *regX_stby_delay* and *delay_time_stby*.

ENABLE1 pin is default disabled after start-up from off state. enable1_stby_en and enable1_inv will enable the input and set the polarity.

ENABLE2/CPU_PWRREQ

ENABLE2 is a dedicated pin to on/off control of SD0. *enable2_enable* and *enable2_inv* will enable the input and set the polarity.

THERM

Is an external signal which triggers an immediate power down similar to VSUP_low or a chip over-temperature event. The chip will not power-on again before the THERM signal is de-asserted.

AC_OK

Additional power_on input which is used to e.g. detect a charger adapter.

With *ac_ok_rising_en* the detection can be switched between edge and level, while *ac_ok_pwr_on* will disable/enable the input. *ac_ok_pwr* can be used to check the status. An interrupt can be generated on rising and falling edges.

In addition this input is also used to generate the OC_PG output.

LID

Additional power_on input which is used to e.g. detect the open/close stated of the lid from a clam shell device.

With *lid_rising_en* the detection can be switched between edge and level, while *lid_pwr_on* will disable/enable the input. *lid_pwr* can be used to check the status. An interrupt can be generated on rising and falling edges.

Output Pins

VBAT_ALARM (not de-bounced)

Will go high if VSUP falls below *ResVoltFall* and *SupResEn* = 0.

CLK32K

Dedicated pin for providing a 32kHz clock from the RTC oscillator. The pin can be disabled with *clk32out_en*.

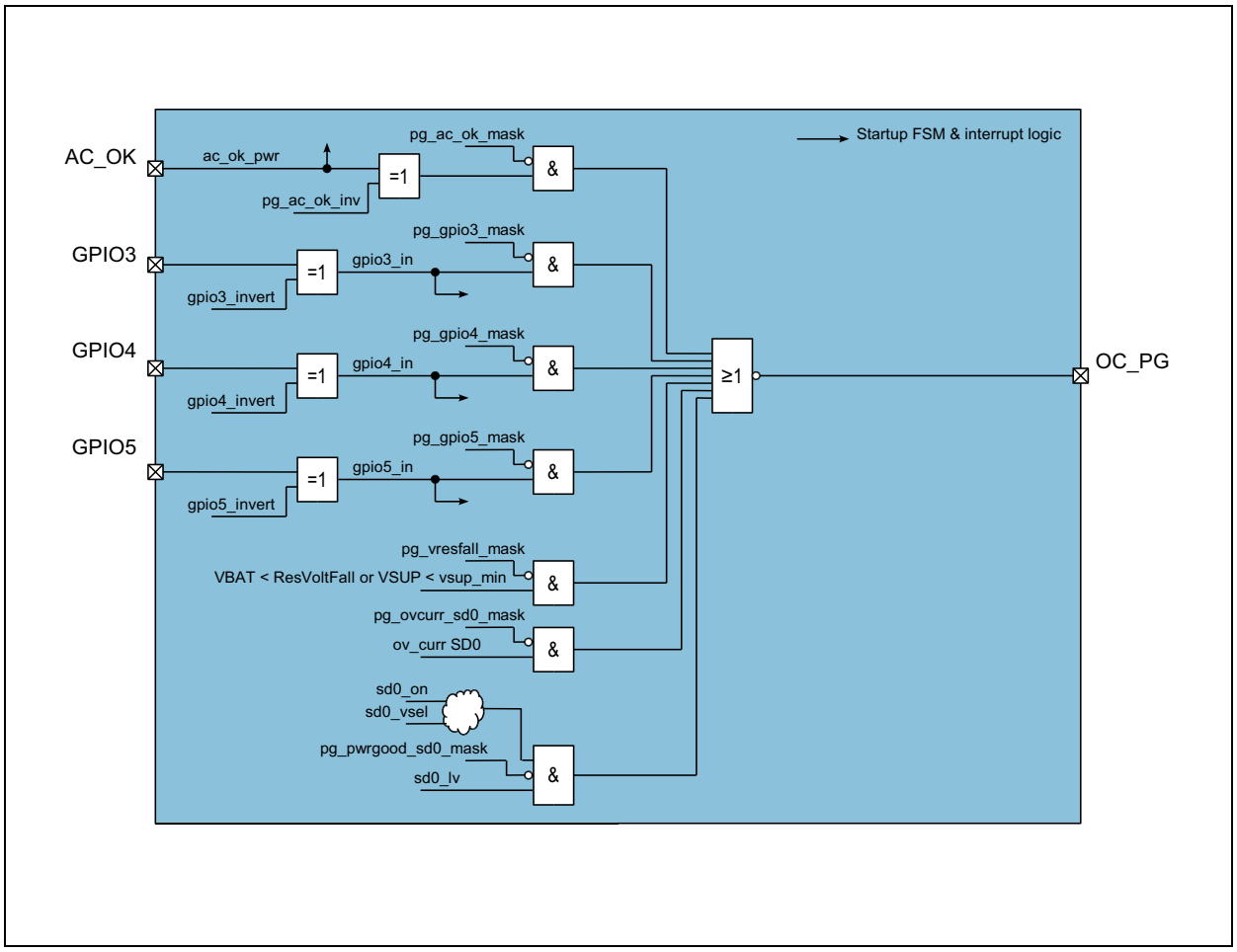
XINT

Dedicated pin for providing an active low output signal on any enabled (un-masked) interrupt event. For XINT pin an internal pull-up can be enabled to VDD_GPIO_lv (*INT_pullup*). This bit also switches the output driver to open drain.

OC_PG

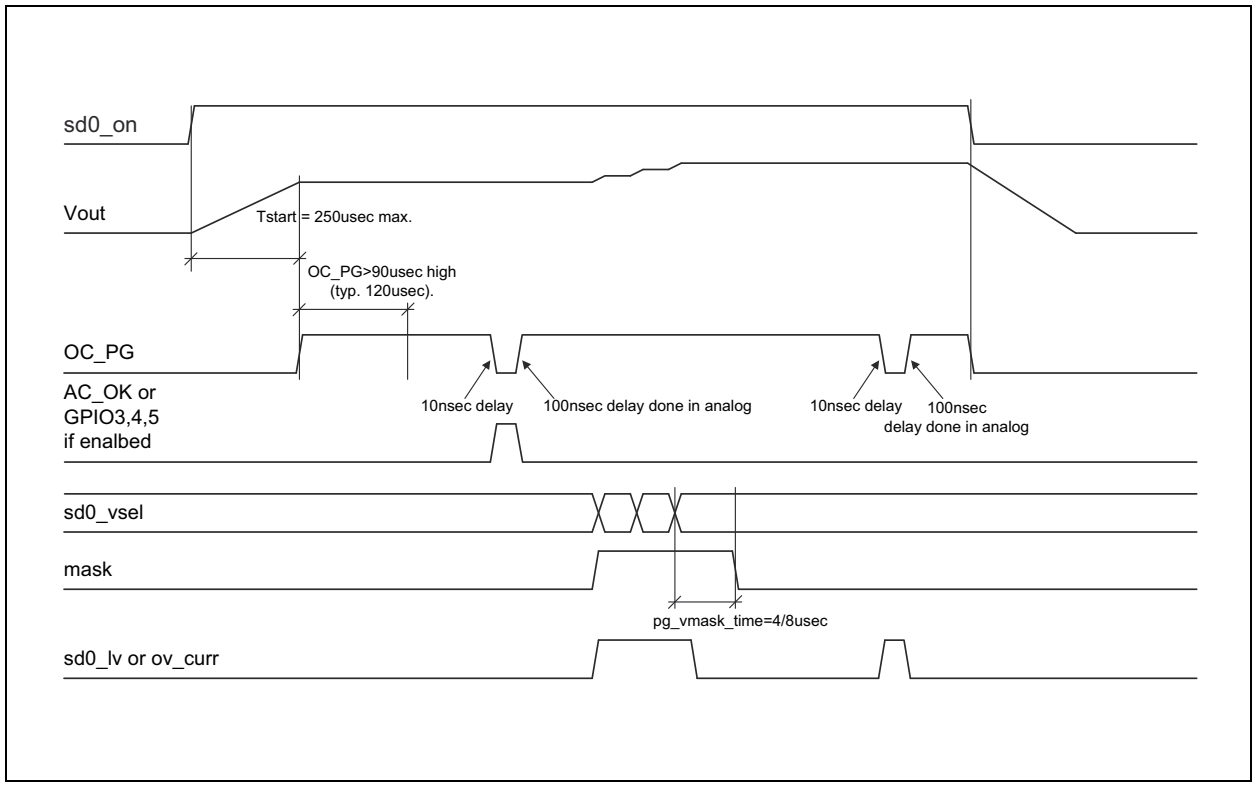
Is a dedicated output pin signaling over-current and power good events of SD0 plus additional inputs (see block diagram below).

Figure 65:
OC_PG Block Diagram



OC_PG Block Diagram: Shows the internal structure of the overcurrent-power-good output.

Figure 66:
OC_PG Timing Diagram



OC_PG Timing Diagram: Shows the signal timing of the overcurrent-power-good output.

Supervisor

The PMIC has a build in over-temperature protection, which could be switched off with the serial interface signal *temp_pmc_on* (enabled by default; it is not recommended to disable the over-temperature protection).

Temperature Supervision

The chip has three signals for the serial interface: *ov_temp_alarm0, ov_temp_alarm1* and *ov_temp_shutdown*. The flags *ov_temp_alarm0/1* are automatically reset if the over-temperature condition is removed, whereas *ov_temp_shutdown* has to be reset by the serial interface with the signal *rst_ov_temp_shutdown*.

If the flag *ov_temp_shutdown* is set, an automatic reset of the complete chip is initiated. The chip will only start-up when the temperature falls below the T_{alarm0} level (including hysteresis).

The flag *ov_temp_shutdown* is not affected by this reset cycle allowing the software to detect the reason for this unexpected shutdown:

A similar supervision is done for the power-stage dies. The over-temperature alarm flag (*temp_sdX_alarm*)is set, when a sub die reaches the alarm level. The over-temperature alarm flag is set anyway and cleared when the temperature falls below the threshold. When reaching the shutdown level an automatic reset (can be masked) of the AS3722 is initiated. The

corresponding status bit (*temp_sdX_shutdown*) can only be cleared by reading the register. It's possible to generate an interrupt (mask able) on reaching both the alarm and the shutdown level.

Figure 67:
Temperature Supervision Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{alarm0}	ov_temp_alarm0 rising threshold		79	94	109	°C
T_{alarm1}	ov_temp_alarm1 rising threshold		98	113	128	°C
$T_{shutdown}$	ov_temp_shutdown rising threshold		125	140	155	°C
T_{hyst}	ov_temp_110/140 hysteresis			5		°C
T_{SDx_alarm}	temp_sdX_alarm rising threshold		95	110	1125	°C
$T_{SDx_shutdown}$	temp_sdX_shutdown rising threshold		125	140	155	°C

Temperature Supervision Characteristic: Shows the key electrical parameter of the over-temperature supervision.

Current Supervision

All LDO's and DCDC step downs have an integrated over-current protection.

When a regulator runs into its current limit, the output voltage will drop and trigger a "low voltage" interrupt when hitting the threshold (-5% for SD0-6).

Watchdog

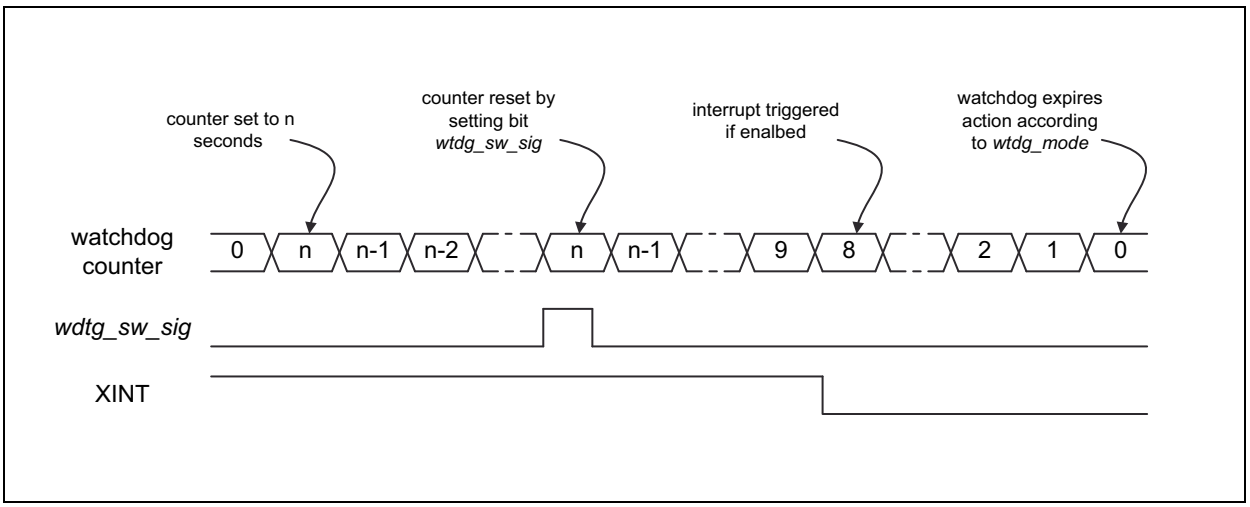
Description

The purpose of the watchdog is to detect a deadlock of the software. If the watchdog is active, it must receive a continuous trigger signal within a programmable time window. If there is no signal anymore for a certain time period from a defined pad or special serial interface bit, it starts either a complete reset cycle or initiates the power off sequence.

The watchdog is highly configurable by the following register bits:

- The complete block can be switched on by *wtdg_on = 1* and off by *wtdg_on* = 0.
- The watchdog time window is defined by the register *wtdg_timer* between 1s and 128s.
- The trigger signal can be either triggered by setting *wtdg_sw_sig* or using a HW signal on one of the GPIO pins *(gpioX_iosf*=9).
- If the watchdog expires, the system waits another second before reacting according to *wtdg_mode* (OTP setting)
- 0: interrupt 8s before the watchdog expires, only if the interrupt is not masked
- 1: reset_cycle with re-start
- 2: power_off
- 3: reset_cycle with re-start up to two times, if the watchdog expires a third time the systems goes into power_off
- Whether the watchdog caused a reset can be seen in the *reset_reason*.

Figure 68:
Watchdog Timing



Watchdog Timing: Shows the basic timing relations of the watchdog counter and related signals.

Interrupt Generation

Description

The interrupt controller generates an interrupt request for the host controller as soon as one or more of the bits in the *Interrupt* 1…3 register are set by pulling low pin XINT. All the interrupt sources can be enabled in the Interrupt Mask 1…3 register. The Interrupt 1…3 registers are cleared automatically after the host controller has read them. To prevent the AS3722device from losing an interrupt event, the register that is read is captured before it is transmitted to the host controller via the serial interface. As soon as the transmission of the captured value is complete a logical AND operation with the bit wise inverted captured value is applied to the register to clear all interrupt bits that have already been transmitted. Clearing the read interrupt bits takes 2 clock cycles, a read access to the same register before the clearing process has completed will yield a value of '0'. Note that an interrupt that has been present at the previous read access will be cleared as well in case it occurs again before the clearing process has completed.

10-Bit ADC

Description

This general purpose ADC can be used for measuring several voltages and currents to perform functions like battery monitor, temperature supervision, button press detection, etc.

Figure 69:
ADC Input Sources

#	Source	Range	LSB	Mode	Description
0	SD0_current	1.6V	1.56mV	1:1	output current of SD0
1	SD1_current	1.6V	1.56mV	1:1	output current of SD1
2	SD6_current	1.6V	1.56mV	1:1	output current of SD6
3	DIE temperature	1.6V	1.56mV	1:1	Tj = (0.7698 * ADC10<9:0>) - 274
4	VSUP	5.5V	6.25mV	4:1	check main system supply voltage
5	GPIO1	1.6V / 5.5V	1.56 / 6.25mV	1:1 / 4:1	
6	GPIO2	1.6V / 5.5V	1.56 / 6.25mV	1:1 / 4:1	
7	GPIO3	1.6V / 5.5V	1.56 / 6.25mV	1:1 / 4:1	
8	GPIO4	1.6V / 5.5V	1.56 / 6.25mV	1:1 / 4:1	
9	GPIO6	1.6V / 5.5V	1.56 / 6.25mV	1:1 / 4:1	
10	GPIO7	1.6V / 5.5V	1.56 / 6.25mV	1:1 / 4:1	
11	VBAT	15V	23.44mV	15:1	value valid below 15V only
12	PWM_CLK2/ ADC1	1.6V / 5.5V	1.56 / 6.25mV	1:1 / 4:1	
13	PWM_DAT2/ ADC2	1.6V / 5.5V	1.56 / 6.25mV	1:1 / 4:1	
14	-				reserved
15	-				reserved
16	TEMP1_SD0		1.56mV		Tj = 326.5 - ADC10<9:0> * 0.3734
17	TEMP2_SD0		1.56mV		Tj = 326.5 - ADC10<9:0> * 0.3734
18	TEMP3_SD0		1.56mV		Tj = 326.5 - ADC10<9:0> * 0.3734
19	TEMP4_SD0		1.56mV		Tj = 326.5 - ADC10<9:0> * 0.3734

#	Source	Range	LSB	Mode	Description
20	TEMP_SD1		1.56mV		Tj = 326.5 - ADC10<9:0> * 0.3734
21	TEMP1_SD6		1.56mV		Tj = 326.5 - ADC10<9:0> * 0.3734
22	TEMP2_SD6		1.56mV		Tj = 326.5 - ADC10<9:0> * 0.3734

ADC Input Sources: Shows the various inputs with the corresponding resolution which can be measured by the internal ADC.

The ADC-10 features 2 control register for measuring 2 different sources. By writing to the control register of channel 0 or channel 1 the selected measurement will be performed and the result placed in the corresponding result register. ADC10 has only one conversion unit, meaning measurements for source 1 and source 2 will be done time multiplexed.

ADC channel 1 is capable to perform automatic conversion in 0.5s or 1s intervals of the selected source. In addition a free programmable threshold with hysteresis (*ADC1_threshold_lo/hi*) can be set to generate interrupts once the threshold is passed.

adc1_interrupt_mode defines if an interrupt is generated on every threshold passing or only if the measured value rises above the high threshold or fall below the low threshold. The ADC interrupt can be masked as every other interrupt.

By setting *adc_buf_on* the buffered 1.6V ADC reference is available on GPIO7 during the conversion time. To give the ADC reference output enough time to settle the pre-sample time gets stretched from 32us to 62us. The *gpio7_mode* should be set to “3” (tristate) *gpio7_iosf* should be set to “0” (normal).

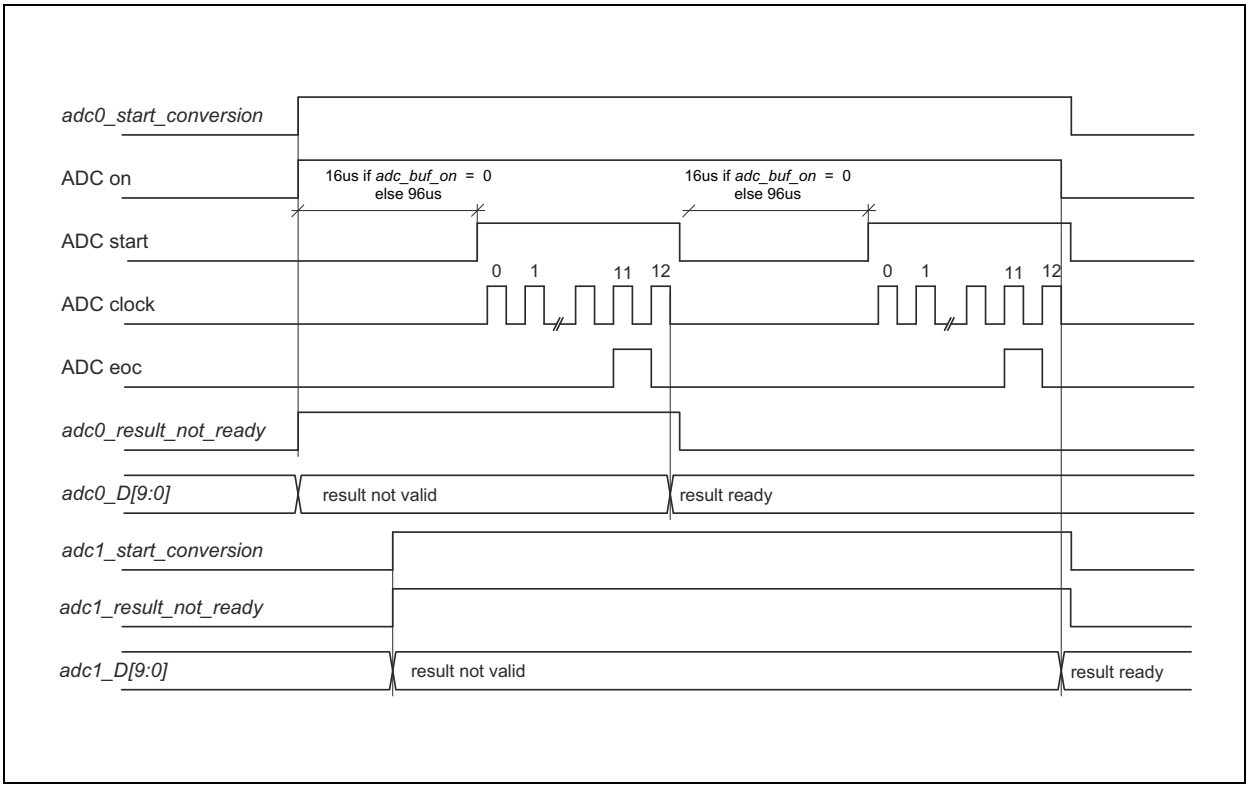
Parameter

Figure 70:
ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Resolution		10			Bit
Vin	Input Voltage Range	for 1:1 mode	0		1.6	V
DNL	Differential Nonlinearity	1LSB 1.56mV for 1:1 (depending on selected channel)		± 0.3		LSB
INL	Integral Nonlinearity			± 0.9		LSB
Vos	Input Offset Voltage			2		LSB
Rin	Input Impedance	1:1	100			MΩ
		4:1		200		kΩ
Cin	Input Capacitance				9	pF
Idd	Power Supply Current	during conversion only		500		µA
Idd	Power Down Current			100		nA
Transient Parameters (25°C)						
Tc	Conversion Time			40		µs
fc	Clock Frequency	internal CLK frequency/8		f_{clk_int}/ 8		kHz
ts	Settling time of S&H		1			µs
ADC Reference Buffer						
V_{OUT}	Output voltage		-1.2%	1.6	+1.2%	V
I_{OUT}	Output current	R_{OUT}>6.4kΩ	0		250	uA
C_{OUT}	Output capacitor		0		50	pF
t_{START}	Start-up time				10	us

ADC Characteristics: Shows the key electrical parameter of the internal ADC.

Figure 71:
ADC Timing Diagram



ADC Timing Diagram: Shows timing of the control and data signals of the internal ADC.

Real Time Clock

Description

The RTC module provides time information to the system. It is implemented as second counter derived from the 32kHz oscillator delivering the necessary accurate time base. The actual time can be read from the second, minute, hour, day month year registers in BCD format. Both 24h and am/pm mode is supported. All counters are set to 0 at a power-on-reset. The host controller can set the counter to any value by setting the RTC registers.

To prevent ambiguous time information because some of the registers being incremented before all of the registers have been read or written, a parallel shadow register is implemented. Every time a write/read access via the serial interface occurs the parallel shadow register is updated with the current value of the RTC counter. Any write access to the RTCsecond register will disable the update of the parallel shadow register and set the value of the appropriate byte of the parallel shadow register. Any subsequent write access to the RTCyear register will transfer the current value of the parallel shadow register to the RTCsecond/minute/hour/…/year register and the update of the parallel shadow register is enabled again. Similarly, any read access to the RTCsecond register will freeze the current value of the parallel shadow register and submit the appropriate byte

to the host controller via the serial interface. Any subsequent read access to the RTCyear register will enable the update of the parallel register again. This mechanism makes sure that the maximum error of the value that is written to or read from the registers is 1 second.

With the *rtc_lock* bit in OTP, the write access to the RTC registers can be locked and only be eabled by writing a “magic” word to the appropriate address.

To start the RTC, *rtc_on* bit has to be set to 1.
The RTC stops automatically at its highest value to prevent overrun.

Alarm

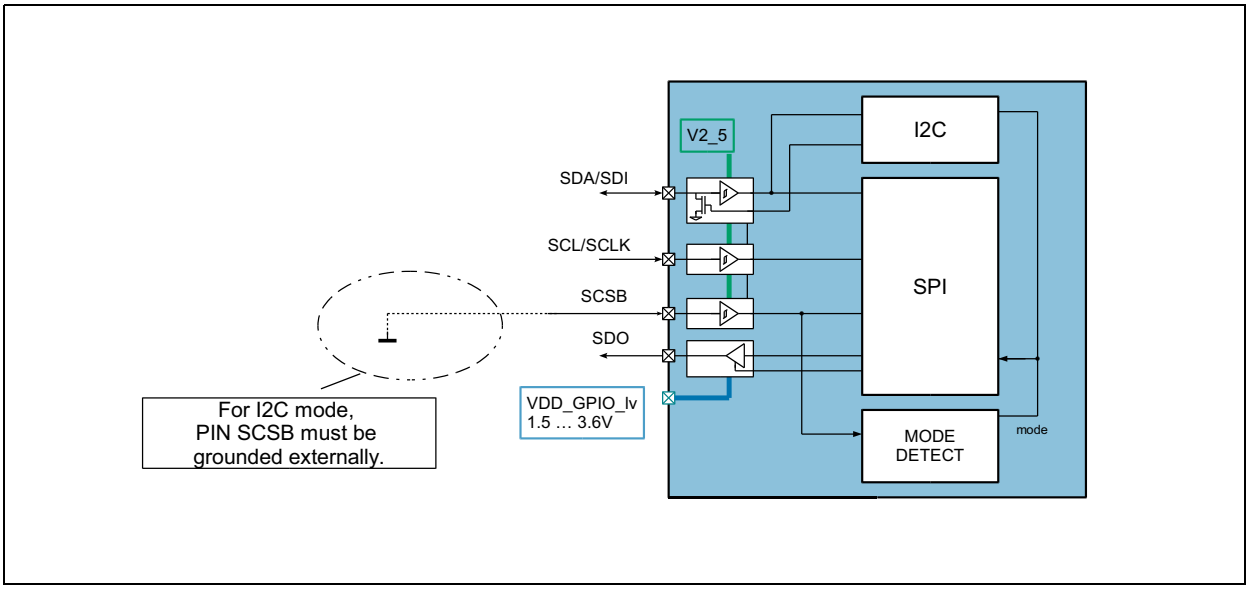
The RTC module includes an alarm function. When the content of the RTCAlarm registers equals the content of the RTC registers bit *rtc_alarm* will be set in the interrupt register. Furthermore the RTC module can generate a repeating interrupt every second, every minute, every 2 minutes or every 8 minutes.

To avoid ambiguous behavior during write access to the RTCAlarm registers any write access to the RTCAlarmSecond register will disable the alarm function; any subsequent write access to the RTCAlarmyear will enable the alarm function again.

Serial Control Interfaces

AS3722 features an I2C and SPI interface. Both interfaces are sharing the same pins and can therefore not be used at the same time.

Figure 72:
I2C-SPI Block Diagram



I2C-SPI Block Diagram: Shows the internal structure and connections between the I2C and SPI interface.

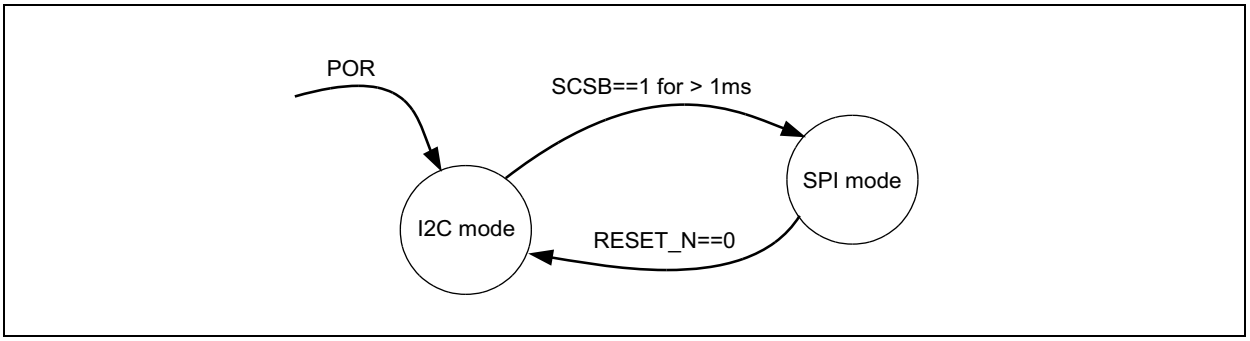
I2C-SPI Mode Selection

The AS3722 provides automatic selection of serial interface modes SPI and I2C. I2C/SPI configuration is chosen by the SPI chip select pin SCSB. Initially after power-on-reset the chip is in I2C mode. As soon as SCSB goes high for more than 1ms (with an internal de-bouncer in MODE DEDECT block), the device switches to SPI mode and stays in SPI mode till the next reset.

For SPI that means that the interface must go inactive (high) for >1ms before the first SPI access can be done.

For I2C mode operation the device pin SCSB must always be connected to ground.

Figure 73:
I2C-SPI Mode Selection



I2C-SPI Mode Selection: Shows the state diagram on how to change between the I2C and SPI interface.

I2C Feature List

- High Speed mode capability [max. SCL-frequency is 3.4MHz (2.7MHz for sequential reads)]
- 7+1-bit addressing mode
- 60h x 8-bit data registers (word address 0x00 - 0x60)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

I2C Protocol

Figure 74:
I2C Symbol Definition

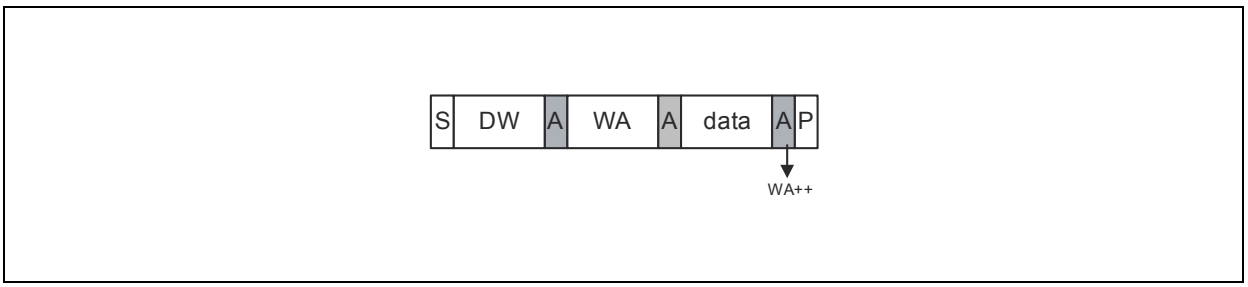
Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 0000b (80h)
DR	Device address for read	R	1000 0001b (81h)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	during acknowledge

I2C Symbol Definition: Shows the symbols used in the following mode descriptions.

I2C Write Access

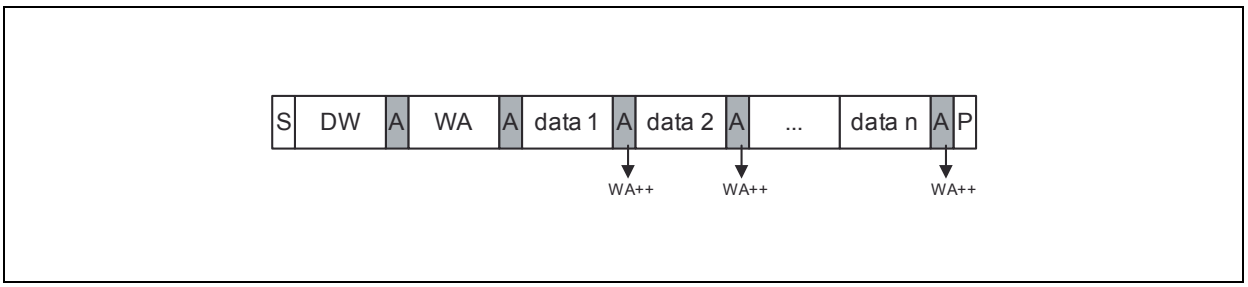
Byte Write and Page Write formats are used to write data to the slave.

Figure 75:
I2C Page Write



I2C Byte Write: Shows the format of an I2C byte write access.

Figure 76:
I2C Page Write



I2C Page Write: Shows the format of an I2C page write access.

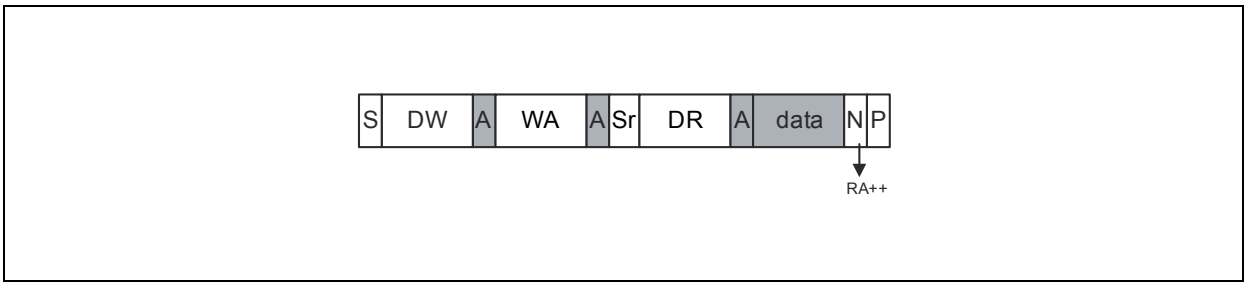
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

I2C Read Access

Random, Sequential and Current Address Read are used to read data from the slave.

Figure 77:
I2C Random Read



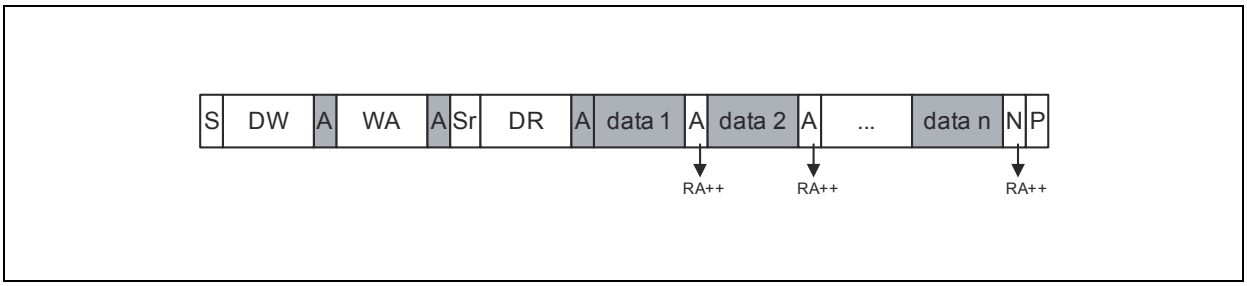
I2C Random Read: Shows the format of an I2C random read access.

Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

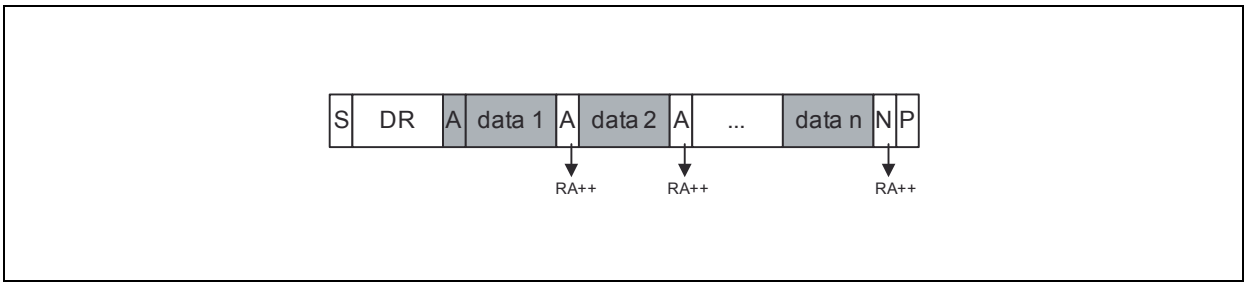
Figure 78:
I2C Sequential Read



I2C Sequential Read: Shows the format of an I2C sequential read access.

Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 79:
I2C Current Address Read



I2C Current Address Read: Shows the format of an I2C current address read access.

To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

I2C Parameter

Figure 80:
I2C Characteristics

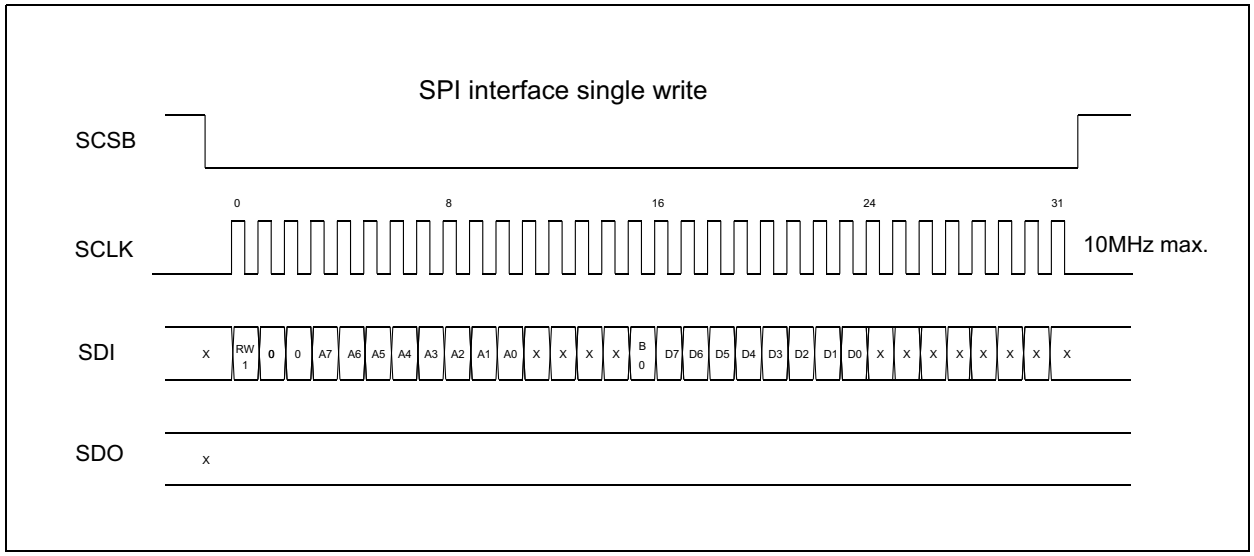
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	SCL,SDA Low Level input voltage		-0.3		0.4	V
V_{IH}	SCL,SDA High Level input voltage		1.4		VSUP_ GPIO	V
V_{OH}	High-Level Output Voltage	at -2.0mA	0.8x VDD_ GPIO_lv			V
V_{OL}	Low-Level Output Voltage	at 2.0mA			0.2x VDD_ GPIO_lv	V
C_{LOAD}	Capacitive Load	FS mode			400	pF
		HS mode			100	pF
R_{PULLUP}	Internal pull-up to VDD_GPIO_lv	SCL, SDA =2V, VDD_GPIO_LV=3V	1.5		2.9	kΩ
	external pull-up	HS mode		1		kΩ

I2C Characteristic: Shows the key electrical parameter of the I2C interface.

The AS3722 is compatible to the NXP two wire specification http://www.nxp.com/documents/user_manual/UM10204.pdf Version 4.0 Feb 2012 for standard mode, fast mode, fast mode plus and high speed mode (up to 2.7MHz for sequential reads).

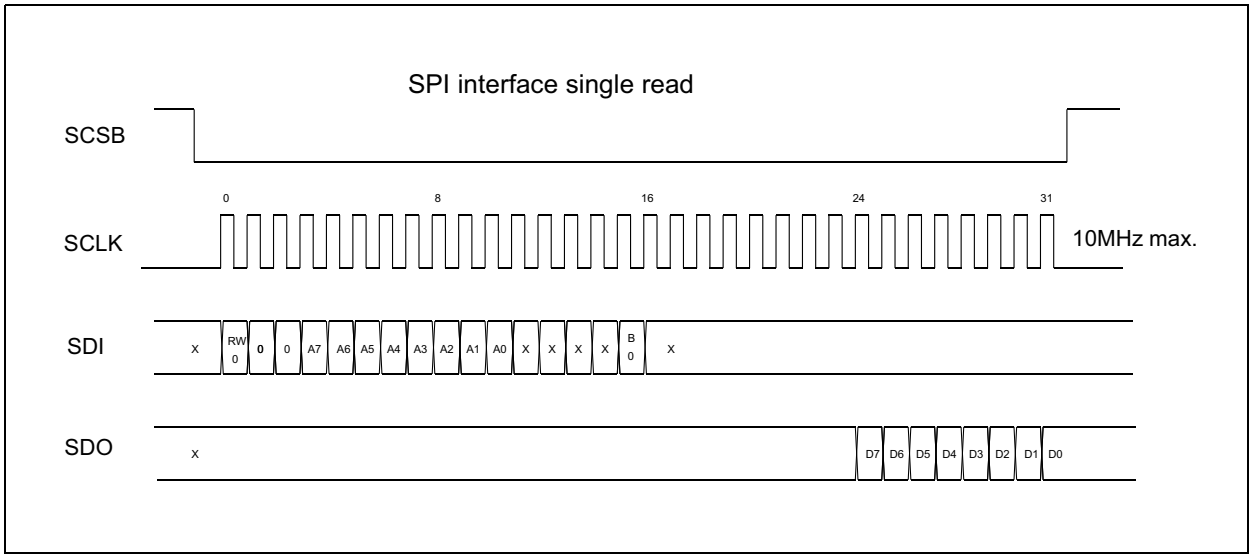
SPI Protocol

Figure 81:
SPI Single Write



SPI Single Write: Shows the timing of an SPI single write access.

Figure 82:
SPI Single Read



SPI Single Read: Shows the timing of an SPI single write read.

Data is captured at the falling edge of SCLK and written to SDO at the falling edge of SCLK. The maximum clock rate is 10MHz.

SPI Parameter

Figure 83:
SPI Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
SCLK/SDI/SCSB Pins						
V_{IH}	High-Level Input Voltage		1.4		VSUP_GPIO	V
V_{IL}	Low-Level Input Voltage				0.4	V
V_{HYS}	Hysteresis		0.2 x VSUP_GPIO			V
I_{LEAK}	Input Leakage Current	to VSUP_GPIO and GND_PAD	-5		5	µA
SDO Pin						
V_{OH}	High-Level Output Voltage	at -2.0mA	0.8 x VDD_GPIO_lv			V
V_{OL}	Low-Level Output Voltage	at 2.0mA			0.2 x VDD_GPIO_lv	V
C_{LOAD}	Capacitive Load				50	pF

SPI Characteristic: Shows the key electrical parameter of the SPI interface.

PMW DVS Control Interfaces

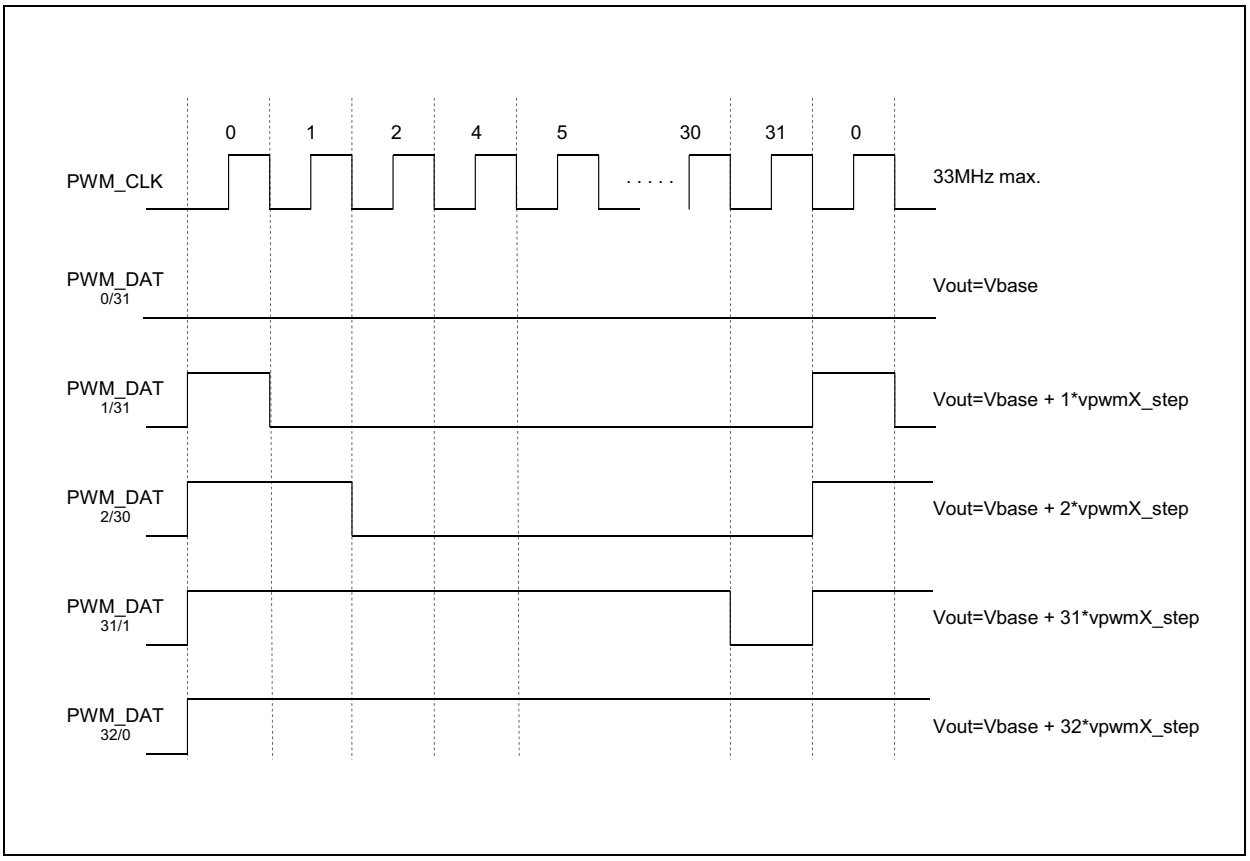
Description

Two dedicated PMW interfaces can be used to perform DVS on SD0 and SD6.

The voltage is determined by a base value (*vpwmX_base*) and the increments according to the duty cycle of the pwm signal. The step-size and reset behavior can be programmed individually for both interfaces.

A threshold value of 0.6-to 1.84V can be set in the OTP to limit the maximum allowed output voltage for each of the two regulators.

Figure 84:
PWM DVS Control



PWM DVS Control: Shows the PWM timing of the DVS interface for SD0 and SD6.

Parameter

Figure 85:
PWM Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Low level input voltage	digital input	–0.3		0.4	V
V_{IH}	High level input voltage	digital input	1.4		VSUP_GPIO	V

PWM Pin Characteristics: Shows the key electrical parameter of the PWM control pins. VSUP=2.7 to 5.5V; T amb = -20 to 70°C; unless otherwise mentioned

Register Description

Register Overview

Figure 86:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
00h	SD0Voltage	sd0_low_power					sd0_vsel<6:0>	
01h	SD1Voltage	sd0_low_power					sd1_vsel<6:0>	
02h	SD2Voltage	sd2_frequ					sd2_vsel<6:0>	
03h	SD3Voltage	sd3_frequ					sd3_vsel<6:0>	
04h	SD4Voltage	sd4_frequ					sd4_vsel<6:0>	
05h	SD5Voltage	sd5_frequ					sd5_vsel<6:0>	
06h	SD6Voltage	sd6_low_power					sd6_vsel<6:0>	
08h	GPIO0control	gpio0_invert			gpio0_iosf<6:3>			
09h	GPIO1control	gpio1_invert			gpio1_iosf<6:3>			
0Ah	GPIO2control	gpio2_invert			gpio2_iosf<6:3>			
0Bh	GPIO3control	gpio3_invert			gpio3_iosf<6:3>			
0Ch	GPIO4control	gpio4_invert			gpio4_iosf<6:3>			
0Dh	GPIO5control	gpio5_invert			gpio5_iosf<6:3>			
0Eh	GPIO6control	gpio6_invert			gpio6_iosf<6:3>			
0Fh	GPIO7control	gpio7_invert			gpio7_iosf<6:3>			
10h	LDO0Voltage	ldo0_ilimit	-				ldo0_vsel<	

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
11h	LDO1Voltage	ldo1_ilimit	ldo1_vsel<6:0>					
12h	LDO2Voltage	ldo2_ilimit	ldo2_vsel<6:0>					
13h	LDO3Voltage	ldo3_mode<7:6>		ldo3_vsel<5:0>				
14h	LDO4Voltage	ldo4_ilimit	ldo4_vsel<6:0>					
15h	LDO5Voltage	ldo5_ilimit	ldo5_vsel<6:0>					
16h	LDO6Voltage	ldo6_ilimit	ldo6_vsel<6:0>					
17h	LDO7Voltage	ldo7_ilimit	ldo7_vsel<6:0>					
19h	LDO9Voltage	ldo9_ilimit	ldo9_vsel<6:0>					
1Ah	LDO10Voltage	ldo10_ilimit	ldo10_vsel<6:0>					
1Bh	LDO11Voltage	ldo11_ilimit	ldo11_vsel<6:0>					
1Dh	LDO3_settings	-						
1Eh	GPIO_deb1	gpio3_deb<7:6>		gpio2_deb<5:4>		gpio1_deb<3:2>		
1Fh	GPIO_deb2	gpio7_deb<7:6>		gpio6_deb<5:4>		gpio5_deb<3:2>		
20h	GPIOsignal_out	gpio7_out	gpio6_out	gpio5_out	gpio4_out	gpio3_out	gpio2_out	
21h	GPIOsignal_in	gpio7_in	gpio6_in	gpio5_in	gpio4_in	gpio3_in	gpio2_in	
22h	Reg_sequ_mod1	-	sd6_sequ_on	sd5_sequ_on	sd4_sequ_on	sd3_sequ_on	sd2_sequ_on	
23h	Reg_sequ_mod2	ldo7_sequ_on	ldo6_sequ_on	ldo5_sequ_on	ldo4_sequ_on	ldo3_sequ_on	ldo2_sequ_on	
24h	Reg_sequ_mod3	-				ldo11_sequ_on	ldo10_sequ_on	

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
27h	SD_phsw_ctrl	-		sd0_nph_min<5:3>			sd6_phsw_on	
28h	SD_phsw_status	sdmph_clk_div<7:6>		-	sd6_nph_auto	sd1_nph_auto		
29h	SD0_control	sd0_trim_gm<7:6>		sd0_force_pwm	sd0_fast	sd0_combine_phase		
2Ah	SD1_control	sd1_trim_gm<7:6>		sd1_force_pwm	sd1_fast	sd1_combine_phase	sd0_low_noise	
2Bh	SDmph_control	disable_sd0_pulld	-	sd6_startslew<5:4>		sd1_startslew<3:2>		
2Ch	SD23_control	-	sd3_fast	sd3_force_pwm	sd3_low_noise	-	sd2_fast	
2Dh	SD4_control	-					sd4_fast	
2Eh	SD5_control	-					sd5_fast	
2Fh	SD6_control	sd6_trim_gm<7:6>		sd6_force_pwm	sd6_fast	sd6_combine_phase	sd6_ph2c_on	
30h	SD_dvm	-		dvm_time_sd6<5:4>		dvm_time_sd1<3:2>		
31h	Resetreason	reset_reason<7:4>				startup		
32h	Battery_voltage_monitor	FastResEn	SupResEn	ResVoltFall<5:3>				
33h	Startup_Control	-				onkey_lpress_reset	lid_rising_en	
34h	ResetTimer	-	stby_reset_enable	auto_off	off_delay<4:3>		-	

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
35h	ReferenceControl	force_softreset	-	clk_div2	standby_mode_on	clk_int<3:1>		
36h	ResetControl	-			reset_debounce<4:3>		onkey_input	
37h	OvertemperatureControl	-			ov_temp_alarm0	rst_ov_temp_shutdown	ov_temp_shutdown	ov
38h	WatchdogControl	-					wtdg_mode	
39h	Reg_standby_mod1	disable_regpd	sd6_stby_on	sd5_stby_on	sd4_stby_on	sd3_stby_on	sd2_stby_on	
3Ah	Reg_standby_mod2	ldo7_stby_on	ldo6_stby_on	ldo5_stby_on	ldo4_stby_on	ldo3_stby_on	ldo2_stby_on	
3Bh	Reg_standby_mod3	-				ldo11_stby_on	ldo10_stby_on	
3Ch	ENABLEctrl1	enable_ctrl_sd3<7:6>		enable_ctrl_sd2<5:4>		enable_ctrl_sd1<3:2>		
3Dh	ENABLEctrl2	-		enable_ctrl_sd6<5:4>		enable_ctrl_sd5<3:2>		
3Eh	ENABLEctrl3	enable_ctrl_ldo3<7:6>		enable_ctrl_ldo2<5:4>		enable_ctrl_ldo1<3:2>		
3Fh	ENABLEctrl4	enable_ctrl_ldo7<7:6>		enable_ctrl_ldo6<5:4>		enable_ctrl_ldo5<3:2>		
40h	ENABLEctrl5	enable_ctrl_ldo11<7:6>		enable_ctrl_ldo10<5:4>		enable_ctrl_ldo9<3:2>		
41h	pwm_control_l	pwm_l_time<7:0>						
42h	pwm_control_h	pwm_h_time<7:0>						
46h	Watchdog_timer	-	wtdg_timer<6:0>					
48h	WatchdogSoftwareSignal	pwm_div<7:6>		-				

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
49h	IOVoltage	-		INT_pull up	I2C_bus_p ullup	-		
4Ah	Battery_voltage_monit or2	-			vsup_min<4:2>			
4Dh	SDcontrol	-	sd6_enabl e	sd5_ena ble	sd4_enabl e	sd3_en able	sd2_enable	
4Eh	LDOcontrol0	ldo7_enable	ldo6_ena ble	ldo5_en able	ldo4_enab le	ldo3_e nable	ldo2_enable	
4Fh	LDOcontrol1	-				ldo11_ enable	ldo10_enable	
50h	SD0_protect	-					sd0_vmax<	
51h	SD6_protect	-					sd6_vmax<	
52h	PWM_vcontrol1	vpwm1_step	vpwm1_o n	vpwm1_vbase<5:0>				
53h	PWM_vcontrol2	vpwm2_step	vpwm2_o n	vpwm2_vbase<5:0>				
54h	PWM_vcontrol3	vpwm1_reset<7:6>		vpwm1_value<5:0>				
55h	PWM_vcontrol4	vpwm2_reset<7:6>		vpwm2_value<5:0>				
57h	BBcharger	BBCActive	BBCPwrSa ve	BBCVolt	BBCCur<4:3>		BBCResOff	
58h	CTRLsequ1	enable3_inv	onkey_no debounce	enable1 _stby_e n	enable1_in v	enable 2_inv	therm_inv	
59h	CTRLsequ2	lid_invert	ac_ok_inv ert	on_shutdown_delay<5:3>			onkey_invert	
5Ah	OVcurrent	-	sd1_ilimit<6:5>		sd0_ilimit<4:3>			s

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
5Bh	OVcurrent_deb	-			sd6_ilimit<4:3>		-	
5Ch	SDlv_deb	pg_sd6_vmask_time<7:6>		sd6_lv_deb<5:4>		sd1_lv_deb<3:2>		
5Dh	OC_pg_ctrl	pg_vresfall_mask	pg_ovcurr_sd0_mask	pg_pwrgood_sd0_mask	pg_gpio5_mask	pg_gpio4_mask	pg_gpio3_mask	p
5Eh	OC_pg_ctrl2	pg_ovcurr_sd6_mask	pg_pwrgood_sd6_mask	pg_sd6_ovc_alarm<5:3>			pg_vmask_tin	
5Fh	CTRLstatus	sd0_pwr_ok	enable3	enable2	enable1	ov_curr	therm	
60h	RTCcontrol	am_pm_mode	-	clk32out_en	rtc_irq_mode<4:3>		rtc_on	rtc_
61h	RTCsecond	-	second1<6:4>					sec
62h	RTCminute	-	minute1<6:4>					mir
63h	RTChour	pm	-	hour1<5:4>				ho
64h	RTCday	-		day1<5:4>				d
65h	RTCmonth	-			month1			mo
66h	RTCyear	-	year1<6:4>					ye
67h	RTCAlarmSecond	-	Alarmsecond1<6:4>					Alarms
68h	RTCAlarmMinute	-	Alarmminute1<6:4>					Alarm
69h	RTCAlarmHour	Alarmpm	-	Alarmhour1<5:4>				Alarn
6Ah	RTCAlarmday	-		Alarmday1<5:4>				Aları
6Bh	RTCAlarmmonth	-			Alarmmonth1			Alarm

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
6Ch	RTCAlarmyear	-	Alarmyear1<6:4>			Alarm		
6Dh	SRAM	SRAM<7:0>						
6Fh	RTC_Access	rtc_write_ena	-					
73h	RegStatus	-	sd6_lv	sd5_lv	sd4_lv	sd3_lv	sd2_lv	
74h	InterruptMask1	LowBat_int_m	ovtmp_int_m	onkey_int_m	onkey_lpress_int_m	occur_alarm_sd0_int_m	enable1_int_m	
75h	InterruptMask2	rtc_rep_int_m	sd6_lv_int_m	enable2_int_m	PWM2_ovprot_int_m	PWM1_ovprot_int_m	sd2345_lv_int_m	
76h	InterruptMask3	enable3_int_m	wtdg_int_m	gpio5_int_m	gpio4_int_m	gpio3_int_m	gpio2_int_m	
77h	InterruptMask4	adc_int_m	occur_alarm_sd6_int_m	temp_sd6_alarm_int_m	temp_sd1_alarm_int_m	temp_sd0_alarm_int_m	temp_sd6_shutdown_int_m	tem
78h	InterruptStatus1	LowBat_int_i	ovtmp_int_i	onkey_int_i	onkey_lpress_int_i	occur_alarm_sd0_int_i	enable1_int_i	
79h	InterruptStatus2	rtc_rep_int_i	sd6_lv_int_i	enable2_int_i	PWM2_ovprot_int_i	PWM1_ovprot_int_i	sd2345_lv_int_i	
7Ah	InterruptStatus3	enable3_int_i	wtdg_int_i	gpio5_int_i	gpio4_int_i	gpio3_int_i	gpio2_int_i	
7Bh	InterruptStatus4	adc_int_i	occur_alarm_sd6_int_i	temp_sd6_alarm_int_i	temp_sd1_alarm_int_i	temp_sd0_alarm_int_i	temp_sd6_shutdown_int_i	tem

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
7Dh	Temp_Status	-	temp_sd6_alarm	temp_sd1_alarm	temp_sd0_alarm	mask_ovtemp	temp_sd6_shutdown	tem
80h	ADC0_control	adc0_start_conversion	-	adc0_gpio_lv	adc0_select			
81h	ADC1_control	adc1_start_conversion	adc1_interval_scan	adc1_gpio_lv	adc1_select			
82h	ADC0_MSB_result	adc0_result_not_ready	adc0_D[9:3]<6:0>					
83h	ADC0_LSB_result	-						
84h	ADC1_MSB_result	adc1_result_not_ready	adc1_D[9:3]<6:0>					
85h	ADC1_LSB_result	-						
86h	ADC1_threshold_hi_MSB	-	adc1_threshold_hi[9:3]<6:0>					
87h	ADC1_threshold_hi_LSB	-						adc1_
88h	ADC1_threshold_lo_MSB	-	adc1_threshold_lo[9:3]<6:0>					
89h	ADC1_threshold_lo_LSB	-						adc1_
8Ah	ADC_configuration	-					adc_buf_on	adc
90h	ASIC_ID1	ID1<7:0>						
91h	ASIC_ID2	-						rev
9Eh	LockRegister	-						

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
A7h	Fuse7	sd5_slave	sd4_slave	sd3_slave	sd0_v_minus_200mV		-	
A8h	Fuse8	-	sd2_hcurr_tr	ldo3_vtrack_tr<5:4>		sd5_fast	sd4_fast	
A9h	Fuse9	auto_off	em_shutdown_direct	res_timer<5:4>		ResVoltRise<3:1>		
AAh	Fuse10	unique_id	power_off_at_vsuplow	i2c_deva_bit1	rtc_on	lid_pwr_on	ac_ok_pwr_on	
Abh	Fuse11	onkey_lpress_reset	onkey_shutdown_delay<6:5>		ac_ok_invert	onkey_invert	SupResEn	
Ach	Fuse12	sdmph_clk_div<7:6>		wtdg_mode<5:4>		wtdg_on	enable3_inv	
Adh	Fuse13	sd0_vmax_0<7:6>		sd6_trim_gm<5:4>		sd1_trim_gm<3:2>		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
Aeh	Fuse14	sd6_vmax_1<7:3>						
Afh	Fuse15	rtc_lock	-	I2C_bus_pullup	vsup_min<4:2>			
B0h	Fuse16	Reg3_delay	Reg3_select_MSB	Reg2_delay	Reg2_select_MSB	Reg1_delay	Reg1_select_MSB	
B1h	Fuse17	Reg1_select_LSB<7:4>				Reg0_s		
B2h	Fuse18	reg0_v<7:0>						
B3h	Fuse19	reg1_v<7:0>						
B4h	Fuse20	Reg3_select_LSB<7:4>				Reg2_s		
B5h	Fuse21	reg2_v<7:0>						
B6h	Fuse22	reg3_v<7:0>						

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
B7h	Fuse23	Reg7_delay	Reg7_select_MSB	Reg6_delay	Reg6_select_MSB	Reg5_delay	Reg5_select_MSB	
B8h	Fuse24	Reg5_select_LSB<7:4>				Reg4_s		
B9h	Fuse25	reg4_v<7:0>						
Bah	Fuse26	reg5_v<7:0>						
BBh	Fuse27	Reg7_select_LSB<7:4>				Reg6_s		
BCh	Fuse28	reg6_v<7:0>						
BDh	Fuse29	reg7_v<7:0>						
Beh	Fuse30	Reg11_delay	Reg11_select_MSB	Reg10_delay	Reg10_select_MSB	Reg9_delay	Reg9_select_MSB	
BFh	Fuse31	Reg9_select_LSB<7:4>				Reg8_s		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
C0h	Fuse32	reg8_v<7:0>						
C1h	Fuse33	reg9_v<7:0>						
C2h	Fuse34	Reg11_select_LSB<7:4>				Reg10_		
C3h	Fuse35	reg10_v<7:0>						
C4h	Fuse36	reg11_v<7:0>						
C5h	Fuse37	Reg15_delay	Reg15_select_MSB	Reg14_delay	Reg14_select_MSB	Reg13_delay	Reg13_select_MSB	
C6h	Fuse38	Reg13_select_LSB<7:4>				Reg12_		
C7h	Fuse39	reg12_v<7:0>						
C8h	Fuse40	reg13_v<7:0>						
C9h	Fuse41	Reg15_select_LSB<7:4>				Reg14_		

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
Cah	Fuse42_uniqueID0	reg14_v<7:0>						
CBh	Fuse43_uniqueID1	reg15_v<7:0>						
CCh	Fuse44_uniqueID2	ASIC_ID3				Reg17_delay	Reg17_select_MSB	
CDh	Fuse45_uniqueID3	Reg17_select_LSB<7:4>				Reg16_		
Ceh	Fuse46_uniqueID4	reg16_v<7:0>						
CFh	Fuse47_uniqueID5	reg17_v<7:0>						
E0h	Reg0_control	-	delay_time_stby	Reg0_delay_stby	Reg0_select_st			
E1h	Reg1_control	-		Reg1_delay_stby	Reg1_select_st			
E2h	Reg2_control	-		Reg2_delay_stby	Reg2_select_st			
E3h	Reg3_control	-		Reg3_delay_stby	Reg3_select_st			
E4h	Reg4_control	-		Reg4_delay_stby	Reg4_select_st			

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	
E5h	Reg5_control	-		Reg5_delay_stby				Reg5_select_st
E6h	Reg6_control	-		Reg6_delay_stby				Reg6_select_st
E7h	Reg7_control	-		Reg7_delay_stby				Reg7_select_st
E8h	Reg8_control	-		Reg8_delay_stby				Reg8_select_st
E9h	Reg9_control	-		Reg9_delay_stby				Reg9_select_st
Eah	Reg0_Voltage	Reg0_voltage_stby<7:0>						
Ebh	Reg1_Voltage	Reg1_voltage_stby<7:0>						
Ech	Reg2_Voltage	Reg2_voltage_stby<7:0>						
Edh	Reg3_Voltage	Reg3_voltage_stby<7:0>						
Eeh	Reg4_Voltage	Reg4_voltage_stby<7:0>						
Efh	Reg5_Voltage	Reg5_voltage_stby<7:0>						
F0h	Reg6_Voltage	Reg6_voltage_stby<7:0>						
F1h	Reg7_Voltage	Reg7_voltage_stby<7:0>						
F2h	Reg8_Voltage	Reg8_voltage_stby<7:0>						
F3h	Reg9_Voltage	Reg9_voltage_stby<7:0>						
F4h	SpareRegister1	disable_stby_lid_int						

Register Overview: Shows all the available registers.

Detailed Register Description

Figure 87:
Chip Revision ID

Chip Revision	ASIC_ID1 (90h)	ASIC_ID2 (91h)	ASIC_ID3 (CCh)
1v0	0Ch	0h	0h
1v1	0Ch	1h	0h
1v2	0Ch	1h	0h
1v21	0Ch	1h	1h

Figure 88:
SD0Voltage

Addr:00h		SD0Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	sd0_low_power	0	RW	Controls low power mode for sd0 0 : normal mode 1 : low power mode. Reduced current capability only 1 phase enabled and reduced output current on that phase
6:0	sd0_vsel	0	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. (0.61..1.5V) 00h : DC/DC powered down 01h-5Ah : V_SD0=0.6V+sd0_vsel*10mV 5Bh-7Fh : NA if sd0_v_minus_200mV=1 then (0.41..1.5V) 01h-6Eh : V_SD0=0.4V+sd0_vsel*10mV 6Fh-7Fh : NA

Figure 89:
SD1Voltage

Addr:01h		SD1Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd1_low_power	0	RW	Controls low power mode for sd1 0 : normal mode 1 : low power mode. Reduced current capability only 1 phase enabled and reduced output current on that phase
6:0	sd1_vsel	0	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. (0.61..1.5V) 00h : DC/DC powered down 01h-5Ah : V_SD1=0.6V+sd1_vsel*10mV 5Bh-7Fh : NA

Figure 90:
SD2Voltage

Addr:02h		SD2Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd2_frequ	0	RW	Selects between high and low frequency 0 : 3 MHz 1 : 4 MHz
6:0	sd2_vsel	0	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00h : DC/DC powered down 01h-40h : V_SD2=0.6V+sd2_vsel*12.5mV 41h-70h : V_SD2=1.4V+(sd2_vsel-40h)*25mV 71h-7Fh : V_SD2=2.6V+(sd2_vsel-70h)*50mV

Figure 91:
SD3Voltage

Addr:03h		SD3Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd3_frequ	0	RW	Selects between high and low frequency 0 : 3 MHz 1 : 4 MHz
6:0	sd3_vsel	0	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00h : DC/DC powered down 01h-40h : V_SD3=0.6V+sd3_vsel*12.5mV 41h-70h : V_SD3=1.4V+(sd3_vsel-40h)*25mV 71h-7Fh : V_SD3=2.6V+(sd3_vsel-70h)*50mV

Figure 92:
SD4Voltage

Addr:04h		SD4Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd4_frequ	0	RW	Selects between high and low frequency 0 : 3 MHz 1 : 4 MHz
6:0	sd4_vsel	0	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00h : DC/DC powered down 01h-40h : V_SD4=0.6V+sd4_vsel*12.5mV 41h-70h : V_SD4=1.4V+(sd4_vsel-40h)*25mV 71h-7Fh : V_SD4=2.6V+(sd4_vsel-70h)*50mV

Figure 93:
SD5Voltage

Addr:05h		SD5Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	sd5_frequ	0	RW	Selects between high and low frequency 0 : 3 MHz 1 : 4 MHz
6:0	sd5_vsel	0	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00h : DC/DC powered down 01h-40h : V_SD5=0.6V+sd5_vsel*12.5mV 41h-70h : V_SD5=1.4V+(sd5_vsel-40h)*25mV 71h-7Fh : V_SD5=2.6V+(sd5_vsel-70h)*50mV

Figure 94:
SD6Voltage

Addr:06h		SD6Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	sd6_low_power	0	RW	Controls low power mode for sd6 0 : normal mode 1 : low power mode. Reduced current capability only 1 phase enabled and reduced output current on that phase
6:0	sd6_vsel	0	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. (0.61..1.5V) 00h : DC/DC powered down 01h-5Ah : V_SD6=0.6V+sd6_vsel*10mV 5Bh-7Fh : NA

Figure 95:
GPIO0control

Addr:08h		GPIO0control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio0_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio0_iosf	0	RW	Select the GPIO special function 0 : Normal i/o operation 1 : Interrupt output 2 : VSUP_VBAT_low undebounced output 3 : GPIO interrupt input 4 : PWM input (internal PWM overide) 5 : Voltage_stby input: rising edge .. Goto Standby; (Leave standby by arbitrary interrupt) 6 : OC_PG_SD0 function on GPIO 7 : pwr_good output 8 : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used) 9 : Watchdog input 10 : NC 11 : Soft reset input 12 : PWM output 13 : VSUP_VBAT_low debounced output 14 : OC_PG_SD6 function on GPIO 15 : NC
2:0	gpio0_mode	3	RW_SM	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) VSUP_GPIO 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pull-up to VDD_GPIO_lv 5 : Input with pull-down 6 : Output/Input open drain (nmos) with pull-up to VDD_GPIO_lv, 7 : Output (push and pull) VDD_GPIO_lv

Figure 96:
GPIO1control

Addr:09h		GPIO1control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio1_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio1_iosf	0	RW	Select the GPIO special function 0 : Normal i/o operation 1 : Interrupt output 2 : VSUP_VBAT_low undebounced output 3 : GPIO interrupt input 4 : PWM input (internal PWM overide) 5 : Voltage_stby input: rising edge .. Goto Standby; (Leave standby by arbitrary interrupt) 6 : OC_PG_SD0 function on GPIO 7 : pwr_good output 8 : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used) 9 : Watchdog input 10 : NC 11 : Soft reset input 12 : PWM output 13 : VSUP_VBAT_low debounced output 14 : OC_PG_SD6 function on GPIO 15 : NC
2:0	gpio1_mode	3	RW_SM	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) VSUP_GPIO 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pull-up to VDD_GPIO_lv 5 : Input with pull-down 6 : Output/Input open drain (nmos) with pull-up to VDD_GPIO_lv, 7 : Output (push and pull) VDD_GPIO_lv

Figure 97:
GPIO2control

Addr:0ah		GPIO2control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio2_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio2_iosf	0	RW	Select the GPIO special function 0 : Normal i/o operation 1 : Interrupt output 2 : VSUP_VBAT_low undebounced output 3 : GPIO interrupt input 4 : PWM input (internal PWM overide) 5 : Voltage_stby input: rising edge .. Goto Standby; (Leave standby by arbitrary interrupt) 6 : OC_PG_SD0 function on GPIO 7 : pwr_good output 8 : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used) 9 : Watchdog input 10 : NC 11 : Soft reset input 12 : PWM output 13 : VSUP_VBAT_low debounced output 14 : OC_PG_SD6 function on GPIO 15 : NC
2:0	gpio2_mode	3	RW_SM	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) VSUP_GPIO 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pull-up to VDD_GPIO_lv 5 : Input with pull-down 6 : Output/Input open drain (nmos) with pull-up to VDD_GPIO_lv, 7 : Output (push and pull) VDD_GPIO_lv

Figure 98:
GPIO3control

Addr:0bh		GPIO3control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio3_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio3_iosf	0	RW	Select the GPIO special function 0 : Normal i/o operation 1 : Interrupt output 2 : VSUP_VBAT_low undebounced output 3 : GPIO interrupt input 4 : PWM input (internal PWM overide) 5 : Voltage_stby input: rising edge .. Goto Standby; (Leave standby by arbitrary interrupt) 6 : OC_PG_SD0 function on GPIO 7 : pwr_good output 8 : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used) 9 : Watchdog input 10 : NC 11 : Soft reset input 12 : PWM output 13 : VSUP_VBAT_low debounced output 14 : OC_PG_SD6 function on GPIO 15 : NC
2:0	gpio3_mode	3	RW_SM	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) VSUP_GPIO 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pull-up to VDD_GPIO_lv 5 : Input with pull-down 6 : Output/Input open drain (nmos) with pull-up to VDD_GPIO_lv, 7 : Output (push and pull) VDD_GPIO_lv

Figure 99:
GPIO4control

Addr:0ch		GPIO4control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio4_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio4_iosf	0	RW	Select the GPIO special function 0 : Normal i/o operation 1 : Interrupt output 2 : VSUP_VBAT_low undebounced output 3 : GPIO interrupt input 4 : PWM input (internal PWM overide) 5 : Voltage_stby input: rising edge .. Goto Standby; (Leave standby by arbitrary interrupt) 6 : OC_PG_SD0 function on GPIO 7 : pwr_good output 8 : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used) 9 : Watchdog input 10 : NC 11 : Soft reset input 12 : PWM output 13 : VSUP_VBAT_low debounced output 14 : OC_PG_SD6 function on GPIO 15 : NC
2:0	gpio4_mode	3	RW_SM	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) VSUP_GPIO 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pull-up to VDD_GPIO_lv 5 : Input with pull-down 6 : Output/Input open drain (nmos) with pull-up to VDD_GPIO_lv, 7 : Output (push and pull) VDD_GPIO_lv

Figure 100:
GPIO5control

Addr:0dh		GPIO5control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio5_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio5_iosf	0	RW	Select the GPIO special function 0 : Normal i/o operation 1 : Interrupt output 2 : VSUP_VBAT_low undebounced output 3 : GPIO interrupt input 4 : PWM input (internal PWM overide) 5 : Voltage_stby input: rising edge .. Goto Standby; (Leave standby by arbitrary interrupt) 6 : OC_PG_SD0 function on GPIO 7 : pwr_good output 8 : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used) 9 : Watchdog input 10 : NC 11 : Soft reset input 12 : PWM output 13 : VSUP_VBAT_low debounced output 14 : OC_PG_SD6 function on GPIO 15 : NC
2:0	gpio5_mode	3	RW_SM	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) VSUP_GPIO 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pull-up to VDD_GPIO_lv 5 : Input with pull-down 6 : Output/Input open drain (nmos) with pull-up to VDD_GPIO_lv, 7 : Output (push and pull) VDD_GPIO_lv

Figure 101:
GPIO6control

Addr:0eh		GPIO6control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio6_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio6_iosf	0	RW	Select the GPIO special function 0 : Normal i/o operation 1 : Interrupt output 2 : VSUP_VBAT_low undebounced output 3 : GPIO interrupt input 4 : PWM input (internal PWM overide) 5 : Voltage_stby input: rising edge .. Goto Standby; (Leave standby by arbitrary interrupt) 6 : OC_PG_SD0 function on GPIO 7 : pwr_good output 8 : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used) 9 : Watchdog input 10 : NC 11 : Soft reset input 12 : PWM output 13 : VSUP_VBAT_low debounced output 14 : OC_PG_SD6 function on GPIO 15 : NC
2:0	gpio6_mode	3	RW_SM	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) VSUP_GPIO 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pull-up to VDD_GPIO_lv 5 : Input with pull-down 6 : Output/Input open drain (nmos) with pull-up to VDD_GPIO_lv, 7 : Output (push and pull) VDD_GPIO_lv

Figure 102:
GPIO7control

Addr:0fh		GPIO7control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio7_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio7_iosf	0	RW	Select the GPIO special function 0 : Normal i/o operation 1 : Interrupt output 2 : VSUP_VBAT_low undebounced output 3 : GPIO interrupt input 4 : PWM input (internal PWM overide) 5 : Voltage_stby input: rising edge .. Goto Standby; (Leave standby by arbitrary interrupt) 6 : OC_PG_SD0 function on GPIO 7 : pwr_good output 8 : Q32k output (if osc_pd=1 then internal RC oscillator with 32kHz divider is used) 9 : Watchdog input 10 : NC 11 : Soft reset input 12 : PWM output 13 : VSUP_VBAT_low debounced output 14 : OC_PG_SD6 function on GPIO 15 : NC
2:0	gpio7_mode	3	RW_SM	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) VSUP_GPIO 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pull-up to VDD_GPIO_lv 5 : Input with pull-down 6 : Output/Input open drain (nmos) with pull-up to VDD_GPIO_lv, 7 : Output (push and pull) VDD_GPIO_lv

Figure 103:
LDO0Voltage

Addr:10h		LDO0Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo0_ilimit	0	RW	Sets limit of LDO0 (NMOS LDO) 0 : 150mA operating range 1 : 300mA operating range
4:0	ldo0_vsel	0	RW	The voltage select bits set the LDO output voltage 0.825V...1.25V, 25mV stepFs 00h : LDO off 01h-12h : V_LDO0=0.8V+ldo0_vsel*25mV

Figure 104:
LDO1Voltage

Addr:11h		LDO1Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo1_ilimit	0	RW	Sets limit of LDO1 (PMOS1 LDO) 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo1_vsel	0	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO off 01h-24h : V_LDO1=0.8V+ldo1_vsel*25mV 25h-3Fh : do not use 40h-7Fh : V_LDO1=1.725V+(ldo1_vsel-40h)*25mV

Figure 105:
LDO2Voltage

Addr:12h		LDO2Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo2_ilimit	0	RW	Sets limit of LDO2 (PMOS1 LDO) 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo2_vsel	0	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO off 01h-24h : V_LDO2=0.8V+ldo2_vsel*25mV 25h-3Fh : do not use 40h-7Fh : V_LDO2=1.725V+(ldo2_vsel-40h)*25mV

Figure 106:
LDO3Voltage

Addr:13h		LDO3Voltage		
Bit	Bit Name	Default	Access	Bit Description
7:6	ldo3_mode	0	RW	Sets Mode of LDO3 0 : PMOS LDO mode (VIN_LDO3 used) 1 : PMOS LDO in tracking SD1/SD6 mode, if SD1/SD6 enabled (SD1/SD6 selection in OTP) 2 : NMOS LDO mode (VIN_LDO3_LV used) 3 : Switch mode, if SD6 is enabled. (VIN_LDO3_SW used)
5:0	ldo3_vsel	0	RW	The voltage select bits set the LDO output voltage 0.62V...1.5V, 20mV steps 00h : LDO off 01h-2Dh : V_LDO3=0.6V+ldo3_vsel*20mV 2Eh-3Fh : do not use

Figure 107:
LDO4Voltage

Addr:14h		LDO4Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	ldo4_ilimit	0	RW	Sets limit of LDO4 (PMOS1 LDO) 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo4_vsel	0	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO off 01h-24h : V_LDO4=0.8V+ldo4_vsel*25mV 25h-3Fh : do not use 40h-7Fh : V_LDO4=1.725V+(ldo4_vsel-40h)*25mV

Figure 108:
LDO5Voltage

Addr:15h		LDO5Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	ldo5_ilimit	0	RW	Sets limit of LDO5 (PMOS1 LDO) 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo5_vsel	0	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO off 01h-24h : V_LDO5=0.8V+ldo5_vsel*25mV 25h-3Fh : do not use 40h-7Fh : V_LDO5=1.725V+(ldo5_vsel-40h)*25mV

Figure 109:
LDO6Voltage

Addr:16h		LDO6Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	ldo6_ilimit	0	RW	Sets limit of LDO6 (PMOS1 LDO) 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo6_vsel	0	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO off 01h-24h : V_LDO6=0.8V+ldo6_vsel*25mV 25h-3Eh : do not use 3Fh : bypass mode 40h-7fh : V_LDO6=1.725V+(ldo6_vsel-40h)*25mV

Figure 110:
LDO7Voltage

Addr:17h		LDO7Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	ldo7_ilimit	0	RW	Sets limit of LDO7 (PMOS1 LDO) 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo7_vsel	0	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO off 01h-24h : V_LDO7=0.8V+ldo7_vsel*25mV 25h-3Fh : do not use 40h-7Fh : V_LDO7=1.725V+(ldo7_vsel-40h)*25mV

Figure 111:
LDO9Voltage

Addr:19h		LDO9Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	ldo9_ilimit	0	RW	Sets limit of LDO9 (PMOS1 LDO) 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo9_vsel	0	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO off 01h-24h : V_LDO9=0.8V+ldo9_vsel*25mV 25h-3Fh : do not use 40h-7Fh : V_LDO9=1.725V+(ldo9_vsel-40h)*25mV

Figure 112:
LDO10Voltage

Addr:1ah		LDO10Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	ldo10_ilimit	0	RW	Sets limit of LDO10 (PMOS1 LDO) 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo10_vsel	0	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO off 01h-24h : V_LDO10=0.8V+ldo10_vsel*25mV 25h-3Fh : do not use 40h-7Fh : V_LDO10=1.725V+(ldo10_vsel-40h)*25mV

Figure 113:
LDO11Voltage

Addr:1bh		LDO11Voltage		
Bit	Bit Name	Default	Access	Bit Description
7	ldo11_ilimit	0	RW	Sets limit of LDO11 (PMOS1 LDO) 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo11_vsel	0	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO off 01h-24h : V_LDO11=0.8V+ldo11_vsel*25mV 25h-3Fh : do not use 40h-7Fh : V_LDO11=1.725V+(ldo11_vsel-40h)*25mV

Figure 114:
LDO3_settings

Addr:1dh		LDO3_settings		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1:0	ldo3_vtrack_tr	0	RW_SM	Selects offset a trimming for tracking mode 0 : no offset 1 : +10mV offset of LDO3 at 1.2V Vout (+0.83%) 2 : +20mV offset of LDO3 at 1.2V Vout (+1.66%) 3 : +30mV offset of LDO3 at 1.2V Vout (+2.5%)

Figure 115:
GPIO_deb1

Addr:1eh		GPIO_deb1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	gpio3_deb	0	RW	Sets debounce time on GPIO input 00h : no debounce time 01h : approx. 100 us 02h : approx. 1 ms 03h : approx. 10 ms
5:4	gpio2_deb	0	RW	Sets debounce time on GPIO input 00h : no debounce time 01h : approx. 100 us 02h : approx. 1 ms 03h : approx. 10 ms
3:2	gpio1_deb	0	RW	Sets debounce time on GPIO input 00h : no debounce time 01h : approx. 100 us 02h : approx. 1 ms 03h : approx. 10 ms
1:0	gpio0_deb	0	RW	Sets debounce time on GPIO input 00h : no debounce time 01h : approx. 100 us 02h : approx. 1 ms 03h : approx. 10 ms

Figure 116:
GPIO_deb2

Addr:1fh		GPIO_deb2		
Bit	Bit Name	Default	Access	Bit Description
7:6	gpio7_deb	0	RW	Sets debounce time on GPIO input 00h : no debounce time 01h : approx. 100 us 02h : approx. 1 ms 03h : approx. 10 ms
5:4	gpio6_deb	0	RW	Sets debounce time on GPIO input 00h : no debounce time 01h : approx. 100 us 02h : approx. 1 ms 03h : approx. 10 ms
3:2	gpio5_deb	0	RW	Sets debounce time on GPIO input 00h : no debounce time 01h : approx. 100 us 02h : approx. 1 ms 03h : approx. 10 ms
1:0	gpio4_deb	0	RW	Sets debounce time on GPIO input 00h : no debounce time 01h : approx. 100 us 02h : approx. 1 ms 03h : approx. 10 ms

Figure 117:
GPIOsignal_out

Addr:20h		GPIOsignal_out		
Bit	Bit Name	Default	Access	Bit Description
7	gpio7_out	0	RW	This bit determines the output signal of the GPIO7 pin when selected as output source
6	gpio6_out	0	RW	This bit determines the output signal of the GPIO6 pin when selected as output source
5	gpio5_out	0	RW	This bit determines the output signal of the GPIO5 pin when selected as output source
4	gpio4_out	0	RW	This bit determines the output signal of the GPIO4 pin when selected as output source
3	gpio3_out	0	RW	This bit determines the output signal of the GPIO3 pin when selected as output source
2	gpio2_out	0	RW	This bit determines the output signal of the GPIO2 pin when selected as output source

Addr:20h		GPIOsignal_out		
Bit	Bit Name	Default	Access	Bit Description
1	gpio1_out	0	RW	This bit determines the output signal of the GPIO1 pin when selected as output source
0	gpio0_out	0	RW	This bit determines the output signal of the GPIO0 pin when selected as output source

Figure 118:
GPIOsignal_in

Addr:21h		GPIOsignal_in		
Bit	Bit Name	Default	Access	Bit Description
7	gpio7_in	0	RO	This bit reflects the logic level of the GPIO7 pin when configured as digital input pin
6	gpio6_in	0	RO	This bit reflects the logic level of the GPIO6 pin when configured as digital input pin
5	gpio5_in	0	RO	This bit reflects the logic level of the GPIO5 pin when configured as digital input pin
4	gpio4_in	0	RO	This bit reflects the logic level of the GPIO4 pin when configured as digital input pin
3	gpio3_in	0	RO	This bit reflects the logic level of the GPIO3 pin when configured as digital input pin
2	gpio2_in	0	RO	This bit reflects the logic level of the GPIO2 pin when configured as digital input pin
1	gpio1_in	0	RO	This bit reflects the logic level of the GPIO1 pin when configured as digital input pin
0	gpio0_in	0	RO	This bit reflects the logic level of the GPIO0 pin when configured as digital input pin

Figure 119:
Reg_sequ_mod1

Addr:22h		Reg_sequ_mod1		
Bit	Bit Name	Default	Access	Bit Description
6	sd6_sequ_on	0	RW_SS	Step down 6 controlled by sequencer for ramping down (reset or power_off)
5	sd5_sequ_on	0	RW_SS	Step down 5 controlled by sequencer for ramping down (reset or power_off)

Addr:22h		Reg_sequ_mod1		
Bit	Bit Name	Default	Access	Bit Description
4	sd4_sequ_on	0	RW_SS	Step down 4 controlled by sequencer for ramping down (reset or power_off)
3	sd3_sequ_on	0	RW_SS	Step down 3 controlled by sequencer for ramping down (reset or power_off)
2	sd2_sequ_on	0	RW_SS	Step down 2 controlled by sequencer for ramping down (reset or power_off)
1	sd1_sequ_on	0	RW_SS	Step down 1 controlled by sequencer for ramping down (reset or power_off)
0	sd0_sequ_on	0	RW_SS	Step down 0 controlled by sequencer for ramping down (reset or power_off)

Figure 120:
Reg_sequ_mod2

Addr:23h		Reg_sequ_mod2		
Bit	Bit Name	Default	Access	Bit Description
7	ldo7_sequ_on	0	RW_SS	LDO8 controlled by sequencer for ramping down (reset or power_off)
6	ldo6_sequ_on	0	RW_SS	LDO7 controlled by sequencer for ramping down (reset or power_off)
5	ldo5_sequ_on	0	RW_SS	LDO6 controlled by sequencer for ramping down (reset or power_off)
4	ldo4_sequ_on	0	RW_SS	LDO5 controlled by sequencer for ramping down (reset or power_off)
3	ldo3_sequ_on	0	RW_SS	LDO4 controlled by sequencer for ramping down (reset or power_off)
2	ldo2_sequ_on	0	RW_SS	LDO3 controlled by sequencer for ramping down (reset or power_off)
1	ldo1_sequ_on	0	RW_SS	LDO2 controlled by sequencer for ramping down (reset or power_off)
0	ldo0_sequ_on	0	RW_SS	LDO1 controlled by sequencer for ramping down (reset or power_off)

Figure 121:
Reg_sequ_mod3

Addr:24h		Reg_sequ_mod3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	ldo11_sequ_on	0	RW_SS	LDO11 controlled by sequencer for ramping down (reset or power_off)
2	ldo10_sequ_on	0	RW_SS	LDO10 controlled by sequencer for ramping down (reset or power_off)
1	ldo9_sequ_on	0	RW_SS	LDO9 controlled by sequencer for ramping down (reset or power_off)

Figure 122:
SD_phsw_ctrl

Addr:27h		SD_phsw_ctrl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5:3	sd0_nph_min	0	RW	Select the minimum number of phases for automatic phaseswitching of SD0 0 : 1 phase 1 : 2 phases 2 : 3 phases 3 : 4 phases 4 : NA 5 : 6 phases 6 : NA 7 : 8 phases
2	sd6_phsw_on	0	RW	Switch on automatic phase switching for sd6
1	sd1_phsw_on	0	RW	Switch on automatic phase switching for sd1
0	sd0_phsw_on	0	RW	Switch on automatic phase switching for sd0

Figure 123:
SD_phsw_status

Addr:28h		SD_phsw_status		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	sdmph_clk_div	0	RW_SM	Divide clock of sd0,sd1,sd6 by 1,2 or 4 0 : 2.7MHz 1 : 1.35MHz 2 : 0.675MHz 3 : 0.675MHz
4	sd6_nph_auto	0	R	Status of the actual number of phases used ,if phase switching enabled 0 : 1 phase 1 : 2 phases
3	sd1_nph_auto	0	R	Status of the actual number of phases used ,if phase switching enabled 0 : 1 phase 1 : 2 phases
2:0	sd0_nph_auto	0	R	Status of the actual number of phases used ,if phase switching enabled 0 : 1 phase 1 : 2 phases 2 : 3 phases 3 : 4 phases 4 : NA 5 : 6 phases 6 : NA 7 : 8 phases

Figure 124:
SD0_control

Addr:29h		SD0_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	sd0_trim_gm	0	RW_SM	Selects gm setting of OTA 0 : fast setting 1 : slow setting 2 : medium setting 3 : very slow setting
5	sd0_force_pwm	0	RW	Selects force pwm mode 0 : normal mode 1 : force pwm, inverted coil current possible to keep the fixed frequency
4	sd0_fast	0	RW	Selects a faster regulation mode for SD0 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required
3	sd0_combine_phase	0	RW_SM	Selects phase mode (set during startup power_stage test) 0 : normal mode 1 : combine phase 1 and 2 , 3 and 4, 5 and 6, 7 and 8
2:0	sd0_phases	0	RW_SM	Selects number of phases for sd0 (set during startup power_stage test, can be changed after that) 0 : 1 phases used 1 : 2 phases used 2 : 3 phases used 3 : 4 phases used 4 : 5 phases used 5 : 6 phases used 6 : 7 phases used 7 : 8 phases used

Figure 125:
SD1_control

Addr:2ah		SD1_control		
Bit	Bit Name	Default	Access	Bit Description
7:6	sd1_trim_gm	0	RW_SM	Selects gm setting of OTA 0 : fast setting 1 : slow setting 2 : medium setting 3 : very slow setting
5	sd1_force_pwm	0	RW	Selects force pwm mode 0 : normal mode 1 : force pwm, inverted coil current possible to keep the fixed frequency
4	sd1_fast	0	RW	Selects a faster regulation mode for SD1 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required
3	sd1_combine_phase	0	RW_SM	Selects phase mode (set during startup power_stage test) 0 : normal mode 1 : combine phase 1 and 2
2	sd0_low_noise	0	RW	Enables low noise mode of SD0. If enabled smaller current pulses and output ripple are activated 0 : Normal mode. Minimum current pulses of about 10% the current limit are applied in skip mode 1 : Low noise mode. Only minimum on time applied in skip mode
1	sd1_low_noise	0	RW	Enables low noise mode of SD1. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of about 10% the current limit are applied in skip mode 1 : Low noise mode. Only minimum on time applied in skip mode
0	sd1_phases	1	RW_SM	Selects number of phases for sd1 (set during startup power_stage test, can be changed after that) 0 : 1 phase used 1 : 2 phases used

Figure 126:
SDmph_control

Addr:2bh		SDmph_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	disable_sd0_pulld	0	RW	Disable Regulator SD0 pull-down 0 : normal mode (pull-down if SD0 is disabled) 1 : pull-down disabled (only if sd0 controlled by enable1/2/3 in active (ON) state)
5:4	sd6_startslew	0	RW	Sets the startup slew rate of SD6 0 : 5mV / us 1 : 10mV / us 2 : 20mV / us 3 : 40mV / us
3:2	sd1_startslew	0	RW	Sets the startup slew rate of SD1 0 : 5mV / us 1 : 10mV / us 2 : 20mV / us 3 : 40mV / us
1:0	sd0_startslew	0	RW	Sets the startup slew rate of SD0 0 : 5mV / us 1 : 10mV / us 2 : 20mV / us 3 : 40mV / us

Figure 127:
SD23_control

Addr:2ch		SD23_control		
Bit	Bit Name	Default	Access	Bit Description
6	sd3_fast	0	RW_SS	Selects a faster regulation mode for SD3 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required
5	sd3_force_pwm	0	RW	Selects force pwm mode 0 : normal mode 1 : force pwm, inverted coil current possible to keep the fixed frequency
4	sd3_low_noise	0	RW	Enables low noise mode of SD3. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of about 10% the current limit are applied in skip mode 1 : Low noise mode. Only minimum on time applied in skip mode
2	sd2_fast	0	RW_SS	Selects a faster regulation mode for SD2 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required
1	sd2_force_pwm	0	RW	Selects force pwm mode 0 : normal mode 1 : force pwm, inverted coil current possible to keep the fixed frequency
0	sd2_low_noise	0	RW	Enables low noise mode of SD2. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of about 10% the current limit are applied in skip mode 1 : Low noise mode. Only minimum on time applied in skip mode

Figure 128:
SD4_control

Addr:2dh		SD4_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	sd4_fast	0	RW_SS	Selects a faster regulation mode for SD4 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required
1	sd4_force_pwm	0	RW	Selects force pwm mode 0 : normal mode 1 : force pwm, inverted coil current possible to keep the fixed frequency
0	sd4_low_noise	0	RW	Enables low noise mode of SD4. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of about 10% the current limit are applied in skip mode 1 : Low noise mode. Only minimum on time applied in skip mode

Figure 129:
SD5_control

Addr:2eh		SD5_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	sd5_fast	0	RW_SS	Selects a faster regulation mode for SD5 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required
1	sd5_force_pwm	0	RW	Selects force pwm mode 0 : normal mode 1 : force pwm, inverted coil current possible to keep the fixed frequency
0	sd5_low_noise	0	RW	Enables low noise mode of SD5. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of about 10% the current limit are applied in skip mode 1 : Low noise mode. Only minimum on time applied in skip mode

Figure 130:
SD6_control

Addr:2fh		SD6_control		
Bit	Bit Name	Default	Access	Bit Description
7:6	sd6_trim_gm	0	RW_SM	Selects gm setting of OTA 0 : fast setting 1 : slow setting 2 : medium setting 3 : very slow setting
5	sd6_force_pwm	0	RW	Selects force pwm mode 0 : normal mode 1 : force pwm, inverted coil current possible to keep the fixed frequency
4	sd6_fast	0	RW	Selects a faster regulation mode for SD6 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required
3	sd6_combine_phase	0	RW_SM	Selects phase mode (set during startup subdie test) 0 : normal mode 1 : combine phase 1 and 2
2	sd6_ph2c_on	0	RW_SM	Selects high current mode of SD6 (doubled current) (set during startup subdie test) 0 : normal mode (only one supdie connected) 1 : second subdie on pin TEMP2_SD6 detected (short CTRL1 and CTRL2 of each subdie and connect to CTRL1_SD6 and CTRL2_SD6)
1	sd6_low_noise	0	RW	Enables low noise mode of SD6. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of about 100f the current limit are applied in skip mode 1 : Low noise mode. Only minimum on time applied in skip mode
0	sd6_phases	1	RW_SM	Selects number of phases for SD6 (set during startup subdie test, can be changed after that) 0 : 1 phase used 1 : 2 phases used

Figure 131:
SD_dvm

Addr:30h		SD_dvm		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5:4	dvm_time_sd6	0	RW	Time steps of DVM voltage change of selected step down If voltage of step Down is changed during operation (sdx_vsel) voltage is de/increased 0 : immediate change (no DVM) 1 : 40mV/us 2 : 10mV/us 3 : 5mV/us
3:2	dvm_time_sd1	0	RW	Time steps of DVM voltage change of selected step down If voltage of step Down is changed during operation (sdx_vsel) voltage is de/increased 0 : immediate change (no DVM) 1 : 40mV/us 2 : 10mV/us 3 : 5mV/us
1:0	dvm_time_sd0	0	RW	Time steps of DVM voltage change of selected step down If voltage of step Down is changed during operation (sdx_vsel) voltage is de/increased 0 : immediate change (no DVM) 1 : 40mV/us 2 : 10mV/us 3 : 5mV/us

Figure 132:
Resetreason

Addr:31h		Resetreason		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	reset_reason	0	RW_SM	This flag indicates the exit of active mode reason 0 : VPOR has been reached (battery or supply insertion from scratch) 1 : ResVoltFall reached by VBAT or vsup_min reached by VSUP 2 : Software forced by force_reset (soft or hard) 3 : Software forced by power_off 4 : ONKEY longpress has been detected 5 : XRES_IN pin 6 : THERM pin 7 : overtemperature T140 (die, SD0, SD1, or SD6) 8 : watchdog 9 : VSUP overvoltage reached 10 : Transition to standby mode
3:0	startup_reason	0	RW_SM	This flag indicates the startup reason after power off 0 : VPOR has been reached (battery or supply insertion from scratch) 1 : ONKEY has been pulled high in power off mode 2 : AC_OK has been detected in power off mode 3 : LID has been detected in power off mode 4 : RTC wakeup has been detected in power off mode 5 : Interrupt in standby mode has been detected 6 : Reset cycle 7 : Soft reset cycle 8 : ResVoltRise was reached

Figure 133:
Battery_voltage_monitor

Addr:32h		Battery_voltage_monitor		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	FastResEn	0	RW	0 : ResVoltFall debounce time = 4 ms 1 : ResVoltFall debounce time = 4 us
6	SupResEn	0	RW_SS	0 : A reset is generated if VBAT or VSUP falls below 2.5V. If VBAT falls below ResVoltFall only an interrupt is generated (if enabled) and the uProcessor can shut down the system) 1 : A reset is generated if VBAT falls below ResVoltFall or VSUP falls below vsup_min
5:3	ResVoltFall	0	RW_SM	This value determines the reset level ResVoltFall for falling VBAT. For stacked battery systems (ncells>0) the level gets multiplied with the number of cells. It is recommended to set this value at least 200mV lower than ResVoltRise 0 : 2.5V * (ncells+1) 1 : 2.7V * (ncells+1) 2 : 2.95V * (ncells+1) 3 : 3.1V * (ncells+1) 4 : 3.2V * (ncells+1) 5 : 3.3V * (ncells+1) 6 : 3.4V * (ncells+1) 7 : 3.6V * (ncells+1)
2:0	ResVoltRise	0	RW_SM	This value determines the reset level ResVoltRise for rising VBAT. For stacked battery systems (ncells>0) the level gets multiplied with the number of cells. It is recommended to set this value at least 200mV higher than ResVoltFall 0 : 2.5V * (ncells+1) 1 : 2.7V * (ncells+1) 2 : 2.95V * (ncells+1) 3 : 3.1V * (ncells+1) 4 : 3.2V * (ncells+1) 5 : 3.3V * (ncells+1) 6 : 3.4V * (ncells+1) 7 : 3.6V * (ncells+1)

Figure 134:
Startup_Control

Addr:33h		Startup_Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	onkey_lpress_reset	0	RW_SS	Selects behavior on onkey_lpress 0 : change to power_off mode on long press 1 : apply reset on long press
2	lid_rising_en	0	RW	Select LID detection in power off mode Read write 0 : Exit of Power Off mode, if LID is detected (level detection) 1 : Exit of Power Off mode, if LID active is detected (rising edge detection after possible inversion)
1	ac_ok_rising_en	0	RW	Select AC_OK detection in power off mode Read Write 0 : Exit of Power Off mode, if AC_OK is detected (level detection) 1 : Exit of Power Off mode, if AC_OK active is detected (rising edge detection after possible inversion)
0	power_off_at_vsuplow	0	RW_SS	Switch on Power_Off mode if low VBAT/VSUP is detected during Active or Standby mode (pin ONKEY=low and bit auto_off=0) 0 : If low VBAT/VSUP is detected, continuously monitor battery voltage and startup if battery voltage is above ResVoltRise 1 : If low VBAT/VSUP is detected, enter Power_Off mode

Figure 135:
ResetTimer

Addr:34h		ResetTimer		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6	stby_reset_enable	0	RW	Enable Reset output signal (pin XRES_OUT) in standby mode 0 : No reset (XRES_OUT=1) in standby mode and during exit of standby mode 1 : Reset is active (XRES_OUT=0) in standby mode
5	auto_off	0	RW_SS	Defines startup behavior at first battery insertion or reset cycle 0 : Startup of chip if VBAT>ResVoltRise 1 : Enter power off mode (waiting for start-up event e.g. ONKEY)
4:3	off_delay	1	RW	Set Delay between I2C command, GPIO or Reset signal for power_off, standby mode or reset and execution of that command 0 : no delay 1 : 8 ms 2 : 16 ms 3 : 32 ms
1:0	res_timer	0	RW_SM	Set Reset Time, after the last regulator has started 0 : RESTIME = 0 ms 1 : RESTIME = 5 ms 2 : RESTIME = 11 ms 3 : RESTIME = 15 ms

Figure 136:
ReferenceControl

Addr:35h		ReferenceControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	force_softreset	0	RW_SM	Setting to 1 starts a soft reset cycle Reset_out is activated and startup sequence is executed without switching of the regulators (voltage preset)
5	clk_div2	0	RW_SM	Divide internal clock oscillator by 2 to reduce quiescent current for low power operation 0 : Normal mode 1 : Internal clock frequency divided by two. All timings are increased by two. Switching frequency of all stepdown converters are divided by two. Reduced transient performance of stepdown converters.
4	standby_mode_on	0	RW_SM	Setting to 1 sets the PMU into standby mode.

Addr:35h		ReferenceControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:1	clk_int	0	RW_SM	Sets the internal CLK frequency fCLK used for Stepdowns, PWM, ... 0 : 4 MHz (default) 1 : 3.8 MHz 2 : 3.6 MHz 3 : 3.4 MHz 4 : 3.2 MHz 5 : 3.0 MHz 6 : 2.8 MHz 7 : 2.6 MHz All frequencies, timings and delays in this datasheet are based on 4MHz clk_int
0	low_power_on	0	RW_SM	Enable low power mode of internal reference. 0 : Standard mode 1 : Low power mode - all specification except noise parameters are still valid. Iq reduced by approx. 45uA

Figure 137:
ResetControl

Addr:36h		ResetControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4:3	reset_debounce	0	RW	Sets debounce time for RESET_IN 0 : 0.1 ms 1 : 4 ms 2 : 8 ms 3 : 16 ms
2	onkey_input	0	R_PUSH	READ : This flag represents the state of the ONkey pad directly WRITE : Setting to 1 resets the 2/4/8 sec. Onkey reset timer
1	power_off	0	RW_SM	Setting to 1 starts a reset cycle, and puts the PMIC into Power_off state
0	force_reset	0	RW	Setting to 1 starts a complete reset cycle

Figure 138:
OvertemperatureControl

Addr:37h		OvertemperatureControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	ov_temp_alarm0	0	RO	Temperature alarm0 reached if bit is set First temperature alarm proposed to be set at 94C, reset at 88C
3	rst_ov_temp_shutdown	0	RW_SMP	If the overtemperature threshold ov_temp_max has been reached, the flag ov_temp_shutdown is set and a reset cycle is started. ov_temp_shutdown should be reset by writing 1 and afterward 0 to rst_ov_temp_shutdown
2	ov_temp_shutdown	0	RO	Flag that the overtemperature threshold 2 (T140) has been reached - this flag is not reset by a overtemperature caused reset and has to be reset by rst_ov_temp_shutdown Shutdown temperature proposed to be set at 140C reset at 135C
1	ov_temp_alarm1	0	RO	Temperature alarm1 reached if bit is set Second temperature alarm proposed to be set at 113C, reset at 107C
0	temp_pmc_on	1	RW	Switch on/off temperature supervision, default: on Leave at 1, do not disable all other OvertemperatureControl bits are only valid if this bit is set

Figure 139:
WatchdogControl

Addr:38h		WatchdogControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2:1	wtdg_mode	0	RW_SM	Defines actions when the watchdog expires 0 : interrupt only 1 : performs a reset cycle, then try restart 2 : power-off 3 : performs up to 2 reset cycles, then power-off bit are set to their OTP values at startup, bit 0 can only be set
0	wtdg_on	0	RW_SS	Switches on the complete watchdog 0 : watchdog off 1 : watchdog on bit is set to its OTP value at startup, bit can only be set

Figure 140:
Reg_standby_mod1

Addr:39h		Reg_standby_mod1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	disable_regpd	0	RW	This bit disables the pull-down of all regulators 0 : normal mode with pull-down for all internal regulators 1 : pull-down disabled; >100kOhm for all internal regulators
6	sd6_stby_on	0	RW	Enable Step down 6 in standby mode
5	sd5_stby_on	0	RW	Enable Step down 5 in standby mode
4	sd4_stby_on	0	RW	Enable Step down 4 in standby mode
3	sd3_stby_on	0	RW	Enable Step down 3 in standby mode
2	sd2_stby_on	0	RW	Enable Step down 2 in standby mode
1	sd1_stby_on	0	RW	Enable Step down 1 in standby mode
0	sd0_stby_on	0	RW	Enable Step down 0 in standby mode

Figure 141:
Reg_standby_mod2

Addr:3ah		Reg_standby_mod2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo7_stby_on	0	RW	Enable LDO7 in standby mode
6	ldo6_stby_on	0	RW	Enable LDO6 in standby mode
5	ldo5_stby_on	0	RW	Enable LDO5 in standby mode
4	ldo4_stby_on	0	RW	Enable LDO4 in standby mode
3	ldo3_stby_on	0	RW	Enable LDO3 in standby mode
2	ldo2_stby_on	0	RW	Enable LDO2 in standby mode
1	ldo1_stby_on	0	RW	Enable LDO1 in standby mode
0	ldo0_stby_on	0	RW	Enable LDO0 in standby mode

Figure 142:
Reg_standby_mod3

Addr:3bh		Reg_standby_mod3		
Bit	Bit Name	Default	Access	Bit Description
3	ldo11_stby_on	0	RW	Enable LDO11 in standby mode
2	ldo10_stby_on	0	RW	Enable LDO10 in standby mode
1	ldo9_stby_on	0	RW	Enable LDO9 in standby mode

Figure 143:
ENABLEctrl1

Addr:3ch		ENABLEctrl1		
Bit	Bit Name	Default	Access	Bit Description
7:6	enable_ctrl_sd3	0	RW	Enable control of SD3. only enabled, if sd3_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
5:4	enable_ctrl_sd2	0	RW	Enable control of SD2. only enabled, if sd2_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
3:2	enable_ctrl_sd1	0	RW	Enable control of SD1. only enabled, if sd1_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
1:0	enable_ctrl_sd0	0	RW	Enable control of SD0. only enabled, if sd0_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3

Figure 144:
ENABLEctrl2

Addr:3dh		ENABLEctrl2		
Bit	Bit Name	Default	Access	Bit Description
5:4	enable_ctrl_sd6	0	RW	Enable control of SD6. only enabled, if sd6_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
3:2	enable_ctrl_sd5	0	RW	Enable control of SD5. only enabled, if sd5_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
1:0	enable_ctrl_sd4	0	RW	Enable control of SD4. only enabled, if sd4_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3

Figure 145:
ENABLEctrl3

Addr:3eh		ENABLEctrl3		
Bit	Bit Name	Default	Access	Bit Description
7:6	enable_ctrl_ldo3	0	RW	Enable control of ldo3. only enabled, if ldo3_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
5:4	enable_ctrl_ldo2	0	RW	Enable control of ldo2. only enabled, if ldo2_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
3:2	enable_ctrl_ldo1	0	RW	Enable control of ldo1. only enabled, if ldo1_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3

Addr:3eh		ENABLEctrl3		
Bit	Bit Name	Default	Access	Bit Description
1:0	enable_ctrl_ldo0	0	RW	Enable control of ldo0. only enabled, if ldo0_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3

Figure 146:
ENABLEctrl4

Addr:3fh		ENABLEctrl4		
Bit	Bit Name	Default	Access	Bit Description
7:6	enable_ctrl_ldo7	0	RW	Enable control of ldo7. only enabled, if ldo7_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
5:4	enable_ctrl_ldo6	0	RW	Enable control of ldo6. only enabled, if ldo6_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
3:2	enable_ctrl_ldo5	0	RW	Enable control of ldo5. only enabled, if ldo5_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
1:0	enable_ctrl_ldo4	0	RW	Enable control of ldo4. only enabled, if ldo4_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3

Figure 147:
ENABLEctrl5

Addr:40h		ENABLEctrl5		
Bit	Bit Name	Default	Access	Bit Description
7:6	enable_ctrl_ldo11	0	RW	Enable control of ldo11. only enabled, if ldo11_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
5:4	enable_ctrl_ldo10	0	RW	Enable control of ldo10. only enabled, if ldo10_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3
3:2	enable_ctrl_ldo9	0	RW	Enable control of ldo9. only enabled, if ldo9_vsel>0 0 : no ENABLE control 1 : controlled by enable1 2 : controlled by enable2 3 : controlled by enable3

Figure 148:
pwm_control_l

Addr:41h		pwm_control_l		
Bit	Bit Name	Default	Access	Bit Description
7:0	pwm_l_time	0	RW	This bit defines the low time of the pwm generator in 1MHz units 0 : pwm_div * 1us 1 : pwm_div * 2us 2 : pwm_div * 3us .. : .. 254 : pwm_div * 255us 255 : pwm_div * 256us

Figure 149:
pwm_control_h

Addr:42h		pwm_control_h		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	pwm_h_time	0	RW	This bit defines the high time of the pwm generator in 1MHz units 0 : pwm_div * 1us 1 : pwm_div * 2us 2 : pwm_div * 3us .. : .. 254 : pwm_div * 255us 255 : pwm_div * 256us

Figure 150:
Watchdog_timer

Addr:46h		Watchdog_timer		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6:0	wtdg_timer	0	RW	Watchdog timer Write watchdog timer, Read actual countdown starting from (LSB=1s, range: 1 - 128s) writing of wtdg_sw_sig or risigng edge of GPIO (if GPIOx_iosf=9) resets the watchdog to wtdg_timer 0 : 1 second 1 : 2 seconds 2 : 3 seconds 3 : 4 seconds .. : .. 126 : 127 seconds 127 : 128 seconds

Figure 151:
WatchdogSoftwareSignal

Addr:48h		WatchdogSoftwareSignal		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	pwm_div	0	RW	This bit defines the divider ratio of the prescaler for the PWM generator 0 : Divide by 1 1 : Divide by 16 2 : Divide by 256 3 : Divide by 16384
0	wtdg_sw_sig	0	PUSH	Trigger input by the serial interface, if gpioX_iosf<>9

Figure 152:
IOVoltage

Addr:49h		IOVoltage		
Bit	Bit Name	Default	Access	Bit Description
0	level33	0	RW	Voltage level of input signals 0 : IO voltage 1.8 V 1 : IO voltage 3.3 V
4	I2C_bus_pullup	0	RW_SS	I2C data and CLK internal pull-ups enabled/disabled 0 : pull-ups disabled 1 : pull-ups enabled
5	INT_pullup_dis	0	RW	Interrupt signal pull-up enabled/disabled on pin XINT 0 : pull-up enabled (open drain mode) 1 : pull-up disabled (push/pull mode)f

Figure 153:
Battery_voltage_monitor2

Addr:4ah		Battery_voltage_monitor2		
Bit	Bit Name	Default	Access	Bit Description
1:0	ncells	0	RW_SM	Selects number of cells that are connected to VBAT pin 0 : 1 cell: ResVoltRise = 2.5...3.6 1 : 2 cell: ResVoltRise = 2*(2.5...3.6V) = 5.0....7.2V 2 : 3 cell: ResVoltRise = 3*(2.5...3.6V) = 7.5...10.8V 3 : 4 cell: ResVoltRise = 4*(2.5...3.6V) = 10....14.4V
4:2	vsup_min	0	RW_SM	Defines minimum value on VSUP for startup/reset 0 : 2.55V 1 : 2.7V 2 : 3.0V 3 : 3.2V 4 : 4.5V 5 : 4.7V 6 : 4.8V

Figure 154:
SDcontrol

Addr:4dh		SDcontrol		
Bit	Bit Name	Default	Access	Bit Description
6	sd6_enable	1	RW	Global stepdown6 enable
5	sd5_enable	1	RW	Global stepdown5 enable
4	sd4_enable	1	RW	Global stepdown4 enable
3	sd3_enable	1	RW	Global stepdown3 enable
2	sd2_enable	1	RW	global stepdown2 enable
1	sd1_enable	1	RW	Global stepdown1 enable
0	sd0_enable	1	RW	Global stepdown0 enable

Figure 155:
LDOcontrol0

Addr:4eh		LDOcontrol0		
Bit	Bit Name	Default	Access	Bit Description
7	ldo7_enable	1	RW	Global ldo7 enable
6	ldo6_enable	1	RW	Global ldo6 enable
5	ldo5_enable	1	RW	Global ldo5 enable
4	ldo4_enable	1	RW	Global ldo4 enable
3	ldo3_enable	1	RW	Global ldo3 enable
2	ldo2_enable	1	RW	Global ldo2 enable
1	ldo1_enable	1	RW	Global ldo1 enable
0	ldo0_enable	1	RW	Global ldo0 enable

Figure 156:
LDOcontrol1

Addr:4fh		LDOcontrol1		
Bit	Bit Name	Default	Access	Bit Description
3	ldo11_enable	1	RW	Global ldo11 enable
2	ldo10_enable	1	RW	Global ldo10 enable
1	ldo9_enable	1	RW	Global ldo9 enable

Figure 157:
SD0_protect

Addr:50h		SD0_protect		
Bit	Bit Name	Default	Access	Bit Description
4:0	sd0_vmax	0	RW_SM	Overvoltage protection function for SD0 Will be programmed into OTP and cannot be changed by SW. 0 : protection disabled other : max voltage set by OTP

Figure 158:
SD6_protect

Addr:51h		SD6_protect		
Bit	Bit Name	Default	Access	Bit Description
4:0	sd6_vmax	0	RW_SM	Overvoltage protection function for SD6 Will be programmed into OTP and cannot be changed by SW. 0 : protection disabled other : max voltage set by OTP

Figure 159:
PWM_vcontrol1

Addr:52h		PWM_vcontrol1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	vpwm1_step	0	RW	Select step size of PWM1 mode 0 : 10mV 1 : 20mV
6	vpwm1_on	0	RW_SM	Enable PWM1 control of SD0 0 : PWM1 control disabled 1 : PWM1 control enabled (if vpwm1_value is reset, then PWM control is enabled after first PWM1 interface word only)
5:0	vpwm1_vbase	0	RW	Base voltage register of SD0 from 0.6V to 1.1V in 10m steps 0 : 0.6 V 1 : 0.61 V 2 : 0.62 V .. : .. 49 : 1.09 V 50 : 1.10 V

Figure 160:
PWM_vcontrol2

Addr:53h		PWM_vcontrol2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	vpwm2_step	0	RW	Select step size of PWM2 mode 0 : 10mV 1 : 20mV
6	vpwm2_on	0	RW_SM	Enable PWM2 control of SD6 0 : PWM2 control disabled 1 : PWM2 control enabled (if vpwm2_value is reset, then PWM control is enabled after first PWM2 interface word only)
5:0	vpwm2_vbase	0	RW	Base voltage register of SD6 from 0.6V to 1.1V in 10m steps 0 : 0.6 V 1 : 0.61 V 2 : 0.62 V .. : .. 49 : 1.09 V 50 : 1.10 V

Figure 161:
PWM_vcontrol3

Addr:54h		PWM_vcontrol3		
Bit	Bit Name	Default	Access	Bit Description
7:6	vpwm1_reset	0	RW	Select reset behavior if SD0 gets disabled 0 : vpwm1_on and vpwm1_value reset 1 : vpwm1_on reset, vpwm1_value not reset 2 : vpwm1_on and vpwm1_value not reset 3 : do not use
5:0	vpwm1_value	0	R	Actual PWM1 value SD0 voltage = vpwm1_vbase + vpwm1_step * vpwm1_value

Figure 162:
PWM_vcontrol4

Addr:55h		PWM_vcontrol4		
Bit	Bit Name	Default	Access	Bit Description
7:6	vpwm2_reset	0	RW	Select reset behavior if SD6 gets disabled 0 : vpwm2_on and vpwm2_value reset 1 : vpwm2_on reset, vpwm2_value not reset 2 : vpwm2_on and vpwm1_value not reset 3 : do not use
5:0	vpwm2_value	0	R	Actual PWM2 value SD6 voltage = vpwm2_vbase + vpwm2_step * vpwm2_value

Figure 163:
BBcharger

Addr:57h		BBcharger		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	BBCActive	0	RO	Status of backup battery charger 0 : Charger is not active 1 : Charger charges backup battery
6	BBCPwrSave	1	RW	0 : Normal operation of the backup battery charger 1 : The backup battery charger checks if it is actually charging the battery (bit BBCActive=1) and it is disabled if it is not. Every 10s (every 64s in state Off) the voltage of the backup battery is checked again to determine if charging is required. This practically reduces the current consumption to 0 if the backup battery is full.
5	BBCVolt	0	RW	This value determines the maximum charging voltage VBBC 0 : VBBC=2.5V 1 : VBBC=3.0V
4:3	BBCCur	0	RW	This value determines the charge current IBBC 0 : IBBC=50uA 1 : IBBC=100uA 2 : IBBC=200uA 3 : IBBC=400uA
2	BBCResOff	0	RW	0 : Enable output resistor 1 : Bypass output resistor
1:0	BBCMode	0	RW	Enable and disable backup battery charger. Activation in PowerOff and standby mode requires 32kHz OSC to be enabled (rtc_on=1). 0 : Backup battery charger is disabled 1 : Backup battery charger is enabled in state Active mode 2 : Backup battery charger is enabled in states Active mode and Standby mode 3 : Backup battery charger is enabled in states PowerOff mode, Active mode and Standby mode

Figure 164:
CTRLsequ1

Addr:58h		CTRLsequ1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	ac_ok_pwr_on	0	RW_SS	Enables exit out of PWR OFF mode with pin AC_OK (pin enabled in PWR off mode) 0 : AC_OK disabled 1 : AC_OK enabled
1	lid_pwr_on	0	RW_SS	Enables exit out of PWR OFF mode with pin LID (pin enabled in PWR off mode) 0 : LID disabled 1 : LID enabled
2	therm_inv	0	RW_SS	Sets the polarity of the THERM pin 0 : High active for THERM event 1 : Inverted: Low active for THERM event
3	enable2_inv	0	RW_SS	Sets the polarity of the ENABLE2 pin 0 : High active for ENALBE2 1 : Inverted: Low active for ENABLE2
4	enable1_inv	0	RW	Sets the polarity of the ENABLE1 pin 0 : High active for ENABLE1 1 : Inverted: Low active for ENABLE1
5	enable1_deepsleep	0	RW	ENABLE1 signal enable for controlling deepsleep/stand_by 0 : ENABLE1 signal not used for stand_by entry/exit 1 : ENABLE1 signal used for stand_by entry/exit
6	onkey_nodebounce	0	RW	Sets the debounce on ONKEY 0 : debounce on 1 : debounce off
7	enable3_inv	0	RW_SS	Sets the polarity of the ENABLE3 pin 0 : High active for ENABLE3 1 : Inverted: Low active for ENABLE3

Figure 165:
CTRLsequ2

Addr:59h		CTRLsequ2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1:0	on_shutdown_delay	0	RW_SM	Sets the ONKEY shutdown delay time. After timer expired onkey_lpress_i interrupt status bit is set and one additional second wait is added before shutdown is initiated. If interrupt status register is read out during that second, the delay timer is reset, and no shutdown is done. 0 : disabled 1 : 2 sec 2 : 4 sec 3 : 8 sec
2	onkey_invert	0	RW_SS	Sets the polarity of the ONKEY pin 0 : High active for ONKEY 1 : Inverted: Low active for ONKEY
5:3	on_shutdown_delay_cnt	0	R	On-reset delay counter in seconds. Starts with 0sec when onkey is pressed.
6	ac_ok_invert	0	RW_SS	Sets the polarity of the AC_OK pin 0 : High active for AC_OK 1 : Inverted: Low active for AC_OK
7	lid_invert	0	RW_SS	Sets the polarity of the LID pin 0 : High active for LID 1 : Inverted: Low active for LID

Figure 166:
OVcurrent

Addr:5ah		OVcurrent		
Bit	Bit Name	Default	Access	Bit Description
2:0	sd0_ovc_alarm	0	RW	Selects overcurrent alarm threshold of SD0 per phase 0 : disabled 1 : 1.6A 2 : 1.8A 3 : 2.0A 4 : 2.2A 5 : 2.4A 6 : 2.6A 7 : 2.8A
4:3	sd0_ilimit	0	RW	Selects overcurrent trip threshold of SD0 per phase 0 : 2.5A 1 : 3A 2 : 3.5A 3 : do not use
6:5	sd1_ilimit	0	RW	Selects overcurrent trip threshold of SD1 per phase 0 : 2.5A 1 : 3A 2 : 3.5A 3 : do not use

Figure 167:
OVcurrent_deb

Addr:5bh		OVcurrent_deb		
Bit	Bit Name	Default	Access	Bit Description
1:0	sd06_ovc_alarm_deb	0	RW	Selects debounce time of ovc_alarm0 and ovc_alarm6 signals 0 : no debouncing 1 : 1 us 2 : 4 us 3 : 20 us
4:3	sd6_ilimit	0	RW	Selects overcurrent trip threshold of SD6 per phase 0 : 2.5A 1 : 3A 2 : 3.5A 3 : do not use

Figure 168:
SDlv_deb

Addr:5ch		SDlv_deb		
Bit	Bit Name	Default	Access	Bit Description
7:6	pg_sd6_vmask_time	0	RW	Mask pwrgood_sd6 (=sd6_lv) and ovcurr after voltage change (DVS) 0 : no masking 1 : 4us 2 : 8us 3 : do not use
5:4	sd6_lv_deb	0	RW	Selects debounce time of sd6_lv signal 0 : no debouncing 1 : 1 us 2 : 4 us 3 : 20 us
3:2	sd1_lv_deb	0	RW	Selects debounce time of sd1_lv signal 0 : no debouncing 1 : 1 us 2 : 4 us 3 : 20 us
1:0	sd0_lv_deb	0	RW	Selects debounce time of sd0_lv signal 0 : no debouncing 1 : 1 us 2 : 4 us 3 : 20 us

Figure 169:
OC_pg_ctrl

Addr:5dh		OC_pg_ctrl		
Bit	Bit Name	Default	Access	Bit Description
0	pg_ac_ok_inv	0	RW	Invert AC_OK for OC_PG signal
1	pg_ac_ok_mask	0	RW	Mask AC_OK for OC_PG signal
2	pg_gpio3_mask	0	RW	Mask gpio3 for OC_PG signal
3	pg_gpio4_mask	0	RW	Mask gpio4 for OC_PG signal
4	pg_gpio5_mask	0	RW	Mask gpio5 for OC_PG signal
5	pg_pwrgood_sd0_mask	0	RW	Mask pwrgood for OC_PG signal power good is the sd0_lv signal
6	pg_ovcurr_sd0_mask	0	RW	Mask ovc_alarm threshold of SD0
7	pg_vresfall_mask	0	RW	Mask ResVoltFall (alarm threshold)

Figure 170:
OC_pg_ctrl2

Addr:5eh		OC_pg_ctrl2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	-	0	RW	N/A, has to be set to "0"
2:1	pg_vmask_time	0	RW	Mask pwrgood_sd0 (=sd0_lv) and ovcurr after voltage change (DVS) 0 : no masking 1 : 4us 2 : 8us 3 : do not use
5:3	pg_sd6_ovc_alarm	0	RW	Selects overcurrent alarm threshold of dcdc6 per phase 0 : disabled 1 : 1.6A 2 : 1.8A 3 : 2.0A 4 : 2.2A 5 : 2.4A 6 : 2.6A 7 : 2.8A
6	pg_pwrgood_sd6_mask	0	RW	Mask power good for dcdc6 (dcdc6_lv) signal on selected GPIO output
7	pg_ovcurr_sd6_mask	0	RW	Mask overcurrent alarm threshold of dcdc6 on selected GPIO output if bits 7 and 6 are 0, pg_sd6 (if selected as GPIO out function) represents power good and overcurrent function of sd6

Figure 171:
CTRLstatus

Addr:5fh		CTRLstatus		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	ac_ok	0	RO	Status of AC_OK pin
1	lid	0	RO	Status of LID pin
2	therm	0	RO	Status of THERM pin
3	ov_curr	0	RO	Over current of SD0 reached
4	enable1	0	RO	Status of enable1 signal (enable1 XOR enable1_inv)

Addr:5fh		CTRLstatus		
Bit	Bit Name	Default	Access	Bit Description
5	enable2	0	RO	Status of enable2 signal (enable2 XOR enable2_inv)
6	enable3	0	RO	Status of enable3 signal (enable3 XOR enable3_inv)
7	sd0_pwr_ok	0	RO	Status of sd0_pwrgood

Figure 172:
RTCcontrol

Addr:60h		RTCcontrol		
Bit	Bit Name	Default	Access	Bit Description
7	am_pm_mode	0	RW	12h/24h mode switch 0 : 24hour mode 1 : 12hour am/pm mode
5	clk32out_en	1	RW	0 : CLK32OUT pin disabled 1 : CLK32OUT pin enabled (push/pull to VDD_GPIO_lv)
4:3	rtc_irq_mode	0	RW	0 : generates an interrupt every second 1 : generates an interrupt every minute 2 : generates an interrupt every 2 minutes 3 : generates an interrupt every 8 minutes
2	rtc_on	0	RW_SM	Switch on the 32kHz RTC oscillator 0 : 32kHz oscillator disabled 1 : 32kHz oscillator enabled
1	rtc_alarm_wakeup_en	0	RW	0 : Disables RTC alarm wakeup in power off mode 1 : Enable RTC alarm wakeup in power off mode
0	rtc_rep_wakeup_en	0	RW	0 : Disables RTC repeated wakeup in power off mode 1 : Enable RTC repeated wakeup in power off mode

Figure 173:
RTCsecond

Addr:61h		RTCsecond		
Bit	Bit Name	Default	Access	Bit Description
3:0	second0	0	RW_SM	Seconds digit (BCD coded) RTCyear has to be written to latch the whole RTC register
6:4	second1	0	RW_SM	10-seconds digit (BCD coded), RTCsecond counts seconds, minutes roll over after 59 seconds to 00 RTCyear has to be written to latch the whole RTC register

Figure 174:
RTCminute

Addr:62h		RTCminute		
Bit	Bit Name	Default	Access	Bit Description
3:0	minute0	0	=	Minutes digit (BCD coded) RTCyear has to be written to latch the whole RTC register
6:4	minute1	0	=	10-minutes digit (BCD coded), RTCminute counts minutes, hour roll over after 59 minutes to 00 RTCyear has to be written to latch the whole RTC register

Figure 175:
RTChour

Addr:63h		RTChour		
Bit	Bit Name	Default	Access	Bit Description
3:0	hour0	0	=	Hours digit (BCD coded) RTCyear has to be written to latch the whole RTC register
5:4	hour1	0	=	10-hours digit (BCD coded), RTChour counts hours, day roll over after 12 hours to 01 (when am_pm_mode is 1), after 23 hours to 00 (when am_pm_mode is 0) RTCyear has to be written to latch the whole RTC register

Addr:63h		RTChour		
Bit	Bit Name	Default	Access	Bit Description
7	pm	0	RW	AM/PM flag (only valid when am_pm_mode is 1, otherwise read returns 0) 0 : AM 1 : PM RTCyear has to be written to latch the whole RTC register

Figure 176:
RTCday

Addr:64h		RTCday		
Bit	Bit Name	Default	Access	Bit Description
3:0	day0	1	RW_SM	Days digit (BCD coded) RTCyear has to be written to latch the whole RTC register
5:4	day1	0	=	10-days digit (BCD coded), RTCday counts days, month roll over after 31/30/29/28 days to 01 RTCyear has to be written to latch the whole RTC register

Figure 177:
RTCmonth

Addr:65h		RTCmonth		
Bit	Bit Name	Default	Access	Bit Description
3:0	month0	1	=	Months digit (BCD coded) RTCyear has to be written to latch the whole RTC register
4	month1	0	=	10-months digit (BCD coded), RTCmonth counts month, year roll over after 12 months to 01 RTCyear has to be written to latch the whole RTC register

Figure 178:
RTCyear

Addr:66h		RTCyear		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	year0	0	=	Years digit (BCD coded)
6:4	year1	0	=	10-years digit (BCD coded), RTCyear counts years

Figure 179:
RTCAlarmSecond

Addr:67h		RTCAlarmSecond		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	Alarmsecond0	0	RW	Seconds digit (BCD coded) RTCAlarmyear has to be written to latch the whole alarm register
6:4	Alarmsecond1	0	=	10-seconds digit (BCD coded) RTCAlarmyear has to be written to latch the whole alarm register

Figure 180:
RTCAlarmMinute

Addr:68h		RTCAlarmMinute		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	Alarmminute0	0	=	Minutes digit (BCD coded) RTCAlarmyear has to be written to latch the whole alarm register
6:4	Alarmminute1	0	=	10-minutes digit (BCD coded) RTCAlarmyear has to be written to latch the whole alarm register

Figure 181:
RTCAlarmHour

Addr:69h		RTCAlarmHour		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	Alarmhour0	0	=	Hours digit (BCD coded) RTCAlarmyear has to be written to latch the whole alarm register
5:4	Alarmhour1	0	=	10-hours digit (BCD coded) RTCAlarmyear has to be written to latch the whole alarm register
7	Alarmpm	0	=	AM/PM flag (only valid when am_pm_mode is 1, otherwise read returns 0) 0 : AM 1 : PM RTCAlarmyear has to be written to latch the whole alarm register

Figure 182:
RTCAlarmday

Addr:6ah		RTCAlarmday		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	Alarmday0	Fh	=	Days digit (BCD coded) RTCAlarmyear has to be written to latch the whole alarm register
5:4	Alarmday1	3h	=	10-days digit (BCD coded) RTCAlarmyear has to be written to latch the whole alarm register

Figure 183:
RTCAlarmmonth

Addr:6bh		RTCAlarmmonth		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	Alarmmonth0	Fh	=	Months digit (BCD coded) RTCAlarmyear has to be written to latch the whole alarm register
4	Alarmmonth1	1h	=	10-months digit (BCD coded) RTCAlarmyear has to be written to latch the whole alarm register

Figure 184:
RTCAlarmyear

Addr:6ch		RTCAlarmyear		
Bit	Bit Name	Default	Access	Bit Description
3:0	Alarmyear0	Fh	=	Years digit (BCD coded)
6:4	Alarmyear1	7h	=	10-years digit (BCD coded)

Figure 185:
SRAM

Addr:6dh		SRAM		
Bit	Bit Name	Default	Access	Bit Description
7:0	SRAM	0	RW	Bits are free to store any information

Figure 186:
RTC_Access

Addr:6fh		RTC_Access		
Bit	Bit Name	Default	Access	Bit Description
7	rtc_write_ena	0	RW_SS	

Figure 187:
RegStatus

Addr:73h		RegStatus		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6	sd6_lv	0	RO	Bit is set when voltage of step down6 drops below low voltage threshold (-5%) (1ms debounce time default)
5	sd5_lv	0	RO	Bit is set when voltage of step down5 drops below low voltage threshold (-5%) (1ms debounce time default)
4	sd4_lv	0	RO	Bit is set when voltage of step down4 drops below low voltage threshold (-5%) (1ms debounce time default)
3	sd3_lv	0	RO	Bit is set when voltage of step down3 drops below low voltage threshold (-5%) (1ms debounce time default)
2	sd2_lv	0	RO	Bit is set when voltage of step down2 drops below low voltage threshold (-5%) (1ms debounce time default)
1	sd1_lv	0	RO	Bit is set when voltage of step down1 drops below low voltage threshold (-5%) (1ms debounce time default)
0	sd0_lv	0	RO	Bit is set when voltage of step down0 drops below low voltage threshold (-5%) (1ms debounce time default)

Figure 188:
InterruptMask1

Addr:74h		InterruptMask1		
Bit	Bit Name	Default	Access	Bit Description
7	LowBat_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
6	ovtmp_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
5	onkey_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
4	onkey_lpress_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
3	occur_alarm_sd0_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
2	enable1_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
1	acok_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
0	lid_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)

Figure 189:
InterruptMask2

Addr:75h		InterruptMask2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	rtc_rep_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
6	sd6_lv_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
5	enable2_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
4	PWM2_ovprot_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
3	PWM1_ovprot_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
2	sd2345_lv_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
1	sd1_lv_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
0	sd0_lv_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)

Figure 190:
InterruptMask3

Addr:76h		InterruptMask3		
Bit	Bit Name	Default	Access	Bit Description
7	enable3_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
6	wtdg_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
5	gpio5_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
4	gpio4_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
3	gpio3_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
2	gpio2_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
1	gpio1_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
0	rtc_alarm_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)

Figure 191:
InterruptMask4

Addr:77h		InterruptMask4		
Bit	Bit Name	Default	Access	Bit Description
0	temp_sd0_shutdown_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
1	temp_sd1_shutdown_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
2	temp_sd6_shutdown_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
3	temp_sd0_alarm_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
4	temp_sd1_alarm_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
5	temp_sd6_alarm_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)

Addr:77h		InterruptMask4		
Bit	Bit Name	Default	Access	Bit Description
6	occur_alarm_sd6_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
7	adc_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)

Figure 192:
InterruptStatus1

Addr:78h		InterruptStatus1		
Bit	Bit Name	Default	Access	Bit Description
7	LowBat_int_i	0	SS_RC	Bit is set when VSUP drops below vres_fall
6	ovtmp_int_i	0	SS_RC	Bit is set when 110deg is exceeded on main or subdies
5	onkey_int_i	0	SS_RC	Rising and falling edge
4	onkey_lpress_int_i	0	SS_RC	Bit is set at ONkey longpress interrupt (rising edge) Reading out that register resets the ONkey longreset timer
3	occur_alarm_sd0_int_i	0	SS_RC	Rising edge only
2	enable1_int_i	0	SS_RC	Rising and falling edge
1	acok_int_i	0	SS_RC	Rising and falling edge
0	lid_int_i	0	SS_RC	Rising and falling edge

Figure 193:
InterruptStatus2

Addr:79h		InterruptStatus2		
Bit	Bit Name	Default	Access	Bit Description
7	rtc_rep_int_i	0	SS_RC	Rising edge only
6	sd6_lv_int_i	0	SS_RC	Rising edge only
5	enable2_int_i	0	SS_RC	Rising and falling edge
4	PWM2_ovprot_int_i	0	SS_RC	Rising edge only overvoltage protection reached with VPWM2 control
3	PWM1_ovprot_int_i	0	SS_RC	Rising edge only overvoltage protection reached with VPWM1 control
2	sd2345_lv_int_i	0	SS_RC	Rising edge only low voltage of sd2,3,4 or 5
1	sd1_lv_int_i	0	SS_RC	Rising edge only
0	sd0_lv_int_i	0	SS_RC	Rising edge only

Figure 194:
InterruptStatus3

Addr:7ah		InterruptStatus3		
Bit	Bit Name	Default	Access	Bit Description
7	enable3_int_i	0	SS_RC	Rising and falling edge
6	wtdg_int_i	0	SS_RC	Watchdog expired
5	gpio5_int_i	0	SS_RC	Rising and falling edge
4	gpio4_int_i	0	SS_RC	Rising and falling edge
3	gpio3_int_i	0	SS_RC	Rising and falling edge
2	gpio2_int_i	0	SS_RC	Rising and falling edge
1	gpio1_int_i	0	SS_RC	Rising and falling edge
0	rtc_alarm_int_i	0	SS_RC	Rising edge only

Figure 195:
InterruptStatus4

Addr:7bh		InterruptStatus4		
Bit	Bit Name	Default	Access	Bit Description
7	adc_int_i	0	SS_RC	Rising and falling edge
6	occur_alarm_sd6_int_i	0	SS_RC	Rising edge only
5	temp_sd6_alarm_int_i	0	SS_RC	Rising and falling edge
4	temp_sd1_alarm_int_i	0	SS_RC	Rising and falling edge
3	temp_sd0_alarm_int_i	0	SS_RC	Rising and falling edge
2	temp_sd6_shutdown_int_i	0	SS_RC	Rising and falling edge
1	temp_sd1_shutdown_int_i	0	SS_RC	Rising and falling edge
0	temp_sd0_shutdown_int_i	0	SS_RC	Rising and falling edge

Figure 196:
Temp_Status

Addr:7dh		Temp_Status		
Bit	Bit Name	Default	Access	Bit Description
0	temp_sd0_shutdown	0	POP	Indicates over temperature >140deg in subdie and ovtmp reset initated if mask_ovtemp=0 Bit is reset by readout only
1	temp_sd1_shutdown	0	POP	Indicates over temperature >140deg in subdie and ovtmp reset initated if mask_ovtemp=0 Bit is reset by readout only
2	temp_sd6_shutdown	0	POP	Indicates over temperature >140deg in subdie of sd6 and ovtmp reset initated if mask_ovtemp=0 Bit is reset by readout only
3	mask_ovtemp	0	RW	Inhibit reset caused by over temperature of SD0, SD1, or SD6 0 : Over temperature of SD0, SD1, or SD6 causes reset 1 : Over temperature of SD0, SD1, or SD6 causes interrupt only
4	temp_sd0_alarm	0	R	Indicates over temperature >110deg in subdie
5	temp_sd1_alarm	0	R	Indicates over temperature >110deg in subdie
6	temp_sd6_alarm	0	R	Indicates over temperature >110deg in subdie

Figure 197:
ADC0_control

Addr:80h		ADC0_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	adc0_start_conversion	0	RW_SC	Writing a 1 into this bit starts one ADC conversion. Self cleared at begin of ADC conversion
5	adc0_gpio_lv	0	RW	0 : High voltage range of GPIO1,2,6,7, PWM_CLK2, PWM_DAT2 (4:1 divider active) 1 : Low voltage range of GPIO1,2,4,7, PWM_CLK2, PWM_DAT2 (1:1 divider, 1.6V max)
4:0	adc0_select	0	RW	Selects an ADC channel 0 : Output Current SD0 1 : Output Current SD1 2 : Output Current SD6 3 : Temperature sensor:DIE temperature [C] = adc_result * 0.7698 - 274 (1:1) 4 : VSUP (4:1) 5 : GPIO1 (4:1 or 1:1) 6 : GPIO2 (4:1 or 1:1) 7 : GPIO3 (4:1 or 1:1) 8 : GPIO4 (4:1 or 1:1) 9 : GPIO6 (4:1 or 1:1) 10 : GPIO7 (4:1 or 1:1) 11 : VBAT (15:1) value valid below 15V only 12 : PWM_CLK2/ADC1 (4:1 or 1:1) 13 : PWM_DAT2/ADC2 (4:1 or 1:1) 14 : do not use 15 : do not use 16 : TEMP1_SD0: Tj = 326.5 – adc0_D[9:0] * 0.3734 (1:1) 17 : TEMP2_SD0: Tj = 326.5 - adc0_D[9:0] * 0.3734 (1:1) 18 : TEMP3_SD0: Tj = 326.5 - adc0_D[9:0] * 0.3734 (1:1) 19 : TEMP4_SD0: Tj = 326.5 - adc0_D[9:0] * 0.3734 (1:1) 20 : TEMP_SD1: Tj = 326.5 - adc0_D[9:0] * 0.3734 (1:1) 21 : TEMP1_SD6: Tj = 326.5 - adc0_D[9:0] * 0.3734 (1:1) 22 : TEMP2_SD6: Tj = 326.5 - adc0_D[9:0] * 0.3734 (1:1)

Figure 198:
ADC1_control

Addr:81h		ADC1_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	adc1_start_conversion	0	RW_SM	Writing a 1 into this bit starts one ADC conversion. Self cleared at begin of ADC conversion
6	adc1_interval_scan	0	RW	ADC conversion mode 0 : no interval conversion, single shot 1 : interval conversion, convert every 500/1000ms
5	adc1_gpio_lv	0	RW	0 : High voltage range of GPIO1,2,6,7, PWM_CLK2, PWM_DAT2 (4:1 divider active) 1 : Low voltage range of GPIO1,2,4,7, PWM_CLK2, PWM_DAT2 (1:1 divider, 1.6V max)
4:0	adc1_select	0	RW	Selects an ADC channel 0 : Output Current SD0 1 : Output Current SD1 2 : Output Current SD6 3 : Temperature sensor:DIE temperature [C] = adc_result * 0.7698 - 274 (1:1) 4 : VSUP (4:1) 5 : GPIO1 (4:1 or 1:1) 6 : GPIO2 (4:1 or 1:1) 7 : GPIO3 (4:1 or 1:1) 8 : GPIO4 (4:1 or 1:1) 9 : GPIO6 (4:1 or 1:1) 10 : GPIO7 (4:1 or 1:1) 11 : VBAT (15:1) value valid below 15V only 12 : PWM_CLK2/ADC1 (4:1 or 1:1) 13 : PWM_DAT2/ADC1 (4:1 or 1:1) 14 : do not use 15 : do not use 16 : TEMP1_SD0: Tj = 326.5 – adc1_D[9:0] * 0.3734 (1:1) 17 : TEMP2_SD0: Tj = 326.5 - adc1_D[9:0] * 0.3734 (1:1) 18 : TEMP3_SD0: Tj = 326.5 - adc1_D[9:0] * 0.3734 (1:1) 19 : TEMP4_SD0: Tj = 326.5 - adc1_D[9:0] * 0.3734 (1:1) 20 : TEMP_SD1: Tj = 326.5 - adc1_D[9:0] * 0.3734 (1:1) 21 : TEMP1_SD6: Tj = 326.5 - adc1_D[9:0] * 0.3734 (1:1) 22 : TEMP2_SD6: Tj = 326.5 - adc1_D[9:0] * 0.3734 (1:1)

Figure 199:
ADC0_MSB_result

Addr:82h		ADC0_MSB_result		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	adc0_result_not_ready	0	RO	Indicates end of conversion 0 : result is ready 1 : conversion is running
6:0	adc0_D[9:3]	0	RO	ADC result register Bit9..Bit3

Figure 200:
ADC0_LSB_result

Addr:83h		ADC0_LSB_result		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2:0	adc0_D[2:0]	0	RO	ADC result register Bit2..Bit0

Figure 201:
ADC1_MSB_result

Addr:84h		ADC1_MSB_result		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	adc1_result_not_ready	0	RO	Indicates end of conversion 0 : result is ready 1 : conversion is running
6:0	adc1_D[9:3]	0	RO	ADC result register Bit9..Bit3

Figure 202:
ADC1_LSB_result

Addr:85h		ADC1_LSB_result		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2:0	adc1_D[2:0]	0	RO	ADC result register Bit2..Bit0

Figure 203:
ADC1_threshold_hi_MSB

Addr:86h		ADC1_threshold_hi_MSB		
Bit	Bit Name	Default	Access	Bit Description
6:0	adc1_threshold_hi[9:3]	7'hff	RW	Upper threshold MSB bits

Figure 204:
ADC1_threshold_hi_LSB

Addr:87h		ADC1_threshold_hi_LSB		
Bit	Bit Name	Default	Access	Bit Description
2:0	adc1_threshold_hi[2:0]	3'hf	RW	Upper threshold LSB bits

Figure 205:
ADC1_threshold_lo_MSB

Addr:88h		ADC1_threshold_lo_MSB		
Bit	Bit Name	Default	Access	Bit Description
6:0	adc1_threshold_lo[9:3]	7'h00	RW	Lower threshold MSB bits

Figure 206:
ADC1_threshold_lo_LSB

Addr:89h		ADC1_threshold_lo_LSB		
Bit	Bit Name	Default	Access	Bit Description
2:0	adc1_threshold_lo[2:0]	3'h0	RW	Lower threshold LSB bits

Figure 207:
ADC_configuration

Addr:8ah		ADC_configuration		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	adc1_interval_time	0	RW	Interval time of ADC1 conversions 0 : ~500ms 1 : ~1000ms
1	adc1_interrupt_mode	0	RW	Interrupt generation when ADC1 conversion is ready (when adc1_interval_scan is set) 0 : when ADC1 data rises above adc1_threshold_hi or falls below adc1_threshold_lo 1 : always Interrupts are only generated when the thresholds are crossed
2	adc_buf_on	0	RW	Controls ADC0/1 presample time 0 : 32us 1 : 62us (also enables buffered 1.6V reference voltage on GPIO 7 within conversion time)

Figure 208:
ASIC_ID1

Addr:90h		ASIC_ID1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ID1	0Ch	R	

Figure 209:
ASIC_ID2

Addr:91h		ASIC_ID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	revision	1	RO	

Figure 210:
Fuse7

Addr:a7h		Fuse7		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd5_slave	0	RW	Enables slave mode of SD4 0 : Normal mode of SD5 1 : SD5 is slave of SD4
6	sd4_slave	0	RW	Enables slave mode of SD4 0 : Normal mode of SD4 1 : SD4 is slave of SD2
5	sd3_slave	0	RW	Enables slave mode of SD3 0 : Normal mode of SD3 1 : SD3 is slave of SD2.
4	sd0_v_minus_200mV	0	RW	Enables low voltage mode of SD0 0 : Normal mode of SD0 Code starts with 0.61V 1 : Low voltage mode code starts with 0.41V (-0.2V Offset)
3	trim_gpio_pulld	0	RW	Enables pulldown mode of GPIO1 and GPIO2 0 : Normal mode 1 : Pull down of GPIO1 and GPIO2 enabled
2:1	ldo10_tr	0	RW	
0	ldo9_tr_1	0	RW	

Figure 211:
Fuse8

Addr:a8h		Fuse8		
Bit	Bit Name	Default	Access	Bit Description
6	sd2_hcurr_tr	0	RW	Selects high current mode of SD2
5:4	ldo3_vtrack_tr	0	RW	Selects offset for tracking mode 0 : no offset 1 : +10mV offset of LDO3 at 1.2V Vout (+0.83%) 2 : +20mV offset of LDO3 at 1.2V Vout (+1.66%) 3 : +30mV offset of LDO3 at 1.2V Vout (+2.5%)
3	sd5_fast	0	RW	Selects a faster regulation mode for SD5 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required
2	sd4_fast	0	RW	Selects a faster regulation mode for SD4 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required
1	sd3_fast	0	RW	Selects a faster regulation mode for SD3 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required
0	sd2_fast	0	RW	Selects a faster regulation mode for SD2 suitable for larger load changes. 0 : normal mode, Cout (according spec) 1 : fast mode, 2 x Cout (according spec) required

Figure 212:
Fuse9

Addr:a9h		Fuse9		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	auto_off	0	RW	Defines startup behavior at first battery insertion or reset cycle 0 : Startup of chip if VBAT>ResVoltRise 1 : Enter power off mode (waiting for start-up event e.g. ONKEY)
6	em_shutdown_direct	0	RW	Emergency shutdown 0 : use powerdown sequence 1 : direct (skip powerdown sequence)
5:4	res_timer	0	RW	Set Reset Time, after the last regulator has started 0 : RESTIME = 0 ms 1 : RESTIME = 5 ms 2 : RESTIME = 11 ms 3 : RESTIME = 15 ms
3:1	ResVoltRise	0	RW	This value determines the reset level ResVoltRise for rising VBAT. ResVoltFall is set to ResVoltRise - 2 steps by default 0 : 2.7V * (ncells+1) 1 : 2.95V * (ncells+1) 2 : 3.1V * (ncells+1) 3 : 3.2V * (ncells+1) 4 : 3.3V * (ncells+1) 5 : 3.4V * (ncells+1) 6 : 3.5V * (ncells+1) 7 : 3.6V * (ncells+1)

Figure 213:
Fuse10

Addr:aah		Fuse10		
Bit	Bit Name	Default	Access	Bit Description
7	unique_id	0	RW	Enable/Disable unique ID If enabled, Fuse42..47 are used for UID and not for startup
6	power_off_at_vsuplow	0	RW	Switch on Power_Off mode if low VBAT/VSUP is detected during Active or Standby mode (pin ONKEY=low and bit auto_off=0) 0 : If low VBAT/VSUP is detected, continuously monitor battery voltage and startup if battery voltage is above ResVoltRise 1 : If low VBAT/VSUP is detected, enter Power_Off mode
5	i2c_deva_bit1	0	RW	Set to 0
4	rtc_on	0	RW	Switch on the 32kHz RTC oscillator 0 : 32kHz oscillator disabled 1 : 32kHz oscillator enabled. This will add 200 ms delay after POR to ensure proper operation.
3	lid_pwr_on	0	RW	Enables exit out of PWR OFF mode with pin LID (pin enabled in PWR off mode) 0 : LID disabled 1 : LID enabled
2	ac_ok_pwr_on	0	RW	Enables exit out of PWR OFF mode with pin AC_OK (pin enabled in PWR off mode) 0 : AC_OK disabled 1 : AC_OK enabled
1	del_time	0	RW	0 : 1 ms delay time 1 : 4 ms delay time
0	sequ_on	0	RW	Set to "1" to enable the start_up sequence

Figure 214:
Fuse11

Addr:abh		Fuse11		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	onkey_lpress_reset	0	RW	Selects behavior on onkey_lpress 0 : change to power_off mode on long press 1 : apply reset on long press
6:5	onkey_shutdown_delay	0	RW	Selects default state of the bit on_shutdown_delay
4	ac_ok_invert	0	RW	Sets the polarity of the AC_OK pin 0 : High active for AC_OK 1 : Inverted: Low active for AC_OK
3	onkey_invert	0	RW	Sets the polarity of the ONKEY pin 0 : High active for ONKEY 1 : Inverted: Low active for ONKEY
2	SupResEn	0	RW	0 : A reset is generated if VBAT or VSUP falls below 2.5V. If VBAT falls below ResVoltFall only an interrupt is generated (if enabled) and the uProcessor can shut down the system) 1 : A reset is generated if VBAT falls below ResVoltFall or VSUP falls below vsup_min
1	gpio12_in_en	0	RW	Don't use
0	lid_invert	0	RW	Sets the polarity of the LID pin 0 : High active for LID 1 : Inverted: Low active for LID

Figure 215:
Fuse12

Addr:ach		Fuse12		
Bit	Bit Name	Default	Access	Bit Description
7:6	sdmph_clk_div	0	RW	Divide clock of SD0,SD1,SD6 by 1,2 or 4 0 : 2.7MHz 1 : 1.35MHz 2 : 0.675MHz 3 : 0.675MHz
5:4	wtdg_mode	0	RW	defines actions when the watchdog expires 0 : interrupt only 1 : performs a reset cycle, then try restart 2 : power-off 3 : performs up to 2 reset cycles, then power-off
3	wtdg_on	0	RW	Enable the watch dog timer. Expiry of the timer will reset the device (see WatchdogControl).
2	enable3_inv	0	RW	Sets the polarity of the ENABLE3 pin 0 : High active for ENABLE3 1 : Inverted: Low active for ENABLE3
1	enable2_inv	0	RW	Sets the polarity of the ENABLE2 pin 0 : High active for ENABLE2 1 : Inverted: Low active for ENABLE2
0	therm_inv	0	RW	Sets the polarity of the THERM pin 0 : High active for THERM event 1 : Inverted: Low active for THERM event

Figure 216:
Fuse13

Addr:adh		Fuse13		
Bit	Bit Name	Default	Access	Bit Description
7:6	sd0_vmax_0	0	RW	
5:4	sd6_trim_gm	0	RW	
3:2	sd1_trim_gm	0	RW	
1:0	sd0_trim_gm	0	RW	

Figure 217:
Fuse14

Addr:aeh		Fuse14		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	sd6_vmax_1	0	RW	Overvoltage protection for SD6 Output voltages are limited to vmax 0 : protection disabled 1 : 1 V 2 : 1.02 V 3 : 1.04 V .. : .. 25 : 1.48 V 26 : 1.50 V
2:0	sd0_vmax_1	0	RW	Overvoltage protection for SD0 Output voltages are limited to vmax 0 : protection disabled 1 : 1 V 2 : 1.02 V 3 : 1.04 V .. : .. 25 : 1.48 V 26 : 1.50 V

Figure 218:
Fuse15

Addr:afh		Fuse15		
Bit	Bit Name	Default	Access	Bit Description
7	rtc_lock	0	RW	RTC write access lock/unlock state at startup 0 : unlock 1 : lock
1:0	ncells	0	RW	Selects number of cells that are connected to VBAT pin 0 : 1 cell: reset_rise = 2.5...3.6 1 : 2 cell: reset_rise = 2*(2.5...3.6) = 5.0....7.2 2 : 3 cell: reset_rise = 3*(2.5...3.6) = 7.5...10.8 3 : 4 cell: reset_rise = 4*(2.5...3.6) = 10....14.4
4:2	vsup_min	0	RW	Defines minimum value on VSUP for startup/reset : vsys_hi 0 : 2.55V 1 : 2.7V 2 : 3.0V 3 : 3.2V 4 : 4.5V 5 : 4.7V 6 : 4.8V 7 : 4.9V
5	I2C_bus_pullup	0	RW	I2C data and CLK PMIC internal pull-ups enabled/dissabled 0 : pull-ups disabled 1 : pull-ups enabled

Figure 219:
Fuse16

Addr:b0h		Fuse16		
Bit	Bit Name	Default	Access	Bit Description
0	Reg0_select_MSB	0	RW	
1	Reg0_delay	0	RW	Selects delay before Slot0 for startup Selects delay after Slot0 for shutdown
2	Reg1_select_MSB	0	RW	
3	Reg1_delay	0	RW	
4	Reg2_select_MSB	0	RW	
5	Reg2_delay	0	RW	
6	Reg3_select_MSB	0	RW	
7	Reg3_delay	0	RW	

Figure 220:
Fuse17

Addr:b1h		Fuse17		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	Reg0_select_LSB	0	RW	Selects Regulator address for startup sequence(Slot0) Address 00..1f selectable (use 1Ch for unused timeslot) 00h : SD0 01h : SD1 .. : .. 06h : SD6 07h : n/a 08h : GPIO0 .. : .. 0Fh : GPIO7 10h : LDO0 .. : .. 1Bh : LDO11 1Ch : unused time slot 1Dh : LD03_settings 1Eh : GPIO_deb1 1Fh : GPIO_deb2
7:4	Reg1_select_LSB	0	RW	

Figure 221:
Fuse44_uniqueID2

Addr:cch		Fuse44_uniqueID2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
0	Reg16_select_MSB	0	RW	
1	Reg16_delay	0	RW	
2	Reg17_select_MSB	0	RW	
3	Reg17_delay	0	RW	
7:4	ASIC_ID3	0	RW	Additional ASIC ID 0 : for die rev. 1v0,1v1,1v2 1 : for die rev. 1v21 (OC_PG function fixed)

Figure 222:
Reg0_control

Addr:e0h		Reg0_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4:0	Reg0_select_stby	1Fh	RW	Selects regulator address for mapping; if Reg0_select_stby>=1Fh then timeslot is unused 00h : SD0 01h : SD1 .. : .. 06h : SD6 07h : n/a 08h : GPIO0 .. : .. 0Fh : GPIO7 10h : LDO0 .. : .. 1Bh : LDO11 1Ch : n/a 1Dh : LD03_settings 1Eh : GPIO_deb1 1Fh : timeslot unused
5	Reg0_delay_stby	0	RW	Selects delay for standby entry after reg0_select is executed; selects delay for standby exit before reg0_select is executed
6	delay_time_stby	0	RW	Selects delay time for standby entry/exit 0 : 1msec delay 1 : 4msec delay

Figure 223:
Reg1_control

Addr:e1h		Reg1_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4:0	Reg1_select_stby	1Fh	RW	Selects regulator for mapping; if Reg1_select_stby>=1Fh then timeslot is unused
5	Reg1_delay_stby	0	RW	

Figure 224:
Reg0_Voltage

Addr:eah		Reg0_Voltage		
Bit	Bit Name	Default	Access	Bit Description
7:0	Reg0_voltage_stby	0	RW	This register is mapped to the register address 0h+Reg0_select, if standby is entered. 0 ..FFh : Selects voltage, ilimit, on or frequency bits of LDO, SD or GPIOs

Figure 225:
Reg1_Voltage

Addr:ebh		Reg1_Voltage		
Bit	Bit Name	Default	Access	Bit Description
7:0	Reg1_voltage_stby	0	RW	This register is mapped to the register address 0h+Reg1_select, if standby is entered. 0 ..FFh : Selects voltage, ilimit, on or frequency bits of LDO, SD or GPIOs

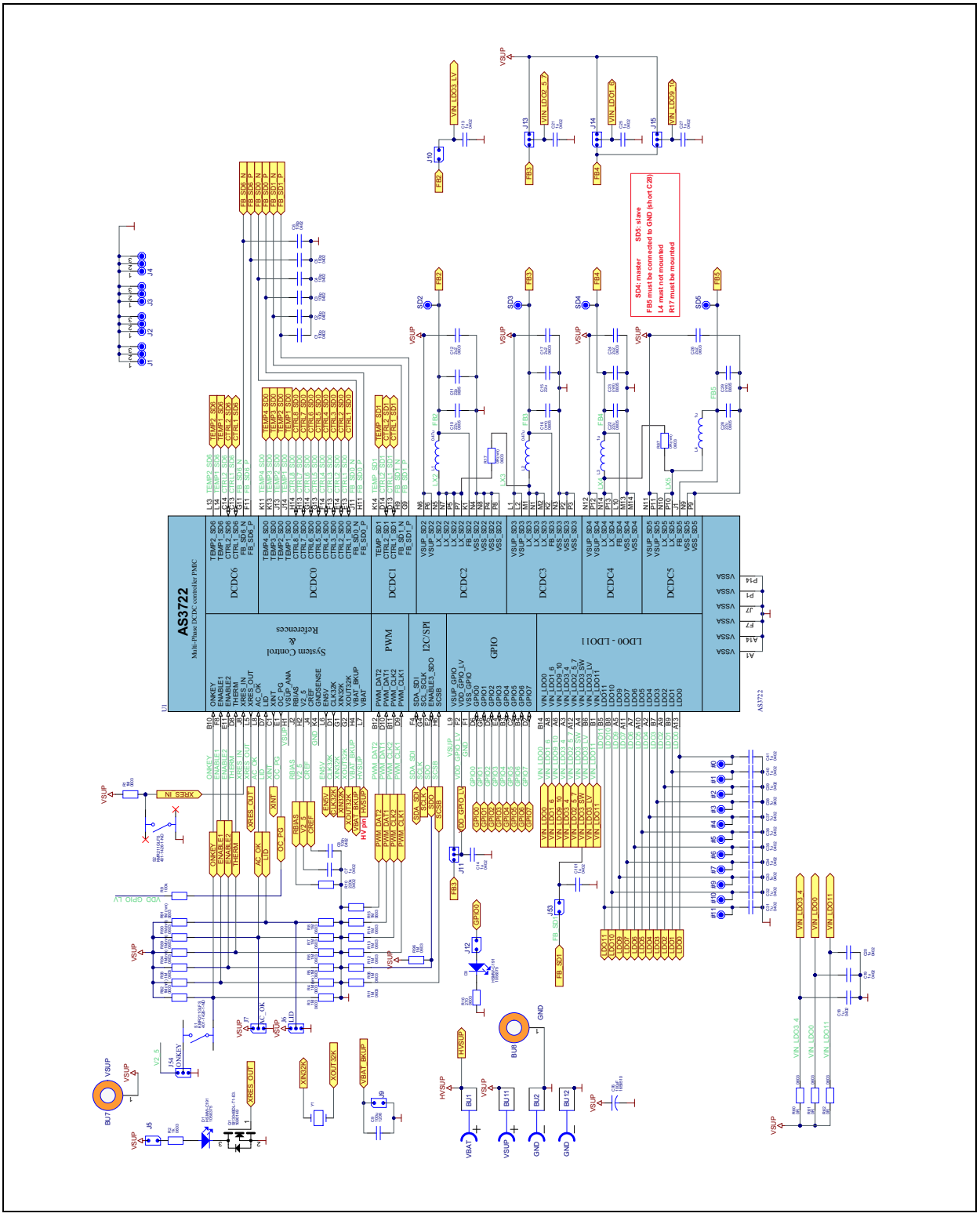
Figure 226:
SpareRegister1

Addr:f4h		SpareRegister1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	disable_stby_lid_int	0	RW_SM	Selection, if LID interrupt is used to exit standby mode directly 0 : Exit stanby mode with LID interrupt 1 : Do not exit stanby mode with LID interrupt, if enable1_deepsleep=1
6	disable_stby_acok_int	0	RW_SM	Selection, if ACOK interrupt is used to exit standby mode directly 0 : Exit stanby mode with AC_OK interrupt 1 : Do not exit stanby mode with AC_OK interrupt, if enable1_deepsleep=1
5	sparereg1	0	RW_SM	
4:0	osc32k_trim	0	RW_SM	Select internal load capacitor on XIN32K and XOUT32k 0h : 12 pF 1h : 12.5 pF 2h : 13 pF 3h : 13.5 pF 4h : 14 pF 5h : 14.5 pF 6h : 15 pF 7h : 15.5 pF .. : .. pF Eh : 19 pF Fh : 19.5 pF 10h : 4 pF 11h : 4.5 pF .. : .. pF 1E : 12 pF 1F : 12.5 pF

Application Information

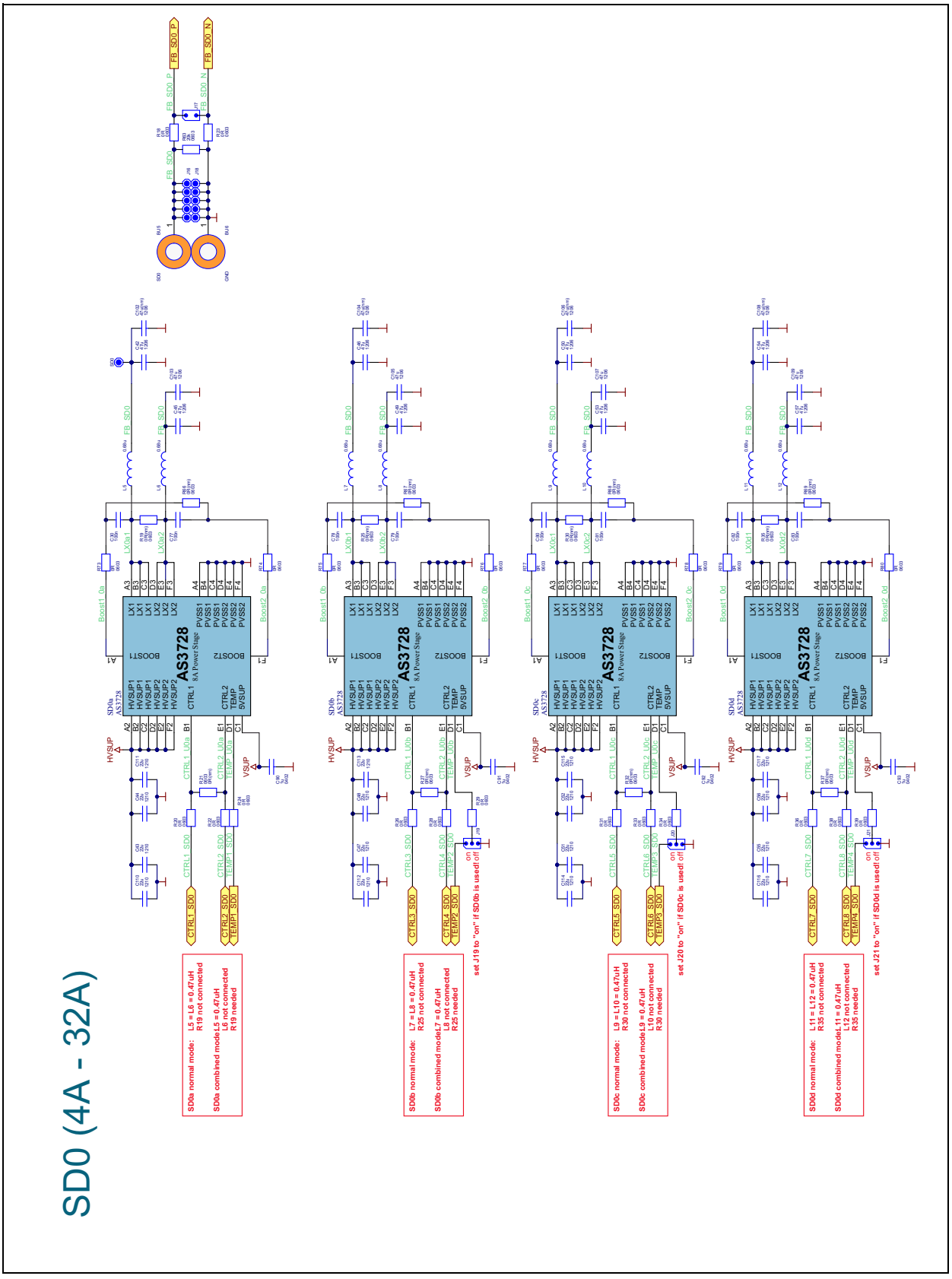
Application Schematics

Figure 227:
Application Schematic 1/3



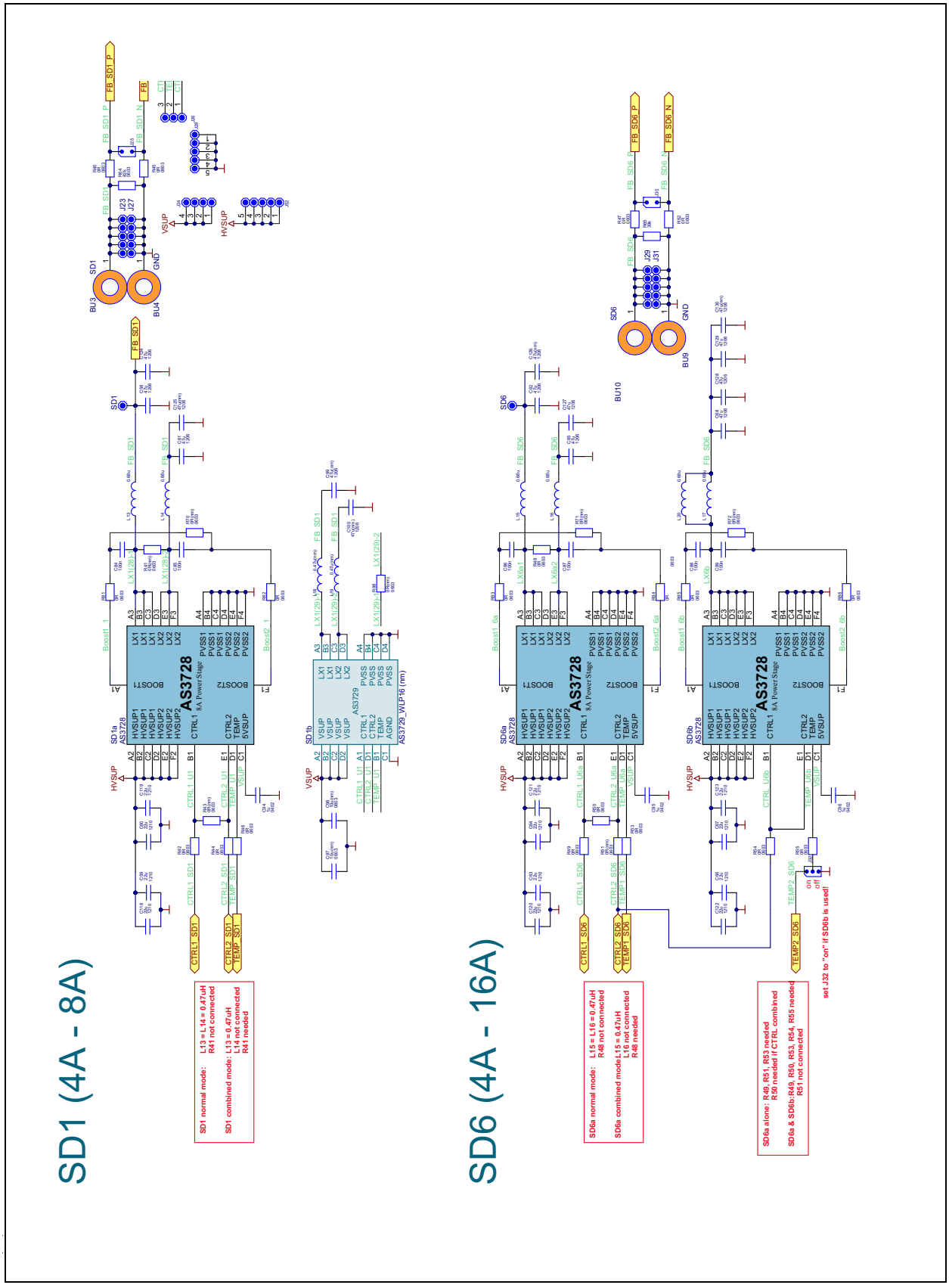
Application Schematic 1/3: Shows a basic application schematic for the internal DCDC/LDOs and system functions

Figure 228:
Application Schematic 2/3



Application Schematic 2/3: Shows a basic application schematic for the SD0 power stages

Figure 229:
Application Schematic 3/3



Application Schematic 3/3: Shows a basic application schematic for the SD1/6 power stages

PCB Routing Recommendations

RBIAS

A critical line on the PMIC is RBIAS. This is a high ohmic node and may pick up noise from nearby clock lines rather easily. Please keep the trace as short as possible and do not route any clock line near to it.

Internal DCDC

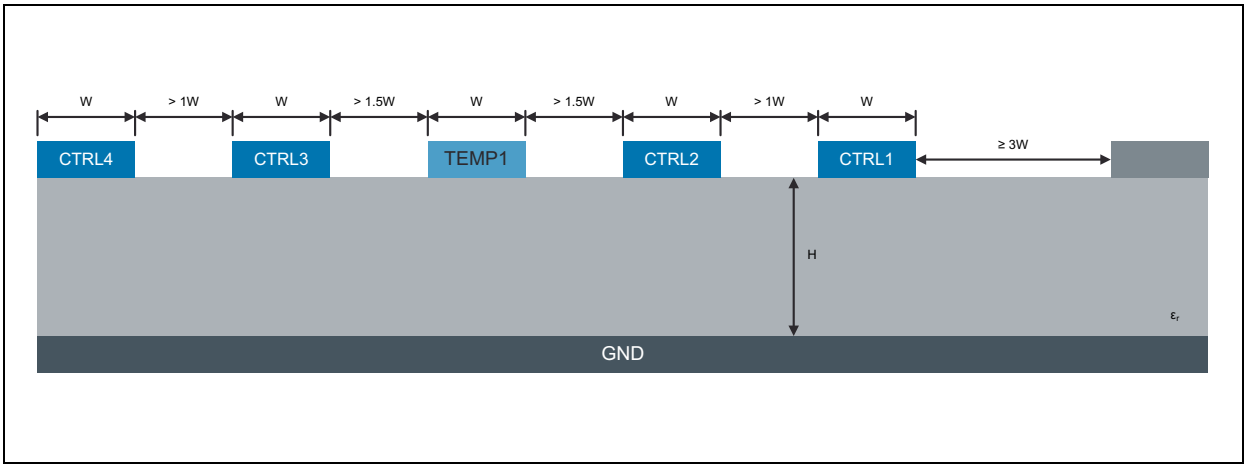
Attention should be paid to the routing of the VSUP, LX and GND traces of the DCDC converter.

- Keep the VSUP traces to the input capacitor as short as possible. Do not use vias for this connection.
- Make a common ground area for the input cap, output cap and PVSS terminal of the DCDC. Connect this ground area with vias to the system ground plane.
- Use short wide traces for LX node. If you need to set vias, use it on the LX trace and not on the capacitor connections.

Power Stage Connections

To avoid cross talk to other lines a minimum spacing of minimum 3W should be kept. For a proper DCDC operation it's recommended to avoid routing other clock traces being routed in parallel (also on other layers) to the control lines.

Figure 230:
PCB Control Line Routing

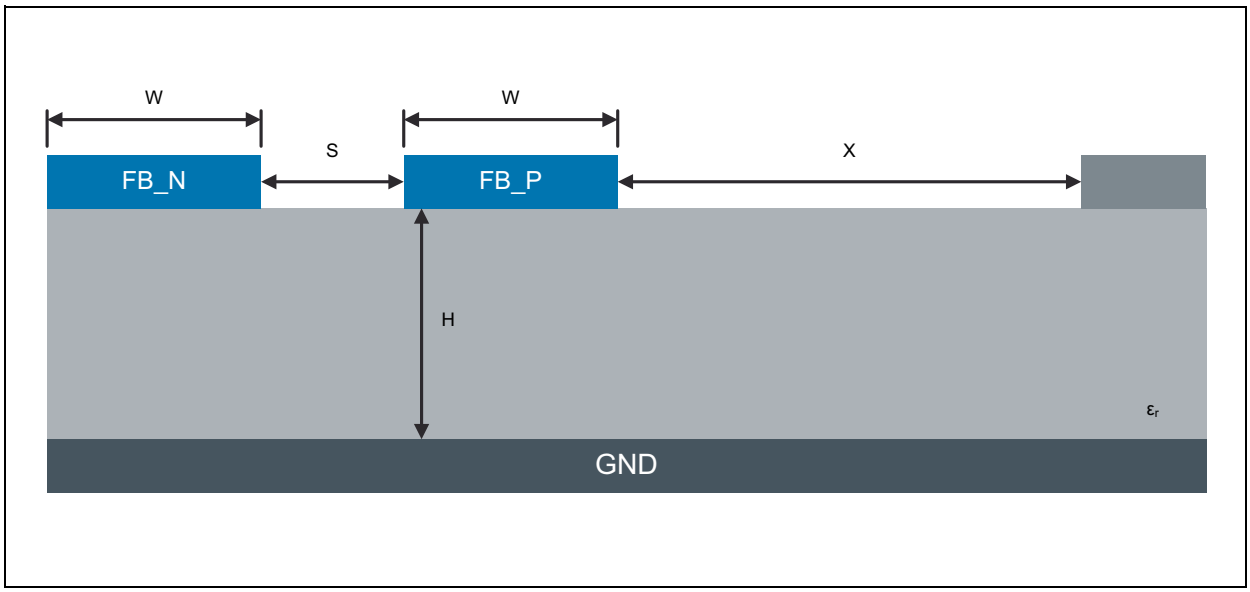


PCB Control Line Routing: Shows an example PCB routing for the control lines of the multiphase controllers.

CTRL1&2, are not interfering with each other as they are running at 180° phase shift. They can be routed with a minimum spacing. The TEMP lines should be used as "guard traces" to other control line pairs (e.g. CTRL3&4 or CTRL 5&6 or CTRL 7&8) as well as to other sensitive or clock traces on the PCB. A minimum spacing of >1.5W should be used as spacing between TEMP and CTRL traces.

To minimize the cross talk of these clock lines, the width of the traces (W) should be the minimum acceptable width for manufacturing (e.g. 4mil).The differential feedback lines are less critical, nevertheless to ensure a good coupling between the differential lines and a low coupling to other traces and ground planes its recommended to have: S<W, S<H, X≥2W and 2S

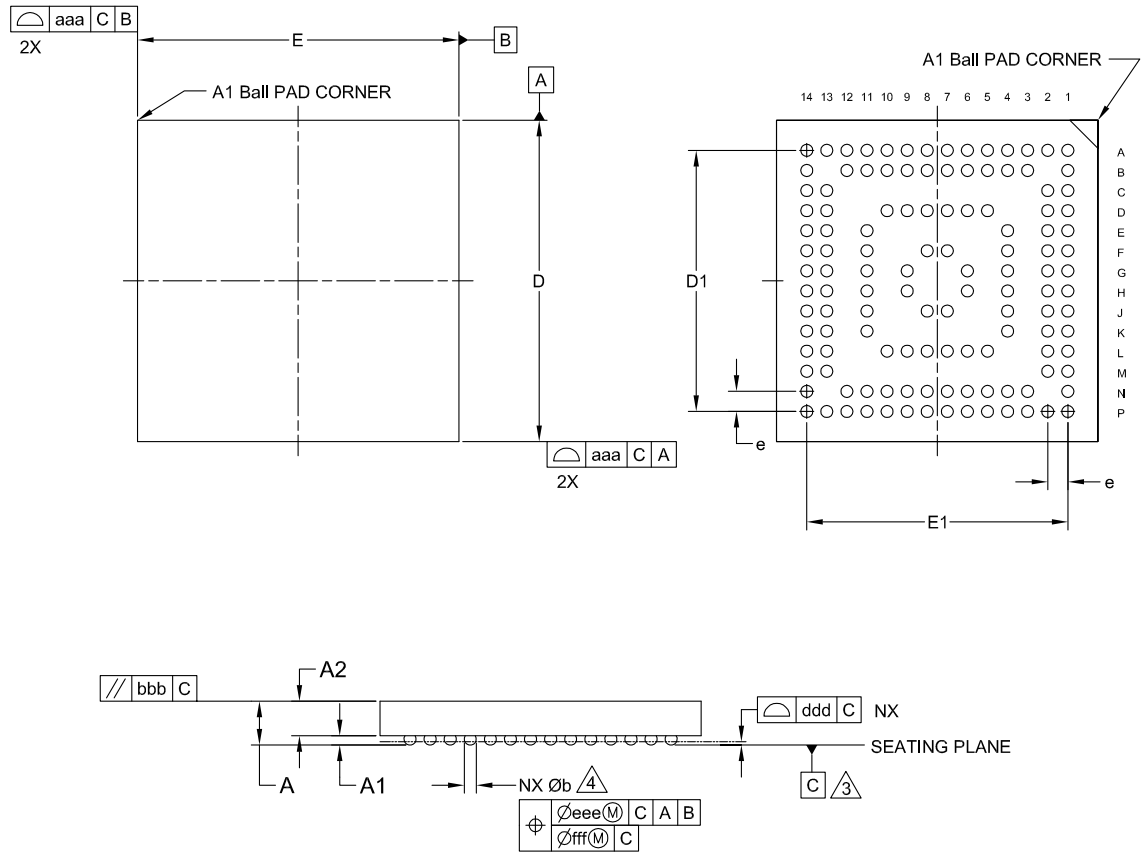
Figure 231:
PCB Differential Feedback Routing



PCB Differential Feedback Routing: Shows an example PCB routing for the differential feedback lines of the multiphase controllers.

Package Drawings & Markings

Figure 232:
Package Drawing (CTBGA)



Ref	Min	Typ	Max
A	-	-	1.20
A1	0.15	-	-
A2	-	-	1.00
b	0.25	0.30	0.35
e		0.50 BSC	
D		8.00	
E		8.00	
E1		6.50	

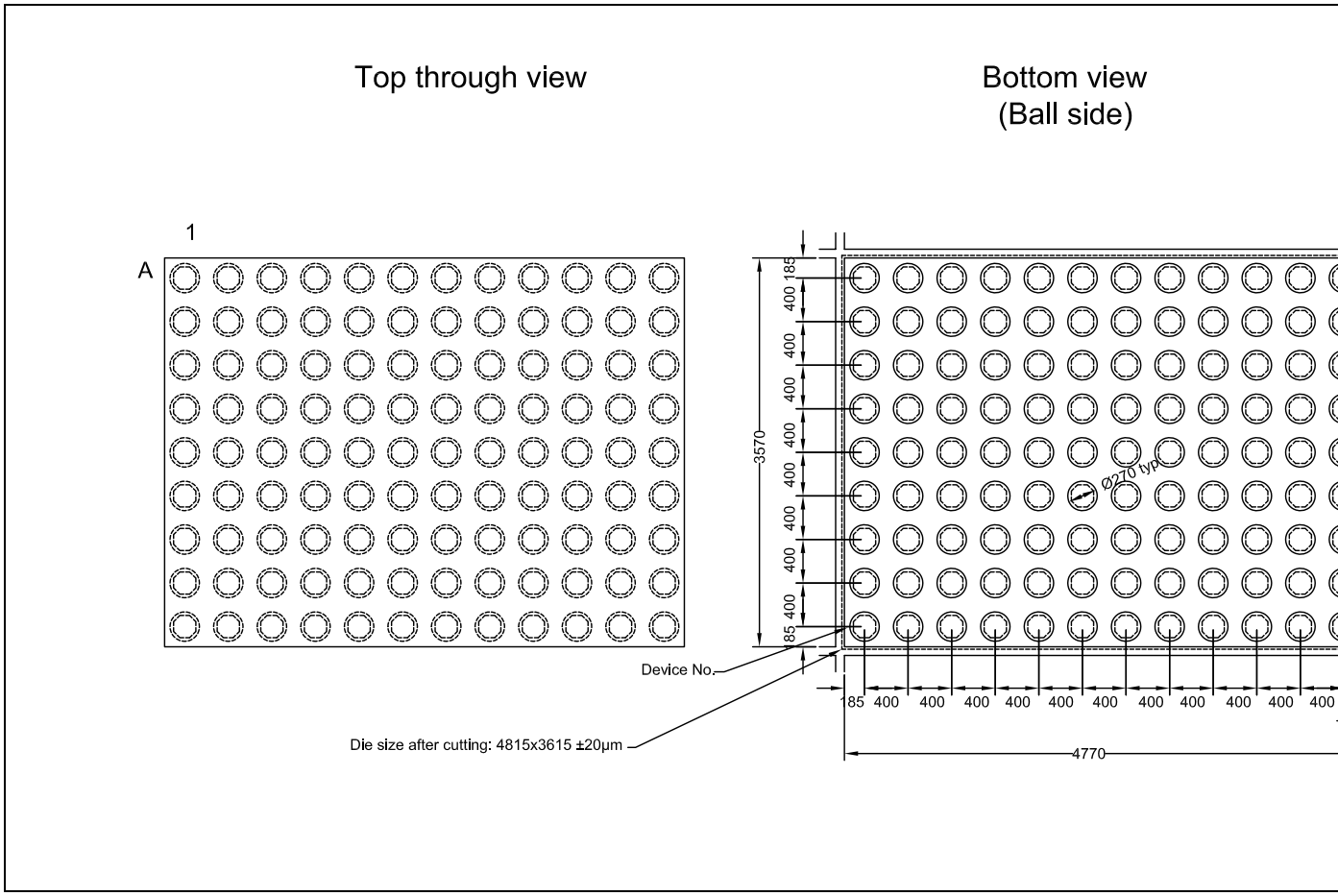
Ref	Min	Typ	Max
D1		6.50	
aaa	-	0.10	-
bbb	-	0.10	-
ddd	-	0.08	-
eee	-	0.15	-
fff	-	0.05	-
N		124	

Package Drawings: Shows the outline dimensions of the CTBGA124 package

Note(s) and/or Footnote(s):

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters.
3. Primary datum C and seating plane are defined by the spherical crowns of the contact balls.
4. Dimensions 'b' is measured at the maximum ball diameter, parallel to primary datum C.

Figure 233:
Package Drawing (WL-CSP)



Package Drawings: Shows the outline dimensions of the WL-CSP108 package

Note(s) and/or Footnote(s):

1. Pin 1=A1
2. ccc Coplanarity
3. All dimensions are in µm

Figure 234:
Package Marking

Package Marking: Shows the package marking for different product versions.

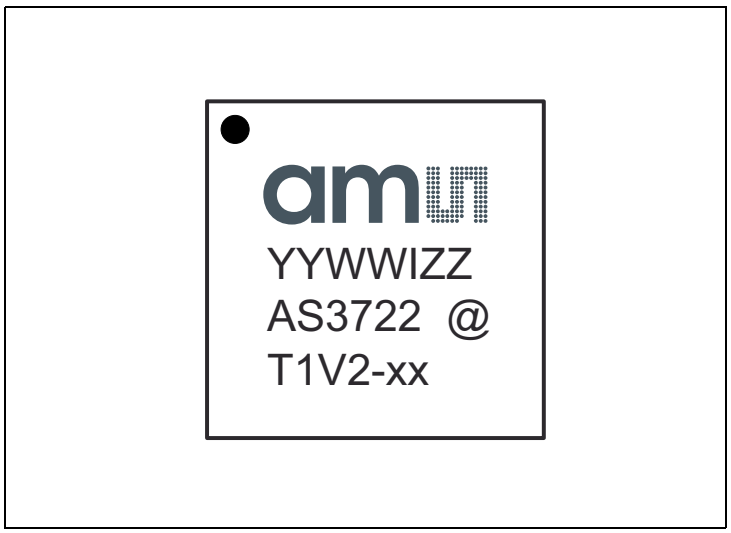


Figure 235:
Package Code

YY	WW	I	ZZ	@
Year	Manufacturing week	Plant identifier	Free choice	Sublot identifier (CTBGA only)

Package Code: Shows the coding of the package marking.

Figure 236:
Start-Up Revision Code

xx	Sequence
ES	Engineering samples, no sequence programmed or sequence programmed on request
00	Standard programming (no sequence programmed)
xx	Other customer specified sequence programmed during production test

Start-Up Revision Code: Shows the coding of the different startup sequences.

Ordering & Contact Information

Figure 237:
Ordering Information

Ordering Code	Marking	OTP programming	Delivery Form	Package
AS3722-BCTR-ES	T1V2-ES	sequence programmable on request	Tray	124-pin CTBGA 0.5mm pitch
AS3722-BCTT-00	T1V2-00	standard programming, no sequence	Tape & Reel	124-pin CTBGA 0.5mm pitch
AS3722-BCTT-xx	T1V2-xx	other customer specified programming	Tape & Reel	124-pin CTBGA 0.5mm pitch
AS3722-BWLW-ES	T1V2-ES	sequence programmable on request	Waffle Pack	108-pin WL-CSP 0.4mm pitch
AS3722-BWLT-00	T1V2-00	standard programming, no sequence	Tape & Reel	108-pin WL-CSP 0.4mm pitch
AS3722-BWLT-xx	T1V2-xx	other customer specified programming	Tape & Reel	108-pin WL-CSP 0.4mm pitch

Ordering Information: Shows the ordering information for the different product versions

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Document Status

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
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Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

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Updated Figure 164	148

Note(s) and/or Footnote(s):

1. Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
2. Correction of typographical errors is not explicitly mentioned.

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66 *Watchdog Input*
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