THE DATASHEET OF

AS1526-BSOT

AS1526, AS1527

DataSheet

10-Bit, Single Supply, Low-Power, 73ksps A/D Converters

1 General Description

The AS1526/AS1527 are low-power, 10-bit, 73ksps analog-to-digital (A/D) converters specifically designed for single-supply A/D applications. Superior AC characteristics, very low power consumption, and robust packaging make these ultra-small devices perfect for battery-powered analog-data collection devices.

The integrated successive-approximation register (SAR) and a fast (1.5µs) sampling track/hold time provide an economic and highly-reliable A/D conversion solution.

The AS1526/AS1527 operate from a single 2.7 to 3.6V supply. The AS1527 requires an external reference, using less power than the AS1526, however, the AS1526 features an internal 2.5V reference.

As with the AS1527, the AS1526 can also be used with an external reference, which uses the input range 0V to V_{REF}, including the positive supply range.

The AS1527 consumes only 3mW (V_{DD} = 3V) at the 73ksps maximum sampling speed. Both devices feature a low-current (0.3µA) shutdown mode, which reduces power consumption at slower throughput rates.

Data accesses are made via the standard, high-speed 3-wire serial interface, which is SPI-, QSPI-, and Microwire-compatible. Both devices contain an internal clock, however, both devices also support an external clock for increased flexibility.

The AS1526/AS1527 are available in an 8-pin SOIC-150 package.

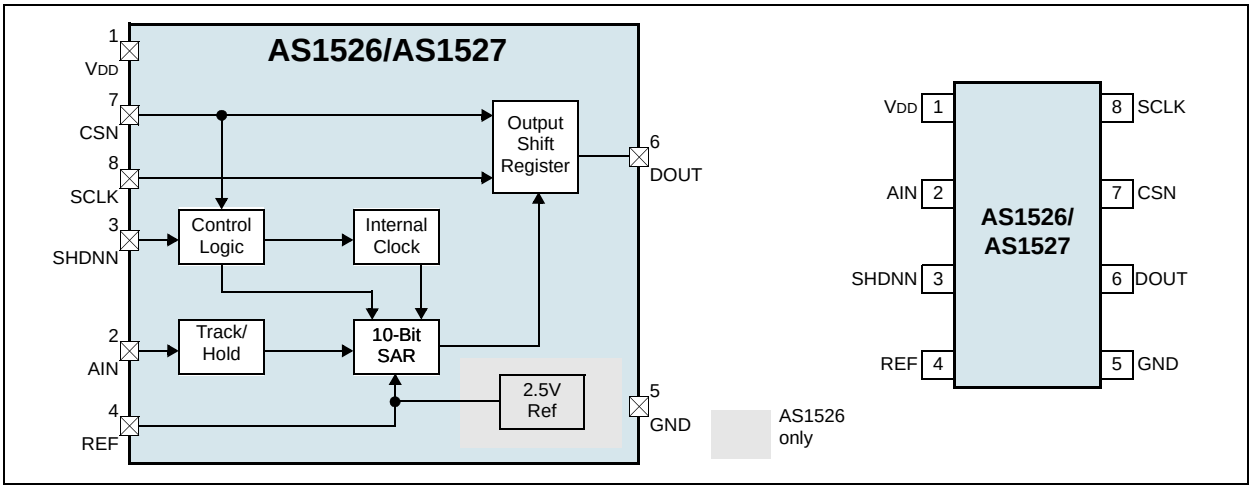
2 Key Features

- 10-Bit Resolution with 7.5µs Conversion Time
- Sampling Rate: 73ksps
- Straight Binary (Unipolar) Data Format
- Single-Supply Operation:+2.7 to +3.6V
- Internal 2.5V Reference (AS1526)
- Low Power-Consumption:
  - 4mW (73ksps, AS1526)
  - 3mW (73ksps, AS1527)
  - 66µW (1ksps, AS1527)
  - 1µW (Shutdown Mode)
- Integrated Track/Hold Amplifier
- Internal Clock
- SPI/QSPI/Microwire 3-Wire Serial Interface
- Operating Temperature Range: -40 to +85ºC
- 8-pin SOIC-150 Package

3 Applications

The devices are ideal for remote sensors, data-acquisition, data logging devices, lab instruments, or for any other space-limited A/D devices with low power consumption and single-supply requirements.

Figure 1. Block Diagram and Pin Assignments



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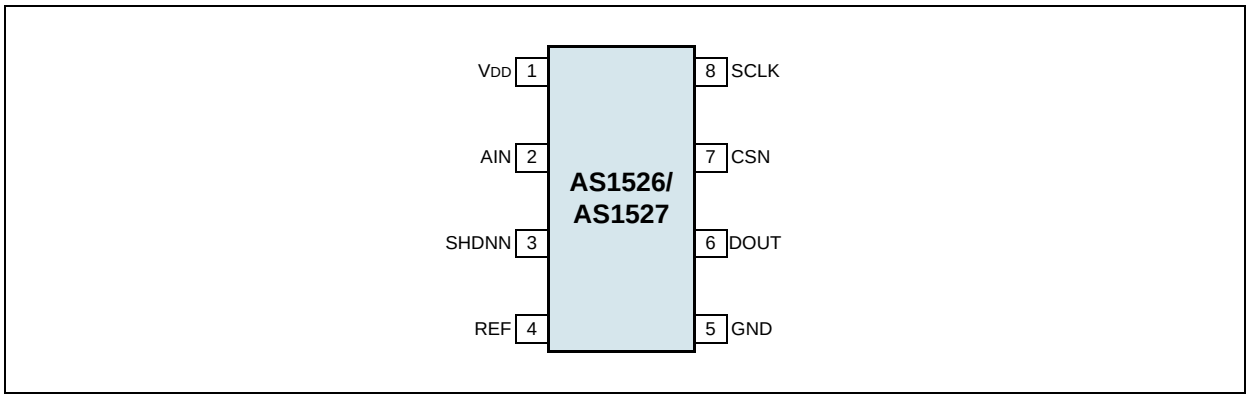
4 Pinout and Packaging

Pin Assignments

Figure 2. Pin Assignments (Top View)



Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Pin Name	Description
1	VDD	**Positive Supply Voltage**. +2.7 to +3.6V
2	AIN	**Sampling Analog Input**. 0V to VREF range.
3	SHDNN	**Three-Level Shutdown Input**. Pulling this pin low puts the AS1526/AS1527 in shutdown mode, down to 4µA (max) supply current. The devices are fully operational with this pin high or floating. **Note:** For the AS1526, pulling this pin high enables the internal reference; letting this pin float disables the internal reference allowing for the use of an external reference. See also pin 4.
4	REF	**A/D Conversion Reference Voltage**. This pin serves as the internal 2.5V reference output for the AS1526; bypass this pin with a 4.7µF capacitor. This pin also serves as the external reference voltage input for the AS1527, or for AS1526 if the internal reference is disabled. Bypass this pin with a minimum of 0.1µF when using an external reference. See also pin 3.
5	GND	**Analog and Digital Ground**
6	DOUT	**Serial Data Output**. Data changes state at SCLK's falling edge. **Note:** This pin is high-impedance when pin CSN is high.
7	CSN	**Active-Low Chip Select**. The falling edge of this pin initiates a conversion. **Note:** When this pin is high, DOUT is high-impedance.
8	SCLK	**Serial Clock Input**. This pin clocks data out at rates up to 2.1MHz.

5 Absolute Maximum Ratings

Stresses beyond those listed in Table 2 may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in Section 6 Electrical Characteristics on page 5 is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Min	Max	Units	Comments
V_{DD} to GND	0.3	+5	V	
AIN to GND	-0.3	V_{DD} + 0.3V	V	
REF to GND	-0.3	V_{DD} + 0.3V	V	
Digital Inputs to GND	-0.3	V_{DD} + 0.3V	V	
DOUT to GND	-0.3	V_{DD} + 0.3V	V	
DOUT Current	-25	+25	mA	
Continuous Power Dissipation (T_{AMB} = +70ºC)		471	mW	Derate 5.88mW/ºC above +70ºC
Operating Temperature Range	-40	+85	ºC	
Storage Temperature Range	-60	+150	ºC	
Package-Body Peak Temperature		260	°C	The reflow peak soldering temperature (body temperature) specified is in accordance with *IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices"*.

6 Electrical Characteristics

V_{DD} = +2.7 to +3.6V, 73ksps, f_{SCLK} = 2.1MHz (50% duty cycle); AS1526:4.7µF capacitor at REF, AS1527: external reference; V_{REF} = 2.5V applied to REF; T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified).

Table 3. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy [1]						
	Resolution		10			Bits
	Relative Accuracy [2]				±0.5	LSB
DNL	Differential Non-Linearity	No missing codes over temperature			±1	LSB
	Offset Error				±2	LSB
	Gain Error [3]				±2	LSB
	Gain Temperature Coefficient			±1		ppm/°C
Dynamic Specifications (10kHz sine-wave input, 0V to 2.5Vp-p, 73ksps, f_{SCLK} =2.1MHz)						
SINAD	Signal-to-Noise + Distortion Ratio			61		dB
THD	Total Harmonic Distortion	Up to the 5th harmonic		-70		dB
SFDR	Spurious-Free Dynamic Range			70		dB
	Small-Signal Bandwidth	-3dB rolloff		2.5		MHz
	Full-Power Bandwidth			2.5		MHz
Conversion Rate						
t_{CONV}	Conversion Time		5.5		7.5	µs
t_{ACQ}	Track/Hold Acquisition Time				1.5	µs
	Throughput Rate [4]	f_{SCLK} = 2.1MHz			73	ksps
t_{AP}	Aperture Delay	Figure 27 on page 13		7		ns
	Aperture Jitter			<50		ps
Analog Input						
	Input Voltage Range		0		V_{REF}	V
	Input Capacitance			21		pF
Internal Reference (AS1526 only)						
	REF Output Voltage	T_{AMB} = +25ºC [5]	2.47	2.50	2.53	V
	REF Short-Circuit Current				45	mA
	REF Temperature Coefficient	AS1526		±30		ppm/°C
	Load Regulation [6]	0 to 0.2mA output load		0.35		mV
C_{REFBYP}	Capacitive Bypass at *REF*		4.7			µF
External Reference (V_{REF} = 2.5V)						
	Input Voltage Range		1.00		V_{DD} + 50mV	V
	Input Current			100	150	µA
	Input Resistance		18	25		kΩ
	REF Input Current in Shutdown	SHDNN = 0V		±0.01	10	µA
C_{REFBYP}	Capacitive Bypass at *REF*		0.1			µF

Table 3. Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital Inputs: SCLK, SHDNN, CSN						
V_{IH}	SCLK, CSN Input High Voltage		0.7x V_{DD}			V
V_{IL}	SCLK, CSN Input Low Voltage				0.3x V_{DD}	V
V_{HYST}	SCLK, CSN Input Hysteresis			0.2		V
I_{IN}	SCLK, CSN Input Leakage	V_{IN} = 0V or V_{DD}		±0.01	±1	µA
C_{IN}	SCLK, CSN Input Capacitance [7]				15	pF
V_{SH}	SHDNN Input High Voltage		V_{DD} - 0.4			V
V_{SL}	SHDNN Input Low Voltage				0.4	V
	SHDNN Input Current	SHDNN = 0V or V_{DD}			±4.0	µA
V_{SM}	SHDNN Input Mid Voltage		1.1		V_{DD} - 1.1	V
V_{FLT}	SHDNN Voltage, Floating	SHDNN = float		$V_{DD}/2$		V
	SHDNN Max Allowed Leakage, Mid Input	SHDNN = float			±50	nA
Digital Output: DOUT						
V_{OL}	Output Voltage Low	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA			0.8	
V_{OH}	Output Voltage High	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
I_L	Tri-State Leakage Current	CSN = V_{DD}		±0.01	±10	µA
C_{OUT}	Tri-State Output Capacitance	CSN = V_{DD} [7]			15	pF
Power Requirements						
V_{DD}	Supply Voltage		2.7		3.6	V
I_{DD}	Supply Current	Int. Reference (AS1526), V_{DD} = 3.6V		1.4	2.0	mA
		External Reference, V_{DD} = 3.6V		1.0	1.4	
		Shutdown mode, V_{DD} = 3.6V		0.3	2	µA
PSR	Power-Supply Rejection [8]	V_{DD} = V_{DDMIN} to V_{DDMAX}, full-scale input		±1		mV

1. Tested at V_{DD} = +2.7V.
2. Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range and offset have been calibrated.
3. Offset nulled.
4. Achievable with standard timing (see Figure 25 on page 13).
5. Sample tested at 0.1% AQL.
6. External load should not change during conversion for specified accuracy.
7. Guaranteed by design; not subject to production testing.
8. Measured as [$V_{FS}(V_{DDMIN})$ - $V_{FS}(V_{DDMAX})$] with external reference.

Timing Characteristics

V_{DD} = +2.7 to +3.6V, T_{AMB} = T_{MIN} to T_{MAX} (unless otherwise specified).

Table 4. Timing Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Acquisition Time [1]	t_{ACQ}		1.5			µs
SCLK Falling-to-DOUT Valid	t_{DO}	Figure 3, C_{LOAD} = 50pF	20		200	ns
CSN Falling-to-Output Enable	t_{DV}	Figure 3, C_{LOAD} = 50pF			240	ns
CSN Rising-to-Output Disable	t_{TR}	Figure 4, C_{LOAD} = 50pF			240	ns
SCLK Clock Frequency	f_{SCLK}		0		2.1	MHz
SCLK Pulse Width High	t_{CH}		200			ns
SCLK Pulse Width Low	t_{CL}		200			ns
SCLK Low-to-CSN Falling Setup Time	t_{CS0}		50			ns
DOUT Rising-to-SCLK Rising [2]	t_{STR}		0			ns
CSN Pulse Width	t_{CS}		240			ns

1. To guarantee acquisition time, t_{ACQ} is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the signal to be acquired
2. Guaranteed by design; not subject to production testing.

Figure 3. DOUT Enable-Time Load Circuits

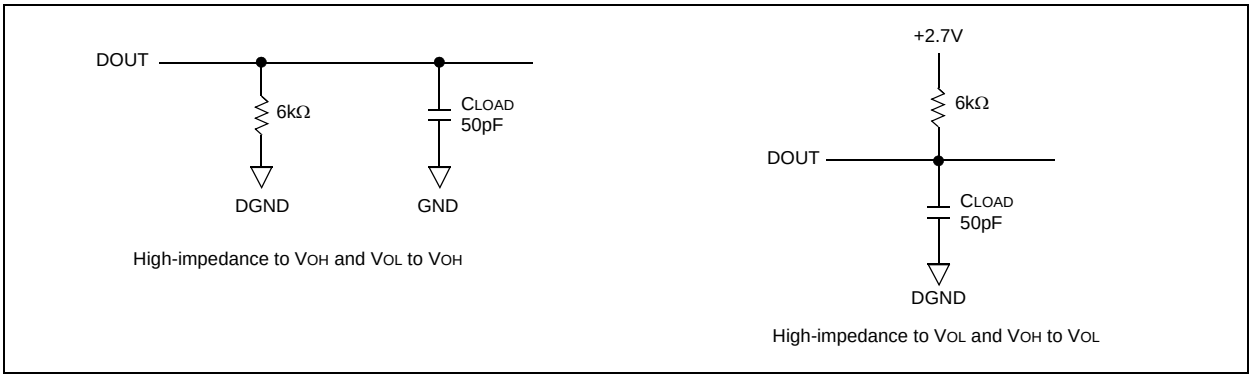
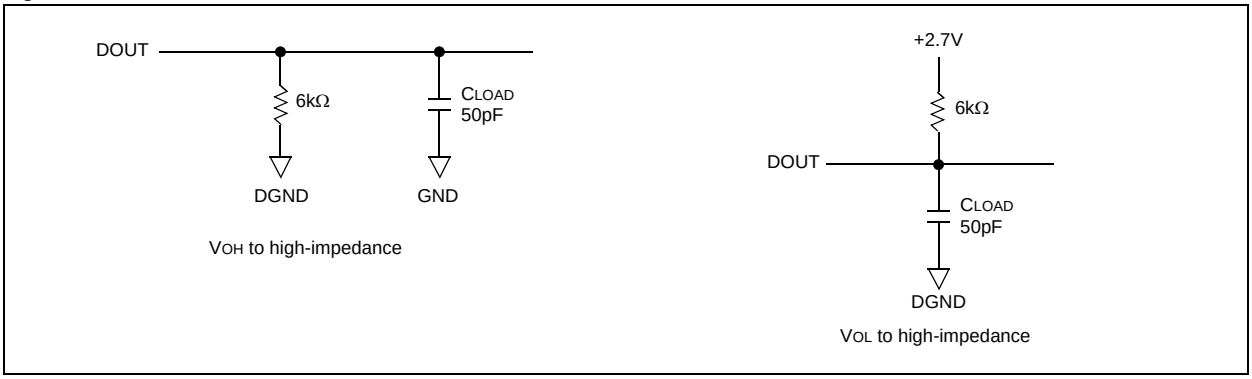


Figure 4. DOUT Disable-Time Load Circuits



7 Typical Operating Characteristics

V_{DD} = 3.0V, V_{REF} = 2.5V, f_{SCLK} = 2.1MHz, C_{LOAD} = 50pF, T_{AMB} = +25ºC (unless otherwise specified).

Figure 5. Integral Nonlinearity vs. Digital Output Code

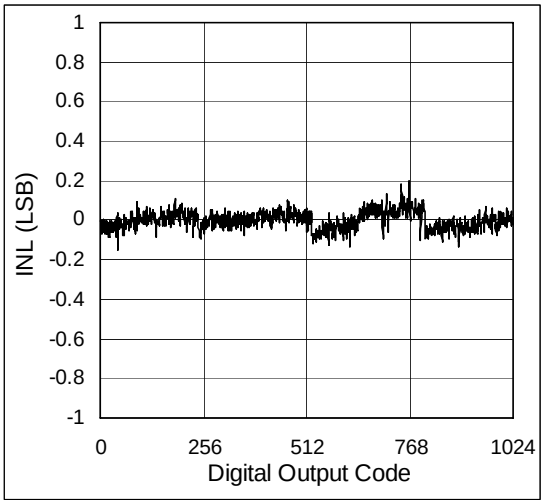


Figure 6. Differential Nonlinearity vs. Digital Output Code

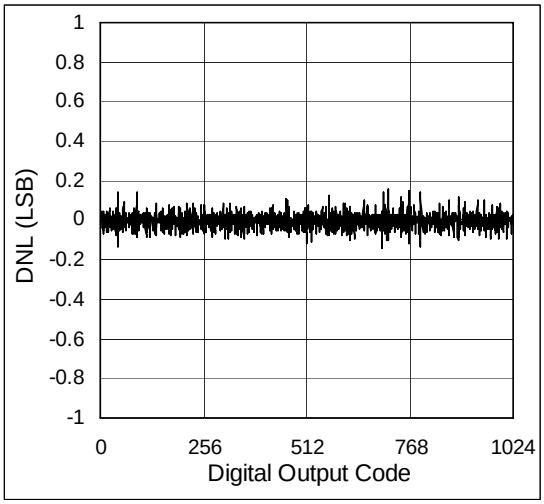


Figure 7. FFT @ 1kHz

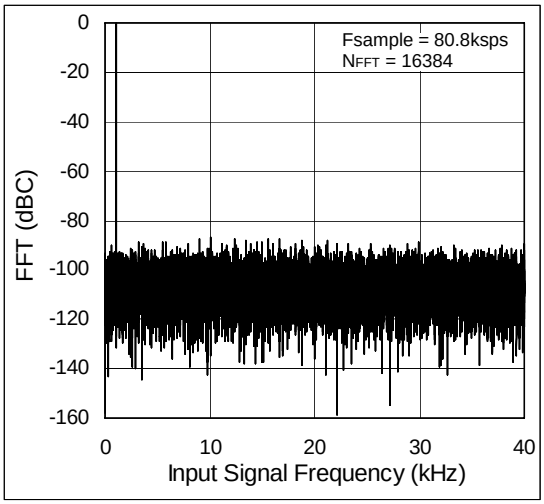


Figure 8. FFT @ 10kHz

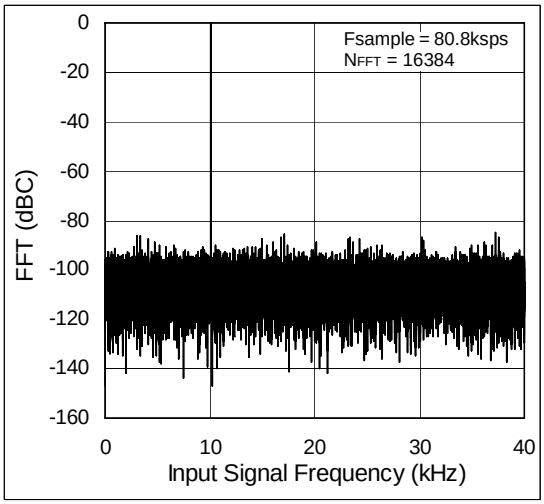


Figure 9. ENOB vs. V_{REF}

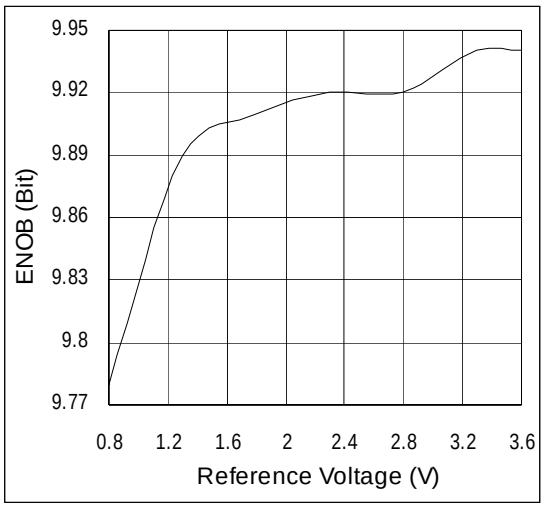


Figure 10. ENOB vs. Input Signal Frequency

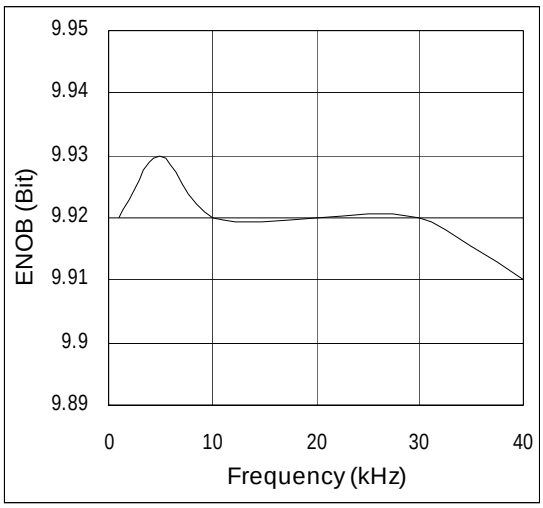


Figure 11. Supply Current vs. Supply Voltage

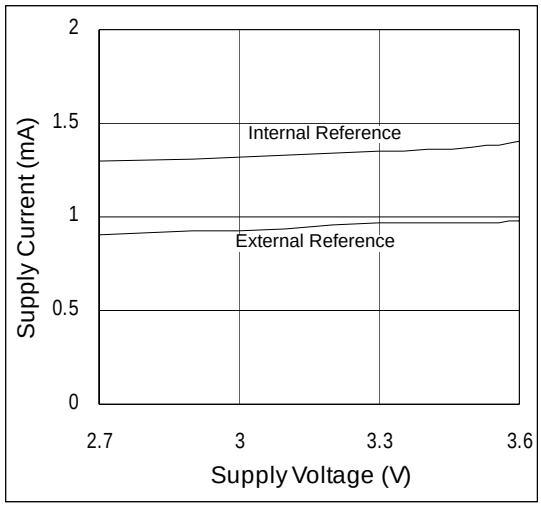


Figure 12. Supply Current vs. Temperature

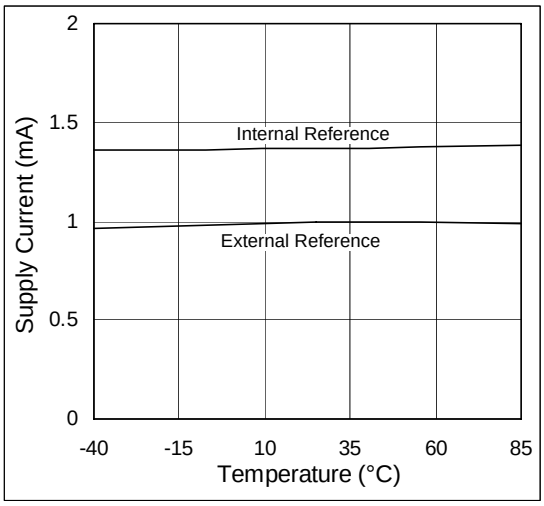


Figure 13. Shutdown Supply Current vs. Supply Voltage

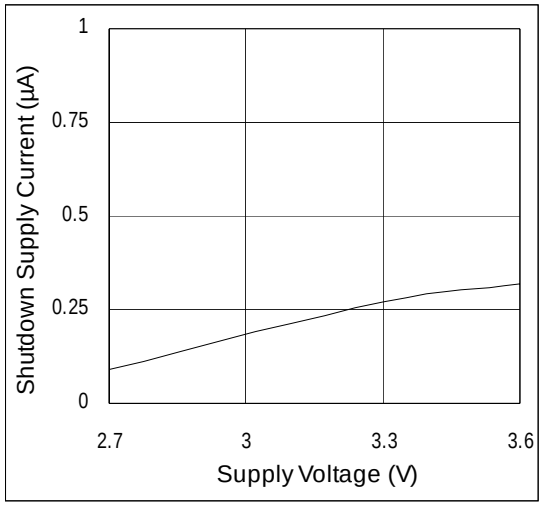


Figure 14. Shutdown Supply Current vs. Temperature

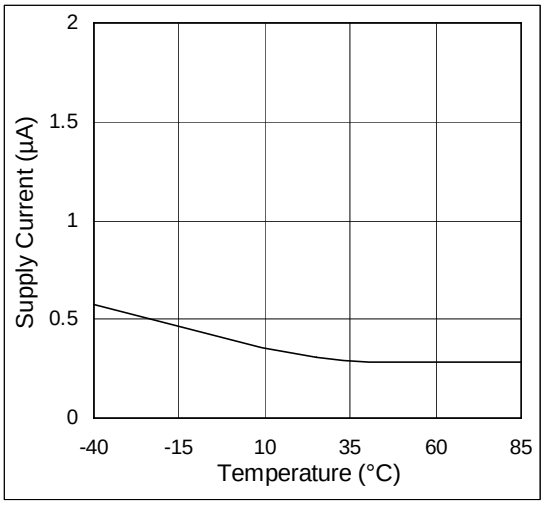


Figure 15. Offset Error vs. Supply Voltage

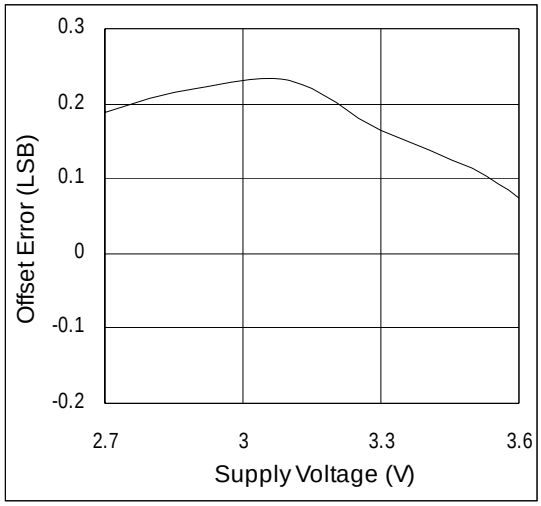


Figure 16. Offset Voltage vs. Temperature

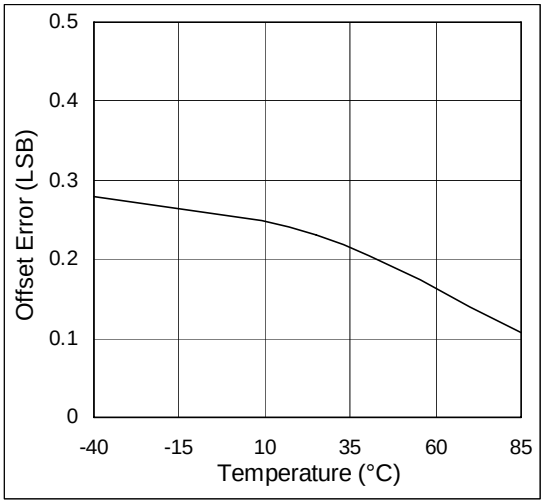


Figure 17. Gain Error vs. Supply Voltage

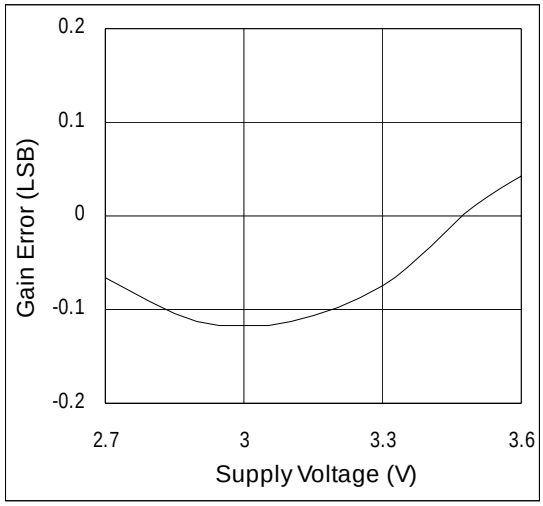


Figure 18. Gain Error vs. Temperature

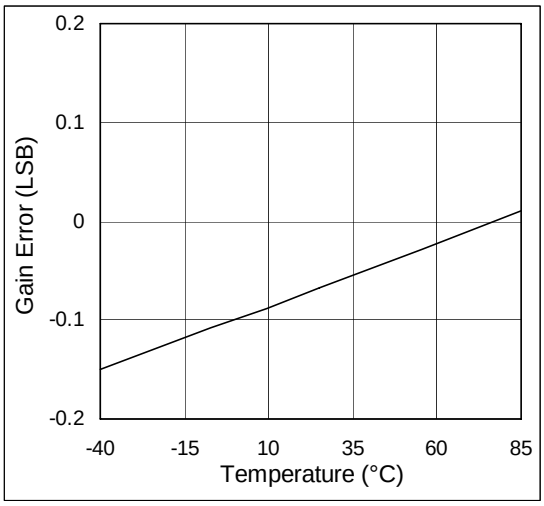


Figure 19. Internal Reference Voltage vs. Supply Voltage

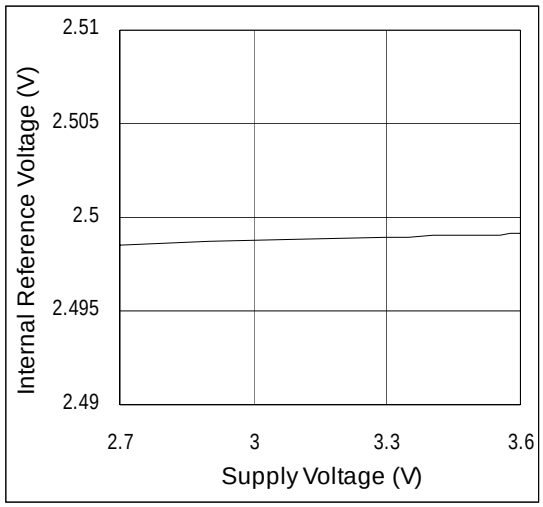


Figure 20. Internal Reference Voltage vs. Temperature

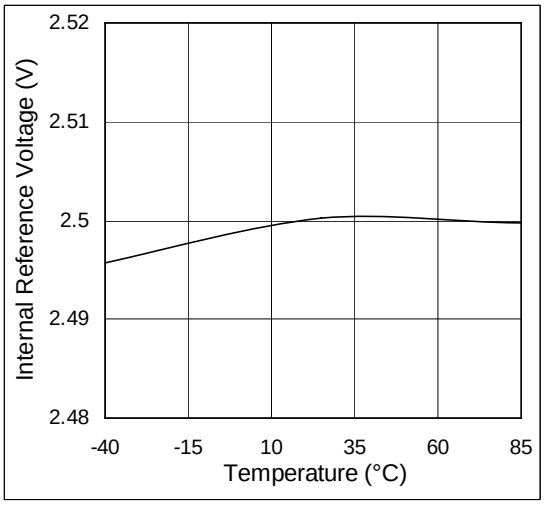


Figure 21. Integral Nonlinearity vs. Supply Voltage

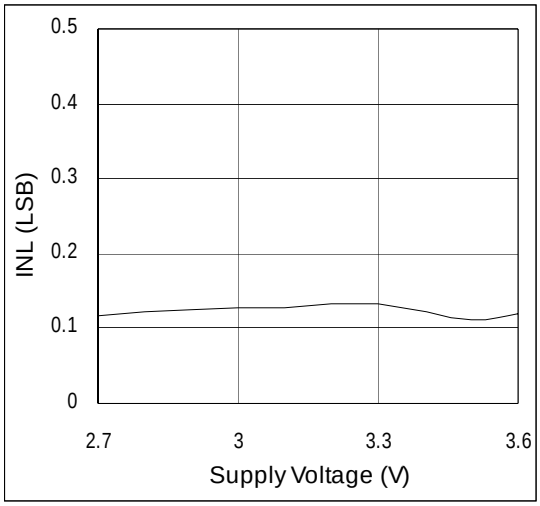
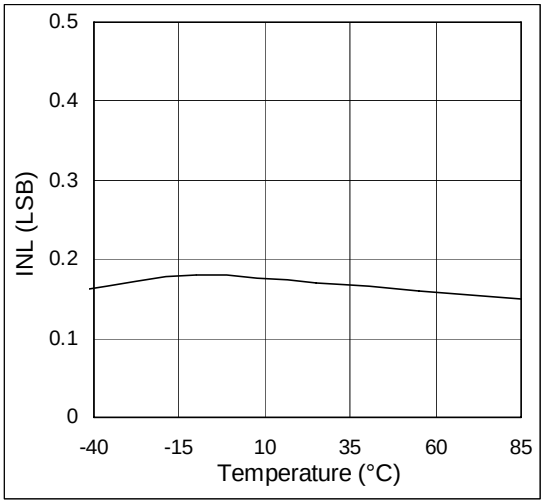


Figure 22. Integral Nonlinearity vs. Temperature



8 Detailed Description

The AS1526/AS1527 analog-to-digital converters have two modes of operation:

- Normal A/D Conversion Mode – Pulling pin SHDNN high or leaving it open puts the device into normal A/D conversion mode.
- Shutdown Mode – Pulling pin SHDNN low shuts the device down and reduces supply current below 2µA ($V_{DD} \leq$ 3.6V).

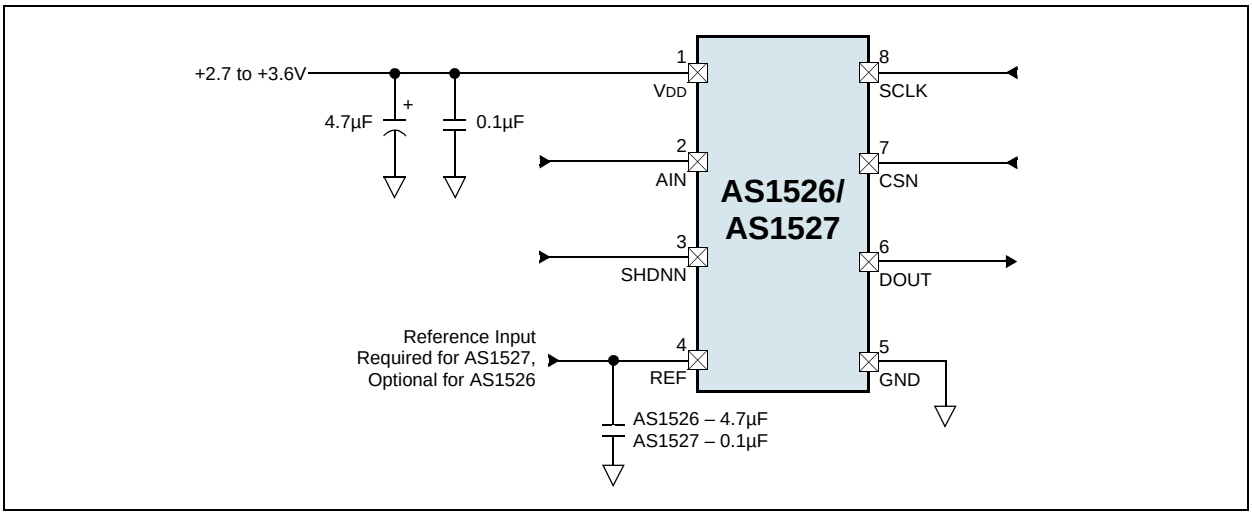
Note: Pulling pin CSN low starts a conversion. The conversion result is available at pin DOUT in unipolar serial format (see Timing and Control on page 12).

Figure 23 shows a basic configuration for the AS1526/AS1527. The integrated input track/hold circuitry and a successive-approximation register (SAR) circuitry convert analog input signals to a digital 10-bit output. No external-hold capacitor is needed for the track/hold circuit.

The devices convert analog input signals in the 0V to V_{REF} range in 13µs (includes track/hold acquisition time).

The AS1526 internal reference is trimmed to 2.5V; the AS1527 requires an external reference. Both devices can accept external reference voltages from 1.0V to V_{DD}. The serial interface requires only three digital lines (at pins SCLK, CSN, and DOUT) and provides a simple microprocessor interface.

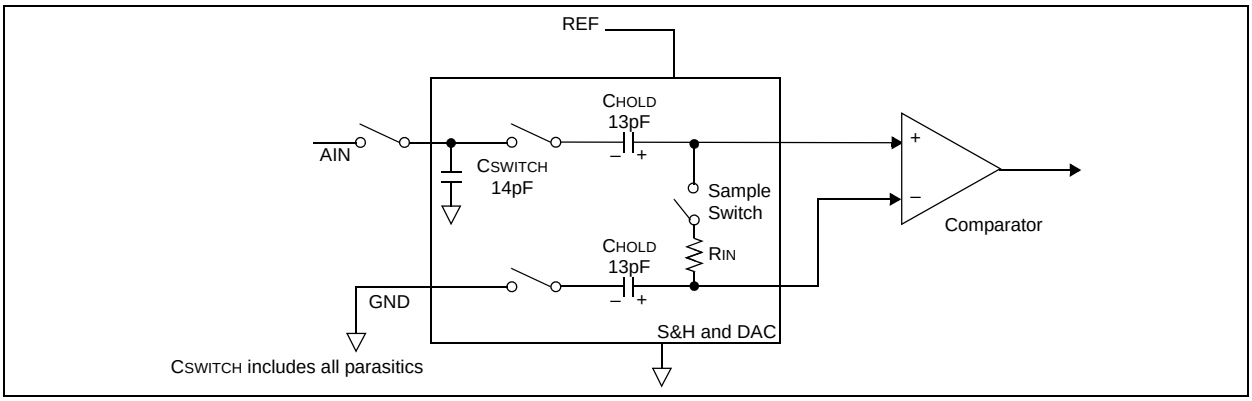
Figure 23. Operational Diagram



Analog Input

Figure 24 illustrates the integrated comparator sampling architecture. The full scale input voltage is set by the voltage at pin REF.

Figure 24. Equivalent Input Circuit



The devices' input tracking circuitry has a 2.5MHz small-signal bandwidth, thus it is possible to under-sample (digitize high-speed transient events) and measure periodic signals with bandwidths exceeding the devices' sampling rate.

Note: Anti-aliasing filtering should be used to avoid aliasing of unwanted high-frequency signals into the bandwidth of interest.

Input Protection

Internal protection diodes clamp the analog input to V_{DD} and GND, allowing the input to swing from (GND - 0.3V) to (V_{DD} + 0.3V) without damage. However, for accurate conversions near full scale, the input must not exceed V_{DD} by more than 50mV, or be lower than GND by 50mV.

Note: If the analog input exceeds the supply by 50mV, limit the input current to 2mA.

Track/Hold

In track mode, the analog signal is acquired and stored in the internal hold capacitors. During acquisition, the analog input at pin AIN charges capacitor C_{HOLD} (see Figure 24 on page 11). Bringing CSN low ends the acquisition interval and the charge on C_{HOLD} represent the sampled input voltage.

In hold mode, the T/H switches are opened thus the input is disconnected from the capacitor C_{HOLD}. During this mode the successive approximation is performed which in turn forms a digital representation of the analog input signal. At the end of the conversion, the input side of the in meantime discharged C_{HOLD} switches back to AIN, and C_{HOLD} charges to the input signal again.

The maximum time for the T/H to acquire a signal (t_{ACQ}) is a function of how quickly its input capacitance is charged. t_{ACQ} increases proportionally to the input signal's impedance, and at higher impedances more time must be allowed between conversions. t_{ACQ} is also the minimum time needed for the signal to be acquired, and is calculated by:

$$t_{ACQ} = 7(R_S + R_{IN}) \times 21pF \qquad (EQ\ 1)$$

Where:

R_{IN} = 4.5kΩ

R_S = the input signal's source impedance.

t_{ACQ} is never less than 1.5µs. Source impedances < 1kΩ do not significantly affect the AC performance of the devices.

Note: Higher source impedances can be used if a 0.01µF capacitor is connected to the analog input. Note that the input capacitor forms an RC filter with the input source impedance, limiting the devices' input signal bandwidth.

External Clock

The AS1526/AS1527 do not require an external clock for analog-to-digital data conversion. This allows the microprocessor to read back the conversion results at any clock rate from up to 2.1MHz at any time. The clock duty cycle is unrestricted if each clock phase is at least 200ns.

Note: The external clock must not be run while a conversion is in progress.

Timing and Control

Conversion-start and data-read operations are controlled by digital inputs CSN and SCLK. Refer to Figures 25 - 27 (see page 13) for graphical timing and control information.

The falling edge on pin CSN initiates a conversion sequence:

1. The T/H stage holds the voltage at pin AIN, and the A/D conversion begins.
2. Pin DOUT changes from high-impedance to logic-low. SCLK must be kept low during the conversion.
3. The internal SAR stores the data during the conversion process.
4. Pin DOUT going high indicates the conversion process has completed.
5. The rising edge of pin DOUT can be used as a framing signal.
6. SCLK shifts the data out of this register any time after the conversion is complete.
7. DOUT transitions on the falling edge of pin SCLK.
8. The next falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are 10 data bits and one leading high-bit or 10 data bits, two sub bits, and one leading high-bit, at least 11 or 13 falling clock edges are needed to shift out these bits, respectively.

9. Extra clock pulses occurring after the conversion result has been clocked out, and prior to a rising edge of CSN, produce trailing zeros at DOUT and have no effect on the conversion process.
10. For minimum cycle time, clock out the data with 10.5 clock cycles at full speed using the rising edge of DOUT as the EOC signal. Pull CSN high after reading the conversion's LSB. After the specified minimum time (tCS) CSN can be pulled low to initiate the next conversion.

Figure 25. Serial Interface Standard Cycle Timing Diagram

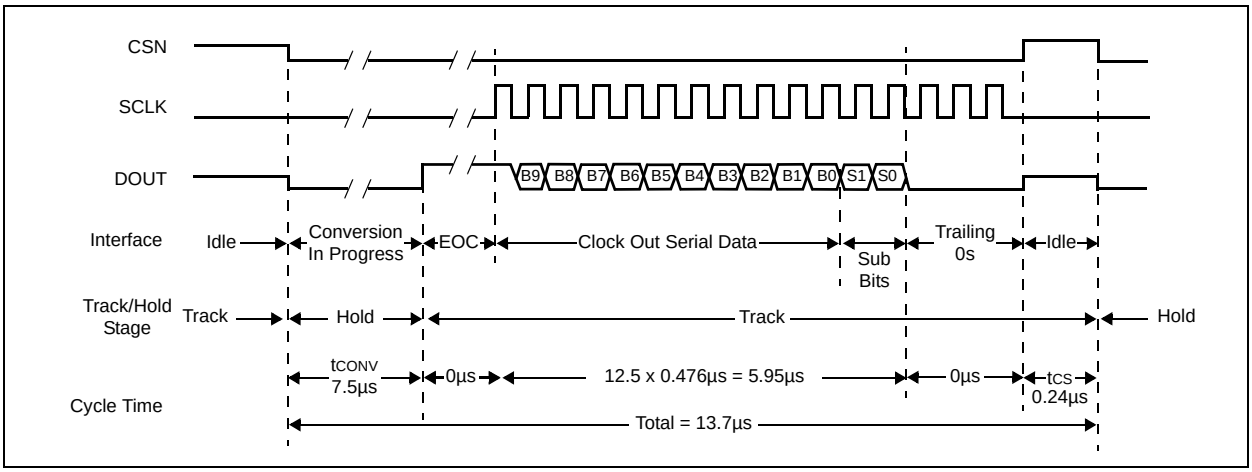


Figure 26. Serial Interface Minimum Cycle Timing Diagram

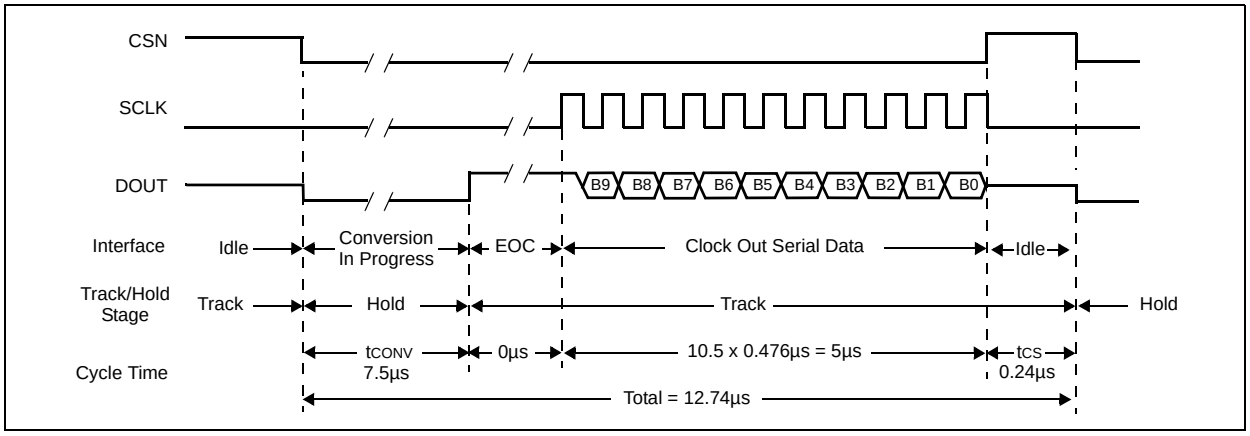
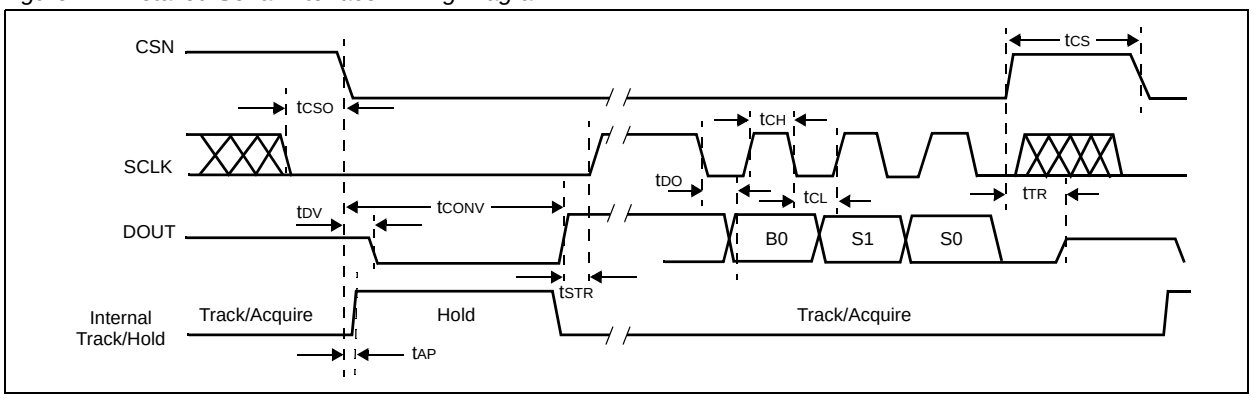


Figure 27. Detailed Serial Interface Timing Diagram

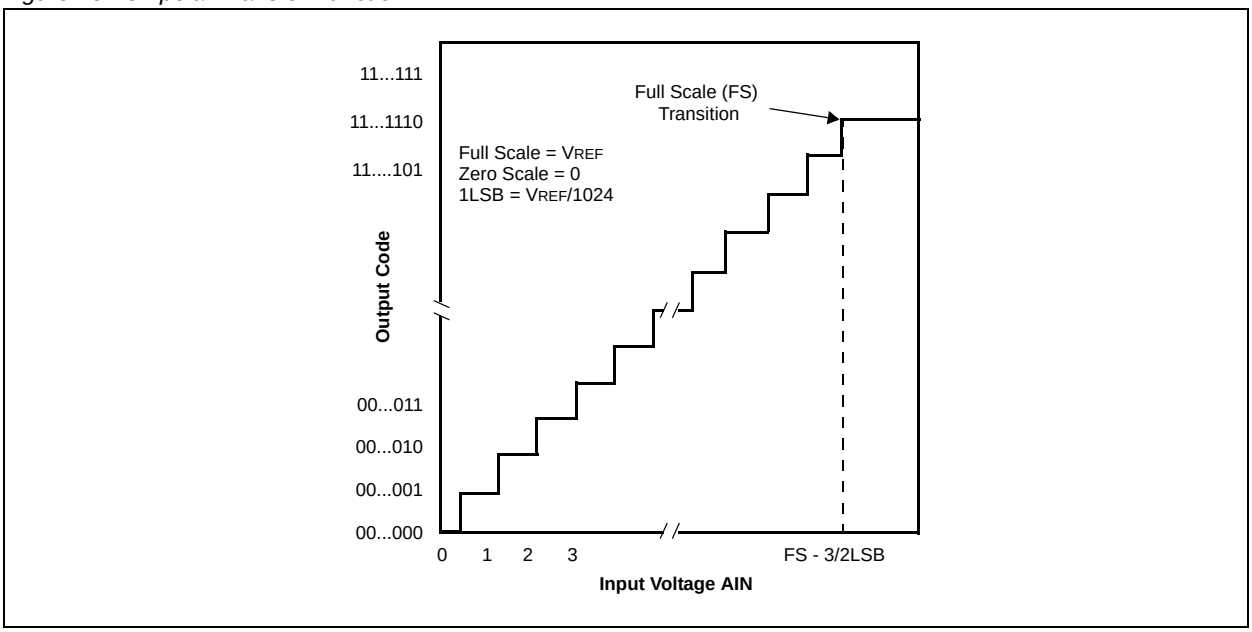


Transfer Function

The data output from the AS1526/AS1527 is binary (unipolar), and Figure 28 depicts the nominal transfer function. Code transitions occur midway between successive integer LSB values.

Note: If VREF = +2.50V, then 1 LSB = 2.44mV (2.50V/1024).

Figure 28. Unipolar Transfer Function

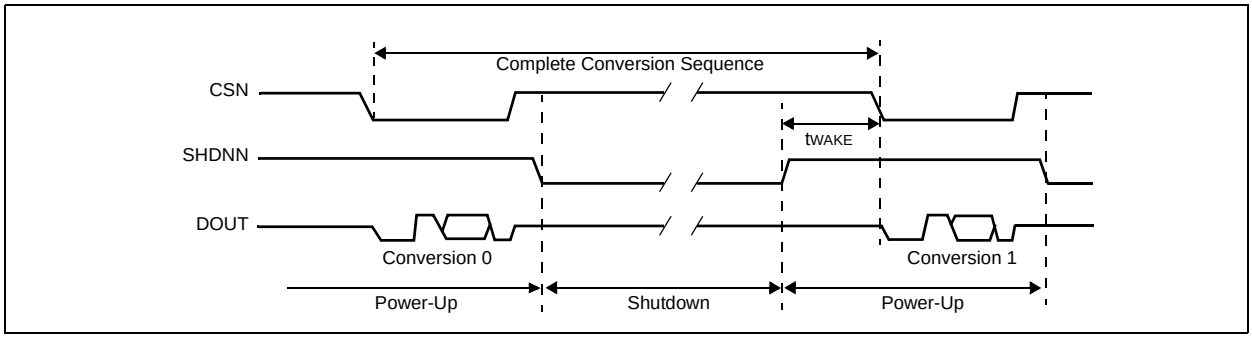


Reducing Supply Current

Power consumption can be reduced significantly by powering down the devices between conversions. Figure 30 shows a plot of an average supply current versus sampling rate.

Wake-up time (tWAKE) can also factor into reduced power consumption. tWAKE is defined as the time from when pin SHDNN is deasserted to the time when a conversion may be initiated (see Figure 29).

Figure 29. Shutdown Sequence Timing Diagram



For the AS1526 using the internal reference, tWAKE depends on the time in shutdown mode (see Figure 31) since the external 4.7µF reference bypass capacitor slowly loses charge during shutdown. The wakeup time for AS1526 and AS1527 using an internal reference are largely dependent on the external reference's power-up time. The wakeup time for the ADC itself from shutdown mode is approximately 4µs.

Figure 30. Supply Current vs. Sampling Rate

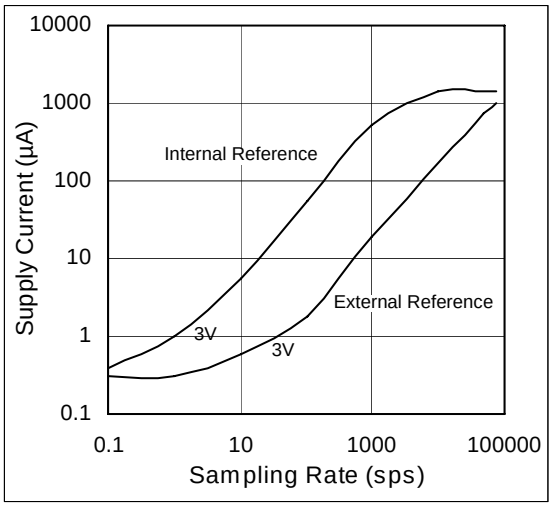
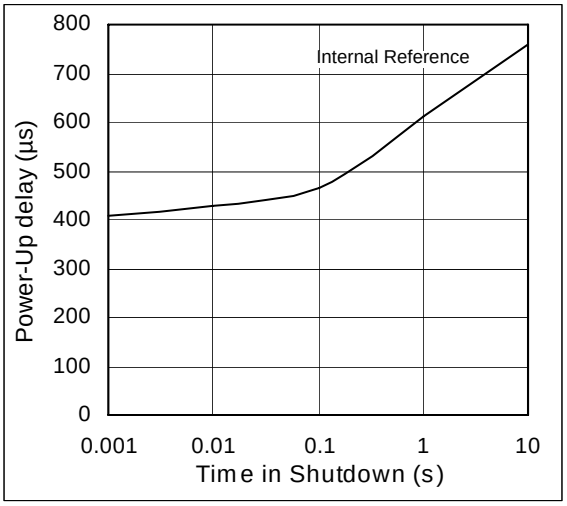


Figure 31. Powerup Time vs. Time in Shutdown



Internal 2.5V Reference (AS1526)

The AS1526 internal 2.5V reference output is connected to pin REF and also drives the internal DAC (see Figure 24 on page 11). REF output can be used as a reference voltage source for other components and can source up to 400µA.

The internal reference is enabled by pulling pin SHDNN high. Letting SHDNN float disables the internal reference, which allows the use of an external reference (see External Reference on page 15).

Pin REF should be bypassed with a 4.7µF capacitor as shown in Figure 23 on page 11. Larger capacitors increase wake-up time when the devices exit shutdown mode (see Layout Considerations on page 18)

External Reference

Both devices can operate with an external reference at pin REF. The external reference should be within the +1.0V to V_{DD} voltage range to achieve specified accuracy. The minimum input impedance is 18kΩ for DC currents.

Note: To use an external reference with the AS1526, disable the internal reference by letting pin SHDNN float.

During conversion, the external reference should be capable of delivering up to 250µA of DC load current and have an output impedance ≤ 10Ω. The recommended minimum value for the bypass capacitor is 0.1µF. If the reference has higher output impedance or is noisy, bypass it close to pin REF with a 4.7µF capacitor.

9 Application Information

Initialization

When power is first applied, and if SHDNN is not pulled low, it takes the fully discharged 4.7µF reference bypass capacitor up to 20ms to provide adequate charge for specified accuracy.

With an external reference, the initialization time is 10µs after the power supplies have stabilized.

Note: A/D conversions must not be started during initialization of the AS1526/AS1527.

Serial Interface

The AS1526/AS1527 fully support SPI, QSPI, and Microwire interfaces. For SPI, select the correct clock polarity and sampling edge in the SPI control registers (set CPOL = 0 and CPHA = 0).

Microwire, SPI, and QSPI all transmit a byte and receive a byte at the same time.

Serial Interface Configuration

The AS1526/AS1527 serial interface can be configured with the following procedure:

1. Put the microprocessor's serial interface into master mode (so that it generates the serial clock).
2. Select a clock frequency up to 2.1MHz.
3. Keeping SCLK low, pull CSN low via one of the microprocessor's general-purpose I/O lines.
4. Monitor DOUT for its rising edge to determine the EOC, or wait the maximum conversion time specified before activating SCLK.
5. Activate SCLK for a minimum of 11 clock cycles. The first falling clock edge produces the MSB of the conversion. Output data transitions on the falling edge of SCLK, and is available in MSB-first format at pin DOUT. Observe the SCLK to DOUT valid timing characteristic. Data can be clocked into the microprocessor on the rising edge of SCLK.
6. CSN should be pulled high at or after the 13th falling clock edge. If CSN remains low, trailing zeros are clocked out after the LSB.
7. With CSN = high, wait the minimum specified time, t_{CS}, before initiating a new conversion by pulling CSN low. If a conversion is aborted by pulling CSN high before the conversion's end, wait for the minimum acquisition time, t_{ACQ}, before starting a new conversion.

   Note: CSN must be held low until all data bits are clocked out.
8. Data can be output in two bytes or continuously (see Figure 34 on page 17). The bytes contain the result of the conversion padded with one leading 1, two sub-bits, and trailing 0s.

SPI and Microwire Interfaces

When interfacing the AS1526/AS1527 to a microprocessor's SPI or Microwire interface (see Figure 32 and Figure 33), set SPI control registers CPOL = 0 and CPHA = 0.

Figure 32. SPI Serial Interface Connections

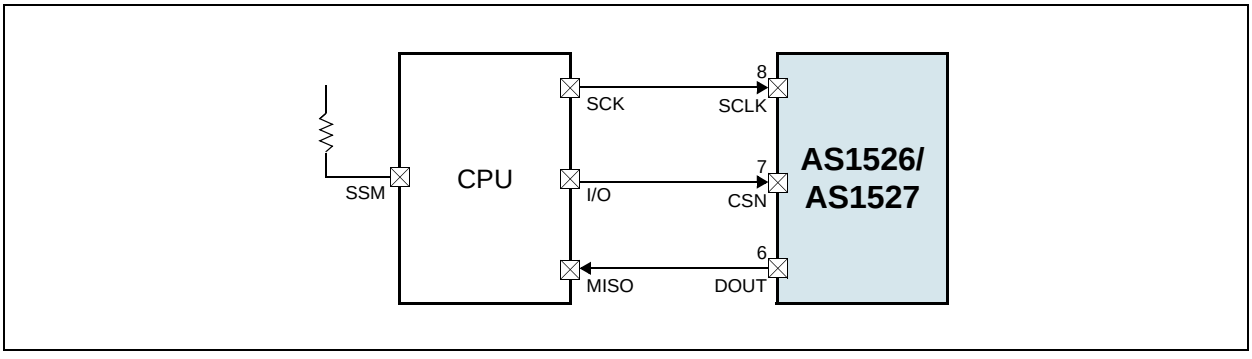
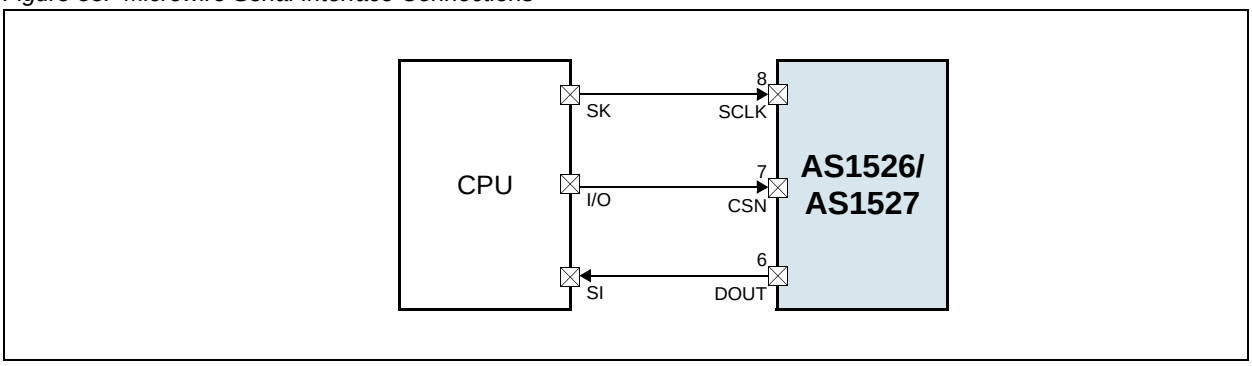


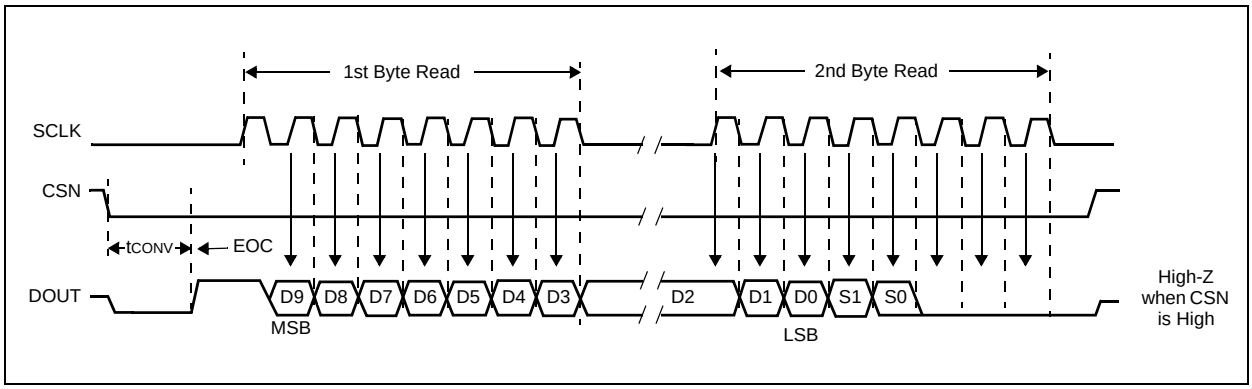
Figure 33. Microwire Serial Interface Connections



A conversion process begins on the falling edge of CSN (see Figure 34). DOUT goes low, indicating a conversion is in progress. Wait until DOUT goes high or until the maximum specified conversion time elapses before starting another conversion. Two consecutive 1-byte reads are required to retrieve the full 10+2 bits from the devices.

Output data transitions occurs on the falling edge of SCLK, and is clocked into the microprocessor on the rising edge of SCLK. The first byte contains a leading 1, and seven bits of conversion result data. The second byte contains the remaining three bits of conversion result data, two sub-bits, and three trailing zeros.

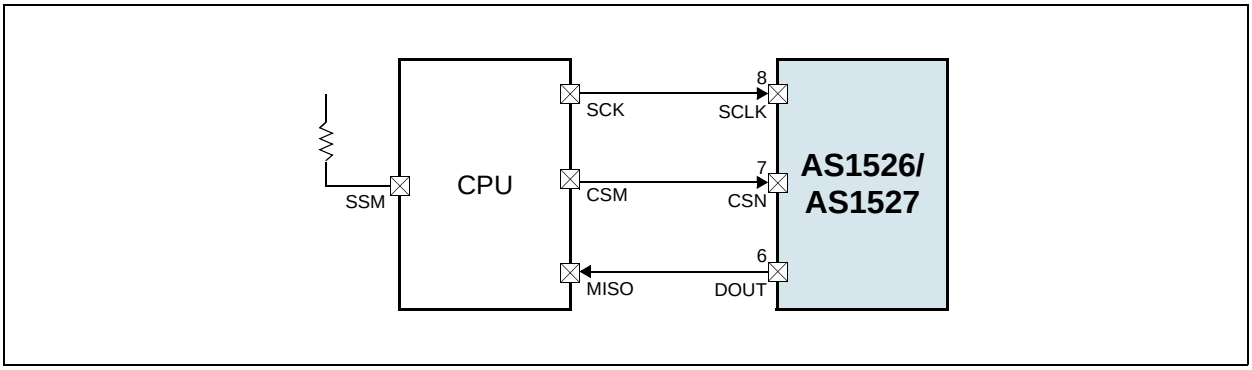
Figure 34. SPI/Microwire Serial Interface Timing (CPOL = CPHA = 0)



QSPI

When interfacing the AS1526/AS1527 to a microprocessor's QSPI interface (see Figure 35), set QSPI control register CPOL = CPHA = 0.

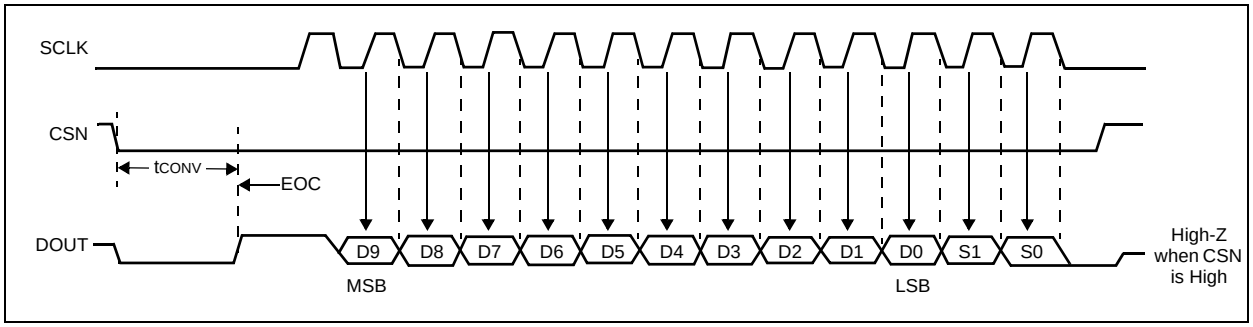
Figure 35. QSPI Serial Interface Connections



Unlike the SPI interface, which requires two 1-byte reads to acquire the 10 data bits from the AS1526/AS1527, QSPI allows the minimum number of clock cycles necessary to clock in the data. The devices require 11 clock cycles from the microprocessor to clock out the 10 data bits with no trailing zeros or 13 clock cycles from the microprocessor to clock out the 10 data bits and two sub-bits with no trailing zeros (see Figure 36).

Note: The maximum clock frequency to ensure compatibility with QSPI is 2.097MHz.

Figure 36. QSPI Serial Interface Timing (CPOL = CPHA = 0)

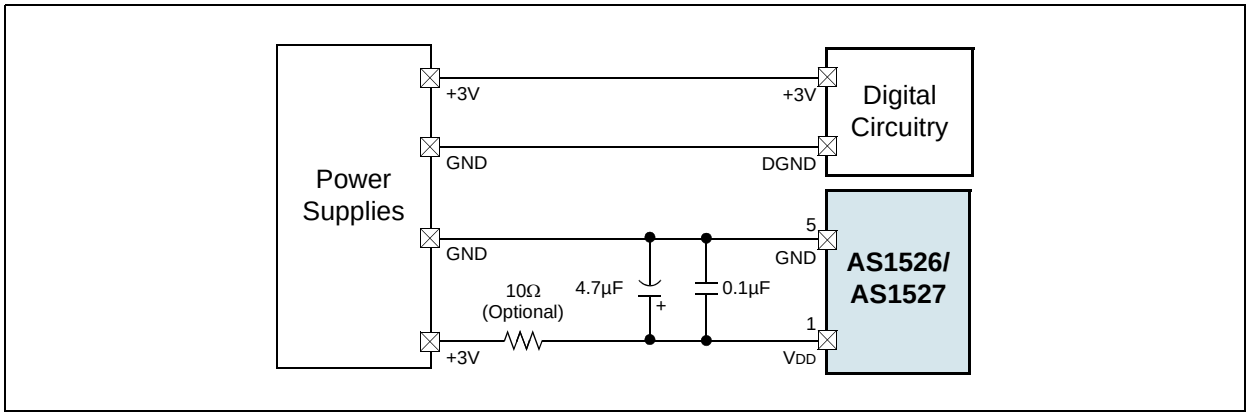


Layout Considerations

The AS1526/AS1527 require proper layout and design procedures for optimum performance.

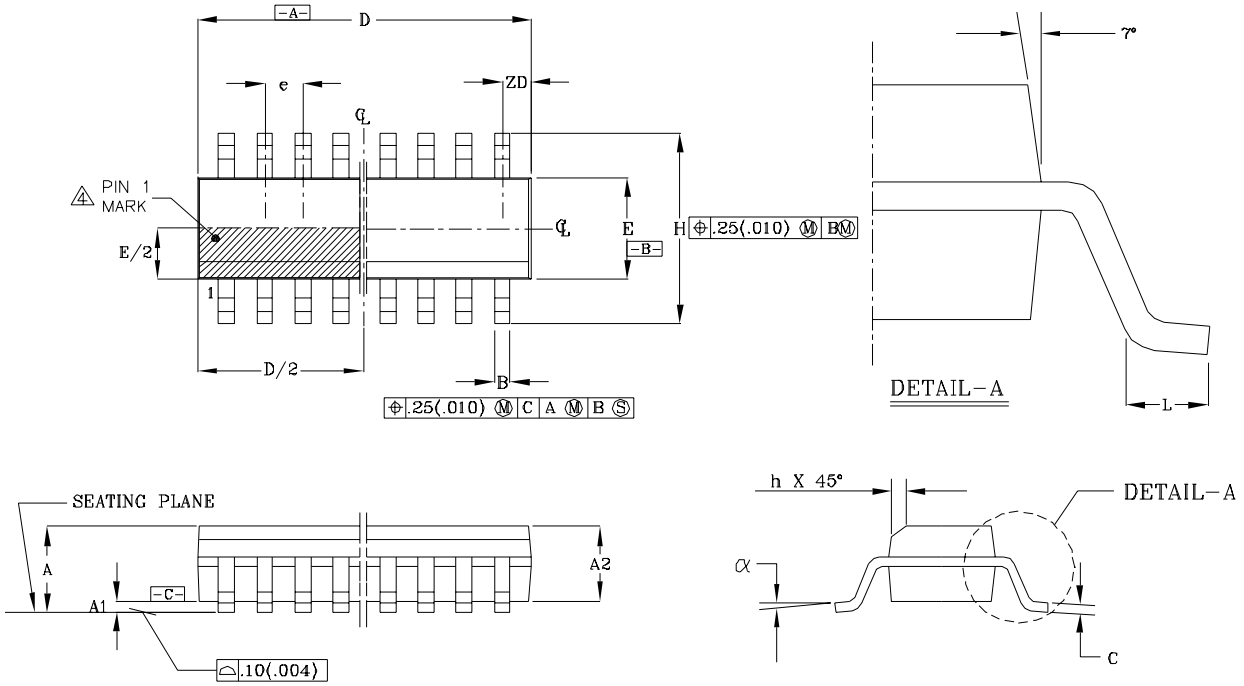
- Use printed circuit boards; wirewrap boards should not be used.
- Separate analog and digital traces from each other. Analog and digital traces should not run parallel to each other (especially clock traces).
- Digital traces should not run beneath the AS1526/AS1527.
- Use a single-point analog ground at GND, separate from the digital ground (see Figure 37). Connect all other analog grounds and DGND to this star ground point for further noise reduction. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.
- High-frequency noise in the V_{DD} power supply may affect the AS1526/AS1527 high-speed comparator. Bypass this supply to the single-point analog ground with 0.1µF and 4.7µF bypass capacitors (see Figure 37). The bypass capacitors should be placed as close to the device as possible for optimum power supply noise-rejection. If the power supply is very noisy, a 10Ω resistor can be connected as a low-pass filter to attenuate supply noise.

Figure 37. Recommended Ground Design



Package Drawings and Markings

Figure 38. 8-pin SOIC-150 Package



Notes:

1. Lead coplanarity should be 0 to 0.10mm (.004") max.
2. Package surface finishing:
   (2.1) Top: matte (charmilles #18-30).
   (2.2) All sides: matte (charmilles #18-30).
   (2.3) Bottom: smooth or matte (charmilles #18-30).
3. All dimensions exclusive of mold flash, and end flash from the package body shall not exceed 0.24mm (0.10") per side (D).
4. Details of pin #1 identifier are optional but must be located within the zone indicated.

Symbol	Min	Max
A1	0.10	0.25
B	0.36	0.46
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27BSC	
H	5.80	6.20
h	0.25	0.50
L	.041	1.27
A	1.52	1.72
	0º	8º
ZD	0.53REF	
A2	1.37	1.57

10 Ordering Information

The devices are available as the standard products shown in Table 5.

Table 5. Ordering Information

Type	Description	Delivery Form	Package
AS1526-BSOU	Single-Supply, Low-Power, 73ksps A/D Converter with Internal +2.5V Reference	Tubes	8-pin SOIC-150
AS1526-BSOT	Single-Supply, Low-Power, 73ksps A/D Converter with Internal +2.5V Reference	Tape and Reel	8-pin SOIC-150
AS1527-BSOU	Single-Supply, Low-Power, 73ksps A/D Converter	Tubes	8-pin SOIC-150
AS1527-BSOT	Single-Supply, Low-Power, 73ksps A/D Converter	Tape and Reel	8-pin SOIC-150

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Contact Information

Headquarters
austriamicrosystems AG
A-8141 Schloss Premstaetten, Austria

Tel: +43 (0) 3136 500 0
Fax: +43 (0) 3136 525 01

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- Alternative Solution
- Excess Inventory Management