



# THE DATASHEET OF AM3505AZERA



## AM3517, AM3505 Sitara™ Processors

### 1 Device Summary

#### 1.1 Features

- AM3517/05 Sitara Processor:
  - MPU Subsystem
    - 600-MHz Sitara ARM Cortex®-A8 Core
    - NEON™ SIMD Coprocessor and Vector Floating-Point (FP) Coprocessor
  - Memory Interfaces:
    - 166-MHz 16- and 32-Bit mDDR/DDR2 Interface with 1GB of Total Addressable Space
    - Up to 83 MHz General-Purpose Memory Interface Supporting 16-Bit-Wide Multiplexed Address/Data Bus
    - 64KB of SRAM
    - 3 Removable Media Interfaces [MMC/SD/SDIO]
  - IO Voltage:
    - mDDR/DDR2 IOs: 1.8V
    - Other IOs: 1.8V and 3.3V
  - Core Voltage: 1.2V
  - Commercial and Extended Temperature Grade (operating restrictions apply)
  - 16-Bit Video Input Port Capable of Capturing HD Video
  - HD Resolution Display Subsystem
  - Serial Communication
    - High-End CAN Controller
    - 10/100 Mbit Ethernet MAC
    - USB OTG Subsystem with Standard DP/DM Interface [HS/FS/LS]
    - Multiport USB Host Subsystem [HS/FS/LS]
      - 12-Pin ULPI or 6-, 4-, or 3-Pin Serial Interface
    - Four Master and Slave Multichannel Serial Port Interface (McSPI) Ports
    - Five Multichannel Buffered Serial Ports (McBSPs)
      - 512-Byte Transmit and Receive Buffer (McBSP1/3/4/5)
      - 5-KB Transmit and Receive Buffer (McBSP2)
      - SIDETONE Core Support (McBSP2 and McBSP3 Only) For Filter, Gain, and Mix Operations
      - 128-Channel Transmit and Receive Mode
      - Direct Interface to I2S and PCM Device and TDM Buses
    - HDQ/1-Wire Interface
  - 4 UARTs (One with Infrared Data Association [IrDA] and Consumer Infrared [CIR] Modes)
  - 3 Master and Slave High-Speed Inter-Integrated Circuit (I<sup>2</sup>C) Controllers
  - Twelve 32-bit General-Purpose Timers
  - One 32-bit Watchdog Timer
  - One 32-bit 32-kHz Sync Timer
  - Up to 186 General-Purpose I/O (GPIO) Pins
- Display Subsystem
  - Parallel Digital Output
  - Up to 24-Bit RGB
  - Supports Up to 2 LCD Panels
  - Support for Remote Frame Buffer Interface (RFB) LCD Panels
  - Two 10-Bit Digital-to-Analog Converters (DACs) Supporting
    - Composite NTSC/PAL Video
    - Luma/Chroma Separate Video (S-Video)
  - Rotation of 90, 180, and 270 Degrees
  - Resize Images From 1/4x to 8x
  - Color Space Converter
  - 8-Bit Alpha Blending
- Video Processing Front End (VPFE) 16-Bit Video Input Port
  - RAW Data Interface
  - 75-MHz Maximum Pixel Clock
  - Supports REC656/CCIR656 Standard
  - Supports YCbCr422 Format (8-Bit or 16-Bit with Discrete Horizontal and Vertical Sync Signals)
  - Generates Optical Black Clamping Signals
  - Built-in Digital Clamping and Black Level Compensation
  - 10-Bit to 8-Bit A-law Compression Hardware
  - Supports up to 16K Pixels (Image Size) in Horizontal and Vertical Directions
- System Direct Memory Access (sDMA) Controller (32 Logical Channels with Configurable Priority)
- Comprehensive Power, Reset, and Clock Management
- ARM Cortex-A8 Memory Architecture
  - ARMv7 Architecture
  - In-Order, Dual-Issue, Superscalar Microprocessor Core
  - ARM NEON Multimedia Architecture
  - Over 2x Performance of ARMv6 SIMD



- Supports Both Integer and Floating-Point SIMD
- Jazelle® RCT Execution Environment Architecture
- Dynamic Branch Prediction with Branch Target Address Cache, Global History Buffer and 8-Entry Return Stack
- Embedded Trace Macrocell [ETM] Support for Noninvasive Debug
- 16KB of Instruction Cache (4-Way Set-Associative)
- 16KB of Data Cache (4-Way Set-Associative)
- 256KB of L2 Cache
- PowerVR SGX™ Graphics Accelerator (AM3517 Only)
  - Tile-Based Architecture Delivering up to 10 MPoly/sec
  - Universal Scalable Shader Engine: Multi-threaded Engine Incorporating Pixel and Vertex Shader Functionality
  - Industry Standard API Support: OpenGL ES 1.1 and 2.0, OpenVG1.0
  - Fine-Grained Task Switching, Load Balancing, and Power Management
  - Programmable, High-Quality Image Anti-Aliasing
- Endianess
  - ARM Instructions – Little Endian
  - ARM Data – Configurable
- SDRC Memory Controller
  - 16- and 32-Bit Memory Controller with 1GB of Total Address Space
  - Double Data Rate (DDR2) SDRAM, Mobile Double Data Rate (mDDR)SDRAM
  - SDRAM Memory Scheduler (SMS) and Rotation Engine
- General Purpose Memory Controller (GPMC)
  - 16-Bit-Wide Multiplexed Address/Data Bus
  - Up to 8 Chip-Select Pins with 128MB of Address Space per Chip-Select Pin
  - Glueless Interface to NOR Flash, NAND Flash (with ECC Hamming Code Calculation), SRAM and Pseudo-SRAM
  - Flexible Asynchronous Protocol Control for Interface to Custom Logic (FPGA, CPLD, ASICs, and so forth)
  - Nonmultiplexed Address/Data Mode (Limited 2-KB Address Space)
- Test Interfaces
  - IEEE-1149.1 (JTAG) Boundary-Scan Compatible
  - Embedded Trace Macro Interface (ETM)
- 65-nm CMOS Technology
- Packages:
  - 491-Pin BGA (17 x 17, 0.65-mm Pitch) [ZCN Suffix]
  - 484-Pin PBGA (23 x 23, 1-mm Pitch) [ZER Suffix]

## 1.2 Applications

- Single-Board Computers
- Industrial and Home Automation
- Digital Signage
- Point of Service
- Portable Media Player
- Portable Industrial
- Transportation
- Navigation
- Smart White Goods
- Digital TV
- Digital Video Camera
- Gaming

### 1.3 Description

AM3517/05 is a high-performance ARM Cortex-A8 microprocessor with speeds up to 600 MHz. The device offers 3D graphics acceleration while also supporting numerous peripherals, including DDR2, CAN, EMAC, and USB OTG PHY that are well suited for industrial applications.

The processor can support other applications, including:

- Single-board computers
- Home and industrial automation
- Human machine Interface

The device supports high-level operating systems (OSs), such as:

- Linux®
- Windows® CE
- Android™

The following subsystems are part of the device:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8 microprocessor
- PowerVR SGX graphics accelerator (AM3517 device only) subsystem for 3D graphics acceleration to support display and gaming effects
- Display subsystem with several features for multiple concurrent image manipulation, and a programmable interface supporting a wide variety of displays. The display subsystem also supports NTSC/PAL video out.
- High-performance interconnects provide high-bandwidth data transfers for multiple initiators to the internal and external memory controllers and to on-chip peripherals. The device also offers a comprehensive clock-management scheme.

AM3517/05 devices are available in a 491-pin BGA package and a 484-pin PBGA package.

This AM3517/05 data manual presents the electrical and mechanical specifications for the AM3517/05 Sitara processor.

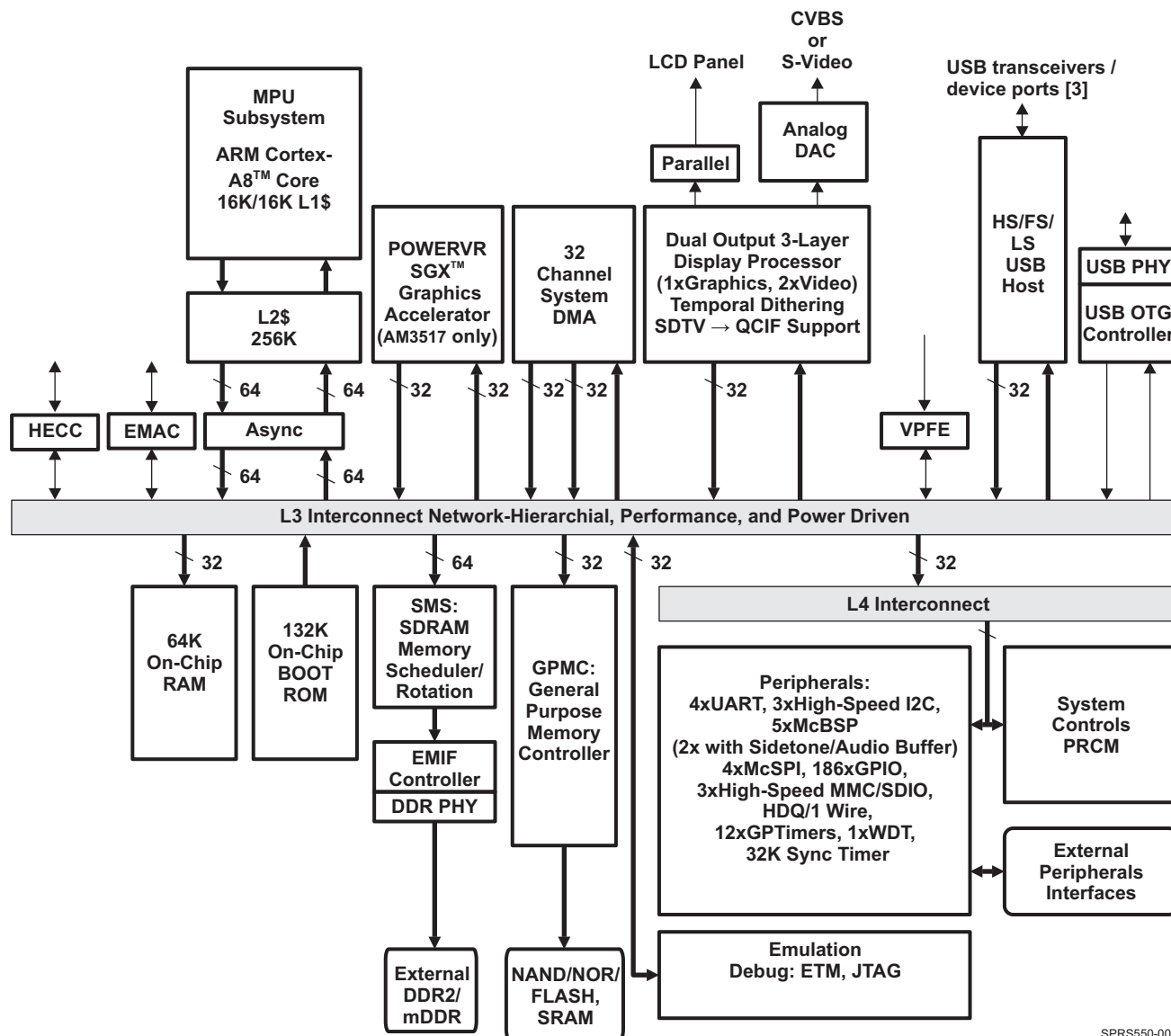
**Device Information<sup>(1)</sup>**

| PART NUMBER | PACKAGE     | BODY SIZE           |
|-------------|-------------|---------------------|
| AM3505      | NFBGA (491) | 17.10 mm x 17.10 mm |
| AM3505      | BGA (484)   | 23.20 mm x 23.20 mm |
| AM3517      | NFBGA (491) | 17.10 mm x 17.10 mm |
| AM3517      | BGA (484)   | 23.20 mm x 23.20 mm |

(1) For more information, see [Section 8, Mechanical Packaging and Orderable Information](#).

## 1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram of the AM3517/05 Sitara ARM microprocessor.



SPRS550-006

Figure 1-1. AM3517/05 Functional Block Diagram

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## 2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

This data manual revision history table highlights the technical and major format changes made from Revision E to Revision F.

| SEE                           | ADDITIONS/MODIFICATIONS/DELETIONS                                                                                                                                                            |
|-------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
|                               | Description:                                                                                                                                                                                 |
| <a href="#">Section 3</a>     | Added Device Information table                                                                                                                                                               |
|                               | Device Comparison:                                                                                                                                                                           |
|                               | Added <a href="#">Section 3</a> , Device Comparison                                                                                                                                          |
|                               | Added <a href="#">Section 3.1</a> , Device Features Comparison                                                                                                                               |
|                               | Moved <a href="#">Section 3.2</a> , ZCN and ZER Package Differences to <a href="#">Section 3</a> , Device Comparison                                                                         |
| <a href="#">Section 4</a>     | Terminal Configuration and Functions:                                                                                                                                                        |
|                               | Changed title from Terminal Description to Terminal Configuration and Functions                                                                                                              |
| <a href="#">Section 4.4.9</a> | Signal Description:                                                                                                                                                                          |
|                               | Added pin N22 to VDD5 row of the ZCN package in <a href="#">Table 4-27</a> , Power Supplies Description.                                                                                     |
| <a href="#">Section 5</a>     | Specifications:                                                                                                                                                                              |
|                               | Changed title from Electrical Characteristics to Specifications                                                                                                                              |
|                               | Extracted handling ratings from <a href="#">Table 5-1</a> , Absolute Maximum Ratings Over Operating Junction Temperature Range and added <a href="#">Table 5-2</a> , Handling Ratings        |
|                               | Moved <a href="#">Section 5.9</a> , Clock Specifications to <a href="#">Section 5</a> , Specifications                                                                                       |
|                               | Moved <a href="#">Section 5.10</a> , Video DAC Specifications to <a href="#">Section 5</a> , Specifications                                                                                  |
| <a href="#">Section 5.4</a>   | Power Consumption Summary:                                                                                                                                                                   |
|                               | Moved <a href="#">Table 5-4</a> , Estimated Power Consumption at Ball Level to its own section.                                                                                              |
| <a href="#">Section 5.5</a>   | Electrical Characteristics:                                                                                                                                                                  |
|                               | Changed title from DC Electrical Characteristics to Electrical Characteristics                                                                                                               |
| <a href="#">Section 5.6</a>   | Thermal Characteristics:                                                                                                                                                                     |
|                               | Changed title from Package Thermal Resistance to Thermal Characteristics                                                                                                                     |
|                               | Moved section from Package Characteristics to separate section                                                                                                                               |
|                               | Added $\theta_{JA}$ , $\theta_{JC}$ , $\theta_{JB}$ values to tables ( <a href="#">Table 5-6</a> and <a href="#">Table 5-7</a> ) for ZCN and ZER package thermal resistance characteristics. |
| <a href="#">Section 7</a>     | Device and Documentation Support                                                                                                                                                             |
|                               | Changed title Package Characteristics to Device and Documentation Support                                                                                                                    |
|                               | Changed title Device and Development Support - Support Tool Nomenclature to <a href="#">Section 7.1.2</a> , Device Nomenclature                                                              |
|                               | Added <a href="#">Section 7.1.1</a> , Development Support                                                                                                                                    |
|                               | Changed title Related Documentation From Texas Instruments to <a href="#">Section 7.2.1</a> , Related Documentation                                                                          |
|                               | Moved section Related Documentation to <a href="#">Section 7.2.1</a> , Related Documentation                                                                                                 |
| <a href="#">Section 8</a>     | Mechanical Packaging and Orderable Information                                                                                                                                               |
|                               | Changed title Mechanical Data to Mechanical Packaging and Orderable Information                                                                                                              |

## 3 Device Comparison

### 3.1 Device Features Comparison

**Table 3-1. Device Features Comparison**

| FEATURE                          | AM3505 | AM3517 |
|----------------------------------|--------|--------|
| PowerVR SGX Graphics Accelerator | No     | Yes    |

### 3.2 ZCN and ZER Package Differences

[Table 3-2](#) lists the ZER and ZCN package differences on the device.

**Table 3-2. ZCN and ZER Package Differences**

| FEATURE          | ZCN PACKAGE                                                                                          | ZER PACKAGE                                                                                          |
|------------------|------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|
| Pin Assignments  | For ZCN package pin assignments, see <a href="#">Section 4, Terminal Configuration and Functions</a> | For ZER package pin assignments, see <a href="#">Section 4, Terminal Configuration and Functions</a> |
| Video Interfaces | TV Out available                                                                                     | TV Out not available                                                                                 |

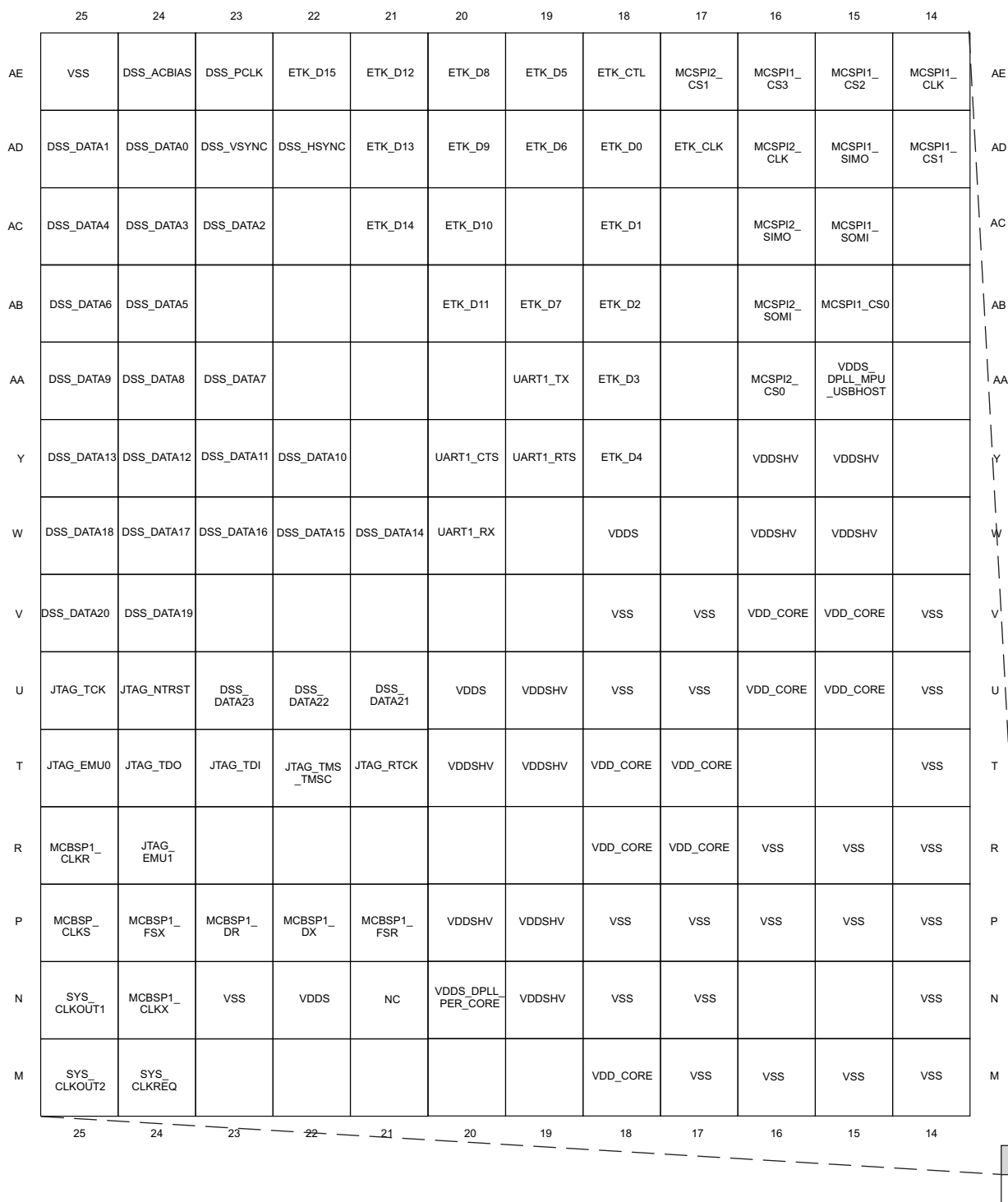
## 4 Terminal Configuration and Functions

### 4.1 Pin Assignments

#### 4.1.1 Pin Map (Top View)

The following illustrations show the top views of the 484-pin [ZER] and 491-pin [ZCN] package pin assignments in four quadrants (A, B, C, and D).

**Note:** A pin with an NC designator indicates No Connection. For proper device operation, these pins must be left unconnected.


**Figure 4-1. ZCN Pin Map [Quadrant A]**

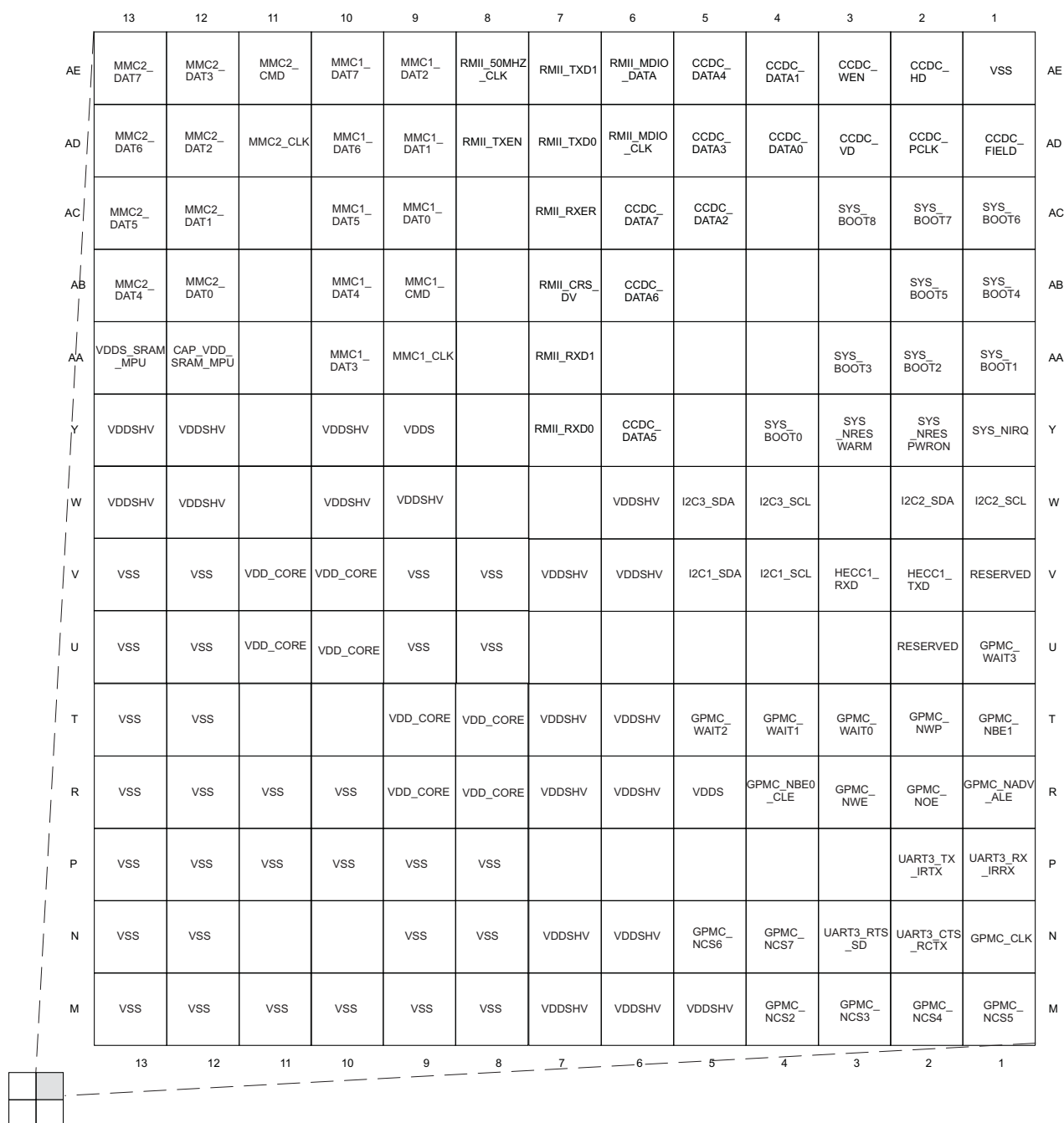
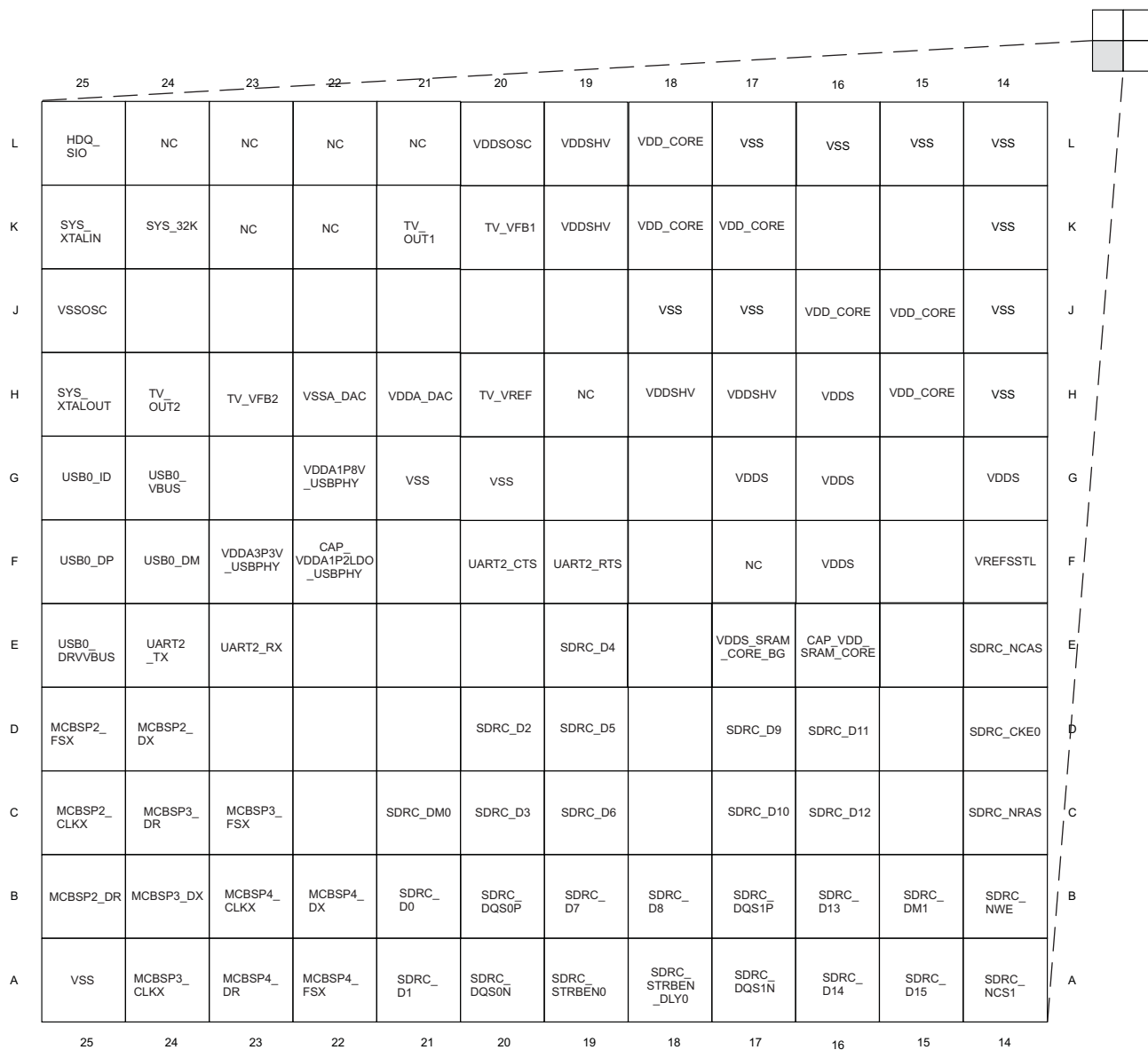


Figure 4-2. ZCN Pin Map [Quadrant B]


**Figure 4-3. ZCN Pin Map [Quadrant C]**

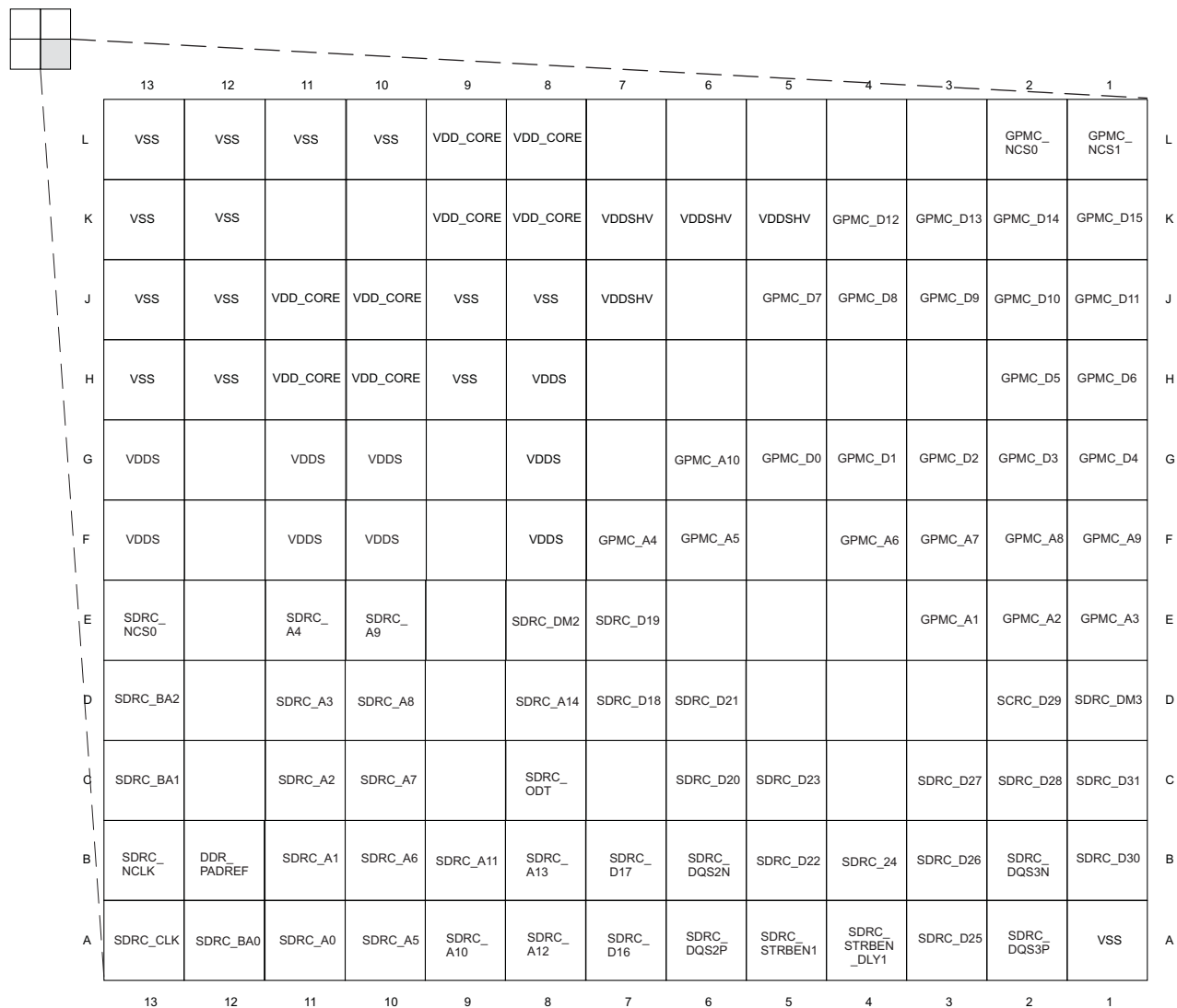


Figure 4-4. ZCN Pin Map [Quadrant D]

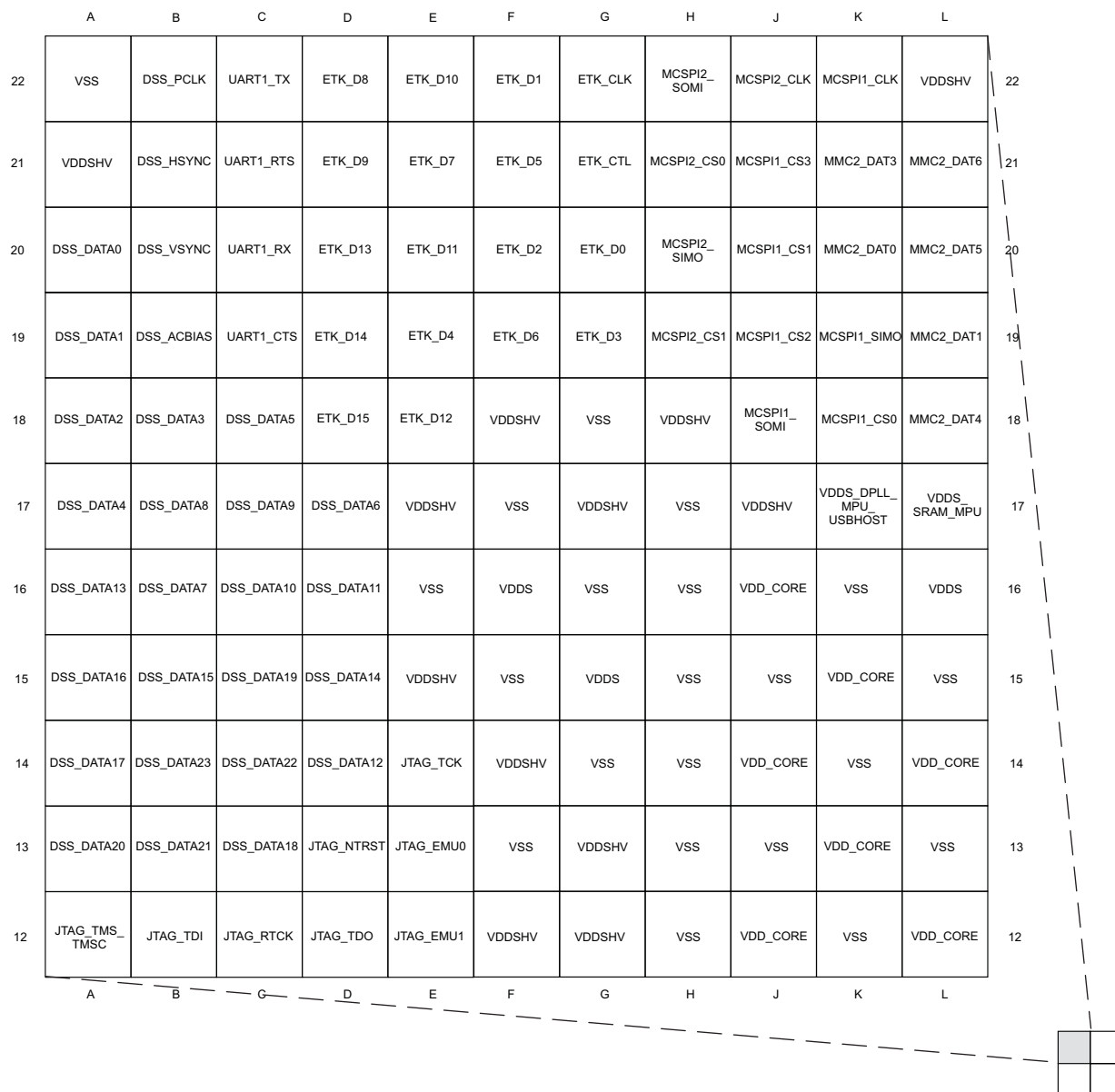


**Figure 4-5. ZER Pin Map [Quadrant A]**

|    | M                | N         | P         | R              | T           | U              | V          | W              | Y             | AA             | AB        |    |
|----|------------------|-----------|-----------|----------------|-------------|----------------|------------|----------------|---------------|----------------|-----------|----|
| 22 | VSS              | MMC1_DAT4 | MMC1_CLK  | RMII_RXER      | RMII_TXD0   | RMII_MDIO_CLK  | CCDC_DATA4 | CCDC_DATA0     | CCDC_VD       | VDDSHV         | VSS       | 22 |
| 21 | MMC2_CLK         | MMC1_CMD  | MMC1_DAT0 | RMII_50MHZ_CLK | RMII_CRS_DV | RMII_MDIO_DATA | CCDC_DATA2 | CCDC_WEN       | CCDC_HD       | CCDC_FIELD     | CCDC_PCLK | 21 |
| 20 | MMC2_CMD         | MMC1_DAT1 | MMC1_DAT3 | RMII_TXD1      | RMII_RXD1   | CCDC_DATA5     | CCDC_DATA6 | CCDC_DATA1     | SYS_BOOT8     | SYS_BOOT7      | SYS_BOOT1 | 20 |
| 19 | MMC2_DAT7        | MMC1_DAT5 | MMC1_DAT2 | RMII_TXEN      | RMII_RXD0   | CCDC_DATA7     | CCDC_DATA3 | SYS_BOOT6      | SYS_BOOT5     | SYS_BOOT3      | SYS_BOOT0 | 19 |
| 18 | MMC2_DAT2        | MMC1_DAT6 | MMC1_DAT7 | VDDSHV         | VSS         | VDDSHV         | SYS_BOOT4  | SYS_BOOT2      | SYS_NRE_SWARM | SYS_NRES_PWRON | SYS_NIRQ  | 18 |
| 17 | CAP_VDD_SRAM_MPU | VSS       | VDDSHV    | VSS            | VDDSHV      | VSS            | VDDSHV     | I2C3_SDA       | I2C2_SCL      | I2C1_SCL       | I2C1_SDA  | 17 |
| 16 | VSS              | VDDSHV    | VSS       | VDDSHV         | VSS         | VDDSHV         | RESERVED   | I2C3_SCL       | I2C2_SDA      | GPMC_WAIT1     | HECC1_RXD | 16 |
| 15 | VDD_CORE         | VSS       | VDD_CORE  | VSS            | VDD         | VSS            | RESERVED   | UART3_CTS_RCTX | GPMC_NBE1     | GPMC_NWE       | HECC1_TXD | 15 |
| 14 | VSS              | VDD_CORE  | VSS       | VDD_CORE       | VSS         | VDDSHV         | GPMC_WAIT3 | GPMC_NWP       | GPMC_WAIT2    | GPMC_NADV_ALE  | GPMC_NOE  | 14 |
| 13 | VDD_CORE         | VSS       | VDD_CORE  | VSS            | VDDSHV      | VSS            | GPMC_WAIT0 | UART3_RTS_SD   | UART3_TX_IRTX | UART3_RX_IRRX  | GPMC_CLK  | 13 |
| 12 | VSS              | VDD_CORE  | VSS       | VDD_CORE       | VSS         | VDDSHV         | GPMC_NCS3  | GPMC_NCS5      | GPMC_NCS2     | GPMC_NCS6      | VSS       | 12 |
|    | M                | N         | P         | R              | T           | U              | V          | W              | Y             | AA             | AB        |    |

Figure 4-6. ZER Pin Map [Quadrant B]

|    | A            | B           | C           | D               | E                     | F                  | G        | H          | J                 | K                 | L         |    |
|----|--------------|-------------|-------------|-----------------|-----------------------|--------------------|----------|------------|-------------------|-------------------|-----------|----|
| 11 | VSS          | MCBSP1_CLKR | MCBSP1_FSX  | MCBSP1_FSR      | MCBSP_CLKS            | VDDS_DPLL_PER_CORE | VSS      | VSS        | VSS               | VDD_CORE          | VSS       | 11 |
| 10 | SYS_XTALIN   | VSSOSC      | MCBSP1_DX   | NC              | SYS_CLKOUT2           | NC                 | VDDSHV   | VSS        | VDD_CORE          | VSS               | VDD_CORE  | 10 |
| 9  | SYS_XTALOUT  | HDQ_SIO     | MCBSP1_DR   | NC              | SYS_CLKOUT1           | NC                 | VDDSHV   | VSS        | VSS               | VDD_CORE          | VSS       | 9  |
| 8  | SYS_32K      | SYS_CLKREQ  | MCBSP1_CLKX | NC              | NC                    | NC                 | VDDSHV   | VSS        | VDD_CORE          | VSS               | VDD_CORE  | 8  |
| 7  | USB0_DRVVBUS | USB0_ID     | USB0_VBUS   | VDDA1P8V_USBPHY | CAP_VDDA1P2LDO_USBPHY | VDDA3P3V_USBPHY    | VSS      | VSS        | NC                | VDDS              | VSS       | 7  |
| 6  | USB0_DP      | USB0_DM     | UART2_RX    | UART2_TX        | VSS                   | VSS                | NC       | VSS        | VDDS_SRAM_CORE_BG | CAP_VDD_SRAM_CORE | VDDS      | 6  |
| 5  | UART2_CTS    | UART2_RTS   | MCBSP2_DR   | MCBSP2_CLKX     | MCBSP2_FSX            | VDDS               | VSS      | VDDS       | SDRC_BA2          | SDRC_BA1          | VREFSSTL  | 5  |
| 4  | MCBSP3_FSX   | MCBSP3_DR   | MCBSP3_DX   | MCBSP3_CLKX     | MCBSP2_DX             | SDRC_DM0           | SDRC_D11 | SDRC_D12   | SDRC_NCS0         | SDRC_NCS1         | SDRC_BA0  | 4  |
| 3  | MCBSP4_CLKX  | MCBSP4_DR   | SDRC_D2     | SDRC_D1         | SDRC_D0               | SDRC_D4            | SDRC_D9  | SDRC_D10   | SDRC_D14          | SDRC_CKE0         | SDRC_NCAS | 3  |
| 2  | MCBSP4_DX    | MCBSP4_FSX  | SDRC_D3     | SDRC_D5         | SDRC_DQS0P            | SDRC_STRBEN0       | SDRC_D8  | SDRC_DQS1P | SDRC_DM1          | SDRC_NWE          | SDRC_NCLK | 2  |
| 1  | VSS          | VDDSHV      | SDRC_D6     | SDRC_D7         | SDRC_DQS0N            | SDRC_STRBEN_DLY0   | SDRC_D13 | SDRC_DQS1N | SDRC_D15          | SDRC_NRAS         | SDRC_CLK  | 1  |
|    | A            | B           | C           | D               | E                     | F                  | G        | H          | J                 | K                 | L         |    |

**Figure 4-7. ZER Pin Map [Quadrant C]**

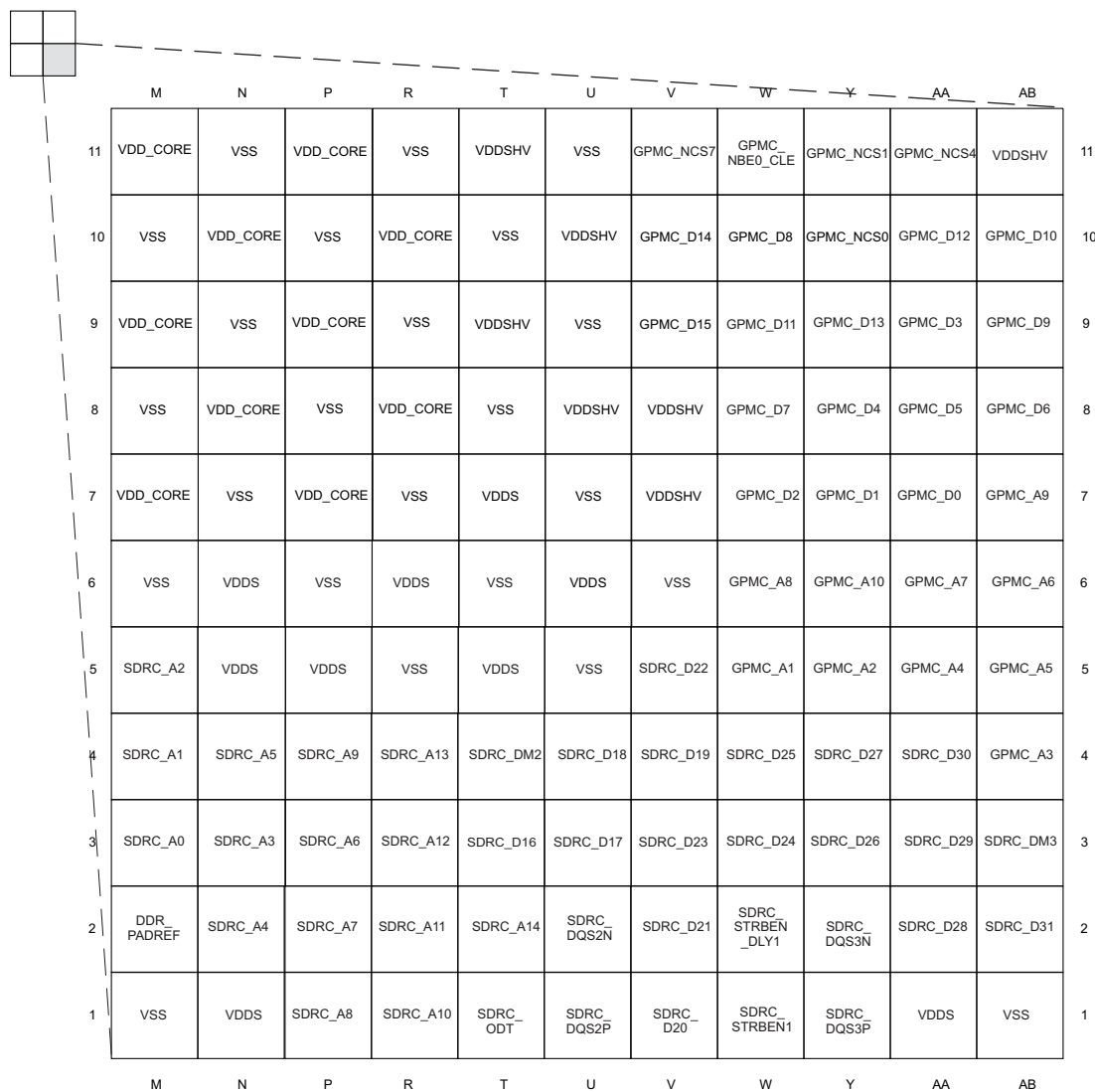


Figure 4-8. ZER Pin Map [Quadrant D]

## 4.2 Ball Characteristics

Table 4-1 and Table 4-2 describe the terminal characteristics and the signals multiplexed on each pin for the ZCN/ZER packages. The following list describes the table column headers.

1. **BALL LOCATION:** Ball number(s) on the bottom side associated with each signal(s) on the bottom.
2. **PIN NAME:** Names of signals multiplexed on each ball (also notice that the name of the pin is the signal name in mode 0).  
**Note:** The *Ball Characteristics* table does not take into account subsystem pin multiplexing options. Subsystem pin multiplexing options are described in Section 4.4, *Signal Description*.
3. **MODE:** Multiplexing mode number.
  - (a) Mode 0 is the primary mode; this means that when mode 0 is set, the function mapped on the pin corresponds to the name of the pin. There is always a function mapped on the primary mode. Notice that primary mode is not necessarily the default mode.  
**Note:** The default mode is the mode which is automatically configured on release of the internal GLOBAL\_PWRON reset; also see the RESET REL. MODE column.
  - (b) Modes 1 to 7 are possible modes for alternate functions. On each pin, some modes are effectively used for alternate functions, while some modes are not used and do not correspond to a functional configuration.
4. **TYPE:** Signal direction
  - I = Input
  - O = Output
  - I/O = Input/Output
  - D = Open drain
  - DS = Differential
  - A = Analog**Note:** In the safe\_mode, the buffer is configured in high-impedance.
5. **BALL RESET STATE:** The state of the terminal at reset (power up).
  - 0: The buffer drives  $V_{OL}$  (pulldown/pullup resistor not activated)
  - 0(PD): The buffer drives  $V_{OL}$  with an active pulldown resistor.
  - 1: The buffer drives  $V_{OH}$  (pulldown/pullup resistor not activated)
  - 1(PU): The buffer drives  $V_{OH}$  with an active pullup resistor.
  - Z: High-impedance
  - L: High-impedance with an active pulldown resistor
  - H: High-impedance with an active pullup resistor
6. **BALL RESET REL. STATE:** The state of the terminal at reset release.
  - 0: The buffer drives  $V_{OL}$  (pulldown/pullup resistor not activated)
  - 0(PD): The buffer drives  $V_{OL}$  with an active pulldown resistor.
  - 1: The buffer drives  $V_{OH}$  (pulldown/pullup resistor not activated)
  - 1(PU): The buffer drives  $V_{OH}$  with an active pullup resistor.
  - Z: High-impedance
  - L: High-impedance with an active pulldown resistor
  - H : High-impedance with an active pullup resistor
7. **RESET REL. MODE:** This mode is automatically configured on release of the internal GLOBAL\_PWRON reset.
8. **POWER:** The voltage supply that powers the terminal's I/O buffers.
9. **VOLTAGE:** Supply voltage for associated pin.
10. **HYS:** Indicates if the input buffer is with hysteresis.
11. **LOAD:** Load capacitance of the associated output buffer.
12. **PULL U/D - TYPE:** Denotes the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.

### 13. IO CELL: IO cell information.

**Note:** Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration.

**Table 4-1. Ball Characteristics (ZCN Pkg.)**

| BALL LOCATION [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|--------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| B21               | sdrc_d0      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| A21               | sdrc_d1      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| D20               | sdrc_d2      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C20               | sdrc_d3      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| E19               | sdrc_d4      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| D19               | sdrc_d5      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C19               | sdrc_d6      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| B19               | sdrc_d7      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| B18               | sdrc_d8      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| D17               | sdrc_d9      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C17               | sdrc_d10     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| D16               | sdrc_d11     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C16               | sdrc_d12     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| B16               | sdrc_d13     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| A16               | sdrc_d14     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| A15               | sdrc_d15     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| A7                | sdrc_d16     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| B7                | sdrc_d17     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| D7                | sdrc_d18     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| E7                | sdrc_d19     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C6                | sdrc_d20     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| D6                | sdrc_d21     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| B5                | sdrc_d22     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C5                | sdrc_d23     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| B4                | sdrc_d24     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| A3                | sdrc_d25     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| B3                | sdrc_d26     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C3                | sdrc_d27     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C2                | sdrc_d28     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| D2                | sdrc_d29     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| B1                | sdrc_d30     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C1                | sdrc_d31     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| A12               | sdrc_ba0     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| C13               | sdrc_ba1     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| D13               | sdrc_ba2     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| A11               | sdrc_a0      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| B11               | sdrc_a1      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| C11               | sdrc_a2      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| D11               | sdrc_a3      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| E11               | sdrc_a4      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| A10               | sdrc_a5      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| B10               | sdrc_a6      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| C10               | sdrc_a7      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| D10               | sdrc_a8      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| E10               | sdrc_a9      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| A9                | sdrc_a10     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| B9                | sdrc_a11     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| A8                | sdrc_a12     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| B8                | sdrc_a13     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]     | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|------------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| D8                | sdrc_a14         | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| E13               | sdrc_ncs0        | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| A14               | sdrc_ncs1        | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| A13               | sdrc_clk         | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
| B13               | sdrc_nclk        | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| D14               | sdrc_cke0        | 0        | O        | L                    | PD                        | 7                   | VDD5      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
|                   | sdrc_cke0_safe   | 7        |          | L                    |                           |                     |           |             |          |                |                    |              |
| C14               | sdrc_nras        | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| E14               | sdrc_ncas        | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| B14               | sdrc_nwe         | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| C21               | sdrc_dm0         | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| B15               | sdrc_dm1         | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| E8                | sdrc_dm2         | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| D1                | sdrc_dm3         | 0        | O        | L                    | Z                         | 0                   | VDD5      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| B20               | sdrc_dqs0p       | 0        | IO       | L                    | Z                         | 0                   | VDD5      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
| B17               | sdrc_dqs1p       | 0        | IO       | L                    | Z                         | 0                   | VDD5      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
| A6                | sdrc_dqs2p       | 0        | IO       | L                    | Z                         | 0                   | VDD5      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
| A2                | sdrc_dqs3p       | 0        | IO       | L                    | Z                         | 0                   | VDD5      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
| A20               | sdrc_dqs0n       | 0        | IO       | L                    | Z                         | 0                   | VDD5      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| A17               | sdrc_dqs1n       | 0        | IO       | L                    | Z                         | 0                   | VDD5      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| B6                | sdrc_dqs2n       | 0        | IO       | L                    | Z                         | 0                   | VDD5      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| B2                | sdrc_dqs3n       | 0        | IO       | L                    | Z                         | 0                   | VDD5      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| C8                | sdrc_odt         | 0        |          | L                    | Z                         | 0                   | VDD5      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| A19               | sdrc_strben0     | 0        |          | L                    | Z                         | 0                   | VDD5      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| A18               | sdrc_strben_dly0 | 0        |          | L                    | Z                         | 0                   | VDD5      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| A5                | sdrc_strben1     | 0        |          | L                    | Z                         | 0                   | VDD5      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| A4                | sdrc_strben_dly1 | 0        |          | L                    | Z                         | 0                   | VDD5      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| B12               | ddr_padref       | 0        | A        |                      |                           |                     | VDD5      | 1.8V        |          |                |                    |              |
| E3                | gpmc_a1          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_34          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode        | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| E2                | gpmc_a2          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_35          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode        | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| E1                | gpmc_a3          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_36          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode        | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| F7                | gpmc_a4          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_37          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode        | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| F6                | gpmc_a5          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_38          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode        | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| F4                | gpmc_a6          | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_39          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode        | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| F3                | gpmc_a7          | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_40          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode        | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| F2                | gpmc_a8          | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_41          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode        | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| F1                | gpmc_a9          | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |

Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)

| BALL LOCATION [1] | PIN NAME [2]  | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|---------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
|                   | sys_ndmareq2  | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_42       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| G6                | gpmc_a10      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | sys_ndmareq3  | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_43       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| G5                | gpmc_d0       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   |          | 30             | PU/ PD             | LVC MOS      |
| G4                | gpmc_d1       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| G3                | gpmc_d2       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| G2                | gpmc_d3       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| G1                | gpmc_d4       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| H2                | gpmc_d5       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| H1                | gpmc_d6       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| J5                | gpmc_d7       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| J4                | gpmc_d8       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_44       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| J3                | gpmc_d9       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_45       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| J2                | gpmc_d10      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_46       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| J1                | gpmc_d11      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_47       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| K4                | gpmc_d12      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_48       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| K3                | gpmc_d13      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_49       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| K2                | gpmc_d14      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_50       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| K1                | gpmc_d15      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_51       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| L2                | gpmc_ncs0     | 0        | O        | H                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | NA                 | LVC MOS      |
| L1                | gpmc_ncs1     | 0        | O        | H                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_52       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| M4                | gpmc_ncs2     | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpt9_pwm_evt  | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_53       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| M3                | gpmc_ncs3     | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | sys_ndmareq0  | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt10_pwm_evt | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_54       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| M2                | gpmc_ncs4     | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | sys_ndmareq1  | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt9_pwm_evt  | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_55       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]   | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| M1                | gpmc_ncs5      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_ndmareq2   | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt10_pwm_evt  | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_56        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| N5                | gpmc_ncs6      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_ndmareq3   | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt11_pwm_evt  | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_57        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| N4                | gpmc_ncs7      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpmc_io_dir    | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt8_pwm_evt   | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_58        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| N1                | gpmc_clk       | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_59        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| R1                | gpmc_nadv_ale  | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
| R2                | gpmc_noe       | 0        | O        | H                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
| R3                | gpmc_nwe       | 0        | O        | H                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
| R4                | gpmc_nbe0_cle  | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_60        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| T1                | gpmc_nbe1      | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_61        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| T2                | gpmc_nwp       | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_62        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| T3                | gpmc_wait0     | 0        | I        | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
| T4                | gpmc_wait1     | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart4_tx       | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_63        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| T5                | gpmc_wait2     | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart4_rx       | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_64        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| U1                | gpmc_wait3     | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_ndmareq1   | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart3_cts_rctx | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_65        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE23              | dss_pclk       | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_66        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg12       | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD22              | dss_hsync      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_67        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg13       | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |

Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)

| BALL LOCATION [1] | PIN NAME [2]  | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|---------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| AD23              | dss_vsync     | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_68       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE24              | dss_acbias    | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_69       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD24              | dss_data0     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart1_cts     | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_70       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD25              | dss_data1     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart1_rts     | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_71       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC23              | dss_data2     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_72       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC24              | dss_data3     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_73       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC25              | dss_data4     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart3_rx_irrx | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_74       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AB24              | dss_data5     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart3_tx_irtx | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_75       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AB25              | dss_data6     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart1_tx      | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_76       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg14      | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AA23              | dss_data7     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart1_rx      | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_77       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg15      | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AA24              | dss_data8     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_78       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg16      | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AA25              | dss_data9     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_79       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg17      | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| Y22               | dss_data10    | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_80       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| Y23               | dss_data11    | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_81       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| Y24               | dss_data12    | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_82       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode     | 7        |          |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|--------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| Y25               | dss_data13   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_83      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| W21               | dss_data14   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_84      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| W22               | dss_data15   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_85      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| W23               | dss_data16   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_86      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| W24               | dss_data17   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_87      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| W25               | dss_data18   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | mcspi3_clk   | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | dss_data4    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_88      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| V24               | dss_data19   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | mcspi3_simo  | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | dss_data3    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_89      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| V25               | dss_data20   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | mcspi3_somi  | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | dss_data2    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_90      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| U21               | dss_data21   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | mcspi3_cs0   | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | dss_data1    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_91      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| U22               | dss_data22   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | mcspi3_cs1   | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | dss_data0    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_92      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| U23               | dss_data23   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | dss_data5    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_93      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| H24               | tv_out2      | 0        | O        |                      |                           | 0                   | VDDA_DAC  | 1.8V        |          |                | NA                 | 10-bit DAC   |
| K21               | tv_out1      | 0        | O        |                      |                           | 0                   | VDDA_DAC  | 1.8V        |          |                | NA                 | 10-bit DAC   |
| K20               | tv_vfb1      | 0        | O        | Z                    | NA                        | 0                   | VDDA_DAC  | 1.8V        |          |                | NA                 | 10-bit DAC   |
| H23               | tv_vfb2      | 0        | O        | Z                    | NA                        | 0                   | VDDA_DAC  | 1.8V        |          |                | NA                 | 10-bit DAC   |
| H20               | tv_vref      | 0        | I        | Z                    | NA                        | 0                   | VDDA_DAC  | 1.8V        |          |                | NA                 | 10-bit DAC   |
| AD2               | ccdc_pclk    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | gpio_94      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg0      | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]   | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| AD1               | ccdc_field     | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | ccdc_data8     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_tx       | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | i2c3_scl       | 3        | IOD      |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_95        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg1        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE2               | ccdc_hd        | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | uart4_rts      | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_96        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD3               | ccdc_vd        | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | uart4_cts      | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_97        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg2        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE3               | ccdc_wen       | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/PD              | LVCMOS       |
|                   | ccdc_data9     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_rx       | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_98        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg3        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD4               | ccdc_data0     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/PD              | LVCMOS       |
|                   | i2c3_sda       | 3        | IOD      |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_99        | 4        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE4               | ccdc_data1     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/PD              | LVCMOS       |
|                   | gpio_100       | 4        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC5               | ccdc_data2     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | gpio_101       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg4        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD5               | ccdc_data3     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | gpio_102       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg5        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE5               | ccdc_data4     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | gpio_103       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg6        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| Y6                | ccdc_data5     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | gpio_104       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg7        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AB6               | ccdc_data6     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/PD              | LVCMOS       |
|                   | gpio_105       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC6               | ccdc_data7     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/PD              | LVCMOS       |
|                   | gpio_106       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE6               | rmii_mdio_data | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/PD              | LVCMOS       |
|                   | ccdc_data8     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_107       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]   | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD6               | rmii_mdio_clk  | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/PD              | LVCMOS       |
|                   | ccdc_data9     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_108       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| Y7                | rmii_rxd0      | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/ PD             | LVCMOS       |
|                   | ccdc_data10    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_109       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg8        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AA7               | rmii_rxd1      | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/ PD             | LVCMOS       |
|                   | ccdc_data11    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_110       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg9        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AB7               | rmii_crs_dv    | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/ PD             | LVCMOS       |
|                   | ccdc_data12    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_111       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC7               | rmii_rxer      | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/ PD             | LVCMOS       |
|                   | ccdc_data13    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_167       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg10       | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD7               | rmii_txd0      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/ PD             | LVCMOS       |
|                   | ccdc_data14    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_126       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg11       | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE7               | rmii_txd1      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/PD              | LVCMOS       |
|                   | ccdc_data15    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_112       | 4        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD8               | rmii_txen      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | NA       | 25             | PU/PD              | LVCMOS       |
|                   | gpio_113       | 4        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE8               | rmii_50mhz_clk | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | NA       | 25             | PU/ PD             | LVCMOS       |
|                   | gpio_114       | 4        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| D25               | mcbsp2_fsx     | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_116       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| C25               | mcbsp2_clkx    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_117       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| B25               | mcbsp2_dr      | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_118       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| D24               | mcbsp2_dx      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_119       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AA9               | mmc1_clk       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_120       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|--------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AB9               | mmc1_cmd     | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_121     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC9               | mmc1_dat0    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi2_clk   | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_122     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD9               | mmc1_dat1    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi2_simo  | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_123     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE9               | mmc1_dat2    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi2_somi  | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_124     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AA10              | mmc1_dat3    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi2_cs0   | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_125     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AB10              | mmc1_dat4    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_126     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC10              | mmc1_dat5    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_127     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD10              | mmc1_dat6    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_128     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE10              | mmc1_dat7    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_129     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD11              | mmc2_clk     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi3_clk   | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_cts    | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_130     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE11              | mmc2_cmd     | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi3_simo  | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_rts    | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_131     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AB12              | mmc2_dat0    | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi3_somi  | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_tx     | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_132     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC12              | mmc2_dat1    | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart4_rx     | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_133     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD12              | mmc2_dat2    | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi3_cs1   | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]   | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| AE12              | gpio_134       | 4        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc2_dat3      | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcspi3_cs0     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_135       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB13              | safe_mode      | 7        |          | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat4      | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc2_dir_dat0  | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat0      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_136       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AC13              | safe_mode      | 7        |          | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat5      | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc2_dir_dat1  | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat1      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_137       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AD13              | mm_fsusb3_rxdp | 6        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc2_dat6      | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc2_dir_cmd   | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat2      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AE13              | gpio_138       | 4        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc2_dat7      | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc2_clkin     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat3      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B24               | gpio_139       | 4        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mm_fsusb3_rxdm | 6        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_dx     | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart2_cts      | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
| C24               | gpio_140       | 4        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_dr     | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart2_rts      | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_141       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A24               | safe_mode      | 7        |          | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcbasp3_clkx   | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart2_tx       | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_142       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| C23               | safe_mode      | 7        |          | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcbasp3_fsx    | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart2_rx       | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_143       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| F20               | safe_mode      | 7        |          | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart2_cts      | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_dx     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt9_pwm_evt   | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_144       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| F19               | uart2_rts      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]    | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
|                   | mcbasp3_dr      | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt10_pwm_evt   | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_145        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| E24               | uart2_tx        | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcbasp3_clkx    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt11_pwm_evt   | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_146        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| E23               | uart2_rx        | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcbasp3_fsx     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt8_pwm_evt    | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_147        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AA19              | uart1_tx        | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_148        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| Y19               | uart1_rts       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_149        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| Y20               | uart1_cts       | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_150        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| W20               | uart1_rx        | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcbasp1_clkr    | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcspi4_clk      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_151        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| B23               | mcbasp4_clkx    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_152        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb3_txe0  | 6        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| A23               | mcbasp4_dr      | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_153        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb3_rxcv  | 6        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| B22               | mcbasp4_dx      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_154        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb3_txd   | 6        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| A22               | mcbasp4_fsx     | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_155        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb3_txe_n | 6        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| R25               | mcbasp1_clkr    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi4_clk      | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_156        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| P21               | mcbasp1_fsr     | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]   | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8]       | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|----------------|----------|----------|----------------------|---------------------------|---------------------|-----------------|-------------|----------|----------------|--------------------|--------------|
|                   | gpio_157       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| P22               | mcbsp1_dx      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | mcspi4_simo    | 1        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | mcbsp3_dx      | 2        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_158       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| P23               | mcbsp1_dr      | 0        | I        | L                    | PD                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | mcspi4_somi    | 1        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | mcbsp3_dr      | 2        | I        |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_159       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| P25               | mcbsp_clks     | 0        | I        | L                    | PD                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_160       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | uart1_cts      | 5        | I        |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| P24               | mcbsp1_fsx     | 0        | IO       | L                    | PD                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | mcspi4_cs0     | 1        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | mcbsp3_fsx     | 2        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_161       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| N24               | mcbsp1_clkx    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | mcbsp3_clkx    | 2        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_162       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| N2                | uart3_cts_rctx | 0        | IO       | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_163       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| N3                | uart3_rts_sd   | 0        | O        | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_164       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| P1                | uart3_rx_irrx  | 0        | I        | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_165       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| P2                | uart3_tx_irtx  | 0        | O        | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_166       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| F25               | usb0_dp        | 0        | IO       |                      |                           |                     |                 | 5.0V        | Yes      |                | PU/ PD             | USB_PHY      |
|                   | uart3_tx_irtx  | 1        | O        |                      |                           |                     |                 |             |          |                |                    |              |
| F24               | usb0_dm        | 0        | IO       |                      |                           |                     |                 | 5.0V        | Yes      |                | PU/ PD             | USB_PHY      |
|                   | uart3_rx_irrx  | 1        | I        |                      |                           |                     |                 |             |          |                |                    |              |
| G24               | usb0_vbus      | 0        | A        |                      |                           |                     | VDDA3P3V_USBPHY | 3.3V        | Yes      |                | PU/ PD             | USB_PHY      |
| G25               | usb0_id        | 0        | A        |                      |                           |                     | VDDA3P3V_USBPHY | 3.3V        | Yes      |                | PU/ PD             | USB_PHY      |
| E25               | usb0_drvvbus   | 0        | O        | L                    | PD                        | 7                   | VDDSHV          | 1.8V/3.3V   |          | 30             |                    | LVC MOS      |
|                   | uart3_tx_irtx  | 2        | O        |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_125       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | safe_mode      | 7        |          |                      |                           |                     |                 |             |          |                |                    |              |
| V2                | hecc1_txd      | 0        | O        | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 24             | PU/ PD             | LVC MOS      |
|                   | uart3_rx_irrx  | 2        | I        |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_130       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|--------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| V3                | hecc1_rxd    | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 24             | PU/ PD             | LVCMOS       |
|                   | uart3_rts_sd | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_131     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| V4                | i2c1_scl     | 0        | IOD      | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
| V5                | i2c1_sda     | 0        | IOD      | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
| W1                | i2c2_scl     | 0        | IOD      | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
|                   | gpio_168     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| W2                | i2c2_sda     | 0        | IOD      | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
|                   | gpio_183     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| W4                | i2c3_scl     | 0        | IOD      | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
|                   | gpio_184     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| W5                | i2c3_sda     | 0        | IOD      | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
|                   | gpio_185     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| L25               | hdq_sio      | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | LVCMOS       |
|                   | sys_altclk   | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | i2c2_sccbe   | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | i2c3_sccbe   | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_170     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE14              | mcspi1_clk   | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat4    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_171     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD15              | mcspi1_simo  | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat5    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_172     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC15              | mcspi1_somi  | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat6    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_173     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AB15              | mcspi1_cs0   | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat7    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_174     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD14              | mcspi1_cs1   | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc3_cmd     | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_175     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE15              | mcspi1_cs2   | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc3_clk     | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_176     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode    | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE16              | mcspi1_cs3   | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | hsusb2_data2 | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_177     | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]    | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
|                   | mm_fsusb2_txd   | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AD16              | mcspi2_clk      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | hsusb2_data7    | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_178        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AC16              | mcspi2_simo     | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpt9_pwm_evt    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_data4    | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_179        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AB16              | mcspi2_somi     | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpt10_pwm_evt   | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_data5    | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_180        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AA16              | mcspi2_cs0      | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpt11_pwm_evt   | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_data6    | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_181        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| AE17              | mcspi2_cs1      | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpt8_pwm_evt    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_data3    | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_182        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb2_xen_n | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| K24               | sys_32k         | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| K25               | sys_xtalin      | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V        | NA       |                | PU/ PD             | LVC MOS      |
| H25               | sys_xtalout     | 0        | O        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V        | NA       |                | PU/ PD             | LVC MOS      |
| M24               | sys_clkreq      | 0        | IO       | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_1          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| Y1                | sys_nirq        | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_0          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| Y2                | sys_nrespwrn    | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| Y3                | sys_nreswarm    | 0        | IO       | L                    | PD                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_30         | 4        | IO       |                      |                           |                     |           |             |          |                |                    | Open Drain   |
| Y4                | sys_boot0       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_2          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA1               | sys_boot1       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_3          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA2               | sys_boot2       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_4          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |

Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)

| BALL LOCATION [1] | PIN NAME [2]    | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| AA3               | sys_boot3       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_5          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB1               | sys_boot4       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dir_data2  | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_6          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB2               | sys_boot5       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dir_data3  | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_7          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AC1               | sys_boot6       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_8          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AC2               | sys_boot7       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
| AC3               | sys_boot8       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
| N25               | sys_clkout1     | 0        | O        | H                    | PD                        | 0/7 <sup>(1)</sup>  | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_10         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| M25               | sys_clkout2     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 10             | PU/ PD             | LVCMOS       |
|                   | gpio_186        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | safe_mode       | 7        |          |                      |                           |                     |           |             |          |                |                    |              |
| U24               | jtag_nrst       | 0        | I        | L                    | PD                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| U25               | jtag_tck        | 0        | I        | L                    | PD                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| T21               | jtag_rtk        | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| T22               | jtag_tms_tmsc   | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| T23               | jtag_tdi        | 0        | I        | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| T24               | jtag_tdo        | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| T25               | jtag_emu0       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_11         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| R24               | jtag_emu1       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_31         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AD17              | etk_clk         | 0        | O        | H                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mcbssp5_clkx    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_clk        | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_stp      | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_12         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AE18              | etk_ctl         | 0        | O        | H                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mmc3_cmd        | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_clk      | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_13         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb1_rxdp  | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AD18              | etk_d0          | 0        | O        | H                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mcspi3_simo     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat4       | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_data0    | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_14         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb1_rxrcv | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AC18              | etk_d1          | 0        | O        | H                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mcspi3_somi     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_data1    | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |

(1) Mux0 if sys\_boot6 is pulled down (clock master).

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]      | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|-------------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| AB18              | gpio_15           | 4        | IO       | H                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mm_fsusb1_t_xse0  | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d2            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcsapi3_cs0       | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_data2      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA18              | gpio_16           | 4        | IO       | L                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mm_fsusb1_t_xdat  | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d3            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcsapi3_clk       | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat3         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| Y18               | hsusb1_data7      | 3        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | gpio_17           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d4            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp5_dr        | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat0         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AE19              | hsusb1_data4      | 3        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | gpio_18           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d5            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp5_fsx       | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat1         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AD19              | hsusb1_data5      | 3        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | gpio_19           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d6            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp5_dx        | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat2         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB19              | hsusb1_data6      | 3        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | gpio_20           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d7            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcsapi3_cs1       | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat7         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AE20              | hsusb1_data3      | 3        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | gpio_21           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb1_t_xen_n | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d8            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat6         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AD20              | hsusb1_dir        | 3        | I        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | gpio_22           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d9            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat5         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_nxt        | 3        | I        |                      |                           |                     |           |             |          |                |                    |              |
| AC20              | gpio_23           | 4        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mm_fsusb1_r_xdm   | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d10           | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart1_rx          | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_clk        | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
| AB20              | gpio_24           | 4        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | etk_d11           | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcsapi3_clk       | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |

Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)

| BALL LOCATION [1]                                                                                                                                 | PIN NAME [2]           | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|---------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
|                                                                                                                                                   | hsusb2_stp             | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                   | gpio_25                | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                   | mm_fsusb2_r_xdp        | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AE21                                                                                                                                              | etk_d12                | 0        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                                                                                                                                                   | hsusb2_dir             | 3        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                   | gpio_26                | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AD21                                                                                                                                              | etk_d13                | 0        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                                                                                                                                                   | hsusb2_nxt             | 3        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                   | gpio_27                | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                   | mm_fsusb2_r_xdm        | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AC21                                                                                                                                              | etk_d14                | 0        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                                                                                                                                                   | hsusb2_data0           | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                   | gpio_28                | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                   | mm_fsusb2_r_xrcv       | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AE22                                                                                                                                              | etk_d15                | 0        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                                                                                                                                                   | hsusb2_data1           | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                   | gpio_29                | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                   | mm_fsusb2_t_xse0       | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| V16, V15, V11, V10, U16, U15, U11, U10, T18, T17, T9, T8, R18, R17, R9, R8, M18, L18, L9, L8, K18, K17, K9, K8, J16, J15, J11, J10, H15, H11, H10 | VDD_CORE               | 0        | PWR      |                      |                           |                     |           | 1.2V        |          |                |                    |              |
| AA13                                                                                                                                              | VDDS_SRAM_MPU          | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| E17                                                                                                                                               | VDDS_SRAM_CORE_B       | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| AA12                                                                                                                                              | CAP_VDD_SRAM_MPU       | 0        | PWR      |                      |                           |                     |           | 1.2V        |          |                |                    |              |
| E16                                                                                                                                               | CAP_VDD_SRAM_CORE      | 0        | PWR      |                      |                           |                     |           | 1.2V        |          |                |                    |              |
| AA15                                                                                                                                              | VDDS_DPLL_MPU_USB_HOST | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| N20                                                                                                                                               | VDDS_DPLL_PER_CORE     | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| H21                                                                                                                                               | VDDA_DAC               | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| F23                                                                                                                                               | VDDA3P3V_USBPHY        | 0        | PWR      |                      |                           |                     |           | 3.3V        |          |                |                    |              |
| G22                                                                                                                                               | VDDA1P8V_USBPHY        | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| F22                                                                                                                                               | CAP_VDDA1P2LDO_USBPHY  | 0        | PWR      |                      |                           |                     |           | 1.2V        |          |                |                    |              |

**Table 4-1. Ball Characteristics (ZCN Pkg.) (continued)**

| BALL LOCATION [1]                                                                                                                                                                                                                                                                                                                                                                                      | PIN NAME [2]      | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| Y16, Y15, Y13, Y12, Y10, W16, W15, W13, W12, W10, W9, W6, V7, V6, U19, T20, T19, T7, T6, R7, R6, P20, P19, N19, N7, N6, M7, M6, M5, L19, K19, K7, K6, K5, J7, H18, H17                                                                                                                                                                                                                                 | VDDSHV            | 0        | PWR      |                      |                           |                     |           | 1.8V/3.3V   |          |                |                    |              |
| Y9, W18, U20, R5, N22, H16, H8, G17, G16, G14, G13, G11, G10, G8, F16, F13, F11, F10, F8                                                                                                                                                                                                                                                                                                               | VDDS              | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| F14                                                                                                                                                                                                                                                                                                                                                                                                    | VREFSSTL          | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
| L20                                                                                                                                                                                                                                                                                                                                                                                                    | VDDSOSC           | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| J25                                                                                                                                                                                                                                                                                                                                                                                                    | VSSOSC            | 0        | GND      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| AE25, AE1, V18, V17, V14, V13, V12, V9, V8, U18, U17, U14, U13, U12, U9, U8, T14, T13, T12, R16, R15, R14, R13, R12, R11, R10, P18, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, N18, N17, N14, N13, N12, N9, N8, M17, M16, M15, M14, M13, M12, M11, M10, M9, M8, L17, L16, L15, L14, L13, L12, L11, L10, K14, K13, K12, J18, J17, J14, J13, J12, J9, J8, H14, H13, H12, H9, A25, A1, N23, G20, G21 | VSS               | 0        | GND      |                      |                           |                     |           |             |          |                |                    |              |
| H22                                                                                                                                                                                                                                                                                                                                                                                                    | VSSA_DAC          | 0        | GND      |                      |                           |                     |           |             |          |                |                    |              |
| L24, L23, L22, L21, K23, K22, H19, N21, F17                                                                                                                                                                                                                                                                                                                                                            | NC <sup>(2)</sup> |          |          |                      |                           |                     |           |             |          |                |                    |              |
| U2 <sup>(3)</sup>                                                                                                                                                                                                                                                                                                                                                                                      | Reserved          |          |          |                      |                           |                     |           |             |          |                |                    |              |
| V1 <sup>(3)</sup>                                                                                                                                                                                                                                                                                                                                                                                      | Reserved          |          |          |                      |                           |                     |           |             |          |                |                    |              |

(2) "NC" indicates "No Connect". For proper device operation, these pins **must be** left unconnected.

(3) For proper device operation, this pin **must be** pulled up to VDDSHV via a 10k-Ω resistor.

Table 4-2. Ball Characteristics (ZER Pkg.)

| BALL LOCATION [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|--------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| E3                | sdrc_d0      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| D3                | sdrc_d1      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C3                | sdrc_d2      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C2                | sdrc_d3      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| F3                | sdrc_d4      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| D2                | sdrc_d5      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| C1                | sdrc_d6      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| D1                | sdrc_d7      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| G2                | sdrc_d8      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| G3                | sdrc_d9      | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| H3                | sdrc_d10     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| G4                | sdrc_d11     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| H4                | sdrc_d12     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| G1                | sdrc_d13     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| J3                | sdrc_d14     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| J1                | sdrc_d15     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| T3                | sdrc_d16     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| U3                | sdrc_d17     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| U4                | sdrc_d18     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| V4                | sdrc_d19     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| V1                | sdrc_d20     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| V2                | sdrc_d21     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| V5                | sdrc_d22     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| V3                | sdrc_d23     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| W3                | sdrc_d24     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| W4                | sdrc_d25     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| Y3                | sdrc_d26     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| Y4                | sdrc_d27     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| AA2               | sdrc_d28     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| AA3               | sdrc_d29     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| AA4               | sdrc_d30     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| AB2               | sdrc_d31     | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 4              | PU/ PD             | LVC MOS      |
| L4                | sdrc_ba0     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| K5                | sdrc_ba1     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| J5                | sdrc_ba2     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| M3                | sdrc_a0      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| M4                | sdrc_a1      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| M5                | sdrc_a2      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| N3                | sdrc_a3      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| N2                | sdrc_a4      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| N4                | sdrc_a5      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| P3                | sdrc_a6      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| P2                | sdrc_a7      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| P1                | sdrc_a8      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| P4                | sdrc_a9      | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| R1                | sdrc_a10     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| R2                | sdrc_a11     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| R3                | sdrc_a12     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| R4                | sdrc_a13     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| T2                | sdrc_a14     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| J4                | sdrc_ncs0    | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| K4                | sdrc_ncs1    | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| L1                | sdrc_clk     | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
| L2                | sdrc_nclk    | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |

**Table 4-2. Ball Characteristics (ZER Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]     | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|------------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| K3                | sdrc_cke0        | 0        | O        | L                    | PD                        | 7                   | VDDS      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
|                   | sdrc_cke0_safe   | 7        | I        |                      |                           |                     |           |             |          |                |                    |              |
| K1                | sdrc_nras        | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| L3                | sdrc_ncas        | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| K2                | sdrc_nwe         | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| F4                | sdrc_dm0         | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| J2                | sdrc_dm1         | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| T4                | sdrc_dm2         | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| AB3               | sdrc_dm3         | 0        | O        | L                    | Z                         | 0                   | VDDS      | 1.8V        | No       | 8              | PU/ PD             | LVC MOS      |
| E2                | sdrc_dqs0p       | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
| H2                | sdrc_dqs1p       | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
| U1                | sdrc_dqs2p       | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
| Y1                | sdrc_dqs3p       | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        | Yes      | 8              | PU/ PD             | LVC MOS      |
| E1                | sdrc_dqs0n       | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| H1                | sdrc_dqs1n       | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| U2                | sdrc_dqs2n       | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| Y2                | sdrc_dqs3n       | 0        | IO       | L                    | Z                         | 0                   | VDDS      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| T1                | sdrc_odt         | 0        |          | L                    | Z                         | 0                   | VDDS      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| F2                | sdrc_strben0     | 0        |          | L                    | Z                         | 0                   | VDDS      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| F1                | sdrc_strben_dly0 | 0        |          | L                    | Z                         | 0                   | VDDS      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| W1                | sdrc_strben1     | 0        |          | L                    | Z                         | 0                   | VDDS      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| W2                | sdrc_strben_dly1 | 0        |          | L                    | Z                         | 0                   | VDDS      | 1.8V        |          | 8              | PU/ PD             | LVC MOS      |
| W5                | gpmc_a1          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_34          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| Y5                | gpmc_a2          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_35          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB4               | gpmc_a3          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_36          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA5               | gpmc_a4          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_37          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB5               | gpmc_a5          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_38          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB6               | gpmc_a6          | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_39          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA6               | gpmc_a7          | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_40          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| W6                | gpmc_a8          | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | gpio_41          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB7               | gpmc_a9          | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | sys_ndmareq2     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_42          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| Y6                | gpmc_a10         | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
|                   | sys_ndmareq3     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_43          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA7               | gpmc_d0          | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   |          | 30             | PU/ PD             | LVC MOS      |
| Y7                | gpmc_d1          | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| W7                | gpmc_d2          | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| AA9               | gpmc_d3          | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| Y8                | gpmc_d4          | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| AA8               | gpmc_d5          | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| AB8               | gpmc_d6          | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |
| W8                | gpmc_d7          | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVC MOS      |

Table 4-2. Ball Characteristics (ZER Pkg.) (continued)

| BALL LOCATION [1] | PIN NAME [2]  | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|---------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| W10               | gpmc_d8       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_44       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB9               | gpmc_d9       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_45       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB10              | gpmc_d10      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_46       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| W9                | gpmc_d11      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_47       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA10              | gpmc_d12      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_48       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| Y9                | gpmc_d13      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_49       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| V10               | gpmc_d14      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_50       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| V9                | gpmc_d15      | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_51       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| Y10               | gpmc_ncs0     | 0        | O        | H                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | NA                 | LVCMOS       |
|                   | gpmc_ncs1     | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
| Y11               | gpio_52       | 4        | IO       | H                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpmc_ncs2     | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
| Y12               | gpt9_pwm_evt  | 2        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_53       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| V12               | gpmc_ncs3     | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_ndmareq0  | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
| AA11              | gpt10_pwm_evt | 2        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_54       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA11              | gpmc_ncs4     | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_ndmareq1  | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
| W12               | gpt9_pwm_evt  | 3        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_55       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| W12               | gpmc_ncs5     | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_ndmareq2  | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
| AA12              | gpt10_pwm_evt | 3        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_56       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA12              | gpmc_ncs6     | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_ndmareq3  | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
| V11               | gpt11_pwm_evt | 3        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_57       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| V11               | gpmc_ncs7     | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpmc_io_dir   | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
| AB13              | gpt8_pwm_evt  | 3        | IO       | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_58       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB13              | gpmc_clk      | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_59       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA14              | gpmc_nadv_ale | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
| AB14              | gpmc_noe      | 0        | O        | H                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
| AA15              | gpmc_nwe      | 0        | O        | H                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |

**Table 4-2. Ball Characteristics (ZER Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]    | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| W11               | gpmc_nbe0_cle   | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_60         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| Y15               | gpmc_nbe1       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_61         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| W14               | gpmc_nwp        | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_62         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| V13               | gpmc_wait0      | 0        | I        | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
| AA16              | gpmc_wait1      | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart4_tx        | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_63         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| Y14               | gpmc_wait2      | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart4_rx        | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_64         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| V14               | gpmc_wait3      | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_ndmareq1    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart3_cts_rct_x | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_65         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B22               | dss_pclk        | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_66         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg12        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| B21               | dss_hsync       | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_67         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg13        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| B20               | dss_vsync       | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_68         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B19               | dss_acbias      | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_69         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A20               | dss_data0       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart1_cts       | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_70         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A19               | dss_data1       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart1_rts       | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_71         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A18               | dss_data2       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_72         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B18               | dss_data3       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_73         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A17               | dss_data4       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart3_rx_irrx   | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_74         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C18               | dss_data5       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart3_tx_irtx   | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_75         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D17               | dss_data6       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart1_tx        | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_76         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg14        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| B16               | dss_data7       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | uart1_rx        | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_77         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg15        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| B17               | dss_data8       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_78         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |

Table 4-2. Ball Characteristics (ZER Pkg.) (continued)

| BALL LOCATION [1] | PIN NAME [2] | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|--------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| C17               | hw_dbg16     | 5        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | dss_data9    | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_79      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg17     | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| C16               | dss_data10   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_80      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D16               | dss_data11   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_81      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D14               | dss_data12   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_82      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A16               | dss_data13   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_83      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D15               | dss_data14   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_84      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B15               | dss_data15   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_85      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A15               | dss_data16   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_86      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A14               | dss_data17   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_87      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C13               | dss_data18   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | mcspi3_clk   | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | dss_data4    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_88      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C15               | dss_data19   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | mcspi3_simo  | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | dss_data3    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_89      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A13               | dss_data20   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | mcspi3_somi  | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | dss_data2    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_90      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B13               | dss_data21   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | mcspi3_cs0   | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | dss_data1    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_91      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C14               | dss_data22   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | mcspi3_cs1   | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_92      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B14               | dss_data23   | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | dss_data5    | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_93      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB21              | ccdc_pclk    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | gpio_94      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg0      | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| AA21              | ccdc_field   | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | ccdc_data8   | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_tx     | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | i2c3_scl     | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_95      | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg1      | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| Y21               | ccdc_hd      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | uart4_rts    | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-2. Ball Characteristics (ZER Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]   | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| Y22               | gpio_96        | 4        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | ccdc_vd        | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_cts      | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_97        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| W21               | hw_dbg2        | 5        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/PD              | LVCMOS       |
|                   | ccdc_wen       | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | ccdc_data9     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_rx       | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_98        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| W22               | hw_dbg3        | 5        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/PD              | LVCMOS       |
|                   | ccdc_data0     | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | i2c3_sda       | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| W20               | gpio_99        | 4        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/PD              | LVCMOS       |
|                   | ccdc_data1     | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_100       | 4        | I        |                      |                           |                     |           |             |          |                |                    |              |
| V21               | ccdc_data2     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | gpio_101       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg4        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| V19               | ccdc_data3     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | gpio_102       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg5        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| V22               | ccdc_data4     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | gpio_103       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg6        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| U20               | ccdc_data5     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/ PD             | LVCMOS       |
|                   | gpio_104       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg7        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| V20               | ccdc_data6     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/PD              | LVCMOS       |
|                   | gpio_105       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| U19               | ccdc_data7     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 15             | PU/PD              | LVCMOS       |
|                   | gpio_106       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| U21               | rmii_mdio_data | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/PD              | LVCMOS       |
|                   | ccdc_data8     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_107       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| U22               | rmii_mdio_clk  | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/PD              | LVCMOS       |
|                   | ccdc_data9     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_108       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| T19               | rmii_rxd0      | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/ PD             | LVCMOS       |
|                   | ccdc_data10    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_109       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg8        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| T20               | rmii_rxd1      | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/ PD             | LVCMOS       |
|                   | ccdc_data11    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_110       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg9        | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| T21               | rmii_crs_dv    | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/ PD             | LVCMOS       |
|                   | ccdc_data12    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_111       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| R22               | rmii_rxer      | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/ PD             | LVCMOS       |
|                   | ccdc_data13    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_167       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg10       | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |

Table 4-2. Ball Characteristics (ZER Pkg.) (continued)

| BALL LOCATION [1] | PIN NAME [2]   | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| T22               | rmii_txd0      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/ PD             | LVCMOS       |
|                   | ccdc_data14    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_126       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hw_dbg11       | 5        | O        |                      |                           |                     |           |             |          |                |                    |              |
| R20               | rmii_txd1      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 25             | PU/PD              | LVCMOS       |
|                   | ccdc_data15    | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_112       | 4        | I        |                      |                           |                     |           |             |          |                |                    |              |
| R19               | rmii_txen      | 0        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | NA       | 25             | PU/PD              | LVCMOS       |
|                   | gpio_113       | 4        | I        |                      |                           |                     |           |             |          |                |                    |              |
| R21               | rmii_50mhz_clk | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | NA       | 25             | PU/ PD             | LVCMOS       |
|                   | gpio_114       | 4        | I        |                      |                           |                     |           |             |          |                |                    |              |
| E5                | mcbasp2_fsx    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_116       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D5                | mcbasp2_clkx   | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_117       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C5                | mcbasp2_dr     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_118       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| E4                | mcbasp2_dx     | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_119       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| P22               | mmc1_clk       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_120       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| N21               | mmc1_cmd       | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_121       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| P21               | mmc1_dat0      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi2_clk     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_122       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| N20               | mmc1_dat1      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi2_simo    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_123       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| P19               | mmc1_dat2      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi2_somi    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_124       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| P20               | mmc1_dat3      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi2_cs0     | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_125       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| N22               | mmc1_dat4      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_126       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| N19               | mmc1_dat5      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_127       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| N18               | mmc1_dat6      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_128       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| P18               | mmc1_dat7      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | No       | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_129       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| M21               | mmc2_clk       | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi3_clk     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_cts      | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_130       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| M20               | mmc2_cmd       | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi3_simo    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_rts      | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_131       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| K20               | mmc2_dat0      | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi3_somi    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-2. Ball Characteristics (ZER Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]   | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| L19               | uart4_tx       | 2        | O        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_132       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc2_dat1      | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart4_rx       | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
| M18               | gpio_133       | 4        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat2      | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcspi3_cs1     | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_134       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| K21               | mmc2_dat3      | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspi3_cs0     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_135       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc2_dat4      | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| L18               | mmc2_dir_dat0  | 1        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc3_dat0      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_136       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc2_dat5      | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| L20               | mmc2_dir_dat1  | 1        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc3_dat1      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_137       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb3_rxdp | 6        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| L21               | mmc2_dat6      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dir_cmd   | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat2      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_138       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| M19               | mmc2_dat7      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_clkln     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat3      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_139       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C4                | mm_fsusb3_rxdm | 6        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcbasp3_dx     | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart2_cts      | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_140       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B4                | mcbasp3_dr     | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart2_rts      | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_141       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_clkx   | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D4                | uart2_tx       | 1        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_142       | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_fsx    | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart2_rx       | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
| A4                | gpio_143       | 4        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart2_cts      | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_dx     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt9_pwm_evt   | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A5                | gpio_144       | 4        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart2_rts      | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_dr     | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt10_pwm_evt  | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B5                | gpio_145       | 4        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart2_tx       | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_dx     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt9_pwm_evt   | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D6                | gpio_146       | 4        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | uart2_tx       | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_dx     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt9_pwm_evt   | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |

Table 4-2. Ball Characteristics (ZER Pkg.) (continued)

| BALL LOCATION [1] | PIN NAME [2]      | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|-------------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
|                   | mcbasp3_clkx      | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt11_pwm_evt     | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_146          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C6                | uart2_rx          | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcbasp3_fsx       | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpt8_pwm_evt      | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_147          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C22               | uart1_tx          | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_148          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C21               | uart1_rts         | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_149          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C19               | uart1_cts         | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_150          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C20               | uart1_rx          | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcbasp1_clkx      | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcsapi4_clk       | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_151          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A3                | mcbasp4_clkx      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_152          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb3_t_xse0  | 6        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B3                | mcbasp4_dr        | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_153          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb3_r_xrcv  | 6        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A2                | mcbasp4_dx        | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_154          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb3_t_xdat  | 6        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B2                | mcbasp4_fsx       | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_155          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb3_t_xen_n | 6        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| B11               | mcbasp1_clkx      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcsapi4_clk       | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_156          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D11               | mcbasp1_fsr       | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_157          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C10               | mcbasp1_dx        | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcsapi4_simo      | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_dx        | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_158          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C9                | mcbasp1_dr        | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcsapi4_somi      | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_dr        | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_159          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| E11               | mcbasp1_clks      | 0        | I        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_160          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart1_cts         | 5        | I        |                      |                           |                     |           |             |          |                |                    |              |
| C11               | mcbasp1_fsx       | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcsapi4_cs0       | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp3_fsx       | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_161          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| C8                | mcbasp1_clkx      | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |

**Table 4-2. Ball Characteristics (ZER Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]   | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8]       | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|----------------|----------|----------|----------------------|---------------------------|---------------------|-----------------|-------------|----------|----------------|--------------------|--------------|
|                   | mcbasp3_clkx   | 2        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_162       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| W15               | uart3_cts_rctx | 0        | IO       | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_163       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| W13               | uart3_rts_sd   | 0        | O        | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_164       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| AA13              | uart3_rx_irrx  | 0        | I        | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_165       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| Y13               | uart3_tx_irtx  | 0        | O        | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_166       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| A6                | usb0_dp        | 0        | IO       |                      |                           |                     |                 | 5.0V        | Yes      |                | PU/ PD             | LVCMOS       |
| B6                | usb0_dm        | 0        | IO       |                      |                           |                     |                 | 5.0V        | Yes      |                | PU/ PD             | LVCMOS       |
| C7                | usb0_vbus      | 0        | A        |                      |                           |                     | VDDA3P3V_USBPHY | 3.3V        | Yes      |                | PU/ PD             | LVCMOS       |
| B7                | usb0_id        | 0        | A        |                      |                           |                     | VDDA3P3V_USBPHY | 3.3V        | Yes      |                | PU/ PD             | LVCMOS       |
| A7                | usb0_drvvbus   | 0        | O        | L                    | PD                        | 7                   | VDDSHV          | 1.8V/3.3V   |          | 30             |                    |              |
|                   | uart3_tx_irtx  | 2        | O        |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_125       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| AB15              | hecc1_txd      | 0        | O        | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 24             | PU/ PD             | LVCMOS       |
|                   | uart3_rx_irrx  | 2        | I        |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_130       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| AB16              | hecc1_rxd      | 0        | I        | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 24             | PU/ PD             | LVCMOS       |
|                   | uart3_rts_sd   | 2        | O        |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_131       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| AA17              | i2c1_scl       | 0        | IOD      | H                    | PU                        | 0                   | VDDSHV          | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
| AB17              | i2c1_sda       | 0        | IOD      | H                    | PU                        | 0                   | VDDSHV          | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
| Y17               | i2c2_scl       | 0        | IOD      | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
|                   | gpio_168       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| Y16               | i2c2_sda       | 0        | IOD      | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
|                   | gpio_183       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| W16               | i2c3_scl       | 0        | IOD      | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
|                   | gpio_184       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| W17               | i2c3_sda       | 0        | IOD      | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | Open Drain   |
|                   | gpio_185       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| B9                | hdq_sio        | 0        | IO       | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 40             | PU/ PD             | LVCMOS       |
|                   | sys_altclk     | 1        | I        |                      |                           |                     |                 |             |          |                |                    |              |
|                   | i2c2_sccbe     | 2        | O        |                      |                           |                     |                 |             |          |                |                    |              |
|                   | i2c3_sccbe     | 3        | O        |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_170       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| K22               | mcspl1_clk     | 0        | IO       | L                    | PD                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat4      | 1        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_171       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| K19               | mcspl1_simo    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat5      | 1        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_172       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| J18               | mcspl1_somi    | 0        | IO       | L                    | PD                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat6      | 1        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_173       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| K18               | mcspl1_cs0     | 0        | IO       | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dat7      | 1        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
|                   | gpio_174       | 4        | IO       |                      |                           |                     |                 |             |          |                |                    |              |
| J20               | mcspl1_cs1     | 0        | O        | H                    | PU                        | 7                   | VDDSHV          | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |

Table 4-2. Ball Characteristics (ZER Pkg.) (continued)

| BALL LOCATION [1] | PIN NAME [2]      | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|-------------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| J19               | mmc3_cmd          | 3        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_175          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcspl1_cs2        | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_clk          | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
| J21               | gpio_176          | 4        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspl1_cs3        | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_data2      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_177          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| J22               | mm_fsusb2_t_xdat  | 5        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mcspl2_clk        | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_data7      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_178          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| H20               | mcspl2_simo       | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpt9_pwm_evt      | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_data4      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_179          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| H22               | mcspl2_somi       | 0        | IO       | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpt10_pwm_evt     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_data5      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_180          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| H21               | mcspl2_cs0        | 0        | IO       | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpt11_pwm_evt     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_data6      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_181          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| H19               | mcspl2_cs1        | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpt8_pwm_evt      | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_data3      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_182          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| A8                | mm_fsusb2_t_xen_n | 5        | IO       | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_32k           | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | sys_xtalin        | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | sys_xtalout       | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
| B8                | sys_clkreq        | 0        | IO       | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_1            | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AB18              | sys_nirq          | 0        | I        | H                    | PU                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_0            | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA18              | sys_nrespwron     | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_nreswarm      | 0        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| Y18               | gpio_30           | 4        | IO       | L                    | PD                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_boot0         | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
| AB19              | gpio_2            | 4        | IO       | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_boot1         | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
| AB20              | gpio_3            | 4        | IO       | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_boot2         | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |
| W18               | gpio_4            | 4        | IO       | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | sys_boot2         | 0        | I        |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-2. Ball Characteristics (ZER Pkg.) (continued)**

| BALL LOCATION [1] | PIN NAME [2]    | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|-----------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| AA19              | sys_boot3       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_5          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| V18               | sys_boot4       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dir_data2  | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_6          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| Y19               | sys_boot5       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | mmc2_dir_data3  | 1        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_7          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| W19               | sys_boot6       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_8          | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| AA20              | sys_boot7       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
| Y20               | sys_boot8       | 0        | I        | Z                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
| E9                | sys_clkout1     | 0        | O        | H                    | PD                        | 0/7 <sup>(1)</sup>  | VDDSHV    | 1.8V/3.3V   | Yes      | 30             | PU/ PD             | LVCMOS       |
|                   | gpio_10         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| E10               | sys_clkout2     | 0        | O        | L                    | PD                        | 7                   | VDDSHV    | 1.8V/3.3V   | Yes      | 10             | PU/ PD             | LVCMOS       |
|                   | gpio_186        | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D13               | jtag_nrst       | 0        | I        | L                    | PD                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| E14               | jtag_tck        | 0        | I        | L                    | PD                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| C12               | jtag_rtck       | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| A12               | jtag_tms_tmsc   | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| B12               | jtag_tdi        | 0        | I        | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| D12               | jtag_tdo        | 0        | O        | L                    | Z                         | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
| E13               | jtag_emu0       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_11         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| E12               | jtag_emu1       | 0        | IO       | H                    | PU                        | 0                   | VDDSHV    | 1.8V/3.3V   | Yes      | 20             | PU/ PD             | LVCMOS       |
|                   | gpio_31         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| G22               | etk_clk         | 0        | O        | H                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mcbasp5_clkx    | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_clk        | 2        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_stp      | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_12         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| G21               | etk_ctl         | 0        | O        | H                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mmc3_cmd        | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_clk      | 3        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_13         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb1_rxdp  | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| G20               | etk_d0          | 0        | O        | H                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mcspi3_simo     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat4       | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_data0    | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_14         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb1_rxcv  | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| F22               | etk_d1          | 0        | O        | H                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mcspi3_somi     | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_data1    | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_15         | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb1_txse0 | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |

(1) Mux0 if sys\_boot6 is pulled down (clock master).

Table 4-2. Ball Characteristics (ZER Pkg.) (continued)

| BALL LOCATION [1] | PIN NAME [2]      | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------|-------------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| F20               | etk_d2            | 0        | O        | H                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mcspi3_cs0        | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_data2      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_16           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb1_t_xdat  | 5        | IO       | L                    | PU                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | etk_d3            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcspi3_clk        | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat3         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_data7      | 3        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | gpio_17           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d4            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp5_dr        | 1        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat0         | 2        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | hsusb1_data4      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_18           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d5            | 0        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
| F21               | mcbasp5_fsx       | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat1         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_data5      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_19           | 4        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | etk_d6            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcbasp5_dx        | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat2         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_data6      | 3        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | gpio_20           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d7            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcspi3_cs1        | 1        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
| E21               | mmc3_dat7         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_data3      | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_21           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | mm_fsusb1_t_xen_n | 5        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | etk_d8            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat6         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_dir        | 3        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_22           | 4        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | etk_d9            | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mmc3_dat5         | 2        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb1_nxt        | 3        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | gpio_23           | 4        | IO       | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | mm_fsusb1_r_xdm   | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d10           | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | uart1_rx          | 2        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_clk        | 3        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | gpio_24           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d11           | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcspi3_clk        | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | hsusb2_stp        | 3        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                   | gpio_25           | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                   | etk_d11           | 0        | O        |                      |                           |                     |           |             |          |                |                    |              |
|                   | mcspi3_clk        | 1        | IO       |                      |                           |                     |           |             |          |                |                    |              |

**Table 4-2. Ball Characteristics (ZER Pkg.) (continued)**

| BALL LOCATION [1]                                                                                                                                | PIN NAME [2]          | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|--------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
|                                                                                                                                                  | mm_fsusb2_r_xdp       | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| E18                                                                                                                                              | etk_d12               | 0        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                                                                                                                                                  | hsusb2_dir            | 3        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                  | gpio_26               | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D20                                                                                                                                              | etk_d13               | 0        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                                                                                                                                                  | hsusb2_nxt            | 3        | I        |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                  | gpio_27               | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                  | mm_fsusb2_r_xdm       | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D19                                                                                                                                              | etk_d14               | 0        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                                                                                                                                                  | hsusb2_data0          | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                  | gpio_28               | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                  | mm_fsusb2_r_xrcv      | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| D18                                                                                                                                              | etk_d15               | 0        | O        | L                    | PD                        | 4                   | VDDSHV    | 1.8V/3.3V   | Yes      | 9, 25          | PU/ PD             | LVCMOS       |
|                                                                                                                                                  | hsusb2_data1          | 3        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                  | gpio_29               | 4        | IO       |                      |                           |                     |           |             |          |                |                    |              |
|                                                                                                                                                  | mm_fsusb2_t_xse0      | 5        | IO       |                      |                           |                     |           |             |          |                |                    |              |
| M2                                                                                                                                               | ddr_padref            | 0        | A        |                      |                           |                     | VDDS      | 1.8V        |          |                |                    |              |
| J8, J10, J12, J14, J16, K9, K11, K13, K15, L8, L10, L12, L14, M7, M9, M11, M13, M15, N8, N10, N12, N14, P7, P9, P11, P13, P15, R8, R10, R12, R14 | VDD_CORE              | 0        | PWR      |                      |                           |                     |           | 1.2V        |          |                |                    |              |
| L17                                                                                                                                              | VDDS_SRAM_MPU         | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| J6                                                                                                                                               | VDDS_SRAM_CORE_BG     | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| M17                                                                                                                                              | CAP_VDD_SRAM_MPU      | 0        | PWR      |                      |                           |                     |           | 1.2V        |          |                |                    |              |
| K6                                                                                                                                               | CAP_VDD_SRAM_CORE     | 0        | PWR      |                      |                           |                     |           | 1.2V        |          |                |                    |              |
| K17                                                                                                                                              | VDDS_DPLL_MPU_USBHOST | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| F11                                                                                                                                              | VDDS_DPLL_PER_CORE    | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| F7                                                                                                                                               | VDDA3P3V_USBPHY       | 0        | PWR      |                      |                           |                     |           | 3.3V        |          |                |                    |              |
| D7                                                                                                                                               | VDDA1P8V_USBPHY       | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| E7                                                                                                                                               | CAP_VDDA1P2LDO_USBPHY | 0        | PWR      |                      |                           |                     |           | 1.2V        |          |                |                    |              |

Table 4-2. Ball Characteristics (ZER Pkg.) (continued)

| BALL LOCATION [1]                                                                                                                                                                                                                                                                                                                                                                                                 | PIN NAME [2]            | MODE [3] | TYPE [4] | BALL RESET STATE [5] | BALL RESET REL. STATE [6] | RESET REL. MODE [7] | POWER [8] | VOLTAGE [9] | HYS [10] | LOAD (pF) [11] | PULL U/D TYPE [12] | IO CELL [13] |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------|----------|----------|----------------------|---------------------------|---------------------|-----------|-------------|----------|----------------|--------------------|--------------|
| A21, B1, E15, E17, F12, F14, F18, G10, G12, G13, G8, G17, H18, J17, L22, N16, P17, R16, R18, T9, T11, T13, T17, U8, U10, U12, U14, U16, U18, V7, V8, V17, AA22, AB11                                                                                                                                                                                                                                              | VDDSHV                  | 0        | PWR      |                      |                           |                     |           | 1.8V/3.3V   |          |                |                    |              |
| F5, F16, G15, H5, K7, L6, L16, N1, N5, N6, P5, R6, T5, T7, T15, U6, AA1                                                                                                                                                                                                                                                                                                                                           | VDDS                    | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| L5                                                                                                                                                                                                                                                                                                                                                                                                                | VREFSSTL                | 0        | I        |                      |                           |                     |           | .5 * VDDS   |          |                |                    |              |
| G9                                                                                                                                                                                                                                                                                                                                                                                                                | VDDSOSC                 | 0        | PWR      |                      |                           |                     |           | 1.8V        |          |                |                    |              |
| A1, A11, A22, E6, E16, F6, F13, F15, F17, G5, G7, G11, G14, G16, G18, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, J9, J11, J13, J15, K8, K10, K12, K14, K16, L7, L9, L11, L13, L15, M1, M6, M8, M10, M12, M14, M16, M22, N7, N9, N11, N13, N15, N17, P6, P8, P10, P12, P14, P16, R5, R7, R9, R11, R13, R15, R17, T6, T8, T10, T12, T14, T16, T18, U5, U7, U9, U11, U13, U15, U17, V6, AB1, AB12, AB22 | VSS                     | 0        | GND      |                      |                           |                     |           |             |          |                |                    |              |
| B10                                                                                                                                                                                                                                                                                                                                                                                                               | VSSOSC                  | 0        | GND      |                      |                           |                     |           |             |          |                |                    |              |
| D8, D9, D10, E8, F8, F9, F10, J7, G6                                                                                                                                                                                                                                                                                                                                                                              | NC <sup>(2)</sup>       |          |          |                      |                           |                     |           |             |          |                |                    |              |
| V15                                                                                                                                                                                                                                                                                                                                                                                                               | Reserved <sup>(3)</sup> |          |          |                      |                           |                     |           |             |          |                |                    |              |
| V16                                                                                                                                                                                                                                                                                                                                                                                                               | Reserved <sup>(3)</sup> |          |          |                      |                           |                     |           |             |          |                |                    |              |

(2) "NC" indicates "No Connect". For proper device operation, these pins **must be** left unconnected.(3) For proper device operation, this pin **must be** pulled up via a 10k-Ω resistor.

### 4.3 Multiplexing Characteristics

Table 4-3 provides descriptions of the AM3517/05 pin multiplexing on the ZCN and ZER packages.

**Table 4-3. Multiplexing Characteristics**

| ZER     | ZCN     | MODE 0    | MODE 1 | MODE 2 | MODE 3 | MODE 4 | MODE 5 | MODE 6 | MODE 7 |
|---------|---------|-----------|--------|--------|--------|--------|--------|--------|--------|
| BALL NO | BALL NO |           |        |        |        |        |        |        |        |
| E3      | B21     | sdrc_d0   |        |        |        |        |        |        |        |
| D3      | A21     | sdrc_d1   |        |        |        |        |        |        |        |
| C3      | D20     | sdrc_d2   |        |        |        |        |        |        |        |
| C2      | C20     | sdrc_d3   |        |        |        |        |        |        |        |
| F3      | E19     | sdrc_d4   |        |        |        |        |        |        |        |
| D2      | D19     | sdrc_d5   |        |        |        |        |        |        |        |
| C1      | C19     | sdrc_d6   |        |        |        |        |        |        |        |
| D1      | B19     | sdrc_d7   |        |        |        |        |        |        |        |
| G2      | B18     | sdrc_d8   |        |        |        |        |        |        |        |
| G3      | D17     | sdrc_d9   |        |        |        |        |        |        |        |
| H3      | C17     | sdrc_d10  |        |        |        |        |        |        |        |
| G4      | D16     | sdrc_d11  |        |        |        |        |        |        |        |
| H4      | C16     | sdrc_d12  |        |        |        |        |        |        |        |
| G1      | B16     | sdrc_d13  |        |        |        |        |        |        |        |
| J3      | A16     | sdrc_d14  |        |        |        |        |        |        |        |
| J1      | A15     | sdrc_d15  |        |        |        |        |        |        |        |
| T3      | A7      | sdrc_d16  |        |        |        |        |        |        |        |
| U3      | B7      | sdrc_d17  |        |        |        |        |        |        |        |
| U4      | D7      | sdrc_d18  |        |        |        |        |        |        |        |
| V4      | E7      | sdrc_d19  |        |        |        |        |        |        |        |
| V1      | C6      | sdrc_d20  |        |        |        |        |        |        |        |
| V2      | D6      | sdrc_d21  |        |        |        |        |        |        |        |
| V5      | B5      | sdrc_d22  |        |        |        |        |        |        |        |
| V3      | C5      | sdrc_d23  |        |        |        |        |        |        |        |
| W3      | B4      | sdrc_d24  |        |        |        |        |        |        |        |
| W4      | A3      | sdrc_d25  |        |        |        |        |        |        |        |
| Y3      | B3      | sdrc_d26  |        |        |        |        |        |        |        |
| Y4      | C3      | sdrc_d27  |        |        |        |        |        |        |        |
| AA2     | C2      | sdrc_d28  |        |        |        |        |        |        |        |
| AA3     | D2      | sdrc_d29  |        |        |        |        |        |        |        |
| AA4     | B1      | sdrc_d30  |        |        |        |        |        |        |        |
| AB2     | C1      | sdrc_d31  |        |        |        |        |        |        |        |
| L4      | A12     | sdrc_ba0  |        |        |        |        |        |        |        |
| K5      | C13     | sdrc_ba1  |        |        |        |        |        |        |        |
| J5      | D13     | sdrc_ba2  |        |        |        |        |        |        |        |
| M3      | A11     | sdrc_a0   |        |        |        |        |        |        |        |
| M4      | B11     | sdrc_a1   |        |        |        |        |        |        |        |
| M5      | C11     | sdrc_a2   |        |        |        |        |        |        |        |
| N3      | D11     | sdrc_a3   |        |        |        |        |        |        |        |
| N2      | E11     | sdrc_a4   |        |        |        |        |        |        |        |
| N4      | A10     | sdrc_a5   |        |        |        |        |        |        |        |
| P3      | B10     | sdrc_a6   |        |        |        |        |        |        |        |
| P2      | C10     | sdrc_a7   |        |        |        |        |        |        |        |
| P1      | D10     | sdrc_a8   |        |        |        |        |        |        |        |
| P4      | E10     | sdrc_a9   |        |        |        |        |        |        |        |
| R1      | A9      | sdrc_a10  |        |        |        |        |        |        |        |
| R2      | B9      | sdrc_a11  |        |        |        |        |        |        |        |
| R3      | A8      | sdrc_a12  |        |        |        |        |        |        |        |
| R4      | B8      | sdrc_a13  |        |        |        |        |        |        |        |
| T2      | D8      | sdrc_a14  |        |        |        |        |        |        |        |
| J4      | E13     | sdrc_ncs0 |        |        |        |        |        |        |        |

**Table 4-3. Multiplexing Characteristics (continued)**

| ZER  | ZCN | MODE 0           | MODE 1       | MODE 2        | MODE 3        | MODE 4  | MODE 5 | MODE 6 | MODE 7         |
|------|-----|------------------|--------------|---------------|---------------|---------|--------|--------|----------------|
| K4   | A14 | sdrc_ncs1        |              |               |               |         |        |        |                |
| L1   | A13 | sdrc_clk         |              |               |               |         |        |        |                |
| L2   | B13 | sdrc_nclk        |              |               |               |         |        |        |                |
| K3   | D14 | sdrc_cke0        |              |               |               |         |        |        | sdrc_cke0_safe |
| K1   | C14 | sdrc_nras        |              |               |               |         |        |        |                |
| L3   | E14 | sdrc_ncas        |              |               |               |         |        |        |                |
| K2   | B14 | sdrc_nwe         |              |               |               |         |        |        |                |
| F4   | C21 | sdrc_dm0         |              |               |               |         |        |        |                |
| J2   | B15 | sdrc_dm1         |              |               |               |         |        |        |                |
| T4   | E8  | sdrc_dm2         |              |               |               |         |        |        |                |
| AB3  | D1  | sdrc_dm3         |              |               |               |         |        |        |                |
| E2   | B20 | sdrc_dqs0p       |              |               |               |         |        |        |                |
| H2   | B17 | sdrc_dqs1p       |              |               |               |         |        |        |                |
| U1   | A6  | sdrc_dqs2p       |              |               |               |         |        |        |                |
| Y1   | A2  | sdrc_dqs3p       |              |               |               |         |        |        |                |
| E1   | A20 | sdrc_dqs0n       |              |               |               |         |        |        |                |
| H1   | A17 | sdrc_dqs1n       |              |               |               |         |        |        |                |
| U2   | B6  | sdrc_dqs2n       |              |               |               |         |        |        |                |
| Y2   | B2  | sdrc_dqs3n       |              |               |               |         |        |        |                |
| T1   | C8  | sdrc_odt         |              |               |               |         |        |        |                |
| F2   | A19 | sdrc_strben0     |              |               |               |         |        |        |                |
| F1   | A18 | sdrc_strben_dly0 |              |               |               |         |        |        |                |
| W1   | A5  | sdrc_strben1     |              |               |               |         |        |        |                |
| W2   | A4  | sdrc_strben_dly1 |              |               |               |         |        |        |                |
| W5   | E3  | gpmc_a1          |              |               |               | gpio_34 |        |        | safe_mode      |
| Y5   | E2  | gpmc_a2          |              |               |               | gpio_35 |        |        | safe_mode      |
| AB4  | E1  | gpmc_a3          |              |               |               | gpio_36 |        |        | safe_mode      |
| AA5  | F7  | gpmc_a4          |              |               |               | gpio_37 |        |        | safe_mode      |
| AB5  | F6  | gpmc_a5          |              |               |               | gpio_38 |        |        | safe_mode      |
| AB6  | F4  | gpmc_a6          |              |               |               | gpio_39 |        |        | safe_mode      |
| AA6  | F3  | gpmc_a7          |              |               |               | gpio_40 |        |        | safe_mode      |
| W6   | F2  | gpmc_a8          |              |               |               | gpio_41 |        |        | safe_mode      |
| AB7  | F1  | gpmc_a9          | sys_ndmareq2 |               |               | gpio_42 |        |        | safe_mode      |
| Y6   | G6  | gpmc_a10         | sys_ndmareq3 |               |               | gpio_43 |        |        | safe_mode      |
| AA7  | G5  | gpmc_d0          |              |               |               |         |        |        |                |
| Y7   | G4  | gpmc_d1          |              |               |               |         |        |        |                |
| W7   | G3  | gpmc_d2          |              |               |               |         |        |        |                |
| AA9  | G2  | gpmc_d3          |              |               |               |         |        |        |                |
| Y8   | G1  | gpmc_d4          |              |               |               |         |        |        |                |
| AA8  | H2  | gpmc_d5          |              |               |               |         |        |        |                |
| AB8  | H1  | gpmc_d6          |              |               |               |         |        |        |                |
| W8   | J5  | gpmc_d7          |              |               |               |         |        |        |                |
| W10  | J4  | gpmc_d8          |              |               |               | gpio_44 |        |        |                |
| AB9  | J3  | gpmc_d9          |              |               |               | gpio_45 |        |        |                |
| AB10 | J2  | gpmc_d10         |              |               |               | gpio_46 |        |        |                |
| W9   | J1  | gpmc_d11         |              |               |               | gpio_47 |        |        |                |
| AA10 | K4  | gpmc_d12         |              |               |               | gpio_48 |        |        |                |
| Y9   | K3  | gpmc_d13         |              |               |               | gpio_49 |        |        |                |
| V10  | K2  | gpmc_d14         |              |               |               | gpio_50 |        |        |                |
| V9   | K1  | gpmc_d15         |              |               |               | gpio_51 |        |        |                |
| Y10  | L2  | gpmc_ncs0        |              |               |               |         |        |        |                |
| Y11  | L1  | gpmc_ncs1        |              |               |               | gpio_52 |        |        |                |
| Y12  | M4  | gpmc_ncs2        |              | gpt9_pwm_evt  |               | gpio_53 |        |        | safe_mode      |
| V12  | M3  | gpmc_ncs3        | sys_ndmareq0 | gpt10_pwm_evt |               | gpio_54 |        |        | safe_mode      |
| AA11 | M2  | gpmc_ncs4        | sys_ndmareq1 |               | gpt9_pwm_evt  | gpio_55 |        |        | safe_mode      |
| W12  | M1  | gpmc_ncs5        | sys_ndmareq2 |               | gpt10_pwm_evt | gpio_56 |        |        | safe_mode      |

**Table 4-3. Multiplexing Characteristics (continued)**

| ZER  | ZCN  | MODE 0        | MODE 1       | MODE 2         | MODE 3        | MODE 4   | MODE 5   | MODE 6 | MODE 7    |
|------|------|---------------|--------------|----------------|---------------|----------|----------|--------|-----------|
| AA12 | N5   | gpmc_ncs6     | sys_ndmareq3 |                | gpt11_pwm_evt | gpio_57  |          |        | safe_mode |
| V11  | N4   | gpmc_ncs7     | gpmc_io_dir  |                | gpt8_pwm_evt  | gpio_58  |          |        | safe_mode |
| AB13 | N1   | gpmc_clk      |              |                |               | gpio_59  |          |        |           |
| AA14 | R1   | gpmc_nadv_ale |              |                |               |          |          |        |           |
| AB14 | R2   | gpmc_noe      |              |                |               |          |          |        |           |
| AA15 | R3   | gpmc_nwe      |              |                |               |          |          |        |           |
| W11  | R4   | gpmc_nbe0_cle |              |                |               | gpio_60  |          |        |           |
| Y15  | T1   | gpmc_nbe1     |              |                |               | gpio_61  |          |        | safe_mode |
| W14  | T2   | gpmc_nwp      |              |                |               | gpio_62  |          |        |           |
| V13  | T3   | gpmc_wait0    |              |                |               |          |          |        |           |
| AA16 | T4   | gpmc_wait1    | uart4_tx     |                |               | gpio_63  |          |        | safe_mode |
| Y14  | T5   | gpmc_wait2    | uart4_rx     |                |               | gpio_64  |          |        | safe_mode |
| V14  | U1   | gpmc_wait3    | sys_ndmareq1 | uart3_cts_rctx |               | gpio_65  |          |        | safe_mode |
| B22  | AE23 | dss_pclk      |              |                |               | gpio_66  | hw_dbg12 |        | safe_mode |
| B21  | AD22 | dss_hsync     |              |                |               | gpio_67  | hw_dbg13 |        | safe_mode |
| B20  | AD23 | dss_vsync     |              |                |               | gpio_68  |          |        | safe_mode |
| B19  | AE24 | dss_acbias    |              |                |               | gpio_69  |          |        | safe_mode |
| A20  | AD24 | dss_data0     |              | uart1_cts      |               | gpio_70  |          |        | safe_mode |
| A19  | AD25 | dss_data1     |              | uart1_rts      |               | gpio_71  |          |        | safe_mode |
| A18  | AC23 | dss_data2     |              |                |               | gpio_72  |          |        | safe_mode |
| B18  | AC24 | dss_data3     |              |                |               | gpio_73  |          |        | safe_mode |
| A17  | AC25 | dss_data4     |              | uart3_rx_irrx  |               | gpio_74  |          |        | safe_mode |
| C18  | AB24 | dss_data5     |              | uart3_tx_irtx  |               | gpio_75  |          |        | safe_mode |
| D17  | AB25 | dss_data6     |              | uart1_tx       |               | gpio_76  | hw_dbg14 |        | safe_mode |
| B16  | AA23 | dss_data7     |              | uart1_rx       |               | gpio_77  | hw_dbg15 |        | safe_mode |
| B17  | AA24 | dss_data8     |              |                |               | gpio_78  | hw_dbg16 |        | safe_mode |
| C17  | AA25 | dss_data9     |              |                |               | gpio_79  | hw_dbg17 |        | safe_mode |
| C16  | Y22  | dss_data10    |              |                |               | gpio_80  |          |        | safe_mode |
| D16  | Y23  | dss_data11    |              |                |               | gpio_81  |          |        | safe_mode |
| D14  | Y24  | dss_data12    |              |                |               | gpio_82  |          |        | safe_mode |
| A16  | Y25  | dss_data13    |              |                |               | gpio_83  |          |        | safe_mode |
| D15  | W21  | dss_data14    |              |                |               | gpio_84  |          |        | safe_mode |
| B15  | W22  | dss_data15    |              |                |               | gpio_85  |          |        | safe_mode |
| A15  | W23  | dss_data16    |              |                |               | gpio_86  |          |        | safe_mode |
| A14  | W24  | dss_data17    |              |                |               | gpio_87  |          |        | safe_mode |
| C13  | W25  | dss_data18    |              | mcspi3_clk     | dss_data4     | gpio_88  |          |        | safe_mode |
| C15  | V24  | dss_data19    |              | mcspi3_simo    | dss_data3     | gpio_89  |          |        | safe_mode |
| A13  | V25  | dss_data20    |              | mcspi3_somi    | dss_data2     | gpio_90  |          |        | safe_mode |
| B13  | U21  | dss_data21    |              | mcspi3_cs0     | dss_data1     | gpio_91  |          |        | safe_mode |
| C14  | U22  | dss_data22    |              | mcspi3_cs1     | dss_data0     | gpio_92  |          |        | safe_mode |
| B14  | U23  | dss_data23    |              |                | dss_data5     | gpio_93  |          |        | safe_mode |
| NA   | K20  | tv_vfb1       |              |                |               |          |          |        |           |
| NA   | K21  | tv_out1       |              |                |               |          |          |        |           |
| NA   | H23  | tv_vfb2       |              |                |               |          |          |        |           |
| NA   | H24  | tv_out2       |              |                |               |          |          |        |           |
| NA   | H20  | tv_vref       |              |                |               |          |          |        |           |
| AB21 | AD2  | ccdc_pclk     |              |                |               | gpio_94  | hw_dbg0  |        | safe_mode |
| AA21 | AD1  | ccdc_field    | ccdc_data8   | uart4_tx       | i2c3_scl      | gpio_95  | hw_dbg1  |        | safe_mode |
| Y21  | AE2  | ccdc_hd       |              | uart4_rts      |               | gpio_96  |          |        | safe_mode |
| Y22  | AD3  | ccdc_vd       |              | uart4_cts      |               | gpio_97  | hw_dbg2  |        | safe_mode |
| W21  | AE3  | ccdc_wen      | ccdc_data9   | uart4_rx       |               | gpio_98  | hw_dbg3  |        | safe_mode |
| W22  | AD4  | ccdc_data0    |              |                | i2c3_sda      | gpio_99  |          |        | safe_mode |
| W20  | AE4  | ccdc_data1    |              |                |               | gpio_100 |          |        | safe_mode |
| V21  | AC5  | ccdc_data2    |              |                |               | gpio_101 | hw_dbg4  |        | safe_mode |
| V19  | AD5  | ccdc_data3    |              |                |               | gpio_102 | hw_dbg5  |        | safe_mode |
| V22  | AE5  | ccdc_data4    |              |                |               | gpio_103 | hw_dbg6  |        | safe_mode |

**Table 4-3. Multiplexing Characteristics (continued)**

| ZER | ZCN  | MODE 0         | MODE 1        | MODE 2        | MODE 3     | MODE 4   | MODE 5   | MODE 6           | MODE 7    |
|-----|------|----------------|---------------|---------------|------------|----------|----------|------------------|-----------|
| U20 | Y6   | ccdc_data5     |               |               |            | gpio_104 | hw_dbg7  |                  | safe_mode |
| V20 | AB6  | ccdc_data6     |               |               |            | gpio_105 |          |                  | safe_mode |
| U19 | AC6  | ccdc_data7     |               |               |            | gpio_106 |          |                  | safe_mode |
| U21 | AE6  | rmii_mdio_data | ccdc_data8    |               |            | gpio_107 |          |                  | safe_mode |
| U22 | AD6  | rmii_mdio_clk  | ccdc_data9    |               |            | gpio_108 |          |                  | safe_mode |
| T19 | Y7   | rmii_rxd0      | ccdc_data10   |               |            | gpio_109 | hw_dbg8  |                  | safe_mode |
| T20 | AA7  | rmii_rxd1      | ccdc_data11   |               |            | gpio_110 | hw_dbg9  |                  | safe_mode |
| T21 | AB7  | rmii_crs_dv    | ccdc_data12   |               |            | gpio_111 |          |                  | safe_mode |
| R22 | AC7  | rmii_rxer      | ccdc_data13   |               |            | gpio_167 | hw_dbg10 |                  | safe_mode |
| T22 | AD7  | rmii_txd0      | ccdc_data14   |               |            | gpio_126 | hw_dbg11 |                  | safe_mode |
| R20 | AE7  | rmii_txd1      | ccdc_data15   |               |            | gpio_112 |          |                  | safe_mode |
| R19 | AD8  | rmii_txen      |               |               |            | gpio_113 |          |                  | safe_mode |
| R21 | AE8  | rmii_50mhz_clk |               |               |            | gpio_114 |          |                  | safe_mode |
| E5  | D25  | mcbsp2_fsx     |               |               |            | gpio_116 |          |                  | safe_mode |
| D5  | C25  | mcbsp2_clkx    |               |               |            | gpio_117 |          |                  | safe_mode |
| C5  | B25  | mcbsp2_dr      |               |               |            | gpio_118 |          |                  | safe_mode |
| E4  | D24  | mcbsp2_dx      |               |               |            | gpio_119 |          |                  | safe_mode |
| P22 | AA9  | mmc1_clk       |               |               |            | gpio_120 |          |                  | safe_mode |
| N21 | AB9  | mmc1_cmd       |               |               |            | gpio_121 |          |                  | safe_mode |
| P21 | AC9  | mmc1_dat0      | mcspi2_clk    |               |            | gpio_122 |          |                  | safe_mode |
| N20 | AD9  | mmc1_dat1      | mcspi2_simo   |               |            | gpio_123 |          |                  | safe_mode |
| P19 | AE9  | mmc1_dat2      | mcspi2_somi   |               |            | gpio_124 |          |                  | safe_mode |
| P20 | AA10 | mmc1_dat3      | mcspi2_cs0    |               |            | gpio_125 |          |                  | safe_mode |
| N22 | AB10 | mmc1_dat4      |               |               |            | gpio_126 |          |                  | safe_mode |
| N19 | AC10 | mmc1_dat5      |               |               |            | gpio_127 |          |                  | safe_mode |
| N18 | AD10 | mmc1_dat6      |               |               |            | gpio_128 |          |                  | safe_mode |
| P18 | AE10 | mmc1_dat7      |               |               |            | gpio_129 |          |                  | safe_mode |
| M21 | AD11 | mmc2_clk       | mcspi3_clk    | uart4_cts     |            | gpio_130 |          |                  | safe_mode |
| M20 | AE11 | mmc2_cmd       | mcspi3_simo   | uart4_rts     |            | gpio_131 |          |                  | safe_mode |
| K20 | AB12 | mmc2_dat0      | mcspi3_somi   | uart4_tx      |            | gpio_132 |          |                  | safe_mode |
| L19 | AC12 | mmc2_dat1      |               | uart4_rx      |            | gpio_133 |          |                  | safe_mode |
| M18 | AD12 | mmc2_dat2      | mcspi3_cs1    |               |            | gpio_134 |          |                  | safe_mode |
| K21 | AE12 | mmc2_dat3      | mcspi3_cs0    |               |            | gpio_135 |          |                  | safe_mode |
| L18 | AB13 | mmc2_dat4      | mmc2_dir_dat0 |               | mmc3_dat0  | gpio_136 |          |                  | safe_mode |
| L20 | AC13 | mmc2_dat5      | mmc2_dir_dat1 |               | mmc3_dat1  | gpio_137 |          | mm_fsusb3_rxdp   | safe_mode |
| L21 | AD13 | mmc2_dat6      | mmc2_dir_cmd  |               | mmc3_dat2  | gpio_138 |          |                  | safe_mode |
| M19 | AE13 | mmc2_dat7      | mmc2_clkin    |               | mmc3_dat3  | gpio_139 |          | mm_fsusb3_rxdm   | safe_mode |
| C4  | B24  | mcbsp3_dx      | uart2_cts     |               |            | gpio_140 |          |                  | safe_mode |
| B4  | C24  | mcbsp3_dr      | uart2_rts     |               |            | gpio_141 |          |                  | safe_mode |
| D4  | A24  | mcbsp3_clkx    | uart2_tx      |               |            | gpio_142 |          |                  | safe_mode |
| A4  | C23  | mcbsp3_fsx     | uart2_rx      |               |            | gpio_143 |          |                  | safe_mode |
| A5  | F20  | uart2_cts      | mcbsp3_dx     | gpt9_pwm_evt  |            | gpio_144 |          |                  | safe_mode |
| B5  | F19  | uart2_rts      | mcbsp3_dr     | gpt10_pwm_evt |            | gpio_145 |          |                  | safe_mode |
| D6  | E24  | uart2_tx       | mcbsp3_clkx   | gpt11_pwm_evt |            | gpio_146 |          |                  | safe_mode |
| C6  | E23  | uart2_rx       | mcbsp3_fsx    | gpt8_pwm_evt  |            | gpio_147 |          |                  | safe_mode |
| C22 | AA19 | uart1_tx       |               |               |            | gpio_148 |          |                  | safe_mode |
| C21 | Y19  | uart1_rts      |               |               |            | gpio_149 |          |                  | safe_mode |
| C19 | Y20  | uart1_cts      |               |               |            | gpio_150 |          |                  | safe_mode |
| C20 | W20  | uart1_rx       |               | mcbsp1_clkr   | mcspi4_clk | gpio_151 |          |                  | safe_mode |
| A3  | B23  | mcbsp4_clkx    |               |               |            | gpio_152 |          | mm_fsusb3_txse0  | safe_mode |
| B3  | A23  | mcbsp4_dr      |               |               |            | gpio_153 |          | mm_fsusb3_rxcv   | safe_mode |
| A2  | B22  | mcbsp4_dx      |               |               |            | gpio_154 |          | mm_fsusb3_txdm   | safe_mode |
| B2  | A22  | mcbsp4_fsx     |               |               |            | gpio_155 |          | mm_fsusb3_txen_n | safe_mode |
| B11 | R25  | mcbsp1_clkr    | mcspi4_clk    |               |            | gpio_156 |          |                  | safe_mode |
| D11 | P21  | mcbsp1_fsr     |               |               |            | gpio_157 |          |                  | safe_mode |

**Table 4-3. Multiplexing Characteristics (continued)**

| ZER  | ZCN  | MODE 0                 | MODE 1        | MODE 2        | MODE 3       | MODE 4   | MODE 5           | MODE 6 | MODE 7    |
|------|------|------------------------|---------------|---------------|--------------|----------|------------------|--------|-----------|
| C10  | P22  | mcbasp1_dx             | mcspi4_simo   | mcbasp3_dx    |              | gpio_158 |                  |        | safe_mode |
| C9   | P23  | mcbasp1_dr             | mcspi4_somi   | mcbasp3_dr    |              | gpio_159 |                  |        | safe_mode |
| E11  | P25  | mcbasp_clks            |               |               |              | gpio_160 | uart1_cts        |        | safe_mode |
| C11  | P24  | mcbasp1_fsx            | mcspi4_cs0    | mcbasp3_fsx   |              | gpio_161 |                  |        | safe_mode |
| C8   | N24  | mcbasp1_clkx           |               | mcbasp3_clkx  |              | gpio_162 |                  |        | safe_mode |
| W15  | N2   | uart3_cts_rctx         |               |               |              | gpio_163 |                  |        | safe_mode |
| W13  | N3   | uart3_rts_sd           |               |               |              | gpio_164 |                  |        | safe_mode |
| AA13 | P1   | uart3_rx_irrx          |               |               |              | gpio_165 |                  |        | safe_mode |
| Y13  | P2   | uart3_tx_irtx          |               |               |              | gpio_166 |                  |        |           |
| A6   | F25  | usb0_dp <sup>(1)</sup> | uart3_tx_irtx |               |              |          |                  |        |           |
| B6   | F24  | usb0_dm <sup>(1)</sup> | uart3_rx_irrx |               |              |          |                  |        |           |
| C7   | G24  | usb0_vbus              |               |               |              |          |                  |        |           |
| B7   | G25  | usb0_id                |               |               |              |          |                  |        |           |
| A7   | E25  | usb0_drvvbus           |               | uart3_tx_irtx |              | gpio_125 |                  |        | safe_mode |
| AB15 | V2   | hecc1_txd              |               | uart3_rx_irrx |              | gpio_130 |                  |        | safe_mode |
| AB16 | V3   | hecc1_rxd              |               | uart3_rts_sd  |              | gpio_131 |                  |        | safe_mode |
| AA17 | V4   | i2c1_scl               |               |               |              |          |                  |        |           |
| AB17 | V5   | i2c1_sda               |               |               |              |          |                  |        |           |
| Y17  | W1   | i2c2_scl               |               |               |              | gpio_168 |                  |        | safe_mode |
| Y16  | W2   | i2c2_sda               |               |               |              | gpio_183 |                  |        | safe_mode |
| W16  | W4   | i2c3_scl               |               |               |              | gpio_184 |                  |        | safe_mode |
| W17  | W5   | i2c3_sda               |               |               |              | gpio_185 |                  |        | safe_mode |
| B9   | L25  | hdq_sio                | sys_altdclk   | i2c2_sccbe    | i2c3_sccbe   | gpio_170 |                  |        | safe_mode |
| K22  | AE14 | mcspi1_clk             | mmc2_dat4     |               |              | gpio_171 |                  |        | safe_mode |
| K19  | AD15 | mcspi1_simo            | mmc2_dat5     |               |              | gpio_172 |                  |        | safe_mode |
| J18  | AC15 | mcspi1_somi            | mmc2_dat6     |               |              | gpio_173 |                  |        | safe_mode |
| K18  | AB15 | mcspi1_cs0             | mmc2_dat7     |               |              | gpio_174 |                  |        | safe_mode |
| J20  | AD14 | mcspi1_cs1             |               |               | mmc3_cmd     | gpio_175 |                  |        | safe_mode |
| J19  | AE15 | mcspi1_cs2             |               |               | mmc3_clk     | gpio_176 |                  |        | safe_mode |
| J21  | AE16 | mcspi1_cs3             |               |               | hsusb2_data2 | gpio_177 | mm_fsusb2_txdat  |        | safe_mode |
| J22  | AD16 | mcspi2_clk             |               |               | hsusb2_data7 | gpio_178 |                  |        | safe_mode |
| H20  | AC16 | mcspi2_simo            | gpt9_pwm_evt  |               | hsusb2_data4 | gpio_179 |                  |        | safe_mode |
| H22  | AB16 | mcspi2_somi            | gpt10_pwm_evt |               | hsusb2_data5 | gpio_180 |                  |        | safe_mode |
| H21  | AA16 | mcspi2_cs0             | gpt11_pwm_evt |               | hsusb2_data6 | gpio_181 |                  |        | safe_mode |
| H19  | AE17 | mcspi2_cs1             | gpt8_pwm_evt  |               | hsusb2_data3 | gpio_182 | mm_fsusb2_txen_n |        | safe_mode |
| AB18 | Y1   | sys_nirq               |               |               |              | gpio_0   |                  |        | safe_mode |
| E10  | M25  | sys_clkout2            |               |               |              | gpio_186 |                  |        | safe_mode |
| G22  | AD17 | etk_clk                | mcbasp5_clkx  | mmc3_clk      | hsusb1_stp   | gpio_12  |                  |        | hw_dbg0   |
| G21  | AE18 | etk_ctl                |               | mmc3_cmd      | hsusb1_clk   | gpio_13  | mm_fsusb1_rxdp   |        | hw_dbg1   |
| G20  | AD18 | etk_d0                 | mcspi3_simo   | mmc3_dat4     | hsusb1_data0 | gpio_14  | mm_fsusb1_rxrcv  |        | hw_dbg2   |
| F22  | AC18 | etk_d1                 | mcspi3_somi   |               | hsusb1_data1 | gpio_15  | mm_fsusb1_txse0  |        | hw_dbg3   |
| F20  | AB18 | etk_d2                 | mcspi3_cs0    |               | hsusb1_data2 | gpio_16  | mm_fsusb1_txdat  |        | hw_dbg4   |
| G19  | AA18 | etk_d3                 | mcspi3_clk    | mmc3_dat3     | hsusb1_data7 | gpio_17  |                  |        | hw_dbg5   |
| E19  | Y18  | etk_d4                 | mcbasp5_dr    | mmc3_dat0     | hsusb1_data4 | gpio_18  |                  |        | hw_dbg6   |
| F21  | AE19 | etk_d5                 | mcbasp5_fsx   | mmc3_dat1     | hsusb1_data5 | gpio_19  |                  |        | hw_dbg7   |
| F19  | AD19 | etk_d6                 | mcbasp5_dx    | mmc3_dat2     | hsusb1_data6 | gpio_20  |                  |        | hw_dbg8   |
| E21  | AB19 | etk_d7                 | mcspi3_cs1    | mmc3_dat7     | hsusb1_data3 | gpio_21  | mm_fsusb1_txen_n |        | hw_dbg9   |
| D22  | AE20 | etk_d8                 |               | mmc3_dat6     | hsusb1_dir   | gpio_22  |                  |        | hw_dbg10  |
| D21  | AD20 | etk_d9                 |               | mmc3_dat5     | hsusb1_nxt   | gpio_23  | mm_fsusb1_rxdm   |        | hw_dbg11  |
| E22  | AC20 | etk_d10                |               | uart1_rx      | hsusb2_clk   | gpio_24  |                  |        | hw_dbg12  |
| E20  | AB20 | etk_d11                | mcspi3_clk    |               | hsusb2_stp   | gpio_25  | mm_fsusb2_rxdp   |        | hw_dbg13  |
| E18  | AE21 | etk_d12                |               |               | hsusb2_dir   | gpio_26  |                  |        | hw_dbg14  |
| D20  | AD21 | etk_d13                |               |               | hsusb2_nxt   | gpio_27  | mm_fsusb2_rxdm   |        | hw_dbg15  |

(1) This mux selection is controlled by CONTROL\_DEVCONF2 register.

**Table 4-3. Multiplexing Characteristics (continued)**

| ZER  | ZCN  | MODE 0        | MODE 1        | MODE 2 | MODE 3       | MODE 4  | MODE 5              | MODE 6 | MODE 7    |
|------|------|---------------|---------------|--------|--------------|---------|---------------------|--------|-----------|
| D19  | AC21 | etk_d14       |               |        | hsusb2_data0 | gpio_28 | mm_fsusb2_rxrcv     |        | hw_dbg16  |
| D18  | AE22 | etk_d15       |               |        | hsusb2_data1 | gpio_29 | mm_fsusb2_txse<br>0 |        | hw_dbg17  |
| A8   | K24  | sys_32k       |               |        |              |         |                     |        |           |
| A10  | K25  | sys_xtalin    |               |        |              |         |                     |        |           |
| A9   | H25  | sys_xtalout   |               |        |              |         |                     |        |           |
| B8   | M24  | sys_clkreq    |               |        |              | gpio_1  |                     |        |           |
| AA18 | Y2   | sys_nrespwrn  |               |        |              |         |                     |        |           |
| Y18  | Y3   | sys_nreswarm  |               |        |              | gpio_30 |                     |        |           |
| AB19 | Y4   | sys_boot0     |               |        |              | gpio_2  |                     |        |           |
| AB20 | AA1  | sys_boot1     |               |        |              | gpio_3  |                     |        |           |
| W18  | AA2  | sys_boot2     |               |        |              | gpio_4  |                     |        |           |
| AA19 | AA3  | sys_boot3     |               |        |              | gpio_5  |                     |        |           |
| V18  | AB1  | sys_boot4     | mmc2_dir_dat2 |        |              | gpio_6  |                     |        |           |
| Y19  | AB2  | sys_boot5     | mmc2_dir_dat3 |        |              | gpio_7  |                     |        |           |
| W19  | AC1  | sys_boot6     |               |        |              | gpio_8  |                     |        |           |
| AA20 | AC2  | sys_boot7     |               |        |              |         |                     |        |           |
| Y20  | AC3  | sys_boot8     |               |        |              |         |                     |        |           |
| E9   | N25  | sys_clkout1   |               |        |              | gpio_10 |                     |        | safe_mode |
| D13  | U24  | jtag_ntrst    |               |        |              |         |                     |        |           |
| E14  | U25  | jtag_tck      |               |        |              |         |                     |        |           |
| C12  | T21  | jtag_rtck     |               |        |              |         |                     |        |           |
| A12  | T22  | jtag_tms_tmsc |               |        |              |         |                     |        |           |
| B12  | T23  | jtag_tdi      |               |        |              |         |                     |        |           |
| D12  | T24  | jtag_tdo      |               |        |              |         |                     |        |           |
| E13  | T25  | jtag_emu0     |               |        |              | gpio_11 |                     |        |           |
| E12  | R24  | jtag_emu1     |               |        |              | gpio_31 |                     |        |           |
| M2   | B12  | ddr_padref    |               |        |              |         |                     |        |           |

## 4.4 Signal Description

Many signals are available on multiple pins according to the software configuration of the pin multiplexing options.

1. **SIGNAL NAME:** The signal name
2. **DESCRIPTION:** Description of the signal
3. **TYPE:** Type = Ball type for this specific function:
  - I = Input
  - O = Output
  - Z = High-impedance
  - D = Open Drain
  - DS = Differential
  - A = Analog
4. **BALL:** Associated ball location
5. **SUBSYSTEM PIN MULTIPLEXING:** Contains a list of the pin multiplexing options at the module/subsystem level. The pin function is selected at the module/system level.

**Note:** The Subsystem Multiplexing Signals are not described in [Table 4-1](#) and [Table 4-2](#).

### 4.4.1 External Memory Interfaces

**Table 4-4. External Memory Interfaces - GPMC Signals Description**

| SIGNAL NAME <sup>[1]</sup> | DESCRIPTION <sup>[2]</sup>                  | TYPE <sup>[3]</sup> | ZCN BALL <sup>[4]</sup> | ZER BALL <sup>[4]</sup> | SUBSYSTEM PIN MULTIPLEXING <sup>[5]</sup> |
|----------------------------|---------------------------------------------|---------------------|-------------------------|-------------------------|-------------------------------------------|
| gpmc_a1                    | GPMC Address bit 1                          | O                   | E3/G5                   | W5/AA7                  | gpmc_a17                                  |
| gpmc_a2                    | GPMC Address bit 2                          | O                   | E2/G4                   | Y5/Y7                   | gpmc_a18                                  |
| gpmc_a3                    | GPMC Address bit 3                          | O                   | E1/G3                   | AB4/W7                  | gpmc_a19                                  |
| gpmc_a4                    | GPMC Address bit 4                          | O                   | F7/G2                   | AA5/AA9                 | gpmc_a20                                  |
| gpmc_a5                    | GPMC Address bit 5                          | O                   | F6/G1                   | AB5/Y8                  | gpmc_a21                                  |
| gpmc_a6                    | GPMC Address bit 6                          | O                   | F4/H2                   | AB6/AA8                 | gpmc_a22                                  |
| gpmc_a7                    | GPMC Address bit 7                          | O                   | F3/H1                   | AA6/AB8                 | gpmc_a23                                  |
| gpmc_a8                    | GPMC Address bit 8                          | O                   | F2/J5                   | W6/W8                   | gpmc_a24                                  |
| gpmc_a9                    | GPMC Address bit 9                          | O                   | F1/J4                   | AB7/W10                 | gpmc_a25                                  |
| gpmc_a10                   | GPMC Address bit 10                         | O                   | G6/J3                   | Y6/AB9                  | gpmc_a26                                  |
| gpmc_a11                   | GPMC Address bit 11 multiplexed on gpmc_d10 | O                   | J2                      | AB10                    |                                           |
| gpmc_a12                   | GPMC Address bit 12 multiplexed on gpmc_d11 | O                   | J1                      | W9                      |                                           |
| gpmc_a13                   | GPMC Address bit 13 multiplexed on gpmc_d12 | O                   | K4                      | AA10                    |                                           |
| gpmc_a14                   | GPMC Address bit 14 multiplexed on gpmc_d13 | O                   | K3                      | Y9                      |                                           |
| gpmc_a15                   | GPMC Address bit 15 multiplexed on gpmc_d14 | O                   | K2                      | V10                     |                                           |
| gpmc_a16                   | GPMC Address bit 16 multiplexed on gpmc_d15 | O                   | K1                      | V9                      |                                           |
| gpmc_a17                   | GPMC Address bit 17 multiplexed on gpmc_a1  | O                   | E3                      | W5                      |                                           |

**Table 4-4. External Memory Interfaces - GPMC Signals Description (continued)**

| <b>SIGNAL NAME</b> <sup>[1]</sup> | <b>DESCRIPTION</b> <sup>[2]</sup>                | <b>TYPE</b> <sup>[3]</sup> | <b>ZCN BALL</b> <sup>[4]</sup> | <b>ZER BALL</b> <sup>[4]</sup> | <b>SUBSYSTEM PIN<br/>MULTIPLEXING</b> <sup>[5]</sup> |
|-----------------------------------|--------------------------------------------------|----------------------------|--------------------------------|--------------------------------|------------------------------------------------------|
| gpmc_a18                          | GPMC Address bit18<br>multiplexed on<br>gpmc_a2  | O                          | E2                             | Y5                             |                                                      |
| gpmc_a19                          | GPMC Address bit19<br>multiplexed on<br>gpmc_a3  | O                          | E1                             | AB4                            |                                                      |
| gpmc_a20                          | GPMC Address bit20<br>multiplexed on<br>gpmc_a4  | O                          | F7                             | AA5                            |                                                      |
| gpmc_a21                          | GPMC Address bit21<br>multiplexed on<br>gpmc_a5  | O                          | F6                             | AB5                            |                                                      |
| gpmc_a22                          | GPMC Address bit22<br>multiplexed on<br>gpmc_a6  | O                          | F4                             | AB6                            |                                                      |
| gpmc_a23                          | GPMC Address bit23<br>multiplexed on<br>gpmc_a7  | O                          | F3                             | AA6                            |                                                      |
| gpmc_a24                          | GPMC Address bit24<br>multiplexed on<br>gpmc_a8  | O                          | F2                             | W6                             |                                                      |
| gpmc_a25                          | GPMC Address bit25<br>multiplexed on<br>gpmc_a9  | O                          | F1                             | AB7                            |                                                      |
| gpmc_a26                          | GPMC Address bit26<br>multiplexed on<br>gpmc_a10 | O                          | G6                             | Y6                             |                                                      |
| gpmc_d0                           | GPMC Data bit 0                                  | IO                         | G5                             | AA7                            | gpmc_a1/gpmc_d0                                      |
| gpmc_d1                           | GPMC Data bit 1                                  | IO                         | G4                             | Y7                             | gpmc_a2/gpmc_d1                                      |
| gpmc_d2                           | GPMC Data bit 2                                  | IO                         | G3                             | W7                             | gpmc_a3/gpmc_d2                                      |
| gpmc_d3                           | GPMC Data bit 3                                  | IO                         | G2                             | AA9                            | gpmc_a4/gpmc_d3                                      |
| gpmc_d4                           | GPMC Data bit 4                                  | IO                         | G1                             | Y8                             | gpmc_a5/gpmc_d4                                      |
| gpmc_d5                           | GPMC Data bit 5                                  | IO                         | H2                             | AA8                            | gpmc_a6/gpmc_d5                                      |
| gpmc_d6                           | GPMC Data bit 6                                  | IO                         | H1                             | AB8                            | gpmc_a7/gpmc_d6                                      |
| gpmc_d7                           | GPMC Data bit 7                                  | IO                         | J5                             | W8                             | gpmc_a8/gpmc_d7                                      |
| gpmc_d8                           | GPMC Data bit 8                                  | IO                         | J4                             | W10                            | gpmc_a9/gpmc_d8                                      |
| gpmc_d9                           | GPMC Data bit 9                                  | IO                         | J3                             | AB9                            | gpmc_a10/gpmc_d9                                     |
| gpmc_d10                          | GPMC Data bit 10                                 | IO                         | J2                             | AB10                           | gpmc_a11/gpmc_d10                                    |
| gpmc_d11                          | GPMC Data bit 11                                 | IO                         | J1                             | W9                             | gpmc_a12/gpmc_d11                                    |
| gpmc_d12                          | GPMC Data bit 12                                 | IO                         | K4                             | AA10                           | gpmc_a13/gpmc_d12                                    |
| gpmc_d13                          | GPMC Data bit 13                                 | IO                         | K3                             | Y9                             | gpmc_a14/gpmc_d13                                    |
| gpmc_d14                          | GPMC Data bit 14                                 | IO                         | K2                             | V10                            | gpmc_a15/gpmc_d14                                    |
| gpmc_d15                          | GPMC Data bit 15                                 | IO                         | K1                             | V9                             | gpmc_a16/gpmc_d15                                    |
| gpmc_ncs0                         | GPMC Chip Select 0                               | O                          | L2                             | Y10                            |                                                      |
| gpmc_ncs1                         | GPMC Chip Select 1                               | O                          | L1                             | Y11                            |                                                      |
| gpmc_ncs2                         | GPMC Chip Select 2                               | O                          | M4                             | Y12                            |                                                      |
| gpmc_ncs3                         | GPMC Chip Select 3                               | O                          | M3                             | V12                            |                                                      |
| gpmc_ncs4                         | GPMC Chip Select 4                               | O                          | M2                             | AA11                           |                                                      |
| gpmc_ncs5                         | GPMC Chip Select 5                               | O                          | M1                             | W12                            |                                                      |
| gpmc_ncs6                         | GPMC Chip Select 6                               | O                          | N5                             | AA12                           |                                                      |
| gpmc_ncs7                         | GPMC Chip Select 7                               | O                          | N4                             | V11                            |                                                      |
| gpmc_clk                          | GPMC clock                                       | O                          | N1                             | AB13                           |                                                      |

**Table 4-4. External Memory Interfaces - GPMC Signals Description (continued)**

| SIGNAL NAME <sup>[1]</sup> | DESCRIPTION <sup>[2]</sup>                            | TYPE <sup>[3]</sup> | ZCN BALL <sup>[4]</sup> | ZER BALL <sup>[4]</sup> | SUBSYSTEM PIN MULTIPLEXING <sup>[5]</sup> |
|----------------------------|-------------------------------------------------------|---------------------|-------------------------|-------------------------|-------------------------------------------|
| gpmc_nadv_ale              | Address Valid or Address Latch Enable                 | O                   | R1                      | AA14                    |                                           |
| gpmc_noe                   | Output Enable                                         | O                   | R2                      | AB14                    |                                           |
| gpmc_nwe                   | Write Enable                                          | O                   | R3                      | AA15                    |                                           |
| gpmc_nbe0_cle              | Lower Byte Enable. Also used for Command Latch Enable | O                   | R4                      | W11                     |                                           |
| gpmc_nbe1                  | Upper Byte Enable                                     | O                   | T1                      | Y15                     |                                           |
| gpmc_nwp                   | Flash Write Protect                                   | O                   | T2                      | W14                     |                                           |
| gpmc_wait0                 | External indication of wait                           | I                   | T3                      | V13                     |                                           |
| gpmc_wait1                 | External indication of wait                           | I                   | T4                      | AA16                    |                                           |
| gpmc_wait2                 | External indication of wait                           | I                   | T5                      | Y14                     |                                           |
| gpmc_wait3                 | External indication of wait                           | I                   | U1                      | V14                     |                                           |

**Table 4-5. External Memory Interfaces - SDRAM Signals Description**

| SIGNAL NAME <sup>[1]</sup> | DESCRIPTION <sup>[2]</sup> | TYPE <sup>[3]</sup> | ZCN BALL <sup>[4]</sup> | ZER BALL <sup>[4]</sup> |
|----------------------------|----------------------------|---------------------|-------------------------|-------------------------|
| sdrc_d0                    | SDRAM data bit 0           | IO                  | B21                     | E3                      |
| sdrc_d1                    | SDRAM data bit 1           | IO                  | A21                     | D3                      |
| sdrc_d2                    | SDRAM data bit 2           | IO                  | D20                     | C3                      |
| sdrc_d3                    | SDRAM data bit 3           | IO                  | C20                     | C2                      |
| sdrc_d4                    | SDRAM data bit 4           | IO                  | E19                     | F3                      |
| sdrc_d5                    | SDRAM data bit 5           | IO                  | D19                     | D2                      |
| sdrc_d6                    | SDRAM data bit 6           | IO                  | C19                     | C1                      |
| sdrc_d7                    | SDRAM data bit 7           | IO                  | B19                     | D1                      |
| sdrc_d8                    | SDRAM data bit 8           | IO                  | B18                     | G2                      |
| sdrc_d9                    | SDRAM data bit 9           | IO                  | D17                     | G3                      |
| sdrc_d10                   | SDRAM data bit 10          | IO                  | C17                     | H3                      |
| sdrc_d11                   | SDRAM data bit 11          | IO                  | D16                     | G4                      |
| sdrc_d12                   | SDRAM data bit 12          | IO                  | C16                     | H4                      |
| sdrc_d13                   | SDRAM data bit 13          | IO                  | B16                     | G1                      |
| sdrc_d14                   | SDRAM data bit 14          | IO                  | A16                     | J3                      |
| sdrc_d15                   | SDRAM data bit 15          | IO                  | A15                     | J1                      |
| sdrc_d16                   | SDRAM data bit 16          | IO                  | A7                      | T3                      |
| sdrc_d17                   | SDRAM data bit 17          | IO                  | B7                      | U3                      |
| sdrc_d18                   | SDRAM data bit 18          | IO                  | D7                      | U4                      |
| sdrc_d19                   | SDRAM data bit 19          | IO                  | E7                      | V4                      |
| sdrc_d20                   | SDRAM data bit 20          | IO                  | C6                      | V1                      |
| sdrc_d21                   | SDRAM data bit 21          | IO                  | D6                      | V2                      |
| sdrc_d22                   | SDRAM data bit 22          | IO                  | B5                      | V5                      |
| sdrc_d23                   | SDRAM data bit 23          | IO                  | C5                      | V3                      |
| sdrc_d24                   | SDRAM data bit 24          | IO                  | B4                      | W3                      |
| sdrc_d25                   | SDRAM data bit 25          | IO                  | A3                      | W4                      |
| sdrc_d26                   | SDRAM data bit 26          | IO                  | B3                      | Y3                      |

**Table 4-5. External Memory Interfaces - SDRG Signals Description (continued)**

| <b>SIGNAL NAME</b> <sup>[1]</sup> | <b>DESCRIPTION</b> <sup>[2]</sup>            | <b>TYPE</b> <sup>[3]</sup> | <b>ZCN BALL</b> <sup>[4]</sup> | <b>ZER BALL</b> <sup>[4]</sup> |
|-----------------------------------|----------------------------------------------|----------------------------|--------------------------------|--------------------------------|
| sdrc_d27                          | SDRAM data bit 27                            | IO                         | C3                             | Y4                             |
| sdrc_d28                          | SDRAM data bit 28                            | IO                         | C2                             | AA2                            |
| sdrc_d29                          | SDRAM data bit 29                            | IO                         | D2                             | AA3                            |
| sdrc_d30                          | SDRAM data bit 30                            | IO                         | B1                             | AA4                            |
| sdrc_d31                          | SDRAM data bit 31                            | IO                         | C1                             | AB2                            |
| sdrc_ba0                          | SDRAM bank select 0                          | O                          | A12                            | L4                             |
| sdrc_ba1                          | SDRAM bank select 1                          | O                          | C13                            | K5                             |
| sdrc_ba2                          | SDRAM bank select 2                          | O                          | D13                            | J5                             |
| sdrc_a0                           | SDRAM address bit 0                          | O                          | A11                            | M3                             |
| sdrc_a1                           | SDRAM address bit 1                          | O                          | B11                            | M4                             |
| sdrc_a2                           | SDRAM address bit 2                          | O                          | C11                            | M5                             |
| sdrc_a3                           | SDRAM address bit 3                          | O                          | D11                            | N3                             |
| sdrc_a4                           | SDRAM address bit 4                          | O                          | E11                            | N2                             |
| sdrc_a5                           | SDRAM address bit 5                          | O                          | A10                            | N4                             |
| sdrc_a6                           | SDRAM address bit 6                          | O                          | B10                            | P3                             |
| sdrc_a7                           | SDRAM address bit 7                          | O                          | C10                            | P2                             |
| sdrc_a8                           | SDRAM address bit 8                          | O                          | D10                            | P1                             |
| sdrc_a9                           | SDRAM address bit 9                          | O                          | E10                            | P4                             |
| sdrc_a10                          | SDRAM address bit 10                         | O                          | A9                             | R1                             |
| sdrc_a11                          | SDRAM address bit 11                         | O                          | B9                             | R2                             |
| sdrc_a12                          | SDRAM address bit 12                         | O                          | A8                             | R3                             |
| sdrc_a13                          | SDRAM address bit 13                         | O                          | B8                             | R4                             |
| sdrc_a14                          | SDRAM address bit 14                         | O                          | D8                             | T2                             |
| sdrc_ncs0                         | Chip select 0                                | O                          | E13                            | J4                             |
| sdrc_ncs1                         | Chip select 1                                | O                          | A14                            | K4                             |
| sdrc_clk                          | Clock                                        | O                          | A13                            | L1                             |
| sdrc_nclk                         | Clock Invert                                 | O                          | B13                            | L2                             |
| sdrc_cke0                         | Clock Enable 0                               | O                          | D14                            | K3                             |
| sdrc_nras                         | SDRAM Row Access                             | O                          | C14                            | K1                             |
| sdrc_ncas                         | SDRAM column address strobe                  | O                          | E14                            | L3                             |
| sdrc_nwe                          | SDRAM write enable                           | O                          | B14                            | K2                             |
| sdrc_dm0                          | Data Mask 0                                  | O                          | C21                            | F4                             |
| sdrc_dm1                          | Data Mask 1                                  | O                          | B15                            | J2                             |
| sdrc_dm2                          | Data Mask 2                                  | O                          | E8                             | T4                             |
| sdrc_dm3                          | Data Mask 3                                  | O                          | D1                             | AB3                            |
| sdrc_strben0                      | PCB layout trace loop 0 pin 0                | A                          | A19                            | F2                             |
| sdrc_strben_dly0                  | PCB layout trace loop 0 pin 1                | A                          | A18                            | F1                             |
| sdrc_strben1                      | PCB layout trace loop 1 pin 0                | A                          | A5                             | W1                             |
| sdrc_strben_dly1                  | PCB layout trace loop 1 pin 1                | A                          | A4                             | W2                             |
| sdrc_odt                          | On-die termination output for sdrc_ncs0 only | O                          | C8                             | T1                             |
| sdrc_dqs0p                        | Data Strobe 0                                | IO                         | B20                            | E2                             |
| sdrc_dqs0n                        | Data Strobe 0                                | IO                         | A20                            | E1                             |
| sdrc_dqs1p                        | Data Strobe 1                                | IO                         | B17                            | H2                             |

**Table 4-5. External Memory Interfaces - SDR3 Signals Description (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                                                                                              | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|--------------------------------------------------------------------------------------------------------------|----------|--------------|--------------|
| sdrc_dqs1n      | Data Strobe 1                                                                                                | IO       | A17          | H1           |
| sdrc_dqs2p      | Data Strobe 2                                                                                                | IO       | A6           | U1           |
| sdrc_dqs2n      | Data Strobe 2                                                                                                | IO       | B6           | U2           |
| sdrc_dqs3p      | Data Strobe 3                                                                                                | IO       | A2           | Y1           |
| sdrc_dqs3n      | Data Strobe 3                                                                                                | IO       | B2           | Y2           |
| ddr_padref      | Impedance control for DDR2 output. This pin must be connected to ground via a 50-ohm ( $\pm 2\%$ ) resistor. | A        | B12          | M2           |
| VREFSSTL        | VREFSSTL is $.5 * V_{DDS} = 0.9V$ for DDR data PHY0 reference voltage input                                  | IO       | F14          | L5           |

#### 4.4.2 Video Interfaces

**Table 4-6. Video Interfaces - CCDC Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]      | TYPE [3] | ZCN BALL [4] | ZER BALL [4] | SYSTEM MUX MODE <sup>(1)</sup> |
|-----------------|----------------------|----------|--------------|--------------|--------------------------------|
| ccdc_pclk       | CCDC pixel clock     | IO       | AD2          | AB21         | mode0                          |
| ccdc_field      | CCDC field ID signal | IO       | AD1          | AA21         | mode0                          |
| ccdc_hd         | CCDC horizontal sync | IO       | AE2          | Y21          | mode0                          |
| ccdc_vd         | CCDC vertical sync   | IO       | AD3          | Y22          | mode0                          |
| ccdc_wen        | CCDC write enable    | I        | AE3          | W21          | mode0                          |
| ccdc_data0      | CCDC data bit 0      | I        | AD4          | W22          | mode0                          |
| ccdc_data1      | CCDC data bit 1      | I        | AE4          | W20          | mode0                          |
| ccdc_data2      | CCDC data bit 2      | I        | AC5          | V21          | mode0                          |
| ccdc_data3      | CCDC data bit 3      | I        | AD5          | V19          | mode0                          |
| ccdc_data4      | CCDC data bit 4      | I        | AE5          | V22          | mode0                          |
| ccdc_data5      | CCDC data bit 5      | I        | Y6           | U20          | mode0                          |
| ccdc_data6      | CCDC data bit 6      | I        | AB6          | V20          | mode0                          |
| ccdc_data7      | CCDC data bit 7      | I        | AC6          | U19          | mode0                          |
| ccdc_data8      | CCDC data bit 8      | I        | AE6          | U21          | mode1                          |
| ccdc_data9      | CCDC data bit 9      | I        | AD6          | U22          | mode1                          |
| ccdc_data10     | CCDC data bit 10     | I        | Y7           | T19          | mode1                          |
| ccdc_data11     | CCDC data bit 11     | I        | AA7          | T20          | mode1                          |
| ccdc_data12     | CCDC data bit 12     | I        | AB7          | T21          | mode1                          |
| ccdc_data13     | CCDC data bit 13     | I        | AC7          | R22          | mode1                          |
| ccdc_data14     | CCDC data bit 14     | I        | AD7          | T22          | mode1                          |
| ccdc_data15     | CCDC data bit 15     | I        | AE7          | R20          | mode1                          |

(1) See *Multiplexing Characteristics* table for more information.

**Table 4-7. Video Interfaces - DSS Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]                | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|--------------------------------|----------|--------------|--------------|
| dss_pclk        | LCD Pixel Clock                | O        | AE23         | B22          |
| dss_hsync       | LCD Horizontal Synchronization | O        | AD22         | B21          |
| dss_vsync       | LCD Vertical Synchronization   | O        | AD23         | B20          |

**Table 4-7. Video Interfaces - DSS Signals Description (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                                         | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|---------------------------------------------------------|----------|--------------|--------------|
| dss_acbias      | AC bias control (STN) or pixel data enable (TFT) output | O        | AE24         | B19          |
| dss_data0       | LCD Pixel Data bit 0                                    | IO       | AD24         | A20          |
| dss_data1       | LCD Pixel Data bit 1                                    | IO       | AD25         | A19          |
| dss_data2       | LCD Pixel Data bit 2                                    | IO       | AC23         | A18          |
| dss_data3       | LCD Pixel Data bit 3                                    | IO       | AC24         | B18          |
| dss_data4       | LCD Pixel Data bit 4                                    | IO       | AC25         | A17          |
| dss_data5       | LCD Pixel Data bit 5                                    | IO       | AB24         | C18          |
| dss_data6       | LCD Pixel Data bit 6                                    | IO       | AB25         | D17          |
| dss_data7       | LCD Pixel Data bit 7                                    | IO       | AA23         | B16          |
| dss_data8       | LCD Pixel Data bit 8                                    | IO       | AA24         | B17          |
| dss_data9       | LCD Pixel Data bit 9                                    | IO       | AA25         | C17          |
| dss_data10      | LCD Pixel Data bit 10                                   | IO       | Y22          | C16          |
| dss_data11      | LCD Pixel Data bit 11                                   | IO       | Y23          | D16          |
| dss_data12      | LCD Pixel Data bit 12                                   | IO       | Y24          | D14          |
| dss_data13      | LCD Pixel Data bit 13                                   | IO       | Y25          | A16          |
| dss_data14      | LCD Pixel Data bit 14                                   | IO       | W21          | D15          |
| dss_data15      | LCD Pixel Data bit 15                                   | IO       | W22          | B15          |
| dss_data16      | LCD Pixel Data bit 16                                   | IO       | W23          | A15          |
| dss_data17      | LCD Pixel Data bit 17                                   | IO       | W24          | A14          |
| dss_data18      | LCD Pixel Data bit 18                                   | IO       | W25          | C13          |
| dss_data19      | LCD Pixel Data bit 19                                   | IO       | V24          | C15          |
| dss_data20      | LCD Pixel Data bit 20                                   | O        | V25          | A13          |
| dss_data21      | LCD Pixel Data bit 21                                   | O        | U21          | B13          |
| dss_data22      | LCD Pixel Data bit 22                                   | O        | U22          | C14          |
| dss_data23      | LCD Pixel Data bit 23                                   | O        | U23          | B14          |

**Table 4-8. Video Interfaces – RFBI Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]           | TYPE [3] | ZCN BALL [4] | ZER BALL [4] | SUBSYSTEM PIN MULTIPLEXING [5] |
|-----------------|---------------------------|----------|--------------|--------------|--------------------------------|
| rfbi_a0         | RFBI command/data control | O        | AE24         | B19          | dss_acbias                     |
| rfbi_cs0        | 1st LCD chip select       | O        | AD22         | B21          | dss_hsync                      |
| rfbi_da0        | RFBI data bus 0           | IO       | AD24         | A20          | dss_data0                      |
| rfbi_da1        | RFBI data bus 1           | IO       | AD25         | A19          | dss_data1                      |
| rfbi_da2        | RFBI data bus 2           | IO       | AC23         | A18          | dss_data2                      |
| rfbi_da3        | RFBI data bus 3           | IO       | AC24         | B18          | dss_data3                      |
| rfbi_da4        | RFBI data bus 4           | IO       | AC25         | A17          | dss_data4                      |
| rfbi_da5        | RFBI data bus 5           | IO       | AB24         | C18          | dss_data5                      |
| rfbi_da6        | RFBI data bus 6           | IO       | AB25         | D17          | dss_data6                      |
| rfbi_da7        | RFBI data bus 7           | IO       | AA23         | B16          | dss_data7                      |
| rfbi_da8        | RFBI data bus 8           | IO       | AA24         | B17          | dss_data8                      |
| rfbi_da9        | RFBI data bus 9           | IO       | AA25         | C17          | dss_data9                      |
| rfbi_da10       | RFBI data bus 10          | IO       | Y22          | C16          | dss_data10                     |
| rfbi_da11       | RFBI data bus 11          | IO       | Y23          | D16          | dss_data11                     |
| rfbi_da12       | RFBI data bus 12          | IO       | Y24          | D14          | dss_data12                     |
| rfbi_da13       | RFBI data bus 13          | IO       | Y25          | A16          | dss_data13                     |

**Table 4-8. Video Interfaces – RFBI Signals Description (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                                     | TYPE [3] | ZCN BALL [4] | ZER BALL [4] | SUBSYSTEM PIN MULTIPLEXING [5] |
|-----------------|-----------------------------------------------------|----------|--------------|--------------|--------------------------------|
| rfb_da14        | RFBI data bus 14                                    | IO       | W21          | D15          | dss_data14                     |
| rfb_da15        | RFBI data bus 15                                    | IO       | W22          | B15          | dss_data15                     |
| rfb_rd          | Read enable for RFBI                                | O        | AE23         | B22          | dss_pclk                       |
| rfb_wr          | Write Enable for RFBI                               | O        | AD23         | B20          | dss_vsync                      |
| rfb_te_vsync0   | tearing effect removal and Vsync input from 1st LCD | I        | W23          | A15          | dss_data16                     |
| rfb_hsync0      | Hsync for 1st LCD                                   | I        | W24          | A14          | dss_data17                     |
| rfb_te_vsync1   | tearing effect removal and Vsync input from 2nd LCD | I        | W25          | C13          | dss_data18                     |
| rfb_hsync1      | Hsync for 2nd LCD                                   | I        | V24          | C15          | dss_data19                     |
| rfb_cs1         | 2nd LCD chip select                                 | O        | V25          | A13          | dss_data20                     |

**Table 4-9. Video Interfaces – TV Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]                                          | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|----------------------------------------------------------|----------|--------------|--------------|
| tv_out1         | TV analog output Composite: tv_out1                      | O        | K21          | NA           |
| tv_out2         | TV analog output S-VIDEO: tv_out2                        | O        | H24          | NA           |
| tv_vfb1         | tv_vfb1: Feedback through external resistor to composite | O        | K20          | NA           |
| tv_vfb2         | tv_vfb2: Feedback through external resistor to S-VIDEO   | O        | H23          | NA           |
| tv_vref         | External capacitor                                       | I        | H20          | NA           |

### 4.4.3 Serial Communication Interfaces

**Table 4-10. HDQ Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]                                                            | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|----------------------------------------------------------------------------|----------|--------------|--------------|
| hdq_sio         | Bidirectional HDQ 1-Wire control and data Interface. Output is open drain. | IO       | L25          | B9           |

**Table 4-11. Serial Communication Interfaces – I2C Signals Description (I2C1)**

| SIGNAL NAME [1] | DESCRIPTION [2]                                      | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|------------------------------------------------------|----------|--------------|--------------|
| i2c1_scl        | I2C Master Serial clock. Output is open drain.       | IOD      | V4           | AA17         |
| i2c1_sda        | I2C Serial Bidirectional Data. Output is open drain. | IOD      | V5           | AB17         |

**Table 4-12. Serial Communication Interfaces - I2C Signals Description (I2C2)**

| SIGNAL NAME [1] | DESCRIPTION [2]                                      | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|------------------------------------------------------|----------|--------------|--------------|
| i2c2_scl        | I2C Master Serial clock. Output is open drain.       | IOD      | W1           | Y17          |
| i2c2_sda        | I2C Serial Bidirectional Data. Output is open drain. | IOD      | W2           | Y16          |

**Table 4-13. Serial Communication Interfaces - I2C Signals Description (I2C3)**

| SIGNAL NAME [1] | DESCRIPTION [2]                                      | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|------------------------------------------------------|----------|--------------|--------------|
| i2c3_scl        | I2C Master Serial clock. Output is open drain.       | IOD      | W4           | W16          |
| i2c3_sda        | I2C Serial Bidirectional Data. Output is open drain. | IOD      | W5           | W17          |

**Table 4-14. Serial Communication Interfaces – McBSP LP Signals Description**

| SIGNAL NAME [1]                                       | DESCRIPTION [2]                                         | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-------------------------------------------------------|---------------------------------------------------------|----------|--------------|--------------|
| <b>MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 1)</b> |                                                         |          |              |              |
| mcbasp1_dr                                            | Received serial data                                    | I        | P23          | C9           |
| mcbasp1_clkr                                          | Receive Clock                                           | IO       | R25          | B11          |
| mcbasp1_fsr                                           | Receive frame synchronization                           | IO       | P21          | D11          |
| mcbasp1_dx                                            | Transmitted serial data                                 | IO       | P22          | C10          |
| mcbasp1_clkx                                          | Transmit clock                                          | IO       | N24          | C8           |
| mcbasp1_fsx                                           | Transmit frame synchronization                          | IO       | P24          | C11          |
| mcbasp_clks                                           | External clock input (shared by McBSP1, 2, 3, 4, and 5) | I        | P25          | E11          |
| <b>MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 2)</b> |                                                         |          |              |              |
| mcbasp2_dr                                            | Received serial data                                    | I        | B25          | C5           |
| mcbasp2_dx                                            | Transmitted serial data                                 | IO       | D24          | E4           |
| mcbasp2_clkx                                          | Combined serial clock                                   | IO       | C25          | D5           |
| mcbasp2_fsx                                           | Combined frame synchronization                          | IO       | D25          | E5           |
| <b>MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 3)</b> |                                                         |          |              |              |
| mcbasp3_dr                                            | Received serial data                                    | I        | C24          | B4           |
| mcbasp3_dx                                            | Transmitted serial data                                 | IO       | B24          | C4           |
| mcbasp3_clkx                                          | Combined serial clock                                   | IO       | A24          | D4           |
| mcbasp3_fsx                                           | Combined frame synchronization                          | IO       | C23          | A4           |
| <b>MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 4)</b> |                                                         |          |              |              |
| mcbasp4_dr                                            | Received serial data                                    | I        | A23          | B3           |
| mcbasp4_dx                                            | Transmitted serial data                                 | IO       | B22          | A2           |
| mcbasp4_clkx                                          | Combined serial clock                                   | IO       | B23          | A3           |
| mcbasp4_fsx                                           | Combined frame synchronization                          | IO       | A22          | B2           |
| <b>MULTICHANNEL BUFFERED SERIAL PORT (McBSP LP 5)</b> |                                                         |          |              |              |
| mcbasp5_dr                                            | Received serial data                                    | I        | Y18          | E19          |
| mcbasp5_dx                                            | Transmitted serial data                                 | IO       | AD19         | F19          |
| mcbasp5_clkx                                          | Combined serial clock                                   | IO       | AD17         | G22          |
| mcbasp5_fsx                                           | Combined frame synchronization                          | IO       | AE19         | F21          |

**Table 4-15. Serial Communication Interfaces – McSPI Signals Description**

| SIGNAL NAME [1]                                    | DESCRIPTION [2] | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|----------------------------------------------------|-----------------|----------|--------------|--------------|
| <b>MULTICHANNEL SERIAL PORT INTERFACE (McSPI1)</b> |                 |          |              |              |
| mcspi1_clk                                         | SPI Clock       | IO       | AE14         | K22          |

**Table 4-15. Serial Communication Interfaces – McSPI Signals Description (continued)**

| SIGNAL NAME [1]                                    | DESCRIPTION [2]                               | TYPE [3] | ZCN BALL [4]    | ZER BALL [4]       |
|----------------------------------------------------|-----------------------------------------------|----------|-----------------|--------------------|
| mcspi1_simo                                        | Slave data in, master data out                | IO       | AD15            | K19                |
| mcspi1_somi                                        | Slave data out, master data in                | IO       | AC15            | J18                |
| mcspi1_cs0                                         | SPI Enable 0, polarity configured by software | IO       | AB15            | K18                |
| mcspi1_cs1                                         | SPI Enable 1, polarity configured by software | O        | AD14            | J20                |
| mcspi1_cs2                                         | SPI Enable 2, polarity configured by software | O        | AE15            | J19                |
| mcspi1_cs3                                         | SPI Enable 3, polarity configured by software | O        | AE16            | J21                |
| <b>MULTICHANNEL SERIAL PORT INTERFACE (McSPI2)</b> |                                               |          |                 |                    |
| mcspi2_clk                                         | SPI Clock                                     | IO       | AD16,AC9        | J22                |
| mcspi2_simo                                        | Slave data in, master data out                | IO       | AC16,AD9        | H20                |
| mcspi2_somi                                        | Slave data out, master data in                | IO       | AB16,AE9        | H22                |
| mcspi2_cs0                                         | SPI Enable 0, polarity configured by software | IO       | AA16,AA10       | H21                |
| mcspi2_cs1                                         | SPI Enable 1, polarity configured by software | O        | AE17            | H19                |
| <b>MULTICHANNEL SERIAL PORT INTERFACE (McSPI3)</b> |                                               |          |                 |                    |
| mcspi3_clk                                         | SPI Clock                                     | IO       | W25,AD11,AA18   | C13, M21, G19, E20 |
| mcspi3_simo                                        | Slave data in, master data out                | IO       | V24,AE11,AD18   | C15, M20, G20      |
| mcspi3_somi                                        | Slave data out, master data in                | IO       | V25, AB12, AC18 | A13, K20, F22      |
| mcspi3_cs0                                         | SPI Enable 0, polarity configured by software | IO       | U21,AE12,AB18   | B13, K21, F20      |
| mcspi3_cs1                                         | SPI Enable 1, polarity configured by software | O        | U22, AD12, AB19 | C14, M18, E21      |
| <b>MULTICHANNEL SERIAL PORT INTERFACE (McSPI4)</b> |                                               |          |                 |                    |
| mcspi4_clk                                         | SPI Clock                                     | IO       | W20, R25        | C20, B11           |
| mcspi4_simo                                        | Slave data in, master data out                | IO       | P22             | C10                |
| mcspi4_somi                                        | Slave data out, master data in                | IO       | P23             | C9                 |
| mcspi4_cs0                                         | SPI Enable 0, polarity configured by software | IO       | P24             | C11                |

**Table 4-16. Serial Communication Interfaces – HECC Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]          | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|--------------------------|----------|--------------|--------------|
| hecc1_txd       | Transmit serial data pin | O        | V2           | AB15         |
| hecc1_rxd       | Receive serial data pin  | I        | V3           | AB16         |

**Table 4-17. Serial Communication Interfaces – EMAC (RMII) Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]         | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|-------------------------|----------|--------------|--------------|
| rmii_mdio_data  | Management data I/O     | IO       | AE6          | U21          |
| rmii_mdio_clk   | Management data clock   | O        | AD6          | U22          |
| rmii_rxd0       | EMAC receive data pin 0 | I        | Y7           | T19          |
| rmii_rxd1       | EMAC receive data pin 1 | I        | AA7          | T20          |

**Table 4-17. Serial Communication Interfaces – EMAC (RMII) Signals Description (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2]                       | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|---------------------------------------|----------|--------------|--------------|
| rmii_crs_dv     | EMAC carrier sense/receive data valid | I        | AB7          | T21          |
| rmii_rxer       | EMAC receive error                    | I        | AC7          | R22          |
| rmii_txd0       | EMAC transmit data pin 0              | O        | AD7          | T22          |
| rmii_txd1       | EMAC transmit data pin 1              | O        | AE7          | R20          |
| rmii_txen       | EMAC transmit enable                  | O        | AD8          | R19          |
| rmii_50mhz_clk  | EMAC RMII 50 MHz clock                | I        | AE8          | R21          |

**Table 4-18. Serial Communication Interfaces – UARTs Signals Description**

| SIGNAL NAME [1]                                                   | DESCRIPTION [2]                                 | TYPE [3] | ZCN BALL [4]    | ZER BALL [4]     |
|-------------------------------------------------------------------|-------------------------------------------------|----------|-----------------|------------------|
| <b>UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART1)</b>        |                                                 |          |                 |                  |
| uart1_cts                                                         | UART1 Clear To Send                             | I        | AD24,Y20,P25    | C19,A20,E11      |
| uart1_rts                                                         | UART1 Request To Send                           | O        | AD25,Y19        | C21,A19          |
| uart1_rx                                                          | UART1 Receive data                              | I        | AA23,W20,AC20   | C20,B16,E22      |
| uart1_tx                                                          | UART1 Transmit data                             | O        | AB25,AA19       | C22,D17          |
| <b>UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART2)</b>        |                                                 |          |                 |                  |
| uart2_cts                                                         | UART2 Clear To Send                             | I        | B24,F20         | A5,C4            |
| uart2_rts                                                         | UART2 Request To Send                           | O        | C24,F19         | B5,B4            |
| uart2_rx                                                          | UART2 Receive data                              | I        | C23,E23         | C6,A4            |
| uart2_tx                                                          | UART2 Transmit data                             | O        | A24,E24         | D6,D4            |
| <b>UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART3) / IrDA</b> |                                                 |          |                 |                  |
| uart3_cts_rctx                                                    | UART3 Clear To Send (input), Remote TX (output) | IO       | U1,N2           | W15,V14          |
| uart3_rts_sd                                                      | UART3 Request To Send , IR enable               | O        | N3,V3           | W13AB16          |
| uart3_rx_irrx                                                     | UART3 Receive data , IR and Remote RX           | I        | AC25,P1,F25,V2  | AA13,A17,A6,AB15 |
| uart3_tx_irtx                                                     | UART3 Transmit data , IR TX                     | O        | AB24,P2,F24,E25 | Y13,C18,B6,A7    |
| <b>UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER (UART4)</b>        |                                                 |          |                 |                  |
| uart4_cts                                                         | UART4 Clear To Send                             | I        | AD3,AD11        | Y22,M21          |
| uart4_rts                                                         | UART4 Request To Send                           | O        | AE2,AE11        | Y21,M20          |
| uart4_rx                                                          | UART4 Receive data                              | I        | T5,AE3,AC12     | Y14,W21,L19      |
| uart4_tx                                                          | UART4 Transmit data                             | O        | T4,AD1,AB12     | AA16,AA21,K20    |

**Table 4-19. Serial Communication Interfaces – USB Signals Description**

| SIGNAL NAME [1]                              | DESCRIPTION [2]                           | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|----------------------------------------------|-------------------------------------------|----------|--------------|--------------|
| <b>UNIVERSAL SERIAL BUS INTERFACE (USB0)</b> |                                           |          |              |              |
| usb0_dp                                      | USB D+ (differential signal pair)         | A        | F25          | A6           |
| usb0_dm                                      | USB D- (differential signal pair)         | A        | F24          | B6           |
| usb0_drvvbus                                 | Digital output to control external supply | O        | E25          | A7           |
| usb0_id                                      | USB operating mode identification pin     | A        | G25          | B7           |

**Table 4-19. Serial Communication Interfaces – USB Signals Description (continued)**

| <b>SIGNAL NAME [1]</b> | <b>DESCRIPTION [2]</b>                                                                                                                                                                                    | <b>TYPE [3]</b> | <b>ZCN BALL [4]</b> | <b>ZER BALL [4]</b> |
|------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|---------------------|---------------------|
| usb0_vbus              | For host or device mode operation, tie the VBUS/USB power signal to the USB connector. When used in OTG mode operation, tie VBUS to the external charge pump and to the VBUS signal on the USB connector. | A               | G24                 | C7                  |
| <b>MM_FSUSB3</b>       |                                                                                                                                                                                                           |                 |                     |                     |
| mm_fsusb3_rxdm         | Vminus receive data (not used in 3- or 4-pin configurations)                                                                                                                                              | IO              | AE13                | M19                 |
| mm_fsusb3_rxdp         | Vplus receive data (not used in 3- or 4-pin configurations)                                                                                                                                               | IO              | AC13                | L20                 |
| mm_fsusb3_rxrcv        | Differential receiver signal input (not used in 3-pin mode)                                                                                                                                               | IO              | A23                 | B3                  |
| mm_fsusb3_txse0        | Single-ended zero. Used as VM in 4-pin VP_VM mode.                                                                                                                                                        | IO              | B23                 | A3                  |
| mm_fsusb3_txdm         | USB data. Used as VP in 4-pin VP_VM mode.                                                                                                                                                                 | IO              | B22                 | A2                  |
| mm_fsusb3_txen_n       | Transmit enable                                                                                                                                                                                           | IO              | A22                 | B2                  |
| <b>MM_FSUSB2</b>       |                                                                                                                                                                                                           |                 |                     |                     |
| mm_fsusb2_rxdm         | Vminus receive data (not used in 3- or 4-pin configurations)                                                                                                                                              | IO              | AD21                | D20                 |
| mm_fsusb2_rxdp         | Vplus receive data (not used in 3- or 4-pin configurations)                                                                                                                                               | IO              | AB20                | E20                 |
| mm_fsusb2_rxrcv        | Differential receiver signal input (not used in 3-pin mode)                                                                                                                                               | IO              | AC21                | D19                 |
| mm_fsusb2_txse0        | Single-ended zero. Used as VM in 4-pin VP_VM mode.                                                                                                                                                        | IO              | AE22                | D18                 |
| mm_fsusb2_txdm         | USB data. Used as VP in 4-pin VP_VM mode.                                                                                                                                                                 | IO              | AE16                | J21                 |
| mm_fsusb2_txen_n       | Transmit enable                                                                                                                                                                                           | IO              | AE17                | H19                 |
| <b>MM_FSUSB1</b>       |                                                                                                                                                                                                           |                 |                     |                     |
| mm_fsusb1_rxdm         | Vminus receive data (not used in 3- or 4-pin configurations)                                                                                                                                              | IO              | AD20                | D21                 |
| mm_fsusb1_rxdp         | Vplus receive data (not used in 3- or 4-pin configurations)                                                                                                                                               | IO              | AE18                | G21                 |
| mm_fsusb1_rxrcv        | Differential receiver signal input (not used in 3-pin mode)                                                                                                                                               | IO              | AD18                | G20                 |
| mm_fsusb1_txse0        | Single-ended zero. Used as VM in 4-pin VP_VM mode.                                                                                                                                                        | IO              | AC18                | F22                 |
| mm_fsusb1_txdm         | USB data. Used as VP in 4-pin VP_VM mode.                                                                                                                                                                 | IO              | AB18                | F20                 |
| mm_fsusb1_txen_n       | Transmit enable                                                                                                                                                                                           | IO              | AB19                | E21                 |
| <b>HSUSB2</b>          |                                                                                                                                                                                                           |                 |                     |                     |

**Table 4-19. Serial Communication Interfaces – USB Signals Description (continued)**

| <b>SIGNAL NAME [1]</b> | <b>DESCRIPTION [2]</b>                                                                                  | <b>TYPE [3]</b> | <b>ZCN BALL [4]</b> | <b>ZER BALL [4]</b> |
|------------------------|---------------------------------------------------------------------------------------------------------|-----------------|---------------------|---------------------|
| hsusb2_clk             | Dedicated for external transceiver 60-MHz clock input from PHY                                          | O               | AC20                | E22                 |
| hsusb2_stp             | Dedicated for external transceiver Stop signal                                                          | O               | AB20                | E20                 |
| hsusb2_dir             | Dedicated for external transceiver Data direction control from PHY                                      | I               | AE21                | E18                 |
| hsusb2_nxt             | Dedicated for external transceiver Next signal from PHY                                                 | I               | AD21                | D20                 |
| hsusb2_data0           | Dedicated for external transceiver Bidirectional data bus                                               | IO              | AC21                | D19                 |
| hsusb2_data1           | Dedicated for external transceiver Bidirectional data bus                                               | IO              | AE22                | D18                 |
| hsusb2_data2           | Dedicated for external transceiver Bidirectional data bus                                               | IO              | AE16                | J21                 |
| hsusb2_data3           | Dedicated for external transceiver Bidirectional data bus                                               | IO              | AE17                | H19                 |
| hsusb2_data4           | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation. | IO              | AC16                | H20                 |
| hsusb2_data5           | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation. | IO              | AB16                | H22                 |
| hsusb2_data6           | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation. | IO              | AA16                | H21                 |
| hsusb2_data7           | Dedicated for external transceiver Bidirectional data bus                                               | IO              | AD16                | J22                 |
| <b>HSUSB1</b>          |                                                                                                         |                 |                     |                     |
| hsusb1_clk             | Dedicated for external transceiver 60-MHz clock input from PHY                                          | O               | AE18                | G21                 |
| hsusb1_stp             | Dedicated for external transceiver Stop signal                                                          | O               | AD17                | G22                 |
| hsusb1_dir             | Dedicated for external transceiver Data direction control from PHY                                      | I               | AE20                | D22                 |
| hsusb1_nxt             | Dedicated for external transceiver Next signal from PHY                                                 | I               | AD20                | D21                 |
| hsusb1_data0           | Dedicated for external transceiver Bidirectional data bus                                               | IO              | AD18                | G20                 |
| hsusb1_data1           | Dedicated for external transceiver Bidirectional data bus                                               | IO              | AC18                | F22                 |
| hsusb1_data2           | Dedicated for external transceiver Bidirectional data bus                                               | IO              | AB18                | F20                 |

**Table 4-19. Serial Communication Interfaces – USB Signals Description (continued)**

| <b>SIGNAL NAME [1]</b> | <b>DESCRIPTION [2]</b>                                                                                 | <b>TYPE [3]</b> | <b>ZCN BALL [4]</b> | <b>ZER BALL [4]</b> |
|------------------------|--------------------------------------------------------------------------------------------------------|-----------------|---------------------|---------------------|
| hsusb1_data3           | Dedicated for external transceiver Bidirectional data bus                                              | IO              | AB19                | E21                 |
| hsusb1_data4           | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO              | Y18                 | E19                 |
| hsusb1_data5           | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO              | AE19                | F21                 |
| hsusb1_data6           | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO              | AD19                | F19                 |
| hsusb1_data7           | Dedicated for external transceiver Bidirectional data bus additional signals for 12-pin ULPI operation | IO              | AA18                | G19                 |

#### 4.4.4 Removable Media Interfaces

**Table 4-20. Removable Media Interfaces – MMC/SDIO Signals Description**

| <b>SIGNAL NAME [1]</b>                                           | <b>DESCRIPTION [2]</b>                                                                     | <b>TYPE [3]</b> | <b>ZCN BALL [4]</b> | <b>ZER BALL [4]</b> |
|------------------------------------------------------------------|--------------------------------------------------------------------------------------------|-----------------|---------------------|---------------------|
| <b>MULTIMEDIA MEMORY CARD (MMC1) / SECURE DIGITAL IO (SDIO1)</b> |                                                                                            |                 |                     |                     |
| mmc1_clk                                                         | MMC/SD Output Clock                                                                        | O               | AA9                 | P22                 |
| mmc1_cmd                                                         | MMC/SD command signal                                                                      | IO              | AB9                 | N21                 |
| mmc1_dat0                                                        | MMC/SD Card Data bit 0 / SPI Serial Input                                                  | IO              | AC9                 | P21                 |
| mmc1_dat1                                                        | MMC/SD Card Data bit 1                                                                     | IO              | AD9                 | N20                 |
| mmc1_dat2                                                        | MMC/SD Card Data bit 2                                                                     | IO              | AE9                 | P19                 |
| mmc1_dat3                                                        | MMC/SD Card Data bit 3                                                                     | IO              | AA10                | P20                 |
| mmc1_dat4                                                        | MMC/SD Card Data bit 4                                                                     | IO              | AB10                | N22                 |
| mmc1_dat5                                                        | MMC/SD Card Data bit 5                                                                     | IO              | AC10                | N19                 |
| mmc1_dat6                                                        | MMC/SD Card Data bit 6                                                                     | IO              | AD10                | N18                 |
| mmc1_dat7                                                        | MMC/SD Card Data bit 7                                                                     | IO              | AE10                | P18                 |
| <b>MULTIMEDIA MEMORY CARD (MMC2) / SECURE DIGITAL IO (SDIO2)</b> |                                                                                            |                 |                     |                     |
| mmc2_clk                                                         | MMC/SD Output Clock                                                                        | O               | AD11                | M21                 |
| mmc2_dir_dat0                                                    | Direction control for DAT0 signal case an external transceiver used                        | O               | AB13                | L18                 |
| mmc2_dir_dat1                                                    | Direction control for DAT1 and DAT3 signals case an external transceiver used              | O               | AC13                | L20                 |
| mmc2_dir_dat2                                                    | Direction control for DAT2 signal case an external transceiver used                        | O               | AB1                 | V18                 |
| mmc2_dir_dat3                                                    | Direction control for DAT4, DAT5, DAT6, and DAT7 signals case an external transceiver used | O               | AB2                 | Y19                 |
| mmc2_clkin                                                       | MMC/SD input clock                                                                         | I               | AE13                | NA                  |
| mmc2_dat0                                                        | MMC/SD Card Data bit 0                                                                     | IO              | AB12                | K20                 |
| mmc2_dat1                                                        | MMC/SD Card Data bit 1                                                                     | IO              | AC12                | L19                 |
| mmc2_dat2                                                        | MMC/SD Card Data bit 2                                                                     | IO              | AD12                | M18                 |

**Table 4-20. Removable Media Interfaces – MMC/SDIO Signals Description (continued)**

| <b>SIGNAL NAME [1]</b>                                           | <b>DESCRIPTION [2]</b>                                                | <b>TYPE [3]</b> | <b>ZCN BALL [4]</b> | <b>ZER BALL [4]</b> |
|------------------------------------------------------------------|-----------------------------------------------------------------------|-----------------|---------------------|---------------------|
| mmc2_dat3                                                        | MMC/SD Card Data bit 3                                                | IO              | AE12                | K21                 |
| mmc2_dat4                                                        | MMC/SD Card Data bit 4                                                | IO              | AB13                | L18                 |
| mmc2_dat5                                                        | MMC/SD Card Data bit 5                                                | IO              | AC13                | L20                 |
| mmc2_dat6                                                        | MMC/SD Card Data bit 6                                                | IO              | AD13                | L21                 |
| mmc2_dat7                                                        | MMC/SD Card Data bit 7                                                | IO              | AE13                | M19                 |
| mmc2_dir_cmd                                                     | Direction control for CMD signal case an external transceiver is used | O               | AD13                | NA                  |
| mmc2_cmd                                                         | MMC/SD command signal                                                 | IO              | AE11                | M20                 |
| <b>MULTIMEDIA MEMORY CARD (MMC3) / SECURE DIGITAL IO (SDIO3)</b> |                                                                       |                 |                     |                     |
| mmc3_clk                                                         | MMC/SD Output Clock                                                   | O               | AE15,AD17           | J19,G22             |
| mmc3_cmd                                                         | MMC/SD command signal                                                 | IO              | AD14,AE18           | J20,G21             |
| mmc3_dat0                                                        | MMC/SD Card Data bit 0 / SPI Serial Input                             | IO              | AB13,Y18            | E19,L18             |
| mmc3_dat1                                                        | MMC/SD Card Data bit 1                                                | IO              | AC13,AE19           | L20,F21             |
| mmc3_dat2                                                        | MMC/SD Card Data bit 2                                                | IO              | AD13,AD19           | L21,F19             |
| mmc3_dat3                                                        | MMC/SD Card Data bit 3                                                | IO              | AE13,AA18           | M19,G19             |
| mmc3_dat4                                                        | MMC/SD Card Data bit 4                                                | IO              | AD18                | G20                 |
| mmc3_dat5                                                        | MMC/SD Card Data bit 5                                                | IO              | AD20                | D21                 |
| mmc3_dat6                                                        | MMC/SD Card Data bit 6                                                | IO              | AE20                | D22                 |
| mmc3_dat7                                                        | MMC/SD Card Data bit 7                                                | IO              | AB19                | E21                 |

#### 4.4.5 Test Interfaces

**Table 4-21. Test Interfaces – ETK Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| etk_ctl         | ETK trace ctl   | O        | AE18         | G21          |
| etk_clk         | ETK trace clock | O        | AD17         | G22          |
| etk_d0          | ETK data 0      | O        | AD18         | G20          |
| etk_d1          | ETK data 1      | O        | AC18         | F22          |
| etk_d2          | ETK data 2      | O        | AB18         | F20          |
| etk_d3          | ETK data 3      | O        | AA18         | G19          |
| etk_d4          | ETK data 4      | O        | Y18          | E19          |
| etk_d5          | ETK data 5      | O        | AE19         | F21          |
| etk_d6          | ETK data 6      | O        | AD19         | F19          |
| etk_d7          | ETK data 7      | O        | AB19         | E21          |
| etk_d8          | ETK data 8      | O        | AE20         | D22          |
| etk_d9          | ETK data 9      | O        | AD20         | D21          |
| etk_d10         | ETK data 10     | O        | AC20         | E22          |
| etk_d11         | ETK data 11     | O        | AB20         | E20          |
| etk_d12         | ETK data 12     | O        | AE21         | E18          |
| etk_d13         | ETK data 13     | O        | AD21         | D20          |
| etk_d14         | ETK data 14     | O        | AC21         | D19          |
| etk_d15         | ETK data 15     | O        | AE22         | D18          |

**Table 4-22. Test Interfaces – JTAG Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]     | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|---------------------|----------|--------------|--------------|
| jtag_nrst       | Test Reset          | I        | U24          | D13          |
| jtag_tck        | Test Clock          | I        | U25          | E14          |
| jtag_rtck       | ARM Clock Emulation | O        | T21          | C12          |
| jtag_tms_tmsc   | Test Mode Select    | IO       | T22          | A12          |
| jtag_tdi        | Test Data Input     | I        | T23          | B12          |
| jtag_tdo        | Test Data Output    | O        | T24          | D12          |
| jtag_emu0       | Test emulation 0    | IO       | T25          | E13          |
| jtag_emu1       | Test emulation 1    | IO       | R24          | E12          |

**Table 4-23. Test Interfaces – HWDBG Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| hw_dbg0         | Debug signal 0  | O        | AD2,AD17     | G22          |
| hw_dbg1         | Debug signal 1  | O        | AD1,AE18     | G21          |
| hw_dbg2         | Debug signal 2  | O        | AD3,AD18     | G20          |
| hw_dbg3         | Debug signal 3  | O        | AE3,AC18     | F22          |
| hw_dbg4         | Debug signal 4  | O        | AC5,AB18     | F20          |
| hw_dbg5         | Debug signal 5  | O        | AD5,AA18     | G19          |
| hw_dbg6         | Debug signal 6  | O        | Y18,AE5      | E19          |
| hw_dbg7         | Debug signal 7  | O        | Y6,AE19      | F21          |
| hw_dbg8         | Debug signal 8  | O        | Y7,AD19      | F19          |
| hw_dbg9         | Debug signal 9  | O        | AA7,AB19     | E21          |
| hw_dbg10        | Debug signal 10 | O        | AC7,AE20     | D22          |
| hw_dbg11        | Debug signal 11 | O        | AD7,AD20     | D21          |
| hw_dbg12        | Debug signal 12 | O        | AE23,AC20    | E22          |

**Table 4-23. Test Interfaces – HWDBG Signals Description (continued)**

| SIGNAL NAME [1] | DESCRIPTION [2] | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|-----------------|----------|--------------|--------------|
| hw_dbg13        | Debug signal 13 | O        | AD22,AB20    | E20          |
| hw_dbg14        | Debug signal 14 | O        | AB25,AE21    | E18          |
| hw_dbg15        | Debug signal 15 | O        | AA23,AD21    | D20          |
| hw_dbg16        | Debug signal 16 | O        | AA24,AC21    | D19          |
| hw_dbg17        | Debug signal 17 | O        | AA25,AE22    | D18          |

#### 4.4.6 Miscellaneous

**Table 4-24. Miscellaneous – GP Timer Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]              | TYPE [3] | ZCN BALL [4]   | ZER BALL [4]    |
|-----------------|------------------------------|----------|----------------|-----------------|
| gpt8_pwm_evt    | PWM or event for GP timer 8  | IO       | N4,E23,AE17    | V11,C6,H19      |
| gpt9_pwm_evt    | PWM or event for GP timer 9  | IO       | M4,M2,F20,AC16 | Y12,AA11,A5,H20 |
| gpt10_pwm_evt   | PWM or event for GP timer 10 | IO       | M3,M1,F19,AB16 | V12,W12,B5,H22  |
| gpt11_pwm_evt   | PWM or event for GP timer 11 | IO       | N5,E24,AA16    | AA12,D6,H21     |

#### 4.4.7 General-Purpose IOs

**Table 4-25. General-Purpose IOs Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]       | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|-----------------------|----------|--------------|--------------|
| gpio_0          | General-purpose IO 0  | IO       | Y1           | AB18         |
| gpio_1          | General-purpose IO 1  | IO       | M24          | B8           |
| gpio_2          | General-purpose IO 2  | IO       | Y4           | AB19         |
| gpio_3          | General-purpose IO 3  | IO       | AA1          | AB20         |
| gpio_4          | General-purpose IO 4  | IO       | AA2          | W18          |
| gpio_5          | General-purpose IO 5  | IO       | AA3          | AA19         |
| gpio_6          | General-purpose IO 6  | IO       | AB1          | V18          |
| gpio_7          | General-purpose IO 7  | IO       | AB2          | Y19          |
| gpio_8          | General-purpose IO 8  | IO       | AC1          | W19          |
| gpio_10         | General-purpose IO 10 | IO       | N25          | E9           |
| gpio_11         | General-purpose IO 11 | IO       | T25          | E13          |
| gpio_12         | General-purpose IO 12 | IO       | AD17         | G22          |
| gpio_13         | General-purpose IO 13 | IO       | AE18         | G21          |
| gpio_14         | General-purpose IO 14 | IO       | AD18         | G20          |
| gpio_15         | General-purpose IO 15 | IO       | AC18         | F22          |
| gpio_16         | General-purpose IO 16 | IO       | AB18         | F20          |
| gpio_17         | General-purpose IO 17 | IO       | AA18         | G19          |
| gpio_18         | General-purpose IO 18 | IO       | Y18          | E19          |
| gpio_19         | General-purpose IO 19 | IO       | AE19         | F21          |
| gpio_20         | General-purpose IO 20 | IO       | AD19         | F19          |
| gpio_21         | General-purpose IO 21 | IO       | AB19         | E21          |
| gpio_22         | General-purpose IO 22 | IO       | AE20         | D22          |
| gpio_23         | General-purpose IO 23 | IO       | AD20         | D21          |
| gpio_24         | General-purpose IO 24 | IO       | AC20         | E22          |
| gpio_25         | General-purpose IO 25 | IO       | AB20         | E20          |
| gpio_26         | General-purpose IO 26 | IO       | AE21         | E18          |
| gpio_27         | General-purpose IO 27 | IO       | AD21         | D20          |
| gpio_28         | General-purpose IO 28 | IO       | AC21         | D19          |
| gpio_29         | General-purpose IO 29 | IO       | AE22         | D18          |
| gpio_30         | General-purpose IO 30 | IO       | Y3           | Y18          |
| gpio_31         | General-purpose IO 31 | IO       | R24          | E12          |
| gpio_34         | General-purpose IO 34 | IO       | E3           | W5           |
| gpio_35         | General-purpose IO 35 | IO       | E2           | Y5           |
| gpio_36         | General-purpose IO 36 | IO       | E1           | AB4          |
| gpio_37         | General-purpose IO 37 | IO       | F7           | AA5          |
| gpio_38         | General-purpose IO 38 | IO       | F6           | AB5          |
| gpio_39         | General-purpose IO 39 | IO       | F4           | AB6          |
| gpio_40         | General-purpose IO 40 | IO       | F3           | AA6          |
| gpio_41         | General-purpose IO 41 | IO       | F2           | W6           |
| gpio_42         | General-purpose IO 42 | IO       | F1           | AB7          |
| gpio_43         | General-purpose IO 43 | IO       | G6           | Y6           |
| gpio_44         | General-purpose IO 44 | IO       | J4           | W10          |
| gpio_45         | General-purpose IO 45 | IO       | J3           | AB9          |
| gpio_46         | General-purpose IO 46 | IO       | J2           | AB10         |
| gpio_47         | General-purpose IO 47 | IO       | J1           | W9           |

**Table 4-25. General-Purpose IOs Signals Description (continued)**

| <b>SIGNAL NAME [1]</b> | <b>DESCRIPTION [2]</b> | <b>TYPE [3]</b> | <b>ZCN BALL [4]</b> | <b>ZER BALL [4]</b> |
|------------------------|------------------------|-----------------|---------------------|---------------------|
| gpio_48                | General-purpose IO 48  | IO              | K4                  | AA10                |
| gpio_49                | General-purpose IO 49  | IO              | K3                  | Y9                  |
| gpio_50                | General-purpose IO 50  | IO              | K2                  | V10                 |
| gpio_51                | General-purpose IO 51  | IO              | K1                  | V9                  |
| gpio_52                | General-purpose IO 52  | IO              | L1                  | Y11                 |
| gpio_53                | General-purpose IO 53  | IO              | M4                  | Y12                 |
| gpio_54                | General-purpose IO 54  | IO              | M3                  | V12                 |
| gpio_55                | General-purpose IO 55  | IO              | M2                  | AA11                |
| gpio_56                | General-purpose IO 56  | IO              | M1                  | W12                 |
| gpio_57                | General-purpose IO 57  | IO              | N5                  | AA12                |
| gpio_58                | General-purpose IO 58  | IO              | N4                  | V11                 |
| gpio_59                | General-purpose IO 59  | IO              | N1                  | AB13                |
| gpio_60                | General-purpose IO 60  | IO              | R4                  | W11                 |
| gpio_61                | General-purpose IO 61  | IO              | T1                  | Y15                 |
| gpio_62                | General-purpose IO 62  | IO              | T2                  | W14                 |
| gpio_63                | General-purpose IO 63  | IO              | T4                  | AA16                |
| gpio_64                | General-purpose IO 64  | IO              | T5                  | Y14                 |
| gpio_65                | General-purpose IO 65  | IO              | U1                  | V14                 |
| gpio_66                | General-purpose IO 66  | IO              | AE23                | B22                 |
| gpio_67                | General-purpose IO 67  | IO              | AD22                | B21                 |
| gpio_68                | General-purpose IO 68  | IO              | AD23                | B20                 |
| gpio_69                | General-purpose IO 69  | IO              | AE24                | B19                 |
| gpio_70                | General-purpose IO 70  | IO              | AD24                | A20                 |
| gpio_71                | General-purpose IO 71  | IO              | AD25                | A19                 |
| gpio_72                | General-purpose IO 72  | IO              | AC23                | A18                 |
| gpio_73                | General-purpose IO 73  | IO              | AC24                | B18                 |
| gpio_74                | General-purpose IO 74  | IO              | AC25                | A17                 |
| gpio_75                | General-purpose IO 75  | IO              | AB24                | C18                 |
| gpio_76                | General-purpose IO 76  | IO              | AB25                | D17                 |
| gpio_77                | General-purpose IO 77  | IO              | AA23                | B16                 |
| gpio_78                | General-purpose IO 78  | IO              | AA24                | B17                 |
| gpio_79                | General-purpose IO 79  | IO              | AA25                | C17                 |
| gpio_80                | General-purpose IO 80  | IO              | Y22                 | C16                 |
| gpio_81                | General-purpose IO 81  | IO              | Y23                 | D16                 |
| gpio_82                | General-purpose IO 82  | IO              | Y24                 | D14                 |
| gpio_83                | General-purpose IO 83  | IO              | Y25                 | A16                 |
| gpio_84                | General-purpose IO 84  | IO              | W21                 | D15                 |
| gpio_85                | General-purpose IO 85  | IO              | W22                 | B15                 |
| gpio_86                | General-purpose IO 86  | IO              | W23                 | A15                 |
| gpio_87                | General-purpose IO 87  | IO              | W24                 | A14                 |
| gpio_88                | General-purpose IO 88  | IO              | W25                 | C13                 |
| gpio_89                | General-purpose IO 89  | IO              | V24                 | C15                 |
| gpio_90                | General-purpose IO 90  | IO              | V25                 | A13                 |
| gpio_91                | General-purpose IO 91  | IO              | U21                 | B13                 |
| gpio_92                | General-purpose IO 92  | IO              | U22                 | C14                 |
| gpio_93                | General-purpose IO 93  | IO              | U23                 | B14                 |
| gpio_94                | General-purpose IO 94  | IO              | AD2                 | AB21                |

**Table 4-25. General-Purpose IOs Signals Description (continued)**

| <b>SIGNAL NAME [1]</b> | <b>DESCRIPTION [2]</b> | <b>TYPE [3]</b> | <b>ZCN BALL [4]</b> | <b>ZER BALL [4]</b> |
|------------------------|------------------------|-----------------|---------------------|---------------------|
| gpio_95                | General-purpose IO 95  | IO              | AD1                 | AA21                |
| gpio_96                | General-purpose IO 96  | IO              | AE2                 | Y21                 |
| gpio_97                | General-purpose IO 97  | IO              | AD3                 | Y22                 |
| gpio_98                | General-purpose IO 98  | IO              | AE3                 | W21                 |
| gpio_99                | General-purpose IO 99  | I               | AD4                 | W22                 |
| gpio_100               | General-purpose IO 100 | I               | AE4                 | W20                 |
| gpio_101               | General-purpose IO 101 | IO              | AC5                 | V21                 |
| gpio_102               | General-purpose IO 102 | IO              | AD5                 | V19                 |
| gpio_103               | General-purpose IO 103 | IO              | AE5                 | V22                 |
| gpio_104               | General-purpose IO 104 | IO              | Y6                  | U20                 |
| gpio_105               | General-purpose IO 105 | IO              | AB6                 | V20                 |
| gpio_106               | General-purpose IO 106 | IO              | AC6                 | U19                 |
| gpio_107               | General-purpose IO 107 | IO              | AE6                 | U21                 |
| gpio_108               | General-purpose IO 108 | IO              | AD6                 | U22                 |
| gpio_109               | General-purpose IO 109 | IO              | Y7                  | T19                 |
| gpio_110               | General-purpose IO 110 | IO              | AA7                 | T20                 |
| gpio_111               | General-purpose IO 111 | IO              | AB7                 | T21                 |
| gpio_112               | General-purpose IO 112 | I               | AE7                 | R20                 |
| gpio_113               | General-purpose IO 113 | I               | AD8                 | R19                 |
| gpio_114               | General-purpose IO 114 | I               | AE8                 | R21                 |
| gpio_116               | General-purpose IO 116 | IO              | D25                 | E5                  |
| gpio_117               | General-purpose IO 117 | IO              | C25                 | D5                  |
| gpio_118               | General-purpose IO 118 | IO              | B25                 | C5                  |
| gpio_119               | General-purpose IO 119 | IO              | D24                 | E4                  |
| gpio_120               | General-purpose IO 120 | IO              | AA9                 | P22                 |
| gpio_121               | General-purpose IO 121 | IO              | AB9                 | N21                 |
| gpio_122               | General-purpose IO 122 | IO              | AC9                 | P21                 |
| gpio_123               | General-purpose IO 123 | IO              | AD9                 | N20                 |
| gpio_124               | General-purpose IO 124 | IO              | AE9                 | P19                 |
| gpio_125               | General-purpose IO 125 | IO              | E25, AA10           | A7, P20             |
| gpio_126               | General-purpose IO 126 | IO              | AB10, AD7           | N22, T22            |
| gpio_127               | General-purpose IO 127 | IO              | AC10                | N19                 |
| gpio_128               | General-purpose IO 128 | IO              | AD10                | N18                 |
| gpio_129               | General-purpose IO 129 | IO              | AE10                | P18                 |
| gpio_130               | General-purpose IO 130 | IO              | V2, AD11            | M21, AB15           |
| gpio_131               | General-purpose IO 131 | IO              | V3, AE11            | M20, AB16           |
| gpio_132               | General-purpose IO 132 | IO              | AB12                | K20                 |
| gpio_133               | General-purpose IO 133 | IO              | AC12                | L19                 |
| gpio_134               | General-purpose IO 134 | IO              | AD12                | M18                 |
| gpio_135               | General-purpose IO 135 | IO              | AE12                | K21                 |
| gpio_136               | General-purpose IO 136 | IO              | AB13                | L18                 |
| gpio_137               | General-purpose IO 137 | IO              | AC13                | L20                 |
| gpio_138               | General-purpose IO 138 | IO              | AD13                | L21                 |
| gpio_139               | General-purpose IO 139 | IO              | AE13                | M19                 |
| gpio_140               | General-purpose IO 140 | IO              | B24                 | C4                  |
| gpio_141               | General-purpose IO 141 | IO              | C24                 | B4                  |
| gpio_142               | General-purpose IO 142 | IO              | A24                 | D4                  |

**Table 4-25. General-Purpose IOs Signals Description (continued)**

| <b>SIGNAL NAME [1]</b> | <b>DESCRIPTION [2]</b> | <b>TYPE [3]</b> | <b>ZCN BALL [4]</b> | <b>ZER BALL [4]</b> |
|------------------------|------------------------|-----------------|---------------------|---------------------|
| gpio_143               | General-purpose IO 143 | IO              | C23                 | A4                  |
| gpio_144               | General-purpose IO 144 | IO              | F20                 | A5                  |
| gpio_145               | General-purpose IO 145 | IO              | F19                 | B5                  |
| gpio_146               | General-purpose IO 146 | IO              | E24                 | D6                  |
| gpio_147               | General-purpose IO 147 | IO              | E23                 | C6                  |
| gpio_148               | General-purpose IO 148 | IO              | AA19                | C22                 |
| gpio_149               | General-purpose IO 149 | IO              | Y19                 | C21                 |
| gpio_150               | General-purpose IO 150 | IO              | Y20                 | C19                 |
| gpio_151               | General-purpose IO 151 | IO              | W20                 | C20                 |
| gpio_152               | General-purpose IO 152 | IO              | B23                 | A3                  |
| gpio_153               | General-purpose IO 153 | IO              | A23                 | B3                  |
| gpio_154               | General-purpose IO 154 | IO              | B22                 | A2                  |
| gpio_155               | General-purpose IO 155 | IO              | A22                 | B2                  |
| gpio_156               | General-purpose IO 156 | IO              | R25                 | B11                 |
| gpio_157               | General-purpose IO 157 | IO              | P21                 | D11                 |
| gpio_158               | General-purpose IO 158 | IO              | P22                 | C10                 |
| gpio_159               | General-purpose IO 159 | IO              | P23                 | C9                  |
| gpio_160               | General-purpose IO 160 | IO              | P25                 | E11                 |
| gpio_161               | General-purpose IO 161 | IO              | P24                 | C11                 |
| gpio_162               | General-purpose IO 162 | IO              | N24                 | C8                  |
| gpio_163               | General-purpose IO 163 | IO              | N2                  | W15                 |
| gpio_164               | General-purpose IO 164 | IO              | N3                  | W13                 |
| gpio_165               | General-purpose IO 165 | IO              | P1                  | AA13                |
| gpio_166               | General-purpose IO 166 | IO              | P2                  | Y13                 |
| gpio_167               | General-purpose IO 167 | IO              | AC7                 | R22                 |
| gpio_168               | General-purpose IO 168 | IO              | W1                  | Y17                 |
| gpio_170               | General-purpose IO 170 | IO              | L25                 | B9                  |
| gpio_171               | General-purpose IO 171 | IO              | AE14                | K22                 |
| gpio_172               | General-purpose IO 172 | IO              | AD15                | K19                 |
| gpio_173               | General-purpose IO 173 | IO              | AC15                | J18                 |
| gpio_174               | General-purpose IO 174 | IO              | AB15                | K18                 |
| gpio_175               | General-purpose IO 175 | IO              | AD14                | J20                 |
| gpio_176               | General-purpose IO 176 | IO              | AE15                | J19                 |
| gpio_177               | General-purpose IO 177 | IO              | AE16                | J21                 |
| gpio_178               | General-purpose IO 178 | IO              | AD16                | J22                 |
| gpio_179               | General-purpose IO 179 | IO              | AC16                | H20                 |
| gpio_180               | General-purpose IO 180 | IO              | AB16                | H22                 |
| gpio_181               | General-purpose IO 181 | IO              | AA16                | H21                 |
| gpio_182               | General-purpose IO 182 | IO              | AE17                | H19                 |
| gpio_183               | General-purpose IO 183 | IO              | W2                  | Y16                 |
| gpio_184               | General-purpose IO 184 | IO              | W4                  | W16                 |
| gpio_185               | General-purpose IO 185 | IO              | W5                  | W17                 |
| gpio_186               | General-purpose IO 186 | IO              | M25                 | E10                 |

#### 4.4.8 System and Miscellaneous Terminals

**Table 4-26. System and Miscellaneous Signals Description**

| SIGNAL NAME [1] | DESCRIPTION [2]                                                                                      | TYPE [3] | ZCN BALL [4] | ZER BALL [4] |
|-----------------|------------------------------------------------------------------------------------------------------|----------|--------------|--------------|
| sys_32k         | 32-kHz clock input                                                                                   | I        | K24          | A8           |
| sys_xtalin      | Main input clock. Oscillator input                                                                   | I        | K25          | A10          |
| sys_xtalout     | Output of oscillator                                                                                 | O        | H25          | A9           |
| sys_altdclk     | Alternate clock source selectable for GPTIMERS (maximum 54 MHz), USB (48 MHz) , or NTSC/PAL (54 MHz) | I        | L25          | B9           |
| sys_clkreq      | Request from device for system clock (open source type)                                              | IO       | M24          | B8           |
| sys_clkout1     | Configurable output clock1                                                                           | O        | N25          | E9           |
| sys_clkout2     | Configurable output clock2                                                                           | O        | M25          | E10          |
| sys_boot0       | Boot configuration mode bit 0                                                                        | I        | Y4           | AB19         |
| sys_boot1       | Boot configuration mode bit 1                                                                        | I        | AA1          | AB20         |
| sys_boot2       | Boot configuration mode bit 2                                                                        | I        | AA2          | W18          |
| sys_boot3       | Boot configuration mode bit 3                                                                        | I        | AA3          | AA19         |
| sys_boot4       | Boot configuration mode bit 4                                                                        | I        | AB1          | V18          |
| sys_boot5       | Boot configuration mode bit 5                                                                        | I        | AB2          | Y19          |
| sys_boot6       | Boot configuration mode bit 6                                                                        | I        | AC1          | W19          |
| sys_boot7       | Boot configuration mode bit 7                                                                        | I        | AC2          | AA20         |
| sys_boot8       | Boot configuration mode bit 8                                                                        | I        | AC3          | Y20          |
| sys_nrespwron   | Power On Reset                                                                                       | I        | Y2           | AA18         |
| sys_nreswarm    | Warm Boot Reset (open drain output)                                                                  | IOD      | Y3           | Y18          |
| sys_nirq        | External FIQ input                                                                                   | I        | Y1           | AB18         |
| sys_ndmareq0    | External DMA request 0 (system expansion). Level (active low) or edge (falling) selectable.          | I        | M3           | V12          |
| sys_ndmareq1    | External DMA request 1 (system expansion). Level (active low) or edge (falling) selectable.          | I        | M2,U1        | AA11,V14     |
| sys_ndmareq2    | External DMA request 2 (system expansion). Level (active low) or edge (falling) selectable.          | I        | F1,M1        | W12,AB7      |
| sys_ndmareq3    | External DMA request 3 (system expansion). Level (active low) or edge (falling) selectable.          | I        | G6,N5        | AA12,V6      |

#### 4.4.9 Power Supplies

**Table 4-27. Power Supplies Description**

| SIGNAL NAME <sup>[1]</sup> | DESCRIPTION <sup>[2]</sup>                                                                                              | BALL<br>(ZCN Pkg.) <sup>[4]</sup>                                                                                                                                                                                                                                                                                                                                                                      | BALL<br>(ZER Pkg.) <sup>[4]</sup>                                                                                                                                                                                                                                                                                                                                                                                 |
|----------------------------|-------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD_CORE                   | 1.2-V core and oscillator macros power supply.                                                                          | V16, V15, V11, V10, U16, U15, U11, U10, T18, T17, T9, T8, R18, R17, R9, R8, M18, L18, L9, L8, K18, K17, K9, K8, J16, J15, J11, J10, H15, H11, H10                                                                                                                                                                                                                                                      | J8, J10, J12, J14, J16, K9, K11, K13, K15, L8, L10, L12, L14, M7, M9, M11, M13, M15, N8, N10, N12, N14, P7, P9, P11, P13, P15, R8, R10, R12, R14                                                                                                                                                                                                                                                                  |
| VSS                        | Core and I/O common ground.                                                                                             | AE25, AE1, V18, V17, V14, V13, V12, V9, V8, U18, U17, U14, U13, U12, U9, U8, T14, T13, T12, R16, R15, R14, R13, R12, R11, R10, P18, P17, P16, P15, P14, P13, P12, P11, P10, P9, P8, N18, N17, N14, N13, N12, N9, N8, M17, M16, M15, M14, M13, M12, M11, M10, M9, M8, L17, L16, L15, L14, L13, L12, L11, L10, K14, K13, K12, J18, J17, J14, J13, J12, J9, J8, H14, H13, H12, H9, A25, A1, N23, G20, G21 | A1, A11, A22, E6, E16, F6, F13, F15, F17, G5, G7, G11, G14, G16, G18, H6, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16, H17, J9, J11, J13, J15, K8, K10, K12, K14, K16, L7, L9, L11, L13, L15, M1, M6, M8, M10, M12, M14, M16, M22, N7, N9, N11, N13, N15, N17, P6, P8, P10, P12, P14, P16, R5, R7, R9, R11, R13, R15, R17, T6, T8, T10, T12, T14, T16, T18, U5, U7, U9, U11, U13, U15, U17, V6, AB1, AB12, AB22 |
| VDDS_SRAM_MPU              | 1.8-V MPU SLDO analog power supply.                                                                                     | AA13                                                                                                                                                                                                                                                                                                                                                                                                   | L17                                                                                                                                                                                                                                                                                                                                                                                                               |
| VDDS_SRAM_CORE_BG          | 1.8-V Core SLDO and VDDA of BandGap analog power supply.                                                                | E17                                                                                                                                                                                                                                                                                                                                                                                                    | J6                                                                                                                                                                                                                                                                                                                                                                                                                |
| CAP_VDD_SRAM_MPU           | 1.2-V SRAMOUT for MPU SLDO.<br>For proper device operation, connect to a 1µF decoupling capacitor.                      | AA12                                                                                                                                                                                                                                                                                                                                                                                                   | M17                                                                                                                                                                                                                                                                                                                                                                                                               |
| CAP_VDD_SRAM_CORE          | 1.2-V SRAMOUT for Core SLDO.<br>For proper device operation, connect to a 1µF decoupling capacitor.                     | E16                                                                                                                                                                                                                                                                                                                                                                                                    | K6                                                                                                                                                                                                                                                                                                                                                                                                                |
| VDDS_DPLL_MPU_USBH OST     | 1.8-V MPUSS DPLL and USBHOST DPLL analog power supply.                                                                  | AA15                                                                                                                                                                                                                                                                                                                                                                                                   | K17                                                                                                                                                                                                                                                                                                                                                                                                               |
| VDDS_DPLL_PER_CORE         | 1.8-V DPLL and HSDIVIDER/ CORE and HSDIVIDER analog power supply.                                                       | N20                                                                                                                                                                                                                                                                                                                                                                                                    | F11                                                                                                                                                                                                                                                                                                                                                                                                               |
| VDDA_DAC                   | 1.8-V DAC analog power supply.                                                                                          | H21                                                                                                                                                                                                                                                                                                                                                                                                    | NA                                                                                                                                                                                                                                                                                                                                                                                                                |
| VSSA_DAC                   | DAC analog ground.                                                                                                      | H22                                                                                                                                                                                                                                                                                                                                                                                                    | NA                                                                                                                                                                                                                                                                                                                                                                                                                |
| VDDA3P3V_USBPHY            | 3.3-V USB transceiver analog power supply.                                                                              | F23                                                                                                                                                                                                                                                                                                                                                                                                    | F7                                                                                                                                                                                                                                                                                                                                                                                                                |
| VDDA1P8V_USBPHY            | 1.8-V USB transceiver power supply.                                                                                     | G22                                                                                                                                                                                                                                                                                                                                                                                                    | D7                                                                                                                                                                                                                                                                                                                                                                                                                |
| CAP_VDDA1P2LDO_USB PHY     | Output of the 1.2-V internal LDO.<br>For proper device operation, connect a 0.22µF capacitor between this pin and VSSA. | F22                                                                                                                                                                                                                                                                                                                                                                                                    | E7                                                                                                                                                                                                                                                                                                                                                                                                                |

**Table 4-27. Power Supplies Description (continued)**

| SIGNAL NAME <sup>[1]</sup> | DESCRIPTION <sup>[2]</sup>     | BALL<br>(ZCN Pkg.) <sup>[4]</sup>                                                                                                                                                                       | BALL<br>(ZER Pkg.) <sup>[4]</sup>                                                                                                                                                |
|----------------------------|--------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDDSHV                     | 1.8/3.3-V power supply.        | Y16, Y15, Y13,<br>Y12, Y10, W16,<br>W15, W13,<br>W12, W10, W9,<br>W6, V7, V6,<br>U19, T20, T19,<br>T7, T6, R7, R6,<br>P20, P19, N19,<br>N7, N6, M7, M6,<br>M5, L19, K19,<br>K7, K6, K5, J7,<br>H18, H17 | A21, B1, E15, E17, F12, F14, F18,<br>G10, G12, G13, G8, G17, H18, J17,<br>L22, N16, P17, R16, R18, T9, T11,<br>T13, T17, U8, U10, U12, U14, U16,<br>U18, V7, V8, V17, AA22, AB11 |
| VDDS                       | 1.8-V power supply.            | Y9, W18, U20,<br>R5, N22, H16,<br>H8, G17, G16,<br>G14, G13, G11,<br>G10, G8, F16,<br>F13, F11, F10,<br>F8                                                                                              | F5, F16, G15, H5, K7, L6, L16, N1,<br>N5, N6, P5, R6, T5, T7, T15, U6,<br>AA1                                                                                                    |
| VDDSOSC                    | 1.8-V oscillator power supply. | L20                                                                                                                                                                                                     | G9                                                                                                                                                                               |
| VSSOSC                     | Oscillator ground.             | J25                                                                                                                                                                                                     | B10                                                                                                                                                                              |

## 5 Specifications

### 5.1 Absolute Maximum Ratings

Table 5-1 specifies the absolute maximum ratings over the operating junction temperature range of commercial and extended temperature devices. Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**Notes:**

- Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

**Table 5-1. Absolute Maximum Ratings Over Operating Junction Temperature Range**

| PARAMETER             |                                                                      | MIN                                             | MAX  | UNIT          |    |
|-----------------------|----------------------------------------------------------------------|-------------------------------------------------|------|---------------|----|
| VDD_CORE              | Supply voltage range for core macros                                 |                                                 | -0.5 | 1.6           | V  |
| VDDS                  | Second supply voltage range for 1.8-V I/O macros                     |                                                 | -0.5 | 2.25          | V  |
| VDDSHV                | Supply voltage range for 1.8/3.3V I/O macros                         |                                                 | -0.5 | 3.8           | V  |
| VDDS_SRAM_MPU         | Analog Supply voltage range for 1.8-V MPU SLDO                       |                                                 | -0.5 | 2.25          | V  |
| VDDS_SRAM_CORE_BG     | Analog Supply voltage range for 1.8-V Core SLDO and VDDA of BandGap  |                                                 | -0.5 | 2.25          | V  |
| VDDS_DPLL_MPU_USBHOST | Analog power supply for 1.8-V MPUSS DPLL and USBHOST DPLL            |                                                 | -0.5 | 2.1           | V  |
| VDDS_DPLL_PER_CORE    | Analog power supply for 1.8-V DPLL and HSDIVIDER/ CORE and HSDIVIDER |                                                 | -0.5 | 2.1           | V  |
| VDDA_DAC              | Analog Power Supply for 1.8-V DAC                                    |                                                 | -0.5 | 2.43          | V  |
| VDDA3P3V_USBPHY       | Analog power supply for 3.3-V USB transceiver                        |                                                 | -0.5 | 3.6           | V  |
| VDDA1P8V_USBPHY       | Power Supply for 1.8-V USB transceiver                               |                                                 | -0.5 | 2.0           | V  |
| VDDSOSC               | Power Supply for 1.8-V oscillator                                    |                                                 | -0.5 | 2.1           | V  |
| V <sub>PAD</sub>      | Voltage range at PAD                                                 | Oscillator input (sys_xtalin)                   | -0.3 | VDDSOSC + 0.3 | V  |
|                       |                                                                      | VDDS 1.8-V I/O macros                           | -0.3 | VDDS + 0.3    |    |
|                       |                                                                      | Dual-voltage LVCMOS inputs, VDDSHV = 1.8 V      | -0.3 | VDDSHV + 0.3  |    |
|                       |                                                                      | Dual-voltage LVCMOS inputs, VDDSHV = 3.3 V      | -0.3 | 3.8           |    |
|                       |                                                                      | USB VBUS pin (usb0_vbus)                        |      | 5.5           |    |
|                       |                                                                      | USB 5V Tolerant IOs (usb0_dp, usb0_dm, usb0_id) |      | 5.25          |    |
| I <sub>IOI</sub>      | Current-pulse injection on each I/O pin <sup>(1)</sup>               |                                                 |      | 200           | mA |
| I <sub>clamp</sub>    | Clamp current for an input or output                                 |                                                 | -20  | 20            | mA |

(1) Each device is tested with I/O pin injection of 200 mA with a stress voltage of 1.5 times maximum vdd at room temperature.

## 5.2 Handling Ratings

**Table 5-2. Handling Ratings**

| PARAMETER        |                                   |                                           | MIN   | MAX | UNIT |
|------------------|-----------------------------------|-------------------------------------------|-------|-----|------|
| V <sub>ESD</sub> | ESD stress voltage <sup>(1)</sup> | HBM (human body model) <sup>(2)</sup>     | >1000 |     | V    |
|                  |                                   | CDM (charged device model) <sup>(3)</sup> | >500  |     |      |
| T <sub>stg</sub> | Storage temperature range         |                                           | -65   | 150 | °C   |

- (1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the device.
- (2) The level listed above is the passing level per ANSI/ESDA/JEDEC JS-001-2010. JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process, and manufacturing with less than 500V HBM is possible if necessary precautions are taken. Actual performance of the device may exceed the value listed above.
- (3) The level listed above is the passing level per EIA-JEDEC JESD22-C101E. JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process. Actual performance of the device may exceed the value listed above.

### 5.3 Recommended Operating Conditions

All AM3517/05 modules are used under the operating conditions contained in [Table 5-3](#).

**Note:** Logic functions and parameter values are not assured if the device is operated out of the range specified in the recommended operating conditions.

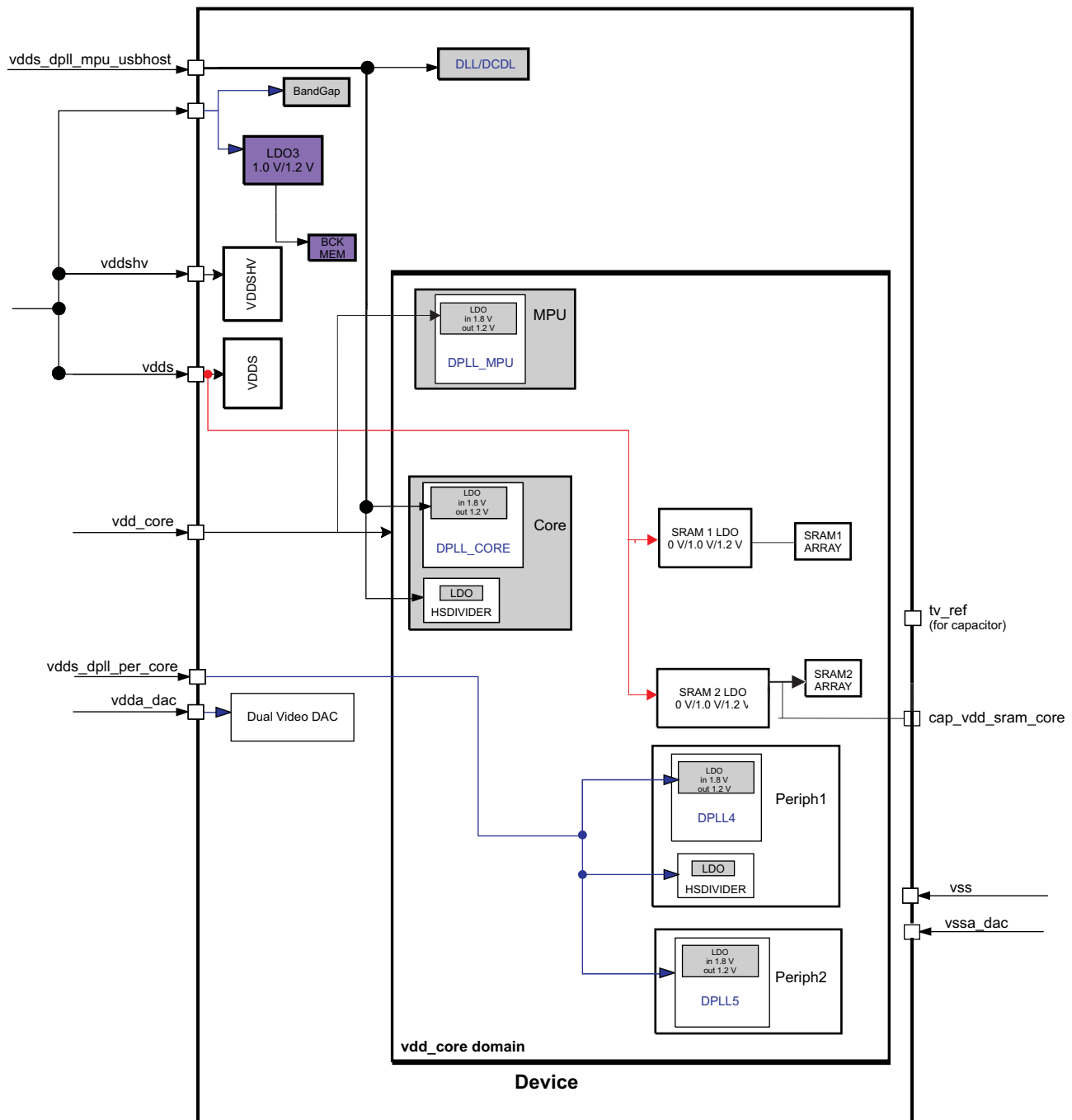
**Table 5-3. Recommended Operating Conditions**

| PARAMETER                                                 | DESCRIPTION                                    |                            | MIN   | NOM                | MAX   | UNIT |
|-----------------------------------------------------------|------------------------------------------------|----------------------------|-------|--------------------|-------|------|
| VDD_CORE                                                  | Core and oscillator macros power supply        |                            | 1.152 | 1.20               | 1.248 | V    |
|                                                           | Noise (peak-peak)                              |                            |       |                    | 24.00 | mVpp |
| VDDS_SRAM_MPU                                             | MPU SRAM LDO analog power supply               |                            | 1.71  | 1.80               | 1.89  | V    |
|                                                           | Noise (peak-peak)                              |                            |       |                    | 50.00 | mVpp |
| VDDS_SRAM_CORE_BG                                         | Core SRAM LDO and BandGap analog power supply  |                            | 1.71  | 1.80               | 1.89  | V    |
|                                                           | Noise (peak-peak)                              |                            |       |                    | 50.00 | mVpp |
| VDDS_DPLL_MPU_USBHOST                                     | MPU and USBHOST DPLL analog power supply       |                            | 1.71  | 1.80               | 1.89  | V    |
|                                                           | Noise (peak-peak)                              |                            |       |                    | 35.00 | mVpp |
| VDDS_DPLL_PER_CORE                                        | Peripherals and Core DPLLs analog power supply |                            | 1.71  | 1.80               | 1.89  | V    |
|                                                           | Noise (peak-peak)                              |                            |       |                    | 35.00 | mVpp |
| VDDA_DAC                                                  | DAC analog power supply                        |                            | 1.71  | 1.80               | 1.89  | V    |
|                                                           | Noise (peak-peak)                              |                            |       |                    | 30.00 | mVpp |
| VSSA_DAC                                                  | DAC analog ground                              |                            |       | 0.00               |       | V    |
| VDDA3P3V_USBPHY                                           | Analog power supply for 3.3-V USB transceiver  |                            | 3.14  | 3.30               | 3.47  | V    |
|                                                           | Noise (peak-peak)                              |                            |       |                    | 70.00 | mVpp |
| VDDA1P8V_USBPHY                                           | Power Supply for 1.8-V USB transceiver         |                            | 1.71  | 1.80               | 1.89  | V    |
|                                                           | Noise (peak-peak)                              |                            |       |                    | 50.00 | mVpp |
| VDDSHV                                                    | 3.3-/1.8-V power supply                        | 1.8 V Mode                 | 1.71  | 1.80               | 1.89  | V    |
|                                                           |                                                | 3.3 V Mode                 | 3.14  | 3.30               | 3.47  | V    |
| VDDS                                                      | 1.8-V power supply                             |                            | 1.71  | 1.80               | 1.89  | V    |
| T <sub>j</sub>                                            | Operating junction temperature range           | Commercial Temperature     | 0     |                    | 90    | °C   |
|                                                           |                                                | Extended Temperature       | -40   |                    | 105   | °C   |
| Device Operating Life Power-On Hours (POH) <sup>(1)</sup> | 500 MHz ARM Clock Freq.                        | < 90°C T <sub>j</sub>      |       | 100K               |       | hrs. |
|                                                           |                                                | 90 - 105 °C T <sub>j</sub> |       | 100K               |       |      |
|                                                           | 600 MHz ARM Clock Freq.                        | < 90°C T <sub>j</sub>      |       | 100K               |       |      |
|                                                           |                                                | 90 - 105 °C T <sub>j</sub> |       | 50K <sup>(2)</sup> |       |      |

(1) The POH information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.

(2) Maximum lifetime will be 100k Power On Hours as long as no more than 50k is greater than 90°C.

Figure 5-1 shows the power domains:



030-003

Figure 5-1. AM3517/05 Voltage Domains

## 5.4 Power Consumption Summary

The supply voltages and power consumption estimates are detailed in [Table 5-4](#).

**Table 5-4. Estimated Power Consumption at Ball Level**

| SIGNAL NAME           | DESCRIPTION                                                      |        | MAX CURRENT (mA) |
|-----------------------|------------------------------------------------------------------|--------|------------------|
| VDD_CORE              | 1.2-V core and oscillator macros power supply                    | AM3517 | 1500 mA          |
|                       |                                                                  | AM3505 | 1400 mA          |
| VDDS_SRAM_MPU         | 1.8-V MPU SLDO analog power supply                               |        | 40 mA            |
| VDDS_SRAM_CORE_BG     | 1.8-V Core SLDO and VDDA of BandGap analog power supply          |        | 40 mA            |
| VDDS_DPLL_MPU_USBHOST | 1.8-V MPUSS DPLL and USBHOST DPLL analog power supply            |        | 25 mA            |
| VDDS_DPLL_PER_CORE    | 1.8-V DPLL and HSDIVIDER/ CORE and HSDIVIDER analog power supply |        | 25 mA            |
| VDDA_DAC              | 1.8-V DAC analog power supply                                    |        | 65 mA            |
| VDDA3P3V_USBPHY       | 3.3-V USB transceiver analog power supply                        |        | 10 mA            |
| VDDA1P8V_USBPHY       | 1.8-V USB transceiver power supply                               |        | 50 mA            |
| VDDSHV                | 3.3-/1.8-V power supply                                          |        | 300 mA           |
| VDDS                  | 1.8-V power supply                                               |        | 200 mA           |
| VDDSOSC               | 1.8-V oscillator power supply                                    |        | 20 mA            |

## 5.5 Electrical Characteristics

Table 5-5 summarizes the DC electrical characteristics.

**Table 5-5. DC Electrical Characteristics**

| PARAMETER                                                |                                                                                                                     |                                                          |                                          | MIN           | NOM | MAX              | UNIT |
|----------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------|------------------------------------------|---------------|-----|------------------|------|
| <b>LVC MOS Pin Buffers</b>                               |                                                                                                                     |                                                          |                                          |               |     |                  |      |
| V <sub>IH</sub>                                          | High-level input voltage                                                                                            | VDDSHV = 1.8 V                                           |                                          | 0.65 x VDDSHV |     |                  | V    |
|                                                          |                                                                                                                     | VDDSHV = 3.3 V <sup>(1)</sup>                            |                                          | 2             |     |                  |      |
|                                                          |                                                                                                                     | sys_xtalin                                               |                                          | 0.8 x VDDSOCS |     |                  |      |
| V <sub>IL</sub>                                          | Low-level input voltage                                                                                             | VDDSHV = 1.8 V <sup>(1)</sup>                            |                                          |               |     | 0.35 x VDDSHV    | V    |
|                                                          |                                                                                                                     | VDDSHV = 3.3 V <sup>(1)</sup>                            |                                          |               |     | 0.8              |      |
|                                                          |                                                                                                                     | sys_xtalin                                               |                                          |               |     | 0.2 x VDDSOCS    |      |
| V <sub>OH</sub>                                          | High-level output voltage                                                                                           | VDDSHV = 1.8 V <sup>(1)</sup><br>I <sub>OH</sub> = -2 mA |                                          | VDDSHV - 0.45 |     |                  | V    |
|                                                          |                                                                                                                     | VDDSHV = 3.3 V <sup>(1)</sup><br>I <sub>OH</sub> = -2 mA |                                          | 2.4           |     |                  |      |
| V <sub>OL</sub>                                          | Low-level output voltage                                                                                            | VDDSHV = 1.8 V <sup>(1)</sup><br>I <sub>OL</sub> = 2 mA  |                                          |               |     | 0.45             | V    |
|                                                          |                                                                                                                     | VDDSHV = 3.3 V <sup>(1)</sup><br>I <sub>OL</sub> = 2 mA  |                                          |               |     | 0.4              |      |
| I <sub>I</sub>                                           | Input current for dual voltage IO pins                                                                              | V <sub>I</sub> = V <sub>SS</sub> to VDDSHV               | Input pins with pull disabled            | -9            |     | 9                | μA   |
|                                                          |                                                                                                                     | V <sub>I</sub> = V <sub>SS</sub> to VDDSHV               | Input pins with 100 μA pull-up enabled   | -310          |     | -70              |      |
|                                                          |                                                                                                                     | V <sub>I</sub> = V <sub>SS</sub> to VDDSHV               | Input pins with 100 μA pull-down enabled | 75            |     | 270              |      |
|                                                          | Input current for DDR2/mDDR 1.8V IO pins                                                                            | V <sub>I</sub> = V <sub>SS</sub> to VDDSHV               | Input pins with 100 μA pull-down enabled | 77            |     | 286              |      |
| I <sub>OZ</sub>                                          | Off-state output current                                                                                            | V <sub>O</sub> = VDDSHV or 0V                            | Pull disabled                            | -20           |     | 20               | μA   |
| I <sub>OH</sub>                                          | High-level output current (dual-voltage LVC MOS IOs)                                                                |                                                          |                                          |               |     | -2               | mA   |
| I <sub>OL</sub>                                          | Low-level output current (dual-voltage LVC MOS IOs)                                                                 |                                                          |                                          |               |     | 2                | mA   |
| t <sub>T</sub>                                           | Input transition time (rise time, t <sub>R</sub> or fall time, t <sub>F</sub> evaluated between 10% and 90% at PAD) | VDDSHV = 1.8 V <sup>(1)</sup>                            | Normal mode                              |               |     | 10               | ns   |
|                                                          |                                                                                                                     |                                                          | High-speed mode                          |               |     | 3                |      |
|                                                          |                                                                                                                     | VDDSHV = 3.3 V <sup>(1)</sup>                            | Normal mode                              |               |     | 10               |      |
|                                                          |                                                                                                                     |                                                          | High-speed mode                          |               |     | 3                |      |
| Capacitan<br>ce                                          | Input capacitance (dual-voltage LVC MOS I/Os)                                                                       |                                                          |                                          |               | 3   |                  | pF   |
|                                                          | Output capacitance (dual-voltage LVC MOS I/Os)                                                                      |                                                          |                                          |               | 3   |                  | pF   |
| <b>Complex IO Dedicated to USB : USB0_DM and USB0_DP</b> |                                                                                                                     |                                                          |                                          |               |     |                  |      |
| V <sub>IH</sub>                                          | High-level input voltage                                                                                            | Low/Full speed                                           |                                          | 2.0           |     |                  | V    |
|                                                          |                                                                                                                     | High speed                                               |                                          |               |     |                  |      |
| <sup>(2)</sup> V <sub>IL</sub>                           | Low-level input voltage                                                                                             | Low/Full speed                                           |                                          |               |     | 0.8              | V    |
|                                                          |                                                                                                                     | High speed                                               |                                          |               |     | <sup>(2)</sup>   |      |
| V <sub>OH</sub>                                          | High-level output voltage                                                                                           | Low/Full speed                                           |                                          | 2.8           |     | VDDA3P3V_ USBPHY | V    |
|                                                          |                                                                                                                     | High speed                                               |                                          | 360           |     | 440              | mV   |

(1) These IO specifications apply to the dual-voltage IOs only and do not apply to the DDR2/mDDR interfaces. DDR2/mDDR IOs are 1.8V IOs and adhere to the JESD79-2A standard.

(2) These parameters must adhere to the requirements defined in section 7.1.7.2 of Universal Serial Bus Specifications revision 2.0.

**Table 5-5. DC Electrical Characteristics (continued)**

| PARAMETER       |                          |                | MIN | NOM | MAX | UNIT |
|-----------------|--------------------------|----------------|-----|-----|-----|------|
| V <sub>OL</sub> | Low-level output voltage | Low/Full speed | 0.0 |     | 0.3 | V    |
|                 |                          | High speed     | -10 |     | 10  | mV   |

## 5.6 Thermal Characteristics

Table 5-6 and Table 5-7 provide the thermal resistance characteristics for the recommended package types used on the AM3517/05.

**Table 5-6. Package Thermal Resistance Characteristics [ZCN Package]**

| NAME            | DESCRIPTION                                   | AIR FLOW (m/s) <sup>(1)</sup> | ZCN (°C/W) <sup>(2)</sup> |
|-----------------|-----------------------------------------------|-------------------------------|---------------------------|
| Θ <sub>JC</sub> | Junction-to-case (1S0P) <sup>(3)</sup>        | NA                            | 2.6                       |
| Θ <sub>JB</sub> | Junction-to-board (2S2P) <sup>(3)</sup>       | NA                            | 10.1                      |
| Θ <sub>JA</sub> | Junction-to-free air (2S2P) <sup>(3)</sup>    | 0.0                           | 24.1                      |
|                 |                                               | 1.0                           | 18.7                      |
|                 |                                               | 2.0                           | 17.5                      |
|                 |                                               | 3.0                           | 16.8                      |
| Ψ <sub>JT</sub> | Junction-to-package top (2S2P) <sup>(3)</sup> | 0.0                           | 0.05                      |
|                 |                                               | 1.0                           | 0.2                       |
|                 |                                               | 2.0                           | 0.2                       |
|                 |                                               | 3.0                           | 0.3                       |
| Ψ <sub>JB</sub> | Junction-to-board (2S2P) <sup>(3)</sup>       | 0.0                           | 10.0                      |
|                 |                                               | 1.0                           | 10.3                      |
|                 |                                               | 2.0                           | 10.2                      |
|                 |                                               | 3.0                           | 10.1                      |

(1) m/s = meters per second.

(2) °C/W = degrees celsius per watt.

(3) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, *Test Board for Area Array Surface Mount Package Thermal Measurements*).

**Table 5-7. Package Thermal Resistance Characteristics [ZER]<sup>(1)</sup>**

| NAME            | DESCRIPTION                                   | AIR FLOW (m/s) <sup>(2)</sup> | ZER (°C/W) <sup>(3)</sup> |
|-----------------|-----------------------------------------------|-------------------------------|---------------------------|
| Θ <sub>JC</sub> | Junction-to-case (2S2P) <sup>(4)</sup>        | NA                            | 6                         |
| Θ <sub>JB</sub> | Junction-to-board (2S2P) <sup>(4)</sup>       | NA                            | 6                         |
| Θ <sub>JA</sub> | Junction-to-free air (2S2P) <sup>(4)</sup>    | 0.0                           | 15.8                      |
|                 |                                               | 1.0                           | 12.0                      |
|                 |                                               | 2.0                           | 11.1                      |
|                 |                                               | 3.0                           | 10.8                      |
| Ψ <sub>JT</sub> | Junction-to-package top (2S2P) <sup>(4)</sup> | 0.0                           | 3.3                       |
|                 |                                               | 1.0                           | 3.7                       |
|                 |                                               | 2.0                           | 3.5                       |
|                 |                                               | 3.0                           | 3.5                       |

(1) Package thermal resistance characteristics for ZER support only 2S2P.

(2) m/s = meters per second.

(3) °C/W = degrees celsius per watt.

(4) The board types are defined by JEDEC (reference JEDEC standard JESD51-9, *Test Board for Area Array Surface Mount Package Thermal Measurements*).

**Table 5-7. Package Thermal Resistance Characteristics [ZER]<sup>(1)</sup> (continued)**

| NAME        | DESCRIPTION                             | AIR FLOW<br>(m/s) <sup>(2)</sup> | ZER (°C/W) <sup>(3)</sup> |
|-------------|-----------------------------------------|----------------------------------|---------------------------|
| $\Psi_{JB}$ | Junction-to-board (2S2P) <sup>(4)</sup> | 0.0                              | 6.0                       |
|             |                                         | 1.0                              | 6.1                       |
|             |                                         | 2.0                              | 5.8                       |
|             |                                         | 3.0                              | 5.7                       |

## 5.7 Core Voltage Decoupling

For module performance, decoupling capacitors are required to suppress the switching noise generated by high frequency and to stabilize the supply voltage. A decoupling capacitor is most effective when it is close to the device because this minimizes the inductance of the circuit board wiring and interconnects.

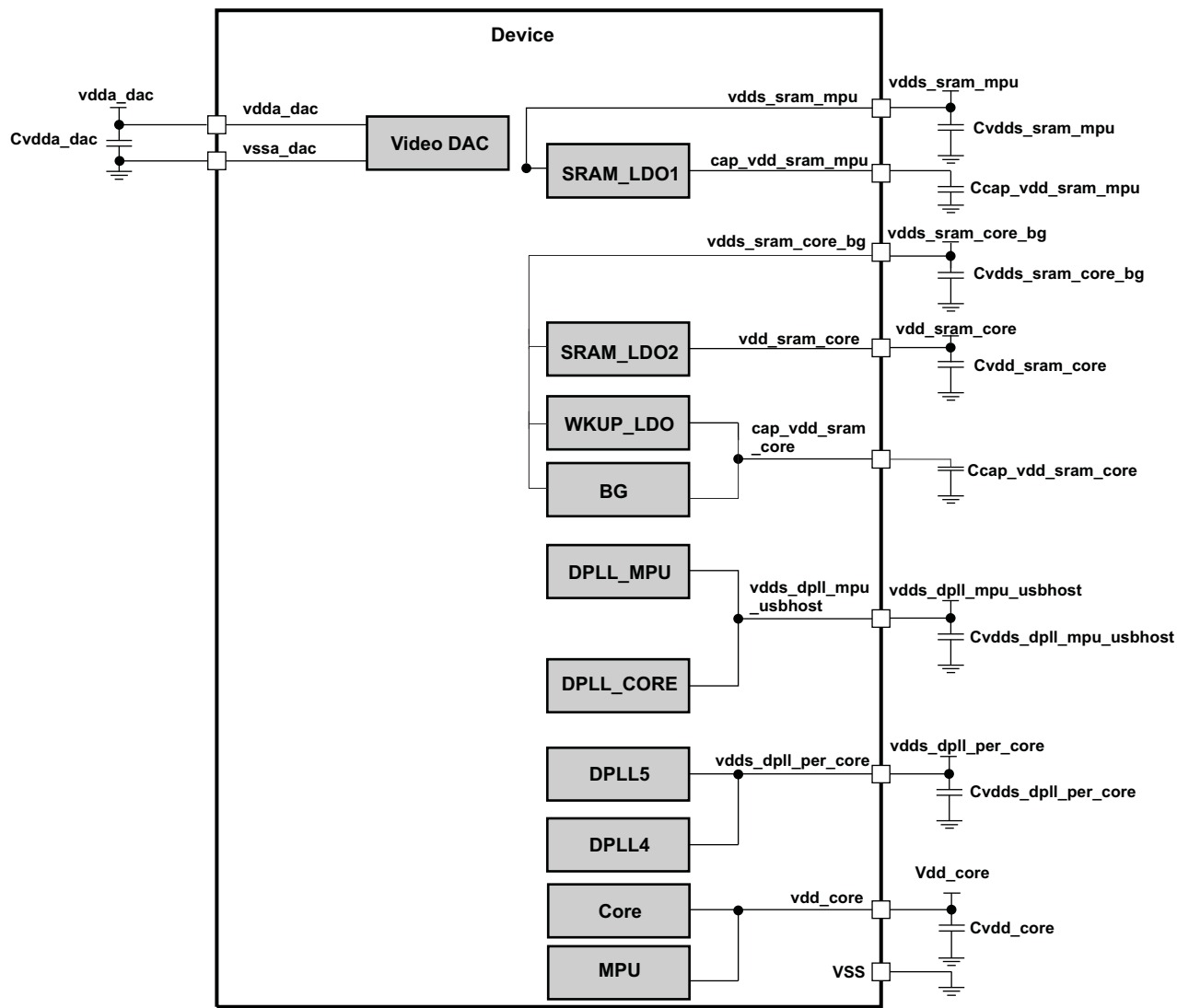
[Table 5-8](#) summarizes the power supplies decoupling characteristics.

**Table 5-8. Core Voltage Decoupling Characteristics**

| PARAMETER                | MIN | TYP | MAX | UNIT |
|--------------------------|-----|-----|-----|------|
| Cvdd_core <sup>(1)</sup> | 50  | 100 | 120 | nF   |
| Ccap_vdd_sram_core       |     | 100 |     | nF   |
| Cvdds_dppll_mpu_usbhost  |     | 100 |     | nF   |
| Cvdds_dppll_per_core     |     | 100 |     | nF   |
| Cvdda_dac                |     | 100 |     | nF   |
| Cvdd_sram_core           |     | 100 |     | nF   |
| Cvdd_sram_core_bg        |     | 100 |     | nF   |
| Cvdds_sram_mpu           |     | 100 |     | nF   |
| Cvddshv                  |     | 100 |     | nF   |
| Cvdda3p3v_usbphy         |     | 100 |     | nF   |
| Cvdda1p8v_usbphy         |     | 100 |     | nF   |

(1) 1 capacitor per 2 to 4 balls

Figure 5-2 shows an example of power supply decoupling.



030-004

- (1) Decoupling capacitors must be placed as close as possible to the power ball. Choose the ground located closest to the power pin for each decoupling capacitor. Place the decoupling capacitor  $C_i$  in a group of 1, 2, or 3 balls; the total must be equal to the decoupling requirement. In case you interconnect powers, first insert the decoupling capacitor and then interconnect the powers.
- (2) The decoupling capacitor value depends on the board characteristics.

**Figure 5-2. Power Supply Decoupling**

## 5.8 Power-up and Power-down

This section provides the timing requirements for the AM3517/05 hardware signals.

### 5.8.1 Power-up Sequence

The following steps give an example of power-up sequence supported by the AM3517/05.

1. IO 1.8V supply (VDDS), Band-gap and LDO supplies (VDDS\_SRAM\_CORE\_BG, VDDS\_SRAM\_MPU) and oscillator supply (VDDSOSC) should come up first to a stable state.
2. IO 3.3V (VDDSHV) supply should be ramped up next to a stable state.
3. Core (VDD\_CORE) supply follows next to a stable state.
4. All the PLL supplies (VDDS\_DPLL\_PER\_CORE, VDDS\_DPLL\_MPU\_USBHOST) and 1.8 V complex IO supplies (VDDA\_DAC, VDDA1P8V\_USBPHY) should be ramped up next to a stable state.
5. Finally, 3.3 V complex IO (VDDA\_3P3V\_USBPHY) should be ramped up.
6. sys\_nrespwrn must be held low at the time the power supplies are ramped up till the time the sys\_32k and sys\_xtalin clocks are stable.

**Note:** In VDDSHV 1.8 V operation mode, VDDSHV can be grouped and powered up together with VDDS, VDDS\_SRAM\_CORE\_BG, VDDS\_SRAM\_MPU and VDDSOSC.

Figure 5-3 shows the power-up sequence.

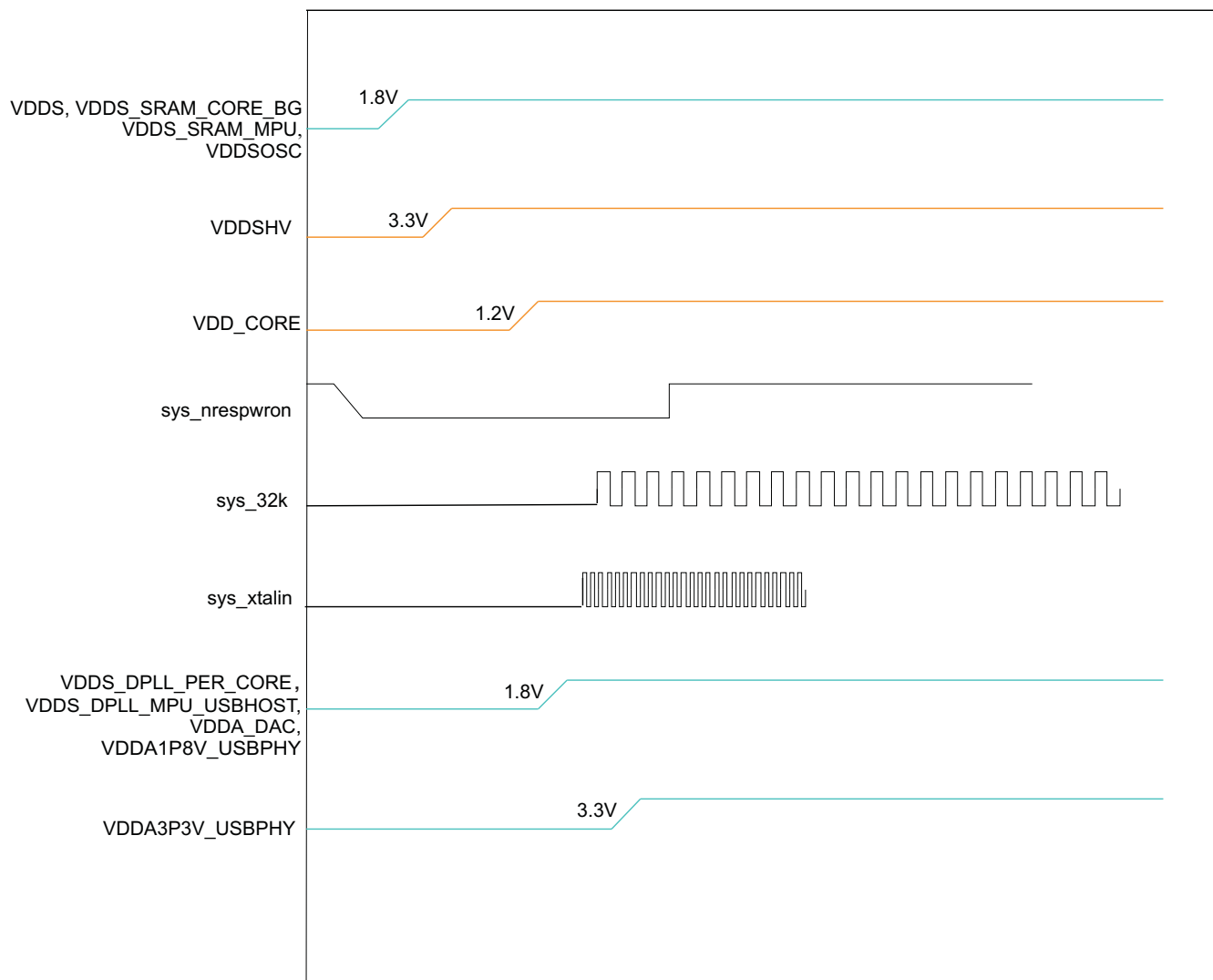


**Figure 5-3. Power-up Sequence**

### 5.8.2 Power-down Sequence

The AM3517/05 device proceeds with the power-down sequence shown below.

The following steps give an example of the power-down sequence supported by the AM3517/05 device.

1. Reset AM3517/05 device.
2. Stop all signals driven to AM3517/05.
3. Option 1: Power down all domains simultaneously.
4. Option 2: If all domains cannot be powered down simultaneously, follow the below sequence:
  - (a) Power off all complex I/O domains
  - (b) Power off core domain (VDD\_CORE)
  - (c) Power off all PLL domains (VDDS\_DPLL\_MPU\_USBHOST and VDDS\_DPLL\_PER\_CORE)
  - (d) Power off all SRAM LDOs
  - (e) Power off all standard I/O domains (VDDS and VDDSHV)

### 5.9 Clock Specifications

The AM3517/05 device has three external input clocks, a low frequency (sys\_32k), a high frequency (sys\_xtalin), and an optional (sys\_altdclk). The AM3517/05 device has two configurable output clocks, sys\_clkout1 and sys\_clkout2.

Figure 5-4 shows the interface to the external clock sources and clock outputs.

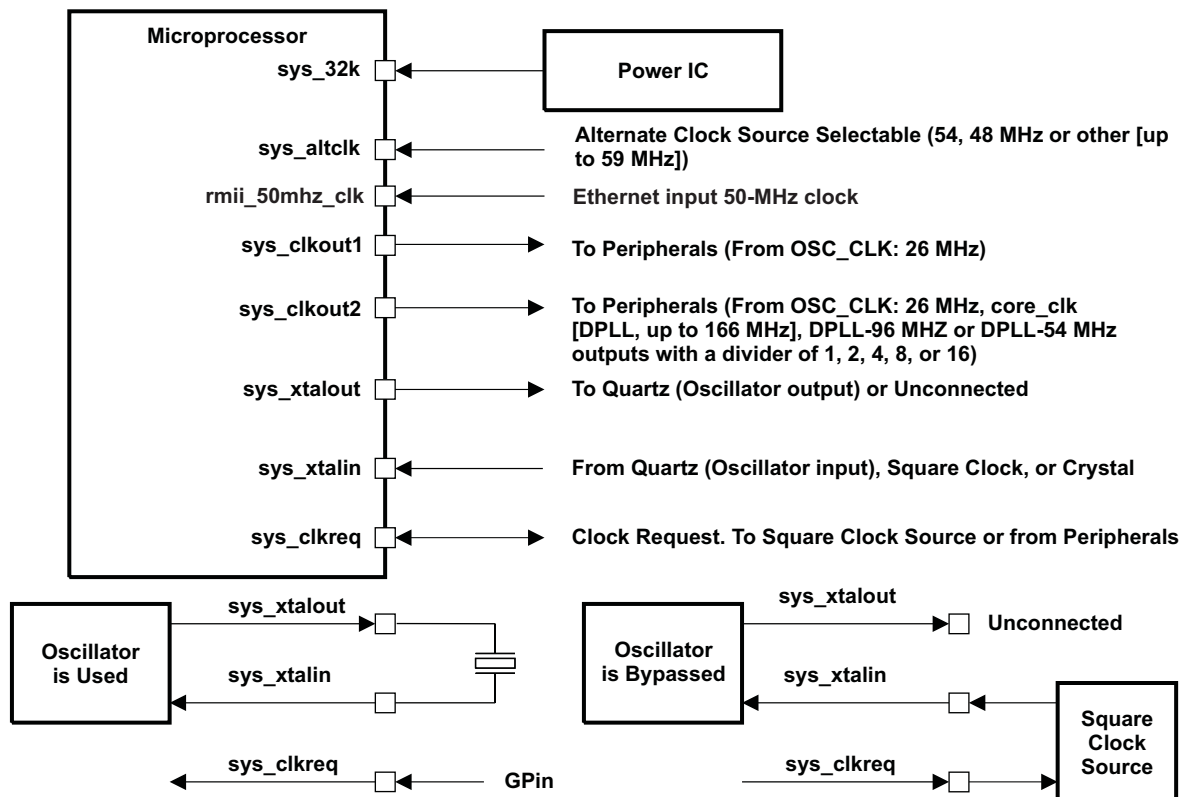


Figure 5-4. Clock Interface

The AM3517/05 device operation requires the following three input clocks:

- The 32-kHz clock can be generated using one of the following options and can be selected via the sys\_boot7 pin. See Figure 5-5.
  - External: Supplied by an oscillator on the sys\_32k pin.
  - Internal: 32-kHz clock generation using a fixed divider on the HS system clock (26MHz).
- The system alternative clock can be used (through the sys\_altclk pin) to provide alternative 48 or 54 MHz or other clock source (up to 54 MHz).
- The system clock input (26 MHz) is used to generate the main source clock of the AM3517/05 device. It supplies the DPLLs as well as several AM3517/05 modules. The system clock input can be connected to either:
  - A crystal oscillator clock managed by sys\_xtalin and sys\_xtalout. In this case, the sys\_clkreq is used as an input (GPIN).
  - A CMOS digital clock through the sys\_xtalin pin. In this case, the sys\_clkreq is used as an output to request the external system clock.

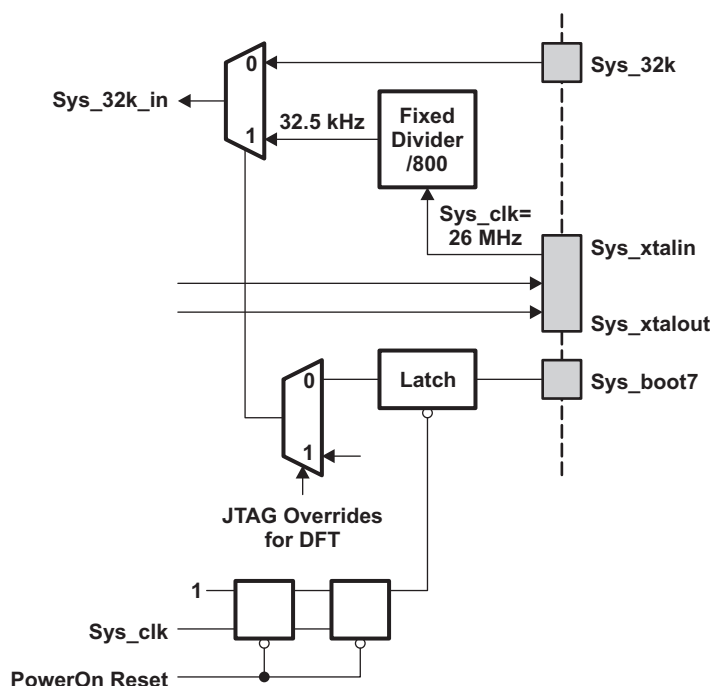


Figure 5-5. 32-kHz Clock Generation

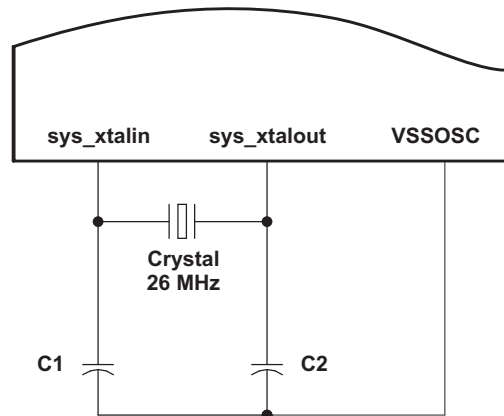
The AM3517/05 outputs externally two clocks:

- sys\_clkout1 can output the oscillator clock (26 MHz) at any time.
- sys\_clkout2 can output the oscillator clock, core\_clk, 96 MHz or 54 MHz. It can be divided by 2, 4, 8, or 16 and its off state polarity is programmable.

### 5.9.1 Oscillator

The sys\_xtalin (26 MHz) oscillator provides the primary reference clock for the device. The on-chip oscillator requires an external crystal connected across the sys\_xtalin and sys\_xtalout pins, along with two load capacitors, as shown in Figure 4-3. The external crystal load capacitors must be connected only to the oscillator ground pin (VSSOSC). Do not connect to board ground (VSS).

Note: If an external oscillator is to be used, the external oscillator clock signal should be connected to the sys\_xtalin pin with a 1.8V amplitude. The sys\_xtalout should be left unconnected and the VSSOSC signal should be connected to board ground (VSS).



- A. Oscillator components (Crystal,  $C_1$ ,  $C_2$ ) must be located close to the AM35x package. Parasitic capacitance to the printed circuit board (PCB) ground and other signals should be minimized to reduce noise coupled into the oscillator. The VSSOSC terminal provides a Kelvin ground reference for the external crystal components. External crystal component grounds should only be connected to the VSSOSC terminal and should not be connected to the PCB ground plane.
- B.  $C_1$  and  $C_2$  represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. The value of capacitors  $C_1$  and  $C_2$  should be selected to provide the total load capacitance,  $C_L$ , specified by the crystal manufacturer. The total load capacitance is  $C_L = [(C_1 * C_2) / (C_1 + C_2)] + C_{shunt}$ , where  $C_{shunt}$  is the crystal shunt capacitance ( $C_0$ ) specified by the crystal manufacturer plus any mutual capacitance ( $C_{pkg} + C_{PCB}$ ) seen across the AM3517/05 sys\_xtalin and sys\_xtalout signals. For recommended values of crystal circuit components, see [Table 5-9](#).

**Figure 5-6. AM3517/05 Oscillator Connections****Table 5-9. Crystal Electrical Characteristics**

| PARAMETER                                     | MIN | TYP | MAX    | UNIT     |
|-----------------------------------------------|-----|-----|--------|----------|
| Oscillation frequency                         |     | 26  |        | MHz      |
| Crystal ESR                                   |     | 50  |        | $\Omega$ |
| Frequency stability                           |     |     | +/- 50 | ppm      |
| Parallel Load Capacitance ( $C_1$ and $C_2$ ) |     |     | 20     | pF       |
| Shunt Capacitance                             |     |     | 5      | pF       |

### 5.9.2 Input Clock Specifications

The clock system accepts three input clock sources:

- 32-kHz digital CMOS clock
- Crystal oscillator clock or CMOS digital clock (26 MHz)
- Alternate clock (48 or 54 MHz, or other up to 54 MHz)

**Table 5-10. 26-MHz SYS\_CLK Input Clock Timing Requirements**

| PARAMETER  | DESCRIPTION                 | MIN | TYP | MAX | UNIT |
|------------|-----------------------------|-----|-----|-----|------|
| f(xtalin)  | Frequency, sys_xtalin       |     | 26  |     | MHz  |
| tw(xtalin) | Duty Cycle, sys_xtalin      | 45  |     | 55  | %    |
| tj(xtalin) | Jitter, sys_xtalin          | -1  |     | 1   | %    |
| tt(xtalin) | Transition time, sys_xtalin |     |     | 5   | ns   |

Table 5-11 and Table 5-12 detail the electrical characteristics and input requirements of the 32-kHz input clock.

**Table 5-11. 32-kHz Input Clock Source Electrical Characteristics**

| PARAMETER      | DESCRIPTION        | MIN  | TYP    | MAX             | UNIT |
|----------------|--------------------|------|--------|-----------------|------|
| f              | Frequency, sys_32k |      | 32.768 |                 | kHz  |
| C <sub>i</sub> | Input capacitance  |      |        | 0.45            | pF   |
| R <sub>i</sub> | Input resistance   | 0.25 |        | 10 <sup>6</sup> | GΩ   |

**Table 5-12. 32-kHz Input Clock Source Timing Requirements<sup>(1)</sup>**

| PARAMETER               | DESCRIPTION                   | MIN | TYP | MAX    | UNIT |
|-------------------------|-------------------------------|-----|-----|--------|------|
| 1 / t <sub>c(32k)</sub> | Frequency, sys_32k            |     | 32  |        | kHz  |
| t <sub>R(32k)</sub>     | Rise transition time, sys_32k |     |     | 20     | ns   |
| t <sub>F(32k)</sub>     | Fall transition time, sys_32k |     |     | 20     | ns   |
| t <sub>J(32k)</sub>     | Frequency stability, sys_32k  |     |     | +/-200 | ppm  |

(1) See *Electrical Characteristics* for Standard LVCMOS IOs part for sys\_32k V<sub>IH</sub>/V<sub>IL</sub> parameters.

Table 5-13 and Table 5-14 detail the electrical characteristics and input requirements of the 48- or 54-MHz input clock.

**Table 5-13. 48-MHz, 54-MHz, or up to 59-MHz Input Clock Source Electrical Characteristics**

| NAME           | DESCRIPTION            | MIN                 | MAX             | UNIT |
|----------------|------------------------|---------------------|-----------------|------|
| f              | Frequency, sys_altdclk | 48, 54, or up to 59 |                 | MHz  |
| C <sub>i</sub> | Input capacitance      |                     | 0.74            | pF   |
| R <sub>i</sub> | Input resistance       | 0.25                | 10 <sup>6</sup> | GΩ   |

**Table 5-14. 48-MHz, 54-MHz, or up to 59-MHz Input Clock Source Timing Requirements<sup>(1) (2)</sup>**

| PARAMETER                       | DESCRIPTION            | MIN                 | MAX | UNIT |
|---------------------------------|------------------------|---------------------|-----|------|
| 1 / t <sub>c(sys_altdclk)</sub> | Frequency, sys_altdclk | 48, 54, or up to 59 |     | MHz  |
| t <sub>w(sys_altdclk)</sub>     | Duty cycle             | 45                  | 60  | %    |
| t <sub>j(sys_altdclk)</sub>     | Jitter                 | -1                  | 1   | %    |
| t <sub>r(sys_altdclk)</sub>     | Rise transition time   |                     | 10  | ns   |
| t <sub>f(sys_altdclk)</sub>     | Fall transition time   |                     | 10  | ns   |
| f <sub>t(sys_altdclk)</sub>     | Frequency tolerance    | -50                 | 50  | ppm  |

(1) Peak-to-peak jitter is defined as the difference between the maximum and the minimum output periods on a statistical population of 300 period samples. The sinusoidal noise is added on top of the vdds supply voltage.

(2) See Section 5, *Electrical Characteristics*, for sys\_altdclk V<sub>IH</sub>/V<sub>IL</sub> parameters.

### 5.9.3 Output Clock Specifications

Two output clocks (pin sys\_clkout1 and pin sys\_clkout2) are available:

- sys\_clkout1 can output the oscillator clock (26 MHz) at any time. It can be controlled by software or externally using sys\_clkreq control. When the device is in the off state, the sys\_clkreq can be asserted to enable the oscillator and activate the sys\_clkout1 without waking up the device. The off state polarity of sys\_clkout1 is programmable.
- sys\_clkout2 can output sys\_clk (26 MHz), core\_clk (core DPLL output), APLL-96 MHz, or APLL-54 MHz. It can be divided by 2, 4, 8, or 16 and its off state polarity is programmable. This output is active only when the core domain is active.

Table 5-15 summarizes the sys\_clkout1 output clock electrical characteristics.

**Table 5-15. SYS\_CLKOUT1 Output Clock Electrical Characteristics**

| NAME           | DESCRIPTION                     |                   | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------|-------------------|-----|-----|-----|------|
| f              | Frequency                       |                   |     | 26  |     | MHz  |
| C <sub>L</sub> | Load capacitance <sup>(1)</sup> | f(max) = 38.4 MHz |     | 70  |     | pF   |
|                |                                 | f(max) = 26 MHz   |     | 125 |     |      |

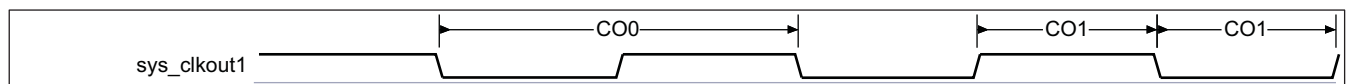
(1) The load capacitance is adapted to a frequency.

Table 5-16 details the sys\_clkout1 output clock timing characteristics.

**Table 5-16. SYS\_CLKOUT1 Output Clock Switching Characteristics**

| NAME | DESCRIPTION              |                                         | MIN                                | TYP | MAX                                | UNIT |
|------|--------------------------|-----------------------------------------|------------------------------------|-----|------------------------------------|------|
| f    | 1 / CO0                  | Frequency                               |                                    | 26  |                                    | MHz  |
| CO1  | t <sub>w</sub> (CLKOUT1) | Pulse duration, sys_clkout1 low or high | 0.40 *<br>t <sub>c</sub> (CLKOUT1) |     | 0.60 *<br>t <sub>c</sub> (CLKOUT1) | ns   |
| CO2  | t <sub>R</sub> (CLKOUT1) | Rise time, sys_clkout1 <sup>(1)</sup>   |                                    |     | 3.31                               | ns   |
| CO3  | t <sub>F</sub> (CLKOUT1) | Fall time, sys_clkout1 <sup>(1)</sup>   |                                    |     | 3.31                               | ns   |

(1) With a load capacitance of 25 pF.



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**Figure 5-7. SYS\_CLKOUT1 System Output Clock**

Table 5-17 summarizes the sys\_clkout2 output clock electrical characteristics.

**Table 5-17. SYS\_CLKOUT2 Output Clock Electrical Characteristics**

| NAME           | DESCRIPTION                           |                  | MIN | TYP | MAX | UNIT |
|----------------|---------------------------------------|------------------|-----|-----|-----|------|
| f              | Frequency, sys_clkout2 <sup>(1)</sup> |                  |     |     | 166 | MHz  |
| C <sub>L</sub> | Load capacitance <sup>(2)</sup>       |                  |     |     |     |      |
|                |                                       | f(max) = 166 MHz | 2   | 8   | 12  | pF   |

(1) The maximum frequency supported is core\_clk/2 MHz.

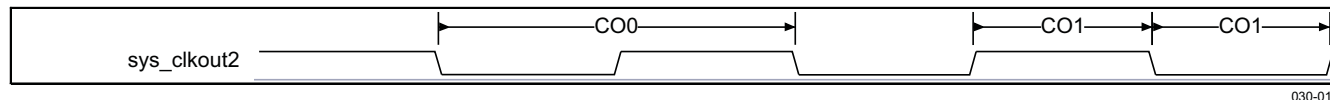
(2) The load capacitance is adapted to a frequency.

Table 5-18 details the sys\_clkout2 output clock timing characteristics.

**Table 5-18. SYS\_CLKOUT2 Output Clock Switching Characteristics**

| NAME |                  | DESCRIPTION                             | MIN                     | TYP | MAX                     | UNIT |
|------|------------------|-----------------------------------------|-------------------------|-----|-------------------------|------|
| f    | 1 / CO0          | Frequency                               |                         |     | 166                     | MHz  |
| CO1  | $t_{w(CLKOUT2)}$ | Pulse duration, sys_clkout2 low or high | $0.40 * t_{c(CLKOUT2)}$ |     | $0.60 * t_{c(CLKOUT2)}$ | ns   |
| CO2  | $t_{R(CLKOUT2)}$ | Rise time, sys_clkout2 <sup>(1)</sup>   |                         |     | 3.7                     | ns   |
| CO3  | $t_{F(CLKOUT2)}$ | Fall time, sys_clkout2 <sup>(1)</sup>   |                         |     | 4.3                     | ns   |

(1) With a load capacitance of 25 pF.



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**Figure 5-8. SYS\_CLKOUT2 System Output Clock**

### 5.9.4 DPLL Specifications

The AM3517/05 integrates four DPLLs. The PRM and CM drive them.

The four main DPLLs are:

- DPLL1 (MPU)
- DPLL3 (Core)
- DPLL4 (Peripherals)
- DPLL5 (Second Peripherals DPLL)

Figure 5-9 shows the DPLL implementation.

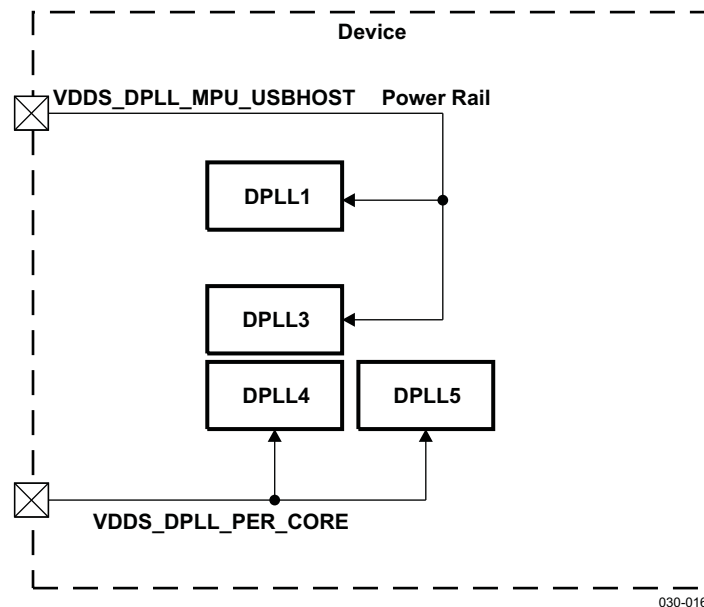


Figure 5-9. DPLL Implementation

#### 5.9.4.1 Digital Phase-Locked Loop (DPLL)

The DPLL provides all interface clocks and some functional clocks (such as the processor clocks) of the AM3517/05 device.

DPLL1 gets an always-on clock used to produce the synthesized clock. They get a high-speed bypass clock used to switch the DPLL output clock on this high-speed clock during bypass mode.

The high-speed bypass clock is an L3 divided clock (programmable by 1 or 2) that saves DPLL processor power consumption when the processor does not need to run faster than the L3 clock speed, or optimizes performance during frequency scaling.

Each DPLL synthesized frequency is set by programming M (multiplier) and N (divider) factors. In addition, all DPLL outputs can be controlled by an independent divider (M2 to M6).

The clock generating DPLLs of the AM3517/05 device have following features:

- Independent power domain per DPLL
- Controlled by clock-manager (CM)
- Fed with always-on system clock with independent gating control per DPLL
- Analog part supplied through dedicated power supply (1.8 V) and an embedded LDO to get rid of 1-MHz noise
- Up to four independent output dividers for simultaneous generation of multiple clock frequencies

**5.9.4.1.1 DPLL1 (MPU)**

DPLL1 is located in the MPU subsystem and supplies all clocks of the subsystem. All MPU subsystem clocks are internally generated in the subsystem. When the core domain is on, it can use the DPLL3 (CORE DPLL) output as a high-frequency bypass input clock.

**5.9.4.1.2 DPLL3 (CORE)**

DPLL3 supplies all interface clocks and also a few module functional clocks. It can be also source of the emulation trace clock. It is located in the core domain area. All interface clocks and a few module functional clocks are generated in the CM. When the core domain is on, it can be used as a bypass input to DPLL1.

**5.9.4.1.3 DPLL4 (Peripherals)**

DPLL4 generates clocks for the peripherals. It supplies five clock sources: 96-MHz functional clocks to subsystems and peripherals, 54 MHz to TV DAC, display functional clock, camera sensor clock, and emulation trace clock. It is located in the core domain area. All interface clocks and few module functional clocks are generated in the CM. Its outputs to the DSS, PER, and EMU domains are propagated with always-on clock trees.

**5.9.4.1.4 DPLL5 (Second peripherals DPLL)**

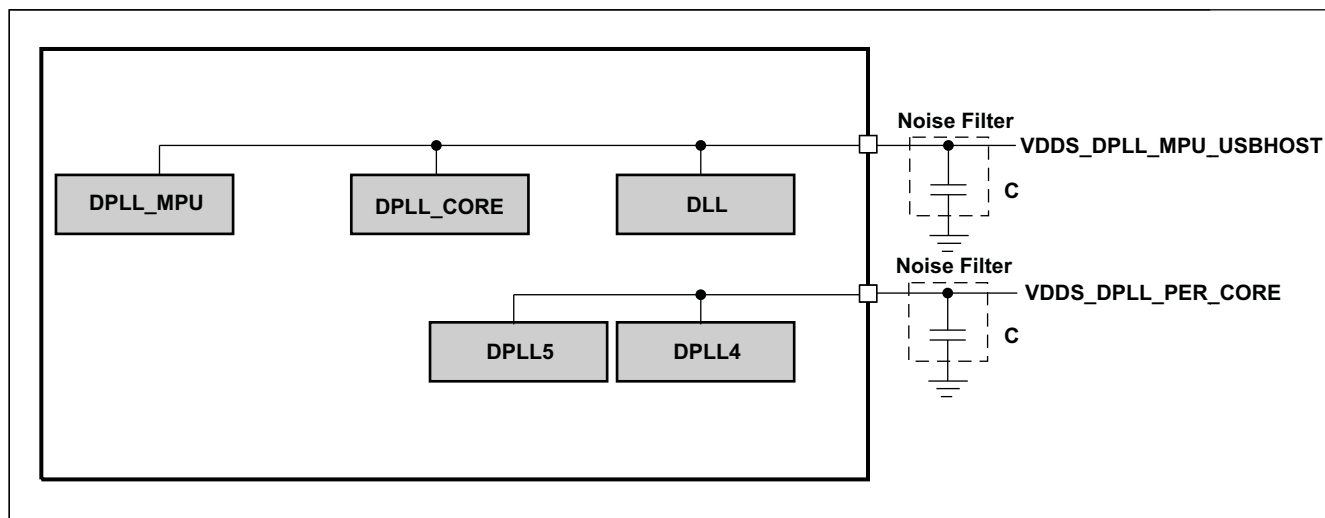
DPLL5 supplies the 120-MHz functional clock to the CM.

### 5.9.4.2 DPLL Noise Isolation

The DPLL requires dedicated power supply pins to isolate the core analog circuit from the switching noise generated by the core logic that can cause jitter on the clock output signal. Guard rings are added to the cell to isolate it from substrate noise injection.

The vdd supplies are the most sensitive to noise; decoupling capacitance is recommended below the supply rails. The maximum input noise level allowed is 30 mV<sub>PP</sub> for frequencies below 1 MHz.

Figure 5-10 shows an example of a noise filter.



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**Figure 5-10. DPLL Noise Filter**

Table 5-19 specifies the noise filter requirements.

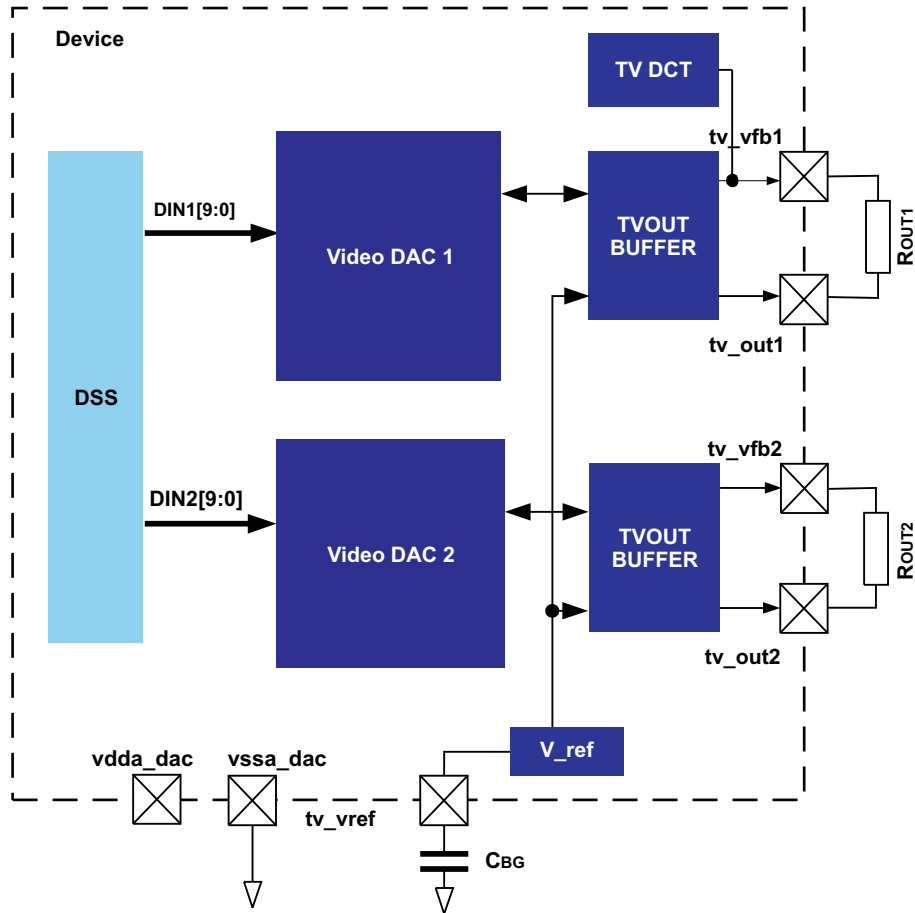
**Table 5-19. DPLL Noise Filter Requirements**

| NAME                | MIN | TYP | MAX | UNIT |
|---------------------|-----|-----|-----|------|
| Filtering capacitor |     | 100 |     | nF   |

- (1) The capacitors must be inserted between power and ground as close as possible.
- (2) This circuit is provided only as an example.
- (3) The filter must be located as close as possible to the device.
- (4) No filtering required if noise is below 10 mV<sub>PP</sub>.

## 5.10 Video DAC Specifications

A dual-display interface equips the AM3517/05 processor. This display subsystem provides the necessary control signals to interface the memory frame buffer directly to the external displays (TV-set). Two (one per channel) 10-bit current steering DACs are inserted between the DSS and the TV set to generate the video analog signal. One of the video DACs also includes TV detection and power-down mode. Figure 5-11 shows the AM3517/05 DAC architecture.



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**Figure 5-11. Video DAC Architecture**

The following paragraphs detail the 10-bit DAC interface pinout, static and dynamic specifications, and noise requirements. The operating conditions and absolute maximum ratings are detailed in [Table 5-21](#) and [Table 5-23](#).

### 5.10.1 Interface Description

Table 5-20 summarizes the external pins of the video DAC.

**Table 5-20. External Pins of 10-bit Video DAC**

| PIN NAME | I/O | DESCRIPTION                                    |                                                                                                                                                                                                 |
|----------|-----|------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| tv_out1  | O   | TV analog output composite                     | DAC1 video output. An external resistor is connected between this node and tv_vfb1. The nominal value of ROUT1 is 1650 . Finally, note that this is the output node that drives the load (75 ). |
| tv_out2  | O   | TV analog output S-VIDEO                       | DAC2 video output. An external resistor is connected between this node and tv_vfb2. The nominal value of ROUT2 is 1650 . Finally, note that this is the output node that drives the load (75 ). |
| tv_vref  | I   | Reference output voltage from internal bandgap | A decoupling capacitor (CBG) needs to be connected for optimum performance.                                                                                                                     |
| tv_vfb1  | O   | Amplifier feedback node                        | Amplifier feedback node. An external resistor is connected between this node and tv_out1. The nominal value of ROUT1 is 1650 (1%).                                                              |
| tv_vfb2  | O   | Amplifier feedback node                        | Amplifier feedback node. An external resistor is connected between this node and tv_out2. The nominal value of ROUT2 is 1650 (1%).                                                              |

### 5.10.2 Electrical Specifications Over Recommended Operating Conditions

( $T_{MIN}$  to  $T_{MAX}$ ,  $v_{dda\_dac} = 1.8\text{ V}$ ,  $R_{OUT1/2} = 1650\Omega$ ,  $R_{LOAD} = 75\Omega$ , unless otherwise noted)

**Table 5-21. DAC Static Electrical Specification**

| PARAMETER                |                                             | CONDITIONS/ASSUMPTIONS                                                                              | MIN   | TYP  | MAX   | UNIT |
|--------------------------|---------------------------------------------|-----------------------------------------------------------------------------------------------------|-------|------|-------|------|
| R                        | Resolution                                  |                                                                                                     |       | 10   |       | Bits |
| <b>DC ACCURACY</b>       |                                             |                                                                                                     |       |      |       |      |
| INL <sup>(1)</sup>       | Integral nonlinearity                       |                                                                                                     | 1     |      | 1     | LSB  |
| DNL <sup>(2)</sup>       | Differential nonlinearity                   |                                                                                                     | 1     |      | 1     | LSB  |
| <b>ANALOG OUTPUT</b>     |                                             |                                                                                                     |       |      |       |      |
| -                        | Full-scale output voltage                   | $R_{LOAD} = 75\Omega$                                                                               | 0.7   | 0.88 | 1     | V    |
| -                        | Output offset voltage                       |                                                                                                     |       | 50   |       | mV   |
| -                        | Output offset voltage drift                 |                                                                                                     |       | 20   |       | mV/C |
| -                        | Gain error                                  |                                                                                                     | 17    |      | 19    | % FS |
| $R_{VOUT}$               | Output impedance                            |                                                                                                     | 67.5  | 75   | 82.5  |      |
| <b>REFERENCE</b>         |                                             |                                                                                                     |       |      |       |      |
| $V_{REF}$                | Reference voltage range                     |                                                                                                     | 0.525 | 0.55 | 0.575 | V    |
| -                        | Reference noise density                     | 100-kHz reference noise bandwidth                                                                   |       | 129  |       |      |
| $R_{SET}$                | Full-scale current adjust resistor          |                                                                                                     | 3700  | 4000 | 4200  |      |
| $P_{SRR}$                | Reference PSRR <sup>(3)</sup> (Up to 6 MHz) |                                                                                                     |       | 40   |       | dB   |
| <b>POWER CONSUMPTION</b> |                                             |                                                                                                     |       |      |       |      |
| $I_{vdda-up}$            | Analog Supply Current <sup>(4)</sup>        | 2 channels, no load                                                                                 |       | 8    |       | mA   |
| -                        | Analog supply driving a 75- load (RMS)      | 2 channels                                                                                          |       | 50   |       | mA   |
| $I_{vdda-up (peak)}$     | Peak analog supply current:                 | Lasts less than 1 ns                                                                                |       | 60   |       | mA   |
| $I_{vdd-up}$             | Digital supply current <sup>(5)</sup>       | Measured at $f_{CLK} = 54\text{ MHz}$ , $f_{OUT} = 2\text{ MHz}$ sine wave, $v_{dd} = 1.3\text{ V}$ |       | 2    |       | mA   |
| $I_{vdd-up (peak)}$      | Peak digital supply current <sup>(6)</sup>  | Lasts less than 1 ns                                                                                |       | 2.5  |       | mA   |
| $I_{vdda-down}$          | Analog power at power-down                  | $T = 30^{\circ}\text{C}$ , $v_{dda} = 1.8\text{ V}$                                                 |       | 1.5  |       | mA   |
| $I_{vdd-down}$           | Digital power at power-down                 | $T = 30^{\circ}\text{C}$ , $v_{dd} = 1.3\text{ V}$                                                  |       | 1    |       | mA   |

(1) The INL is measured at the output of the DAC (accessible at an external pin during bypass mode).

(2) The DNL is measured at the output of the DAC (accessible at an external pin during bypass mode).

(3) Assuming a capacitor of 0.1 F at the  $tv\_ref$  node.

(4) The analog supply current  $I_{vdda}$  is directly proportional to the full-scale output current IFS and is insensitive to  $f_{CLK}$ .

(5) The digital supply current  $I_{VDD}$  is dependent on the digital input waveform, the DAC update rate  $f_{CLK}$ , and the digital supply VDD.

(6) The peak digital supply current occurs at full-scale transition for duration less than 1 ns.

( $T_{MIN}$  to  $T_{MAX}$ ,  $v_{dda\_dac} = 1.8\text{ V}$ ,  $R_{OUT1/2} = 1650$ ,  $R_{LOAD} = 75$ , unless otherwise noted)

**Table 5-22. Video DAC Dynamic Electrical Specification**

| PARAMETER       |                                                   | CONDITIONS/ASSUMPTIONS                                                              | MIN | TYP               | MAX | UNIT |
|-----------------|---------------------------------------------------|-------------------------------------------------------------------------------------|-----|-------------------|-----|------|
| $f_{CLK}^{(1)}$ | Output update rate                                | Equal to input clock frequency                                                      |     | 54                |     | MHz  |
|                 | Clock jitter                                      | rms clock jitter required in order to assure 10-bit accuracy                        |     |                   | 40  | ps   |
|                 | Attenuation at 5.1 MHz                            | Corner frequency for signal                                                         | 0.1 | 0.5               | 1.5 | dB   |
|                 | Attenuation at 54 MHz <sup>(1)</sup>              | Image frequency                                                                     | 25  | 30                | 33  | dB   |
| $t_{ST}$        | Output settling time                              | Time from the start of the output transition to output within 1 LSB of final value. |     | 85                |     | ns   |
| $t_{Rout}$      | Output rise time                                  | Measured from 10% to 90% of full-scale transition                                   |     | 25                |     | ns   |
| $t_{Fout}$      | Output fall time                                  | Measured from 10% to 90% of full-scale transition                                   |     | 25                |     | ns   |
| BW              | Signal bandwidth                                  |                                                                                     |     | 6                 |     | MHz  |
|                 | Differential gain <sup>(2)</sup>                  |                                                                                     |     | 1.5%              |     |      |
|                 | Differential phase <sup>(2)</sup>                 |                                                                                     |     | 1                 |     | deg. |
| SFDR            | Within bandwidth                                  | $f_{CLK} = 54\text{ MHz}$ , $f_{OUT} = 1\text{ MHz}$                                |     | 45                |     | dB   |
| SNR             | Signal-to-noise ratio<br>1 kHz to 6 MHz bandwidth | $f_{CLK} = 54\text{ MHz}$ , $f_{OUT} = 1\text{ MHz}$                                |     | 55 <sup>(3)</sup> |     | dB   |
| PSRR            | Power supply rejection ratio                      | Up to 6 MHz                                                                         |     | 20 <sup>(4)</sup> |     | dB   |
| Crosstalk       | Between the two video channels                    |                                                                                     |     | 50                | 40  | dB   |

(1) For internal input clock information, For more information, see the *Device Display Interface Subsystem Reference Guide* [SPRUFV2].

(2) The differential gain and phase value is for dc coupling. Note that there is degradation for the ac coupling.

(3) The SNR value is for dc coupling. Note that there is a 6-dB degradation for ac coupling.

(4) The PSSR value is for dc coupling. Note that there is a 10-dB degradation for ac coupling.

### 5.10.3 Analog Supply (vdda\_dac) Noise Requirements

In order to assure 10-bit accuracy of the DAC analog output, the analog supply vdda\_dac has to meet the noise requirements stated in this section.

The DAC Power Supply Rejection Ratio is defined as the relative variation of the full-scale output current divided by the supply variation. Thus, it is expressed in percentage of Full-Scale Range (FSR) per volt of

$$PSRR_{DAC} = \frac{100 \cdot \frac{\Delta I_{OUT}}{I_{OUTFS}}}{V_{AC}} \quad \left[ \% \text{ FSR} / V \right]$$

supply variation as shown in the following equation:

Depending on frequency, the PSRR is defined in [Table 5-23](#).

**Table 5-23. Video DAC Power Supply Rejection Ratio**

| Supply Noise Frequency | PSRR % FSR/V                                                                     |
|------------------------|----------------------------------------------------------------------------------|
| 0 to 100 kHz           | 1                                                                                |
| > 100 kHz              | The rejection decreases 20 dB/dec.<br>Example: at 1 MHz the PSRR is 10% of FSR/V |

A graphic representation is shown in [Figure 5-12](#).

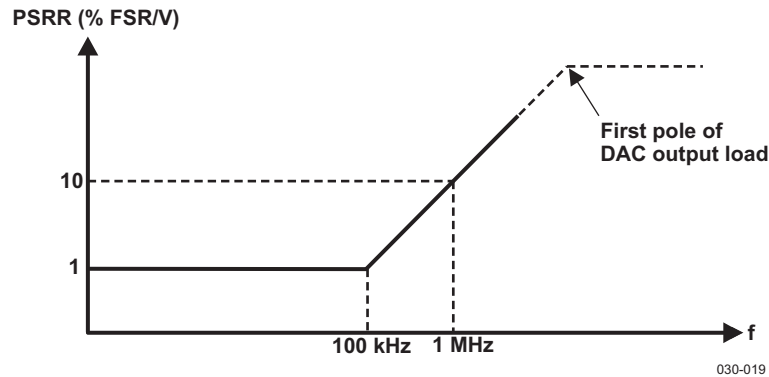


**Figure 5-12. Video DAC Power Supply Rejection Ratio**

To ensure that the DAC SFDR specification is met, the PSRR values and the clock jitter requirements translate to the following limits on vdda\_dac (for the Video DAC).

The maximum peak-to-peak noise on vdda (ripple) is defined in [Table 5-24](#):

**Table 5-24. Video DAC Maximum Peak-to-Peak Noise on vdda\_dac**

| Tone Frequency | Maximum Peak-to-Peak Noise on vdda_dac                          |
|----------------|-----------------------------------------------------------------|
| 0 to 100 kHz   | < 30 mVpp                                                       |
| > 100 kHz      | Decreases 20 dB/dec.<br>Example: at 1 MHz the maximum is 3 mVpp |

The maximum noise spectral density (white noise) is defined in [Table 5-25](#):

**Table 5-25. Video DAC Maximum Noise Spectral Density**

| Supply Noise Bandwidth | Maximum Supply Noise Density                                                                  |
|------------------------|-----------------------------------------------------------------------------------------------|
| 0 to 100 kHz           | < 20 V / $\sqrt{\text{Hz}}$                                                                   |
| > 100 kHz              | Decreases 20 dB/dec.<br>Example: at 1 MHz the maximum noise density is 2 / $\sqrt{\text{Hz}}$ |

Because the DAC PSRR deteriorates at a rate of 20 dB/dec after 100 kHz, it is highly recommended to have vdda\_dac low pass filtered (proper decoupling) (see the illustrated application: [Section 5.10.4, External Component Value Choice](#)).

#### 5.10.4 External Component Value Choice

The full-scale output voltage  $V_{OUTMAX}$  is regulated by the reference amplifier, and is set by an internal resistor  $R_{SET}$ .  $I_{OUTMAX}$  can be expressed as:

$$I_{OUTMAX} = I_{REF} / 8 * (63 + 15/16) \quad (1)$$

Where:

$$V_{REF} = 0.5V \quad (2)$$

$$I_{REF} = V_{REF}/R_{SET} \quad (3)$$

The output current  $I_{OUT}$  appearing at DAC output is a function of both the input code and  $I_{OUTMAX}$  and can be expressed as:

$$I_{OUT} = (DAC\_CODE/1023) * I_{OUTMAX} \quad (4)$$

Where:

$$DAC\_CODE = 0 \text{ to } 1023 \text{ is the DAC input code in decimal.} \quad (5)$$

The output voltage is:

$$V_{OUT} = I_{OUT} * N * R_{CABLE} \quad (6)$$

Where:

$$(N = \text{amplifier gain} = 21) \quad (7)$$

$$R_{CABLE} \Omega \text{ (cable typical impedance)} \quad (8)$$

The TV-out buffer requires a per channel external resistors:  $R_{OUT1/2}$ . The equation below can be used to select different resistor values (if necessary):

$$R_{OUT} = (N+1) R_{CABLE} = 1650\Omega \quad (9)$$

Recommended parameter values are:

**Table 5-26. Video DAC Recommended External Components Values**

|              | Recommended Value | UNIT     |
|--------------|-------------------|----------|
| $C_{BG}$     | 100               | nF       |
| $R_{OUT1/2}$ | 1650              | $\Omega$ |

In order to limit the reference noise bandwidth and to suppress transients on  $V_{REF}$ , it is necessary to connect a large decoupling capacitor ( $C_{BG}$ ) between the tv\_vref and vssa\_dac pins.

## 6 Timing Requirements and Switching Characteristics

**Note:** The timing data shown is *preliminary* data and is subject to change in future revisions.

### 6.1 Timing Test Conditions

All timing requirements and switching characteristics are valid over the recommended operating conditions of [Table 5-3](#), unless otherwise specified.

### 6.2 Interface Clock Specifications

#### 6.2.1 Interface Clock Terminology

The Interface clock is used at the system level to sequence the data and/or control transfers accordingly with the interface protocol.

#### 6.2.2 Interface Clock Frequency

The two interface clock characteristics are:

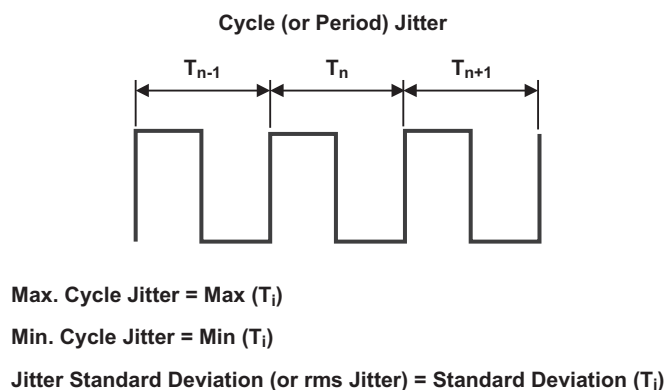
- The maximum clock frequency
- The maximum operating frequency

The interface clock frequency documented in this document is the maximum clock frequency, which corresponds to the maximum frequency programmable on this output clock. This frequency defines the maximum limit supported by the AM3517/05 IC and does not take into account any system consideration (PCB, peripherals).

The system designer will have to consider these system considerations and AM3517/05 IC timings characteristics as well, to define properly the maximum operating frequency, which corresponds to the maximum frequency supported to transfer the data on this interface.

#### 6.2.3 Clock Jitter Specifications

Jitter is a phase noise, which may alter different characteristics of a clock signal. The jitter specified in this document is the time difference between the typical cycle period and the actual cycle period affected by noise sources on the clock. The cycle (or period) jitter terminology identifies this type of jitter.



030-020

**Figure 6-1. Cycle (or Period) Jitter**

### 6.2.4 Clock Duty Cycle Error

The maximum duty cycle error is the difference between the absolute value of the maximum high-level pulse duration or the maximum low-level pulse duration and the typical pulse duration value:

- Maximum pulse duration = typical pulse duration + maximum duty cycle error
- Minimum pulse duration = typical pulse duration - maximum duty cycle error

## 6.3 Timing Parameters

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated as follows:

**Table 6-1. Timing Parameters**

| LOWERCASE SUBSCRIPTS |                                       |
|----------------------|---------------------------------------|
| Symbols              | Parameter                             |
| c                    | Cycle time (period)                   |
| d                    | Delay time                            |
| dis                  | Disable time                          |
| en                   | Enable time                           |
| h                    | Hold time                             |
| su                   | Setup time                            |
| START                | Start bit                             |
| t                    | Transition time                       |
| v                    | Valid time                            |
| w                    | Pulse duration (width)                |
| X                    | Unknown, changing, or dont care level |
| H                    | High                                  |
| L                    | Low                                   |
| V                    | Valid                                 |
| IV                   | Invalid                               |
| AE                   | Active Edge                           |
| FE                   | First Edge                            |
| LE                   | Last Edge                             |
| Z                    | High impedance                        |

## 6.4 External Memory Interfaces

The AM3517/05 processor includes the following external memory interfaces:

- General-purpose memory controller (GPMC)
- SDRAM controller (SDRC)

### 6.4.1 General-Purpose Memory Controller (GPMC)

The GPMC is the AM3517/05 unified memory controller used to interface external memory devices such as:

- Asynchronous SRAM-like memories and ASIC devices
- Asynchronous page mode and synchronous burst NOR flash
- NAND flash

#### 6.4.1.1 GPMC/NOR Flash Interface Synchronous Timing

Table 6-2 through Table 6-4 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-2. GPMC/NOR Flash Synchronous Mode Timing Conditions**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V |     | UNIT |
|----------------------------|-------------------------|------------|-----|------|
|                            |                         | MIN        | MAX |      |
| Input Conditions           |                         |            |     |      |
| t <sub>R</sub>             | Input signal rise time  | 0.3        | 1.8 | ns   |
| t <sub>F</sub>             | Input signal fall time  | 0.3        | 1.8 | ns   |
| Output Conditions          |                         |            |     |      |
| C <sub>LOAD</sub>          | Output load capacitance | 30         |     | pF   |

**Table 6-3. GPMC/NOR Flash Interface Timing Requirements Synchronous Mode**

| NO. | PARAMETER            |                                                                  | 1.8V, 3.3V |     | UNIT |
|-----|----------------------|------------------------------------------------------------------|------------|-----|------|
|     |                      |                                                                  | MIN        | MAX |      |
| F12 | $t_{su}(DV-CLKH)$    | Setup time, read gpmc_d[15:0] valid before gpmc_clk high         | 2.021      |     | ns   |
| F13 | $t_h(CLKH-DV)$       | Hold time, gpmc_d[15:0] valid after gpmc_clk high                | 3.403      |     | ns   |
| F21 | $t_{su}(WAITV-CLKH)$ | Setup time, gpmc_waitx <sup>(1)</sup> valid before gpmc_clk high | 3.782      |     | ns   |
| F22 | $t_h(CLKH-WAITV)$    | Hold Time, gpmc_waitx <sup>(1)</sup> valid after gpmc_clk high   | 3.343      |     | ns   |

(1) Wait monitoring support is limited to a WaitMonitoringTime value > 0.

**Table 6-4. GPMC/NOR Flash Interface Switching Characteristics Synchronous Mode**

| NO. | PARAMETER                |                                                                         | 1.8V, 3.3V              |                        | UNIT |
|-----|--------------------------|-------------------------------------------------------------------------|-------------------------|------------------------|------|
|     |                          |                                                                         | MIN                     | MAX                    |      |
| F0  | $t_{c}(\text{CLK})$      | Cycle time <sup>(1)</sup> , output clock gpmc_clk period                | 10                      |                        | ns   |
| F1  | $t_{w}(\text{CLKH})$     | Typical pulse duration, output clock gpmc_clk high                      | 0.5 P <sup>(2)</sup>    | 0.5 P <sup>(2)</sup>   | ns   |
| F1  | $t_{w}(\text{CLKL})$     | Typical pulse duration, output clock gpmc_clk low                       | 0.5 P <sup>(2)</sup>    | 0.5 P <sup>(2)</sup>   | ns   |
|     | $t_{dc}(\text{CLK})$     | Duty cycle error, output clk gpmc_clk                                   | -500                    | 500                    | ps   |
|     | $t_j(\text{CLK})$        | Jitter standard deviation <sup>(3)</sup> , output clock gpmc_clk        |                         | 33.30                  | ps   |
|     | $t_R(\text{CLK})$        | Rise time, output clock gpmc_clk                                        |                         | 1.6                    | ns   |
|     | $t_F(\text{CLK})$        | Fall time, output clock gpmc_clk                                        |                         | 1.6                    | ns   |
|     | $t_R(\text{DO})$         | Rise time, output data                                                  |                         | 2                      | ns   |
|     | $t_F(\text{DO})$         | Fall time, output data                                                  |                         | 2                      | ns   |
| F2  | $t_d(\text{CLKH-nCSV})$  | Delay time, gpmc_clk rising edge to gpmc_ncsx <sup>(4)</sup> transition | F <sup>(5)</sup> - 1.9  | F <sup>(5)</sup> + 3.3 | ns   |
| F3  | $t_d(\text{CLKH-nCSIV})$ | Delay time, gpmc_clk rising edge to gpmc_ncsx <sup>(4)</sup> invalid    | E <sup>(6)</sup> - 1.9  | E <sup>(6)</sup> + 3.3 | ns   |
| F4  | $t_d(\text{ADDV-CLK})$   | Delay time, address bus valid to gpmc_clk first edge                    | B <sup>(7)</sup> - 4.1  | B <sup>(7)</sup> + 2.1 | ns   |
| F5  | $t_d(\text{CLKH-ADDIV})$ | Delay time, gpmc_clk rising edge to gpmc_a[16:1] invalid                | -2.103                  |                        | ns   |
| F6  | $t_d(\text{nBEV-CLK})$   | Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_clk first edge       | B <sup>(7)</sup> - 1.37 | B <sup>(7)</sup> + 2.1 | ns   |
| F7  | $t_d(\text{CLKH-nBEIV})$ | Delay time, gpmc_clk rising edge to gpmc_nbe0_cle, gpmc_nbe1 invalid    | D <sup>(8)</sup> - 2.1  | D <sup>(8)</sup> + 1.1 | ns   |

(1) Related to the gpmc\_clk output clock maximum and minimum frequencies programmable in the I/F module by setting the GPMC\_CONFIG1\_CSx configuration register bit field GpmcFCLKDivider.

(2) P = gpmc\_clk period

(3) The jitter probability density can be approximated by a Gaussian function.

(4) In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.

(5) **For nCS falling edge (CS activated):**

- **Case GpmcFCLKDivider = 0:**

- $F = 0.5 * \text{CSEExtraDelay} * \text{GPMC\_FCLK}$

- **Case GpmcFCLKDivider = 1:**

- $F = 0.5 * \text{CSEExtraDelay} * \text{GPMC\_FCLK}$  if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)

- $F = (1 + 0.5 * \text{CSEExtraDelay}) * \text{GPMC\_FCLK}$  otherwise

- **Case GpmcFCLKDivider = 2:**

- $F = 0.5 * \text{CSEExtraDelay} * \text{GPMC\_FCLK}$  if ((CSOnTime - ClkActivationTime) is a multiple of 3)

- $F = (1 + 0.5 * \text{CSEExtraDelay}) * \text{GPMC\_FCLK}$  if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)

- $F = (2 + 0.5 * \text{CSEExtraDelay}) * \text{GPMC\_FCLK}$  if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(6) **For single read:**  $E = (\text{CSRdOffTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC\_FCLK}$

**For burst read:**  $E = (\text{CSRdOffTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC\_FCLK}$

**For burst write:**  $E = (\text{CSWrOffTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC\_FCLK}$

(7)  $B = \text{ClkActivationTime} * \text{GPMC\_FCLK}$

(8) **For single read:**  $D = (\text{RdCycleTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC\_FCLK}$

**For burst read:**  $D = (\text{RdCycleTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC\_FCLK}$

**For burst write:**  $D = (\text{WrCycleTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * \text{GPMC\_FCLK}$

**Table 6-4. GPMC/NOR Flash Interface Switching Characteristics Synchronous Mode (continued)**

| NO. | PARAMETER            |                                                              | 1.8V, 3.3V       |                  | UNIT |
|-----|----------------------|--------------------------------------------------------------|------------------|------------------|------|
|     |                      |                                                              | MIN              | MAX              |      |
| F8  | $t_{d(CLKH-nADV)}$   | Delay time, gpmc_clk rising edge to gpmc_nadv_ale transition | $G^{(9)} - 1.9$  | $G^{(9)} + 4.1$  | ns   |
| F9  | $t_{d(CLKH-nADVIV)}$ | Delay time, gpmc_clk rising edge to gpmc_nadv_ale invalid    | $D^{(8)} - 1.9$  | $D^{(8)} + 4.1$  | ns   |
| F10 | $t_{d(CLKH-nOE)}$    | Delay time, gpmc_clk rising edge to gpmc_noie transition     | $H^{(10)} - 2.1$ | $H^{(10)} + 2.1$ | ns   |
| F11 | $t_{d(CLKH-nOEIV)}$  | Delay time, gpmc_clk rising edge to gpmc_noie invalid        | $E^{(6)} - 2.1$  | $E^{(6)} + 2.1$  | ns   |

**(9) For ADV falling edge (ADV activated):**

- **Case GpmcFCLKDivider = 0:**
  - $G = 0.5 * ADVExtraDelay * GPMC\_FCLK$
- **Case GpmcFCLKDivider = 1:**
  - $G = 0.5 * ADVExtraDelay * GPMC\_FCLK$  if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - $G = (1 + 0.5 * ADVExtraDelay) * GPMC\_FCLK$  otherwise
- **Case GpmcFCLKDivider = 2:**
  - $G = 0.5 * ADVExtraDelay * GPMC\_FCLK$  if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 * ADVExtraDelay) * GPMC\_FCLK$  if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 * ADVExtraDelay) * GPMC\_FCLK$  if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

**For ADV rising edge (ADV deactivated) in Reading mode:**

- **Case GpmcFCLKDivider = 0:**
  - $G = 0.5 * ADVExtraDelay * GPMC\_FCLK$
- **Case GpmcFCLKDivider = 1:**
  - $G = 0.5 * ADVExtraDelay * GPMC\_FCLK$  if (ClkActivationTime and ADVrOffTime are odd) or (ClkActivationTime and ADVrOffTime are even)
  - $G = (1 + 0.5 * ADVExtraDelay) * GPMC\_FCLK$  otherwise
- **Case GpmcFCLKDivider = 2:**
  - $G = 0.5 * ADVExtraDelay * GPMC\_FCLK$  if ((ADVrOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 * ADVExtraDelay) * GPMC\_FCLK$  if ((ADVrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 * ADVExtraDelay) * GPMC\_FCLK$  if ((ADVrOffTime - ClkActivationTime - 2) is a multiple of 3)

**For ADV rising edge (ADV deactivated) in Writing mode:**

- **Case GpmcFCLKDivider = 0:**
  - $G = 0.5 * ADVExtraDelay * GPMC\_FCLK$
- **Case GpmcFCLKDivider = 1:**
  - $G = 0.5 * ADVExtraDelay * GPMC\_FCLK$  if (ClkActivationTime and ADVwOffTime are odd) or (ClkActivationTime and ADVwOffTime are even)
  - $G = (1 + 0.5 * ADVExtraDelay) * GPMC\_FCLK$  otherwise
- **Case GpmcFCLKDivider = 2:**
  - $G = 0.5 * ADVExtraDelay * GPMC\_FCLK$  if ((ADVwOffTime - ClkActivationTime) is a multiple of 3)
  - $G = (1 + 0.5 * ADVExtraDelay) * GPMC\_FCLK$  if ((ADVwOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $G = (2 + 0.5 * ADVExtraDelay) * GPMC\_FCLK$  if ((ADVwOffTime - ClkActivationTime - 2) is a multiple of 3)

**(10) For OE falling edge (OE activated) / IO DIR rising edge (Data Bus input direction):**

- **Case GpmcFCLKDivider = 0:**
  - $H = 0.5 * OEExtraDelay * GPMC\_FCLK$
- **Case GpmcFCLKDivider = 1:**
  - $H = 0.5 * OEExtraDelay * GPMC\_FCLK$  if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - $H = (1 + 0.5 * OEExtraDelay) * GPMC\_FCLK$  otherwise
- **Case GpmcFCLKDivider = 2:**
  - $H = 0.5 * OEExtraDelay * GPMC\_FCLK$  if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - $H = (1 + 0.5 * OEExtraDelay) * GPMC\_FCLK$  if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $H = (2 + 0.5 * OEExtraDelay) * GPMC\_FCLK$  if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

**For OE rising edge (OE deactivated):**

- **GpmcFCLKDivider = 0:**
  - $H = 0.5 * OEExtraDelay * GPMC\_FCLK$
- **Case GpmcFCLKDivider = 1:**
  - $H = 0.5 * OEExtraDelay * GPMC\_FC$  if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - $H = (1 + 0.5 * OEExtraDelay) * GPMC\_FCLK$  otherwise
- **Case GpmcFCLKDivider = 2:**
  - $H = 0.5 * OEExtraDelay * GPMC\_FCLK$  if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - $H = (1 + 0.5 * OEExtraDelay) * GPMC\_FCLK$  if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $H = (2 + 0.5 * OEExtraDelay) * GPMC\_FCLK$  if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

**Table 6-4. GPMC/NOR Flash Interface Switching Characteristics Synchronous Mode (continued)**

| NO. | PARAMETER                    |                                                                     | 1.8V, 3.3V       |                  | UNIT |
|-----|------------------------------|---------------------------------------------------------------------|------------------|------------------|------|
|     |                              |                                                                     | MIN              | MAX              |      |
| F14 | $t_{d(\text{CLKH-nWE})}$     | Delay time, gpmc_clk rising edge to gpmc_nwe transition             | $I^{(11)} - 1.9$ | $I^{(11)} + 4.1$ | ns   |
| F15 | $t_{d(\text{CLKH-Data})}$    | Delay time, gpmc_clk rising edge to data bus transition             | $J^{(12)} - 2.1$ | $J^{(12)} + 1.1$ | ns   |
| F17 | $t_{d(\text{CLKH-nBE})}$     | Delay time, gpmc_clk rising edge to gpmc_nbex_cle transition        | $J^{(12)} - 2.1$ | $J^{(12)} + 1.1$ | ns   |
| F18 | $t_{W(\text{nCSV})}$         | Pulse duration, gpmc_ncsx <sup>(4)</sup> low                        | Read             | $A^{(13)}$       | ns   |
|     |                              |                                                                     | Write            | $A^{(13)}$       | ns   |
| F19 | $t_{W(\text{nBEV})}$         | Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 low                        | Read             | $C^{(14)}$       | ns   |
|     |                              |                                                                     | Write            | $C^{(14)}$       | ns   |
| F20 | $t_{W(\text{nADV})}$         | Pulse duration, gpmc_nadv_ale low                                   | Read             | $K^{(15)}$       | ns   |
|     |                              |                                                                     | Write            | $K^{(15)}$       | ns   |
| F23 | $t_{d(\text{CLKH-IODIR})}$   | Delay time, gpmc_clk rising edge to gpmc_io_dir high (IN direction) | $H^{(10)} - 2.1$ | $H^{(10)} + 4.1$ | ns   |
| F24 | $t_{d(\text{CLKH-IODIRIV})}$ | Delay time, gpmc_clk rising edge to gpmc_io_dir low (OUT direction) | $M^{(16)} - 2.1$ | $M^{(16)} + 4.1$ | ns   |

**(11) For WE falling edge (WE activated):**

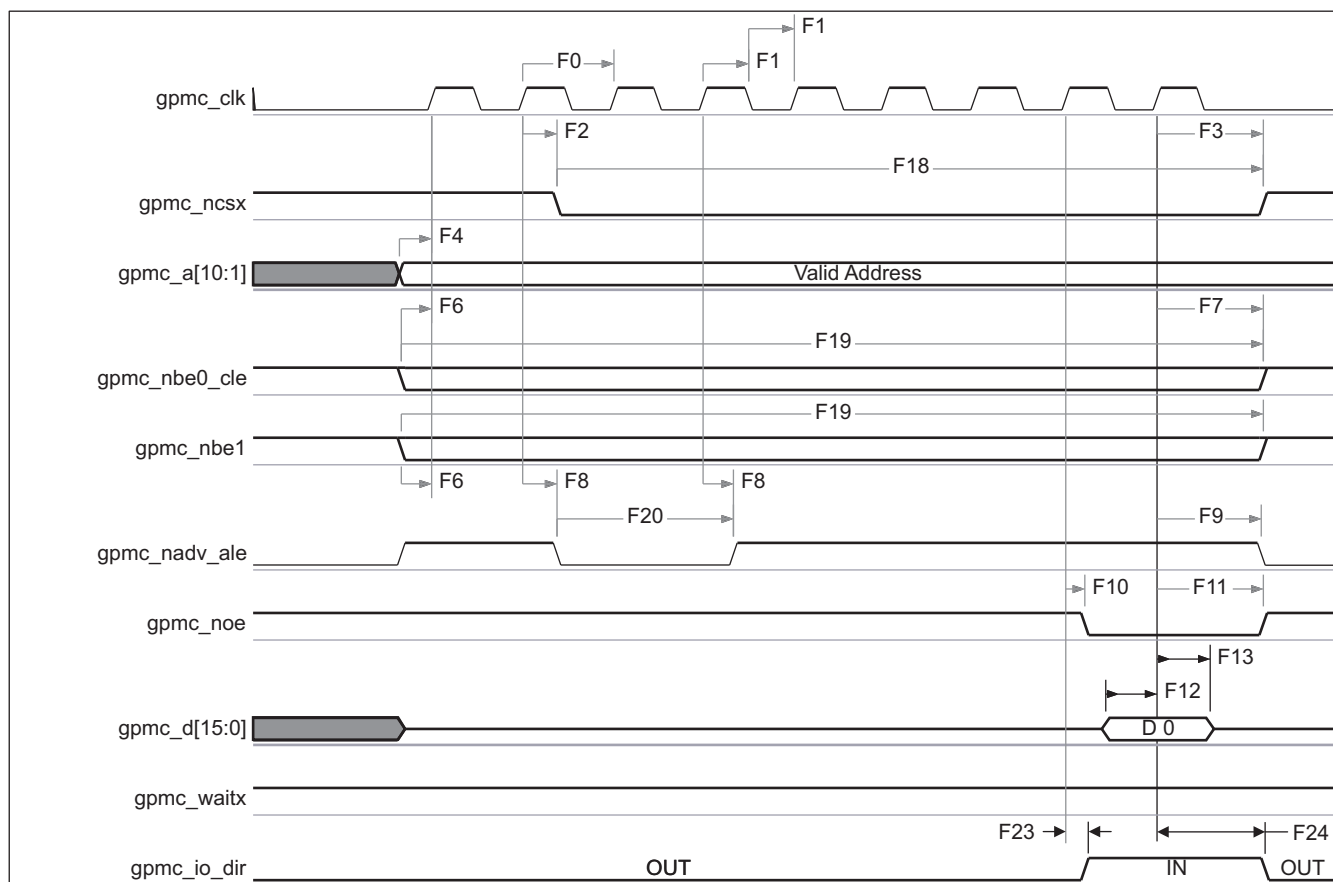
- **Case GpmcFCLKDivider = 0:**
  - $I = 0.5 * WEEExtraDelay * GPMC\_FCLK$
- **Case GpmcFCLKDivider = 1:**
  - $I = 0.5 * WEEExtraDelay * GPMC\_FCLK$  if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - $I = (1 + 0.5 * WEEExtraDelay) * GPMC\_FCLK$  otherwise
- **Case GpmcFCLKDivider = 2:**
  - $I = 0.5 * WEEExtraDelay * GPMC\_FCLK$  if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - $I = (1 + 0.5 * WEEExtraDelay) * GPMC\_FCLK$  if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - $I = (2 + 0.5 * WEEExtraDelay) * GPMC\_FCLK$  if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

**For WE rising edge (WE deactivated):**

- **Case GpmcFCLKDivider = 0:**
  - $I = 0.5 * WEEExtraDelay * GPMC\_FCLK$
- **Case GpmcFCLKDivider = 1:**
  - $I = 0.5 * WEEExtraDelay * GPMC\_FCLK$  if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - $I = (1 + 0.5 * WEEExtraDelay) * GPMC\_FCLK$  otherwise
- **Case GpmcFCLKDivider = 2:**
  - $I = 0.5 * WEEExtraDelay * GPMC\_FCLK$  if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  - $I = (1 + 0.5 * WEEExtraDelay) * GPMC\_FCLK$  if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - $I = (2 + 0.5 * WEEExtraDelay) * GPMC\_FCLK$  if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

**(12)  $J = GPMC\_FCLK$  period****(13) For single read:  $A = (\text{CSRdOffTime} - \text{CSOnTime}) * (\text{TimeParaGranularity} + 1) * GPMC\_FCLK$  period****For burst read:**  $A = (\text{CSRdOffTime} - \text{CSOnTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * GPMC\_FCLK$  period**For burst write:**  $A = (\text{CSWrOffTime} - \text{CSOnTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * GPMC\_FCLK$  period with n being the page burst access number.**(14) For single read:  $C = \text{RdCycleTime} * (\text{TimeParaGranularity} + 1) * GPMC\_FCLK$** **For burst read:**  $C = (\text{RdCycleTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * GPMC\_FCLK$ **For burst write:**  $C = (\text{WrCycleTime} + (n - 1) * \text{PageBurstAccessTime}) * (\text{TimeParaGranularity} + 1) * GPMC\_FCLK$  with n being the page burst access number.**(15) For read:  $K = (\text{ADVrdOffTime} - \text{ADVOnTime}) * (\text{TimeParaGranularity} + 1) * GPMC\_FCLK$** **For write:**  $K = (\text{ADVwrOffTime} - \text{ADVOnTime}) * (\text{TimeParaGranularity} + 1) * GPMC\_FCLK$ **(16)  $M = (\text{RdCycleTime} - \text{AccessTime}) * (\text{TimeParaGranularity} + 1) * GPMC\_FCLK$** 

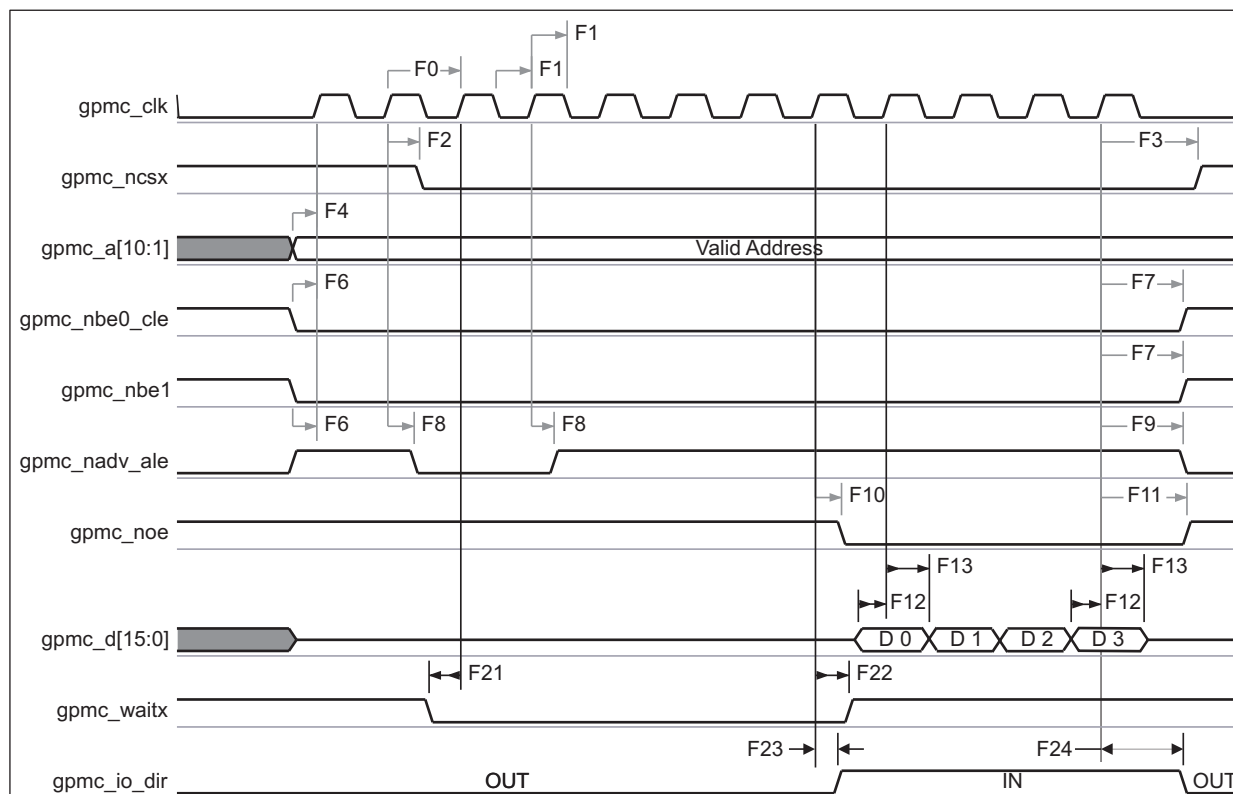
Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behavior of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non-multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behavior is automatically handled by GPMC controller.



030-021

In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.

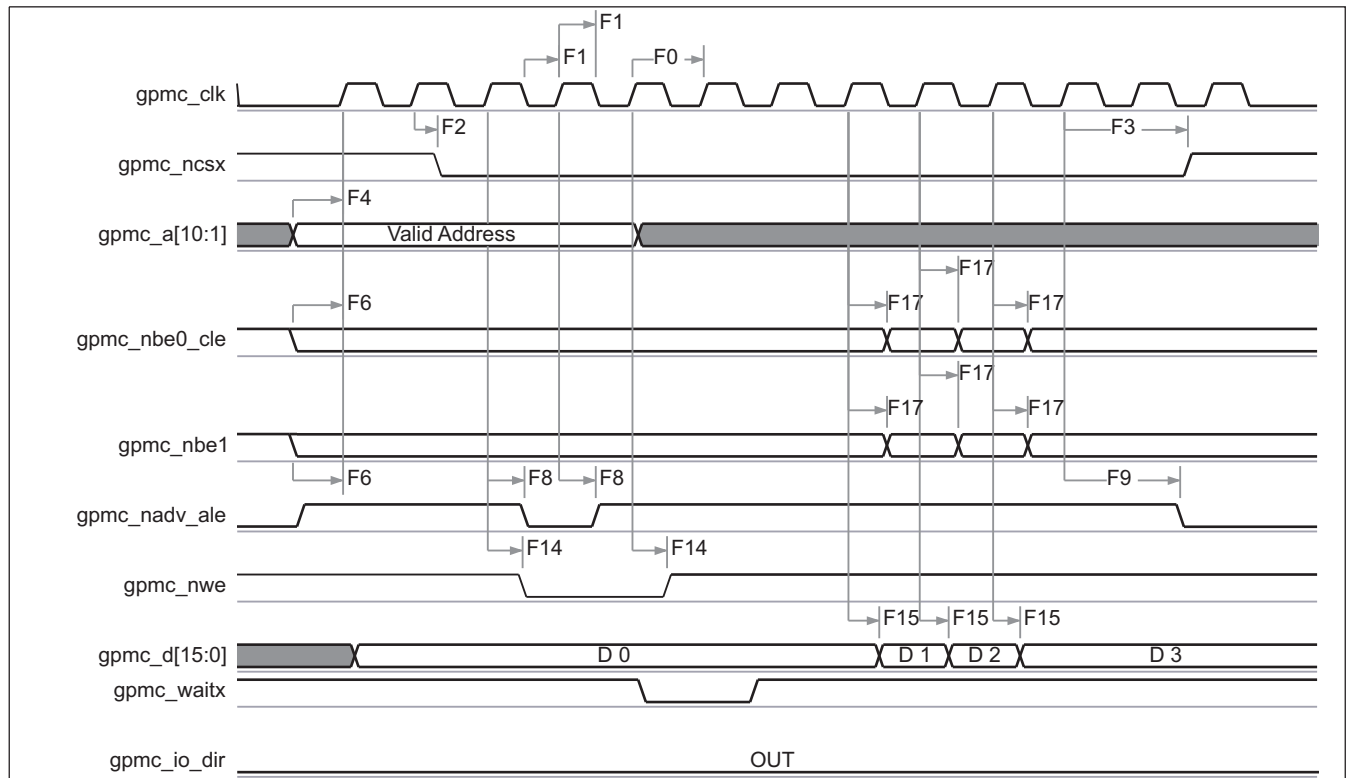
**Figure 6-2. GPMC/NOR Flash Synchronous Single Read (GpmcFCLKDivider = 0)**



030-022

In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.

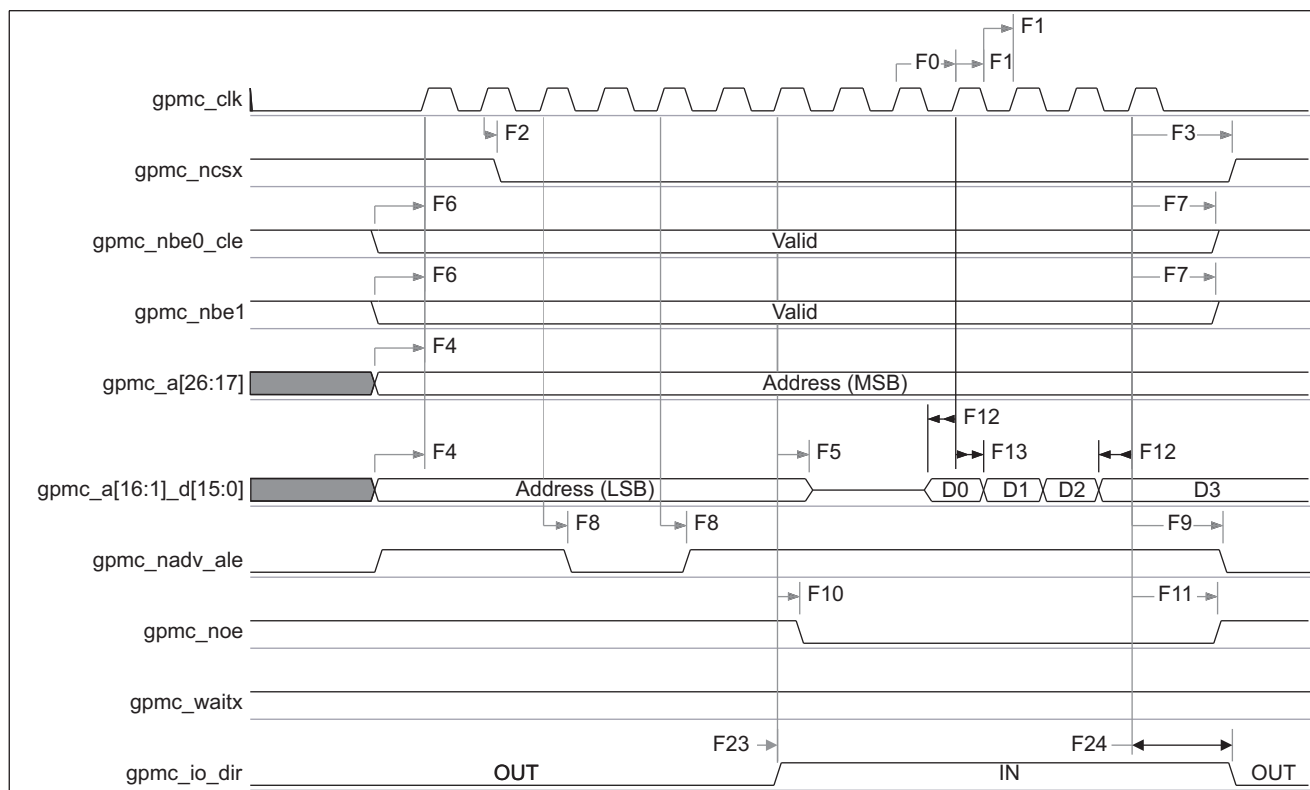
**Figure 6-3. GPMC/NOR Flash Synchronous Burst Read 4x16-bit (GpmcFCLKDivider = 0)**



030-023

In **gpmc\_ncsx**, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In **gpmc\_waitx**, x is equal to 0, 1, 2, or 3.

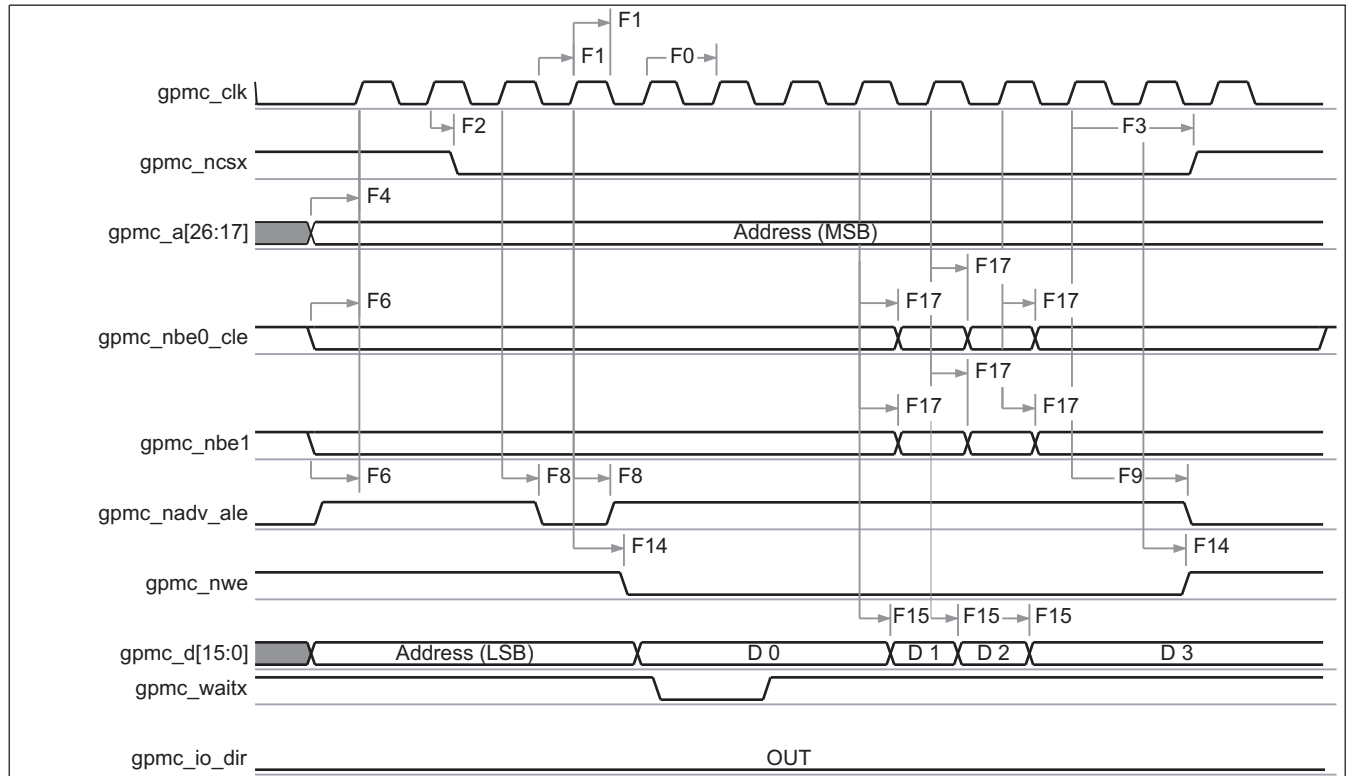
**Figure 6-4. GPMC/NOR Flash Synchronous Burst Write (GpmcFCLKDivider = 0)**



030-024

In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-5. GPMC/Multiplexed NOR Flash Synchronous Burst Read**



030-025

In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-6. GPMC/Multiplexed NOR Flash Synchronous Burst Write**

#### 6.4.1.2 GPMC/NOR Flash Interface Asynchronous Timing

Table 6-5 through Table 6-8 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-5. GPMC/NOR Flash Asynchronous Mode Timing Conditions**

| TIMING CONDITION PARAMETER |                         | VALUE | UNIT |
|----------------------------|-------------------------|-------|------|
| <b>Input Conditions</b>    |                         |       |      |
| $t_R$                      | Input signal rise time  | 1.8   | ns   |
| $t_F$                      | Input signal fall time  | 1.8   | ns   |
| <b>Output Conditions</b>   |                         |       |      |
| $C_{LOAD}$                 | Output load capacitance | 30    | pF   |

**Table 6-6. GPMC/NOR Flash Interface Asynchronous Timing – Internal Parameters<sup>(1) (2)</sup>**

| NO. | PARAMETER                                                             | 1.8V,3.3V |     | UNIT |
|-----|-----------------------------------------------------------------------|-----------|-----|------|
|     |                                                                       | MIN       | MAX |      |
| FI1 | Maximum output data generation delay from internal functional clock   |           | 6.5 | ns   |
| FI2 | Maximum input data capture delay by internal functional clock         |           | 4   | ns   |
| FI3 | Maximum device select generation delay from internal functional clock |           | 6.5 | ns   |
| FI4 | Maximum address generation delay from internal functional clock       |           | 6.5 | ns   |
| FI5 | Maximum address valid generation delay from internal functional clock |           | 6.5 | ns   |
| FI6 | Maximum byte enable generation delay from internal functional clock   |           | 6.5 | ns   |

(1) The internal parameters table must be used to calculate Data Access Time stored in the corresponding CS register bit field.

(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

**Table 6-6. GPMC/NOR Flash Interface Asynchronous Timing – Internal Parameters<sup>(1) (2)</sup> (continued)**

| NO. | PARAMETER                                                             | 1.8V, 3.3V |     | UNIT |
|-----|-----------------------------------------------------------------------|------------|-----|------|
|     |                                                                       | MIN        | MAX |      |
| FI7 | Maximum output enable generation delay from internal functional clock |            | 6.5 | ns   |
| FI8 | Maximum write enable generation delay from internal functional clock  |            | 6.5 | ns   |
| FI9 | Maximum functional clock skew                                         |            | 100 | ps   |

**Table 6-7. GPMC/NOR Flash Interface Timing Requirements – Asynchronous Mode**

| NO.                 | PARAMETER              |                                               | 1.8V, 3.3V |                  | UNIT             |
|---------------------|------------------------|-----------------------------------------------|------------|------------------|------------------|
|                     |                        |                                               | MIN        | MAX              |                  |
| FA5 <sup>(1)</sup>  | $t_{acc}(DAT)$         | Data maximum access time                      |            | H <sup>(2)</sup> | GPMC_FCLK cycles |
| FA20 <sup>(3)</sup> | $t_{acc1-pgmode}(DAT)$ | Page mode successive data maximum access time |            | P <sup>(4)</sup> | GPMC_FCLK cycles |
| FA21 <sup>(5)</sup> | $t_{acc2-pgmode}(DAT)$ | Page mode first data maximum access time      |            | H <sup>(2)</sup> | GPMC_FCLK cycles |

- (1) The FA5 parameter provides the amount of time required to internally sample input Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input Data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
- (2)  $H = AccessTime * (TimeParaGranularity + 1)$
- (3) The FA20 parameter provides amount of time required to internally sample successive input Page Data. It is expressed in number of GPMC functional clock cycles. After each access to input Page Data, next input Page Data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
- (4)  $P = PageBurstAccessTime * (TimeParaGranularity + 1)$
- (5) The FA21 parameter shows amount of time required to internally sample first input Page Data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, First input Page Data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.

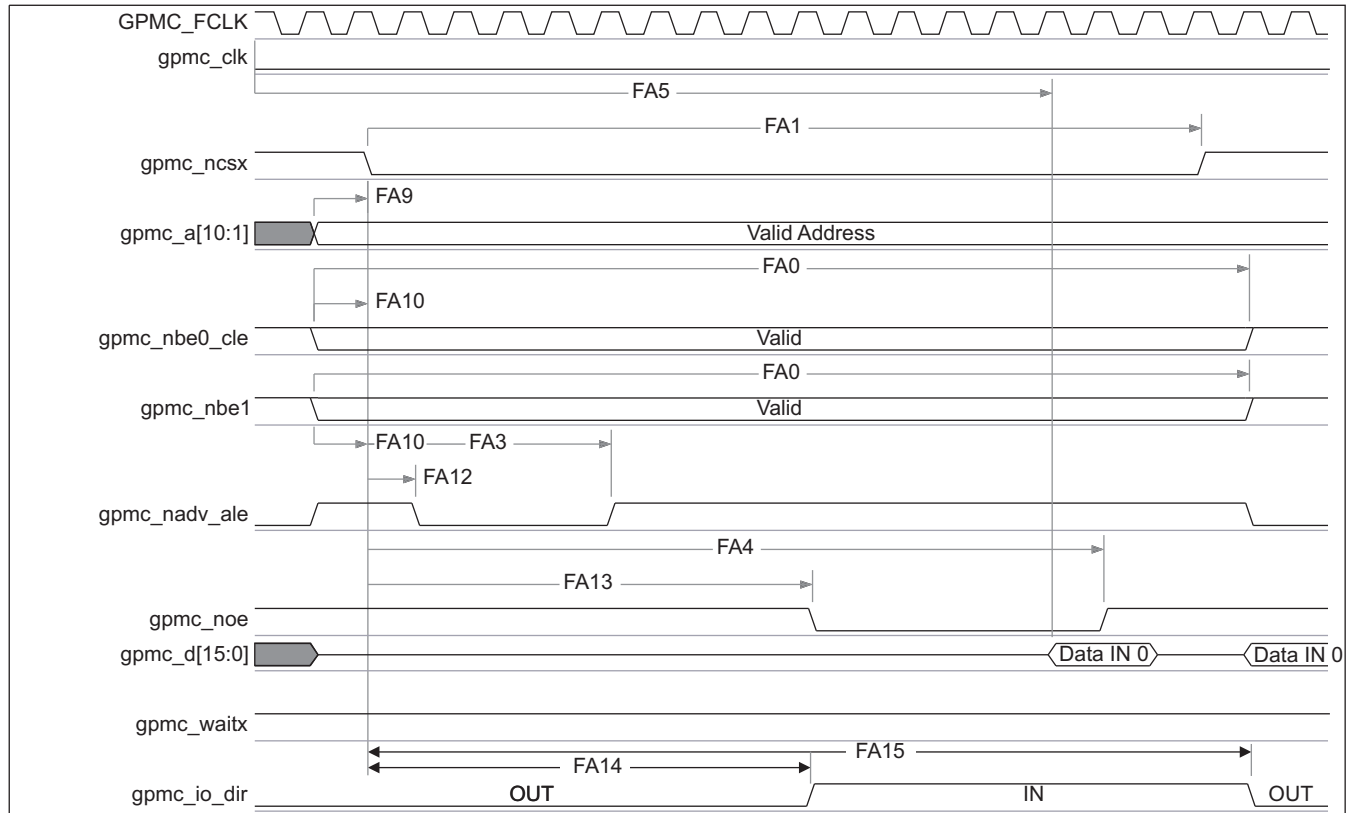
**Table 6-8. GPMC/NOR Flash Interface Switching Characteristics – Asynchronous Mode**

| NO.  | PARAMETER            |                                                                   |       | 1.8V/ 3.3V  |             | UNIT |
|------|----------------------|-------------------------------------------------------------------|-------|-------------|-------------|------|
|      |                      |                                                                   |       | MIN         | MAX         |      |
|      | $t_{R(DO)}$          | Rise time, output data                                            |       |             | 2.0         | ns   |
|      | $t_{F(DO)}$          | Fall time, output data                                            |       |             | 2.0         | ns   |
| FA0  | $t_{W(nBEV)}$        | Pulse duration, gpmc_nbe0_cle, gpmc_nbe1 valid time               | Read  | N(12)       |             | ns   |
|      |                      |                                                                   | Write | N(12)       |             | ns   |
| FA1  | $t_{W(nCSV)}$        | Pulse duration, gpmc_ncsx(13) v low                               | Read  | A(1)        |             | ns   |
|      |                      |                                                                   | Write | A(1)        |             | ns   |
| FA3  | $t_{d(nCSV-nADVIV)}$ | Delay time, gpmc_ncsx(13) valid to gpmc_nadv_ale invalid          | Read  | B(2) – 0.2  | B(2) + 2.0  | ns   |
|      |                      |                                                                   | Write | B(2) – 0.2  | B(2) + 2.0  | ns   |
| FA4  | $t_{d(nCSV-nOEIV)}$  | Delay time, gpmc_ncsx(13) valid to gpmc_noe invalid (Single read) |       | C(3) – 0.2  | C(3) + 2.0  | ns   |
| FA9  | $t_{d(AV-nCSV)}$     | Delay time, address bus valid to gpmc_ncsx(13) valid              |       | J(9) – 0.2  | J(9) + 2.0  | ns   |
| FA10 | $t_{d(nBEV-nCSV)}$   | Delay time, gpmc_nbe0_cle, gpmc_nbe1 valid to gpmc_ncsx(13) valid |       | J(9) – 0.2  | J(9) + 2.0  | ns   |
| FA12 | $t_{d(nCSV-nADVIV)}$ | Delay time, gpmc_ncsx(13) valid to gpmc_nadv_ale valid            |       | K(10) – 0.2 | K(10) + 2.0 | ns   |
| FA13 | $t_{d(nCSV-nOEV)}$   | Delay time, gpmc_ncsx(13) valid to gpmc_noe valid                 |       | L(11) – 0.2 | L(11) + 2.0 | ns   |
| FA14 | $t_{d(nCSV-nODIR)}$  | Delay time, gpmc_ncsx(13) valid to gpmc_io_dir high               |       | L(11) – 0.2 | L(11) + 2.0 | ns   |
| FA15 | $t_{d(nCSV-nIDIR)}$  | Delay time, gpmc_ncsx(13) valid to gpmc_io_dir low                |       | M(14) – 0.2 | M(14) + 2.0 | ns   |
| FA16 | $t_{W(AIV)}$         | Address invalid duration between 2 successive R/W accesses        |       | G(7)        |             | ns   |

**Table 6-8. GPMC/NOR Flash Interface Switching Characteristics – Asynchronous Mode (continued)**

| NO.  | PARAMETER           |                                                                      | 1.8V/ 3.3V |            | UNIT |
|------|---------------------|----------------------------------------------------------------------|------------|------------|------|
|      |                     |                                                                      | MIN        | MAX        |      |
| FA18 | $t_{d(nCSV-nOEIV)}$ | Delay time, gpmc_ncsx(13) valid to gpmc_noe invalid (Burst read)     | I(8) – 0.2 | I(8) + 2.0 | ns   |
| FA20 | $t_{w(AV)}$         | Pulse duration, address valid – 2nd, 3rd, and 4th accesses           | D(4)       |            | ns   |
| FA25 | $t_{d(nCSV-nWEV)}$  | Delay time, gpmc_ncsx(13) valid to gpmc_nwe valid                    | E(5) – 0.2 | E(5) + 2.0 | ns   |
| FA27 | $t_{d(nCSV-nWEIV)}$ | Delay time, gpmc_ncsx(13) valid to gpmc_nwe invalid                  | F(6) – 0.2 | F(6) + 2.0 | ns   |
| FA28 | $t_{d(nWEV-DV)}$    | Delay time, gpmc_new valid to data bus valid                         |            | 2.0        | ns   |
| FA29 | $t_{d(DV-nCSV)}$    | Delay time, data bus valid to gpmc_ncsx(13) valid                    | J(9) – 0.2 | J(9) + 2.0 | ns   |
| FA37 | $t_{d(nOEIV-AIV)}$  | Delay time, gpmc_noe valid to gpmc_a[16:1]_d[15:0] address phase end |            | 2.0        | ns   |

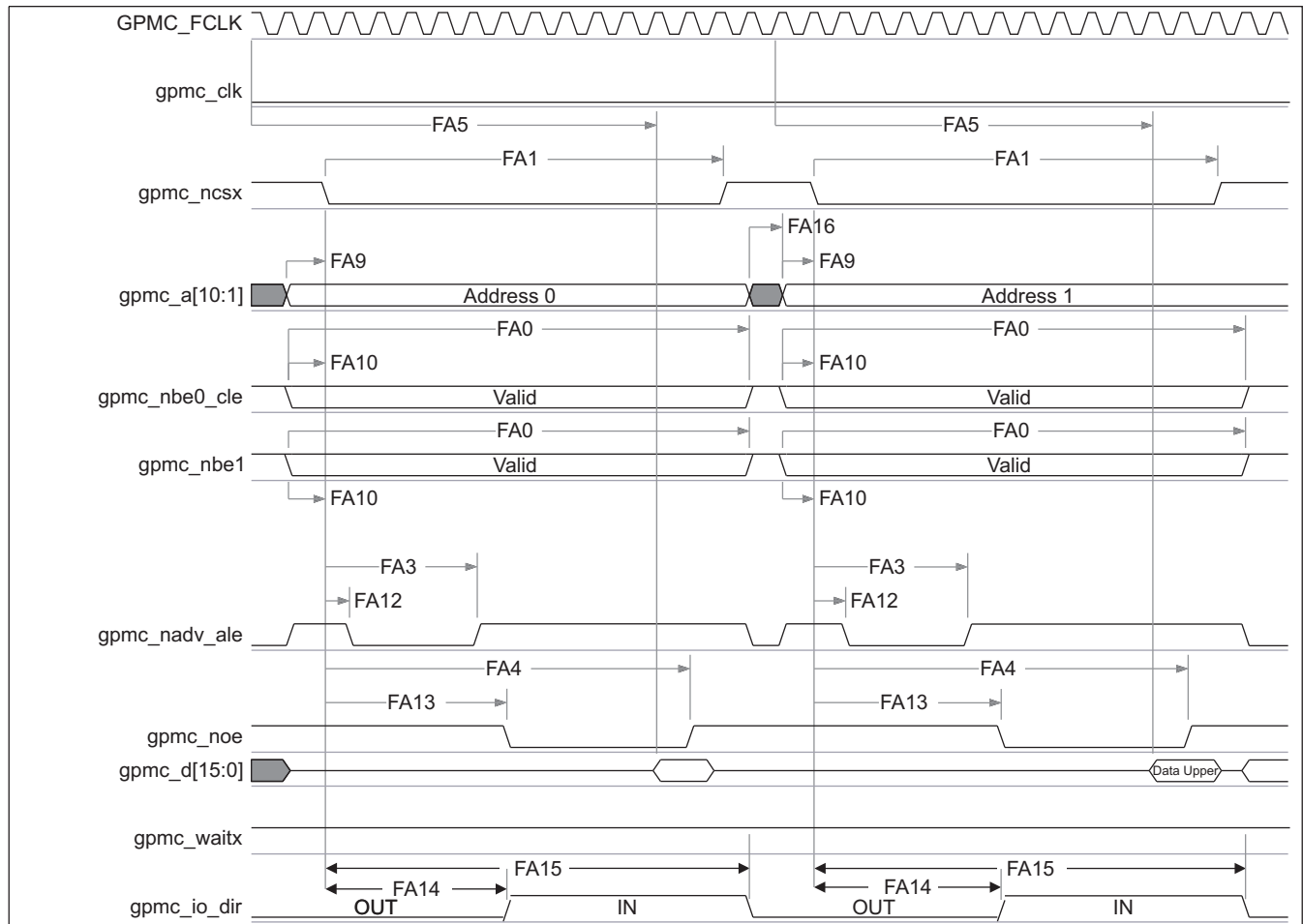
- (1) **For single read:**  $A = (CSRdOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC\_FCLK$   
**For single write:**  $A = (CSWrOffTime - CSOnTime) * (TimeParaGranularity + 1) * GPMC\_FCLK$   
**For burst read:**  $A = (CSRdOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC\_FCLK$   
**For burst write:**  $A = (CSWrOffTime - CSOnTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC\_FCLK$  with n being the page burst access number
- (2) **For reading:**  $B = ((ADVrdOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSEExtraDelay)) * GPMC\_FCLK$   
**For writing:**  $B = ((ADVWrOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSEExtraDelay)) * GPMC\_FCLK$
- (3)  $C = ((OEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSEExtraDelay)) * GPMC\_FCLK$
- (4)  $D = PageBurstAccessTime * (TimeParaGranularity + 1) * GPMC\_FCLK$
- (5)  $E = ((WEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEEExtraDelay - CSEExtraDelay)) * GPMC\_FCLK$
- (6)  $F = ((WEOffTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEEExtraDelay - CSEExtraDelay)) * GPMC\_FCLK$
- (7)  $G = Cycle2CycleDelay * GPMC\_FCLK$
- (8)  $I = ((OEOffTime + (n - 1) * PageBurstAccessTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSEExtraDelay)) * GPMC\_FCLK$
- (9)  $J = (CSOnTime * (TimeParaGranularity + 1) + 0.5 * CSEExtraDelay) * GPMC\_FCLK$
- (10)  $K = ((ADVOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - CSEExtraDelay)) * GPMC\_FCLK$
- (11)  $L = ((OEOnTime - CSOnTime) * (TimeParaGranularity + 1) + 0.5 * (OEExtraDelay - CSEExtraDelay)) * GPMC\_FCLK$
- (12) **For single read:**  $N = RdCycleTime * (TimeParaGranularity + 1) * GPMC\_FCLK$   
**For single write:**  $N = WrCycleTime * (TimeParaGranularity + 1) * GPMC\_FCLK$   
**For burst read:**  $N = (RdCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC\_FCLK$   
**For burst write:**  $N = (WrCycleTime + (n - 1) * PageBurstAccessTime) * (TimeParaGranularity + 1) * GPMC\_FCLK$
- (13) In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.
- (14)  $M = ((RdCycleTime - CSOnTime) * (TimeParaGranularity + 1) - 0.5 * CSEExtraDelay) * GPMC\_FCLK$   
Above M parameter expression is given as one example of GPMC programming. IO DIR signal will go from IN to OUT after both RdCycleTime and BusTurnAround completion. Behavior of IO direction signal does depend on kind of successive Read/Write accesses performed to Memory and multiplexed or non-multiplexed memory addressing scheme, bus keeping feature enabled or not. IO DIR behavior is automatically handled by GPMC controller.



030-026

**Figure 6-7. GPMC/NOR Flash – Asynchronous Read – Single Word Timing(1) (2) (3)**

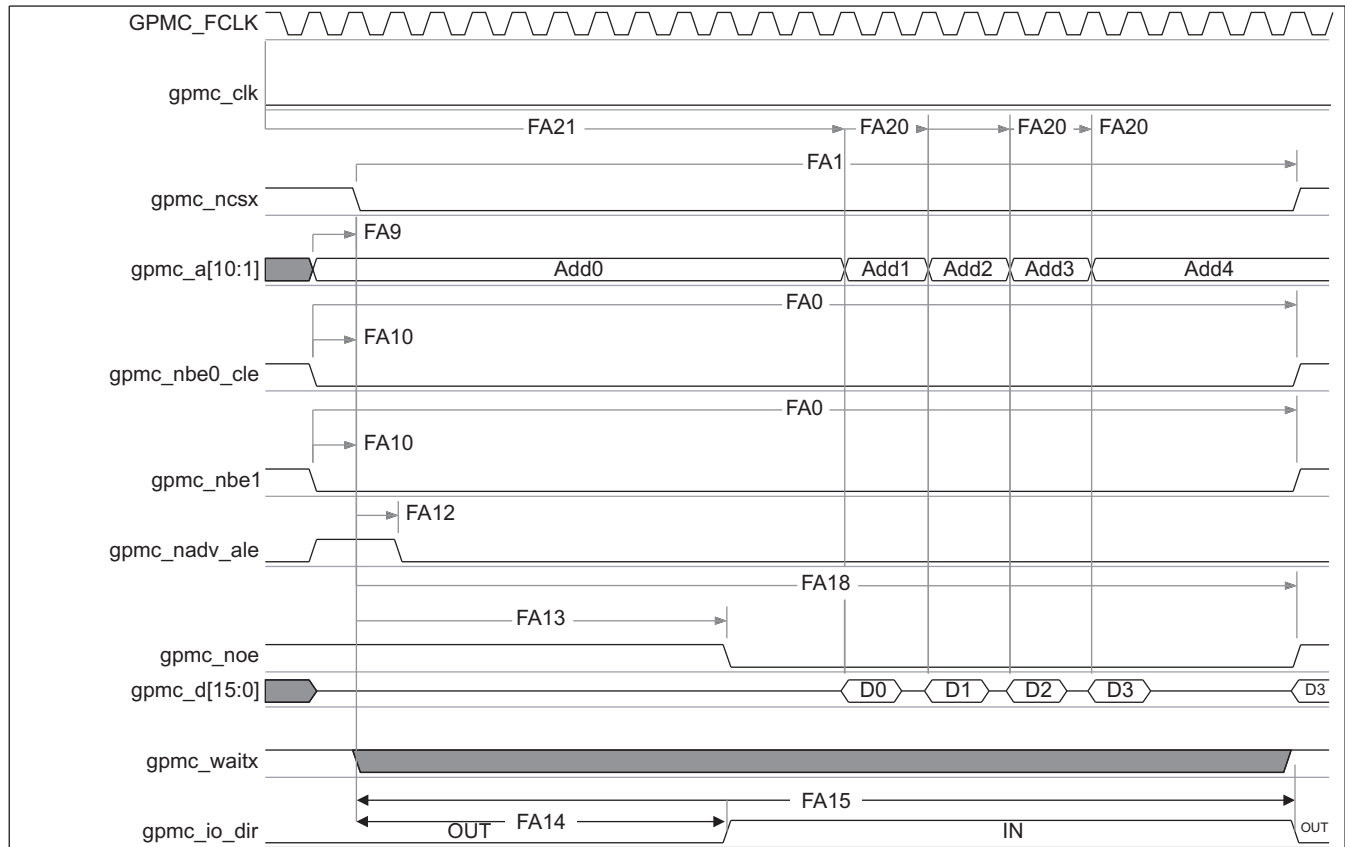
- (1) In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.
- (2) FA5 parameter provides amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bit field.
- (3) GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.



030-027

**Figure 6-8. GPMC/NOR Flash – Asynchronous Read – 32-bit Timing(1) (2) (3)**

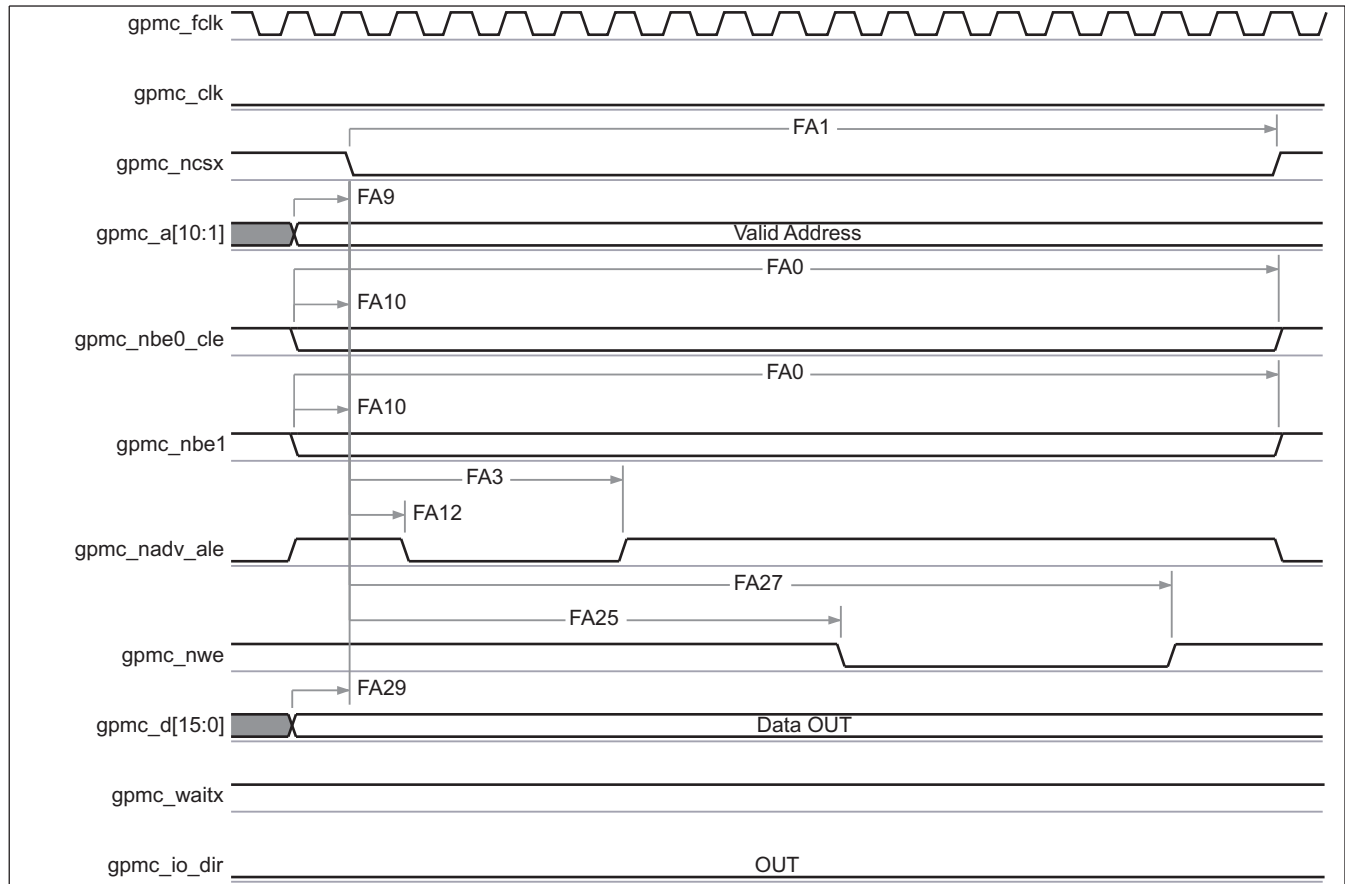
- (1) In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.
- (2) FA5 parameter provides amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bit field.
- (3) GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.



030-028

**Figure 6-9. GPMC/NOR Flash – Asynchronous Read – Page Mode 4x16-bit Timing(1) (2) (3) (4)**

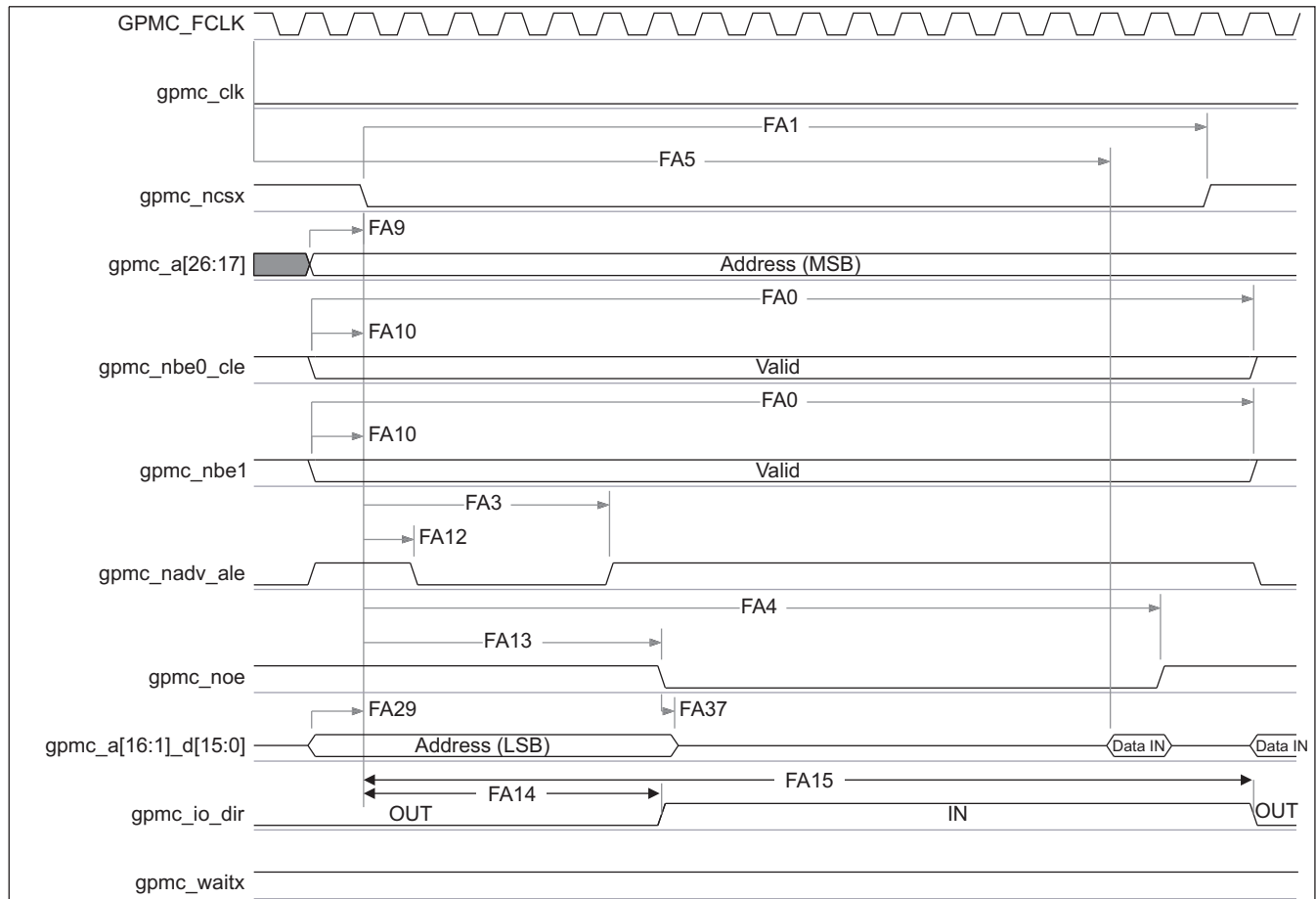
- (1) In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.
- (2) FA21 parameter provides amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside AccessTime register bit field.
- (3) FA20 parameter provides amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bit field.
- (4) GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.



030-029

In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.

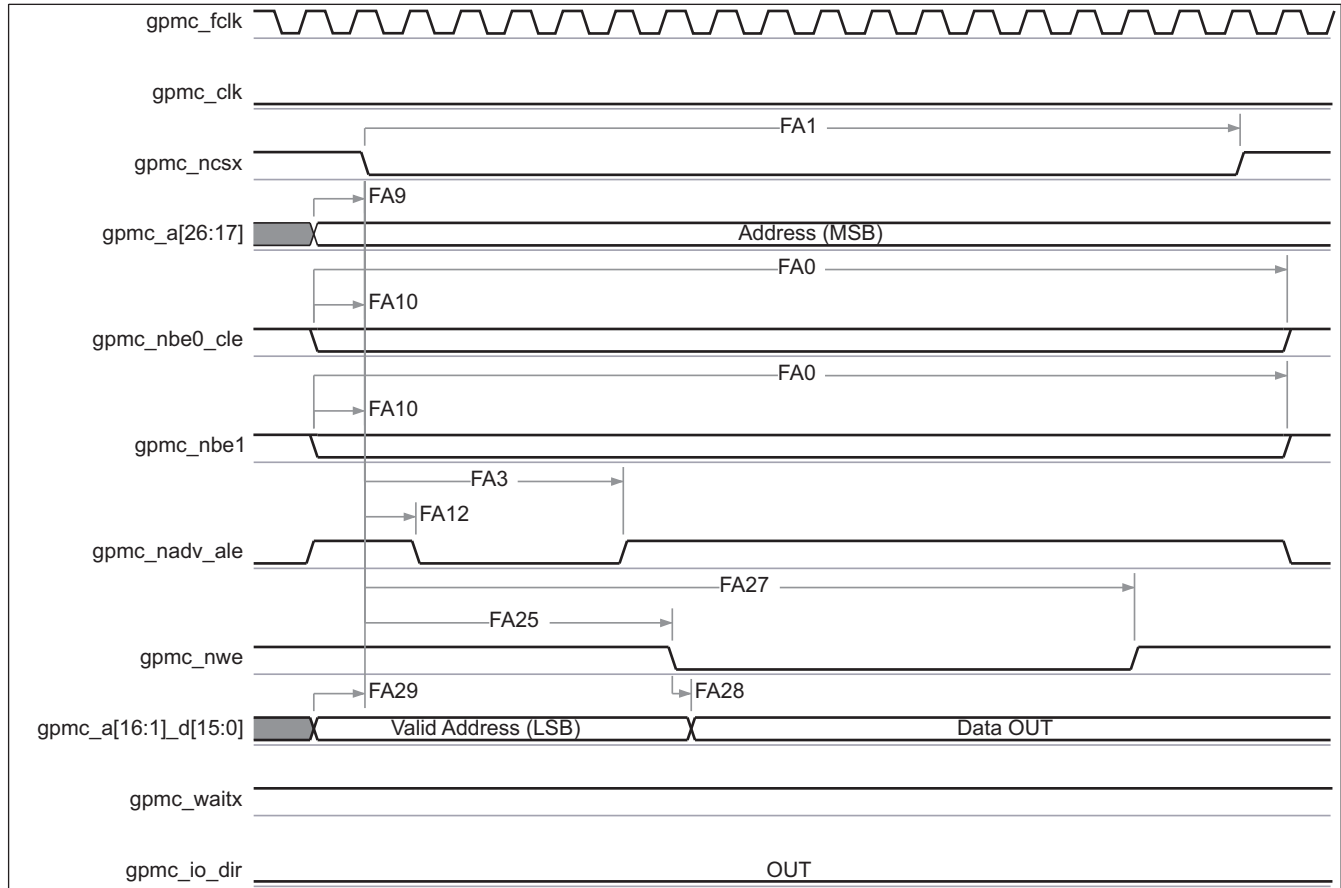
**Figure 6-10. GPMC/NOR Flash – Asynchronous Write – Single Word Timing**



030-030

**Figure 6-11. GPMC/Multiplexed NOR Flash – Asynchronous Read – Single Word Timing(1) (2) (3)**

- (1) In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.
- (2) FA5 parameter provides amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bit field.
- (3) GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.



030-031

In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.

**Figure 6-12. GPMC/Multiplexed NOR Flash – Asynchronous Write – Single Word Timing**

#### 6.4.1.3 GPMC/NAND Flash Interface Timing

Table 6-9 through Table 6-12 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-9. GPMC/NAND Flash Asynchronous Mode Timing Conditions**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V |     | UNIT |
|----------------------------|-------------------------|------------|-----|------|
|                            |                         | MIN        | MAX |      |
| Input Conditions           |                         |            |     |      |
| t <sub>R</sub>             | Input signal rise time  |            | 1.8 | ns   |
| t <sub>F</sub>             | Input signal fall time  |            | 1.8 | ns   |
| C <sub>LOAD</sub>          | Output load capacitance | 30         |     | pF   |

**Table 6-10. GPMC/NAND Flash Interface Asynchronous Timing Internal Parameters<sup>(1) (2)</sup>**

| NO.   | PARAMETER                                                                    | 1.8V, 3.3V |     | UNIT |
|-------|------------------------------------------------------------------------------|------------|-----|------|
|       |                                                                              | MIN        | MAX |      |
| GNFI1 | Maximum output data generation delay from internal functional clock          |            | 6.5 | ns   |
| GNFI2 | Maximum input data capture delay by internal functional clock                |            | 4   | ns   |
| GNFI3 | Maximum device select generation delay from internal functional clock        |            | 6.5 | ns   |
| GNFI4 | Maximum address latch enable generation delay from internal functional clock |            | 6.5 | ns   |
| GNFI5 | Maximum command latch enable generation delay from internal functional clock |            | 6.5 | ns   |
| GNFI6 | Maximum output enable generation delay from internal functional clock        |            | 6.5 | ns   |
| GNFI7 | Maximum write enable generation delay from internal functional clock         |            | 6.5 | ns   |
| GNFI8 | Maximum functional clock skew                                                |            | 100 | ps   |

(1) Internal parameters table must be used to calculate data access time stored in the corresponding CS register bit field.

(2) Internal parameters are referred to the GPMC functional internal clock which is not provided externally.

**Table 6-11. GPMC/NAND Flash Interface Timing Requirements**

| NO.                  | PARAMETER      |                          | 1.8V, 3.3V |                  | UNIT             |
|----------------------|----------------|--------------------------|------------|------------------|------------------|
|                      |                |                          | MIN        | MAX              |                  |
| GNF12 <sup>(1)</sup> | $t_{acc(DAT)}$ | Data maximum access time |            | J <sup>(2)</sup> | GPMC_FCLK cycles |

(1) The GNF12 parameter provides the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.

(2)  $J = \text{AccessTime} * (\text{TimeParaGranularity} + 1)$

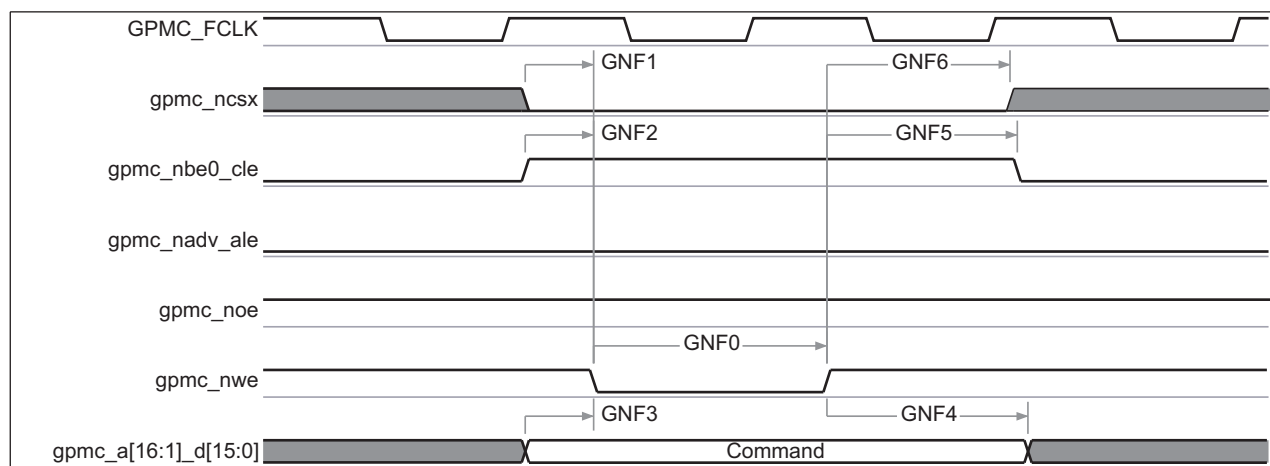
**Table 6-12. GPMC/NAND Flash Interface Switching Characteristics**

| NO.    | PARAMETER            |                                                       | 1.8V, 3.3V |            | UNIT |
|--------|----------------------|-------------------------------------------------------|------------|------------|------|
|        |                      |                                                       | MIN        | MAX        |      |
|        | $t_{R(DO)}$          | Rise time, output data                                |            | 2.0        | ns   |
|        | $t_{F(DO)}$          | Fall time, output data                                |            | 2.0        | ns   |
| GNF0   | $t_{W(nWEV)}$        | Pulse duration, gpmc_nwe valid time                   | A(1)       |            | ns   |
| GNF1   | $t_{d(nCSV-nWEV)}$   | Delay time, gpmc_ncsx(13) valid to gpmc_nwe valid     | B(2) - 0.2 | B(2) + 2.0 | ns   |
| GNF2   | $t_{W(CLEH-nWEV)}$   | Delay time, gpmc_nbe0_cle high to gpmc_nwe valid      | C(3) - 0.2 | C(3) + 2.0 | ns   |
| GNF3   | $t_{W(nWEV-DV)}$     | Delay time, gpmc_d[15:0] valid to gpmc_nwe valid      | D(4) - 0.2 | D(4) + 2.0 | ns   |
| GNF4   | $t_{W(nWEIV-DIV)}$   | Delay time, gpmc_nwe invalid to gpmc_d[15:0] invalid  | E(5) - 0.2 | E(5) + 2.0 | ns   |
| GNF5   | $t_{W(nWEIV-CLEIV)}$ | Delay time, gpmc_nwe invalid to gpmc_nbe0_cle invalid | F(6) - 0.2 | F(6) + 2.0 | ns   |
| GNF6   | $t_{W(nWEIV-nCSV)}$  | Delay time, gpmc_nwe invalid to gpmc_ncsx(13) invalid | G(7) - 0.2 | G(7) + 2.0 | ns   |
| GNF7   | $t_{W(ALEH-nWEV)}$   | Delay time, gpmc_nadv_ale High to gpmc_nwe valid      | C(3) - 0.2 | C(3) + 2.0 | ns   |
| GNF8   | $t_{W(nWEIV-ALEIV)}$ | Delay time, gpmc_nwe invalid to gpmc_nadv_ale invalid | F(6) - 0.2 | F(6) + 2.0 | ns   |
| GNF9   | $t_{c(nWE)}$         | Cycle time, Write cycle time                          | H(8)       |            | ns   |
| GNF10  | $t_{d(nCSV-nOEIV)}$  | Delay time, gpmc_ncsx(13) valid to gpmc_noe valid     | I(9) - 0.2 | I(9) + 2.0 | ns   |
| GNF13  | $t_{W(nOEIV)}$       | Pulse duration, gpmc_noe valid time                   | K(10)      |            | ns   |
| GN F14 | $t_{c(nOE)}$         | Cycle time, Read cycle time                           | L(11)      |            | ns   |

**Table 6-12. GPMC/NAND Flash Interface Switching Characteristics (continued)**

| NO.   | PARAMETER            |                                                       | 1.8V, 3.3V  |             | UNIT |
|-------|----------------------|-------------------------------------------------------|-------------|-------------|------|
|       |                      |                                                       | MIN         | MAX         |      |
| GNF15 | $t_{w(nOEIV-nCSIV)}$ | Delay time, gpmc_noe invalid to gpmc_ncsx(13) invalid | M(12) - 0.2 | M(12) + 2.0 | ns   |

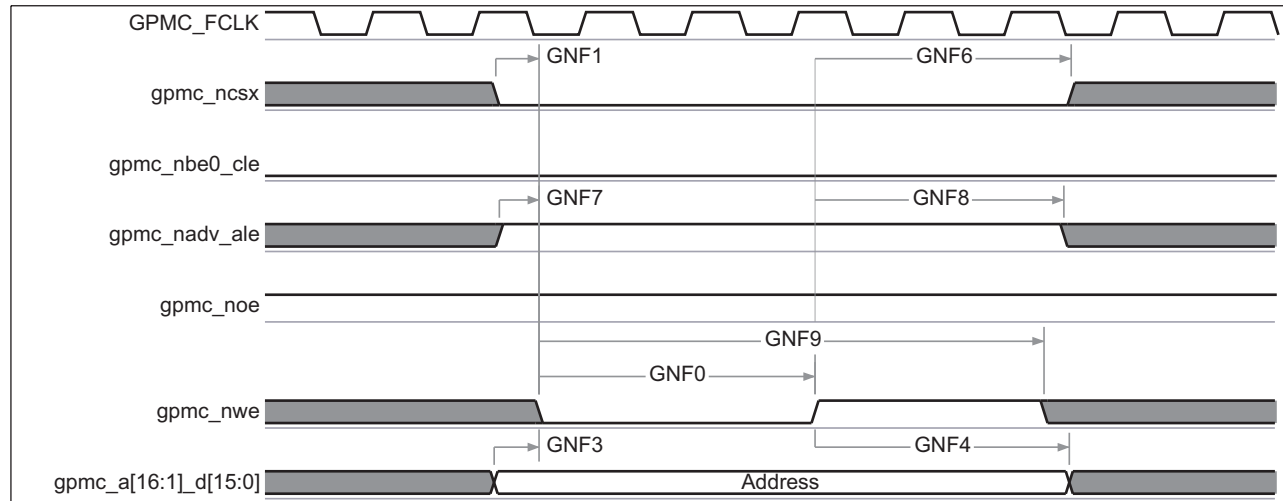
- (1)  $A = (WEOffTime - WEOnTime) * (TimeParaGranularity + 1) * GPMC\_FCLK$   
 (2)  $B = ((WEOnTime - CSONTime) * (TimeParaGranularity + 1) + 0.5 * (WEEExtraDelay - CSEExtraDelay)) * GPMC\_FCLK$   
 (3)  $C = ((WEOnTime - ADVOnTime) * (TimeParaGranularity + 1) + 0.5 * (WEEExtraDelay - ADVExtraDelay)) * GPMC\_FCLK$   
 (4)  $D = (WEOnTime * (TimeParaGranularity + 1) + 0.5 * WEEExtraDelay) * GPMC\_FCLK$   
 (5)  $E = (WrCycleTime - WEOffTime * (TimeParaGranularity + 1) - 0.5 * WEEExtraDelay) * GPMC\_FCLK$   
 (6)  $F = (ADVWrOffTime - WEOffTime * (TimeParaGranularity + 1) + 0.5 * (ADVExtraDelay - WEEExtraDelay)) * GPMC\_FCLK$   
 (7)  $G = (CSWrOffTime - WEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSEExtraDelay - WEEExtraDelay)) * GPMC\_FCLK$   
 (8)  $H = WrCycleTime * (1 + TimeParaGranularity) * GPMC\_FCLK$   
 (9)  $I = ((OEOnTime - CSONTime) * (TimeParaGranularity + 1) + 0.5 * (OEEExtraDelay - CSEExtraDelay)) * GPMC\_FCLK$   
 (10)  $K = (OEOffTime - OEOnTime) * (1 + TimeParaGranularity) * GPMC\_FCLK$   
 (11)  $L = RdCycleTime * (1 + TimeParaGranularity) * GPMC\_FCLK$   
 (12)  $M = (CSRdOffTime - OEOffTime * (TimeParaGranularity + 1) + 0.5 * (CSEExtraDelay - OEEExtraDelay)) * GPMC\_FCLK$   
 (13) In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.



030-032

In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

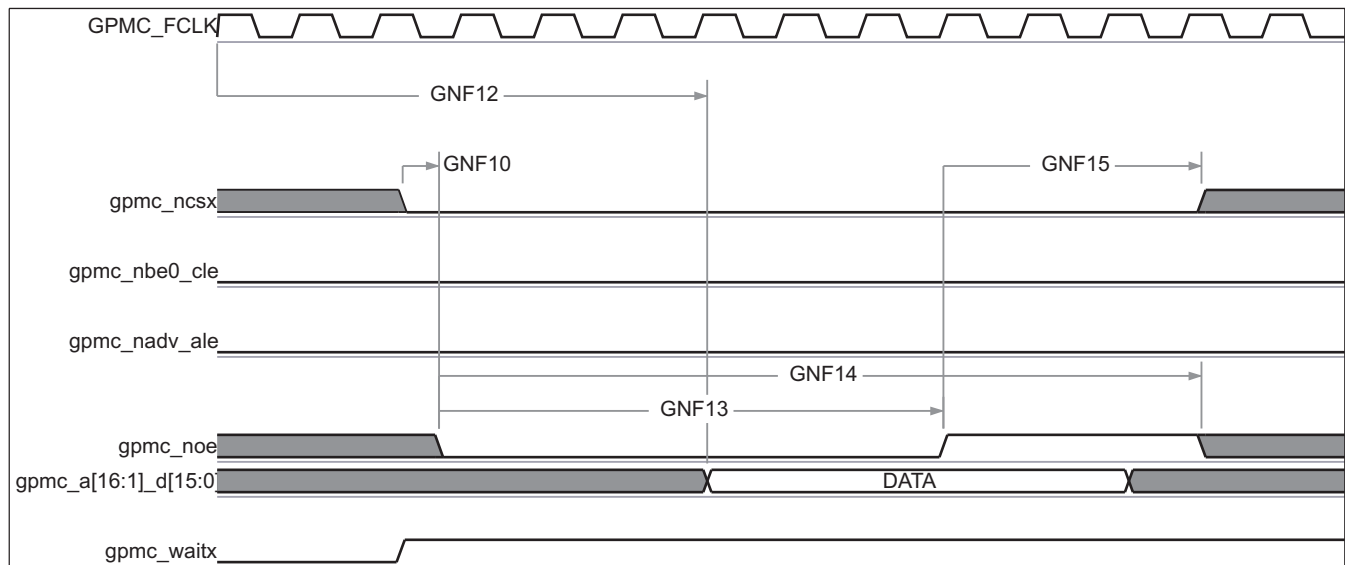
**Figure 6-13. GPMC/NAND Flash – Command Latch Cycle Timing**



030-033

In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7.

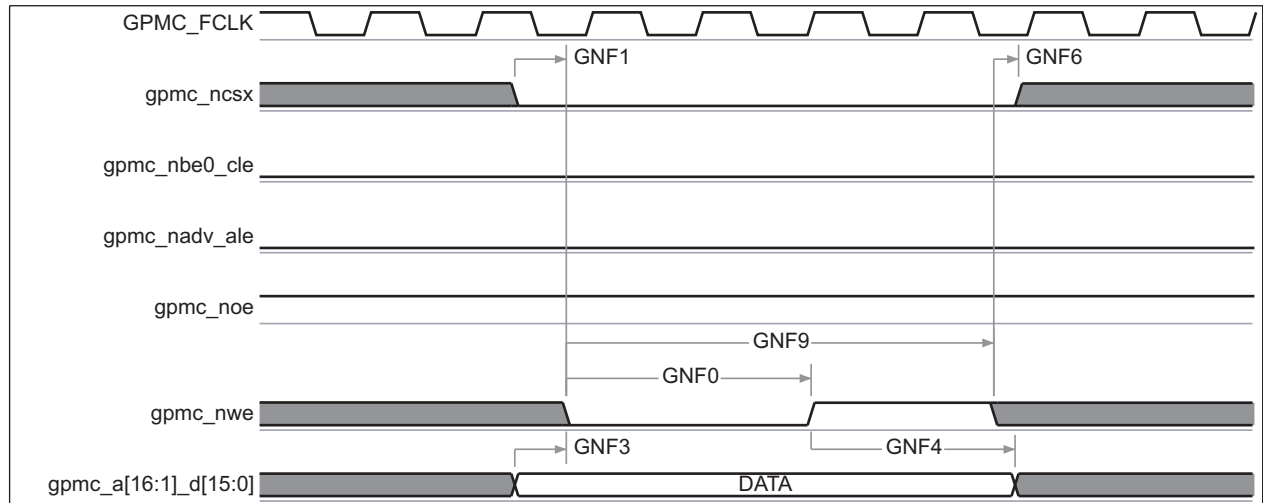
**Figure 6-14. GPMC/NAND Flash – Address Latch Cycle Timing**



030-034

**Figure 6-15. GPMC/NAND Flash – Data Read Cycle Timing(1) (2) (3)**

- (1) The GNF12 parameter provides amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data is internally sampled by active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
- (2) GPMC\_FCLK is an internal clock (GPMC functional clock) not provided externally.
- (3) In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0, 1, 2, or 3.



030-035

In gpmc\_ncsx, x is equal to 0, 1, 2, 3, 4, 5, 6, or 7. In gpmc\_waitx, x is equal to 0 or 1.

**Figure 6-16. GPMC/NAND Flash – Data Write Cycle Timing**

### 6.4.2 SDRAM Controller (SDRC)

The SDRC is a dedicated interface to DDR2/LPDDR1 SDRAM that performs the following functions:

- Buffering of input image data from sensors or video sources
- Intermediate buffering for processing/resizing of image data in the VPFE
- Numerous OSD display buffers
- Intermediate buffering for large raw Bayer data image files while performing image processing functions
- Buffering for intermediate data while performing video encode and decode functions
- Storage of executable code for the ARM

The main features of the controller are:

- Open Core Protocol 2.2 (OCP) compliant [7].
- Supports JEDEC standard compliant DDR2 [2] and LPDDR1 [4] devices.
  - SDRAM address range over 2 chip selects.
  - Supports following data bus widths:

| OCP Data Bus Width | SDRAM Data Bus Width |
|--------------------|----------------------|
| 64 and 128-Bit     | 16, 32, and 64-Bit   |

- Supports following CAS latencies:

| SDRAM Type | CAS Latencies     |
|------------|-------------------|
| DDR2       | 2, 3, 4, 5, and 6 |
| LPDDR1     | 2 and 3           |

- Supports following number of internal banks:

| SDRAM Type | Internal Banks |
|------------|----------------|
| DDR2       | 1, 2, 4, and 8 |
| LPDDR1     | 1, 2, and 4    |

- Supports 256, 512, 1024, and 2048-word page sizes.

- Supports following burst lengths:

| SDRAM Type | Burst Length              |
|------------|---------------------------|
| DDR2       | 8 (4 not supported)       |
| LPDDR1     | 8 (2 and 4 not supported) |

- Supports sequential burst type.
- SDRAM auto initialization from reset or configuration change.
- Supports Bank Interleaving across both the chip selects.
- Supports Clock Stop mode for LPDDR1 for low power.
- Supports Self Refresh and Precharge Power-Down modes for low power.
- Supports Partial Array Self Refresh and Temperature Controlled Self Refresh modes for low power in LPDDR1.
- Temperature Controlled Self Refresh is only supported for mobile SDRAM having on-chip temperature sensor.
- Supports ODT on DDR2.
- Supports prioritized refresh.
- Programmable SDRAM refresh rate and backlog counter.
- Programmable SDRAM timing parameters.
- Supports only little endian.

### 6.4.2.1 LPDDR Interface

This section provides the timing specification for the LPDDR interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable LPDDR memory system without the need for a complex timing closure process. For more information regarding guidelines for using this LPDDR specification, see the *Understanding TI's PCB Routing Rule-Based DDR Timing Specification* Application Report ([SPRAAV0](#)).

#### 6.4.2.1.1 LPDDR Interface Schematic

Figure 6-17 and Figure 6-18 show the LPDDR interface schematics for a LPDDR memory system. The 1 x16 LPDDR system schematic is identical to Figure 6-17 except that the high word LPDDR device is deleted.

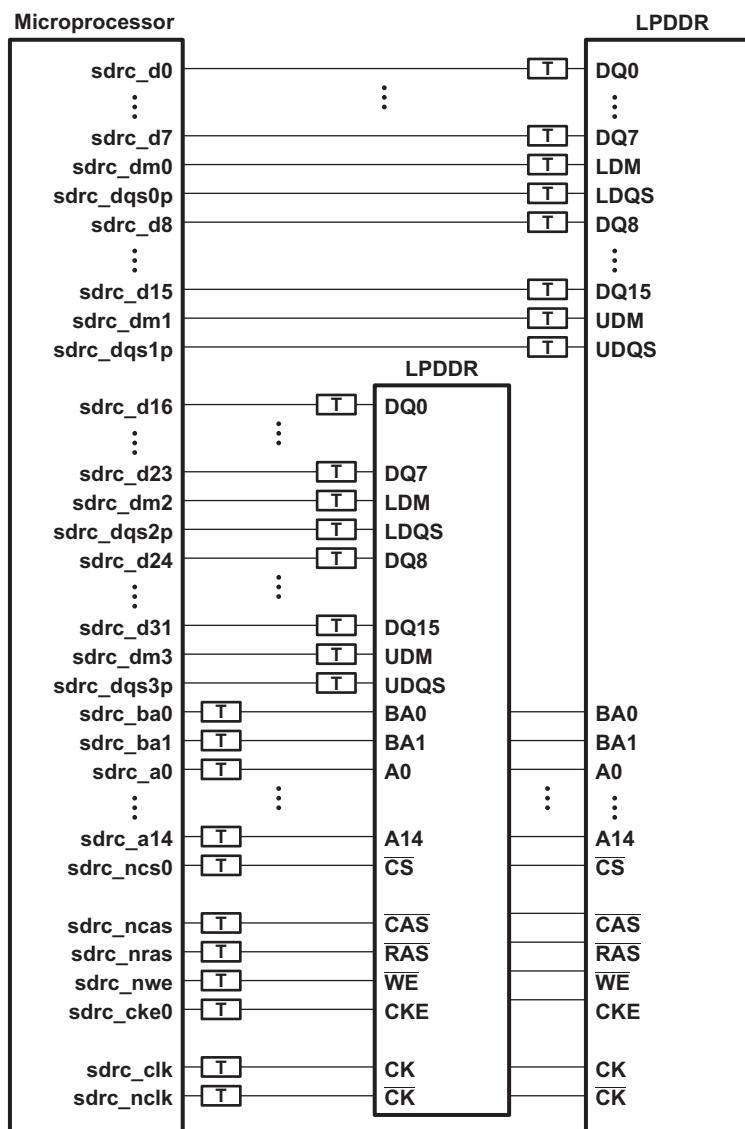


Figure 6-17. AM3517/05 LPDDR High Level Schematic (x16 memories)

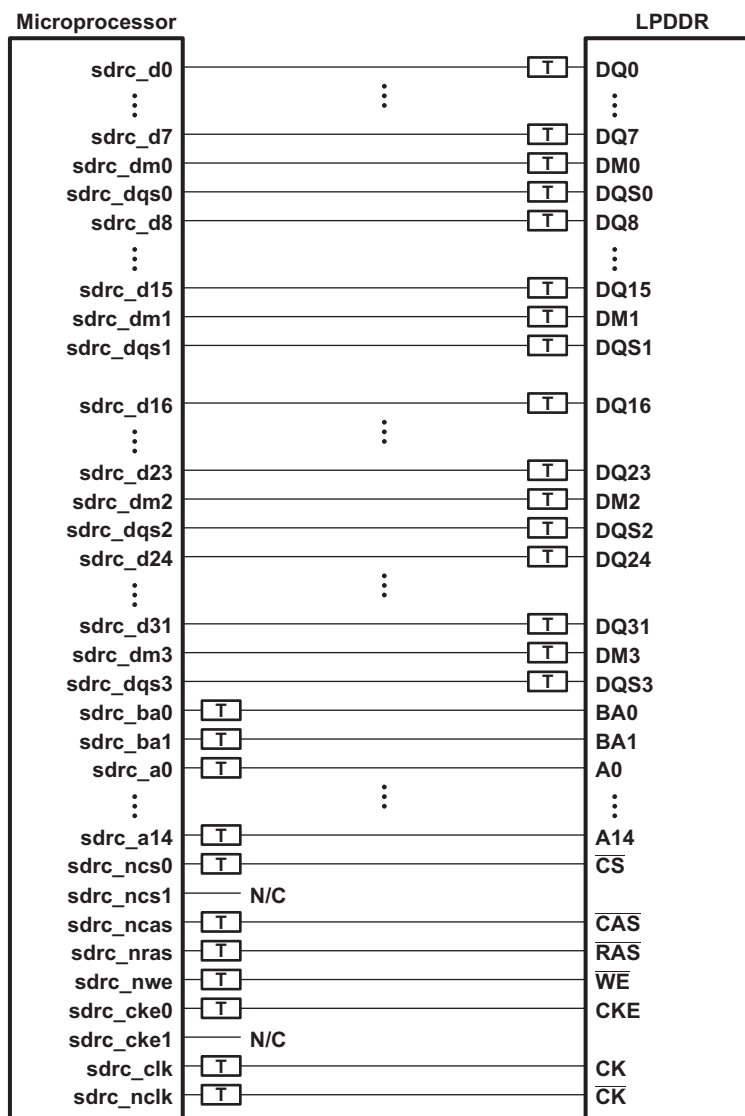


Figure 6-18. AM3517/05 LPDDR High Level Schematic (x32 memory)

#### 6.4.2.1.2 Compatible JEDEC LPDDR Devices

Table 6-13 lists the parameters of the JEDEC LPDDR devices that are compatible with this interface. Generally, the LPDDR interface is compatible with x16 and x32 LPDDR333 speed grade LPDDR devices.

Table 6-13. Compatible JEDEC LPDDR Devices

| NO. | PARAMETER                      | MIN      | MAX | UNIT    | NOTES                   |
|-----|--------------------------------|----------|-----|---------|-------------------------|
| 1   | JEDEC LPDDR Device Speed Grade | LPDDR333 |     |         | See Note <sup>(1)</sup> |
| 2   | JEDEC LPDDR Device Bit Width   | 16       | 32  | Bits    |                         |
| 3   | JEDEC LPDDR Device Count       | 1        | 2   | Devices | See Note <sup>(2)</sup> |
| 4   | JEDEC LPDDR Device Ball Count  | 60       | 90  | Balls   |                         |

(1) Higher LPDDR speed grades operating at the specified speeds are supported due to inherent JEDEC LPDDR backwards compatibility.

(2) 1 x16 LPDDR device is used for 16 bit LPDDR memory system. 1x32 or 2x16 LPDDR devices are used for a 32-bit LPDDR memory system.

#### 6.4.2.1.3 PCB Stackup

The minimum stackup required for routing the microprocessor is a six layer stack as listed in [Table 6-14](#). Additional layers may be added to the PCB stack up to accommodate other circuitry or to reduce the size of the PCB footprint.

**Table 6-14. Minimum PCB Stack Up**

| LAYER | TYPE   | DESCRIPTION                    |
|-------|--------|--------------------------------|
| 1     | Signal | Top Routing Mostly Horizontal  |
| 2     | Plane  | Ground                         |
| 3     | Plane  | Power                          |
| 4     | Signal | Internal Routing               |
| 5     | Plane  | Ground                         |
| 6     | Signal | Bottom Routing Mostly Vertical |

**Table 6-15. PCB Stack Up Specifications**

| NO. | PARAMETER                                                                 | MIN | TYP | MAX   | UNIT | NOTES                   |
|-----|---------------------------------------------------------------------------|-----|-----|-------|------|-------------------------|
| 1   | PCB Routing/Plane Layers                                                  | 6   |     |       |      |                         |
| 2   | Signal Routing Layers                                                     | 3   |     |       |      |                         |
| 3   | Full ground layers under LPDDR routing region                             | 2   |     |       |      |                         |
| 4   | Number of ground plane cuts allowed within LPDDR routing region           |     |     | 0     |      |                         |
| 5   | Number of ground reference planes required for each LPDDR routing 1 layer | 1   |     |       |      |                         |
| 6   | Number of layers between LPDDR routing layer and reference ground 0 plane |     |     | 0     |      |                         |
| 7   | PCB Routing Feature Size                                                  |     | 4   |       | Mils |                         |
| 8   | PCB Trace Width w                                                         |     | 4   |       | Mils |                         |
| 9   | PCB BGA escape via pad size                                               |     | 18  |       | Mils |                         |
| 10  | PCB BGA escape via hole size                                              |     | 8   |       | Mils |                         |
| 11  | Device BGA Pad Size                                                       |     |     |       |      | See Note <sup>(1)</sup> |
| 12  | LPDDR Device BGA Pad Size                                                 |     |     |       |      | See Note <sup>(2)</sup> |
| 13  | Single Ended Impedance, ZO                                                | 50  |     | 75    | Ω    |                         |
| 14  | Impedance Control                                                         | Z-5 | Z   | Z + 5 | Ω    | See Note <sup>(3)</sup> |

(1) Please see the *Flip Chip Ball Grid Array Package* Reference Guide ([SPRU811](#)) for device BGA pad size.

(2) Please see the LPDDR device manufacturer documentation for the LPDDR device BGA pad size.

(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.

#### 6.4.2.1.4 Placement

[Figure 6-19](#) shows the required placement for the microprocessor as well as the LPDDR devices. The dimensions for [Figure 6-19](#) are defined in [Table 6-16](#). The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For 1x16 and 1x32 LPDDR memory systems, the second LPDDR device is omitted from the placement.

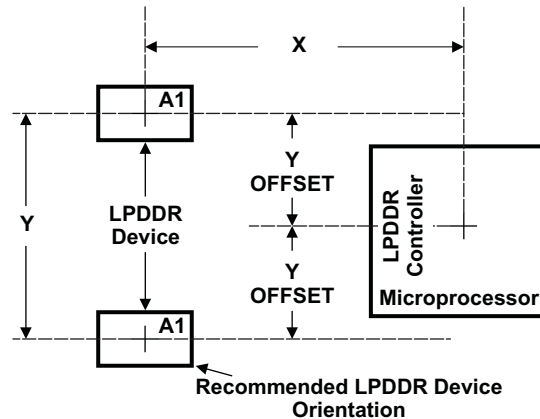


Figure 6-19. AM3517/05 and LPDDR Device Placement

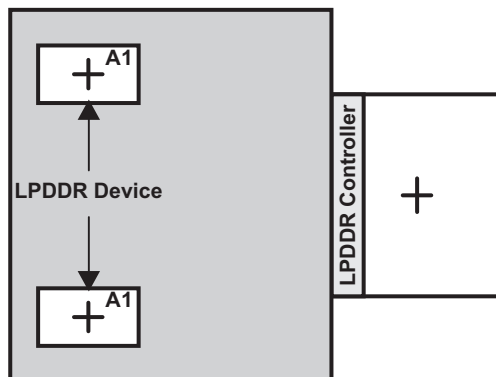
Table 6-16. Placement Specifications

| NO. | PARAMETER                                               | MIN | MAX  | UNIT | NOTES                                                      |
|-----|---------------------------------------------------------|-----|------|------|------------------------------------------------------------|
| 1   | X                                                       |     | 1440 | Mils | See Notes <sup>(1)</sup> , <sup>(2)</sup>                  |
| 2   | Y                                                       |     | 1030 | Mils | See Notes <sup>(1)</sup> , <sup>(2)</sup>                  |
| 3   | Y Offset                                                |     | 525  | Mils | See Notes <sup>(1)</sup> , <sup>(2)</sup> , <sup>(3)</sup> |
| 4   | LPDDR Keepout Region                                    |     |      |      | See Note <sup>(4)</sup>                                    |
| 5   | Clearance from non-LPDDR signal to LPDDR Keepout Region | 4   |      | w    | See Note <sup>(5)</sup>                                    |

- (1) See Figure 6-19 for dimension definitions.  
 (2) Measurements from center of device to center of LPDDR device.  
 (3) For 16 bit memory systems it is recommended that Y Offset be as small as possible.  
 (4) LPDDR keepout region to encompass entire LPDDR routing area.  
 (5) Non-LPDDR signals allowed within LPDDR keepout region provided they are separated from LPDDR routing layers by a ground plane.

#### 6.4.2.1.5 LPDDR Keep Out Region

The region of the PCB used for the LPDDR circuitry must be isolated from other signals. The LPDDR keep out region is defined for this purpose and is shown in Figure 6-20. The size of this region varies with the placement and LPDDR routing. Additional clearances required for the keep out region are listed in Table 6-16.



Region should encompass all LPDDR circuitry and varies depending on placement. Non-LPDDR signals should not be routed on the LPDDR signal layers within the LPDDR keep out region. Non-LPDDR signals may be routed in the region provided they are routed on layers separated from LPDDR signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8 V power plane should cover the entire keep out region.

Figure 6-20. LPDDR Keepout Region

#### 6.4.2.1.6 Net Classes

Table 6-17 lists the clock net classes for the LPDDR interface. Table 6-18 lists the signal net classes, and associated clock net classes, for the signals in the LPDDR interface. These net classes are used for the termination and routing rules that follow.

Table 6-17. Clock Net Class Definitions

| CLOCK NET CLASS | PIN NAMES          |
|-----------------|--------------------|
| CK              | sdrc_clk/sdrc_nclk |
| DQS0            | sdrc_dqs0          |
| DQS1            | sdrc_dqs1          |
| DQS2            | sdrc_dqs2          |
| DQS3            | sdrc_dqs3          |

Table 6-18. Signal Net Class Definitions

| CLOCK NET CLASS | ASSOCIATED CLOCK NET CLASS | PIN NAMES                                                             |
|-----------------|----------------------------|-----------------------------------------------------------------------|
| ADDR_CTRL       | CK                         | sdrc_ba, sdrc_a, sdrc_ncs0, sdrc_ncas, sdrc_nras, sdrc_nwe, sdrc_cke0 |
| DQ0             | DQS0                       | sdrc_d, sdrc_dm0                                                      |
| DQ1             | DQS1                       | sdrc_d, sdrc_dm1                                                      |
| DQ2             | DQS2                       | sdrc_d, sdrc_dm2                                                      |
| DQ3             | DQS3                       | sdrc_d, sdrc_dm3                                                      |

#### 6.4.2.1.7 LPDDR Signal Termination

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. Table 6-19 lists the specifications for the series terminators.

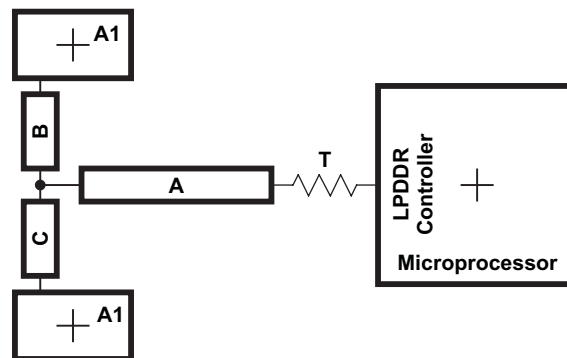
**Table 6-19. LPDDR Signal Terminations**

| NO. | PARAMETER                                     | MIN | TYP | MAX | UNIT     | NOTES                                                      |
|-----|-----------------------------------------------|-----|-----|-----|----------|------------------------------------------------------------|
| 1   | CK Net Class                                  | 0   |     | 10  | $\Omega$ | See Note <sup>(1)</sup>                                    |
| 2   | ADDR_CTRL Net Class                           | 0   | 22  | Zo  | $\Omega$ | See Notes <sup>(1)</sup> , <sup>(2)</sup> , <sup>(3)</sup> |
| 3   | Data Byte Net Classes<br>(DQS0-DQS3, DQ0-DQ3) | 0   | 22  | Zo  | $\Omega$ | See Notes <sup>(1)</sup> , <sup>(2)</sup> , <sup>(3)</sup> |

- (1) Only series termination is permitted, parallel or SST specifically disallowed.  
(2) Terminator values larger than typical only recommended to address EMI issues.  
(3) Termination value should be uniform across net class.

**6.4.2.1.8 LPDDR CK and ADDR\_CTRL Routing**

Figure 6-21 shows the topology of the routing for the CK and ADDR\_CTRL net classes. The route is a balanced T as it is intended that the length of segments B and C be equal. In addition, the length of A should be maximized.

**Figure 6-21. CK and ADDR\_CTRL Routing and Topology****Table 6-20. CK and ADDR\_CTRL Routing Specification**

| NO. | PARAMETER                                                      | MIN      | TYP   | MAX      | UNIT | NOTES                   |
|-----|----------------------------------------------------------------|----------|-------|----------|------|-------------------------|
| 1   | Center to Center CK-CK spacing                                 |          |       | 2w       |      |                         |
| 2   | CK A to B/A to C Skew Length Mismatch                          |          |       | 25       | Mils | See Note <sup>(1)</sup> |
| 3   | CK B to C Skew Length Mismatch                                 |          |       | 25       | Mils |                         |
| 4   | Center to Center CK to other LPDDR trace spacing               | 4w       |       |          |      | See Note <sup>(2)</sup> |
| 5   | CK/ADDR_CTRL nominal trace length                              | CACLM-50 | CACLM | CACLM+50 | Mils | See Note <sup>(3)</sup> |
| 6   | ADDR_CTRL to CK Skew Length Mismatch                           |          |       | 100      | Mils |                         |
| 7   | ADDR_CTRL to ADDR_CTRL Skew Length Mismatch                    |          |       | 100      | Mils |                         |
| 8   | Center to Center ADDR_CTRL to other LPDDR trace 4w spacing     | 4w       |       |          |      | See Note <sup>(2)</sup> |
| 9   | Center to Center ADDR_CTRL to other ADDR_CTRL 3w trace spacing | 3w       |       |          |      | See Note <sup>(2)</sup> |
| 10  | ADDR_CTRL A to B/A to C Skew Length Mismatch                   |          |       | 100      | Mils | See Note <sup>(1)</sup> |
| 11  | ADDR_CTRL B to C Skew Length Mismatch                          |          |       | 100      | Mils |                         |

- (1) Series terminator, if used, should be located closest to device.  
(2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.  
(3) CACLM is the longest Manhattan distance of the CK and ADDR\_CTRL net classes.

Figure 6-22 shows the topology and routing for the DQS and DQ net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

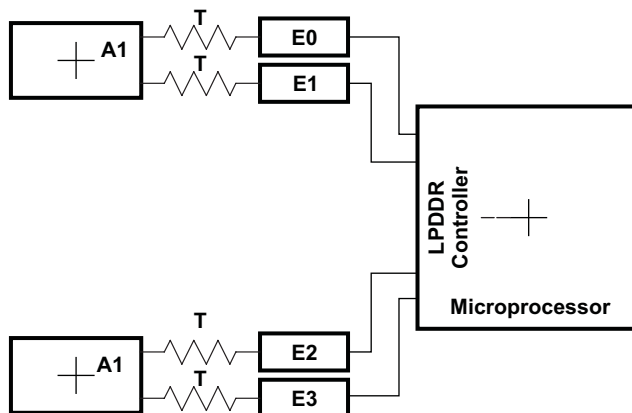


**Figure 6-22. DQS and DQ Routing and Topology**

**Table 6-21. DQS and DQ Routing Specification<sup>(1)</sup>**

| NO. | PARAMETER                                         | MIN       | TYP  | MAX       | UNIT | NOTES                        |
|-----|---------------------------------------------------|-----------|------|-----------|------|------------------------------|
| 2   | DQS E Skew Length Mismatch                        |           |      | 25        | Mils |                              |
| 3   | Center to Center DQS to other LPDDR trace spacing | 4w        |      |           |      | See Note <sup>(2)</sup>      |
| 4   | DQS/DQ nominal trace length                       | DQLM - 50 | DQLM | DQLM + 50 | Mils | See Note <sup>(3)</sup>      |
| 5   | DQ to DQS Skew Length Mismatch                    |           |      | 100       | Mils |                              |
| 6   | DQ to DQ Skew Length Mismatch                     |           |      | 100       | Mils |                              |
| 7   | Center to Center DQ to other LPDDR trace spacing  | 4w        |      |           |      | See Note <sup>(2)</sup>      |
| 8   | Center to Center DQ to other DQ trace spacing     | 3w        |      |           |      | See Note <sup>(2), (4)</sup> |
| 9   | DQ E Skew Length Mismatch                         |           |      | 100       | Mils |                              |

- (1) Series terminator, if used, should be located closest to LPDDR.
- (2) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
- (3) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.
- (4) DQLM is the longest Manhattan distance of the DQS and DQ net classes.

### 6.4.2.2 DDR2 Interface

This section provides the timing specification for the DDR2 interface as a PCB design and manufacturing specification. The design rules constrain PCB trace length, PCB trace skew, signal integrity, cross-talk, and signal timing. These rules, when followed, result in a reliable DDR2 memory system without the need for a complex timing closure process. For more information regarding guidelines for using this DDR2 specification, *Understanding TI's PCB Routing Rule-Based DDR2 Timing Specification* ([SPRAAV0](#)).

#### 6.4.2.2.1 DDR2 Interface Schematic

[Figure 6-23](#) shows the DDR2 interface schematic for a dual-memory DDR2 system. The single-memory system is shown in [Figure 6-24](#). Pin numbers for the AM3517/05 can be obtained from the pin description section.

#### 6.4.2.2.2 Compatible JEDEC DDR2 Devices

[Table 6-22](#) lists the parameters of the JEDEC DDR2 devices that are compatible with this interface. Generally, the DDR2 interface is compatible with x16 or x32 DDR2 speed grade DDR2-333 devices.

**Table 6-22. Compatible JEDEC DDR2 Devices**

| No. | Parameter                     | Min          | Max | Unit    | Notes                   |
|-----|-------------------------------|--------------|-----|---------|-------------------------|
| 1   | JEDEC DDR2 Device Speed Grade | DDR2-333 MHz |     |         | See Note <sup>(1)</sup> |
| 2   | JEDEC DDR2 Device Bit Width   | x16          | x32 | Bits    |                         |
| 3   | JEDEC DDR2 Device Count       | 1            | 2   | Devices | See Note <sup>(2)</sup> |
| 4   | JEDEC DDR2 Device Ball Count  | 84           | 92  | Balls   | See Note <sup>(3)</sup> |

- (1) Higher DDR2 speed grades operating at the specified speeds are supported due to inherent JEDEC DDR2 backwards compatibility.  
 (2) Device count indicates number of dies. If a package contains 2 dies, that is the maximum number of devices that can be connected.  
 (3) 92 ball devices retained for legacy support. New designs should use 84 ball DDR2 devices. Electrically, the 92 and 84 ball DDR2 devices are the same.

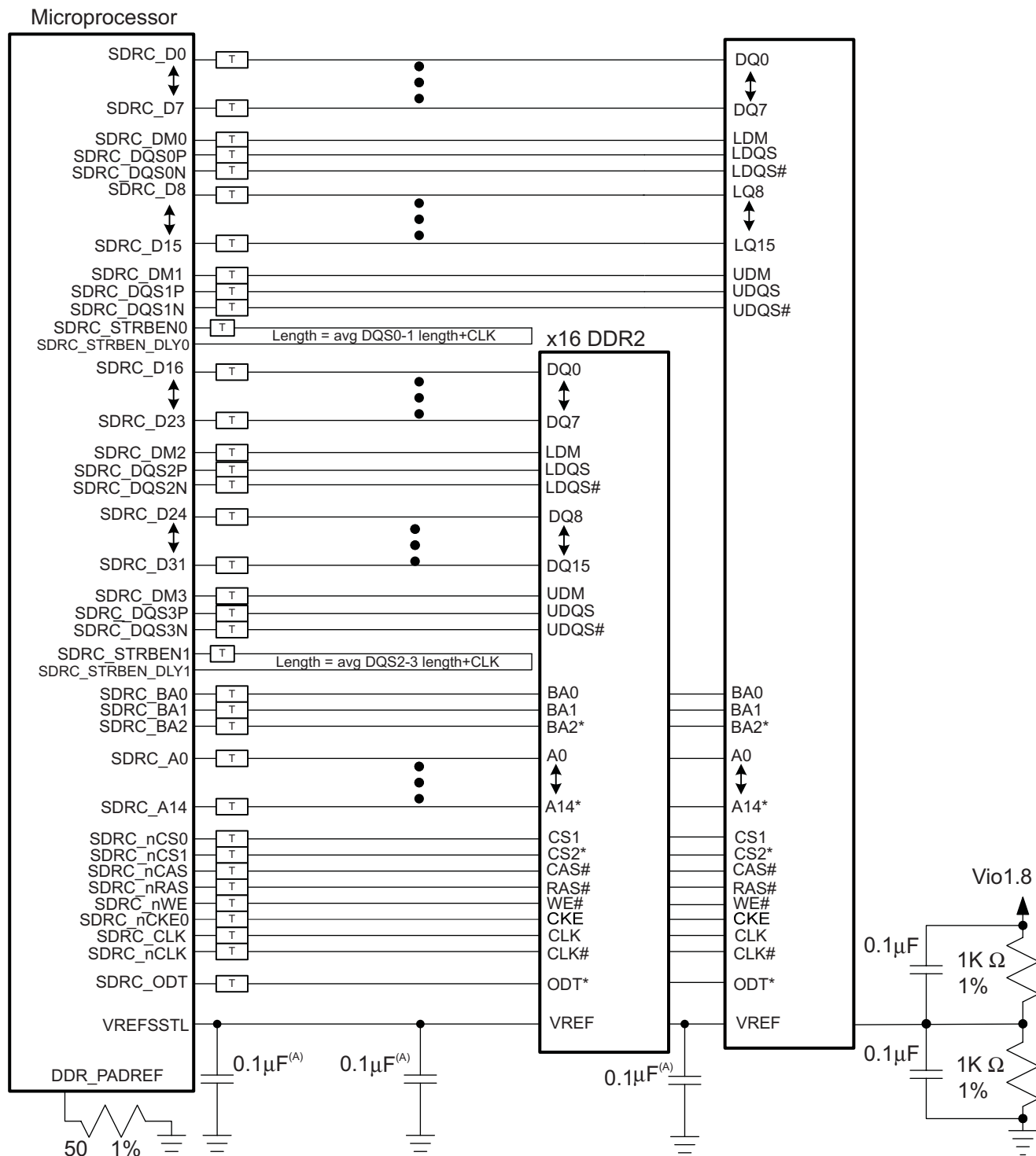
#### 6.4.2.2.3 PCB Stackup

The minimum stackup required for routing the AM3517/05 is a six-layer stack as listed in [Table 6-23](#). Additional layers may be added to the PCB stack up to accommodate other circuitry or to reduce the size of the PCB footprint.

**Table 6-23. Minimum PCB Stack Up**

| Layer | Type   | Description                    |
|-------|--------|--------------------------------|
| 1     | Signal | Top Routing Mostly Horizontal  |
| 2     | Plane  | Ground                         |
| 3     | Plane  | Power                          |
| 4     | Signal | Internal Routing               |
| 5     | Plane  | Ground                         |
| 6     | Signal | Bottom Routing Mostly Vertical |

Complete stack up specifications are provided in [Table 6-24](#).

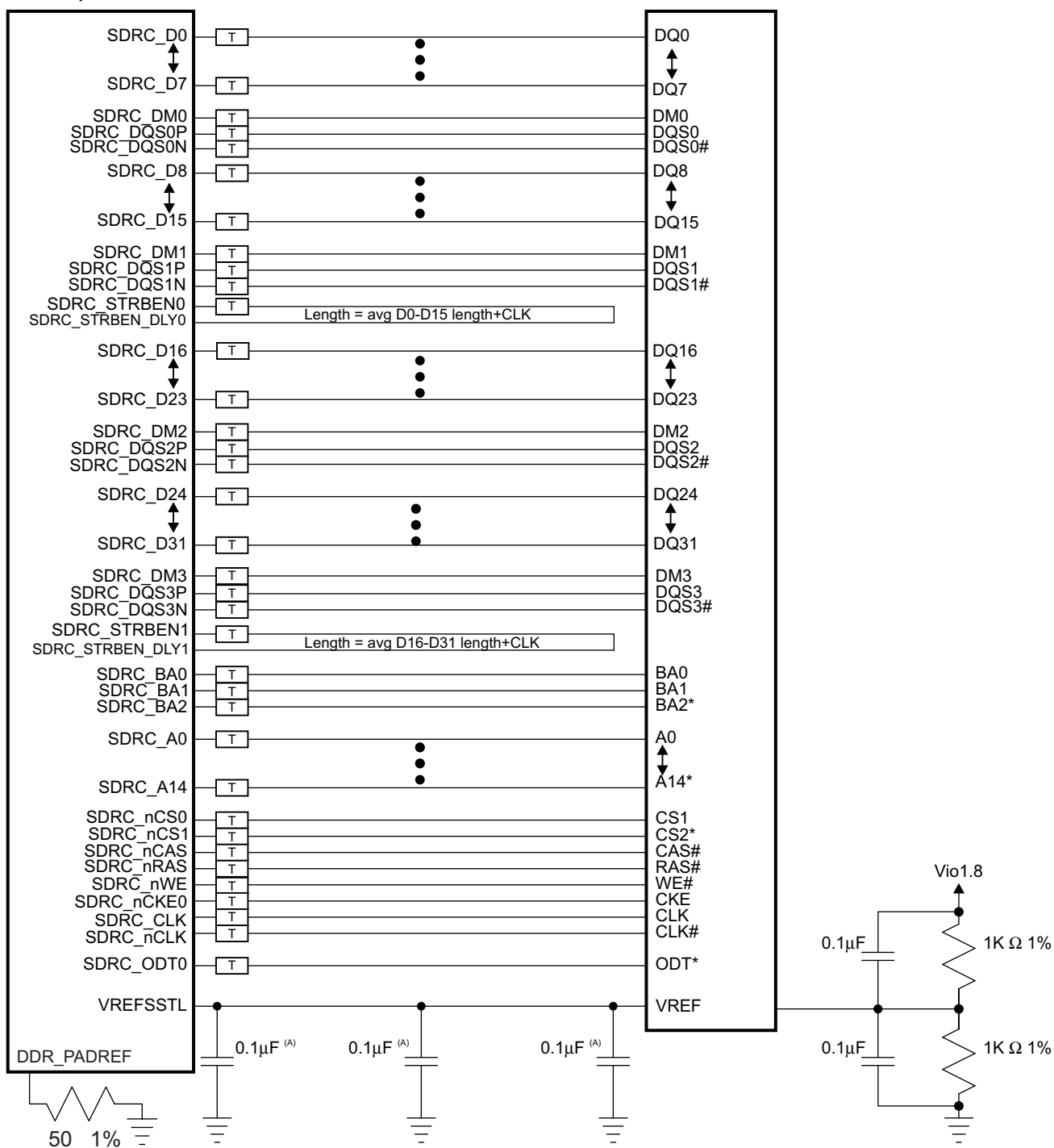


A. See VREF Routing and Topology figure for information on capacitor placement.

**Figure 6-23. DDR2 Dual-Memory High Level Schematic**

## Microprocessor

## DDR2



A. See VREF Routing and Topology figure for information on capacitor placement.

**Figure 6-24. DDR2 Single-Memory High Level Schematic**

**Table 6-24. PCB Stack Up Specifications**

| No. | Parameter                                                              | Min | Typ | Max | Unit | Notes                   |
|-----|------------------------------------------------------------------------|-----|-----|-----|------|-------------------------|
| 1   | PCB Routing/Plane Layers                                               | 6   |     |     |      |                         |
| 2   | Signal Routing Layers                                                  | 3   |     |     |      |                         |
| 3   | Full ground layers under DDR2 routing Region                           | 2   |     |     |      |                         |
| 4   | Number of ground plane cuts allowed within DDR routing region          |     |     | 0   |      |                         |
| 5   | Number of ground reference planes required for each DDR2 routing layer | 1   |     |     |      |                         |
| 6   | Number of layers between DDR2 routing layer and ground plane           |     |     | 0   |      |                         |
| 7   | PCB Routing Feature Size                                               |     | 4   |     | Mils |                         |
| 8   | PCB Trace Width w                                                      |     | 4   |     | Mils |                         |
| 9   | PCB BGA escape via pad size                                            |     | 20  |     | Mils |                         |
| 10  | PCB BGA escape via hole size                                           |     | 10  |     | Mils |                         |
| 11  | AM3517/05 BGA pad size                                                 |     | 12  |     |      | See Note <sup>(1)</sup> |
| 12  | DDR2 Device BGA pad size                                               |     |     |     |      | See Note <sup>(2)</sup> |
| 13  | Single Ended Impedance, Z <sub>0</sub>                                 | 50  |     | 75  | Ω    |                         |
| 14  | Impedance Control                                                      | Z-5 | Z   | Z+5 | Ω    | See Note <sup>(3)</sup> |

(1) The recommended pad size is 0.3 mm per IPC-7351 specification.

(2) Please refer to IPC standard IPC-7351 or manufacturer's recommendations for correct BGA pad size.

(3) Z is the nominal singled ended impedance selected for the PCB specified by item 12.

#### 6.4.2.2.4 Placement

Figure 6-24 shows the required placement for the DDR2 devices. The dimensions for Figure 6-25 are defined in Table 6-25. The placement does not restrict the side of the PCB that the devices are mounted on. The ultimate purpose of the placement is to limit the maximum trace lengths and allow for proper routing space. For single-memory DDR2 systems, the second DDR2 device is omitted from the placement.

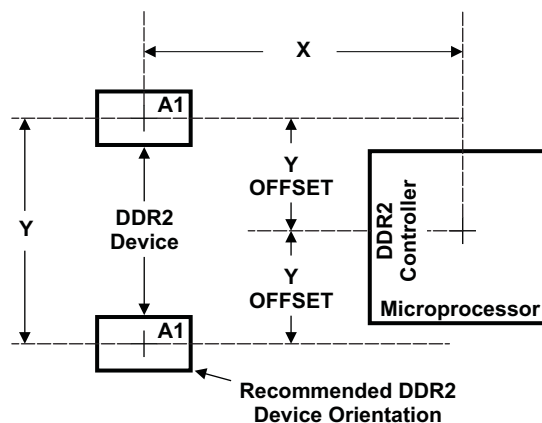
**Figure 6-25. DDR2 Device Placement**

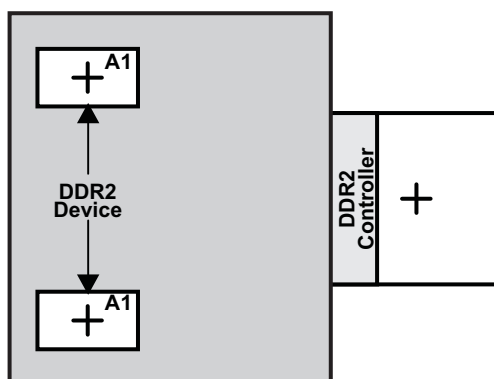
**Table 6-25. Placement Specifications**

| No. | Parameter                                             | Min | Max  | Unit | Notes                                                      |
|-----|-------------------------------------------------------|-----|------|------|------------------------------------------------------------|
| 1   | X                                                     |     | 1750 | Mils | See Notes <sup>(1)</sup> , <sup>(2)</sup>                  |
| 2   | Y                                                     |     | 1280 | Mils | See Notes <sup>(1)</sup> , <sup>(2)</sup>                  |
| 3   | Y Offset                                              |     | 650  | Mils | See Notes <sup>(1)</sup> , <sup>(2)</sup> , <sup>(3)</sup> |
| 4   | DDR2 Keepout Region                                   |     |      |      | See Note <sup>(4)</sup>                                    |
| 5   | Clearance from non-DDR2 signal to DDR2 Keepout Region | 4   |      | w    | See Note <sup>(5)</sup>                                    |

- (1) See [Figure 6-23](#) for dimension definitions.  
(2) Measurements from center of AM3517/05 device to center of DDR2 device.  
(3) For single memory systems it is recommended that Y Offset be as small as possible.  
(4) DDR2 Keepout region to encompass entire DDR2 routing area  
(5) Non-DDR2 signals allowed within DDR2 keepout region provided they are separated from DDR2 routing layers by a ground plane.

#### 6.4.2.2.5 DDR2 Keep Out Region

The region of the PCB used for the DDR2 circuitry must be isolated from other signals. The DDR2 keep out region is defined for this purpose and is shown in [Figure 6-26](#). The size of this region varies with the placement and DDR routing. Additional clearances required for the keep out region are listed in [Table 6-25](#).



Region should encompass all DDR2 circuitry and varies depending on placement. Non-DDR2 signals should not be routed on the DDR signal layers within the DDR2 keep out region. Non-DDR2 signals may be routed in the region provided they are routed on layers separated from DDR2 signal layers by a ground layer. No breaks should be allowed in the reference ground layers in this region. In addition, the 1.8 V power plane should cover the entire keep out region.

**Figure 6-26. DDR2 Keepout Region**

#### 6.4.2.2.6 Bulk Bypass Capacitors

Bulk bypass capacitors are required for moderate speed bypassing of the DDR2 and other circuitry. [Table 6-26](#) contains the minimum numbers and capacitance required for the bulk bypass capacitors. Note that this table only covers the bypass needs of the AM3517/05 and DDR2 interfaces. Additional bulk bypass capacitance may be needed for other circuitry.

**Table 6-26. Bulk Bypass Capacitors**

| No. | Parameter                          | Min | Max | Unit    | Notes                   |
|-----|------------------------------------|-----|-----|---------|-------------------------|
| 1   | VDDS Bulk Bypass Capacitor Count   | 3   |     | Devices | See Note <sup>(1)</sup> |
| 2   | VDDS Bulk Bypass Total Capacitance | 30  |     | uF      |                         |

- (1) These devices should be placed near the device they are bypassing, but preference should be given to the placement of the high-speed (HS) bypass caps.

**Table 6-26. Bulk Bypass Capacitors (continued)**

| No. | Parameter                           | Min | Max | Unit    | Notes              |
|-----|-------------------------------------|-----|-----|---------|--------------------|
| 3   | DDR#1 Bulk Bypass Capacitor Count   | 1   |     | Devices | See Note (1)       |
| 4   | DDR#1 Bulk Bypass Total Capacitance | 22  |     | uF      |                    |
| 5   | DDR#2 Bulk Bypass Capacitor Count   | 1   |     | Devices | See Notes (1), (2) |
| 6   | DDR#2 Bulk Bypass Total Capacitance | 22  |     | uF      | See Note (2)       |

(2) Only used on dual-memory systems

#### 6.4.2.2.7 High-Speed Bypass Capacitors

High-speed (HS) bypass capacitors are critical for proper DDR2 interface operation. It is particularly important to minimize the parasitic series inductance of the HS bypass cap, AM3517/05 DDR2 power, and AM3517/05 DDR2 ground connections. [Table 6-27](#) contains the specification for the HS bypass capacitors as well as for the power connections on the PCB.

#### 6.4.2.2.8 Net Classes

[Table 6-28](#) lists the clock net classes for the DDR2 interface. [Table 6-29](#) lists the signal net classes, and associated clock net classes, for the signals in the DDR2 interface. These net classes are used for the termination and routing rules that follow.

**Table 6-27. High-Speed Bypass Capacitors**

| No. | Parameter                                                            | Min | Max  | Unit    | Notes                                     |
|-----|----------------------------------------------------------------------|-----|------|---------|-------------------------------------------|
| 1   | HS Bypass Capacitor Package Size                                     |     | 0402 | 10 Mils | See Note <sup>(1)</sup>                   |
| 2   | Distance from HS bypass capacitor to device being bypassed           |     | 250  | Mils    |                                           |
| 3   | Number of connection vias for each HS bypass capacitor               | 2   |      | Vias    | See Note <sup>(2)</sup>                   |
| 4   | Trace length from bypass capacitor contact to connection via         | 1   | 30   | Mils    |                                           |
| 5   | Number of connection vias for each DDR2 device power or ground balls | 1   |      | Vias    |                                           |
| 6   | Trace length from DDR2 device power ball to connection via           |     | 35   | Mils    |                                           |
| 7   | VDDS HS Bypass Capacitor Count                                       | 20  |      | Devices | See Note <sup>(3)</sup>                   |
| 8   | VDDS HS Bypass Capacitor Total Capacitance                           | 1.2 |      | μF      |                                           |
| 9   | DDR#1 HS Bypass Capacitor Count                                      | 8   |      | Devices | See Note <sup>(3)</sup>                   |
| 10  | DDR#1 HS Bypass Capacitor Total Capacitance                          | 0.4 |      | μF      |                                           |
| 11  | DDR#2 HS Bypass Capacitor Count                                      | 8   |      | Devices | See Notes <sup>(3)</sup> , <sup>(4)</sup> |
| 12  | DDR#2 HS Bypass Capacitor Total Capacitance                          | 0.4 |      | μF      | See Note <sup>(4)</sup>                   |

(1) LxW, 10 mil units, i.e., a 0402 is a 40x20 mil surface mount capacitor

(2) An additional HS bypass capacitor can share the connection vias only if it is mounted on the opposite side of the board.

(3) These devices should be placed as close as possible to the device being bypassed.

(4) Only used on dual-memory systems

**Table 6-28. Clock Net Class Definitions**

| Clock Net Class | AM3517/05 Device Pin Names |
|-----------------|----------------------------|
| CK              | sdrc_clk/sdrc_nclk         |
| DQS0            | sdrc_dqs0p /sdrc_dqs0n     |
| DQS1            | sdrc_dqs1p /sdrc_dqs1n     |
| DQS2            | sdrc_dqs2p/sdrc_dqs2n      |
| DQS3            | sdrc_dqs3p/sdrc_dqs3n      |

**Table 6-29. Signal Net Class Definitions**

| Clock Net Class | Associated Clock Net Class | AM3517/05 Device Pin Names                                                                  |
|-----------------|----------------------------|---------------------------------------------------------------------------------------------|
| ADDR_CTRL       | CK                         | sdrc_ba[2:0], sdrc_ncs1, sdrc_a[14:0], sdrc_ncs0, sdrc_ncas, sdrc_nras, sdrc_nwe, sdrc_cke0 |
| DQ0             | DQS0                       | sdrc_d[7:0], sdrc_dm0                                                                       |
| DQ1             | DQS1                       | sdrc_d[15:8], sdrc_dm1                                                                      |
| DQ2             | DQS2                       | sdrc_d[23:16],sdrc_dm2                                                                      |
| DQ3             | DQS3                       | sdrc_d[31:24],sdrc_dm3                                                                      |
| SDRC_STRBEN0    | CK,DQS0,DQS1               | sdrc_strben0, sdrc_strben_dly0                                                              |
| SDRC_STRBEN1    | CK,DQS2,DQS3               | sdrc_strben1, sdrc_strben_dly1                                                              |

**6.4.2.2.9 DDR2 Signal Termination**

No terminations of any kind are required in order to meet signal integrity and overshoot requirements. Serial terminators are permitted, if desired, to reduce EMI risk; however, serial terminations are the only type permitted. [Table 6-30](#) lists the specifications for the series terminators.

**Table 6-30. DDR2 Signal Terminations**

| No. | Parameter                                 | Min | Typ | Max | Unit | Notes                                                      |
|-----|-------------------------------------------|-----|-----|-----|------|------------------------------------------------------------|
| 1   | CLK Net Class                             | 0   |     | 10  | Ω    | See Note <sup>(1)</sup>                                    |
| 2   | ADDR_CTRL Net Class                       | 0   | 22  | Zo  | Ω    | See Notes <sup>(1)</sup> , <sup>(2)</sup> , <sup>(3)</sup> |
| 3   | Data Byte Net Classes (DQS0-DQS1, D0-D31) | 0   | 22  | Zo  | Ω    | See Notes <sup>(1)</sup> , <sup>(2)</sup> , <sup>(3)</sup> |
| 4   | SDRC_STRBENx Net Class (SDRC_STRBENx)     | 0   | 10  | Zo  | Ω    | See Notes <sup>(1)</sup> , <sup>(2)</sup> , <sup>(3)</sup> |

- (1) Only series termination is permitted, parallel or SST specifically disallowed.  
 (2) Terminator values larger than typical only recommended to address EMI issues.  
 (3) Termination value should be uniform across net class.

#### 6.4.2.2.10 VREF Routing

VREF is used as a reference by the input buffers of the DDR2 memories as well as the AM3517/05. VREF is intended to be half of the DDR2 power supply voltage and should be created using a resistive divider as shown in Figure 6-23. Other methods of creating VREF are not recommended. Figure 6-27 shows the layout guidelines for VREF.

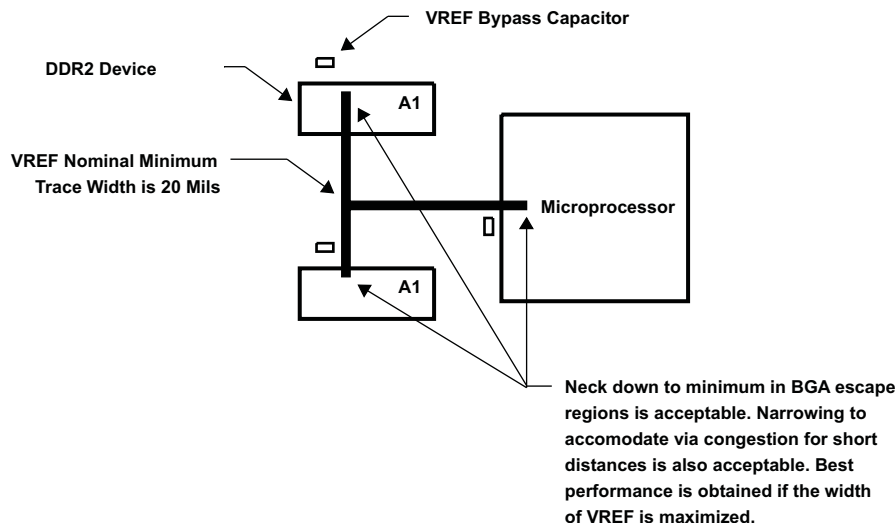


Figure 6-27. VREF Routing and Topology

#### 6.4.2.2.11 DDR2 CLK and ADDR\_CTRL Routing

Figure 6-28 shows the topology of the routing for the CLK and ADDR\_CTRL net classes. The route is a balanced *T* as it is intended that the length of segments B and C be equal. In addition, the length of A should be maximized.

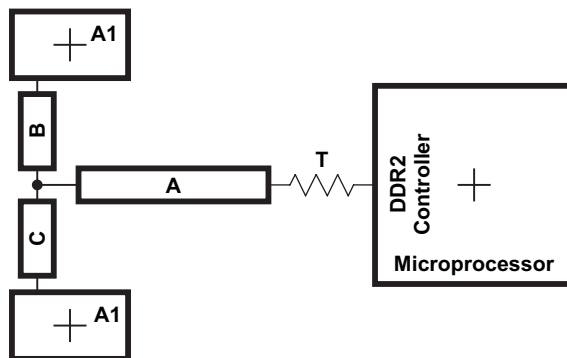


Figure 6-28. CLK and ADDR\_CTRL Routing and Topology

**Table 6-31. CLK and ADDR\_CTRL Routing Specification <sup>(1)</sup>**

| No | Parameter                                                   | Min      | Typ   | Max      | Unit | Notes                   |
|----|-------------------------------------------------------------|----------|-------|----------|------|-------------------------|
| 1  | Center to center DQS-DQSN spacing                           |          |       | 2w       |      |                         |
| 2  | CK differential pair Skew Length Mismatch <sup>(2)</sup>    |          |       | 25       | Mils | See Note <sup>(1)</sup> |
| 3  | CLKB to CLKC Skew Length Mismatch                           |          |       | 25       | Mils |                         |
| 4  | Center to center CLK to other DDR2 trace spacing            | 4w       |       |          |      | See Note <sup>(3)</sup> |
| 5  | CK/ADDR_CTRL nominal trace length                           | CACLM-50 | CACLM | CACLM+50 | Mils | See Note <sup>(4)</sup> |
| 6  | ADDR_CTRL to CLK Skew Length Mismatch                       |          |       | 100      | Mils |                         |
| 7  | ADDR_CTRL to ADDR_CTRL Skew Length Mismatch                 |          |       | 100      | Mils |                         |
| 8  | Center to center ADDR_CTRL to other DDR2 trace spacing      | 4w       |       |          |      | See Note <sup>(3)</sup> |
| 9  | Center to center ADDR_CTRL to other ADDR_CTRL trace spacing | 3w       |       |          |      | See Note <sup>(3)</sup> |
| 10 | ADDR_CTRL A to B, ADDR_CTRL A to C, Skew Length Mismatch    |          |       | 100      | Mils | See Note <sup>(1)</sup> |
| 11 | ADDR_CTRL B to C Skew Length Mismatch                       |          |       | 100      | Mils |                         |

(1) Series terminator, if used, should be located closest to AM3517/05.

(2) Differential impedance should be 100-ohms.

(3) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.

(4) CACLM is the longest Manhattan distance of the CLK and ADDR\_CTRL net classes.

Figure 6-29 shows the topology and routing for the DQS and Dx net classes; the routes are point to point. Skew matching across bytes is not needed nor recommended.

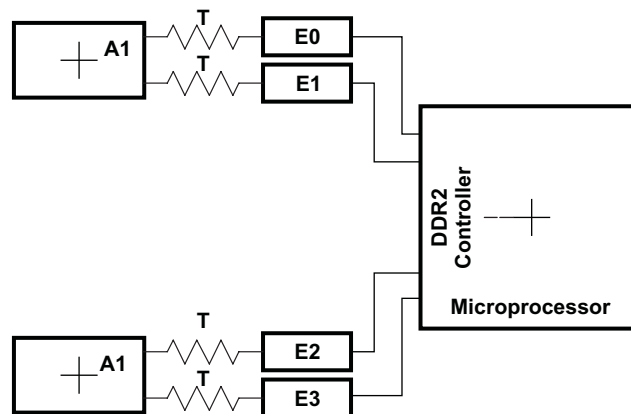
**Figure 6-29. DQS and Dx Routing and Topology**

**Table 6-32. DQS and Dx Routing Specification<sup>(1) (2)</sup>**

| No. | Parameter                                                   | Min     | Typ  | Max     | Unit | Notes                                        |
|-----|-------------------------------------------------------------|---------|------|---------|------|----------------------------------------------|
| 1   | Center to center DQS-DQSN spacing                           |         |      | 2w      |      |                                              |
| 2   | DQS E differential pair Skew Length Mismatch <sup>(3)</sup> |         |      | 25      | Mils |                                              |
| 3   | Center to center DQS to other DDR2 trace spacing            | 4w      |      |         |      | See Note <sup>(4)</sup>                      |
| 4   | DQS/Dx nominal trace length                                 | DQLM-50 | DQLM | DQLM+50 | Mils | See Notes <sup>(2)</sup> ,<br><sup>(5)</sup> |
| 5   | Dx to DQS Skew Length Mismatch                              |         |      | 100     | Mils | See Note <sup>(5)</sup>                      |
| 6   | Dx to Dx Skew Length Mismatch                               |         |      | 100     | Mils | See Note <sup>(5)</sup>                      |
| 7   | Center to center Dx to other DDR2 trace spacing             | 4w      |      |         |      | See Notes <sup>(4)</sup> ,<br><sup>(6)</sup> |
| 8   | Center to Center Dx to other Dx trace spacing               | 3w      |      |         |      | See Notes <sup>(7)</sup> ,<br><sup>(4)</sup> |

(1) "Dx" indicates a data line. E indicates length of DQS differential pair or Dx signal.

(2) Series terminator, if used, should be located closest to DDR.

(3) Differential impedance should be 100-ohms.

(4) Center to center spacing is allowed to fall to minimum (w) for up to 500 mils of routed length to accommodate BGA escape and routing congestion.

(5) There is no need and it is not recommended to skew match across data bytes, i.e., from DQS0 and data byte 0 to DQS1 and data byte 1.

(6) Dx's from other DQS domains are considered *other DDR2 trace*.

(7) DQLM is the longest Manhattan distance of each of the DQS and Dx net classes.

Figure 6-30 shows the routing for the SDRC\_STRBENx net classes. Table 6-33 contains the routing specification. SDRC\_STRBENx net classes should be shielded from or routed on different layers than the DQx net classes.

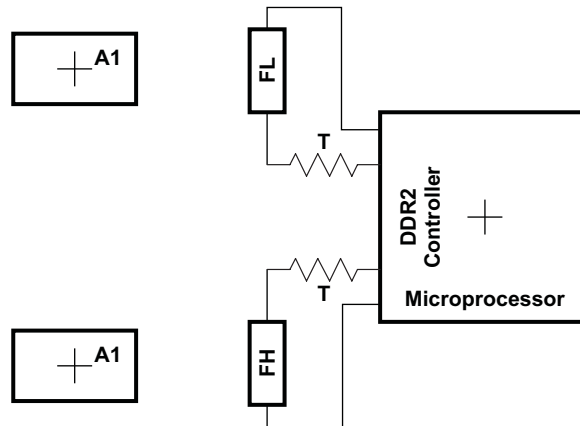


**Figure 6-30. SDRC\_STRBENx Routing**

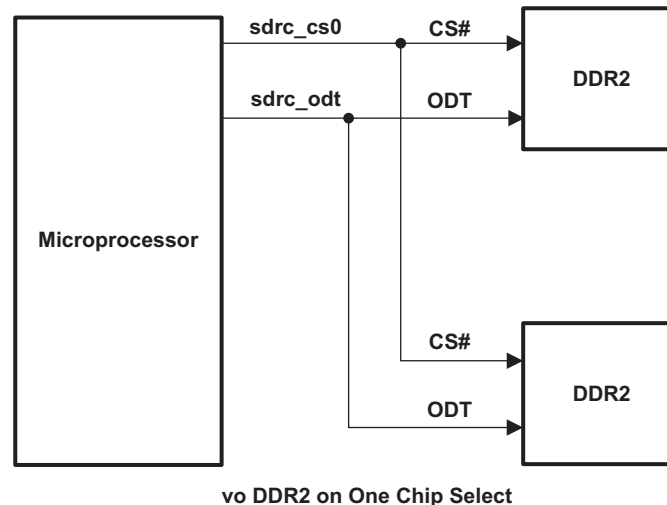
**Table 6-33. SDRC\_STRBENx Routing Specification<sup>(1)(2)</sup>**

| No. | Parameter                                                | Min     | Typ    | Max     | Unit | Notes                   |
|-----|----------------------------------------------------------|---------|--------|---------|------|-------------------------|
| 1   | SDRC_STRBEN0 Length F                                    |         | CKB0B1 |         |      | See Note <sup>(3)</sup> |
|     | SDRC_STRBEN1 Length F                                    |         | CKB0B2 |         |      | See Note <sup>(4)</sup> |
| 3   | Center to center SDRC_STRBENx to any other trace spacing | 4w      |        |         |      |                         |
| 4   | DQS/Dx nominal trace length                              | DQLM-50 | DQLM   | DQLM+50 | Mils |                         |
| 5   | SDRC_STRBENx Skew                                        |         |        | 100     | Mils | See Note <sup>(5)</sup> |

- (1) STRBENx termination resistors should be placed close to AM3517/05 STRBENx signal (not close to STRBEN\_DLYx signal).
- (2) Ensure signal velocities across different layers are taken into account when calculating STRBENx length. For example, if DQS0 and DSQ1 are 1inch each, and DQS0 is on a layer that is 10% faster, use 1.1inch as the length for DQS0.
- (3) CKB0B1 is the sum of the length of the CLK (the portion that goes to the memory associated with DQS0 and DQS1) plus the average length of the DQS0 and DQS1 differential pairs.
- (4) CKB0B2 is the sum of the length of the CLK (the portion that goes to the memory associated with DQS2 and DQS3) plus the average length of the DQS2 and DQS3 differential pairs.
- (5) Skew from CKB0B1 or CKB0B2.

#### 6.4.2.2.12 On Die Termination (ODT)

ODT should only be used with 1 chip select as shown in [Figure 6-31](#). If using sdrc\_cs0 and sdrc\_cs1, sdrc\_odt should not be used. ODT signals should be tied off at the memory.

**Figure 6-31. ODT Connection Using One Chip select (sdrc\_cs0)**

## **6.5 Video Interfaces**

### **6.5.1 Video Processing Subsystem (VPSS)**

The Video Processing Sub-System (VPSS) provides a Video Processing Front End (VPFE) input interface for external imaging peripherals (i.e., image sensors, video decoders, and so forth).

#### **6.5.1.1 Video Processing Front End (VPFE)**

The Video Processing Front-End (VPFE) controller receives input video/image data from external capture devices and stores it to external memory which is transferred into the external memory via a built in DMA engine. An internal buffer block provides a high bandwidth path between the VPSS module and the external memory. The Cortex-A8 will process the image data based on application requirements.

### 6.5.1.1.1 Video Processing Front End (VPFE) Timing

Table 6-34 and Table 6-35 assume testing over recommended operating conditions.

**Table 6-34. VPFE Timing Requirements**

| NO.  | PARAMETER                            |                                                    | 1.8V, 3.3V |     | UNIT |
|------|--------------------------------------|----------------------------------------------------|------------|-----|------|
|      |                                      |                                                    | MIN        | MAX |      |
| VF1  | $t_c(\text{VDIN\_CLK})$              | Cycle time, pixel clock input, VDIN_CLK            | 13.33      | 100 | ns   |
| VF2  | $t_{su}(\text{VDIN\_D-VDIN\_CLK})$   | Setup time, VDIN_D to VDIN_CLK rising edge         | 3.5        |     | ns   |
| VF3  | $t_{su}(\text{VDIN\_HD-VDIN\_CLK})$  | Setup time, VDIN_HD to VDIN_CLK rising edge        | 3.5        |     | ns   |
| VF4  | $t_{su}(\text{VDIN\_VD-VDIN\_CLK})$  | Setup time, VDIN_VD to VDIN_CLK rising edge        | 3.5        |     | ns   |
| VF5  | $t_{su}(\text{VDIN\_WEN-VDIN\_CLK})$ | Setup time, VDIN_WEN to VDIN_CLK rising edge       | 3.5        |     | ns   |
| VF6  | $t_{su}(\text{C\_FLD-VDIN\_CLK})$    | Setup time, VDIN_FIELD to VDIN_CLK rising edge     | 3.5        |     | ns   |
| VF7  | $t_h(\text{VDIN\_CLK-VDIN\_D})$      | Hold time, VDIN_D valid after VDIN_CLK rising edge | 2.5        |     | ns   |
| VF8  | $t_h(\text{VDIN\_HD-VDIN\_CLK})$     | Hold time, VDIN_HD to VDIN_CLK rising edge         | 2.5        |     | ns   |
| VF9  | $t_h(\text{VDIN\_VD-VDIN\_CLK})$     | Hold time, VDIN_VD to VDIN_CLK rising edge         | 2.5        |     | ns   |
| VF10 | $t_h(\text{VDIN\_WEN-VDIN\_CLK})$    | Hold time, VDIN_WEN to VDIN_CLK rising edge        | 2.5        |     | ns   |
| VF11 | $t_h(\text{C\_FLD-VDIN\_CLK})$       | Hold time, VDIN_FIELD to VDIN_CLK rising edge      | 2.5        |     | ns   |

**Table 6-35. VPFE Output Switching Characteristics**

| NO.  | PARAMETER                           |                                                 | 1.8V, 3.3V |     | UNIT |
|------|-------------------------------------|-------------------------------------------------|------------|-----|------|
|      |                                     |                                                 | MIN        | MAX |      |
| VF12 | $t_d(\text{VDIN\_HD-VDIN\_CLK})$    | Output delay time, VDIN_HD to CLK rising edge   |            | 10  | ns   |
| VF13 | $t_d(\text{VDIN\_VD-VDIN\_CLK})$    | Output delay time, VDIN_VD to CLK rising edge   |            | 10  | ns   |
| VF14 | $t_d(\text{VDIN\_WEN-VDIN\_CLK})$   | Output delay time, VDIN_WEN to CLK rising edge  |            | 10  | ns   |
| VF15 | $t_{oh}(\text{VDIN\_HD-VDIN\_CLK})$ | Output hold time, VDIN_HD to CLK rising edge    | 0.5        |     | ns   |
| VF16 | $t_{oh}(\text{VDIN\_VD-VDIN\_CLK})$ | Output hold time, VDIN_VD to CLK rising edge    | 0.5        |     | ns   |
| VF17 | $t_{oh}(\text{C\_FLD-VDIN\_CLK})$   | Output hold time, VDIN_FIELD to CLK rising edge | 0.5        |     | ns   |

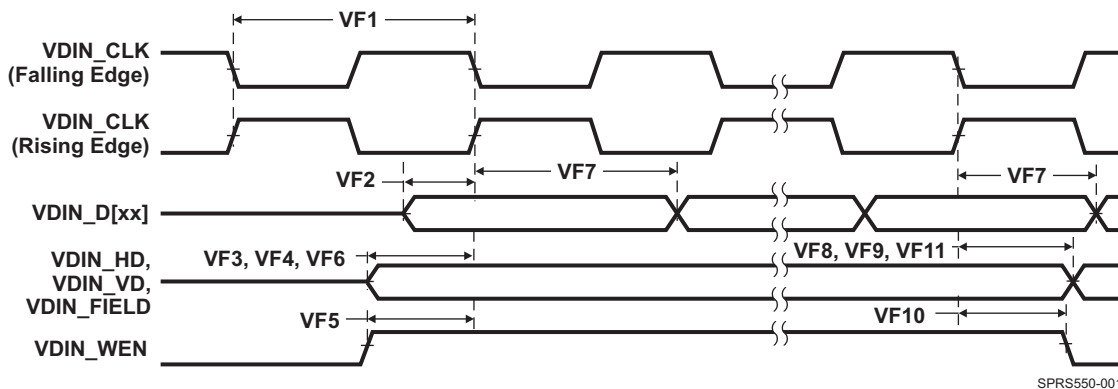


**Figure 6-32. VPFE0 Input Timings**

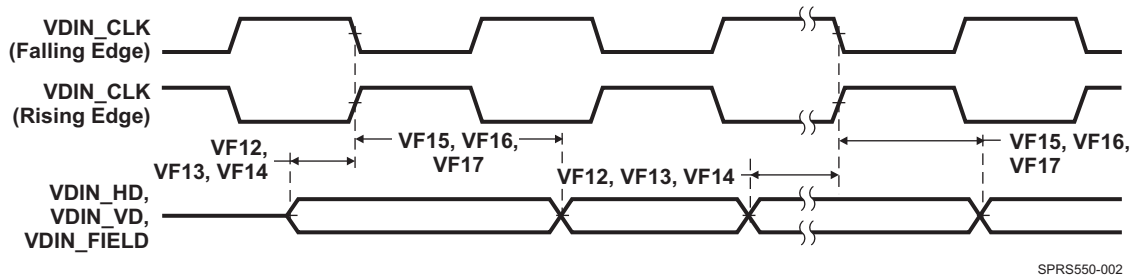


Figure 6-33. VPFE Output Timings

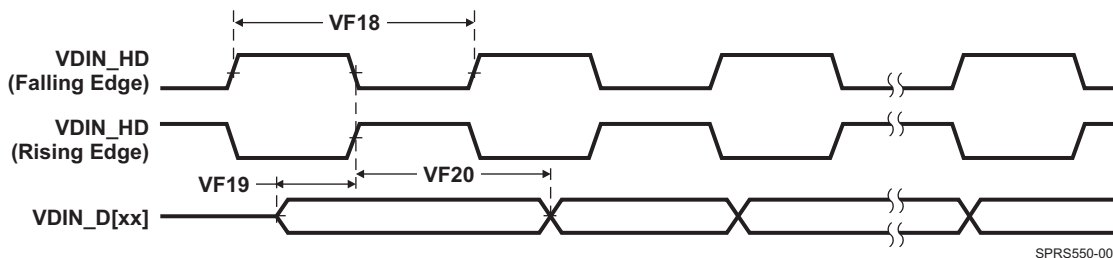


Figure 6-34. VPFE Input Timings With VDIN0\_HD as Pixel Clock

## 6.5.2 Display Subsystem (DSS)

The display subsystem (DSS) provides the logic to display the video frame from external (SDRAM) or internal (SRAM) memory on an LCD panel or a TV set. The DSS integrates a display controller. It can be used in two configurations:

- LCD display support in:
  - Bypass mode (RFBI module bypassed)
  - RFBI mode (through RFBI module)
- TV display support (not discussed in this document because of its analog IO signals)

The two display supports can be active at the same time.

### 6.5.2.1 LCD Display Support in Bypass Mode

Two types of LCD panel are supported:

- Thin film transistor (TFT) or active matrix technology
- Supertwisted nematic (STN) or passive matrix technology

Both configurations are discussed in the following paragraphs.

### 6.5.2.1.1 LCD Display in TFT Mode

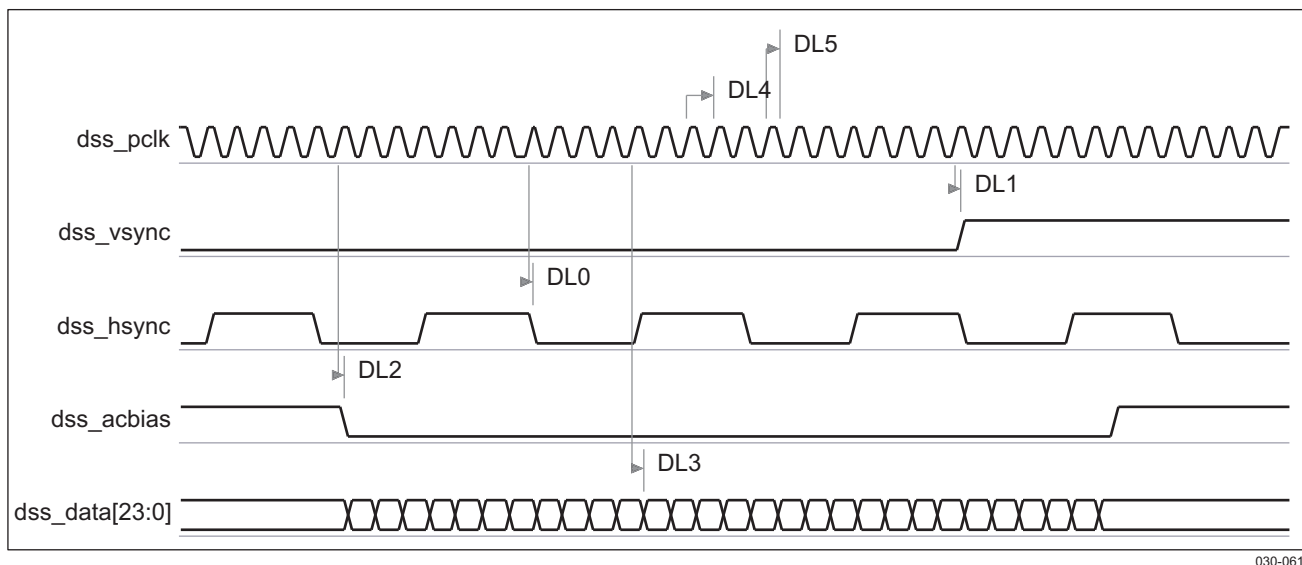
Table 6-36 assumes testing over the recommended operating conditions (see Figure 6-35).

**Table 6-36. LCD Display Interface Switching Characteristics in TFT Mode<sup>(1)</sup>**

| NO. | PARAMETER                   |                                                             | 1.8V, 3.3V |       | UNIT |
|-----|-----------------------------|-------------------------------------------------------------|------------|-------|------|
|     |                             |                                                             | MIN        | MAX   |      |
| DL0 | $t_d(\text{PCLKA-HSYNT})$   | Delay time, dss_pclk active edge to dss_hsync transition    | -4.215     | 4.215 | ns   |
| DL1 | $t_d(\text{PCLKA-VSYNT})$   | Delay time, dss_pclk active edge to dss_vsync transition    | -4.215     | 4.215 | ns   |
| DL2 | $t_d(\text{PCLKA-ACBIASA})$ | Delay time, dss_pclk active edge to dss_acbias active level | -4.215     | 4.215 | ns   |
| DL3 | $t_d(\text{PCLKA-DATAV})$   | Delay time, dss_pclk active edge to dss_data bus valid      | -4.215     | 4.215 | ns   |
| DL4 | $t_c(\text{PCLK})$          | Cycle time <sup>(2)</sup> , dss_pclk                        | 13.468     |       | ns   |
| DL5 | $t_w(\text{PCLK})$          | Pulse duration, dss_pclk low or high                        | 6.06       | 7.46  | ns   |
|     | $C_{load}$                  | Load capacitance                                            |            | 25    | pF   |

(1) The capacitive load is equivalent to 25 pF.

(2) The pixel clock frequency is software programmable via the pixel clock divider configuration from 1 to 255 division range in the DISPC\_DIVISOR register.



030-061

**Figure 6-35. LCD Display in TFT Mode(1) (2) (3) (4)**

(1) The pixel data bus depends on the use of 8-, 9-, 12-, 16-, 18-, or 24-bit per pixel data output pins.

(2) The pixel clock frequency is programmable.

(3) All timings not illustrated in the waveform are programmable by software, control signal polarity, and driven edge of dss\_pclk.

(4) For more information, see the AM35x ARM Microprocessor Technical Reference Manual ([SPRUGR0](#)).

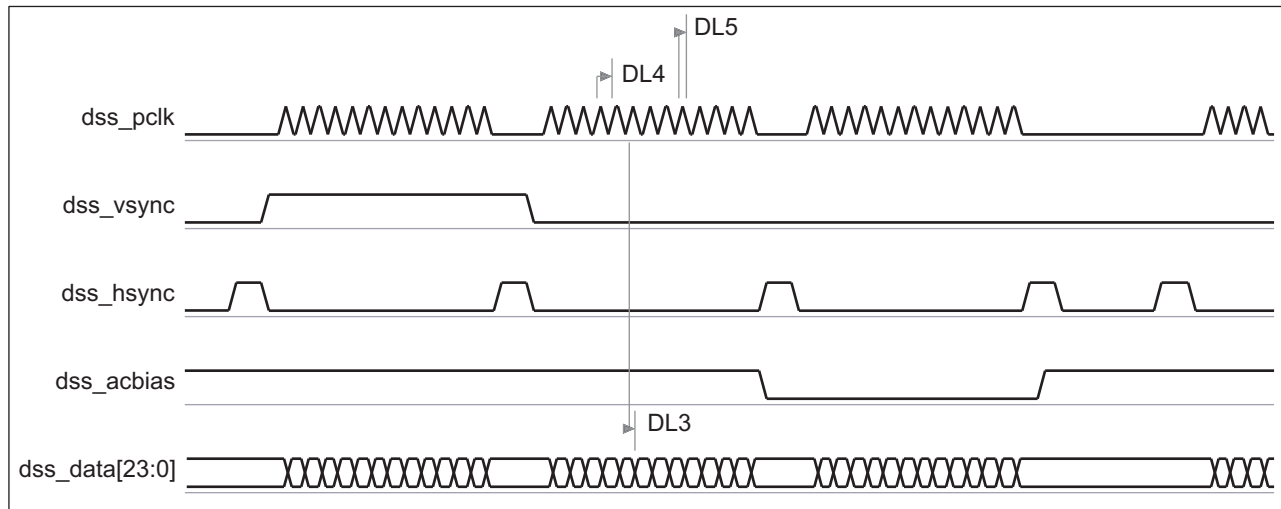
### 6.5.2.1.2 LCD Display in STN Mode

Table 6-37 assumes testing over the recommended operating conditions (see Figure 6-36).

**Table 6-37. LCD Display Interface Switching Characteristics in STN Mode<sup>(1) (2) (3)</sup>**

| NO. | PARAMETER                 |                                                        | 1.8V, 3.3V |      | UNIT |
|-----|---------------------------|--------------------------------------------------------|------------|------|------|
|     |                           |                                                        | MIN        | MAX  |      |
| DL3 | $t_d(\text{PCLKA-DATAV})$ | Delay time, dss_pclk active edge to dss_data bus valid | -4.21      | 6.9  | ns   |
| DL4 | $t_c(\text{PCLK})$        | Cycle time <sup>(4)</sup> , dss_pclk                   | 22.73      |      | ns   |
| DL5 | $t_w(\text{PCLK})$        | Pulse duration, dss_pclk low or high                   | 10.23      | 12.5 | ns   |
|     | $C_{load}$                | Load capacitance                                       |            | 40   | pF   |

- (1) The DSS in STN mode is used with 4 or 8 pins only; unused pixel data bits always remain low.
- (2) The capacitive load is equivalent to 40 pF.
- (3) For more information, see the *AM35x ARM Microprocessor Technical Reference Manual* ([SPRUGR0](#)).
- (4) The pixel clock frequency is software programmable via the pixel clock divider configuration from 1 to 255 division range in the DISPC\_DIVISOR register.



030-062

**Figure 6-36. LCD Display in STN Mode<sup>(1) (2) (3) (4) (5)</sup>**

- (1) The pixel data bus depends on the use 4-, 8-, 12-, 16-, 18-, or 24-bit per pixel data output pins.
- (2) All timings not illustrated in the waveform are programmable by software, control signal polarity, and driven edge of dss\_pclk.
- (3) dss\_vsync width must be programmed to be as small as possible.
- (4) The pixel clock frequency is programmable.
- (5) For more information, see the *AM35x ARM Microprocessor Technical Reference Manual* ([SPRUGR0](#)).

## 6.6 Serial Communications Interfaces

### 6.6.1 Multichannel Buffered Serial Port (McBSP) Timing

There are five McBSP modules called McBSP1 through McBSP5. McBSP provides a full-duplex, direct serial interface between the AM3517/05 device and other devices in a system such as other application devices or codecs. It can accommodate a wide range of peripherals and clocked frame-oriented protocols (I2S, PCM, and TDM) due to its high level of versatility.

The McBSP1-5 modules may support two types of data transfer at the system level:

- The full-cycle mode, for which one clock period is used to transfer the data, generated on one edge and captured on the same edge (one clock period later).
- The half-cycle mode, for which one half clock period is used to transfer the data, generated on one edge and captured on the opposite edge (one half clock period later). Note that a new data is generated only every clock period, which secures the required hold time.

The interface clock (CLKX/CLKR) activation edge (data/frame sync capture and generation) has to be configured accordingly with the external peripheral (activation edge capability) and the type of data transfer required at the system level.

The AM3517/05 McBSP1-5 timing characteristics are described for both rising and falling activation edges. McBSP1 supports:

- 6-pin mode: dx and dr as data pins; clkx, clkr, fsx, and fsr as control pins.
- 4-pin mode: dx and dr as data pins; clkx and fsx pins as control pins. The clkx and fsx pins are internally looped back via software configuration, respectively, to the clkr and fsr internal signals for data receive.

McBSP2, 3, 4, and 5 support only the 4-pin mode.

The following sections describe the timing characteristics for applications in normal mode (that is, AM3517/05 McBSPx connected to one peripheral) and TDM applications in multipoint mode.

#### 6.6.1.1 McBSP in Normal Mode

Table 6-38 through Table 6-40 assume testing over the recommended operating conditions.

**Table 6-38. McBSP Timing Conditions**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3 V      | UNIT |
|----------------------------|-------------------------|------------------|------|
| <b>Input Conditions</b>    |                         | VALUE            |      |
| $t_R$                      | Input signal rise time  | 2 <sup>(1)</sup> | ns   |
| $t_F$                      | Input signal fall time  | 2                | ns   |
| <b>Output Conditions</b>   |                         |                  |      |
| $C_{LOAD}$                 | Output load capacitance | 10               | pF   |

(1) Maximum value.

**Table 6-39. McBSP1,2,4,5 Output Clock Pulse Duration**

| PARAMETER          |                                                                   | VDDSHV = 1.8V, 3.3V  |                      | UNIT |
|--------------------|-------------------------------------------------------------------|----------------------|----------------------|------|
|                    |                                                                   | MIN                  | MAX                  |      |
| $t_C(\text{CLK})$  | Cycle Time,<br>mcbasp1_clkr/mcbasp1_clkx<br>(1)                   | 20.83                |                      | ns   |
| $t_W(\text{CLKH})$ | Typical pulse duration,<br>mcbasp1_clkr /<br>mcbasp1_clkx high(1) | 0.5*P <sup>(2)</sup> | 0.5*P <sup>(2)</sup> | ns   |

(1) In mcbasp1, x identifies the McBSP number; 1, 2, 4, or 5.

(2) P = mcbasp1\_clkr / mcbasp1\_clkx clock period.

**Table 6-39. McBSP1,2,4,5 Output Clock Pulse Duration (continued)**

| PARAMETER |                                                                        | VDDSHV = 1.8V, 3.3V  |                      | UNIT |
|-----------|------------------------------------------------------------------------|----------------------|----------------------|------|
| tW(CLKL)  | Typical pulse duration, mcbbsp1_clkr / mcbbsp1_clkx low <sup>(1)</sup> | 0.5*P <sup>(2)</sup> | 0.5*P <sup>(2)</sup> | ns   |
| tdc(CLK)  | Duty cycle error, mcbbsp1_clkr / mcbbsp1_clkx <sup>(1)</sup>           | -0.75                | 0.75                 | ns   |

**Table 6-40. McBSP3 Output Clock Pulse Duration**

| PARAMETER |                                           | VDDSHV = 1.8V, 3.3V  |                      | UNIT |
|-----------|-------------------------------------------|----------------------|----------------------|------|
|           |                                           | MIN                  | MAX                  |      |
| tC(CLK)   | Cycle time, mcbbsp3_clkx                  | 31.25                |                      | ns   |
| tW(CLKH)  | Typical pulse duration, mcbbsp3_clkx high | 0.5*P <sup>(1)</sup> | 0.5*P <sup>(1)</sup> | ns   |
| tW(CLKL)  | Typical pulse duration, mcbbsp3_clkx low  | 0.5*P <sup>(1)</sup> | 0.5*P <sup>(1)</sup> | ns   |
| tdc(CLK)  | Duty cycle error, mcbbsp3_clkx            | -0.75                | 0.75                 | ns   |

(1) P = mcbbsp3\_clkx clock period

#### 6.6.1.1.1 McBSP1

Table 6-41 through Table 6-48 list the timing requirements and switching characteristics for McBSP1.

**Table 6-41. McBSP1 Timing Requirements - Rising Edge and Receive Mode**

| No. | PARAMETER      |                                                                                            |                   | VDDSHV=3.3V |     | VDDSHV=1.8V |     | UNIT |
|-----|----------------|--------------------------------------------------------------------------------------------|-------------------|-------------|-----|-------------|-----|------|
|     |                |                                                                                            |                   | MIN         | MAX | MIN         | MAX |      |
| B3  | tsu(DRV-CLKAE) | Setup time, mcbbsp1_dr valid before mcbbsp1_clkr / mcbbsp1_clkx active edge                | Half Cycle Master | 5.0         |     | 5.0         |     | ns   |
|     |                |                                                                                            | Half Cycle Slave  | 5.2         |     | 5.2         |     | ns   |
|     |                |                                                                                            | Full Cycle Master | 4.0         |     | 4.0         |     | ns   |
|     |                |                                                                                            | Full Cycle Slave  | 4.2         |     | 4.2         |     | ns   |
| B4  | th(CLKAE-DRV)  | Hold time, mcbbsp1_dr valid after mcbbsp1_clkr / mcbbsp1_clkx active edge                  | Half Cycle Master | 5.8         |     | 5.8         |     | ns   |
|     |                |                                                                                            | Half Cycle Slave  | 5.2         |     | 5.2         |     | ns   |
|     |                |                                                                                            | Full Cycle Master | 1.5         |     | 1.5         |     | ns   |
|     |                |                                                                                            | Full Cycle Slave  | 0.9         |     | 0.9         |     | ns   |
| B5  | tsu(FSV-CLKAE) | Setup time, mcbbsp1_fsr / mcbbsp1_fsx valid before mcbbsp1_clkr / mcbbsp1_clkx active edge | Half Cycle Slave  | 5.2         |     | 5.2         |     | ns   |
|     |                |                                                                                            | Full Cycle Slave  | 4.2         |     | 4.2         |     | ns   |
| B6  | th(CLKAE-FSV)  | Hold time, mcbbsp1_fsr / mcbbsp1_fsx valid after mcbbsp1_clkr / mcbbsp1_clkx active edge   | Half Cycle Slave  | 0.5         |     | 0.5         |     | ns   |
|     |                |                                                                                            | Full Cycle Slave  | 1.0         |     | 1.0         |     | ns   |

**Table 6-42. McBSP1 Switching Characteristics - Rising Edge and Receive Mode**

| No. | PARAMETER     |                                                                         |  | VDDSHV=3.3V |      | VDDSHV=1.8V |      | UNIT |
|-----|---------------|-------------------------------------------------------------------------|--|-------------|------|-------------|------|------|
|     |               |                                                                         |  | MIN         | MAX  | MIN         | MAX  |      |
| B2  | td(CLKAE-FSV) | Delay time, mcbbsp1_clkr active edge to mcbbsp1_fsr / mcbbsp1_fsx valid |  | 0.2         | 14.8 | 0.2         | 14.8 | ns   |

**Table 6-43. McBSP1 Timing Requirements - Rising Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp1_fsx valid before mcbbsp1_clkx active edge | Full Cycle Slave | 5.2           |     | 4.7           |     | ns   |
|     |                  |                                                               | Half Cycle Slave | 4.2           |     | 3.7           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbbsp1_fsx valid after mcbbsp1_clkx active edge   | Full Cycle Slave | 5.2           |     | 4.7           |     | ns   |
|     |                  |                                                               | Half Cycle Slave | 1.0           |     | 0.5           |     | ns   |

**Table 6-44. McBSP1 Switching Characteristics - Rising Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                 |                                                           |        | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp1_clkx active edge to mcbbsp1_fsx valid |        | 0.2           | 14.8 | 0.7           | 14.8 | ns   |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbbsp1_clkx active edge to mcbbsp1_dx valid  | Master | 0.6           | 14.8 | 0.6           | 14.8 | ns   |
|     |                 |                                                           | Slave  | 0.6           | 14.8 | 0.6           | 14.8 | ns   |

**Table 6-45. McBSP1 Timing Requirements - Falling Edge and Receive Mode**

| No. | PARAMETER      |                                                                                            |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|----------------|--------------------------------------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                |                                                                                            |                   | MIN           | MAX | MIN           | MAX |      |
| B3  | tsu(DRV-CLKAE) | Setup time, mcbbsp1_dr valid before mcbbsp1_clkr / mcbbsp1_clkx active edge                | Half Cycle Master | 5.0           |     | 5.0           |     | ns   |
|     |                |                                                                                            | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                |                                                                                            | Full Cycle Master | 4.0           |     | 4.0           |     | ns   |
|     |                |                                                                                            | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |
| B4  | th(CLKAE-DRV)  | Hold time, mcbbsp1_dr valid after mcbbsp1_clkr / mcbbsp1_clkx active edge                  | Half Cycle Master | 5.8           |     | 5.8           |     | ns   |
|     |                |                                                                                            | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                |                                                                                            | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                |                                                                                            | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |
| B5  | tsu(FSV-CLKAE) | Setup time, mcbbsp1_fsr / mcbbsp1_fsx valid before mcbbsp1_clkr / mcbbsp1_clkx active edge | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                |                                                                                            | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |

**Table 6-45. McBSP1 Timing Requirements - Falling Edge and Receive Mode (continued)**

| No. | PARAMETER     |                                                                                          |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|---------------|------------------------------------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |               |                                                                                          |                  | MIN           | MAX | MIN           | MAX |      |
| B6  | th(CLKAE-FSV) | Hold time, mcbbsp1_fsr / mcbbsp1_fsx valid after mcbbsp1_clkx / mcbbsp1_clkx active edge | Half Cycle Slave | 0.5           |     | 0.5           |     | ns   |
|     |               |                                                                                          | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-46. McBSP1 Switching Characteristics - Falling Edge and Receive Mode**

| No. | PARAMETER     |                                                                                        |  | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|---------------|----------------------------------------------------------------------------------------|--|---------------|------|---------------|------|------|
|     |               |                                                                                        |  | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKAE-FSV) | Delay time, mcbbsp1_clkx / mcbbsp1_clkx active edge to mcbbsp1_fsr / mcbbsp1_fsx valid |  | 0.2           | 14.8 | 0.7           | 14.8 | ns   |

**Table 6-47. McBSP1 Timing Requirements - Falling Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp1_fsx valid before mcbbsp1_clkx active edge | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 4.2           |     | 4.2           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbbsp1_fsx valid after mcbbsp1_clkx active edge   | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-48. McBSP1 Switching Characteristics - Falling Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                 |                                                           |        | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp1_clkx active edge to mcbbsp1_fsx valid |        | 0.2           | 14.8 | 0.2           | 14.8 | ns   |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbbsp1_clkx active edge to mcbbsp1_dx valid  | Master | 0.6           | 14.8 | 0.6           | 14.8 | ns   |
|     |                 |                                                           | Slave  | 0.6           | 14.8 | 0.6           | 14.8 | ns   |

### 6.6.1.1.2 McBSP2

Table 6-49 through Table 6-56 list the timing requirements and switching characteristics for McBSP2.

**Table 6-49. McBSP2 Timing Requirements - Rising Edge and Receive Mode**

| No. | PARAMETER       |                                                               |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------------|---------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                 |                                                               |                   | MIN           | MAX | MIN           | MAX |      |
| B3  | tsu(DRV-CLKXAE) | Setup time, mcbbsp2_dr valid before mcbbsp2_clkx active edge  | Half Cycle Master | 5.0           |     | 5.0           |     | ns   |
|     |                 |                                                               | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                               | Full Cycle Master | 4.2           |     | 4.2           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |
| B4  | th(CLKXAE-DRV)  | Hold time, mcbbsp2_dr valid after mcbbsp2_clkx active edge    | Half Cycle Master | 5.8           |     | 5.8           |     | ns   |
|     |                 |                                                               | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                               | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |
| B5  | tsu(FSV-CLKXAE) | Setup time, mcbbsp2_fsx valid before mcbbsp2_clkx active edge | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |
| B6  | th(CLKXAE-FSV)  | Hold time, mcbbsp2_fsx valid after mcbbsp2_clkx active edge   | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 1.0           |     | 1.0           |     | ns   |

**Table 6-50. McBSP2 Switching Characteristics - Rising Edge and Receive Mode**

| No. | PARAMETER       |                                                           |  | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--|---------------|------|---------------|------|------|
|     |                 |                                                           |  | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp2_clkx active edge to mcbbsp2_fsx valid |  | 0.2           | 14.8 | 0.2           | 14.8 | ns   |

**Table 6-51. McBSP2 Timing Requirements - Rising Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp2_fsx valid before mcbbsp2_clkx active edge | Half Cycle Slave | 5.2           |     | 4.7           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 4.2           |     | 3.7           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbbsp2_fsx valid after mcbbsp2_clkx active edge   | Half Cycle Slave | 5.2           |     | 4.7           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 1.0           |     | 0.5           |     | ns   |

**Table 6-52. McBSP2 Switching Characteristics - Rising Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                 |                                                           |        | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp2_clkx active edge to mcbbsp2_fsx valid |        | 0.2           | 14.8 | 0.2           | 14.8 | ns   |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbbsp2_clkx active edge to mcbbsp2_dx valid  | Master | 0.6           | 14.8 | 0.6           | 14.8 | ns   |
|     |                 |                                                           | Slave  | 0.6           | 14.8 | 0.6           | 14.8 | ns   |

**Table 6-53. McBSP2 Timing Requirements - Falling Edge and Receive Mode**

| No. | PARAMETER        |                                                               |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                   | MIN           | MAX | MIN           | MAX |      |
| B3  | tsu(DRV-CLKXAE)  | Setup time, mcbbsp2_dr valid before mcbbsp2_clkx active edge  | Half Cycle Master | 5.0           |     | 5.0           |     | ns   |
|     |                  |                                                               | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Master | 4.2           |     | 4.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |
| B4  | th(CLKXAE-DRV)   | Hold time, mcbbsp2_dr valid after mcbbsp2_clkx active edge    | Half Cycle Master | 5.8           |     | 5.8           |     | ns   |
|     |                  |                                                               | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                  |                                                               | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp2_fsx valid before mcbbsp2_clkx active edge | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbbsp2_fsx valid after mcbbsp2_clkx active edge   | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave  | 1.0           |     | 1.0           |     | ns   |

**Table 6-54. McBSP2 Switching Characteristics - Falling Edge and Receive Mode**

| No. | PARAMETER       |                                                           |  | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--|---------------|------|---------------|------|------|
|     |                 |                                                           |  | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp2_clkx active edge to mcbbsp2_fsx valid |  | 0.2           | 14.8 | 0.2           | 14.8 | ns   |

**Table 6-55. McBSP2 Timing Requirements - Falling Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp2_fsx valid before mcbbsp2_clkx active edge | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 4.2           |     | 4.2           |     | ns   |

**Table 6-55. McBSP2 Timing Requirements - Falling Edge and Transmit Mode (continued)**

| No. | PARAMETER       |                                                             |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------------|-------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                 |                                                             |                  | MIN           | MAX | MIN           | MAX |      |
| B6  | th(CLKXAE-FSXV) | Hold time, mcbbsp2_fsx valid after mcbbsp2_clkx active edge | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                             | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-56. McBSP2 Switching Characteristics - Falling Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                 |                                                           |        | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp2_clkx active edge to mcbbsp2_fsx valid |        | 0.2           | 14.8 | 0.2           | 14.8 | ns   |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbbsp2_clkx active edge to mcbbsp2_dx valid  | Master | 0.6           | 14.8 | 0.6           | 14.8 | ns   |
|     |                 |                                                           | Slave  | 0.6           | 14.8 | 0.6           | 14.8 | ns   |

**6.6.1.1.3 McBSP3****6.6.1.1.3.1 McBSP3 Multiplexed on McBSP3 Pins**

Table 6-57 through Table 6-64 list the timing conditions and switching characteristics for McBSP3 multiplexed on McBSP3 pins.

**Note:** All timings apply only to Set #1- multiplexing on mcbbsp3 pins.

**Table 6-57. McBSP3 (Set #1) Timing Requirements - Rising Edge and Receive Mode**

| No. | PARAMETER       |                                                               |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------------|---------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                 |                                                               |                   | MIN           | MAX | MIN           | MAX |      |
| B3  | tsu(DRV-CLKXAE) | Setup time, mcbbsp3_dr valid before mcbbsp3_clkx active edge  | Half Cycle Master | 7.5           |     | 7.5           |     | ns   |
|     |                 |                                                               | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Master | 5.6           |     | 5.6           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 5.8           |     | 5.8           |     | ns   |
| B4  | th(CLKXAE-DRV)  | Hold time, mcbbsp3_dr valid after mcbbsp3_clkx active edge    | Half Cycle Master | 8.3           |     | 8.3           |     | ns   |
|     |                 |                                                               | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |
| B5  | tsu(FSV-CLKXAE) | Setup time, mcbbsp3_fsx valid before mcbbsp3_clkx active edge | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 5.8           |     | 5.8           |     | ns   |
| B6  | th(CLKXAE-FSV)  | Hold time, mcbbsp3_fsx valid after mcbbsp3_clkx active edge   | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 1.0           |     | 1.0           |     | ns   |

**Table 6-58. McBSP3 (Set #1) Switching Characteristics - Rising Edge and Receive Mode**

| No. | PARAMETER       |                                                           | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|---------------|------|---------------|------|------|
|     |                 |                                                           | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp3_clkx active edge to mcbbsp3_fsx valid | 0.2           | 22.2 | 0.2           | 22.2 | ns   |

**Table 6-59. McBSP3 (Set #1) Timing Requirements - Rising Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp3_fsx valid before mcbbsp3_clkx active edge | Half Cycle Slave | 7.7           |     | 7.7           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 5.8           |     | 5.8           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbbsp3_fsx valid after mcbbsp3_clkx active edge   | Half Cycle Slave | 7.7           |     | 7.7           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 1             |     | 1             |     | ns   |

**Table 6-60. McBSP3 (Set #1) Switching Characteristics - Rising Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                 |                                                           |        | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp3_clkx active edge to mcbbsp3_fsx valid |        | 0.2           | 22.2 | 0.2           | 22.2 | ns   |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbbsp3_clkx active edge to mcbbsp3_dx valid  | Master | 0.6           | 22.2 | 0.6           | 22.2 | ns   |
|     |                 |                                                           | Slave  | 0.6           | 22.2 | 0.6           | 22.2 | ns   |

**Table 6-61. McBSP3 (Set #1) Timing Requirements - Falling Edge and Receive Mode**

| No. | PARAMETER         |                                                               |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-------------------|---------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                   |                                                               |                   | MIN           | MAX | MIN           | MAX |      |
|     | tsu(DRV-CLKXAE)   | Setup time, mcbbsp3_dr valid before mcbbsp3_clkx active edge  | Half Cycle Master | 7.5           |     | 7.5           |     | ns   |
|     |                   |                                                               | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                   |                                                               | Full Cycle Master | 5.6           |     | 5.6           |     | ns   |
|     |                   |                                                               | Full Cycle Slave  | 5.8           |     | 5.8           |     | ns   |
|     | th(CLKXAE-DRV)    | Hold time, mcbbsp3_dr valid after mcbbsp3_clkx active edge    | Half Cycle Master | 8.3           |     | 8.3           |     | ns   |
|     |                   |                                                               | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                   |                                                               | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                   |                                                               | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |
| B5  | tsu(FXSXV-CLKXAE) | Setup time, mcbbsp3_fsx valid before mcbbsp3_clkx active edge | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                   |                                                               | Full Cycle Slave  | 5.8           |     | 5.8           |     | ns   |
| B6  | th(CLKXAE-FSXV)   | Hold time, mcbbsp3_fsx valid after mcbbsp3_clkx active edge   | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                   |                                                               | Full Cycle Slave  | 1.0           |     | 1.0           |     | ns   |

**Table 6-62. McBSP3 (Set #1) Switching Characteristics - Falling Edge and Receive Mode**

| No. | PARAMETER       |                                                           | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|---------------|------|---------------|------|------|
|     |                 |                                                           | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp3_clkx active edge to mcbbsp3_fsx valid | 0.2           | 22.2 | 0.2           | 22.2 | ns   |

**Table 6-63. McBSP3 (Set #1) Timing Requirements - Falling Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp3_fsx valid before mcbbsp3_clkx active edge | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 4.2           |     | 4.2           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbbsp3_fsx valid after mcbbsp3_clkx active edge   | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-64. McBSP3 (Set #1) Switching Characteristics - Falling Edge and Transmit Mode**

| No. | PARAMETER       |                                                           | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |    |
|-----|-----------------|-----------------------------------------------------------|---------------|------|---------------|------|------|----|
|     |                 |                                                           | MIN           | MAX  | MIN           | MAX  |      |    |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp3_clkx active edge to mcbbsp3_fsx valid | 0.2           | 22.2 | 0.2           | 22.2 | ns   |    |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbbsp3_clkx active edge to mcbbsp3_dx valid  | Master        | 0.6  | 22.2          | 0.6  | 22.2 | ns |
|     |                 |                                                           | Slave         | 0.6  | 22.2          | 0.6  | 22.2 | ns |

**6.6.1.1.3.2 McBSP3 Multiplexed on UART2 or McBSP1 Pins**

Table 6-65 through Table 6-72 list the timing conditions and switching characteristics for McBSP3 multiplexed on UART2 or McBSP1 pins.

Note: These timings only apply to Set #2 (multiplexing mode on uart2 pins) and Set #3 (multiplexing on mcbbsp1 pins).

**Table 6-65. McBSP3 (Sets #2 and #3) Timing Requirements - Rising Edge and Receive Mode**

| No. | PARAMETER       |                                                              |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------------|--------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                 |                                                              |                   | MIN           | MAX | MIN           | MAX |      |
| B3  | tsu(DRV-CLKXAE) | Setup time, mcbbsp3_dr valid before mcbbsp3_clkx active edge | Half Cycle Master | 5.0           |     | 5.0           |     | ns   |
|     |                 |                                                              | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                              | Full Cycle Master | 4.2           |     | 4.2           |     | ns   |
|     |                 |                                                              | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |
| B4  | th(CLKXAE-DRV)  | Hold time, mcbbsp3_dr valid after mcbbsp3_clkx active edge   | Half Cycle Master | 5.8           |     | 5.8           |     | ns   |
|     |                 |                                                              | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                              | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                 |                                                              | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |

**Table 6-65. McBSP3 (Sets #2 and #3) Timing Requirements - Rising Edge and Receive Mode (continued)**

| No. | PARAMETER       |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                 |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSV-CLKXAE) | Setup time, mcbbsp3_fsx valid before mcbbsp3_clkx active edge | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                               | Full Cycle Slave | 4.2           |     | 4.2           |     | ns   |
| B6  | th(CLKXAE-FSV)  | Hold time, mcbbsp3_fsx valid after mcbbsp3_clkx active edge   | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                               | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-66. McBSP3 (Sets #2 and #3) Switching Characteristics - Rising Edge and Receive Mode**

| No. | PARAMETER       |                                                           |  | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--|---------------|------|---------------|------|------|
|     |                 |                                                           |  | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp3_clkx active edge to mcbbsp3_fsx valid |  | 0.2           | 14.8 | 0.2           | 14.8 | ns   |

**Table 6-67. McBSP3 (Sets #2 and #3) Timing Requirements - Rising Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp3_fsx valid before mcbbsp3_clkx active edge | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 4.2           |     | 4.2           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbbsp3_fsx valid after mcbbsp3_clkx active edge   | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-68. McBSP3 (Sets #2 and #3) Switching Characteristics - Rising Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                 |                                                           |        | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp3_clkx active edge to mcbbsp3_fsx valid |        | 0.2           | 14.8 | 0.2           | 14.8 | ns   |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbbsp3_clkx active edge to mcbbsp3_dx valid  | Master | 0.6           | 14.8 | 0.6           | 14.8 | ns   |
|     |                 |                                                           | Slave  | 0.6           | 14.8 | 0.6           | 14.8 | ns   |

**Table 6-69. McBSP3 (Sets #2 and #3) Timing Requirements - Falling Edge and Receive Mode**

| No. | PARAMETER       |                                                              |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------------|--------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                 |                                                              |                   | MIN           | MAX | MIN           | MAX |      |
| B3  | tsu(DRV-CLKXAE) | Setup time, mcbbsp3_dr valid before mcbbsp3_clkx active edge | Half Cycle Master | 5.0           |     | 5.0           |     | ns   |
|     |                 |                                                              | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                              | Full Cycle Master | 4.2           |     | 4.2           |     | ns   |
|     |                 |                                                              | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |

**Table 6-69. McBSP3 (Sets #2 and #3) Timing Requirements - Falling Edge and Receive Mode (continued)**

| No. | PARAMETER         |                                                               |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-------------------|---------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                   |                                                               |                   | MIN           | MAX | MIN           | MAX |      |
| B4  | th(CLKXAE-DRV)    | Hold time, mcbbsp3_dr valid after mcbbsp3_clkx active edge    | Half Cycle Master | 5.8           |     | 5.8           |     | ns   |
|     |                   |                                                               | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                   |                                                               | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                   |                                                               | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |
| B5  | tsu(FXSXV-CLKXAE) | Setup time, mcbbsp3_fsx valid before mcbbsp3_clkx active edge | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                   |                                                               | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |
| B6  | th(CLKXAE-FSXV)   | Hold time, mcbbsp3_fsx valid after mcbbsp3_clkx active edge   | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                   |                                                               | Full Cycle Slave  | 1.0           |     | 1.0           |     | ns   |

**Table 6-70. McBSP3 (Sets #2 and #3) Switching Characteristics - Falling Edge and Receive Mode**

| No. | PARAMETER       |                                                           | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|---------------|------|---------------|------|------|
|     |                 |                                                           | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp3_clkx active edge to mcbbsp3_fsx valid | 0.2           | 14.8 | 0.2           | 14.8 | ns   |

**Table 6-71. McBSP3 (Sets #2 and #3) Timing Requirements - Falling Edge and Transmit Mode**

| No. | PARAMETER         |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                   |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FXSXV-CLKXAE) | Setup time, mcbbsp3_fsx valid before mcbbsp3_clkx active edge | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                   |                                                               | Full Cycle Slave | 4.2           |     | 4.2           |     | ns   |
| B6  | th(CLKXAE-FSXV)   | Hold time, mcbbsp3_fsx valid after mcbbsp3_clkx active edge   | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                   |                                                               | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-72. McBSP3 (Sets #2 and #3) Switching Characteristics - Falling Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                 |                                                           |        | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp3_clkx active edge to mcbbsp3_fsx valid |        | 0.2           | 14.8 | 0.2           | 14.8 | ns   |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbbsp3_clkx active edge to mcbbsp3_dx valid  | Master | 0.6           | 14.8 | 0.6           | 14.8 | ns   |
|     |                 |                                                           | Slave  | 0.6           | 14.8 | 0.6           | 14.8 | ns   |

**6.6.1.1.4 McBSP4**

Table 6-73 through Table 6-80 list the timing requirements and switching characteristics for McBSP4.

**Table 6-73. McBSP4 Timing Requirements - Rising Edge and Receive Mode**

| No. | PARAMETER |  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------|--|---------------|-----|---------------|-----|------|
|     |           |  | MIN           | MAX | MIN           | MAX |      |

**Table 6-73. McBSP4 Timing Requirements - Rising Edge and Receive Mode (continued)**

| No. | PARAMETER       |                                                               |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------------|---------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                 |                                                               |                   | MIN           | MAX | MIN           | MAX |      |
| B3  | tsu(DRV-CLKXAE) | Setup time, mcbbsp4_dr valid before mcbbsp4_clkx active edge  | Half Cycle Master | 7.5           |     | 7.5           |     | ns   |
|     |                 |                                                               | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Master | 3.2           |     | 3.2           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |
| B4  | th(CLKXAE-DRV)  | Hold time, mcbbsp4_dr valid after mcbbsp4_clkx active edge    | Half Cycle Master | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                               | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |
| B5  | tsu(FSV-CLKXAE) | Setup time, mcbbsp4_fsx valid before mcbbsp4_clkx active edge | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 4.2           |     | 4.2           |     | ns   |
| B6  | th(CLKXAE-FSV)  | Hold time, mcbbsp4_fsx valid after mcbbsp4_clkx active edge   | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 1.0           |     | 1.0           |     | ns   |

**Table 6-74. McBSP4 Switching Characteristics - Rising Edge and Receive Mode**

| No. | PARAMETER       |                                                           |  | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--|---------------|------|---------------|------|------|
|     |                 |                                                           |  | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp4_clkx active edge to mcbbsp4_fsx valid |  | 0.2           | 16.6 | 0.2           | 16.6 | ns   |

**Table 6-75. McBSP4 Timing Requirements - Rising Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp4_fsx valid before mcbbsp4_clkx active edge | Half Cycle Slave | 7.7           |     | 7.7           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 3.7           |     | 3.7           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbbsp4_fsx valid after mcbbsp4_clkx active edge   | Half Cycle Slave | 1.0           |     | 1.0           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-76. McBSP4 Switching Characteristics - Rising Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |  | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--|---------------|------|---------------|------|------|
|     |                 |                                                           |  | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp4_clkx active edge to mcbbsp4_fsx valid |  | 0.2           | 16.6 | 0.2           | 16.6 | ns   |

**Table 6-76. McBSP4 Switching Characteristics - Rising Edge and Transmit Mode (continued)**

| No. | PARAMETER      |                                                          |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|----------------|----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                |                                                          |        | MIN           | MAX  | MIN           | MAX  |      |
| B8  | td(CLKXAE-DXV) | Delay time, mcbbsp4_clkx active edge to mcbbsp4_dx valid | Master | 0.6           | 16.6 | 0.6           | 16.6 | ns   |
|     |                |                                                          | Slave  | 0.6           | 17.3 | 0.6           | 17.3 | ns   |

**Table 6-77. McBSP4 Timing Requirements - Falling Edge and Receive Mode**

| No. | PARAMETER        |                                                               |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                   | MIN           | MAX | MIN           | MAX |      |
| B3  | tsu(DRV-CLKXAE)  | Setup time, mcbbsp4_dr valid before mcbbsp4_clkx active edge  | Half Cycle Master | 7.5           |     | 7.5           |     | ns   |
|     |                  |                                                               | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                  |                                                               | Full Cycle Master | 5.6           |     | 5.6           |     | ns   |
|     |                  |                                                               | Full Cycle Slave  | 5.8           |     | 5.8           |     | ns   |
| B4  | th(CLKXAE-DRV)   | Hold time, mcbbsp4_dr valid after mcbbsp4_clkx active edge    | Half Cycle Master | 7.7           |     | 7.7           |     | ns   |
|     |                  |                                                               | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                  |                                                               | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |
| B5  | tsu(FXSV-CLKXAE) | Setup time, mcbbsp4_fsx valid before mcbbsp4_clkx active edge | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                  |                                                               | Full Cycle Slave  | 5.8           |     | 5.8           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbbsp4_fsx valid after mcbbsp4_clkx active edge   | Half Cycle Slave  | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave  | 1.0           |     | 1.0           |     | ns   |

**Table 6-78. McBSP4 Switching Characteristics - Falling Edge and Receive Mode**

| No. | PARAMETER       |                                                           |  | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--|---------------|------|---------------|------|------|
|     |                 |                                                           |  | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp4_clkx active edge to mcbbsp4_fsx valid |  | 0.2           | 16.6 | 0.2           | 16.6 | ns   |

**Table 6-79. McBSP4 Timing Requirements - Falling Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp4_fsx valid before mcbbsp4_clkx active edge | Half Cycle Slave | 7.7           |     | 7.7           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 3.7           |     | 3.7           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbbsp4_fsx valid after mcbbsp4_clkx active edge   | Half Cycle Slave | 5.2           |     | 5.2           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-80. McBSP4 Switching Characteristics - Falling Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                 |                                                           |        | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp4_clkx active edge to mcbbsp4_fsx valid |        | 0.2           | 16.6 | 0.2           | 16.6 | ns   |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbbsp4_clkx active edge to mcbbsp4_dx valid  | Master | 0.6           | 16.6 | 0.6           | 16.6 | ns   |
|     |                 |                                                           | Slave  | 0.6           | 17.3 | 0.6           | 17.3 | ns   |

#### 6.6.1.1.5 McBSP5

Table 6-81 through Table 6-88 list the timing conditions and switching characteristics for McBSP5.

**Table 6-81. McBSP5 Timing Requirements - Rising Edge and Receive Mode**

| No. | PARAMETER       |                                                               |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------------|---------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                 |                                                               |                   | MIN           | MAX | MIN           | MAX |      |
| B3  | tsu(DRV-CLKXAE) | Setup time, mcbbsp5_dr valid before mcbbsp5_clkx active edge  | Half Cycle Master | 7.5           |     | 7.5           |     | ns   |
|     |                 |                                                               | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Master | 5.6           |     | 5.6           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 5.8           |     | 5.8           |     | ns   |
| B4  | th(CLKXAE-DRV)  | Hold time, mcbbsp5_dr valid after mcbbsp5_clkx active edge    | Half Cycle Master | 7.5           |     | 7.5           |     | ns   |
|     |                 |                                                               | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |
| B5  | tsu(FSV-CLKXAE) | Setup time, mcbbsp5_fsx valid before mcbbsp5_clkx active edge | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 5.8           |     | 5.8           |     | ns   |
| B6  | th(CLKXAE-FSV)  | Hold time, mcbbsp5_fsx valid after mcbbsp5_clkx active edge   | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 1.0           |     | 1.0           |     | ns   |

**Table 6-82. McBSP5 Switching Characteristics - Rising Edge and Receive Mode**

| No. | PARAMETER       |                                                           |  | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--|---------------|------|---------------|------|------|
|     |                 |                                                           |  | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp5_clkx active edge to mcbbsp5_fsx valid |  | 0.2           | 14.8 | 0.7           | 14.8 | ns   |

**Table 6-83. McBSP5 Timing Requirements - Rising Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbbsp5_fsx valid before mcbbsp5_clkx active edge | Half Cycle Slave | 7.7           |     | 7.7           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 5.8           |     | 5.8           |     | ns   |

**Table 6-83. McBSP5 Timing Requirements - Rising Edge and Transmit Mode (continued)**

| No. | PARAMETER       |                                                             |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------------|-------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                 |                                                             |                  | MIN           | MAX | MIN           | MAX |      |
| B6  | th(CLKXAE-FSXV) | Hold time, mcbbsp5_fsx valid after mcbbsp5_clkx active edge | Half Cycle Slave | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                             | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-84. McBSP5 Switching Characteristics - Rising Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                 |                                                           |        | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp5_clkx active edge to mcbbsp5_fsx valid |        | 0.2           | 14.8 | 0.2           | 14.8 | ns   |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbbsp5_clkx active edge to mcbbsp5_dx valid  | Master | 0.6           | 14.8 | 0.6           | 14.8 | ns   |
|     |                 |                                                           | Slave  | 0.6           | 14.8 | 0.6           | 14.8 | ns   |

**Table 6-85. McBSP5 Timing Requirements - Falling Edge and Receive Mode**

| No. | PARAMETER       |                                                               |                   | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|-----------------|---------------------------------------------------------------|-------------------|---------------|-----|---------------|-----|------|
|     |                 |                                                               |                   | MIN           | MAX | MIN           | MAX |      |
| B3  | tsu(DRV-CLKXAE) | Setup time, mcbbsp5_dr valid before mcbbsp5_clkx active edge  | Half Cycle Master | 7.5           |     | 7.5           |     | ns   |
|     |                 |                                                               | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Master | 5.6           |     | 5.6           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 5.8           |     | 5.8           |     | ns   |
| B4  | th(CLKXAE-DRV)  | Hold time, mcbbsp5_dr valid after mcbbsp5_clkx active edge    | Half Cycle Master | 8.3           |     | 8.3           |     | ns   |
|     |                 |                                                               | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Master | 1.5           |     | 1.5           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 0.9           |     | 0.9           |     | ns   |
| B5  | tsu(FXS-CLKXAE) | Setup time, mcbbsp5_fsx valid before mcbbsp5_clkx active edge | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 5.8           |     | 5.8           |     | ns   |
| B6  | th(CLKXAE-FSXV) | Hold time, mcbbsp5_fsx valid after mcbbsp5_clkx active edge   | Half Cycle Slave  | 7.7           |     | 7.7           |     | ns   |
|     |                 |                                                               | Full Cycle Slave  | 1.0           |     | 1.0           |     | ns   |

**Table 6-86. McBSP5 Switching Characteristics - Falling Edge and Receive Mode**

| No. | PARAMETER       |                                                           |  | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--|---------------|------|---------------|------|------|
|     |                 |                                                           |  | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbbsp5_clkx active edge to mcbbsp5_fsx valid |  | 0.2           | 22.2 | 0.2           | 22.2 | ns   |

**Table 6-87. McBSP5 Timing Requirements - Falling Edge and Transmit Mode**

| No. | PARAMETER        |                                                               |                  | VDDSHV = 3.3V |     | VDDSHV = 1.8V |     | UNIT |
|-----|------------------|---------------------------------------------------------------|------------------|---------------|-----|---------------|-----|------|
|     |                  |                                                               |                  | MIN           | MAX | MIN           | MAX |      |
| B5  | tsu(FSXV-CLKXAE) | Setup time, mcbasp5_fsx valid before mcbasp5_clkx active edge | Half Cycle Slave | 7.7           |     | 7.7           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 5.8           |     | 5.8           |     | ns   |
| B6  | th(CLKXAE-FSXV)  | Hold time, mcbasp5_fsx valid after mcbasp5_clkx active edge   | Half Cycle Slave | 7.7           |     | 7.7           |     | ns   |
|     |                  |                                                               | Full Cycle Slave | 1.0           |     | 1.0           |     | ns   |

**Table 6-88. McBSP5 Switching Characteristics - Falling Edge and Transmit Mode**

| No. | PARAMETER       |                                                           |        | VDDSHV = 3.3V |      | VDDSHV = 1.8V |      | UNIT |
|-----|-----------------|-----------------------------------------------------------|--------|---------------|------|---------------|------|------|
|     |                 |                                                           |        | MIN           | MAX  | MIN           | MAX  |      |
| B2  | td(CLKXAE-FSXV) | Delay time, mcbasp5_clkx active edge to mcbasp5_fsx valid |        | 0.2           | 22.2 | 0.2           | 22.2 | ns   |
| B8  | td(CLKXAE-DXV)  | Delay time, mcbasp5_clkx active edge to mcbasp5_dx valid  | Master | 0.6           | 22.2 | 0.6           | 22.2 | ns   |
|     |                 |                                                           | Slave  | 0.6           | 22.2 | 0.6           | 22.2 | ns   |

#### 6.6.1.1.6 McBSP in TDM Mode

Table 6-89 through Table 6-91 assume testing over the recommended operating conditions.

**Table 6-89. McBSP Timing Conditions – TDM in Multipoint Mode**

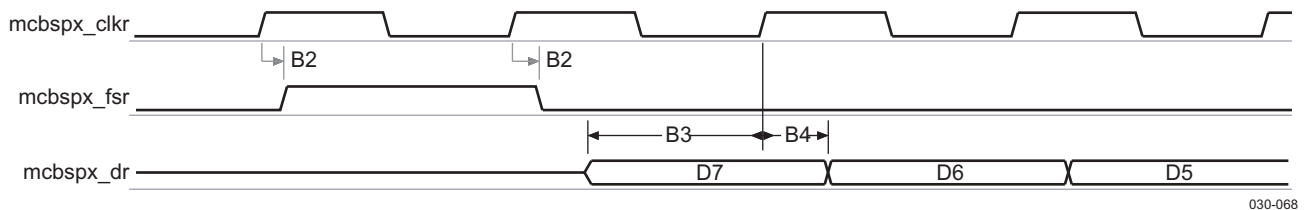
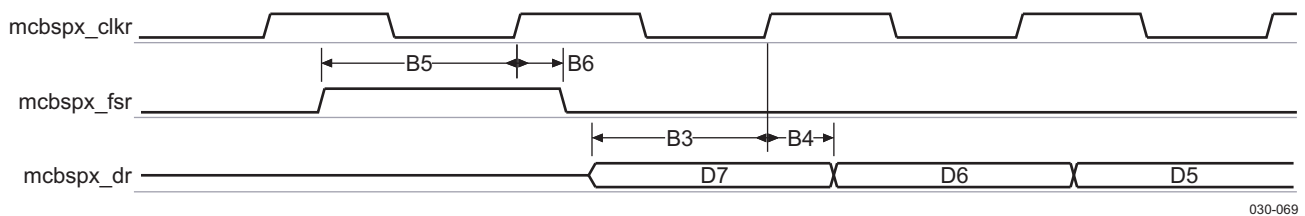
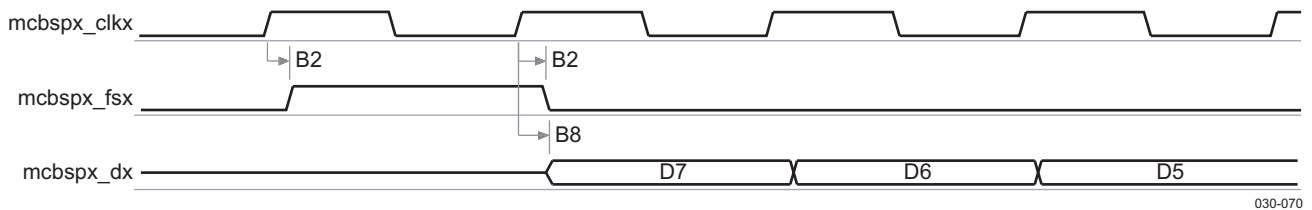
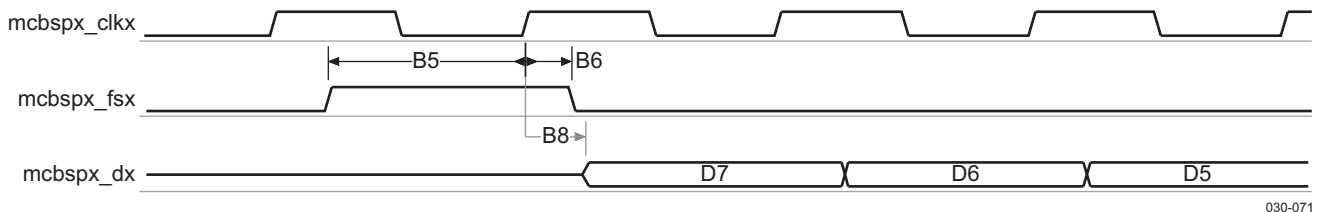
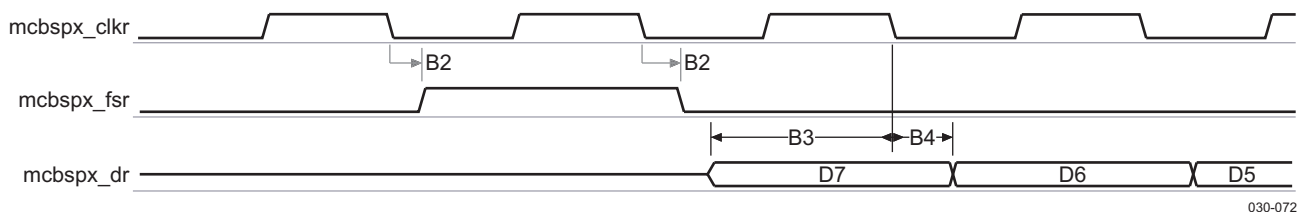
| PARAMETER | DESCRIPTION             | VDDSHV = 1.8V or 3.3V |     | UNIT |
|-----------|-------------------------|-----------------------|-----|------|
|           |                         | MIN                   | MAX |      |
| tr        | Input signal rise time  | 1                     | 8.5 | ns   |
| tf        | Input signal fall time  | 1                     | 8.5 | ns   |
| Cload     | Output load capacitance |                       | 40  | pf   |

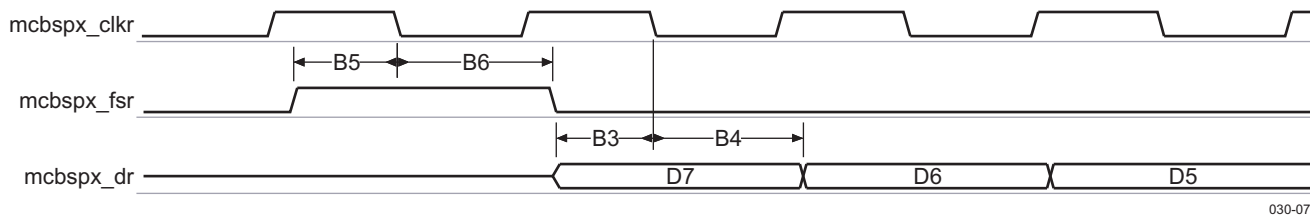
**Table 6-90. McBSP Timing Requirements — TDM in Multipoint Mode**

| INDEX | PARAMETER      | DESCRIPTION                                                   | VDDSHV = 1.8V or 3.3V |      | UNIT |
|-------|----------------|---------------------------------------------------------------|-----------------------|------|------|
|       |                |                                                               | MIN                   | MAX  |      |
|       | tw(CLKH)       | Cycle Time, mcbspcx_clkx                                      | 162.8                 |      | ns   |
|       | tw(CLKH)       | Typical Pulse duration, mcbspcx_clkx high                     | 81.4                  |      | ns   |
|       | tw(CLKL)       | Typical Pulse duration, mcbspcx_clkx low                      | 81.4                  |      | ns   |
|       | tdc(CLK)       | Duty cycle error, mcbspcx_clkx                                | -8.14                 | 8.14 | ns   |
| B3    | tsu(DRV-CLKAE) | Setup time, mcbspcx_dr valid before mcbspcx_clkx active edge  | 9                     |      | ns   |
| B4    | th(CLKAE-DRV)  | Hold time, mcbspcx_dr valid after mcbspcx_clkx active edge    | 2.4                   |      | ns   |
| B5    | tsu(FSV-CLKAE) | Setup time, mcbspcx_fsx valid before mcbspcx_clkx active edge | 9                     |      | ns   |
| B6    | th(CLKAE-FSV)  | Hold time, mcbspcx_fsx valid after mcbspcx_clkx active edge   | 2.4                   |      | ns   |

**Table 6-91. McBSP Switching Characteristics — TDM in Multipoint Mode**

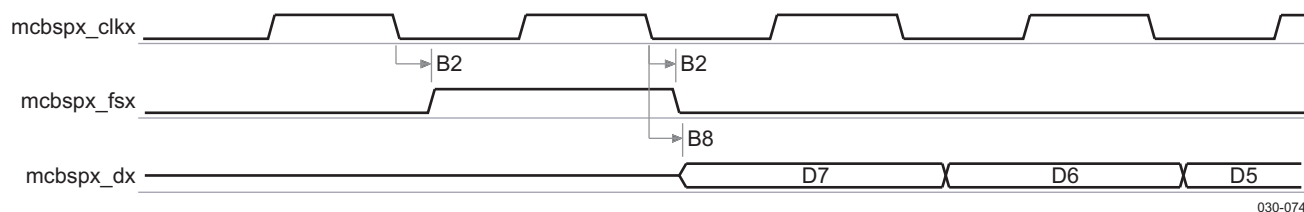
| INDEX | PARAMETER      | DESCRIPTION                                            | VDDSHV = 1.8V or 3.3V |      | UNIT |
|-------|----------------|--------------------------------------------------------|-----------------------|------|------|
|       |                |                                                        | MIN                   | MAX  |      |
| B8    | td(CLKXAE-DXV) | Delay time, mcbspx_clkx active edge to mcbspx_dx valid | 0.6                   | 16.8 | ns   |

**6.6.1.1.7 McBSP Timing Diagrams****Figure 6-37. McBSP Rising Edge Receive Timing in Master Mode****Figure 6-38. McBSP Rising Edge Receive Timing in Slave Mode****Figure 6-39. McBSP Rising Edge Transmit Timing in Master Mode****Figure 6-40. McBSP Rising Edge Transmit Timing in Slave Mode****Figure 6-41. McBSP Falling Edge Receive Timing in Master Mode**



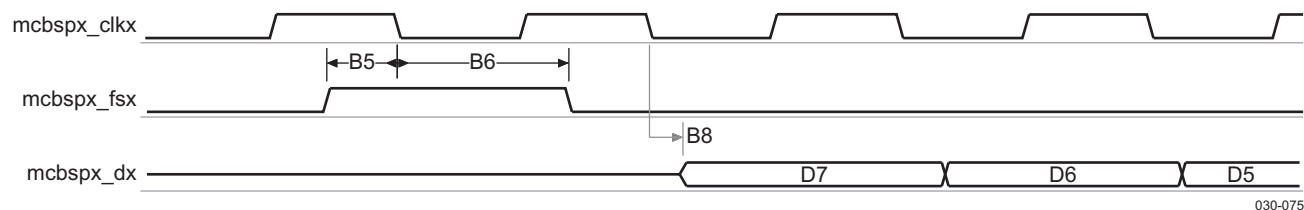
030-073

**Figure 6-42. McBSP Falling Edge Receive Timing in Slave Mode**



030-074

**Figure 6-43. McBSP Falling Edge Transmit Timing in Master Mode**



030-075

**Figure 6-44. McBSP Falling Edge Transmit Timing in Slave Mode**

## 6.6.2 Multichannel Serial Port Interface (McSPI) Timing

The multichannel SPI is a master/slave synchronous serial bus. The McSPI1 module supports up to four peripherals and the others (McSPI2, McSPI3, and McSPI4) support up to two peripherals. The following timings are applicable to the different configurations of McSPI in master/slave mode for any McSPI and any channel (n).

### 6.6.2.1 McSPI in Slave Mode

Table 6-92 and Table 6-93 assume testing over the recommended operating conditions.

**Table 6-92. McSPI Interface Timing Requirements – Slave Mode**

| NO. | PARAMETER             |                                                           | 1.8 V |       | 3.3 V |     | UNIT |
|-----|-----------------------|-----------------------------------------------------------|-------|-------|-------|-----|------|
|     |                       |                                                           | MIN   | MAX   | MIN   | MAX |      |
| SS0 | $t_{c(CLK)}$          | Cycle time, mcspx_clk                                     | 41.67 |       | 41.67 |     | ns   |
| SS1 | $t_{w(CLK)}$          | Pulse duration, mcspx_clk high or low                     | 18.75 | 22.92 | 11.25 |     | ns   |
| SS2 | $t_{su(SIMOV-CLKAE)}$ | Setup time, mcspx_simo valid before mcspx_clk active edge | 4.2   |       | 4     |     | ns   |
| SS3 | $t_{h(SIMOV-CLKAE)}$  | Hold time, mcspx_simo valid after mcspx_clk active edge   | 4.6   |       | 3     |     | ns   |
| SS4 | $t_{su(CS0V-CLKFE)}$  | Setup time, mcspx_cs0 valid before mcspx_clk first edge   | 13.8  |       | 7     |     | ns   |
| SS5 | $t_{h(CS0I-CLKLE)}$   | Hold time, mcspx_cs0 invalid after mcspx_clk last edge    | 13.8  |       | 9.17  |     | ns   |

**Table 6-93. McSPI Interface Switching Characteristics<sup>(1) (2) (3) (4)</sup>**

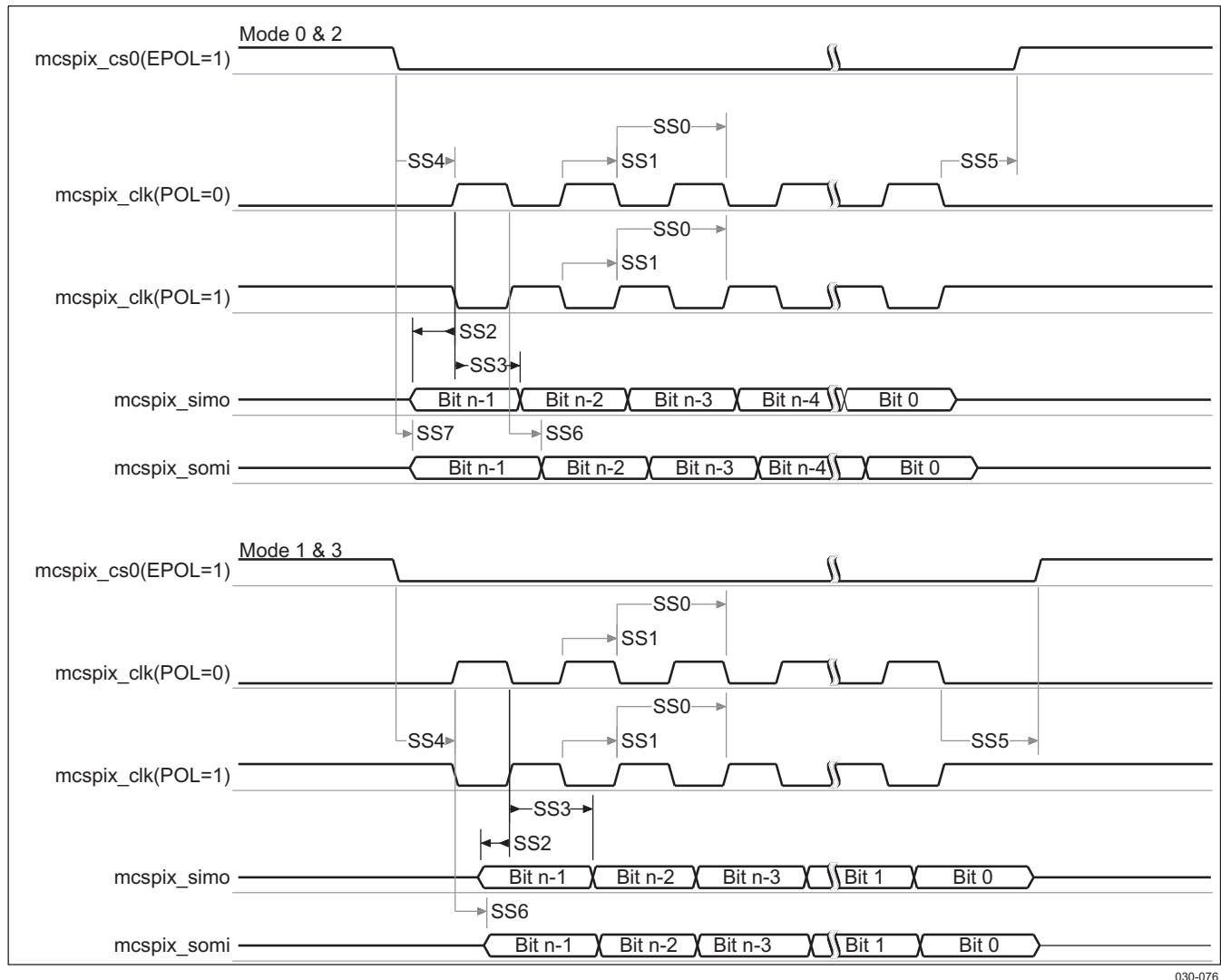
| NO. | PARAMETER          |                                                         | 1.8 V |       | 3.3 V |      | UNIT |
|-----|--------------------|---------------------------------------------------------|-------|-------|-------|------|------|
|     |                    |                                                         | MIN   | MAX   | MIN   | MAX  |      |
| SS6 | $t_d(CLKAE-SOMIV)$ | Delay time, mcspx_clk active edge to mcspx_somi shifted | 1.8   | 15.9  | 2     | 16.5 | ns   |
| SS7 | $t_d(CS0AE-SOMIV)$ | Delay time, mcspx_cs0 active edge to mcspx_somi shifted |       | 16.38 |       | 15.9 | ns   |

(1) The capacitive load is equivalent to 20 pF.

(2) In mcspx, x is equal to 1, 2, 3, or 4.

(3) The polarity of mcspx\_clk and the active edge (rising or falling) on which mcspx\_simo is driven and mcspx\_somi is latched is all software configurable.

(4) This timing applies to all configurations regardless of mcspx\_clk polarity and which clock edges are used to drive output data and capture input data.



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**Figure 6-45. McSPI Interface Transmit and Receive in Slave Mode(1) (2)**

- (1) The active clock edge (rising or falling) on which mcspx\_somi is driven and mcspx\_simo data is latched is software configurable with the bit MSPI\_CHCONFx[0] = PHA and the bit MSPI\_CHCONFx[1] = POL.
- (2) The polarity of mcspx\_csi is software configurable with the bit MSPI\_CHCONFx[6] = EPOL. In mcspx, x is equal to 1, 2, 3, or 4.

### 6.6.2.2 McSPI in Master Mode

Table 6-94 and Table 6-95 assume testing over the recommended operating conditions.

**Table 6-94. McSPI1, 2, and 4 Interface Timing Requirements – Master Mode<sup>(1) (2)</sup>**

| NO. | PARAMETER             |                                                           | 1.8 V |     | 3.3 V |     | UNIT |
|-----|-----------------------|-----------------------------------------------------------|-------|-----|-------|-----|------|
|     |                       |                                                           | MIN   | MAX | MIN   | MAX |      |
| SM2 | $t_{su}(SOMIV-CLKAE)$ | Setup time, mcspx_somi valid before mcspx_clk active edge | 2.56  |     | 4     |     | ns   |
| SM3 | $t_h(SOMIV-CLKAE)$    | Hold time, mcspx_somi valid after mcspx_clk active edge   | 2.93  |     | 4     |     | ns   |

- (1) The input timing requirements are given by considering a rise time and a fall time of 4 ns.
- (2) In mcspx, x is equal to 1, 2, 3, or 4. In mcspx\_csn, n is equal to 0, 1, 2, or 3 for x equal to 1, n is equal to 0 or 1 for x equal to 2 and 3. n is equal to 0 for x equal to 4.

**Table 6-95. McSPI1, 2, and 4 Interface Switching Characteristics – Master Mode<sup>(1) (2) (3)</sup>**

| NO. | PARAMETER            |                                                           | 1.8 V                |                        | 3.3 V                  |                      | UNIT |
|-----|----------------------|-----------------------------------------------------------|----------------------|------------------------|------------------------|----------------------|------|
|     |                      |                                                           | MIN                  | MAX                    | MIN                    | MAX                  |      |
| SM0 | $t_{c(CLK)}$         | Cycle time, mcspix_clk                                    | 20.83                |                        | 20.83                  |                      | ns   |
|     | $t_{j(CLK)}$         | Cycle jitter <sup>(4)</sup> , mcspix_clk                  | -200                 | 200                    | -200                   | 200                  | ps   |
| SM1 | $t_{w(CLK)}$         | Pulse duration, mcspix_clk high or low                    | 0.45P <sup>(5)</sup> | 0.55P <sup>(5)</sup>   | 0.45P <sup>(5)</sup>   | 0.55P <sup>(5)</sup> | ns   |
| SM4 | $t_{d(CLKAE-SIMOV)}$ | Delay time, mcspix_clk active edge to mcspix_simo shifted | -2.1                 | 5                      | -3                     | 6                    | ns   |
| SM5 | $t_{d(CSnA-CLKFE)}$  | Delay time, mcspix_csi active to mcspix_clk first edge    | Modes 1 and 3        | A <sup>(6)</sup> - 3.2 | A <sup>(6)</sup> - 3.0 | 6                    | ns   |
|     |                      |                                                           | Modes 0 and 2        | B <sup>(7)</sup> - 3.2 | B <sup>(7)</sup> - 3.0 | 6                    | ns   |
| SM6 | $t_{d(CLKLE-CSnI)}$  | Delay time, mcspix_clk last edge to mcspix_csi inactive   | Modes 1 and 3        | B <sup>(7)</sup> - 3.2 | B <sup>(7)</sup> - 3.0 |                      | ns   |
|     |                      |                                                           | Modes 0 and 2        | A <sup>(6)</sup> - 3.2 | A <sup>(6)</sup> - 3.0 |                      | ns   |
| SM7 | $t_{d(CSnAE-SIMOV)}$ | Delay time, mcspix_csi active edge to mcspix_simo shifted | Modes 0 and 2        |                        | 5                      | 5                    | ns   |

- (1) Timings are given for a maximum load capacitance of 20 pF for spix\_csn signals, 30 pF for spix\_clk and spix\_simo signals with x = 1 or 2, and 20 pF for spi4\_clk and spi4\_simo signals.
- (2) In mcspix, x is equal to 1, 2, 3, or 4. In mcspix\_csn, n is equal to 0, 1, 2, or 3 for x equal to 1, n is equal to 0 or 1 for x equal to 2 and 3. n is equal to 0 for x equal to 4.
- (3) The polarity of mcspix\_clk and the active edge (rising or falling) on which mcspix\_simo is driven and mcspix\_somi is latched is all software configurable.
- (4) Maximum cycle jitter supported by mcspix\_clk input clock.
- (5) P = mcspix\_clk clock period
- (6) Case P = 20.8 ns, A = (TCS+0.5)\*P (TCS is a bit field of MSPI\_CHCONFx[26:25] register). Case P > 20.8 ns, A = TCS\*P (TCS is a bitfield of MSPI\_CHCONFx[26:25] register). For more information, see the *Device Multichannel Serial Port Interface (McSPI) Reference Guide* [SPRUUFV6].
- (7) B = TCS\*P (TCS is a bit field of MSPI\_CHCONFx[26:25] register). For more information, see the *Device Multichannel Serial Port Interface (McSPI) Reference Guide* [SPRUUFV6].

Table 6-96 and Table 6-97 assume testing over the recommended operating conditions.

**Table 6-96. McSPI 3 Interface Timing Requirements – Master Mode<sup>(1) (2)</sup>**

| NO. | PARAMETER             |                                                             | 1.8 V |     | 3.3 V |     | UNIT |
|-----|-----------------------|-------------------------------------------------------------|-------|-----|-------|-----|------|
|     |                       |                                                             | MIN   | MAX | MIN   | MAX |      |
| SM2 | $t_{su(SOMIV-CLKAE)}$ | Setup time, mcspi3_somi valid before mcspi3_clk active edge | 2.5   |     | 4     |     | ns   |
| SM3 | $t_{h(SOMIV-CLKAE)}$  | Hold time, mcspi3_somi valid after mcspi3_clk active edge   | 2.89  |     | 4     |     | ns   |

- (1) The input timing requirements are given by considering a rise time and a fall time of 4 ns.
- (2) In mcspi3\_csn, n is equal to 0 or 1. The polarity of mcspi3\_clk and the active edge (rising or falling) on which mcspi3\_simo is driven and mcspi3\_somi is latched is all software configurable.

**Table 6-97. McSPI3 Interface Switching Characteristics – Master Mode<sup>(1) (2) (3)</sup>**

| NO. | PARAMETER                    |                                                           |               | 1.8 V                  |                      | 3.3 V                  |                      | UNIT |
|-----|------------------------------|-----------------------------------------------------------|---------------|------------------------|----------------------|------------------------|----------------------|------|
|     |                              |                                                           |               | MIN                    | MAX                  | MIN                    | MAX                  |      |
| SM0 | t <sub>c</sub> (CLK)         | Cycle time, mcspix_clk                                    |               | 41.67                  |                      | 41.67                  |                      | ns   |
|     | t <sub>j</sub> (CLK)         | Cycle jitter <sup>(4)</sup>                               |               | -200                   | 200                  | -200                   | 200                  | ps   |
| SM1 | t <sub>w</sub> (CLK)         | Pulse duration, mcspix_clk high or low                    |               | 0.45P <sup>(5)</sup>   | 0.55P <sup>(5)</sup> | 0.45P <sup>(5)</sup>   | 0.55P <sup>(5)</sup> | ns   |
| SM4 | t <sub>d</sub> (CLKAE-SIMOV) | Delay time, mcspix_clk active edge to mcspix_simo shifted |               | -2.1                   | 11.3                 | -3                     |                      | ns   |
| SM5 | t <sub>d</sub> (CSnA-CLKFE)  | Delay time, mcspix_csi active to mcspix_clk first edge    | Modes 1 and 3 | A <sup>(6)</sup> - 4.4 |                      | A <sup>(6)</sup> - 3.0 | 6                    | ns   |
|     |                              |                                                           | Modes 0 and 2 | B <sup>(7)</sup> - 4.4 |                      | B <sup>(7)</sup> - 3.0 | 6                    | ns   |
| SM6 | t <sub>d</sub> (CLKLE-CSnI)  | Delay time, mcspix_clk last edge to mcspix_csi inactive   | Modes 1 and 3 | B <sup>(7)</sup> - 4.4 |                      | B <sup>(7)</sup> - 3.0 |                      | ns   |
|     |                              |                                                           | Modes 0 and 2 | A <sup>(6)</sup> - 4.4 |                      | A <sup>(6)</sup> - 3.0 |                      | ns   |
| SM7 | t <sub>d</sub> (CSnAE-SIMOV) | Delay time, mcspix_csi active edge to mcspix_simo shifted | Modes 0 and 2 |                        | 11.3                 |                        | 5                    | ns   |

(1) The capacitive load is equivalent to 20 pF.

(2) In mcspi3\_csn, n is equal to 0 or 1. The polarity of mcspi3\_clk and the active edge (rising or falling) on which mcspi3\_simo is driven and mcspi3\_somi is latched are all software configurable.

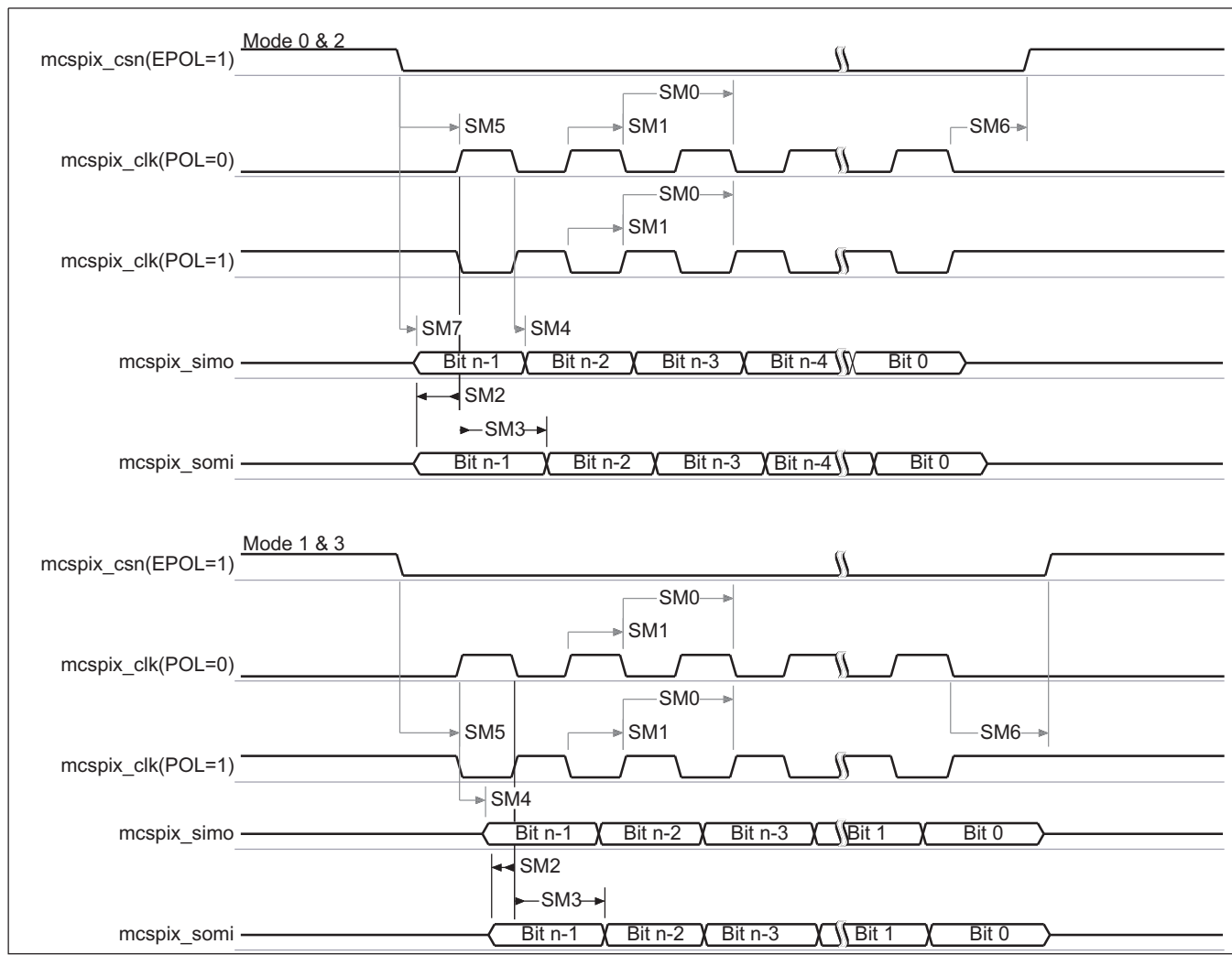
(3) This timing applies to all configurations regardless of McSPI3\_CLK polarity and which clock edges are used to drive output data and capture input data.

(4) Maximum cycle jitter supported by mcspix\_clk input clock.

(5)  $P$  = mcspix\_clk clock period.

(6) Case  $P = 20.8$  ns,  $A = (TCS + 0.5) * P$  (TCS is a bit field of MSPI\_CHCONFx[26:25] register). Case  $P > 20.8$  ns,  $A = TCS * P$  (TCS is a bit field of MSPI\_CHCONFx[26:25] register). For more information, see the *Device Multichannel Serial Port Interface (McSPI) Reference Guide* [SPRUFG6].

(7)  $B = TCS * P$  (TCS is a bit field of MSPI\_CHCONFx[26:25] register). For more information, see the *Device Multichannel Serial Port Interface (McSPI) Reference Guide* [SPRUFG6].



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**Figure 6-46. McSPI Interface Transmit and Receive in Master Mode(1) (2) (3)**

- (1) The active clock edge (rising or falling) on which mcspx\_simo is driven and mcspx\_somi data is latched is software configurable with the bit MSPI\_CHCONFx[0] = PHA and the bit MSPI\_CHCONFx[1] = POL.
- (2) The polarity of mcspx\_csi is software configurable with the bit MSPI\_CHCONFx[6] = EPOL.
- (3) In mcspx, x is equal to 1. In mcspx\_csn, n is equal to 0, 1, 2, or 3.

### 6.6.3 Multiport Full-Speed Universal Serial Bus (USB) Interface

The AM3517/05 microprocessor provides three USB ports working in full- and low-speed data transactions (up to 12Mbit/s).

Connected to either a serial link controller or a serial PHY (PHY interface modes) it supports:

- 6-pin (Tx: Dat/Se0 or Tx: Dp/Dm) unidirectional mode
- 4-pin bidirectional mode
- 3-pin bidirectional mode

#### 6.6.3.1 Multiport Full-Speed Universal Serial Bus (USB) – Unidirectional Standard 6-pin Mode

Table 6-98 through Table 6-100 assume testing over the recommended operating conditions.

**Table 6-98. Low-/Full-Speed USB Timing Conditions Unidirectional Standard 6-pin Mode**

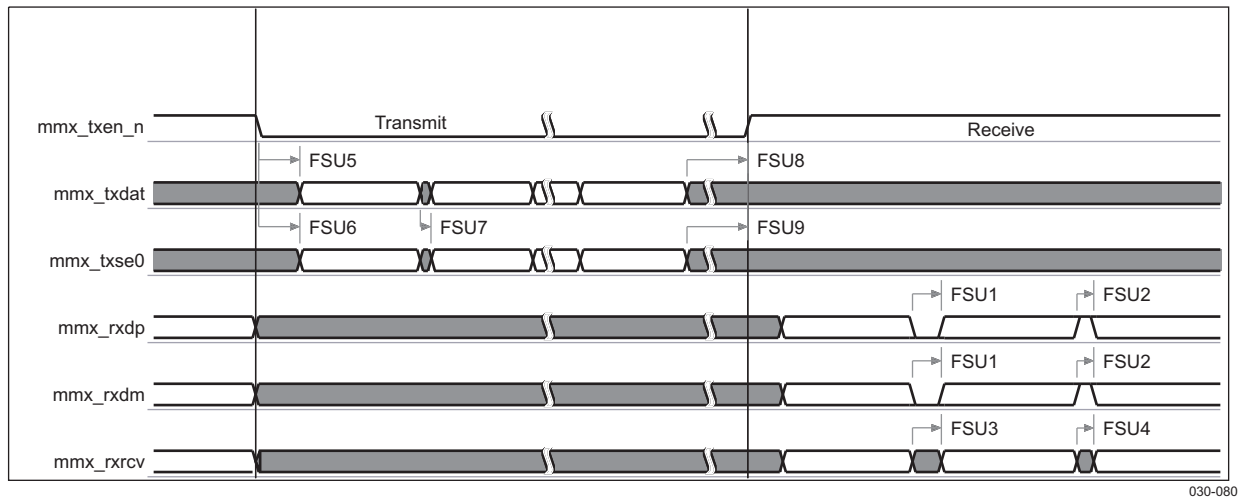
| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V | UNIT |
|----------------------------|-------------------------|------------|------|
| <b>Input Conditions</b>    |                         |            |      |
| $t_R$                      | Input signal rise time  | 2.0        | ns   |
| $t_F$                      | Input signal fall time  | 2.0        | ns   |
| <b>Output Conditions</b>   |                         |            |      |
| $C_{LOAD}$                 | Output load capacitance | 15.0       | pF   |

**Table 6-99. Low-/Full-Speed USB Timing Requirements Unidirectional Standard 6-pin Mode**

| NO.  | PARAMETER       |                                                                                              | 1.8V, 3.3V |      | UNIT |
|------|-----------------|----------------------------------------------------------------------------------------------|------------|------|------|
|      |                 |                                                                                              | MIN        | MAX  |      |
| FSU1 | $t_d(V_p, V_m)$ | Time duration, mmx_rxdp and mmx_rxdm low together during transition                          |            | 14.0 | ns   |
| FSU2 | $t_d(V_p, V_m)$ | Time duration, mmx_rxdp and mmx_rxdm high together during transition                         |            | 8.0  | ns   |
| FSU3 | $t_d(RCVU0)$    | Time duration, mmx_rxcv undefine during a single end 0 (mmx_rxdp and mmx_rxdm low together)  |            | 14.0 | ns   |
| FSU4 | $t_d(RCVU1)$    | Time duration, mmx_rxcv undefine during a single end 1 (mmx_rxdp and mmx_rxdm high together) |            | 8.0  | ns   |

**Table 6-100. Low-/Full-Speed USB Switching Characteristics Unidirectional Standard 6-pin Mode**

| NO.  | PARAMETER         |                                                  | 1.8V, 3.3V |      | UNIT |
|------|-------------------|--------------------------------------------------|------------|------|------|
|      |                   |                                                  | MIN        | MAX  |      |
| FSU5 | $t_d(TXENL-DATV)$ | Delay time, mmx_txen_n low to mmx_txdat valid    | 81.8       | 84.8 | ns   |
| FSU6 | $t_d(TXENL-SE0V)$ | Delay time, mmx_txen_n low to mmx_txse0 valid    | 81.8       | 84.8 | ns   |
| FSU7 | $t_s(DAT-SE0)$    | Skew between mmx_txdat and mmx_txse0 transition  |            | 1.5  | ns   |
| FSU8 | $t_d(DATI-TXENH)$ | Delay time, mmx_txdat invalid to mmx_txen_n high | 81.8       |      | ns   |
| FSU9 | $t_d(SE0I-TXENH)$ | Delay time, mmx_txse0 invalid to mmx_txen_n high | 81.8       |      | ns   |
|      | $t_R(do)$         | Rise time, mmx_txen_n                            |            | 4.0  | ns   |
|      | $t_F(do)$         | Fall time, mmx_txen_n                            |            | 4.0  | ns   |
|      | $t_R(do)$         | Rise time, mmx_txdat                             |            | 4.0  | ns   |
|      | $t_F(do)$         | Fall time, mmx_txdat                             |            | 4.0  | ns   |
|      | $t_R(do)$         | Rise time, mmx_txse0                             |            | 4.0  | ns   |
|      | $t_F(do)$         | Fall time, mmx_txse0                             |            | 4.0  | ns   |



In mmx, x is equal to 0, 1, or 2.

**Figure 6-47. Low-/Full-Speed USB Unidirectional Standard 6-pin Mode**

### 6.6.3.2 Multiport Full-Speed Universal Serial Bus (USB) – Bidirectional Standard 4-pin Mode

Table 6-101 through Table 6-103 assume testing over the recommended operating conditions.

**Table 6-101. Low-/Full-Speed USB Timing Conditions Bidirectional Standard 4-pin Mode**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V | UNIT |
|----------------------------|-------------------------|------------|------|
| <b>Input Conditions</b>    |                         |            |      |
| $t_R$                      | Input signal rise time  | 2.0        | ns   |
| $t_F$                      | Input signal fall time  | 2.0        | ns   |
| <b>Output Conditions</b>   |                         |            |      |
| $C_{LOAD}$                 | Output load capacitance | 15.0       | pF   |

**Table 6-102. Low-/Full-Speed USB Timing Requirements Bidirectional Standard 4-pin Mode**

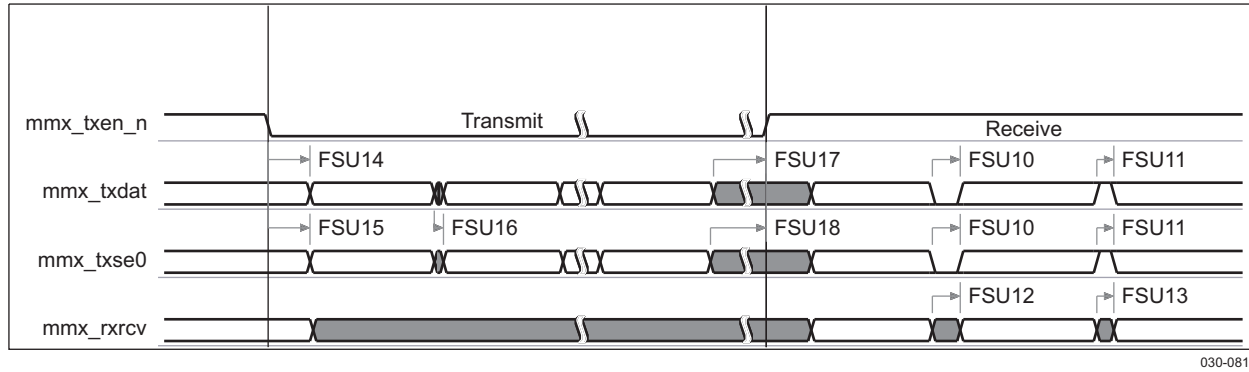
| NO.   | PARAMETER        |                                                                                                | 1.8V, 3.3V |      | UNIT |
|-------|------------------|------------------------------------------------------------------------------------------------|------------|------|------|
|       |                  |                                                                                                | MIN        | MAX  |      |
| FSU10 | $t_{d(DAT,SE0)}$ | Time duration, mmx_txdat and mmx_txse0 low together during transition                          |            | 14.0 | ns   |
| FSU11 | $t_{d(DAT,SE0)}$ | Time duration, mmx_txdat and mmx_txse0 high together during transition                         |            | 8.0  | ns   |
| FSU12 | $t_{d(RCVU0)}$   | Time duration, mmx_rxcv undefine during a single end 0 (mmx_txdat and mmx_txse0 low together)  |            | 14.0 | ns   |
| FSU13 | $t_{d(RCVU1)}$   | Time duration, mmx_rxcv undefine during a single end 1 (mmx_txdat and mmx_txse0 high together) |            | 8.0  | ns   |

**Table 6-103. Low-/Full-Speed USB Switching Characteristics Bidirectional Standard 4-pin Mode**

| NO.   | PARAMETER           |                                                      | 1.8V, 3.3V |      | UNIT |
|-------|---------------------|------------------------------------------------------|------------|------|------|
|       |                     |                                                      | MIN        | MAX  |      |
| FSU14 | $t_{d(TXENL-DATV)}$ | Delay time, mmx_txen_n low to mmx_txdat valid        | 81.8       | 84.8 | ns   |
| FSU15 | $t_{d(TXENL-SE0V)}$ | Delay time, mmx_txen_n low to mmx_txse0 valid        | 81.8       | 84.8 | ns   |
| FSU16 | $t_s(DAT-SE0)$      | Skew between mmx_txdat and mmx_txse0 transition      |            | 1.5  | ns   |
| FSU17 | $t_{d(DATV-TXENH)}$ | Delay time, mmx_txdat invalid before mmx_txen_n high | 81.8       |      | ns   |
| FSU18 | $t_{d(SE0V-TXENH)}$ | Delay time, mmx_txse0 invalid before mmx_txen_n high | 81.8       |      | ns   |
|       | $t_R(txen)$         | Rise time, mmx_txen_n                                |            | 4.0  | ns   |

**Table 6-103. Low-/Full-Speed USB Switching Characteristics Bidirectional Standard 4-pin Mode (continued)**

| NO. | PARAMETER     |                       | 1.8V, 3.3V |     | UNIT |
|-----|---------------|-----------------------|------------|-----|------|
|     |               |                       | MIN        | MAX |      |
|     | $t_{F(txen)}$ | Fall time, mmx_txen_n |            | 4.0 | ns   |
|     | $t_{R(dat)}$  | Rise time, mmx_txdat  |            | 4.0 | ns   |
|     | $t_{F(dat)}$  | Fall time, mmx_txdat  |            | 4.0 | ns   |
|     | $t_{R(se0)}$  | Rise time, mmx_txse0  |            | 4.0 | ns   |
|     | $t_{F(se0)}$  | Fall time, mmx_txse0  |            | 4.0 | ns   |



In mmx, x is equal to 0, 1, or 2.

**Figure 6-48. Low-/Full-Speed USB Bidirectional Standard 4-pin Mode**

### 6.6.3.3 Multiport Full-Speed Universal Serial Bus (USB) – Bidirectional Standard 3-pin Mode

Table 6-104 through Table 6-106 assume testing over the recommended operating conditions.

**Table 6-104. Low-/Full-Speed USB Timing Conditions Bidirectional Standard 3-pin Mode**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V | UNIT |
|----------------------------|-------------------------|------------|------|
| <b>Input Conditions</b>    |                         |            |      |
| $t_R$                      | Input signal rise time  | 2.0        | ns   |
| $t_F$                      | Input signal fall time  | 2.0        | ns   |
| <b>Output Conditions</b>   |                         |            |      |
| $C_{LOAD}$                 | Output load capacitance | 15.0       | pF   |

**Table 6-105. Low-/Full-Speed USB Timing Requirements Bidirectional Standard 3-pin Mode**

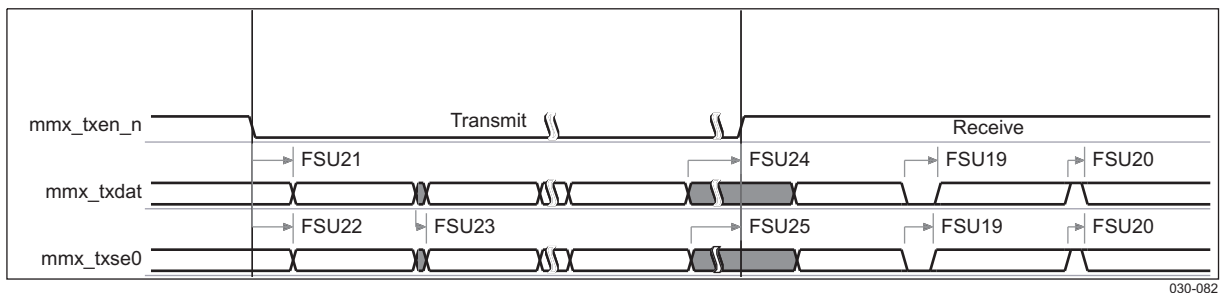
| NO.   | PARAMETER        |                                                                        | 1.8V, 3.3V |      | UNIT |
|-------|------------------|------------------------------------------------------------------------|------------|------|------|
|       |                  |                                                                        | MIN        | MAX  |      |
| FSU19 | $t_{d(DAT,SE0)}$ | Time duration, mmx_txdat and mmx_txse0 low together during transition  |            | 14.0 | ns   |
| FSU20 | $t_{d(DAT,SE0)}$ | Time duration, mmx_txdat and mmx_txse0 high together during transition |            | 8.0  | ns   |

**Table 6-106. Low-/Full-Speed USB Switching Characteristics Bidirectional Standard 3-pin Mode**

| NO.   | PARAMETER           |                                                 | 1.8V, 3.3V |      | UNIT |
|-------|---------------------|-------------------------------------------------|------------|------|------|
|       |                     |                                                 | MIN        | MAX  |      |
| FSU21 | $t_{d(TXENL-DATV)}$ | Delay time, mmx_txen_n low to mmx_txdat valid   | 81.8       | 84.8 | ns   |
| FSU22 | $t_{d(TXENL-SE0V)}$ | Delay time, mmx_txen_n low to mmx_txse0 valid   | 81.8       | 84.8 | ns   |
| FSU23 | $t_{s(DAT-SE0)}$    | Skew between mmx_txdat and mmx_txse0 transition |            | 1.5  | ns   |

**Table 6-106. Low-/Full-Speed USB Switching Characteristics Bidirectional Standard 3-pin Mode (continued)**

| NO.   | PARAMETER           |                                                  | 1.8V, 3.3V |     | UNIT |
|-------|---------------------|--------------------------------------------------|------------|-----|------|
|       |                     |                                                  | MIN        | MAX |      |
| FSU24 | $t_{d(DATI-TXENH)}$ | Delay time, mmx_txdat invalid to mmx_txen_n high | 81.8       |     | ns   |
| FSU25 | $t_{d(SE0I-TXENH)}$ | Delay time, mmx_txse0 invalid to mmx_txen_n high | 81.8       |     | ns   |
|       | $t_{R(do)}$         | Rise time, mmx_txen_n                            |            | 4.0 | ns   |
|       | $t_{F(do)}$         | Fall time, mmx_txen_n                            |            | 4.0 | ns   |
|       | $t_{R(do)}$         | Rise time, mmx_txdat                             |            | 4.0 | ns   |
|       | $t_{F(do)}$         | Fall time, mmx_txdat                             |            | 4.0 | ns   |
|       | $t_{R(do)}$         | Rise time, mmx_txse0                             |            | 4.0 | ns   |
|       | $t_{F(do)}$         | Fall time, mmx_txse0                             |            | 4.0 | ns   |



In mmx, x is equal to 0, 1, or 2.

**Figure 6-49. Low-/Full-Speed USB Bidirectional Standard 3-pin Mode**

### 6.6.4 Multiport High-Speed Universal Serial Bus (USB) Timing

In addition to the full-speed USB controller, a high-speed (HS) USB controller is instantiated inside the AM3517/05. It allows high-speed transactions (up to 480 Mbit/s) on the USB ports 1 and 2.

- Port 1 and port 2:
  - 12-bit master mode (SDR)

#### 6.6.4.1 High-Speed Universal Serial Bus (USB) on Ports 1 and 2 12-bit Master Mode

Table 6-107 through Table 6-109 assume testing over the recommended operating conditions.

**Table 6-107. High-Speed USB Timing Conditions 12-bit Master Mode**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V | UNIT |
|----------------------------|-------------------------|------------|------|
| <b>Input Conditions</b>    |                         |            |      |
| $t_R$                      | Input signal rise time  | 2          | ns   |
| $t_F$                      | Input signal fall time  | 2          | ns   |
| <b>Output Conditions</b>   |                         |            |      |
| $C_{LOAD}$                 | Output load capacitance | 3          | pF   |

**Table 6-108. High-Speed USB Timing Requirements 12-bit Master Mode<sup>(1)</sup>**

| NO.  | PARAMETER           |                                                          | 1.8V, 3.3V |     | UNIT |
|------|---------------------|----------------------------------------------------------|------------|-----|------|
|      |                     |                                                          | MIN        | MAX |      |
| HSU3 | $t_{s(DIRV-CLKH)}$  | Setup time, hsubx_dir valid before hsubx_clk rising edge | 7.5        |     | ns   |
|      | $t_{s(NXTV-CLKH)}$  | Setup time, hsubx_nxt valid before hsubx_clk rising edge | 7.5        |     | ns   |
| HSU4 | $t_{h(CLKH-DIRIV)}$ | Hold time, hsubx_dir valid after hsubx_clk rising edge   | 0.2        |     | ns   |

(1) In hsubx, x is equal to 1 or 2.

**Table 6-108. High-Speed USB Timing Requirements 12-bit Master Mode<sup>(1)</sup> (continued)**

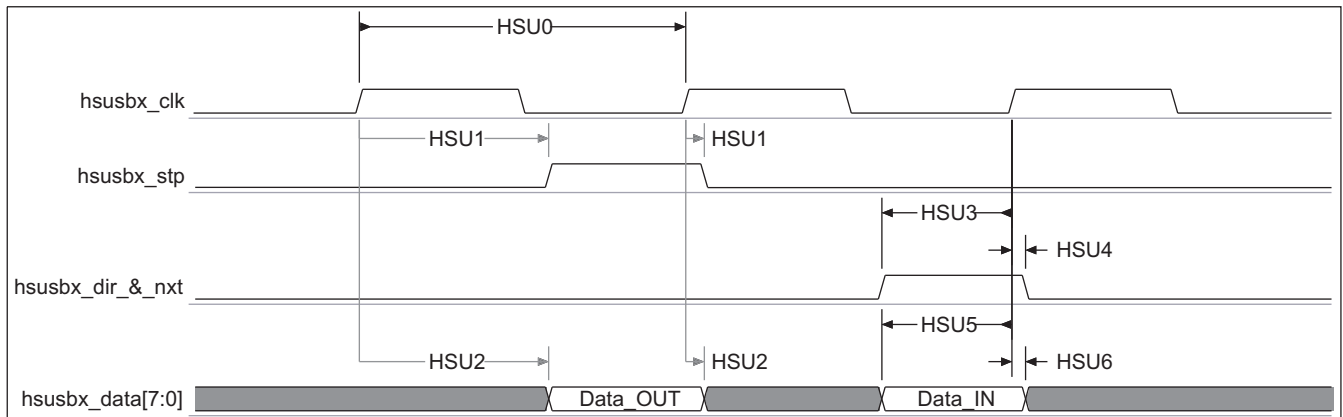
| NO.  | PARAMETER            |                                                                | 1.8V, 3.3V |     | UNIT |
|------|----------------------|----------------------------------------------------------------|------------|-----|------|
|      |                      |                                                                | MIN        | MAX |      |
|      | $t_{h(CLKH-NXT/IV)}$ | Hold time, hsubx_nxt valid after hsubx_clk rising edge         | 0.2        |     | ns   |
| HSU5 | $t_{s(DATAV-CLKH)}$  | Setup time, hsubx_data[0:7] valid before hsubx_clk rising edge | 7.5        |     | ns   |
| HSU6 | $t_{h(CLKH-DATIV)}$  | Hold time, hsubx_data[0:7] valid after hsubx_clk rising edge   | 0.2        |     | ns   |

**Table 6-109. High-Speed USB Switching Characteristics 12-bit Master Mode<sup>(1)</sup>**

| N O. | PARAMETER           |                                                              | 1.8V, 3.3V |     | UNIT |
|------|---------------------|--------------------------------------------------------------|------------|-----|------|
|      |                     |                                                              | MIN        | MAX |      |
| HSU0 | $f_{p(CLK)}$        | hsubx_clk clock frequency                                    |            | 60  | MHz  |
|      | $t_{j(CLK)}$        | Jitter standard deviation <sup>(2)</sup> , hsubx_clk         |            | 200 | ps   |
| HSU1 | $t_{d(CLKH-STPV)}$  | Delay time, hsubx_clk high to output hsubx_stp valid         |            | 13  | ns   |
|      | $t_{d(CLKH-STPIV)}$ | Delay time, hsubx_clk high to output hsubx_stp invalid       | 2          |     | ns   |
| HSU2 | $t_{d(CLKH-DV)}$    | Delay time, hsubx_clk high to output hsubx_data[0:7] valid   |            | 13  | ns   |
|      | $t_{d(CLKH-DIV)}$   | Delay time, hsubx_clk high to output hsubx_data[0:7] invalid | 2          |     | ns   |
|      | $t_{R(do)}$         | Rise time, output signals                                    |            | 2   | ns   |
|      | $t_{F(do)}$         | Fall time, output signals                                    |            | 2   | ns   |

(1) In hsubx, x is equal to 1 or 2.

(2) The jitter probability density can be approximated by a Gaussian function.



030-087

In hsubx, x is equal to 1 or 2.

**Figure 6-50. High-Speed USB 12-bit Master Mode**

### 6.6.5 USB0 OTG (USB2.0 OTG)

The AM3517/05 USB2.0 peripheral supports the following features:

- USB 2.0 peripheral at speeds high speed (HS: 480 Mb/s) and full speed (FS: 12 Mb/s)
- USB 2.0 host at speeds HS, FS, and low speed (LS: 1.5 Mb/s)
- All transfer modes (control, bulk, interrupt, and isochronous)
- 16 Transmit (TX) and 16 Receive (RX) endpoints in addition to endpoint 0
- FIFO RAM
  - 32K endpoint
  - Programmable size
- Integrated USB 2.0 High Speed PHY
- Connects to a standard Charge Pump for VBUS 5 V generation
- RNDIS mode for accelerating RNDIS type protocols using short packet termination over USB

#### 6.6.5.1 USB OTG Electrical Parameters

The USB OTG electrical parameters meet or exceed those specified in the following documents which can be obtained from the USB Implementers Forum:

- *Universal Serial Bus Specification, Revision 2.0, April 27, 2000*
- *On-The-Go Supplement to the USB 2.0 Specification, Revision 1.3, December 5, 2006*
- *Engineering Change Notice “Pull-up/pull-down resistors”, Universal Serial Bus Specification Revision 2.0*

For additional information related to USB OTG electrical parameters, please see the respective documents on the USB Implementers Forum web site (<http://www.usb.org>).

### 6.6.6 High-End Controller Area Network Controller (HECC) Timing

The AM3517/05 device has a High-End Controller Area Network Controller (HECC). The HECC uses established protocol to communicate serially with other controllers in harsh environments. The HECC is fully compliant with the Controller Area Network (CAN) protocol, version 2.0B.

Key features of the HECC include the following:

- CAN, version 2.0B compliant
- 32 RX/TX message objects
- 32 receive identifier masks
- Programmable wake-up on bus activity
- Programmable interrupt scheme
- Automatic reply to a remote request
- Automatic re-transmission in case of error or loss of arbitration
- Protection against reception of a new message
- 32-bit time stamp
- Local network time counter
- Programmable priority register for each message
- Programmable transmission and reception time-out
- HECC/SCC mode of operation
- Standard-Extended Identifier
- Self-test mode

#### 6.6.6.1 HECC Timing Requirements

Table 6-110. Timing Requirements for HECC Receive (see Figure 6-51)

| NO. |                                                           | 1.8 V, 3.3 V       |                    | UNIT |
|-----|-----------------------------------------------------------|--------------------|--------------------|------|
|     |                                                           | MIN                | MAX                |      |
| 1   | $f_{(\text{baud})}$ Maximum programmable baud rate        |                    | 1                  | Mbps |
| 2   | $t_{w(\text{HECC\_RX})}$ Pulse duration, receive data bit | H-1 <sup>(1)</sup> | H+3 <sup>(1)</sup> | ns   |

(1) These values are relative to H (where H = 1/(baud rate)).

#### 6.6.6.2 HECC Switching Characteristics

Table 6-111. Switching Characteristics Over Recommended Operating Conditions for HECC Transmit (see Figure 6-51)

| NO. | PARAMETER                                                  | 1.8 V, 3.3 V       |                    | UNIT |
|-----|------------------------------------------------------------|--------------------|--------------------|------|
|     |                                                            | MIN                | MAX                |      |
| 3   | $f_{(\text{baud})}$ Maximum programmable baud rate         |                    | 1                  | Mbps |
| 4   | $t_{w(\text{HECC\_TX})}$ Pulse duration, transmit data bit | H-1 <sup>(1)</sup> | H+3 <sup>(1)</sup> | ns   |

(1) These values are relative to H (where H = 1/(baud rate)).

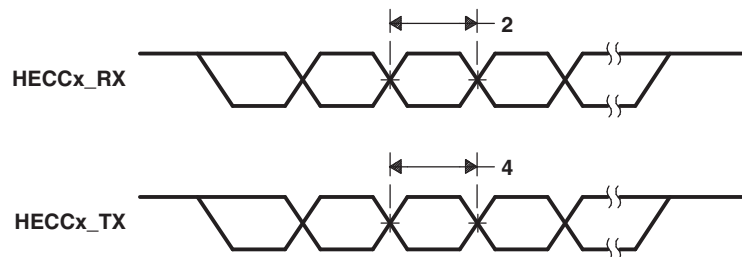


Figure 6-51. HECC Transmit/Receive Timing

### 6.6.7 Ethernet Media Access Controller (EMAC)

The Ethernet Media Access Controller (EMAC) provides an efficient interface between the AM3517/05 and the network. The EMAC supports both 10Base-T and 100Base-TX, or 10 Mbits/second (Mbps) and 100 Mbps in either half- or full-duplex mode, with hardware flow control and quality of service (QOS) support.

The EMAC controls the flow of packet data from the AM3517/05 device to the PHY. The MDIO module controls PHY configuration and status monitoring.

Both the EMAC and the MDIO modules interface to the AM3517/05 device through a custom interface that allows efficient data transmission and reception. This custom interface is referred to as the EMAC control module, and is considered integral to the EMAC/MDIO peripheral. The control module is also used to multiplex and control interrupts.

#### 6.6.7.1 EMAC Electrical Data/ Timing

Table 6-112 through Table 6-114 assume testing over the recommended operating conditions.

**Table 6-112. RMII Input Timing Requirements**

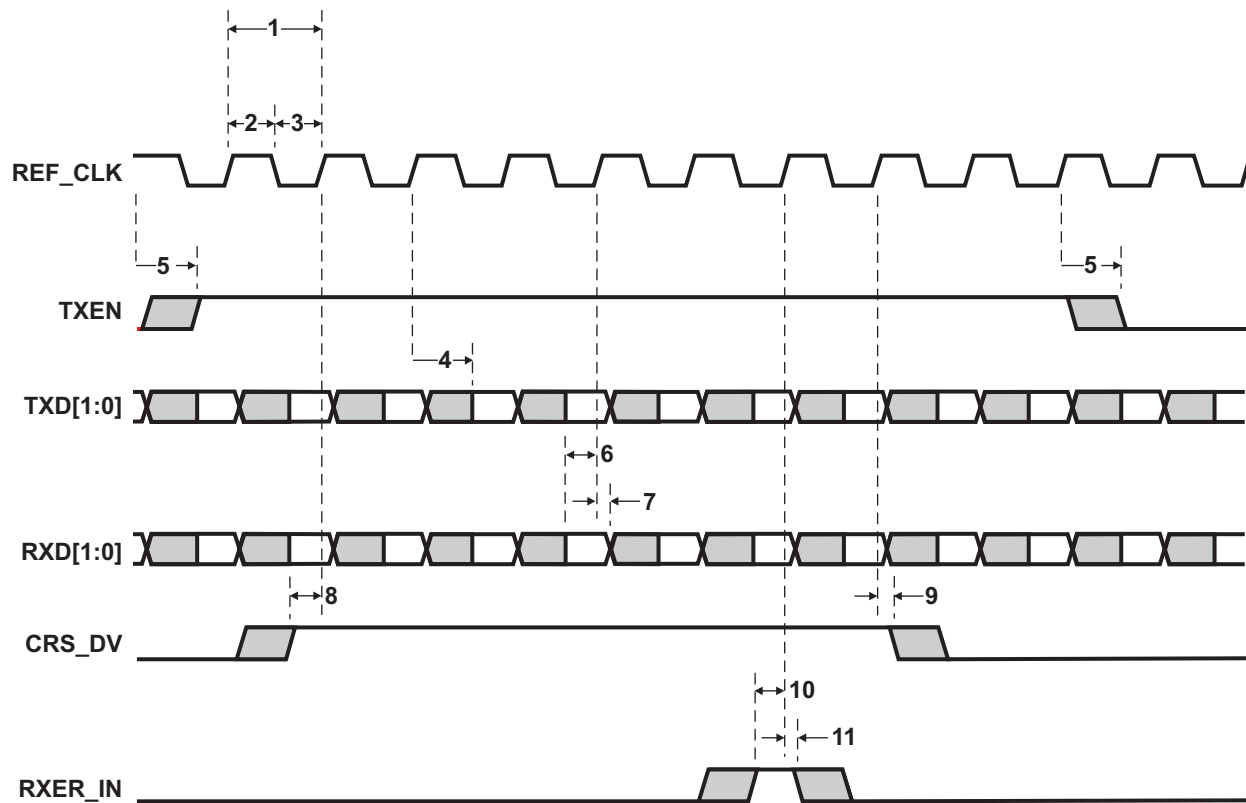
| NO. | PARAMETER         |                                                   | 1.8V, 3.3V |     |     |      |
|-----|-------------------|---------------------------------------------------|------------|-----|-----|------|
|     |                   |                                                   | MIN        | TYP | MAX | UNIT |
|     | fc(REFCLK)        | Frequency, REF_CLK                                | 50         |     |     | MHz  |
|     | ft (REFCLK)       | Frequency stability, REF_CLK                      | +/-50      |     |     | ppm  |
| 1   | tc(REFCLK)        | Cycle Time, REF_CLK                               | 20         |     |     | ns   |
| 2   | tw(REFCLKH)       | Pulse Width, REF_CLK High                         | 7          |     | 13  | ns   |
| 3   | tw(REFCLKL)       | Pulse Width, REF_CLK Low                          | 7          |     | 13  | ns   |
| 6   | tsu(RXD-REFCLK)   | Input Setup Time, RXD Valid before REF_CLK High   | 4          |     |     | ns   |
| 7   | th(REFCLK-RXD)    | Input Hold Time, RXD Valid after REF_CLK High     | 2          |     |     | ns   |
| 8   | tsu(CRSDV-REFCLK) | Input Setup Time, CRSDV Valid before REF_CLK High | 4          |     |     | ns   |
| 9   | th(REFCLK-CRSDV)  | Input Hold Time, CRSDV Valid after REF_CLK High   | 2          |     |     | ns   |
| 10  | tsu(RXER-REFCLK)  | Input Setup Time, RXER Valid before REF_CLK High  | 4          |     |     | ns   |
| 11  | th(REFCLK-RXER)   | Input Hold Time, RXER Valid after REF_CLK High    | 2          |     |     | ns   |

**Table 6-113. RMII Timing Conditions**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V |     | UNIT |
|----------------------------|-------------------------|------------|-----|------|
| <b>Input Conditions</b>    |                         | MIN        | MAX |      |
| t <sub>R</sub>             | Input signal rise time  | 1          | 5   | ns   |
| t <sub>F</sub>             | Input signal fall time  | 1          | 5   | ns   |
| <b>Output Conditions</b>   |                         |            |     |      |
| C <sub>LOAD</sub>          | Output load capacitance |            | 5.5 | pF   |

**Table 6-114. RMII Output Switching Characteristics**

| NO. | PARAMETER       |                                               | 1.8V, 3.3V |     |     |      |
|-----|-----------------|-----------------------------------------------|------------|-----|-----|------|
|     |                 |                                               | MIN        | TYP | MAX | UNIT |
| 4   | td(REFCLK-TXD)  | Output Delay Time, REF_CLK High to TXD Valid  | 2.5        |     | 13  | ns   |
| 5   | td(REFCLK-TXEN) | Output Delay Time, REF_CLK High to TXEN Valid | 2.5        |     | 13  | ns   |



SPRS550-004

Figure 6-52. RMII Timing Diagram

### 6.6.8 Management Data Input/Output (MDIO)

The Management Data Input/Output (MDIO) module continuously polls all 32 MDIO addresses in order to enumerate all PHY devices in the system.

The Management Data Input/Output (MDIO) module implements the 802.3 serial management interface to interrogate and control Ethernet PHY(s) using a shared two-wire bus. Host software uses the MDIO module to configure the auto-negotiation parameters of each PHY attached to the EMAC, retrieve the negotiation results, and configure required parameters in the EMAC module for correct operation. The module is designed to allow almost transparent operation of the MDIO interface, with very little maintenance from the core processor. Only one PHY may be connected at any given time.

#### 6.6.8.1 Management Data Input/Output (MDIO) Electrical Data/Timing

**Table 6-115. Timing Requirements for MDIO Input (see Figure 6-53 and Figure 6-54)**

| No. | PARAMETER                                                                  |     |     | UNIT |
|-----|----------------------------------------------------------------------------|-----|-----|------|
|     |                                                                            | MIN | MAX |      |
| 1   | $t_{c(MD\_CLK)}$ Cycle time, MD_CLK                                        | 400 |     | ns   |
| 4   | $t_{su(MDIO-MDCLKH)}$ Setup time, MDIO data input valid before MD_CLK high | 20  |     | ns   |
| 5   | $t_{h(MDCLKH-MDIO)}$ Hold time, MDIO data input valid after MDCLK high     | 0   |     | ns   |

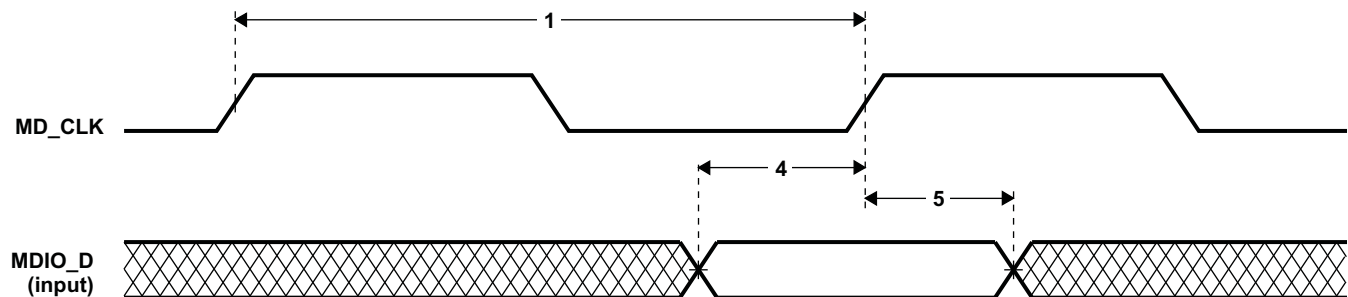


**Figure 6-53. MDIO Input Timing**

**Table 6-116. Switching Characteristics Over Recommended Operating Conditions for MDIO Output (see Figure 6-54)**

| No. | PARAMETER                                                            |     |     | UNIT |
|-----|----------------------------------------------------------------------|-----|-----|------|
|     |                                                                      | MIN | MAX |      |
| 7   | $t_{d(MDCLKL-MDIO)}$ Delay time, MDCLK low to MDIO data output valid | 0   | 100 | ns   |

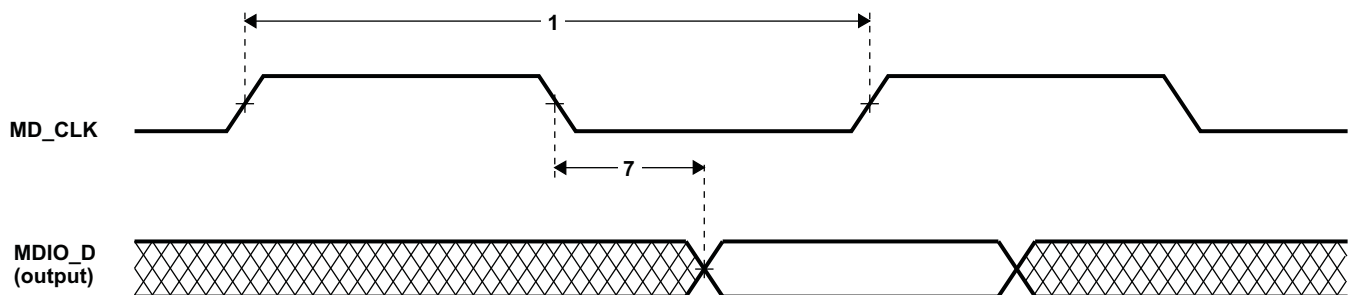


**Figure 6-54. MDIO Output Timing**

### 6.6.9 Universal Asynchronous Receiver/Transmitter (UART)

The AM3517/05 has four UARTs (one with Infrared Data Association [IrDA] and Consumer Infrared [CIR] modes).

**Table 6-117. Timing Requirements for UARTx Receive<sup>(1)</sup>**

| NO. |                |                                         | 1.8V, 3.3V |       | UNIT |
|-----|----------------|-----------------------------------------|------------|-------|------|
|     |                |                                         | MIN        | MAX   |      |
| 4   | $t_{w(URXDB)}$ | Pulse duration, receive data bit (RXDn) | .96U       | 1.05U | ns   |
| 5   | $t_{w(URXSB)}$ | Pulse duration, receive start bit       | .96U       | 1.05U | ns   |

(1) U = UART baud time = 1/programmed baud rate.

**Table 6-118. Switching Characteristics Over Recommended Operating Conditions for UARTx Transmit<sup>(1)</sup>**

| NO. | PARAMETER             |                                                              | 1.8V, 3.3V |       | UNIT |
|-----|-----------------------|--------------------------------------------------------------|------------|-------|------|
|     |                       |                                                              | MIN        | MAX   |      |
| 1   | f <sub>(baud)</sub>   | UART0 Maximum programmable baud rate f <sub>(baud_15)</sub>  | 5          |       | mbps |
|     |                       | UART0 Maximum programmable baud rate f <sub>(baud_30)</sub>  | 0.23       |       |      |
|     |                       | UART0 Maximum programmable baud rate f <sub>(baud_100)</sub> | 0.115      |       |      |
| 2   | t <sub>w(UTXDB)</sub> | Pulse duration, transmit data bit, 15/30/100 pF              | U - 2      | U + 2 | ns   |
| 3   | t <sub>w(UTXSB)</sub> | Pulse duration, transmit start bit, 15/30/100 pF             | U - 2      | U + 2 | ns   |

(1) U = UART baud time = 1/programmed baud rate.

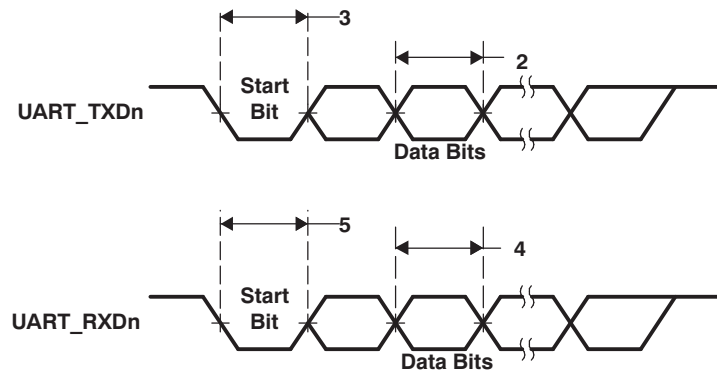
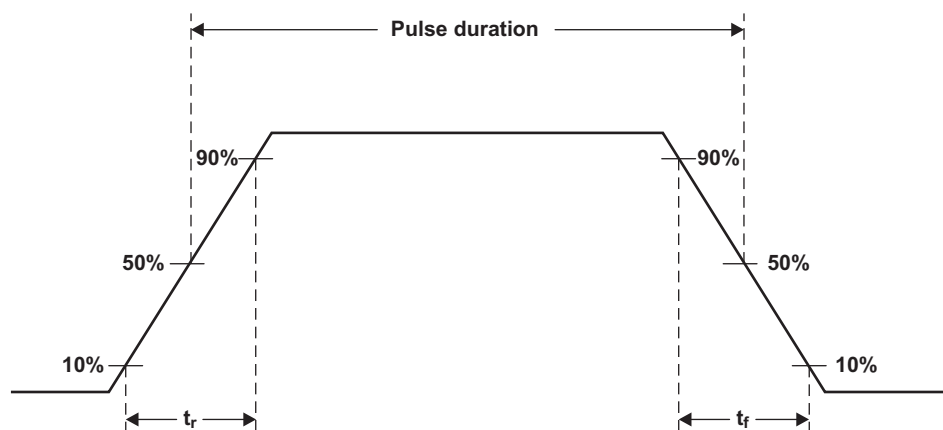


**Figure 6-55. UART Transmit/Receive Timing**

#### 6.6.9.1 UART IrDA Interface

The IrDA module can operate in three different modes:

- Slow infrared (SIR) ( $\leq 115.2$  Kbits/s)
- Medium infrared (MIR) (0.576 Mbits/s and 1.152 Mbits/s)
- Fast infrared (FIR) (4 Mbits/s)



030-118

Figure 6-56. UART IrDA Pulse Parameters

#### 6.6.9.1.1 IrDA—Receive Mode

Table 6-119. UART IrDA—Signaling Rate and Pulse Duration—Receive Mode

| SIGNALING RATE            | ELECTRICAL PULSE DURATION |         |       | UNIT |
|---------------------------|---------------------------|---------|-------|------|
|                           | MIN                       | NOMINAL | MAX   |      |
| SIR                       |                           |         |       |      |
| 2.4 Kbit/s                | 1.41                      | 78.1    | 88.55 | μs   |
| 9.6 Kbit/s                | 1.41                      | 19.5    | 22.13 | μs   |
| 19.2 Kbit/s               | 1.41                      | 9.75    | 11.07 | μs   |
| 38.4 Kbit/s               | 1.41                      | 4.87    | 5.96  | μs   |
| 57.6 Kbit/s               | 1.41                      | 3.25    | 4.34  | μs   |
| 115.2 Kbit/s              | 1.41                      | 1.62    | 2.23  | μs   |
| MIR                       |                           |         |       |      |
| 0.576 Mbit/s              | 297.2                     | 416     | 518.8 | ns   |
| 1.152 Mbit/s              | 149.6                     | 208     | 258.4 | ns   |
| FIR                       |                           |         |       |      |
| 4.0 Mbit/s (Single pulse) | 67                        | 125     | 164   | ns   |
| 4.0 Mbit/s (Double pulse) | 190                       | 250     | 289   | ns   |

Table 6-120. UART IrDA—Rise and Fall Time—Receive Mode

|       | PARAMETER                      | MAX | UNIT |
|-------|--------------------------------|-----|------|
| $t_R$ | Rising time,<br>uart3_rx_irrx  | 200 | ns   |
| $t_F$ | Falling time,<br>uart3_rx_irrx | 200 | ns   |

### 6.6.9.1.2 IrDA—Transmit Mode

**Table 6-121. UART IrDA—Signaling Rate and Pulse Duration—Transmit Mode**

| SIGNALING RATE            | ELECTRICAL PULSE DURATION |         |      | UNIT |
|---------------------------|---------------------------|---------|------|------|
|                           | MIN                       | NOMINAL | MAX  |      |
| SIR                       |                           |         |      |      |
| 2.4 Kbit/s                | 78.1                      | 78.1    | 78.1 | μs   |
| 9.6 Kbit/s                | 19.5                      | 19.5    | 19.5 | μs   |
| 19.2 Kbit/s               | 9.75                      | 9.75    | 9.75 | μs   |
| 38.4 Kbit/s               | 4.87                      | 4.87    | 4.87 | μs   |
| 57.6 Kbit/s               | 3.25                      | 3.25    | 3.25 | μs   |
| 115.2 Kbit/s              | 1.62                      | 1.62    | 1.62 | μs   |
| MIR                       |                           |         |      |      |
| 0.576 Mbit/s              | 414                       | 416     | 419  | ns   |
| 1.152 Mbit/s              | 206                       | 208     | 211  | ns   |
| FIR                       |                           |         |      |      |
| 4.0 Mbit/s (Single pulse) | 123                       | 125     | 128  | ns   |
| 4.0 Mbit/s (Double pulse) | 248                       | 250     | 253  | ns   |

### 6.6.10 HDQ / 1-Wire Interfaces

This module is intended to work with both the HDQ and the 1-Wire protocols. The protocols use a single wire to communicate between the master and the slave. The protocols employ an asynchronous return to 1 mechanism where, after any command, the line is pulled high.

#### 6.6.10.1 HDQ Protocol

Table 6-122 and Table 6-123 assume testing over the recommended operating conditions (see Figure 6-57 through Figure 6-60).

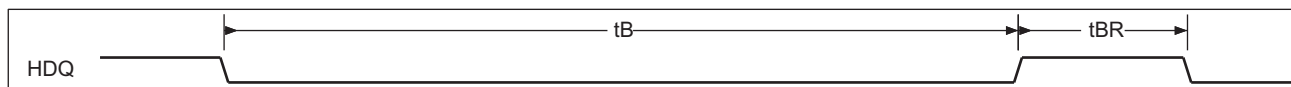
**Table 6-122. HDQ Timing Requirements**

| PARAMETER         | DESCRIPTION                                 | MIN | MAX | UNIT |
|-------------------|---------------------------------------------|-----|-----|------|
| t <sub>CYCD</sub> | Bit window                                  | 253 |     | s    |
| t <sub>HW1</sub>  | Reads 1                                     |     | 68  |      |
| t <sub>HW0</sub>  | Reads 0                                     | 180 |     |      |
| t <sub>RSPS</sub> | Command to host respond time <sup>(1)</sup> |     |     |      |

(1) Defined by software.

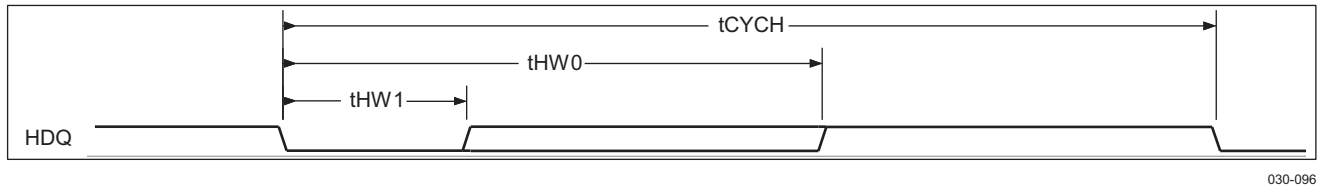
**Table 6-123. HDQ Switching Characteristics**

| PARAMETER         | DESCRIPTION    | MIN | TYP | MAX | UNIT |
|-------------------|----------------|-----|-----|-----|------|
| t <sub>B</sub>    | Break timing   |     | 193 |     | s    |
| t <sub>BR</sub>   | Break recovery |     | 63  |     |      |
| t <sub>CYCH</sub> | Bit window     |     | 253 |     |      |
| t <sub>DW1</sub>  | Sends1 (write) |     | 1.3 |     |      |
| t <sub>DW0</sub>  | Sends0 (write) |     | 101 |     |      |



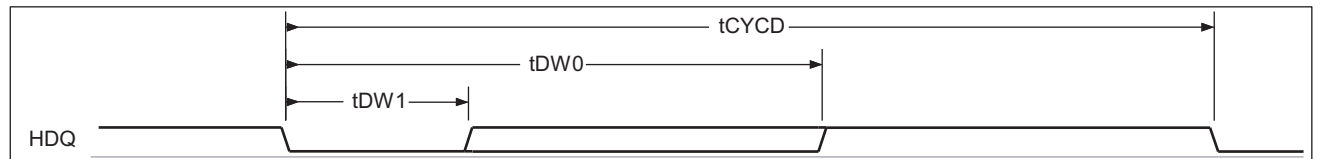
030-095

**Figure 6-57. HDQ Break (Reset) Timing**



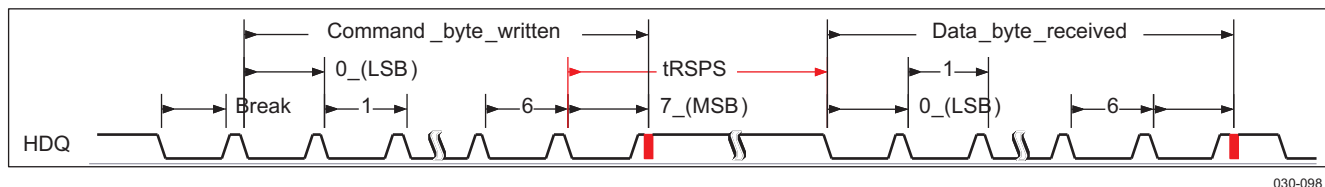
030-096

Figure 6-58. HDQ Read Bit Timing (Data)



030-097

Figure 6-59. HDQ Write Bit Timing (Command/Address or Data)



030-098

Figure 6-60. HDQ Communication Timing

### 6.6.10.2 1-Wire Protocol

Table 6-124 and Table 6-125 assume testing over the recommended operating conditions (see Figure 6-61 through Figure 6-63).

Table 6-124. 1-Wire Timing Requirements

| PARAMETER           | DESCRIPTION               | MIN          | MAX | UNIT |
|---------------------|---------------------------|--------------|-----|------|
| $t_{PDH}$           | Presence pulse delay high |              | 68  | S    |
| $t_{PDL}$           | Presence pulse delay low  | $68 t_{PDH}$ |     |      |
| $t_{RDV} + t_{REL}$ | Read bit-zero time        |              | 102 |      |

Table 6-125. 1-Wire Switching Characteristics

| PARAMETER  | DESCRIPTION          | MIN | TYP | MAX | UNIT |
|------------|----------------------|-----|-----|-----|------|
| $t_{RSTL}$ | Reset time low       |     | 484 |     | S    |
| $t_{RSTH}$ | Reset time high      |     | 484 |     |      |
| $t_{SLOT}$ | Write bit cycle time |     | 102 |     |      |
| $t_{LOW1}$ | Write bit-one time   |     | 1.3 |     |      |
| $t_{LOW0}$ | Write bit-zero time  |     | 101 |     |      |
| $t_{REC}$  | Recovery time        |     | 134 |     |      |
| $t_{LOWR}$ | Read bit strobe time |     | 13  |     |      |



030-099

Figure 6-61. 1-Wire Break (Reset) Timing

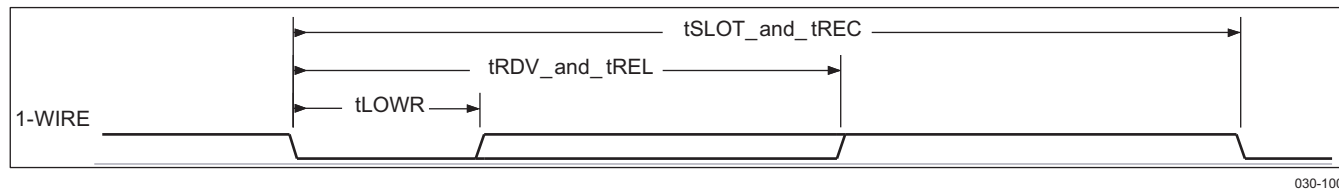


**Figure 6-62. 1-Wire Read Bit Timing (Data)**

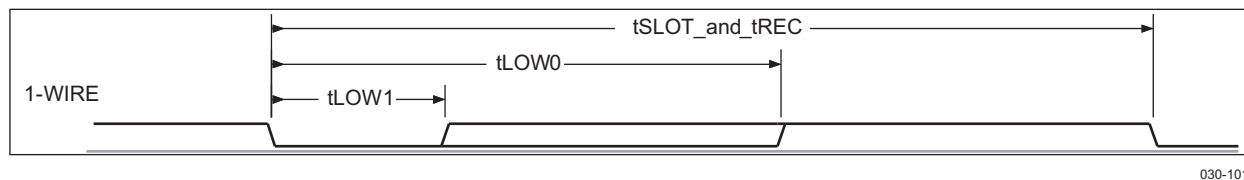


**Figure 6-63. 1-Wire Write Bit Timing (Command/Address or Data)**

### 6.6.11 I<sup>2</sup>C Interface

The multimaster I<sup>2</sup>C peripheral provides an interface between two or more devices via an I<sup>2</sup>C serial bus. The I<sup>2</sup>C controller supports the multimaster mode which allows more than one device capable of controlling the bus to be connected to it. Each I<sup>2</sup>C device is recognized by a unique address and can operate as either transmitter or receiver, according to the function of the device. In addition to being a transmitter or receiver, a device connected to the I<sup>2</sup>C bus can also be considered as master or slave when performing data transfers. This data transfer is carried out via two serial bidirectional wires:

- An SDA data line
- An SCL clock line

The following sections illustrate the data transfer is in master or slave configuration with 7-bit addressing format. The I<sup>2</sup>C interface is compliant with Philips I<sup>2</sup>C specification version 2.1. It supports standard mode (up to 100K bits/s), fast mode (up to 400K bits/s) and high-speed mode (up to 3.4Mb/s) .

#### 6.6.11.1 I<sup>2</sup>C Standard/Fast-Speed Mode

**Table 6-126. I<sup>2</sup>C Standard/Fast-Speed Mode Timings**

| NO. | PARAMETER <sup>(1)</sup>   |                                                                                                                   | 1.8V, 3.3-V   |                     |                    |                    | UNIT |
|-----|----------------------------|-------------------------------------------------------------------------------------------------------------------|---------------|---------------------|--------------------|--------------------|------|
|     |                            |                                                                                                                   | STANDARD MODE |                     | FAST MODE          |                    |      |
|     |                            |                                                                                                                   | MIN           | MAX                 | MIN                | MAX                |      |
|     | f <sub>SCL</sub>           | Clock Frequency, i2cX_scl                                                                                         |               | 100                 |                    | 400                | kHz  |
| I1  | t <sub>w(SCLH)</sub>       | Pulse Duration, i2cX_scl high                                                                                     | 4             |                     | 0.6                |                    | s    |
| I2  | t <sub>w(SCLL)</sub>       | Pulse Duration, i2cX_scl low                                                                                      | 4.7           |                     | 1.3                |                    | s    |
| I3  | t <sub>su(SDAV-SCLH)</sub> | Setup time, i2cX_sda valid before i2cX_scl active level                                                           | 250           |                     | 100 <sup>(2)</sup> |                    | ns   |
| I4  | t <sub>h(SCLHSDAV)</sub>   | Hold time, i2cX_sda valid after i2cX_scl active level                                                             |               | 3.45 <sup>(3)</sup> |                    | 0.9 <sup>(3)</sup> | s    |
| I5  | t <sub>su(SDAL-SCLH)</sub> | Setup time, i2cX_scl high after i2cX_sda low (for a START <sup>(4)</sup> condition or a repeated START condition) | 4.7           |                     | 0.6                |                    | s    |
| I6  | t <sub>h(SCLHSDAH)</sub>   | Hold time, i2cX_sda low level after i2cX_scl high level (STOP condition)                                          | 4             |                     | 0.6                |                    | s    |
| I7  | t <sub>h(SCLHRSTART)</sub> | Hold time, i2cX_sda low level after i2cX_scl high level (for a repeated START condition)                          | 4             |                     | 0.6                |                    | s    |
| I8  | t <sub>w(SDAH)</sub>       | Pulse duration, i2cX_sda high between STOP and START conditions                                                   | 4.7           |                     | 1.3                |                    | s    |
|     | t <sub>R(SCL)</sub>        | Rise time, i2cX_scl                                                                                               |               | 1000                |                    | 300                | ns   |
|     | t <sub>F(SCL)</sub>        | Fall time, i2cX_scl                                                                                               |               | 300                 |                    | 300                | ns   |
|     | t <sub>R(SDA)</sub>        | Rise time, i2cX_sda                                                                                               |               | 1000                |                    | 300                | ns   |
|     | t <sub>F(SDA)</sub>        | Fall time, i2cX_sda                                                                                               |               | 300                 |                    | 300                | ns   |
|     | CB                         | Capacitive load for each bus line                                                                                 |               | 60                  |                    | 60                 | pF   |

(1) In i2cX, X is equal to 1, 2, or 3.

(2) A fast-mode I<sup>2</sup>C-bus device can be used in a standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>su(SDAV-SCLH)</sub> 250 ns must then be met. This is automatically the case if the device does not stretch the low period of the i2cx\_scl. If such a device does stretch the low period of the i2cx\_scl, it must output the next data bit to the i2cx\_sda line t<sub>r(SDA)</sub> max + t<sub>su(SDAV-SCLH)</sub> = 1000 + 250 = 1250 ns (according to the standard-mode I<sup>2</sup>C-bus specification) before the i2cx\_scl line is released.

(3) The maximum t<sub>h(SCLHSDAH)</sub> has only to be met if the device does not stretch the low period of the i2cx\_scl signal.

(4) After this time, the first clock is generated.

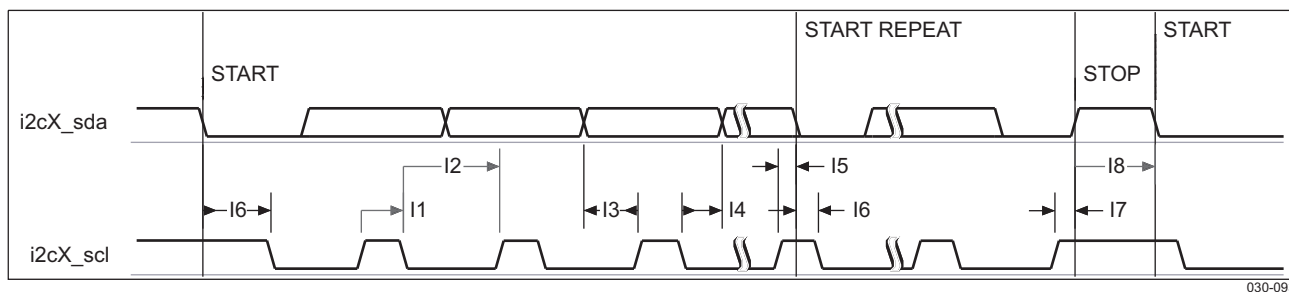


**Figure 6-64. I<sup>2</sup>C Standard/Fast Mode**

### 6.6.11.2 I<sup>2</sup>C High-Speed Mode

**Table 6-127. I<sup>2</sup>C High-Speed Mode Timings<sup>(1) (2)</sup>**

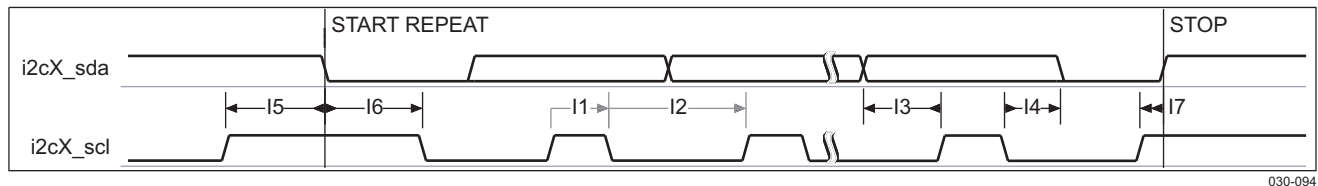
| NO. | PARAMETER                   |                                                                                                                   | 1.8V, 3.3V         |     | UNIT |
|-----|-----------------------------|-------------------------------------------------------------------------------------------------------------------|--------------------|-----|------|
|     |                             |                                                                                                                   | MIN                | MAX |      |
|     | f <sub>SCL</sub>            | Clock frequency, i2cX_scl                                                                                         |                    | 3.4 | MHz  |
| I1  | t <sub>w</sub> (SCLH)       | Pulse duration, i2cX_scl high                                                                                     | 60 <sup>(3)</sup>  |     | s    |
| I2  | t <sub>w</sub> (SCLL)       | Pulse duration, i2cX_scl low                                                                                      | 160 <sup>(3)</sup> |     | s    |
| I3  | t <sub>su</sub> (SDAV-SCLH) | Setup time, i2cX_sda valid before i2cX_scl active level                                                           | 10                 |     | ns   |
| I4  | t <sub>h</sub> (SCLHSDAV)   | Hold time, i2cX_sda valid after i2cX_scl active level                                                             |                    | 70  | s    |
| I5  | t <sub>su</sub> (SDAL-SCLH) | Setup time, i2cX_scl high after i2cX_sda low (for a START <sup>(4)</sup> condition or a repeated START condition) | 160                |     | s    |
| I6  | t <sub>h</sub> (SCLHSDAH)   | Hold time, i2cX_sda low level after i2cX_scl high level (STOP condition)                                          | 160                |     | s    |
| I7  | t <sub>h</sub> (SCLHRSTART) | Hold time, i2cX_sda low level after i2cX_scl high level (for a repeated START condition)                          | 160                |     | ns   |
|     | t <sub>R</sub> (SCL)        | Rise time, i2cX_scl                                                                                               | 10                 | 40  | ns   |
|     | t <sub>R</sub> (SCL)        | Rise time, i2cX_scl after a repeated START condition and after a bit acknowledge                                  | 10                 | 80  | ns   |
|     | t <sub>F</sub> (SCL)        | Fall time, i2cX_scl                                                                                               | 10                 | 40  | ns   |
|     | t <sub>R</sub> (SDA)        | Rise time, i2cX_sda                                                                                               | 10                 | 80  | ns   |
|     | t <sub>F</sub> (SDA)        | Fall time, i2cX_sda                                                                                               | 10                 | 80  | ns   |

(1) In i2cX, X is equal to 1, 2, or 3.

(2) The device provides (via the I<sup>2</sup>C bus) a hold time of at least 300 ns for the i2cx\_sda signal (refer to the fall and rise time of i2cx\_scl) to bridge the undefined region of the falling edge of i2cx\_scl.

(3) HS-mode master devices generate a serial clock signal with a high to low ratio of 1 to 2. t<sub>w</sub>(SCLL) > 2 t<sub>w</sub>(SCLH).

(4) After this time, the first clock is generated.



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**Figure 6-65. I<sup>2</sup>C High-Speed Mode<sup>(1) (2) (3)</sup>**

(1) HS-mode master devices generate a serial clock signal with a high-to-low ratio of 1 to 2. t<sub>w</sub>(SCLL) > 2 x t<sub>w</sub>(SCLH).

(2) In i2cX, X is equal to 1, 2, or 3.

(3) After this time, the first clock is generated.

**Table 6-128. Correspondence Standard vs. TI Timing References**

|    | AM3517/05                    | STANDARD-I <sup>2</sup> C |                     |
|----|------------------------------|---------------------------|---------------------|
|    |                              | S/F Mode                  | HS Mode             |
|    | f <sub>SCL</sub>             | F <sub>SCL</sub>          | F <sub>SCLH</sub>   |
| I1 | t <sub>w</sub> (SCLH)        | T <sub>HIGH</sub>         | T <sub>HIGH</sub>   |
| I2 | t <sub>w</sub> (SCLL)        | T <sub>LOW</sub>          | T <sub>LOW</sub>    |
| I3 | t <sub>su</sub> (SDAV-SCLH)  | T <sub>SU,DAT</sub>       | T <sub>SU,DAT</sub> |
| I4 | t <sub>h</sub> (SCLH-SDAV)   | T <sub>SU,DAT</sub>       | T <sub>SU,DAT</sub> |
| I5 | t <sub>su</sub> (SDAL-SCLH)  | T <sub>SU,STA</sub>       | T <sub>SU,STA</sub> |
| I6 | t <sub>h</sub> (SCLH-SDAH)   | T <sub>HD,STA</sub>       | T <sub>HD,STA</sub> |
| I7 | t <sub>h</sub> (SCLH-RSTART) | T <sub>SU,STO</sub>       | T <sub>SU,STO</sub> |
| I8 | t <sub>w</sub> (SDAH)        | T <sub>BUF</sub>          |                     |

## 6.7 Removable Media Interfaces

### 6.7.1 High-Speed Multimedia Memory Card (MMC) and Secure Digital IO Card (SDIO) Timing

The MMC/SDIO host controller provides an interface to high-speed and standard MMC, SD memory cards, or SDIO cards. The application interface is responsible for managing transaction semantics. The MMC/SDIO host controller deals with MMC/SDIO protocol at transmission level, packing data, adding CRC, start/end bit, and checking for syntactical correctness.

There are three MMC interfaces on the AM3517/05:

- MMC/SD/SDIO Interface 1:
  - 1.8-V/3.3-V support
  - 8 bits
- MMC/SD/SDIO Interface 2:
  - 1.8-V/3.3-V support
  - 8 bits
  - 4 bits with external transceiver allowing to support 1.8-V/3.3-V peripherals in 1.8-V mode operation. Transceiver direction control signals are multiplexed with the upper four data bits.
- MMC/SD/SDIO Interface 3:
  - 1.8-V/3.3-V support
  - 8 bits

#### 6.7.1.1 MMC/SD/SDIO in SD Identification Mode

Table 6-129 through Table 6-131 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-129. MMC/SD/SDIO Timing Conditions SD Identification Mode**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V |     | UNIT |
|----------------------------|-------------------------|------------|-----|------|
|                            |                         | MIN        | MAX |      |
| SD Identification Mode     |                         |            |     |      |
| Input Conditions           |                         |            |     |      |
| t <sub>r</sub>             | Input signal rise time  |            | 10  | ns   |
| t <sub>f</sub>             | Input signal fall time  |            | 10  | ns   |
| Output Conditions          |                         |            |     |      |
| C <sub>LOAD</sub>          | Output load capacitance |            | 30  | pF   |

**Table 6-130. MMC/SD/SDIO Timing Requirements SD Identification Mode<sup>(1) (2) (3) (4)</sup>**

| NO.                     | PARAMETER                     |                                                              | 1.8V, 3.3V |     | UNIT |
|-------------------------|-------------------------------|--------------------------------------------------------------|------------|-----|------|
|                         |                               |                                                              | MIN        | MAX |      |
| SD Identification Mode  |                               |                                                              |            |     |      |
| MMC/SD/SDIO Interface 1 |                               |                                                              |            |     |      |
| HSSD3/SD3               | t <sub>SU</sub> (CMDV-CLKIH)  | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 1198.4     |     | ns   |
| HSSD4/SD4               | t <sub>SU</sub> (CLKIH-CMDIV) | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge   | 1249.2     |     | ns   |
| MMC/SD/SDIO Interface 2 |                               |                                                              |            |     |      |
| HSSD3/SD3               | t <sub>SU</sub> (CMDV-CLKIH)  | Setup time, mmc2_cmd valid before mmc2_clk rising clock edge | 1198.4     |     | ns   |

(1) Timing parameters refer to output clock specified in Table 6-131.

(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-131.

(3) Corresponding figures showing timing parameters are common with other interface modes. (See SD and HS SD modes).

(4) For more information, see the AM35x ARM Microprocessor Technical Reference Manual (SPRUGR0).

**Table 6-130. MMC/SD/SDIO Timing Requirements SD Identification Mode<sup>(1) (2) (3)(4)</sup> (continued)**

| NO.                            | PARAMETER             |                                                              | 1.8V, 3.3V |     | UNIT |
|--------------------------------|-----------------------|--------------------------------------------------------------|------------|-----|------|
|                                |                       |                                                              | MIN        | MAX |      |
| HSSD4/SD4                      | $t_{su}(CLKIH-CMDIV)$ | Hold time, mmc2_cmd valid after mmc2_clk rising clock edge   | 1249.2     |     | ns   |
| <b>MMC/SD/SDIO Interface 3</b> |                       |                                                              |            |     |      |
| HSSD3/SD3                      | $t_{su}(CMDV-CLKIH)$  | Setup time, mmc3_cmd valid before mmc3_clk rising clock edge | 1198.4     |     | ns   |
| HSSD4/SD4                      | $t_{su}(CLKIH-CMDIV)$ | Hold time, mmc3_cmd valid after mmc3_clk rising clock edge   | 1249.2     |     | ns   |

**Table 6-131. MMC/SD/SDIO Switching Characteristics SD Identification Mode<sup>(1)(2)</sup>**

| NO.                     | PARAMETER                 |                                                               | 1.8V, 3.3V               |        | UNIT |
|-------------------------|---------------------------|---------------------------------------------------------------|--------------------------|--------|------|
|                         |                           |                                                               | MIN                      | MAX    |      |
| SD Identification Mode  |                           |                                                               |                          |        |      |
| HSSD1/SD1               | $t_{c(\text{clk})}$       | Cycle time, output clk period                                 |                          | 2500   | ns   |
| HSSD2/SD2               | $t_{W(\text{clkH})}$      | Typical pulse duration, output clk high                       | $X^{(3)} \cdot PO^{(4)}$ |        | ns   |
| HSSD2/SD2               | $t_{W(\text{clkL})}$      | Typical pulse duration, output clk low                        | $Y^{(5)} \cdot PO^{(4)}$ |        | ns   |
|                         | $t_{dc(\text{clk})}$      | Duty cycle error, output clk                                  |                          | 125    | ns   |
|                         | $t_{j(\text{clk})}$       | Jitter standard deviation, output clk                         |                          | 200    | ps   |
| MMC/SD/SDIO Interface 1 |                           |                                                               |                          |        |      |
|                         | $t_{r(\text{clk})}$       | Rise time, output clk                                         |                          | 10     | ns   |
|                         | $t_{f(\text{clkH})}$      | Fall time, output clk                                         |                          | 10     | ns   |
|                         | $t_{r(\text{clkL})}$      | Rise time, output data                                        |                          | 10     | ns   |
|                         | $t_{f(\text{clk})}$       | Fall time, output data                                        |                          | 10     | ns   |
| HSSD5/SD5               | $t_{d(\text{CLKOH-CMD})}$ | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition | 6.3                      | 2492.7 | ns   |
| MMC/SD/SDIO Interface 2 |                           |                                                               |                          |        |      |
|                         | $t_{r(\text{clk})}$       | Rise time, output clk                                         |                          | 10     | ns   |
|                         | $t_{f(\text{clkH})}$      | Fall time, output clk                                         |                          | 10     | ns   |
|                         | $t_{r(\text{clkL})}$      | Rise time, output data                                        |                          | 10     | ns   |
|                         | $t_{f(\text{clk})}$       | Fall time, output data                                        |                          | 10     | ns   |
| HSSD5/SD5               | $t_{d(\text{CLKOH-CMD})}$ | Delay time, mmc2_clk rising clock edge to mmc2_cmd transition | 6.3                      | 2492.7 | ns   |
| MMC/SD/SDIO Interface 3 |                           |                                                               |                          |        |      |
|                         | $t_{r(\text{clk})}$       | Rise time, output clk                                         |                          | 10     | ns   |
|                         | $t_{f(\text{clkH})}$      | Fall time, output clk                                         |                          | 10     | ns   |
|                         | $t_{r(\text{clkL})}$      | Rise time, output data                                        |                          | 10     | ns   |
|                         | $t_{f(\text{clk})}$       | Fall time, output data                                        |                          | 10     | ns   |
| HSSD5/SD5               | $t_{d(\text{CLKOH-CMD})}$ | Delay time, mmc3_clk rising clock edge to mmc3_cmd transition | 6.3                      | 2492.7 | ns   |

(1) Corresponding figures showing timing parameters are common with other interface modes (see SD and HS SD modes).

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The X parameter is defined as listed below.

(4) PO = output clk period in ns.

(5) The Y parameter is defined as listed below.

**Table 6-132. X Parameter**

| CLKD      | X                                             |
|-----------|-----------------------------------------------|
| 1 or Even | 0.5                                           |
| Odd       | $(\text{trunc}[\text{CLKD}/2]+1)/\text{CLKD}$ |

**Table 6-133. Y Parameter**

| CLKD      | Y                    |
|-----------|----------------------|
| 1 or Even | 0.5                  |
| Odd       | (trunc[CLKD/2])/CLKD |

### 6.7.1.2 MMC/SD/SDIO in High-Speed MMC Mode

Table 6-134 through Table 6-136 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-134. MMC/SD/SDIO Timing Conditions High-Speed MMC Mode**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V |     | UNIT |
|----------------------------|-------------------------|------------|-----|------|
|                            |                         | MIN        | MAX |      |
| High-Speed MMC Mode        |                         |            |     |      |
| Input Conditions           |                         |            |     |      |
| t <sub>r</sub>             | Input signal rise time  | 0.19       | 3   | ns   |
| t <sub>f</sub>             | Input signal fall time  | 0.19       | 3   | ns   |
| Output Conditions          |                         |            |     |      |
| C <sub>LOAD</sub>          | Output load capacitance |            | 30  | pF   |

**Table 6-135. MMC/SD/SDIO Timing Requirements High-Speed MMC Mode<sup>(1)(2)(3)(4)</sup>**

| NO.                     | PARAMETER                     |                                                               | 1.8 V |     | 3.3V |     | UNIT |
|-------------------------|-------------------------------|---------------------------------------------------------------|-------|-----|------|-----|------|
|                         |                               |                                                               | MIN   | MAX | MIN  | MAX |      |
| High-Speed MMC Mode     |                               |                                                               |       |     |      |     |      |
| MMC/SD/SDIO Interface 1 |                               |                                                               |       |     |      |     |      |
| MMC3                    | t <sub>SU</sub> (CMDV-CLKIH)  | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge  | 2.13  |     | 2.41 |     | ns   |
| MMC4                    | t <sub>H</sub> (CLKIH-CMDIV)  | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge    | 3.47  |     | 2.09 |     | ns   |
| MMC7                    | t <sub>SU</sub> (DATxV-CLKIH) | Setup time, mmc1_datx valid before mmc1_clk rising clock edge | 2.13  |     | 2.41 |     | ns   |
| MMC8                    | t <sub>H</sub> (CLKIH-DATxIV) | Hold time, mmc1_datx valid after mmc1_clk rising clock edge   | 3.47  |     | 2.09 |     | ns   |
| MMC/SD/SDIO Interface 2 |                               |                                                               |       |     |      |     |      |
| MMC3                    | t <sub>SU</sub> (CMDV-CLKIH)  | Setup time, mmc2_cmd valid before mmc2_clk rising clock edge  | 2.88  |     | 3.23 |     | ns   |
| MMC4                    | t <sub>H</sub> (CLKIH-CMDIV)  | Hold time, mmc2_cmd valid after mmc2_clk rising clock edge    | 2.90  |     | 1.46 |     | ns   |
| MMC7                    | t <sub>SU</sub> (DATxV-CLKIH) | Setup time, mmc2_datx valid before mmc2_clk rising clock edge | 2.88  |     | 3.23 |     | ns   |
| MMC8                    | t <sub>H</sub> (CLKIH-DATxIV) | Hold time, mmc2_datx valid after mmc2_clk rising clock edge   | 2.90  |     | 1.46 |     | ns   |
| MMC/SD/SDIO Interface 3 |                               |                                                               |       |     |      |     |      |
| MMC3                    | t <sub>SU</sub> (CMDV-CLKIH)  | Setup time, mmc3_cmd valid before mmc3_clk rising clock edge  | 3.38  |     | 3.41 |     | ns   |
| MMC4                    | t <sub>H</sub> (CLKIH-CMDIV)  | Hold time, mmc3_cmd valid after mmc3_clk rising clock edge    | 2.83  |     | 1.46 |     | ns   |
| MMC7                    | t <sub>SU</sub> (DATxV-CLKIH) | Setup time, mmc3_datx valid before mmc3_clk rising clock edge | 3.38  |     | 3.41 |     | ns   |
| MMC8                    | t <sub>H</sub> (CLKIH-DATxIV) | Hold time, mmc3_datx valid after mmc3_clk rising clock edge   | 2.83  |     | 1.46 |     | ns   |

(1) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

(2) Timing parameters refer to output clock specified in Table 6-136.

(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in Table 6-136.

(4) Corresponding figures showing timing parameters are common with Standard MMC mode.

**Table 6-136. MMC/SD/SDIO Switching Characteristics High-Speed MMC Mode<sup>(1)(2)</sup>**

| N O.                    | PARAMETER                  |                                                                | 1.8V, 3.3V                          |         | UNIT |
|-------------------------|----------------------------|----------------------------------------------------------------|-------------------------------------|---------|------|
|                         |                            |                                                                | MIN                                 | MAX     |      |
| High-Speed MMC Mode     |                            |                                                                |                                     |         |      |
| MMC1                    | t <sub>c(clk)</sub>        | Cycle time, output clk period                                  |                                     | 20.83   | ns   |
| MMC2                    | t <sub>W(clkH)</sub>       | Typical pulse duration, output clk high                        | X <sup>(3)</sup> *PO <sup>(4)</sup> |         | ns   |
| MMC2                    | t <sub>W(clkL)</sub>       | Typical pulse duration, output clk low                         | Y <sup>(5)</sup> *PO <sup>(4)</sup> |         | ns   |
|                         | t <sub>dc(clk)</sub>       | Duty cycle error, output clk                                   |                                     | 1041.67 | ps   |
|                         | t <sub>j(clk)</sub>        | Jitter standard deviation, output clk                          |                                     | 200     | ps   |
| MMC/SD/SDIO Interface 1 |                            |                                                                |                                     |         |      |
|                         | t <sub>c(clk)</sub>        | Rise time, output clk                                          |                                     | 3       | ns   |
|                         | t <sub>W(clkH)</sub>       | Fall time, output clk                                          |                                     | 3       | ns   |
|                         | t <sub>W(clkL)</sub>       | Rise time, output data                                         |                                     | 3       | ns   |
|                         | t <sub>dc(clk)</sub>       | Fall time, output data                                         |                                     | 3       | ns   |
| MMC5                    | t <sub>d(CLKOH-CMD)</sub>  | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition  | 3.7                                 | 14.11   | ns   |
| MMC6                    | t <sub>d(CLKOH-DATx)</sub> | Delay time, mmc1_clk rising clock edge to mmc1_datx transition | 3.7                                 | 16.50   | ns   |
| MMC/SD/SDIO Interface 2 |                            |                                                                |                                     |         |      |
|                         | t <sub>c(clk)</sub>        | Rise time, output clk                                          |                                     | 3       | ns   |
|                         | t <sub>W(clkH)</sub>       | Fall time, output clk                                          |                                     | 3       | ns   |
|                         | t <sub>W(clkL)</sub>       | Rise time, output data                                         |                                     | 3       | ns   |
|                         | t <sub>dc(clk)</sub>       | Fall time, output data                                         |                                     | 3       | ns   |
| MMC5                    | t <sub>d(CLKOH-CMD)</sub>  | Delay time, mmc2_clk rising clock edge to mmc2_cmd transition  | 3.7                                 | 14.11   | ns   |
| MMC6                    | t <sub>d(CLKOH-DATx)</sub> | Delay time, mmc2_clk rising clock edge to mmc2_datx transition | 3.7                                 | 16.50   | ns   |
| MMC/SD/SDIO Interface 3 |                            |                                                                |                                     |         |      |
|                         | t <sub>c(clk)</sub>        | Rise time, output clk                                          |                                     | 3       | ns   |
|                         | t <sub>W(clkH)</sub>       | Fall time, output clk                                          |                                     | 3       | ns   |
|                         | t <sub>W(clkL)</sub>       | Rise time, output data                                         |                                     | 3       | ns   |
|                         | t <sub>dc(clk)</sub>       | Fall time, output data                                         |                                     | 3       | ns   |
| MMC5                    | t <sub>d(CLKOH-CMD)</sub>  | Delay time, mmc3_clk rising clock edge to mmc3_cmd transition  | 3.7                                 | 14.11   | ns   |
| MMC6                    | t <sub>d(CLKOH-DATx)</sub> | Delay time, mmc3_clk rising clock edge to mmc3_datx transition | 3.7                                 | 14.11   | ns   |

(1) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The X parameter is defined as listed below.

(4) PO = output clk period in ns.

(5) The Y parameter is defined as listed below.

**Table 6-137. X Parameter**

| CLKD      | X                                             |
|-----------|-----------------------------------------------|
| 1 or Even | 0.5                                           |
| Odd       | $(\text{trunc}[\text{CLKD}/2]+1)/\text{CLKD}$ |

**Table 6-138. Y Parameter**

| CLKD      | Y                                            |
|-----------|----------------------------------------------|
| 1 or Even | 0.5                                          |
| Odd       | $(\text{trunc}[\text{CLKD}/2])/ \text{CLKD}$ |

For details about clock division factor CLKD, see the *AM35x ARM Microprocessor Technical Reference Manual* ([SPRUGR0](#)).

### 6.7.1.3 MMC/SD/SDIO in Standard MMC Mode and MMC Identification Mode

[Table 6-139](#) through [Table 6-141](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-139. MMC/SD/SDIO Timing Conditions Standard MMC Mode and MMC Identification Mode**

| TIMING CONDITION PARAMETER                    |                         | 1.8-V,3.3-V |     | UNIT |
|-----------------------------------------------|-------------------------|-------------|-----|------|
|                                               |                         | MIN         | MAX |      |
| Standard MMC Mode and MMC Identification Mode |                         |             |     |      |
| Input Conditions                              |                         |             |     |      |
| t <sub>r</sub>                                | Input signal rise time  | 0.19        | 10  | ns   |
| t <sub>f</sub>                                | Input signal fall time  | 0.19        | 10  | ns   |
| Output Conditions                             |                         |             |     |      |
| C <sub>LOAD</sub>                             | Output load capacitance | 30          |     | pF   |

**Table 6-140. MMC/SD/SDIO Timing Requirements Standard MMC Mode and MMC Identification Mode<sup>(1)(2)(3)</sup>**

| NO.                                           | PARAMETER                     |                                                               | 1.8 V |     | 3.3V |     | UNIT |
|-----------------------------------------------|-------------------------------|---------------------------------------------------------------|-------|-----|------|-----|------|
|                                               |                               |                                                               | MIN   | MAX | MIN  | MAX |      |
| Standard MMC Mode and MMC Identification Mode |                               |                                                               |       |     |      |     |      |
| MMC/SD/SDIO Interface 1                       |                               |                                                               |       |     |      |     |      |
| MMC3                                          | t <sub>su</sub> (CMDV-CLKIH)  | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge  | 2.13  |     | 2.41 |     | ns   |
| MMC4                                          | t <sub>h</sub> (CLKIH-CMDIV)  | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge    | 3.47  |     | 2.09 |     | ns   |
| MMC7                                          | t <sub>su</sub> (DATxV-CLKIH) | Setup time, mmc1_datx valid before mmc1_clk rising clock edge | 2.13  |     | 2.41 |     | ns   |
| MMC8                                          | t <sub>h</sub> (CLKIH-DATxIV) | Hold time, mmc1_datx valid after mmc1_clk rising clock edge   | 3.47  |     | 2.09 |     | ns   |
| MMC/SD/SDIO Interface 2                       |                               |                                                               |       |     |      |     |      |
| MMC3                                          | t <sub>su</sub> (CMDV-CLKIH)  | Setup time, mmc2_cmd valid before mmc2_clk rising clock edge  | 2.88  |     | 3.23 |     | ns   |
| MMC4                                          | t <sub>h</sub> (CLKIH-CMDIV)  | Hold time, mmc2_cmd valid after mmc2_clk rising clock edge    | 2.90  |     | 1.46 |     | ns   |
| MMC7                                          | t <sub>su</sub> (DATxV-CLKIH) | Setup time, mmc2_datx valid before mmc2_clk rising clock edge | 2.88  |     | 3.23 |     | ns   |
| MMC8                                          | t <sub>h</sub> (CLKIH-DATxIV) | Hold time, mmc2_datx valid after mmc2_clk rising clock edge   | 2.90  |     | 1.46 |     | ns   |
| MMC/SD/SDIO Interface 3                       |                               |                                                               |       |     |      |     |      |
| MMC3                                          | t <sub>su</sub> (CMDV-CLKIH)  | Setup time, mmc3_cmd valid before mmc3_clk rising clock edge  | 3.38  |     | 3.41 |     | ns   |
| MMC4                                          | t <sub>h</sub> (CLKIH-CMDIV)  | Hold time, mmc3_cmd valid after mmc3_clk rising clock edge    | 2.83  |     | 1.46 |     | ns   |
| MMC7                                          | t <sub>su</sub> (DATxV-CLKIH) | Setup time, mmc3_datx valid before mmc3_clk rising clock edge | 3.38  |     | 3.41 |     | ns   |
| MMC8                                          | t <sub>h</sub> (CLKIH-DATxIV) | Hold time, mmc3_datx valid after mmc3_clk rising clock edge   | 2.83  |     | 1.46 |     | ns   |

(1) Timing parameters are referred to output clock specified in [Table 6-141](#).

(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in [Table 6-141](#).

(3) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

**Table 6-141. MMC/SD/SDIO Switching Characteristics Standard MMC Mode and MMC Identification Mode<sup>(1)(2)</sup>**

| NO.                     | PARAMETER            |                                         | 1.8V, 3.3V                          |         | UNIT |
|-------------------------|----------------------|-----------------------------------------|-------------------------------------|---------|------|
|                         |                      |                                         | MIN                                 | MAX     |      |
| MMC Identification Mode |                      |                                         |                                     |         |      |
| MMC1                    | t <sub>c(clk)</sub>  | Cycle time                              |                                     | 2500    | ns   |
| MMC2                    | t <sub>W(clkH)</sub> | Typical pulse duration, output clk high | X <sup>(3)</sup> *PO <sup>(4)</sup> |         | ns   |
| MMC2                    | t <sub>W(clkL)</sub> | Typical pulse duration, output clk low  | Y <sup>(5)</sup> *PO <sup>(4)</sup> |         | ns   |
|                         | t <sub>dc(clk)</sub> | Duty cycle error, output clk            |                                     | 2604.17 | ns   |
|                         | t <sub>j(clk)</sub>  | Jitter standard deviation               |                                     | 200     | ps   |
| Standard MMC Mode       |                      |                                         |                                     |         |      |
| MMC1                    | t <sub>c(clk)</sub>  | Cycle time                              |                                     | 2500    | ns   |
| MMC2                    | t <sub>W(clkH)</sub> | Typical pulse duration, output clk high | X <sup>(3)</sup> *PO <sup>(4)</sup> |         | ns   |
| MMC2                    | t <sub>W(clkL)</sub> | Typical pulse duration, output clk low  | Y <sup>(5)</sup> *PO <sup>(4)</sup> |         | ns   |

(1) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The X parameter is defined as listed below.

(4) PO = output clk period in ns.

(5) The Y parameter is defined as listed below.

**Table 6-141. MMC/SD/SDIO Switching Characteristics Standard MMC Mode and MMC Identification Mode<sup>(1)(2)</sup> (continued)**

| NO.                            | PARAMETER         |                                                                | 1.8V, 3.3V |         | UNIT |
|--------------------------------|-------------------|----------------------------------------------------------------|------------|---------|------|
|                                |                   |                                                                | MIN        | MAX     |      |
|                                | $t_{dc}(clk)$     | Duty cycle error, output clk                                   |            | 2604.17 | ps   |
|                                | $t_j(clk)$        | Jitter standard deviation                                      |            | 200     | ps   |
| <b>MMC/SD/SDIO Interface 1</b> |                   |                                                                |            |         |      |
|                                | $t_r(clk)$        | Rise time, output clk                                          |            | 10      | ns   |
|                                | $t_f(clkH)$       | Fall time, output clk                                          |            | 10      | ns   |
|                                | $t_r(clkL)$       | Rise time, output data                                         |            | 10      | ns   |
|                                | $t_f(clk)$        | Fall time, output data                                         |            | 10      | ns   |
| MMC5                           | $t_d(CLKOH-CMD)$  | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition  | 4.3        | 47.78   | ns   |
| MMC6                           | $t_d(CLKOH-DATx)$ | Delay time, mmc1_clk rising clock edge to mmc1_datx transition | 4.3        | 47.78   | ns   |
| <b>MMC/SD/SDIO Interface 2</b> |                   |                                                                |            |         |      |
|                                | $t_r(clk)$        | Rise time, output clk                                          |            | 10      | ns   |
|                                | $t_f(clkH)$       | Fall time, output clk                                          |            | 10      | ns   |
|                                | $t_r(clkL)$       | Rise time, output data                                         |            | 10      | ns   |
|                                | $t_f(clk)$        | Fall time, output data                                         |            | 10      | ns   |
| MMC5                           | $t_d(CLKOH-CMD)$  | Delay time, mmc2_clk rising clock edge to mmc2_cmd transition  | 4.3        | 47.78   | ns   |
| MMC6                           | $t_d(CLKOH-DATx)$ | Delay time, mmc2_clk rising clock edge to mmc2_datx transition | 4.3        | 47.78   | ns   |
| <b>MMC/SD/SDIO Interface 3</b> |                   |                                                                |            |         |      |
|                                | $t_r(clk)$        | Rise time, output clk                                          |            | 10      | ns   |
|                                | $t_f(clkH)$       | Fall time, output clk                                          |            | 10      | ns   |
|                                | $t_r(clkL)$       | Rise time, output data                                         |            | 10      | ns   |
|                                | $t_f(clk)$        | Fall time, output data                                         |            | 10      | ns   |
| MMC5                           | $t_d(CLKOH-CMD)$  | Delay time, mmc3_clk rising clock edge to mmc3_cmd transition  | 4.3        | 47.78   | ns   |
| MMC6                           | $t_d(CLKOH-DATx)$ | Delay time, mmc3_clk rising clock edge to mmc3_datx transition | 4.3        | 47.78   | ns   |

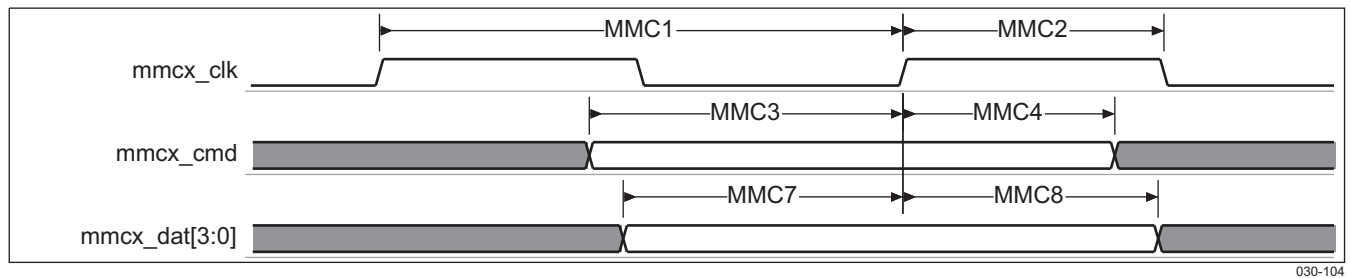
**Table 6-142. X Parameter**

| CLKD      | X                                             |
|-----------|-----------------------------------------------|
| 1 or Even | 0.5                                           |
| Odd       | $(\text{trunc}[\text{CLKD}/2]+1)/\text{CLKD}$ |

**Table 6-143. Y Parameter**

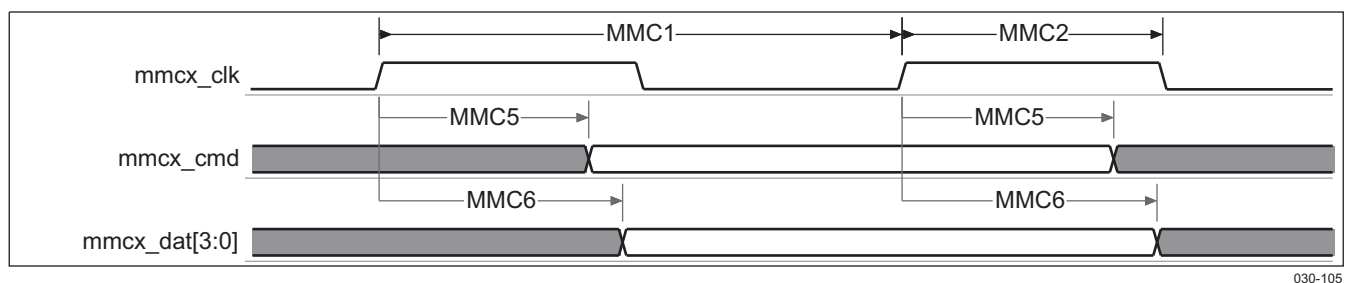
| CLKD      | Y                                            |
|-----------|----------------------------------------------|
| 1 or Even | 0.5                                          |
| Odd       | $(\text{trunc}[\text{CLKD}/2])/ \text{CLKD}$ |

For details about clock division factor CLKD, see the *AM35x ARM Microprocessor Technical Reference Manual* ([SPRUGR0](#)).



In mmc<sub>x</sub>, x is equal to 1, 2, or 3.

**Figure 6-66. MMC/SD/SDIO High-Speed and Standard MMC Modes Data/Command Receive**



In mmc<sub>x</sub>, x is equal to 1, 2, or 3.

**Figure 6-67. MMC/SD/SDIO High-Speed and Standard MMC Modes Data/Command Transmit**

#### 6.7.1.4 MMC/SD/SDIO in High-Speed SD Mode

[Table 6-144](#) through [Table 6-146](#) assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-144. MMC/SD/SDIO Timing Conditions High-Speed SD Mode**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V |     | UNIT |
|----------------------------|-------------------------|------------|-----|------|
|                            |                         | MIN        | MAX |      |
| High-Speed SD Mode         |                         |            |     |      |
| Input Conditions           |                         |            |     |      |
| t <sub>R</sub>             | Input signal rise time  | 0.19       | 3   | ns   |
| t <sub>F</sub>             | Input signal fall time  | 0.19       | 3   | ns   |
| Output Conditions          |                         |            |     |      |
| C <sub>LOAD</sub>          | Output load capacitance | 30         |     | pF   |

**Table 6-145. MMC/SD/SDIO Timing Requirements High-Speed SD Mode<sup>(1)(2)(3)</sup>**

| NO.                     | PARAMETER                    |                                                              | 1.8V, 3.3V |     | UNIT |
|-------------------------|------------------------------|--------------------------------------------------------------|------------|-----|------|
|                         |                              |                                                              | MIN        | MAX |      |
| High-Speed SD Mode      |                              |                                                              |            |     |      |
| MMC/SD/SDIO Interface 1 |                              |                                                              |            |     |      |
| HSSD3                   | t <sub>SU</sub> (CMDV-CLKIH) | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge | 5.61       |     | ns   |
| HSSD4                   | t <sub>H</sub> (CLKIH-CMDIV) | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge   | 2.28       |     | ns   |

(1) In dat<sub>x</sub>, x is equal to 1, 2, 3, 4, 5, 6, or 7.

(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in [Table 6-146](#).

(3) Timing Parameters refer to output clock specified in [Table 6-146](#).

**Table 6-145. MMC/SD/SDIO Timing Requirements High-Speed SD Mode<sup>(1)(2)(3)</sup> (continued)**

| NO.                            | PARAMETER             |                                                               | 1.8V, 3.3V |     | UNIT |
|--------------------------------|-----------------------|---------------------------------------------------------------|------------|-----|------|
|                                |                       |                                                               | MIN        | MAX |      |
| HSSD7                          | $t_{su}(DATxV-CLKIH)$ | Setup time, mmc1_datx valid before mmc1_clk rising clock edge | 5.61       |     | ns   |
| HSSD8                          | $t_h(CLKIH-DATxIV)$   | Hold time, mmc1_datx valid after mmc1_clk rising clock edge   | 2.28       |     | ns   |
| <b>MMC/SD/SDIO Interface 2</b> |                       |                                                               |            |     |      |
| HSSD3                          | $t_{su}(CMDV-CLKIH)$  | Setup time, mmc2_cmd valid before mmc2_clk rising clock edge  | 5.61       |     | ns   |
| HSSD4                          | $t_h(CLKIH-CMDIV)$    | Hold time, mmc2_cmd valid after mmc2_clk rising clock edge    | 2.28       |     | ns   |
| HSSD7                          | $t_{su}(DATxV-CLKIH)$ | Setup time, mmc2_datx valid before mmc2_clk rising clock edge | 5.61       |     | ns   |
| HSSD8                          | $t_h(CLKIH-DATxIV)$   | Hold time, mmc2_datx valid after mmc2_clk rising clock edge   | 2.28       |     | ns   |
| <b>MMC/SD/SDIO Interface 3</b> |                       |                                                               |            |     |      |
| HSSD3                          | $t_{su}(CMDV-CLKIH)$  | Setup time, mmc3_cmd valid before mmc3_clk rising clock edge  | 5.61       |     | ns   |
| HSSD4                          | $t_h(CLKIH-CMDIV)$    | Hold time, mmc3_cmd valid after mmc3_clk rising clock edge    | 2.28       |     | ns   |
| HSSD7                          | $t_{su}(DATxV-CLKIH)$ | Setup time, mmc3_datx valid before mmc3_clk rising clock edge | 5.61       |     | ns   |
| HSSD8                          | $t_h(CLKIH-DATxIV)$   | Hold time, mmc3_datx valid after mmc3_clk rising clock edge   | 2.28       |     | ns   |

**Table 6-146. MMC/SD/SDIO Switching Characteristics High-Speed SD Mode<sup>(1)(2)</sup>**

| NO.                     | PARAMETER                   |                                                                | 1.8 V, 3.3 V                        |         | UNIT |
|-------------------------|-----------------------------|----------------------------------------------------------------|-------------------------------------|---------|------|
|                         |                             |                                                                | MIN                                 | MAX     |      |
| High-Speed SD Mode      |                             |                                                                |                                     |         |      |
| HSSD1                   | t <sub>c</sub> (clk)        | Cycle time                                                     |                                     | 20.83   | ns   |
| HSSD2                   | t <sub>W</sub> (clkH)       | Typical pulse duration, output clk high                        | X <sup>(3)</sup> *PO <sup>(4)</sup> |         | ns   |
| HSSD2                   | t <sub>W</sub> (clkL)       | Typical pulse duration, output clk low                         | Y <sup>(5)</sup> *PO <sup>(4)</sup> |         | ns   |
|                         | t <sub>dc</sub> (clk)       | Duty cycle error, output clk                                   |                                     | 1041.67 | ps   |
|                         | t <sub>j</sub> (clk)        | Jitter standard deviation                                      |                                     | 200     | ps   |
| MMC/SD/SDIO Interface 1 |                             |                                                                |                                     |         |      |
|                         | t <sub>r</sub> (clk)        | Rise time, output clk                                          |                                     | 3       | ns   |
|                         | t <sub>f</sub> (clkH)       | Fall time, output clk                                          |                                     | 3       | ns   |
|                         | t <sub>r</sub> (clkL)       | Rise time, output data                                         |                                     | 3       | ns   |
|                         | t <sub>f</sub> (clk)        | Fall time, output data                                         |                                     | 3       | ns   |
| HSSD5                   | t <sub>d</sub> (CLKOH-CMD)  | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition  | 3.72                                | 14.11   | ns   |
| HSSD6                   | t <sub>d</sub> (CLKOH-DATx) | Delay time, mmc1_clk rising clock edge to mmc1_datx transition | 3.72                                | 14.11   | ns   |
| MMC/SD/SDIO Interface 2 |                             |                                                                |                                     |         |      |
|                         | t <sub>r</sub> (clk)        | Rise time, output clk                                          |                                     | 3       | ns   |
|                         | t <sub>f</sub> (clkH)       | Fall time, output clk                                          |                                     | 3       | ns   |
|                         | t <sub>r</sub> (clkL)       | Rise time, output data                                         |                                     | 3       | ns   |
|                         | t <sub>f</sub> (clk)        | Fall time, output data                                         |                                     | 3       | ns   |

(1) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

(2) The jitter probability density can be approximated by a Gaussian function.

(3) The X parameter is defined as listed in [Table 6-147](#).

(4) PO = output clk period in ns.

(5) The Y parameter is defined as listed in [Table 6-148](#).

**Table 6-146. MMC/SD/SDIO Switching Characteristics High-Speed SD Mode<sup>(1)(2)</sup> (continued)**

| NO.                            | PARAMETER           |                                                                | 1.8 V, 3.3 V |       | UNIT |
|--------------------------------|---------------------|----------------------------------------------------------------|--------------|-------|------|
|                                |                     |                                                                | MIN          | MAX   |      |
| HSSD5                          | $t_{d(CLKOH-CMD)}$  | Delay time, mmc2_clk rising clock edge to mmc2_cmd transition  | 3.72         | 14.11 | ns   |
| HSSD6                          | $t_{d(CLKOH-DATx)}$ | Delay time, mmc2_clk rising clock edge to mmc2_datx transition | 3.72         | 14.11 | ns   |
| <b>MMC/SD/SDIO Interface 3</b> |                     |                                                                |              |       |      |
|                                | $t_{r(clk)}$        | Rise time, output clk                                          |              | 3     | ns   |
|                                | $t_{f(clkH)}$       | Fall time, output clk                                          |              | 3     | ns   |
|                                | $t_{r(clkL)}$       | Rise time, output data                                         |              | 3     | ns   |
|                                | $t_{f(clk)}$        | Fall time, output data                                         |              | 3     | ns   |
| HSSD5                          | $t_{d(CLKOH-CMD)}$  | Delay time, mmc3_clk rising clock edge to mmc3_cmd transition  | 3.72         | 14.11 | ns   |
| HSSD6                          | $t_{d(CLKOH-DATx)}$ | Delay time, mmc3_clk rising clock edge to mmc3_datx transition | 3.72         | 14.11 | ns   |

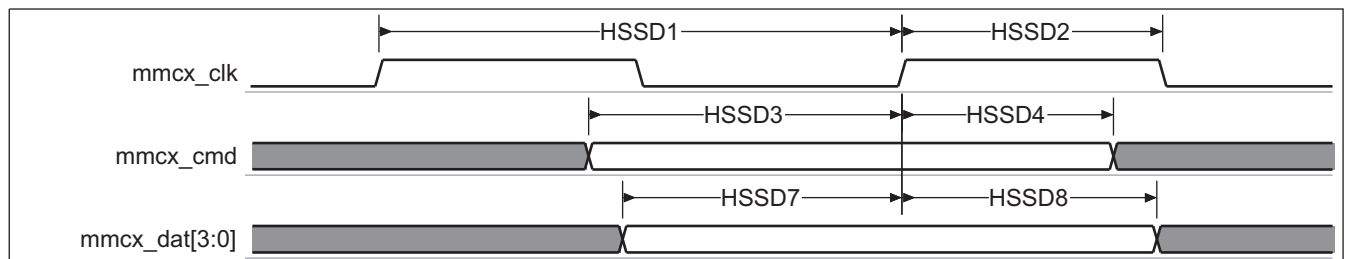
**Table 6-147. X Parameters**

| CLKD      | X                                             |
|-----------|-----------------------------------------------|
| 1 or Even | 0.5                                           |
| Odd       | $(\text{trunc}[\text{CLKD}/2]+1)/\text{CLKD}$ |

**Table 6-148. Y Parameters**

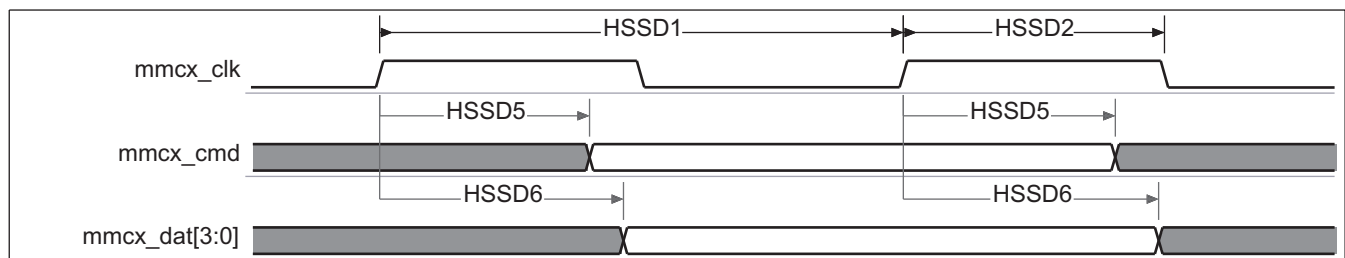
| CLKD      | Y                                            |
|-----------|----------------------------------------------|
| 1 or Even | 0.5                                          |
| Odd       | $(\text{trunc}[\text{CLKD}/2])/ \text{CLKD}$ |

For details about clock division factor CLKD, see the *AM35x ARM Microprocessor Technical Reference Manual* ([SPRUGR0](#)).



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In mmc\_x, x is equal to 1, 2, or 3.

**Figure 6-68. MMC/SD/SDIO High-Speed SD Mode Data/Command Receive**

030-107

In mmc\_x, x is equal to 1, 2, or 3.

**Figure 6-69. MMC/SD/SDIO High-Speed SD Mode Data/Command Transmit**

### 6.7.1.5 MMC/SD/SDIO in Standard SD Mode

Table 6-149 through Table 6-151 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-149. MMC/SD/SDIO Timing Conditions Standard SD Mode**

| TIMING CONDITION PARAMETER |                         | 1.8V, 3.3V |     | UNIT |
|----------------------------|-------------------------|------------|-----|------|
|                            |                         | MIN        | MAX |      |
| Standard SD Mode           |                         |            |     |      |
| Input Conditions           |                         |            |     |      |
| t <sub>R</sub>             | Input signal rise time  | 0.19       | 10  | ns   |
| t <sub>F</sub>             | Input signal fall time  | 0.19       | 10  | ns   |
| Output Conditions          |                         |            |     |      |
| C <sub>LOAD</sub>          | Output load capacitance | 30         |     | pF   |

**Table 6-150. MMC/SD/SDIO Timing Requirements Standard SD Mode<sup>(1)(2)(3)</sup>**

| NO.                     | PARAMETER                     |                                                               | 1.8 V, 3.3V |     | UNIT |
|-------------------------|-------------------------------|---------------------------------------------------------------|-------------|-----|------|
|                         |                               |                                                               | MIN         | MAX |      |
| Standard SD Mode        |                               |                                                               |             |     |      |
| MMC/SD/SDIO Interface 1 |                               |                                                               |             |     |      |
| SD3                     | t <sub>su</sub> (CMDV-CLKIH)  | Setup time, mmc1_cmd valid before mmc1_clk rising clock edge  | 6.23        |     | ns   |
| SD4                     | t <sub>h</sub> (CLKIH-CMDIV)  | Hold time, mmc1_cmd valid after mmc1_clk rising clock edge    | 19.37       |     | ns   |
| SD7                     | t <sub>su</sub> (DATxV-CLKIH) | Setup time, mmc1_datx valid before mmc1_clk rising clock edge | 6.23        |     | ns   |
| SD8                     | t <sub>h</sub> (CLKIH-DATxIV) | Hold time, mmc1_datx valid after mmc1_clk rising clock edge   | 19.37       |     | ns   |
| MMC/SD/SDIO Interface 2 |                               |                                                               |             |     |      |
| SD3                     | t <sub>su</sub> (CMDV-CLKIH)  | Setup time, mmc2_cmd valid before mmc2_clk rising clock edge  | 6.23        |     | ns   |
| SD4                     | t <sub>h</sub> (CLKIH-CMDIV)  | Hold time, mmc2_cmd valid after mmc2_clk rising clock edge    | 19.37       |     | ns   |
| SD7                     | t <sub>su</sub> (DATxV-CLKIH) | Setup time, mmc2_datx valid before mmc2_clk rising clock edge | 6.23        |     | ns   |
| SD8                     | t <sub>h</sub> (CLKIH-DATxIV) | Hold time, mmc2_datx valid after mmc2_clk rising clock edge   | 19.37       |     | ns   |
| MMC/SD/SDIO Interface 3 |                               |                                                               |             |     |      |
| SD3                     | t <sub>su</sub> (CMDV-CLKIH)  | Setup time, mmc3_cmd valid before mmc3_clk rising clock edge  | 6.23        |     | ns   |
| SD4                     | t <sub>h</sub> (CLKIH-CMDIV)  | Hold time, mmc3_cmd valid after mmc3_clk rising clock edge    | 19.37       |     | ns   |
| SD7                     | t <sub>su</sub> (DATxV-CLKIH) | Setup time, mmc3_datx valid before mmc3_clk rising clock edge | 6.23        |     | ns   |
| SD8                     | t <sub>h</sub> (CLKIH-DATxIV) | Hold time, mmc3_datx valid after mmc3_clk rising clock edge   | 19.37       |     | ns   |

(1) Timing parameters refer to output clock specified in [Table 6-151](#).(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified in [Table 6-151](#).

(3) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

**Table 6-151. MMC/SD/SDIO Switching Characteristics Standard SD Mode<sup>(1)(2)</sup>**

| NO.                     | PARAMETER            |                                         | 1.8V, 3.3V                          |         | UNIT |
|-------------------------|----------------------|-----------------------------------------|-------------------------------------|---------|------|
|                         |                      |                                         | MIN                                 | MAX     |      |
| Standard SD Mode        |                      |                                         |                                     |         |      |
| SD1                     | t <sub>C(clk)</sub>  | Cycle time                              |                                     | 41.67   | ns   |
| SD2                     | t <sub>W(clkH)</sub> | Typical pulse duration, output clk high | X <sup>(3)</sup> *PO <sup>(4)</sup> |         | ns   |
| SD2                     | t <sub>W(clkL)</sub> | Typical pulse duration, output clk low  | Y <sup>(5)</sup> *PO <sup>(4)</sup> |         | ns   |
|                         | t <sub>dC(clk)</sub> | Duty cycle error, output clk            |                                     | 2083.33 | ps   |
|                         | t <sub>j(clk)</sub>  | Jitter standard deviation               |                                     | 200     | ps   |
| MMC/SD/SDIO Interface 1 |                      |                                         |                                     |         |      |
|                         | t <sub>r(clk)</sub>  | Rise time, output clk                   |                                     | 10      | ns   |
|                         | t <sub>f(clkH)</sub> | Fall time, output clk                   |                                     | 10      | ns   |
|                         | t <sub>r(clkL)</sub> | Rise time, output data                  |                                     | 10      | ns   |
|                         | t <sub>f(clk)</sub>  | Fall time, output data                  |                                     | 10      | ns   |

(1) The jitter probability density can be approximated by a Gaussian function.

(2) In datx, x is equal to 1, 2, 3, 4, 5, 6, or 7.

(3) The X parameter is defined as listed in [Table 6-152](#).

(4) PO = output clk period in ns.

(5) The Y parameter is defined as listed in [Table 6-153](#).

**Table 6-151. MMC/SD/SDIO Switching Characteristics Standard SD Mode<sup>(1)(2)</sup> (continued)**

| NO.                            | PARAMETER           |                                                                | 1.8V, 3.3V |       | UNIT |
|--------------------------------|---------------------|----------------------------------------------------------------|------------|-------|------|
|                                |                     |                                                                | MIN        | MAX   |      |
| SD5                            | $t_{d(CLKOH-CMD)}$  | Delay time, mmc1_clk rising clock edge to mmc1_cmd transition  | 6.13       | 35.53 | ns   |
| SD6                            | $t_{d(CLKOH-DATx)}$ | Delay time, mmc1_clk rising clock edge to mmc1_datx transition | 6.13       | 35.53 | ns   |
| <b>MMC/SD/SDIO Interface 2</b> |                     |                                                                |            |       |      |
|                                | $t_{r(clk)}$        | Rise time, output clk                                          |            | 10    | ns   |
|                                | $t_{f(clkH)}$       | Fall time, output clk                                          |            | 10    | ns   |
|                                | $t_{r(clkL)}$       | Rise time, output data                                         |            | 10    | ns   |
|                                | $t_{f(clk)}$        | Fall time, output data                                         |            | 10    | ns   |
| SD5                            | $t_{d(CLKOH-CMD)}$  | Delay time, mmc2_clk rising clock edge to mmc2_cmd transition  | 6.13       | 35.53 | ns   |
| SD6                            | $t_{d(CLKOH-DATx)}$ | Delay time, mmc2_clk rising clock edge to mmc2_datx transition | 6.13       | 35.53 | ns   |
| <b>MMC/SD/SDIO Interface 3</b> |                     |                                                                |            |       |      |
|                                | $t_{r(clk)}$        | Rise time, output clk                                          |            | 10    | ns   |
|                                | $t_{f(clkH)}$       | Fall time, output clk                                          |            | 10    | ns   |
|                                | $t_{r(clkL)}$       | Rise time, output data                                         |            | 10    | ns   |
|                                | $t_{f(clk)}$        | Fall time, output data                                         |            | 10    | ns   |
| SD5                            | $t_{d(CLKOH-CMD)}$  | Delay time, mmc3_clk rising clock edge to mmc3_cmd transition  | 6.13       | 35.53 | ns   |
| SD6                            | $t_{d(CLKOH-DATx)}$ | Delay time, mmc3_clk rising clock edge to mmc3_datx transition | 6.13       | 35.53 | ns   |

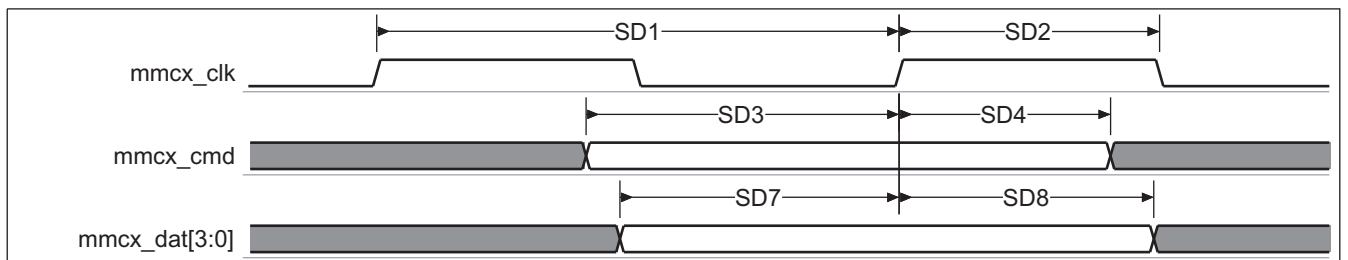
**Table 6-152. X Parameter**

| CLKD      | X                                             |
|-----------|-----------------------------------------------|
| 1 or Even | 0.5                                           |
| Odd       | $(\text{trunc}[\text{CLKD}/2]+1)/\text{CLKD}$ |

**Table 6-153. Y Parameter**

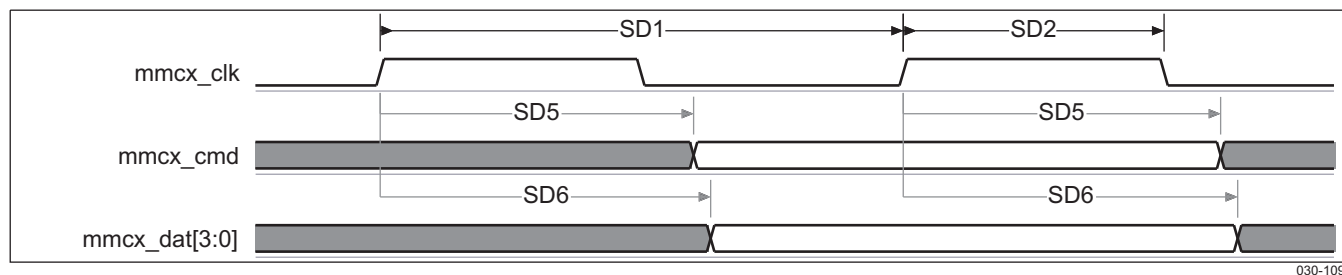
| CLKD      | Y                                            |
|-----------|----------------------------------------------|
| 1 or Even | 0.5                                          |
| Odd       | $(\text{trunc}[\text{CLKD}/2])/ \text{CLKD}$ |

For details about clock division factor CLKD, see the *AM35x ARM Microprocessor Technical Reference Manual* ([SPRUGR0](#)).



In mmc\_x, x is equal to 1, 2, or 3.

**Figure 6-70. MMC/SD/SDIO Standard SD Mode Data/Command Receive**



In mmc\_x, x is equal to 1, 2, or 3.

**Figure 6-71. MMC/SD/SDIO Standard SD Mode Data/Command Transmit**

## 6.8 Test Interfaces

The emulation and trace interfaces allow tracing activities of the following CPUs:

- ARM Cortex™-A8 through an Embedded Trace Macro-cell (ETM11) dedicated to enable real-time trace of the ARM subsystem operations.

All processors can be emulated via JTAG ports.

### 6.8.1 Embedded Trace Macro Interface (ETM)

Table 6-154 assumes testing over the recommended operating conditions.

**Table 6-154. Embedded Trace Macro Interface Switching Characteristics**

| NO.  | PARAMETER        |                                                          | MIN  | MAX | UNIT |
|------|------------------|----------------------------------------------------------|------|-----|------|
| f    | $1/t_{c(CLK)}$   | Frequency, etk_clk                                       |      | 166 | MHz  |
| ETM0 | $t_{c(CLK)}$     | Cycle time                                               | 6.02 |     | ns   |
| ETM1 | $t_{w(CLK)}$     | Clock pulse width, etk_clk                               | 3.01 |     | ns   |
| ETM2 | $t_{d(CLK-CTL)}$ | Delay time, etk_clk clock edge to etk_ctl transition     | -0.5 | 0.5 | ns   |
| ETM3 | $t_{d(CLK-D)}$   | Delay time, etk_clk clock high to etk_d[15:0] transition | -0.5 | 0.5 | ns   |

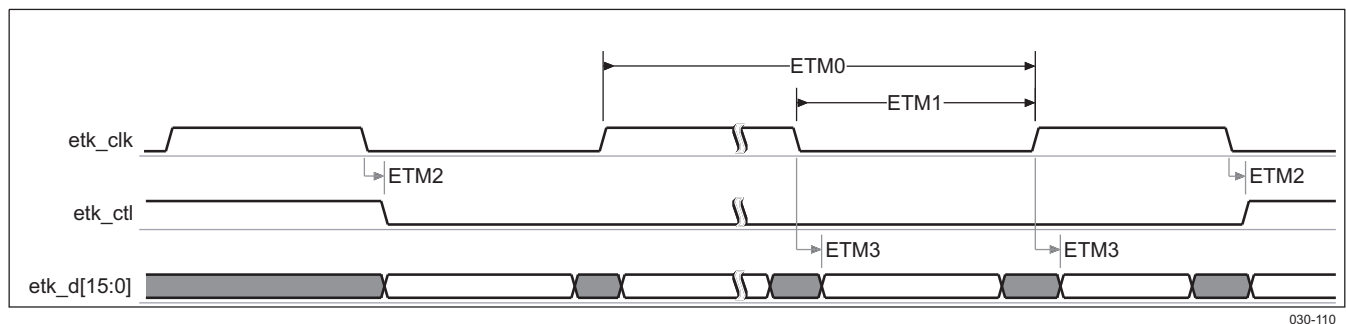


**Figure 6-72. Embedded Trace Macro Interface**

### 6.8.2 JTAG Interfaces

AM3517/05 JTAG TAP controller handles standard IEEE JTAG interfaces. The following sections define the timing requirements for several tools used to test the AM3517/05 processors as:

- Free running clock tool, like XDS560 and XDS510 tools
- Adaptive clock tool, like RealView ICE tool and Lauterbach tool

#### 6.8.2.1 JTAG Free Running Clock Mode

Table 6-155 through Table 6-157 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-155. JTAG Timing Conditions Free Running Clock Mode**

| TIMING CONDITION PARAMETER |                         | 1.8 V | 3.3 V | UNIT |
|----------------------------|-------------------------|-------|-------|------|
|                            |                         | MAX   | MAX   |      |
| Input Conditions           |                         |       |       |      |
| t <sub>R</sub>             | Input signal rise time  | 5     | 3     | ns   |
| t <sub>F</sub>             | Input signal fall time  | 5     | 3     | ns   |
| Output Conditions          |                         |       |       |      |
| C <sub>LOAD</sub>          | Output load capacitance | 30    |       | pF   |

**Table 6-156. JTAG Timing Requirements Free Running Clock Mode<sup>(1)(2)(3)</sup>**

| NO.  | PARAMETER             |                                                  | 1.8V  |      | 3.3V  |      | UNIT |
|------|-----------------------|--------------------------------------------------|-------|------|-------|------|------|
|      |                       |                                                  | MIN   | MAX  | MIN   | MAX  |      |
| JT4  | $t_{c(tck)}$          | Cycle time                                       | 20    |      | 20    |      | ns   |
| JT5  | $t_{w(tckL)}$         | Typical pulse duration, jtag_tck low             | 10    |      | 10    |      | ns   |
| JT6  | $t_{w(tckH)}$         | Typical pulse duration, jtag_tck high            | 10    |      | 10    |      | ns   |
|      | $t_{dc(tck)}$         | Duty cycle error, jtag_tck                       | -1250 | 1250 | -1250 | 1250 | ps   |
|      | $t_{j(tck)}$          | Cycle jitter                                     | -1250 | 1250 | -1250 | 1250 | ps   |
| JT7  | $t_{su(tdiV-rtckH)}$  | Setup time, jtag_tdi valid before jtag_rtck high | 1.8   |      | 3.8   |      | ns   |
| JT8  | $t_{h(tdiV-rtckH)}$   | Hold time, jtag_tdi valid after jtag_rtck high   | 0.7   |      | 2.7   |      | ns   |
| JT9  | $t_{su(tmsV-rtckH)}$  | Setup time, jtag_tms valid before jtag_rtck high | 1.8   |      | 3.8   |      | ns   |
| JT10 | $t_{h(tmsV-rtckH)}$   | Hold time, jtag_tms valid after jtag_rtck high   | 0.7   |      | 2.7   |      | ns   |
| JT12 | $t_{su(emuxV-rtckH)}$ | Setup time, jtag_emux                            | 14.6  |      | 14.6  |      | ns   |
| JT13 | $t_{h(emuxV-rtckH)}$  | Hold time, jtag_emux                             | 2     |      | 2     |      | ns   |

(1) Maximum cycle jitter supported by jtag\_tck input clock.

(2) x = 0 to 1

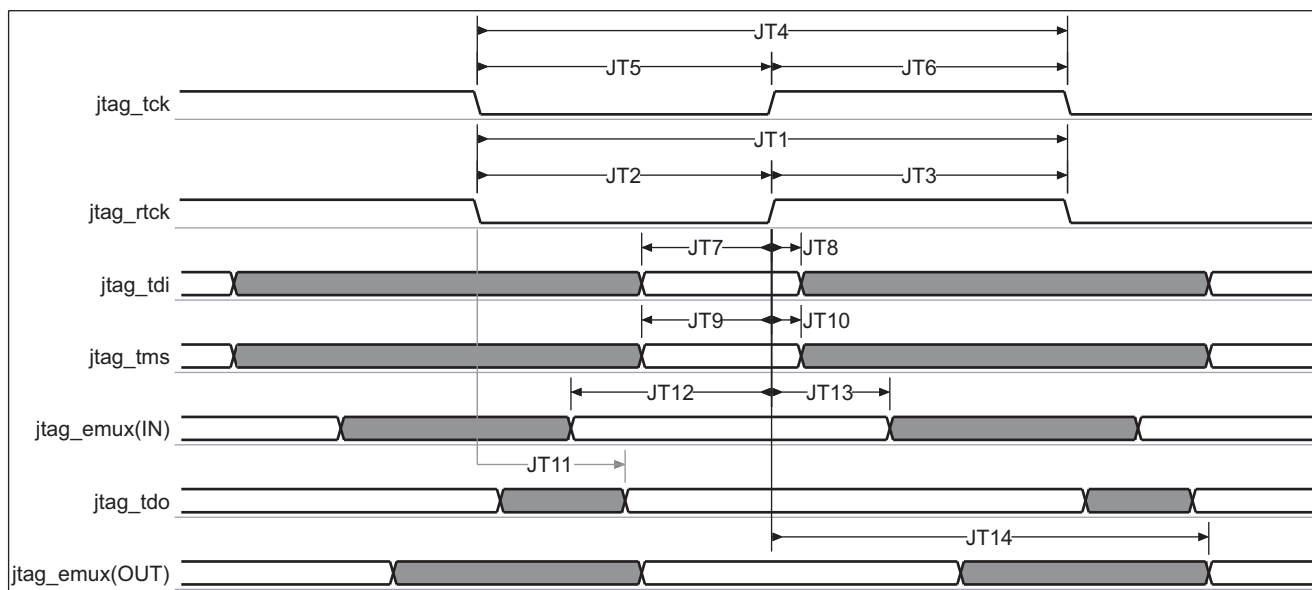
(3) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

**Table 6-157. JTAG Switching Characteristics Free Running Clock Mode<sup>(1)(2)</sup>**

| NO.  | PARAMETER            |                                                      | 1.8 V |       | 3.3 V |       | UNIT |
|------|----------------------|------------------------------------------------------|-------|-------|-------|-------|------|
|      |                      |                                                      | MIN   | MAX   | MIN   | MAX   |      |
| JT1  | $t_{c(rtck)}$        | Cycle time <sup>(1)</sup> , jtag_rtck period         | 20    |       | 20    |       | ns   |
| JT2  | $t_{w(rtckL)}$       | Typical pulse duration, jtag_rtck low                | 10    |       | 10    |       | ns   |
| JT3  | $t_{w(rtckH)}$       | Typical pulse duration, jtag_rtck high               | 10    |       | 10    |       | ns   |
|      | $t_{dc(rtck)}$       | Duty cycle error, jtag_rtck                          | -1250 | 1250  | -1250 | 1250  | ps   |
|      | $t_{j(rtck)}$        | Jitter standard deviation <sup>(2)</sup> , jtag_rtck |       | 33.33 |       | 33.33 | ps   |
|      | $t_{R(rtck)}$        | Rise time, jtag_rtck                                 |       | 4     |       | 4     | ns   |
|      | $t_{F(rtck)}$        | Fall time, jtag_rtck                                 |       | 4     |       | 4     | ns   |
| JT11 | $t_{d(rtckL-tdoV)}$  | Delay time, jtag_rtck low to jtag_tdo valid          | -5.8  | 5.8   | -8    | 8     | ns   |
|      | $t_{R(tdo)}$         | Rise time, jtag_tdo                                  |       | 4     |       | 4     | ns   |
|      | $t_{F(tdo)}$         | Fall time, jtag_tdo                                  |       | 4     |       | 4     | ns   |
| JT14 | $t_{d(rtckH-emuxV)}$ | Delay time, jtag_rtck high to jtag_emux              | 2.7   | 15.1  | 2.7   | 15.1  | ns   |
|      | $t_{R(emux)}$        | Rise time, jtag_emux                                 |       | 6     |       | 6     | ns   |
|      | $t_{F(emux)}$        | Fall time, jtag_emux                                 |       | 6     |       | 6     | ns   |

(1) Related with the jtag\_rtck maximum frequency.

(2) The jitter probability density can be approximated by a Gaussian function.



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In jtag\_emux, x is equal to 0 to 1.

**Figure 6-73. JTAG Interface Timing Free Running Clock Mode**

### 6.8.2.2 JTAG Adaptive Clock Mode

Table 6-158 through Table 6-160 assume testing over the recommended operating conditions and electrical characteristic conditions.

**Table 6-158. JTAG Timing Conditions Adaptive Clock Mode**

| TIMING CONDITION PARAMETER |                         | 1.8 V | 3.3 V | UNIT |
|----------------------------|-------------------------|-------|-------|------|
|                            |                         | MAX   | MAX   |      |
| Input Conditions           |                         |       |       |      |
| t <sub>R</sub>             | Input signal rise time  | 5     | 3     | ns   |
| t <sub>F</sub>             | Input signal fall time  | 5     | 3     | ns   |
| Output Conditions          |                         |       |       |      |
| C <sub>LOAD</sub>          | Output load capacitance |       | 30    | pF   |

**Table 6-159. JTAG Timing Requirements Adaptive Clock Mode<sup>(1)(2)</sup>**

| NO.  | PARAMETER           |                                                 | 1.8 V |      | 3.3 V |      | UNIT |
|------|---------------------|-------------------------------------------------|-------|------|-------|------|------|
|      |                     |                                                 | MIN   | MAX  | MIN   | MAX  |      |
| JA4  | $t_{c(tck)}$        | Cycle time                                      | 20    |      | 20    |      | ns   |
| JA5  | $t_{w(tckL)}$       | Typical pulse duration, jtag_tck low            | 10    |      | 10    |      | ns   |
| JA6  | $t_{w(tckH)}$       | Typical pulse duration, jtag_tck high           | 10    |      | 10    |      | ns   |
|      | $t_{dc(lclk)}$      | Duty cycle error, jtag_tck                      | -2500 | 2500 | -2500 | 2500 | ps   |
|      | $t_{j(lclk)}$       | Cycle jitter                                    | -1500 | 1500 | -1500 | 1500 | ps   |
| JA7  | $t_{su(tdiV-tckH)}$ | Setup time, jtag_tdi valid before jtag_tck high | 13.8  |      | 13.8  |      | ns   |
| JA8  | $t_{h(tdiV-tckH)}$  | Hold time, jtag_tdi valid after jtag_tck high   | 13.8  |      | 13.8  |      | ns   |
| JA9  | $t_{su(tmsV-tckH)}$ | Setup time, jtag_tms valid before jtag_tck high | 13.8  |      | 13.8  |      | ns   |
| JA10 | $t_{h(tmsV-tckH)}$  | Hold time, jtag_tms valid after jtag_tck high   | 13.8  |      | 13.8  |      | ns   |

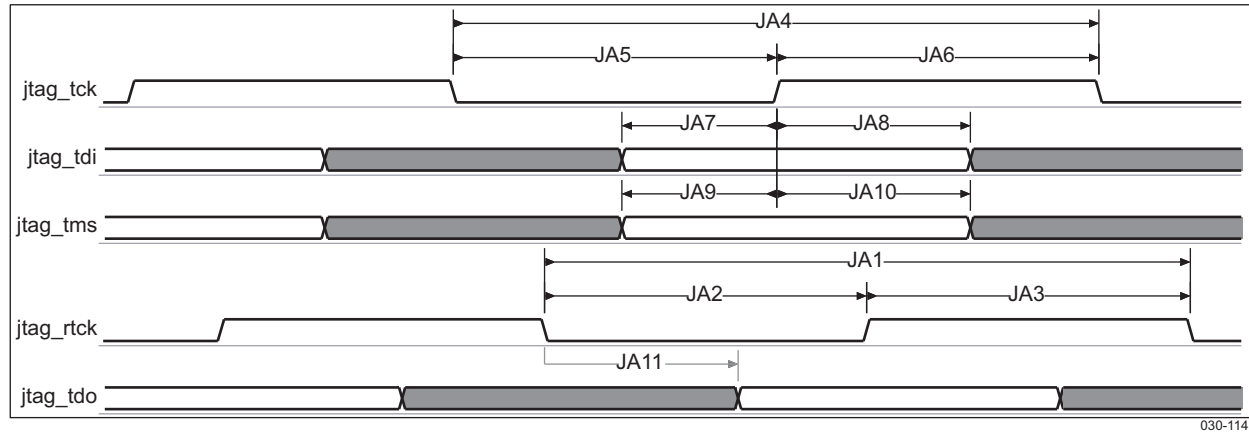
(1) Maximum cycle jitter supported by jtag\_tck input clock.

(2) The timing requirements are assured for the cycle jitter and duty cycle error conditions specified.

**Table 6-160. JTAG Switching Characteristics Adaptive Clock Mode<sup>(1)</sup>**

| NO.  | PARAMETER                                                       | 1.8 V |       | 3.3 V |       | UNIT |
|------|-----------------------------------------------------------------|-------|-------|-------|-------|------|
|      |                                                                 | MIN   | MAX   | MIN   | MAX   |      |
| JA1  | $t_{c(rtck)}$ Cycle time                                        | 20    |       | 20    |       | ns   |
| JA2  | $t_{w(rtckL)}$ Typical pulse duration, jtag_rtck low            | 10    |       | 10    |       | ns   |
| JA3  | $t_{w(rtckH)}$ Typical pulse duration, jtag_rtck high           | 10    |       | 10    |       | ns   |
|      | $t_{dc(rtck)}$ Duty cycle error, jtag_rtck                      | -2500 | 2500  | -2500 | 2500  | ps   |
|      | $t_{j(rtck)}$ Jitter standard deviation                         |       | 33.33 |       | 33.33 | ps   |
|      | $t_{R(rtck)}$ Rise time, jtag_rtck                              |       | 4     |       | 4     | ns   |
|      | $t_{F(rtck)}$ Fall time, jtag_rtck                              |       | 4     |       | 4     | ns   |
| JA11 | $t_{d(rtckL-tdoV)}$ Delay time, jtag_rtck low to jtag_tdo valid | -14.6 | 14.6  | -14.6 | 14.6  | ns   |
|      | $t_{R(tdo)}$ Rise time, jtag_tdo,                               |       | 4     |       | 4     | ns   |
|      | $t_{F(tdo)}$ Fall time, jtag_tdo                                |       | 4     |       | 4     | ns   |

(1) The jitter probability density can be approximated by a Gaussian function.

**Figure 6-74. JTAG Interface Timing Adaptive Clock Mode**

## 7 Device and Documentation Support

### 7.1 Device Support

#### 7.1.1 Development Support

TI offers an extensive line of development tools, including tools to evaluate the performance of the processors, generate code, develop algorithm implementations, and fully integrate and debug software and hardware modules. The tool's support documentation is electronically available within the Code Composer Studio™ Integrated Development Environment (IDE).

##### 7.1.1.1 Getting Started and Next Steps

The following products support development of the AM3517/05 device applications:

##### Software Development Tools:

- Code Composer Studio™ Integrated Development Environment (IDE) for Sitara ARM Processors: an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.
- FlashTool for AM35x, AM37x, DM37x and OMAP35x Devices: a Windows-based application that can be used to transfer binary images from a host PC to TI Sitara AM35x, AM37x, DM37x and OMAP35x target platforms.
- Pin Mux Utility for ARM Microprocessors: a Windows-based software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI ARM MPUs.
- Power Estimation Tool (PET): provides users the ability to gain insight in to the power consumption of select Sitara and OMAP processors.

##### Hardware Development Tools:

- Uniflash Standalone Flash Tool for TI Microcontrollers (MCUs) and Sitara Processors: a standalone tool used to program on-chip flash memory on TI MCUs and on-board flash memory for Sitara processors.
- XDS200 Price/Performance-balanced Debug Probe: a JTAG emulator for TI embedded processors.
- XDS560 High Performance Debug Probe: combines state-of-the-art silicon, hardware, and software technology to provide the best hardware debug capabilities.

For a complete listing of development-support tools for the AM3517/05 platform, visit the Texas Instruments website at [www.ti.com](http://www.ti.com). For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

#### 7.1.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all AM3517/05 processors and support tools. Each device has one of three prefixes: X, P, or null (no prefix). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices/tools (TMDS).

Device development evolutionary flow:

|             |                                                                                                                                                                      |
|-------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>X</b>    | Experimental device that is not necessarily representative of the final devices electrical specifications and may not use production assembly flow. (TMX definition) |
| <b>P</b>    | Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications. (TMP definition)                        |
| <b>null</b> | Production version of the silicon die that is fully qualified. (TMS definition)                                                                                      |

Support tool development evolutionary flow:

**TMDX** Development support product that has not yet completed Texas Instruments internal qualification testing.

**TMDS** Fully qualified development support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

Developmental product is intended for internal evaluation purposes.

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P), have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For additional description of the device nomenclature markings, see the *AM35x ARM Microprocessor Silicon Errata* ([SPRZ306](#)).

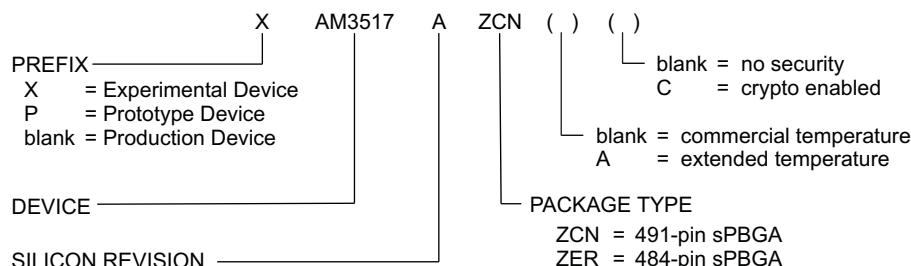


**Figure 7-1. Device Nomenclature**

## 7.2 Documentation Support

### 7.2.1 Related Documentation

The following documents describe the AM3517/05 device. Copies of these documents are available on the Internet at [www.ti.com](http://www.ti.com). Tip: Enter the literature number in the search box provided at [www.ti.com](http://www.ti.com).

The current documentation that describes the AM3517/05 Sitara processor, related peripherals, and other technical collateral, is available in the product folder at: [www.ti.com](http://www.ti.com).

**[SPRUGR0](#) AM35x ARM Microprocessor Technical Reference Manual.** Collection of documents providing detailed information on the Sitara architecture including power, reset, and clock control, interrupts, memory map, and switch fabric interconnect. Detailed information on the microprocessor unit (MPU) subsystem as well a functional description of the peripherals supported on AM3517/05 devices is also included.

The following documents are related to the AM3517/05 device. Copies of these documents can be obtained directly from the internet or from your Texas Instruments representative.

**Cortex-A8 Technical Reference Manual.** This is the technical reference manual for the Cortex-A8 processor. A copy of this document can be obtained via the internet at <http://infocenter.arm.com>. See the *AM35x ARM Microprocessor Silicon Errata* ([SPRZ306](#)) to determine the revision of the Cortex-A8 core used on your device.

**ARM Core Cortex™-A8 (AT400/AT401) Errata Notice.** Provides a list of advisories for the different revisions of the Cortex-A8 processor. Contact your TI representative for a copy of this document. See the *AM35x ARM Microprocessor Silicon Errata* ([SPRZ306](#)) to determine the revision of the Cortex-A8 core used on your device.

## 7.3 Related Links

[Table 7-1](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 7-1. Related Links**

| PARTS  | PRODUCT FOLDER             | SAMPLE & BUY               | TECHNICAL DOCUMENTS        | TOOLS & SOFTWARE           | SUPPORT & COMMUNITY        |
|--------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| AM3517 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |
| AM3505 | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> | <a href="#">Click here</a> |

## 7.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Online Community](#) *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#) *Texas Instruments Embedded Processors Wiki*. Established to help developers get started with Embedded Processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

## 7.5 Trademarks

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NEON is a trademark of ARM Ltd or its subsidiaries.  
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All other trademarks are the property of their respective owners.

## 7.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8 Mechanical Packaging and Orderable Information

### 8.1 Package Option Addendum

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2)            | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| AM3505AZCN       | ACTIVE        | NFBGA        | ZCN                | 491  | 90             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | 0 to 90      | AM3505AZCN<br>532       | <a href="#">Samples</a> |
| AM3505AZCNA      | ACTIVE        | NFBGA        | ZCN                | 491  | 90             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -40 to 105   | AM3505AZCNA<br>532      | <a href="#">Samples</a> |
| AM3505AZCNAC     | ACTIVE        | NFBGA        | ZCN                | 491  | 90             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -40 to 105   | AM3505AZCNAC<br>532     | <a href="#">Samples</a> |
| AM3505AZCNC      | ACTIVE        | NFBGA        | ZCN                | 491  | 90             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | 0 to 90      | AM3505AZCNC<br>532      | <a href="#">Samples</a> |
| AM3505AZER       | ACTIVE        | BGA          | ZER                | 484  | 60             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | 0 to 90      | AM3505AZER<br>532       | <a href="#">Samples</a> |
| AM3505AZERA      | ACTIVE        | BGA          | ZER                | 484  | 60             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -40 to 105   | AM3505AZERA<br>532      | <a href="#">Samples</a> |
| AM3517AZCN       | ACTIVE        | NFBGA        | ZCN                | 491  | 90             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | 0 to 90      | AM3517AZCN<br>532       | <a href="#">Samples</a> |
| AM3517AZCNA      | ACTIVE        | NFBGA        | ZCN                | 491  | 90             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -40 to 105   | AM3517AZCNA<br>532      | <a href="#">Samples</a> |
| AM3517AZCNAC     | ACTIVE        | NFBGA        | ZCN                | 491  | 90             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -40 to 105   | AM3517AZCNAC<br>532     | <a href="#">Samples</a> |
| AM3517AZER       | ACTIVE        | BGA          | ZER                | 484  | 60             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | 0 to 90      | AM3517AZER<br>532       | <a href="#">Samples</a> |
| AM3517AZERA      | ACTIVE        | BGA          | ZER                | 484  | 60             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | -40 to 105   | AM3517AZERA<br>532      | <a href="#">Samples</a> |
| AM3517AZERC      | ACTIVE        | BGA          | ZER                | 484  | 60             | Green (RoHS<br>& no Sb/Br) | SNAGCU                  | Level-3-260C-168 HR  | 0 to 90      | AM3517AZERC<br>532      | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

---

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

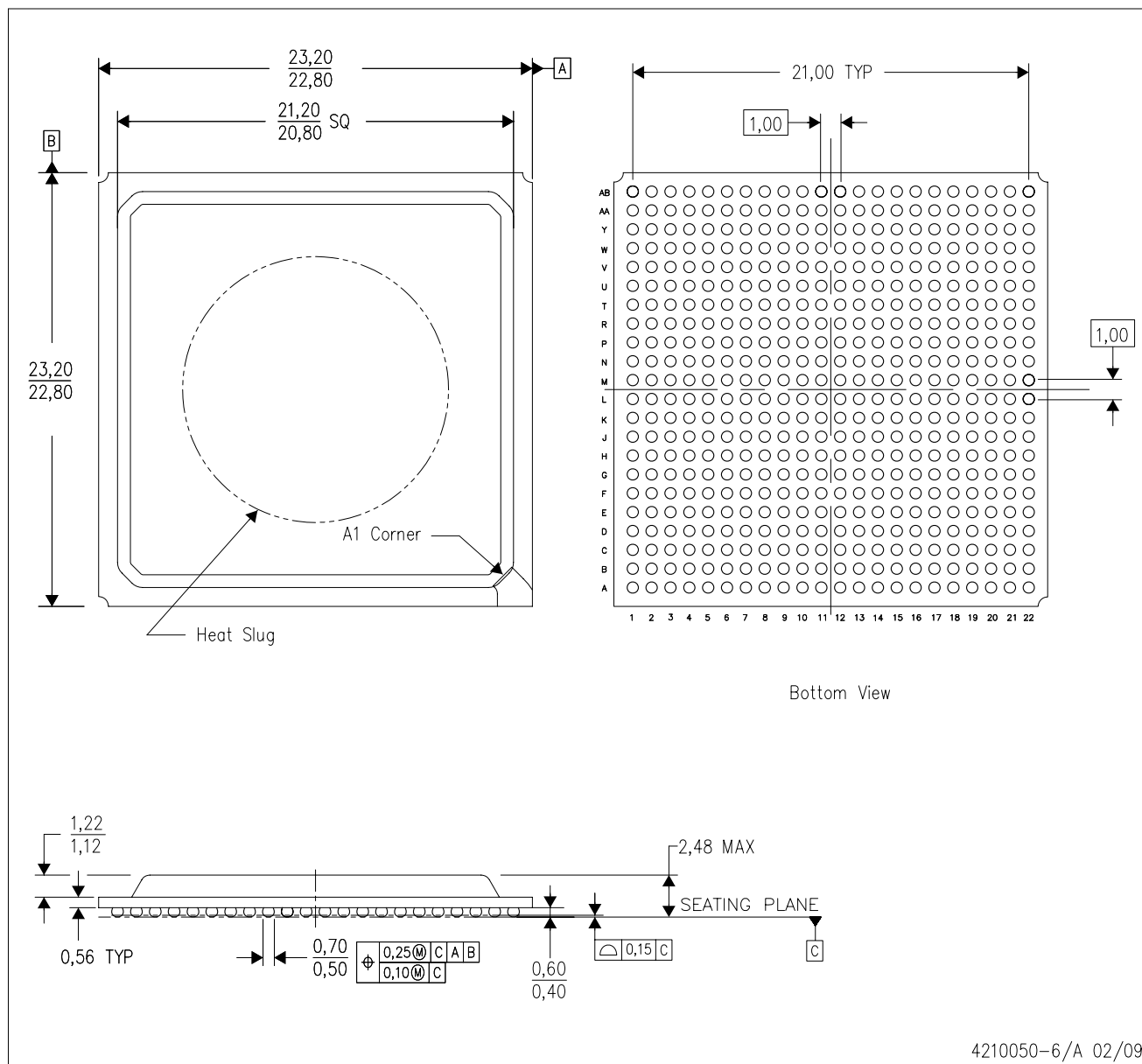
<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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ZER (S-PBGA-N484)

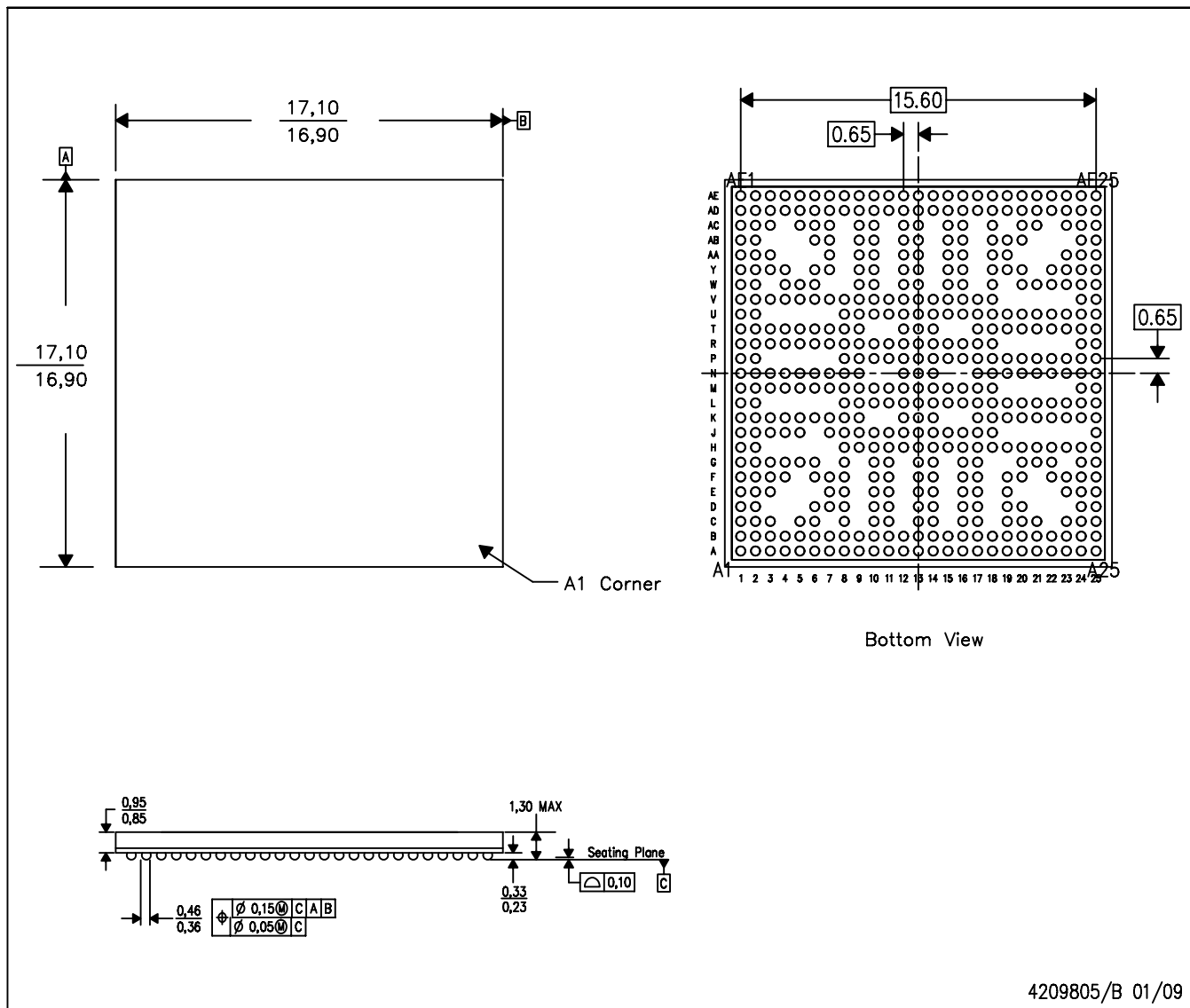
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MO-151
  - D. Thermally enhanced molded plastic package with heat slug (HSL).
  - E. This is a Pb-free solder ball design.

ZCN (S-PBGA-N491)

PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. nFBGA package configuration.
  - D. This is a Pb-free solder ball design.

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