



AK4432

108dB 192kHz 32bit 2-Channel Audio DAC

1. General Description

The AK4432 is a 32-bit Stereo DAC which corresponds to digital audio systems. An internal circuit includes newly developed 32-bit Digital Filter achieving short group delay and high quality sound. The AK4432 has single end SCF outputs, increasing performance for systems with excessive clock jitter. The AK4432 is ideal for a wide range of applications that demands high sound quality including Home Theater and Car audio surround systems. It is housed in a 16-pin TSSOP package, saving more board space.

2. Features

1. 2ch 32bit DAC

- 128 times Oversampling
- 32-bit High Quality Sound Low Group Delay Digital Filter
- Single Ended Output, Smoothing Filter
- THD+N: 91dB
- DR, S/N: 108dB
- Channel Isolation Digital Volume (12dB~-115dB, 0.5dB Step, Mute)
- Soft Mute
- De-emphasis Filter (32kHz, 44.1kHz, 48kHz)
- I/F Format: MSB justified, LSB justified, I²S, TDM
- Zero Detection

2. Sampling Frequency

- Normal Speed Mode: 8kHz to 48kHz
- Double Speed Mode: 64kHz to 96kHz
- Quad Speed Mode: 128kHz to 192kHz

3. Master Clock

- | | |
|------------------------------|---------------------------------------|
| 256fs, 384fs, 512fs or 768fs | (Normal Speed Mode: fs=8kHz ~ 48kHz) |
| 256fs or 384fs | (Double Speed Mode: fs=48kHz ~ 96kHz) |
| 128fs or 192fs | (Quad Speed Mode: fs=96kHz ~ 192kHz) |

4. μ P Interface: 3-wire Serial (7MHz max)/ I²C bus (400kHz Mode, 1MHz Mode)

5. Power Supply

- Analog: AVDD = 3.0 ~ 3.6V
- Input/Output Buffer: LVDD = 3.0 ~ 3.6V
- Integrated LDO for Digital Power Supply

6. Power Consumptions: 7.8mA (fs=48kHz)

7. Operational Temperature: Ta = - 40 ~ 105°C

8. Package: 16-pin TSSOP (0.65mm pitch)

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4. Block Diagram

■ Block Diagram

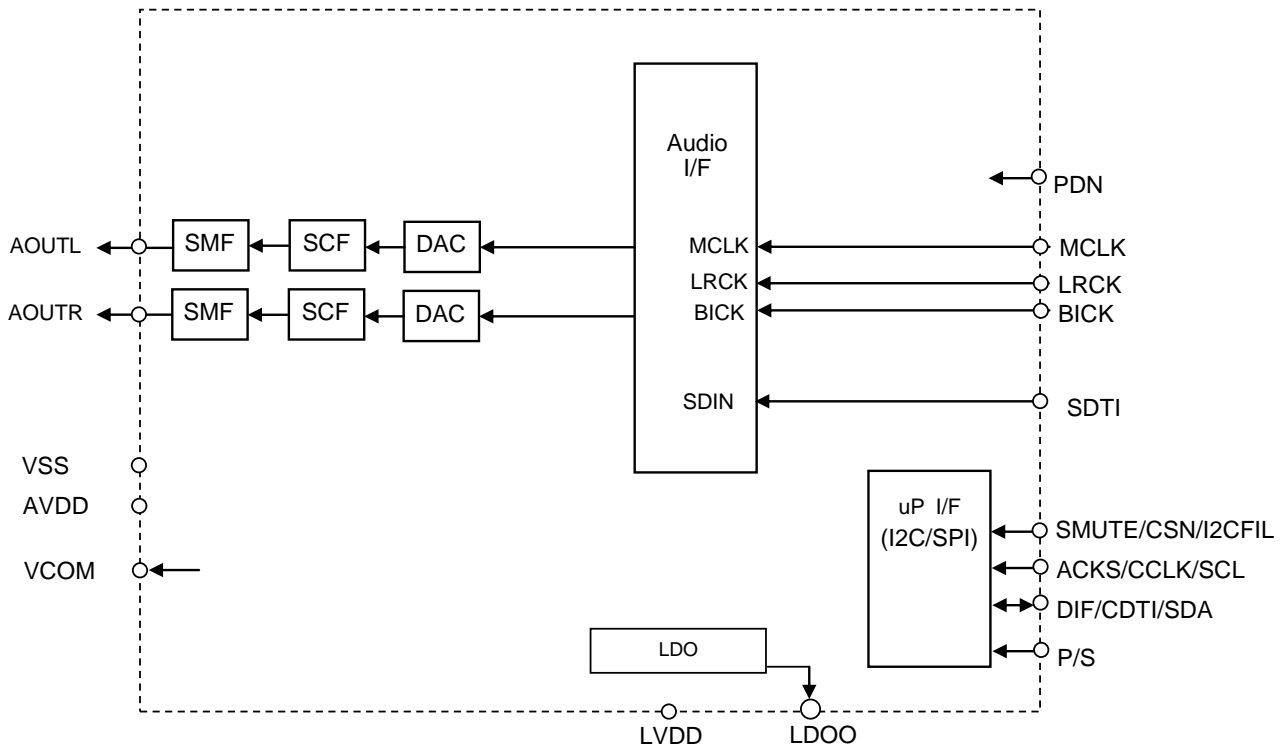


Figure 1. Block Diagram

■Compatibility with AK4438, AK4452 and AK4458

| | | AK4432 | AK4436 / 38 | AK4452 / 54 / 56 / 58 |
|------------------------------|---------------------|---------------------|-----------------------------|--|
| Channel | | 2ch | 6ch / 8ch | 2ch / 4ch / 6ch / 8ch |
| fs | | 8k to 192kHz | 8k to 768kHz | 8k to 768kHz |
| S/(N+D) | | 91dB | 91dB | 107dB |
| DR | | 108dB | 108dB | 115dB |
| AVDD (Analog Supply) | | 3.0 to 3.6V | 3.0 to 3.6V | 3.0 to 5.5V |
| TVDD or LVDD (I/O Buffer) | | 3.0 to 3.6V | 1.7 to 3.6V | 1.7 to 3.6V |
| Digital Filter | SA(Sharp) | 69.9dB | 80dB | 80dB |
| | GD(Sharp) | 26.4/fs | 26.8/fs | 26.8/fs |
| | GD (SD Slow) | 5.2/fs | 4.8/fs | 4.8/fs |
| | Super Slow Roll-off | No | Yes | Yes |
| OSR Doubler (Over Sampling) | | No (128x) | Yes (256x) | Yes (256x) |
| Zero Detection | | No | Yes | Yes |
| Digital Volume | | +12 to -115.0dB | +0 to -127.0dB | +0 to -127.0dB |
| ATT Speed (*Default) | | 1020/fs (*) 4080 | 4080/fs (*) 2040、510、255 | 4080/fs (*) 2040、510、255 |
| LR Ch Output Select | | No | Yes | Yes |
| Reset Function (MCLK detect) | | No | Yes | Yes |
| Clock Synchronization | | Yes (Note) | Yes | Yes |
| Package | | 16-pin TSSOP | 32-pin QFN | AK4452/54: 32-pin QFN AK4456/58: 48-pin QFN |

Note. MSB justified and 32-bit I²S compatible formats are available for audio interface but LSB justified format is not available.

5. Pin Configurations and Functions

■ **Ordering Guide**

| | | |
|----------|---------------------------------|-----------------------------|
| AK4432VT | -40 ~ +105°C | 16-pin TSSOP (0.65mm pitch) |
| AKD4432 | Evaluation Board for the AK4432 | |

■ **Pin Layout**

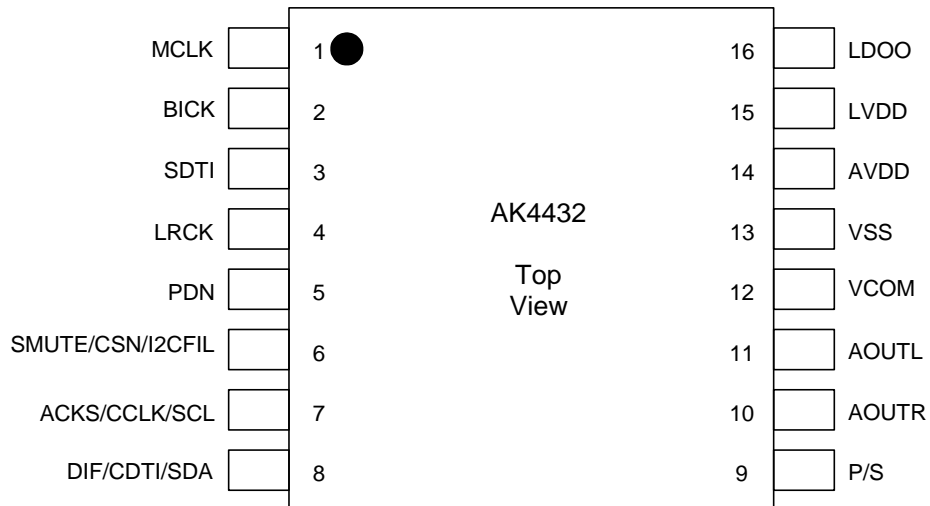


Figure 2. Pin Layout

■ Pin Functions

| No. | Pin Name | I/O | PD state | Function |
|-----|----------|-----|---------------------|--|
| 1 | MCLK | I | - | External Master Clock Input Pin |
| 2 | BICK | I | - | Audio Serial Data Clock Pin |
| 3 | SDTI | I | - | Audio Serial Data Input |
| 4 | LRCK | I | - | Input Channel Clock Pin |
| 5 | PDN | I | - | Power-Down & Reset Pin When "L", the AK4432 is powered-down and the control registers are reset to default state. |
| 6 | SMUTE | I | - | Soft Mute Pin in Parallel control mode. When this pin is changed to "H", soft mute cycle is initiated. When returning "L", the output mute releases. |
| | CSN | I | | Chip Select Pin in 3-wire serial control mode |
| | I2CFIL | I | | I2C Interface Mode Select Pin "L": Fast Mode (400kHz), "H": Fast Mode Plus (1MHz). Do not change this pin during PDN pin = "H". |
| 7 | ACKS | I | - | Auto Setting Mode in Parallel control mode "L": Manual Setting Mode, "H": Auto Setting Mode |
| | CCLK | I | | Control Data Clock Pin in 3-wire serial control mode |
| | SCL | I | | Control Data Clock Pin in I2C Bus serial control mode |
| 8 | DIF | I | - | Audio Data Format Select in Parallel control mode. "L": 32bit MSB, "H": 32bit I2S |
| | CDTI | I | | Control Data Input Pin in 3-wire serial control mode |
| | SDA | I/O | | Control Data Input Pin in I2C Bus serial control mode |
| 9 | P/S | I | - | Parallel/Serial Mode Select Pin "L": Serial Mode, "H": Parallel Mode Do not change this pin during PDN pin = "H". |
| 10 | AOUTR | O | Hi-z | Rch Analog Output Pin |
| 11 | AOUTL | O | Hi-z | Lch Analog Output Pin |
| 12 | VCOM | O | 500ohm Pull-down | Common Voltage Output Pin, AVDDx1/2 Large external capacitor around 2.2μF is used to reduce power-supply noise. |
| 13 | VSS | - | - | Ground Pin |
| 14 | AVDD | - | - | Analog Power Supply Pin, 3.0V~3.6V |
| 15 | LVDD | - | - | LDO Power Supply / Digital I/F Power Supply Pin, 3.0V~3.6V |
| 16 | LDOO | O | 580ohm Pull-down | LDO Output Pin This pin should be connected to ground with 1.0uF. |

Note 1. All digital input pins must not be allowed to float.

■ Handling of Unused Pin

Unused I/O pins must be connected appropriately.

| Classification | Pin Name | Setting |
|----------------|--------------|---------|
| Analog | AOUTL, AOUTR | Open |

6. Absolute Maximum Ratings

(VSS = 0V; [Note 2](#))

| Parameter | Symbol | Min. | Max. | Unit |
|--|--------|------|-------------------|------|
| Power Supply | AVDD | -0.3 | 4.3 | V |
| Power Supply | LVDD | -0.3 | 4.3 | V |
| Input Current (any pins except for supplies) | IIN | - | ±10 | mA |
| Input Voltage (Note 3) | VIN | -0.3 | (LVDD+0.3) or 4.3 | V |
| Ambient Temperature (power applied) | Ta | -40 | 105 | °C |
| Storage Temperature | Tstg | -65 | 150 | °C |

Note 2. All voltages with respect to ground. VSS must be connected to the same analog ground plane.

Note 3. The maximum Digital input voltage is smaller value between (LVDD+0.3)V and 4.3V.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

7. Recommended Operation Conditions

(VSS=0V; [Note 2](#))

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|----------------|--------------------|--------|------|------|------|------|
| Power Supplies | Analog | AVDD | 3.0 | 3.3 | 3.6 | V |
| | LDO, Digital (I/F) | LVDD | 3.0 | 3.3 | 3.6 | V |

Note 4. Do not turn off the power supply of the AK4432 with the power supply of the peripheral device turned on. When using the I²C interface, pull-up resistors of SDA and SCL pins should be connected to LVDD or less voltage.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

8. Analog Characteristics

(Ta=25°C; AVDD = LVDD=3.3V; VSS =0V; fs=48kHz, 96kHz, 192kHz; BICK=64fs; Signal Frequency=1kHz; 32bit Data; Measurement Frequency=20Hz~20kHz at fs=48kHz, 20Hz~40kHz at fs=96kHz, 20Hz~40kHz at fs=192kHz, unless otherwise specified.)

| Parameter | Min. | Typ. | Max. | Unit |
|--|-----------------------|------|------|------|
| DAC Analog Output Characteristics | | | | |
| Resolution | | | 32 | bit |
| Output Voltage (Note 5) | 2.55 | 2.83 | 3.11 | Vpp |
| S/(N+D) (0dBFS) | fs=48kHz | 80 | 91 | dB |
| | fs=96kHz | | 89 | dB |
| | fs=192kHz | | 89 | dB |
| Dynamic Range (-60dBFS) | fs=48kHz (A-weighted) | | 108 | dB |
| | fs=96kHz | | 101 | |
| | fs=192kHz | | 101 | |
| S/N | fs=48kHz (A-weighted) | | 108 | dB |
| | fs=96kHz | | 101 | |
| | fs=192kHz | | 101 | |
| Interchannel Isolation | 90 | 110 | | dB |
| Interchannel Gain Mismatch | | 0 | 0.7 | dB |
| Load Resistance (Note 6) | 10 | | | kΩ |
| Load Capacitance | | | 30 | pF |

Note 5. Full-scale output voltage. The output voltage is always proportional to AVDD (AVDD x 0.86).

Note 6. AC Load

| Parameter | Min. | Typ. | Max. | Unit |
|--|-------------------------|------|------|------|
| Power Supplies | | | | |
| Power Supply Current | | | | |
| Normal Operation (PDN pin = "H") | | | | |
| AVDD | fs=48kHz, 96kHz, 192kHz | 6.5 | 9.0 | mA |
| LVDD | fs=48kHz | 1.3 | 2 | mA |
| | fs=96kHz | 1.6 | 2.5 | mA |
| | fs=192kHz | 2.1 | 3.0 | mA |
| Power-down mode (PDN pin = "L") (Note 7) | | 10 | 200 | μA |

Note 7. Quiescent Current. All digital input pins including clock pins are fixed to VSS.

| |
|---|
| 9. Filter Characteristics (fs=48kHz) |
|---|

(Ta= -40 ~ +105°C; AVDD =3.0~ 3.6V, LVDD=3.0~ 3.6V; DEM=OFF)

■ Sharp Roll-Off Filter (DASD bit = “0”, DASL bit = “0”)

fs=48kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------|--------|-------|-------|-------|------|
| Passband (Note 8) | -0.08dB~+0.08dB | PB | 0 | - | 22.2 | kHz |
| | -6.0dB | PB | - | 23.99 | - | kHz |
| Passband Ripple | | PR | -0.08 | | +0.08 | dB |
| Stopband (Note 8) | | SB | 26.2 | | | kHz |
| Stopband Attenuation | | SA | 69.9 | | | dB |
| Group Delay (Note 9) | | GD | - | 26.4 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 20kHz | | FR | -0.20 | | -0.10 | dB |

fs=96kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------|--------|-------|-------|-------|------|
| Passband (Note 8) | -0.08dB~+0.08dB | PB | 0 | - | 44.4 | kHz |
| | -6.0dB | PB | - | 48.00 | - | kHz |
| Passband Ripple | | PR | -0.08 | | +0.08 | dB |
| Stopband (Note 8) | | SB | 52.5 | | | kHz |
| Stopband Attenuation | | SA | 69.8 | | | dB |
| Group Delay (Note 9) | | GD | - | 26.4 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 40kHz | | FR | -0.50 | | -0.10 | dB |

fs=192kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------|--------|-------|-------|-------|------|
| Passband (Note 8) | -0.08dB~+0.08dB | PB | 0 | - | 88.8 | kHz |
| | -6.0dB | PB | - | 96.00 | - | kHz |
| Passband Ripple | | PR | -0.08 | | +0.08 | dB |
| Stopband (Note 8) | | SB | 104.9 | | | kHz |
| Stopband Attenuation | | SA | 69.8 | | | dB |
| Group Delay (Note 9) | | GD | - | 26.4 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 80kHz | | FR | -2.00 | | 0.00 | dB |

■ Slow Roll-Off Filter (DASD bit = “0”, DASL bit = “1”)

fs=48kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|------------------|--------|-------|-------|--------|------|
| Passband (Note 8) | -0.07dB~+0.021dB | PB | 0 | - | 9.0 | kHz |
| | -3.0dB | PB | - | 19.75 | - | kHz |
| Passband Ripple | | PR | -0.07 | | +0.021 | dB |
| Stopband (Note 8) | | SB | 42.6 | | | kHz |
| Stopband Attenuation | | SA | 72.6 | | | dB |
| Group Delay (Note 9) | | GD | - | 26.4 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 20kHz | | FR | -3.75 | | -2.75 | dB |

fs=96kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|------------------|--------|-------|------|--------|------|
| Passband (Note 8) | -0.07dB~+0.023dB | PB | 0 | - | 18.1 | kHz |
| | -3.0dB | PB | - | 39.6 | - | kHz |
| Passband Ripple | | PR | -0.07 | | +0.023 | dB |
| Stopband (Note 8) | | SB | 85.1 | | | kHz |
| Stopband Attenuation | | SA | 72.6 | | | dB |
| Group Delay (Note 9) | | GD | - | 26.4 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 40kHz | | FR | -4.25 | | -2.75 | dB |

fs=192kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|------------------|--------|-------|------|--------|------|
| Passband (Note 8) | -0.07dB~+0.023dB | PB | 0 | - | 36.1 | kHz |
| | -3.0dB | PB | - | 79.3 | - | kHz |
| Passband Ripple | | PR | -0.07 | | +0.023 | dB |
| Stopband (Note 8) | | SB | 170.3 | | | kHz |
| Stopband Attenuation | | SA | 72.6 | | | dB |
| Group Delay (Note 9) | | GD | - | 26.4 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 80kHz | | FR | -5.00 | | -3.00 | dB |

■ Short Delay Sharp Roll-Off Filter (DASD bit = “1”, DASL bit = “0”)

fs=48kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------|--------|-------|-------|-------|------|
| Passband (Note 8) | -0.07dB~+0.07dB | PB | 0 | - | 22.0 | kHz |
| | -6.0dB | PB | - | 24.11 | - | kHz |
| Passband Ripple | | PR | -0.07 | | +0.07 | dB |
| Stopband (Note 8) | | SB | 26.2 | | | kHz |
| Stopband Attenuation | | SA | 56.6 | | | dB |
| Group Delay (Note 9) | | GD | - | 5.9 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 20kHz | | FR | -0.20 | | -0.10 | dB |

fs=96kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------|--------|-------|-------|-------|------|
| Passband (Note 8) | -0.08dB~+0.08dB | PB | 0 | - | 44.3 | kHz |
| | -6.0dB | PB | - | 48.25 | - | kHz |
| Passband Ripple | | PR | -0.08 | | +0.08 | dB |
| Stopband (Note 8) | | SB | 52.5 | | | kHz |
| Stopband Attenuation | | SA | 56.4 | | | dB |
| Group Delay (Note 9) | | GD | - | 5.9 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 40kHz | | FR | -0.50 | | -0.10 | dB |

fs=192kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------|--------|-------|-------|-------|------|
| Passband (Note 8) | -0.08dB~+0.08dB | PB | 0 | - | 88.6 | kHz |
| | -6.0dB | PB | - | 96.50 | - | kHz |
| Passband Ripple | | PR | -0.08 | | +0.08 | dB |
| Stopband (Note 8) | | SB | 104.9 | | | kHz |
| Stopband Attenuation | | SA | 56.4 | | | dB |
| Group Delay (Note 9) | | GD | - | 5.9 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 80kHz | | FR | -2.00 | | 0.00 | dB |

■ Short Delay Slow Roll-Off Filter (DASD bit = “1”, DASL bit = “1”)

fs=48kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------|--------|-------|-------|-------|------|
| Passband (Note 8) | -0.07dB~+0.05dB | PB | 0 | - | 10.1 | kHz |
| | -3.0dB | PB | - | 20.24 | - | kHz |
| Passband Ripple | | PR | -0.07 | | +0.05 | dB |
| Stopband (Note 8) | | SB | 43.0 | | | kHz |
| Stopband Attenuation | | SA | 74.9 | | | dB |
| Group Delay (Note 9) | | GD | - | 5.2 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 20kHz | | FR | -3.50 | | -2.50 | dB |

fs=96kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------|--------|-------|-------|-------|------|
| Passband (Note 8) | -0.07dB~+0.05dB | PB | 0 | - | 20.3 | kHz |
| | -3.0dB | PB | - | 40.50 | - | kHz |
| Passband Ripple | | PR | -0.07 | | +0.05 | dB |
| Stopband (Note 8) | | SB | 86.0 | | | kHz |
| Stopband Attenuation | | SA | 74.9 | | | dB |
| Group Delay (Note 9) | | GD | - | 5.2 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 40kHz | | FR | -4.00 | | -2.50 | dB |

fs=192kHz

| Parameter | | Symbol | Min. | Typ. | Max. | Unit |
|---------------------------------|-----------------|--------|-------|-------|-------|------|
| Passband (Note 8) | -0.07dB~+0.05dB | PB | 0 | - | 40.6 | kHz |
| | -3.0dB | PB | - | 81.00 | - | kHz |
| Passband Ripple | | PR | -0.07 | | +0.05 | dB |
| Stopband (Note 8) | | SB | 172.0 | | | kHz |
| Stopband Attenuation | | SA | 74.9 | | | dB |
| Group Delay (Note 9) | | GD | - | 5.2 | - | 1/fs |
| Digital Filter + SCF + SMF | | | | | | |
| Frequency Response: 0Hz ~ 80kHz | | FR | -4.75 | | -2.75 | dB |

Note 8. The passband and stopband frequencies are proportional to “fs” (system sampling rate). Each frequency response refers to that of 1kHz.

Note 9. The calculated delay time caused by digital filtering. The digital filter’s delay is calculated as the time from setting 16/24/32bit impulse data into the input register until an analog peak signal is output.

| |
|-------------------------------|
| 10. DC Characteristics |
|-------------------------------|

(Ta= -40 ~ +105°C; AVDD =3.0~ 3.6V, LVDD =3.0~ 3.6V, VSS=0V)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|--------|---------|------|---------|------|
| All digital input pins except SCL and SDA pins | | | | | |
| High-Level Input Voltage | VIH1 | 80%LVDD | - | - | V |
| Low-Level Input Voltage | VIL1 | - | - | 20%LVDD | V |
| SCL, SDA Pin | | | | | |
| High-Level Input Voltage | VIH2 | 70%LVDD | - | - | V |
| Low-Level Input Voltage | VIL2 | - | - | 30%LVDD | V |
| SDA Pin | | | | | |
| Low-Level Output Voltage | | | | | |
| Fast Mode (Iout= 3mA) | VOL1 | - | | 0.4 | V |
| Fast Mode Plus (Iout= 20mA) | VOL2 | - | | 0.4 | V |
| Input Leakage Current | Iin | - | - | ±10 | μA |

| |
|--------------------------------------|
| 11. Switching Characteristics |
|--------------------------------------|

(Ta=-40 ~ 105°C; AVDD=LVDD=3.0 ~ 3.6V; CL=20pF, unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|--------|------------|------|--------------|------|
| Master Clock Timing | | | | | |
| External Clock | | | | | |
| 256fsn: | fCLK | 2.048 | | 12.288 | MHz |
| Pulse Width Low | tCLKL | 32 | | | ns |
| Pulse Width High | tCLKH | 32 | | | ns |
| 384fsn: | fCLK | 3.072 | | 18.432 | MHz |
| Pulse Width Low | tCLKL | 22 | | | ns |
| Pulse Width High | tCLKH | 22 | | | ns |
| 512fsn, 256fsd, 128fsq: | fCLK | 4.096 | | 24.576 | MHz |
| Pulse Width Low | tCLKL | 16 | | | ns |
| Pulse Width High | tCLKH | 16 | | | ns |
| 768fsn, 384fsd, 192fsq: | fCLK | 16.384 | | 36.864 | MHz |
| Pulse Width Low | tCLKL | 11 | | | ns |
| Pulse Width High | tCLKH | 11 | | | ns |
| LRCK Timing (Slave Mode) | | | | | |
| Stereo mode (TDM1-0 bits = "00") | | | | | |
| Normal Speed Mode | fsn | 8 | | 48 | kHz |
| Double Speed Mode | fsd | 48 | | 96 | kHz |
| Quad Speed Mode | fsq | 96 | | 192 | kHz |
| Duty Cycle | Duty | - | 50 | - | % |
| TDM128 mode (TDM1-0 bits = "01") | | | | | |
| LRCK frequency | fsn | 8 | | 48 | kHz |
| | fsd | 48 | | 96 | kHz |
| | fsq | 96 | | 192 | kHz |
| I ² S compatible: Pulse Width Low | tLRL | 1/(128fsq) | | 127/(128fsq) | s |
| MSB or LSB justified: Pulse Width High | tLRH | 1/(128fsq) | | 127/(128fsq) | s |
| TDM256 mode (TDM1-0 bits = "10") | | | | | |
| LRCK frequency | fsn | 8 | | 48 | kHz |
| | fsd | 48 | | 96 | kHz |
| I ² S compatible: Pulse Width Low | tLRL | 1/(256fsd) | | 255/(256fsd) | s |
| MSB or LSB justified: Pulse Width High | tLRH | 1/(256fsd) | | 255/(256fsd) | s |

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|--------|----------|------|------|------|
| Audio Interface Timing | | | | | |
| Normal Mode (TDM1-0 bits = "00") | | | | | |
| BICK Period | | | | | |
| Normal Speed Mode | tBCK | 1/256fsn | | | ns |
| Double Speed Mode | tBCK | 1/256fsd | | | ns |
| Quad Speed Mode | tBCK | 1/128fsq | | | ns |
| BICK Pulse Width Low | tBCKL | 18 | | | ns |
| BICK Pulse Width High | tBCKH | 18 | | | ns |
| BICK "↑" to LRCK Edge (Note 10) | tBLR | 5 | | | ns |
| LRCK Edge to BICK "↑" (Note 10) | tLRB | 5 | | | ns |
| SDTI Hold Time | tSDH | 5 | | | ns |
| SDTI Setup Time | tSDS | 5 | | | ns |
| TDM128 mode (TDM1-0 bits = "01") | | | | | |
| BICK Period | | | | | |
| Normal Speed Mode | tBCK | 1/128fsn | | | ns |
| Double Speed Mode | tBCK | 1/128fsd | | | ns |
| Quad Speed Mode | tBCK | 1/128fsq | | | ns |
| BICK Pulse Width Low | tBCKL | 18 | | | ns |
| BICK Pulse Width High | tBCKH | 18 | | | ns |
| BICK "↑" to LRCK Edge (Note 10) | tBLR | 5 | | | ns |
| LRCK Edge to BICK "↑" (Note 10) | tLRB | 5 | | | ns |
| SDTI Hold Time | tSDH | 5 | | | ns |
| SDTI Setup Time | tSDS | 5 | | | ns |
| TDM256 mode (TDM1-0 bits = "10") | | | | | |
| BICK Period | | | | | |
| Normal Speed Mode | tBCK | 1/256fsn | | | ns |
| Double Speed Mode | tBCK | 1/256fsd | | | ns |
| BICK Pulse Width Low | tBCKL | 18 | | | ns |
| BICK Pulse Width High | tBCKH | 18 | | | ns |
| BICK "↑" to LRCK Edge (Note 10) | tBLR | 5 | | | ns |
| LRCK Edge to BICK "↑" (Note 10) | tLRB | 5 | | | ns |
| SDTI Hold Time | tSDH | 5 | | | ns |
| SDTI Setup Time | tSDS | 5 | | | ns |

Note 10. BICK rising edge must not occur at the same time as LRCK edge.

| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|--|---------|------|------|------|------|
| Control Interface Timing (3-wire Serial mode): | | | | | |
| CCLK frequency | fCCK | | | 7 | MHz |
| CCLK Pulse Width Low | tCCKL | 60 | | | ns |
| Pulse Width High | tCCKH | 60 | | | ns |
| CDTI Setup Time | tCDS | 60 | | | ns |
| CDTI Hold Time | tCDH | 60 | | | ns |
| CSN "H" Time | tCSW | 150 | | | ns |
| CSN "↓" to CCLK "↓" | tCSS | 150 | | | ns |
| CCLK "↑" to CSN "↑" | tCSH | 240 | | | ns |
| Control Interface Timing (I²C Fast mode): | | | | | |
| SCL Clock Frequency | fSCL | - | | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | | - | μs |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 0.6 | | - | μs |
| Clock Low Time | tLOW | 1.3 | | - | μs |
| Clock High Time | tHIGH | 0.6 | | - | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.6 | | - | μs |
| SDA Hold Time from SCL Falling (Note 11) | tHD:DAT | 0 | | - | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | | - | μs |
| Rise Time of Both SDA and SCL Lines | tR | - | | 1.0 | μs |
| Fall Time of Both SDA and SCL Lines | tF | - | | 0.3 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | | - | μs |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | | 50 | ns |
| Capacitive load on bus | Cb | - | | 400 | pF |
| Control Interface Timing (I²C Fast mode Plus): | | | | | |
| SCL Clock Frequency | fSCL | - | | 1 | MHz |
| Bus Free Time Between Transmissions | tBUF | 0.5 | | - | μs |
| Start Condition Hold Time (prior to first clock pulse) | tHD:STA | 0.26 | | - | μs |
| Clock Low Time | tLOW | 0.5 | | - | μs |
| Clock High Time | tHIGH | 0.26 | | - | μs |
| Setup Time for Repeated Start Condition | tSU:STA | 0.26 | | - | μs |
| SDA Hold Time from SCL Falling (Note 12) | tHD:DAT | 0 | | - | μs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.05 | | - | μs |
| Rise Time of Both SDA and SCL Lines | tR | - | | 0.12 | μs |
| Fall Time of Both SDA and SCL Lines | tF | - | | 0.12 | μs |
| Setup Time for Stop Condition | tSU:STO | 0.26 | | - | μs |
| Pulse Width of Spike Noise Suppressed by Input Filter | tSP | 0 | | 50 | ns |
| Capacitive load on bus | Cb | - | | 550 | pF |
| Power-down & Reset Timing | | | | | |
| PDN Pulse Width (Note 13) | tPD | 800 | | | ns |

Note 11. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

Note 12. Data must be held for sufficient time to bridge the 120ns transition time of SCL.

Note 13. The AK4432 can be reset by setting the PDN pin to "L" upon power-up. The PDN pin must held "L" for more than 800ns for a certain reset. The AK4432 is not reset by the "L" pulse less than 50ns.

Note 14. I²C is a trademark of NXP B.V.

■ Timing Diagram

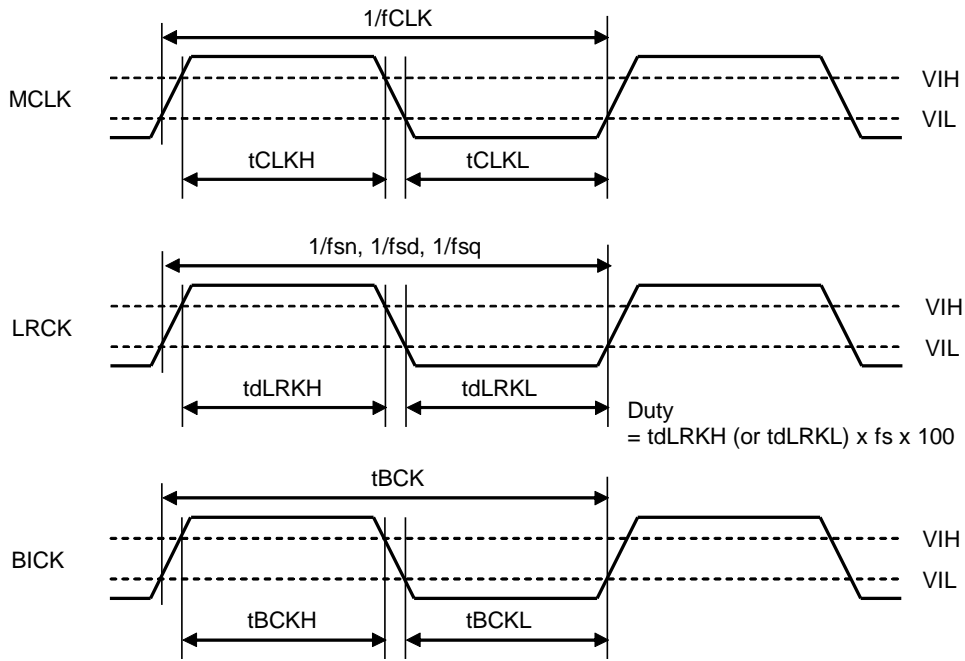


Figure 3. Clock Timing (TDM1-0 bits = "00")

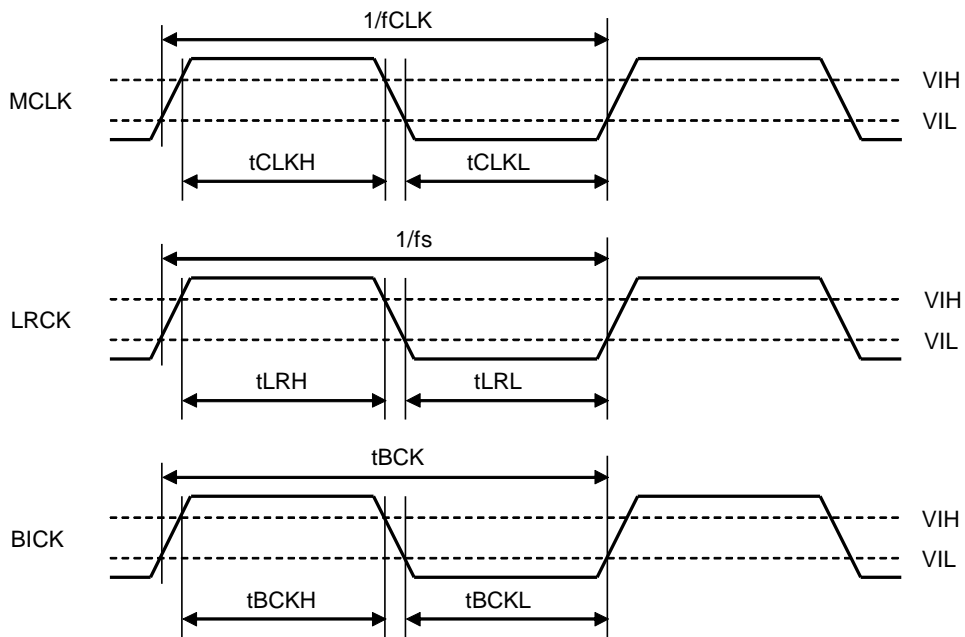


Figure 4. Clock Timing (Except TDM1-0 bits = "00")

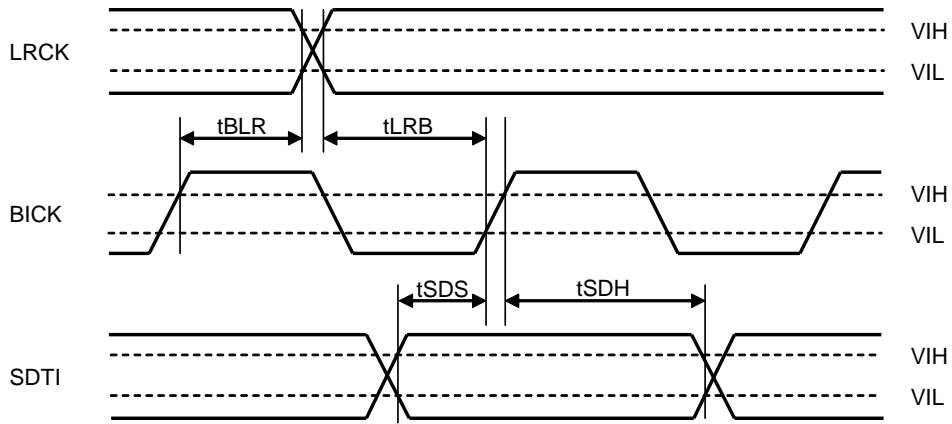


Figure 5. Audio Interface Timing (TDM1-0 bits = "00")

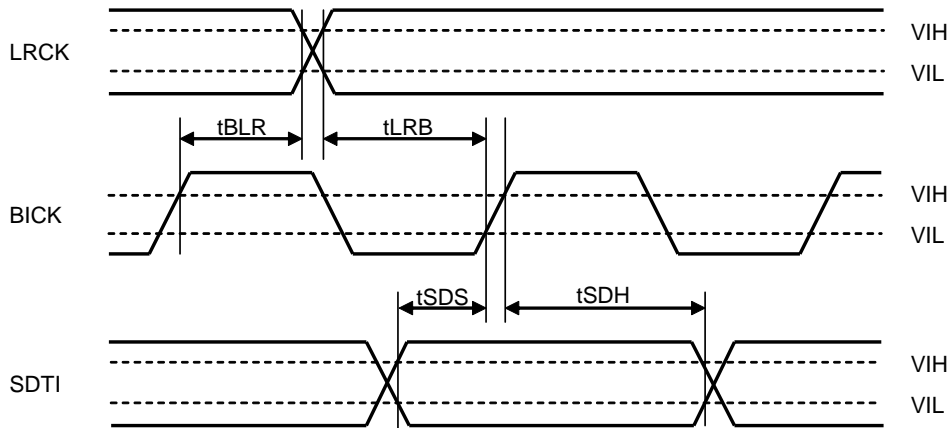


Figure 6. Audio Interface Timing (Except TDM1-0 bits = "00")

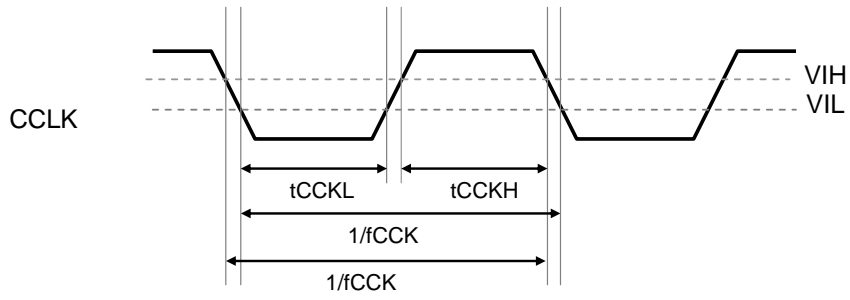


Figure 7. 3-wire Serial Mode Interface Timing

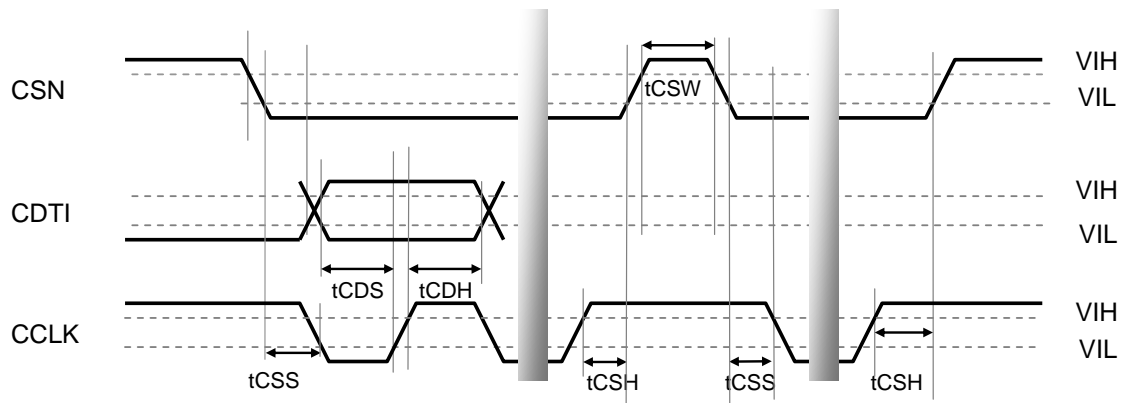


Figure 8. WRITE Data Input Timing (3-wire Serial mode)

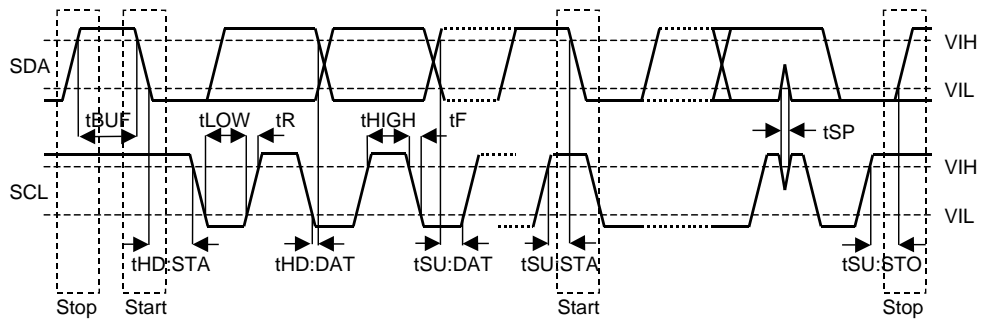


Figure 9. I²C Bus Mode Timing

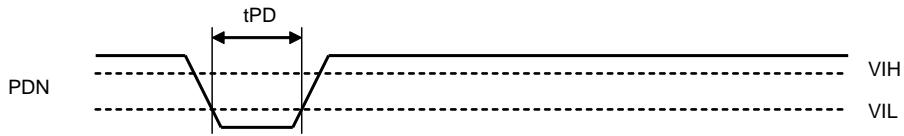


Figure 10. Power-down & Reset Timing

12. Functional Descriptions

■ System Clock

The external clocks which are required to operate the AK4432 are MCLK, LRCK and BICK. MCLK should be synchronized with LRCK and BICK but the phase is not critical. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS bit= "0": Default), the sampling speed is set by DFS0, DFS1 (Table 1). The frequency of MCLK at each sampling speed is set automatically (Table 2, Table 3, Table 4). In Auto Setting Mode (ACKS bit= "1"), as MCLK frequency is detected automatically (Table 5) and the internal master clock attains the appropriate frequency (Table 6), so it is not necessary to set DFS bits.

The AK4432 exits system reset (power-down mode) by inputting MCLK and LRCK after the PDN pin="H".

If the clock is stopped, a click noise occurs when restarting the clock. Mute the digital output externally if the click noise affects system applications.

| DFS1 | DFS0 | Sampling Speed Mode (fs) | |
|------|------|--------------------------|--------------|
| 0 | 0 | Normal Speed Mode | 8kHz~48kHz |
| 0 | 1 | Double Speed Mode | 48kHz~96kHz |
| 1 | 0 | Quad Speed Mode | 96kHz~192kHz |
| 1 | 1 | N/A | - |

(default)

(N/A: Not available)

Table 1. Sampling Speed (Manual Setting Mode)

| LRCK fs | MCLK (MHz) | | | | BICK (MHz) |
|------------|------------|---------|---------|---------|------------|
| | 256fs | 384fs | 512fs | 768fs | |
| 8.0kHz | 2.0480 | 3.0720 | 4.0960 | 6.1440 | 0.512 |
| 44.1kHz | 11.2896 | 16.9344 | 22.5792 | 33.8688 | 2.8224 |
| 48.0kHz | 12.2880 | 18.4320 | 24.5760 | 36.8640 | 3.0720 |

Table 2. System Clock Example (Normal Speed Mode @Manual Setting Mode)

| LRCK fs | MCLK (MHz) | | BICK (MHz) |
|------------|------------|---------|------------|
| | 256fs | 384fs | |
| 88.2kHz | 22.5792 | 33.8688 | 5.6448 |
| 96.0kHz | 24.5760 | 36.8640 | 6.1440 |

Table 3. System Clock Example (Double Speed Mode @Manual Setting Mode)

| LRCK fs | MCLK (MHz) | | BICK (MHz) |
|------------|------------|---------|------------|
| | 128fs | 192fs | |
| 176.4kHz | 22.5792 | 33.8688 | 11.2896 |
| 192.0kHz | 24.5760 | 36.8640 | 12.2880 |

Table 4. System Clock Example (Quad Speed Mode @Manual Setting Mode)

| MCLK | | Sampling Speed Mode |
|-------|-------|---------------------|
| 512fs | 768fs | Normal Speed Mode |
| 256fs | 384fs | Double Speed Mode |
| 128fs | 192fs | Quad Speed Mode |

Table 5. Sampling Speed (Auto Setting Mode)

| LRCK fs | MCLK (MHz) | | | | | | Sampling Speed Mode |
|------------|------------|---------|---------|---------|---------|---------|------------------------|
| | 128fs | 192fs | 256fs | 384fs | 512fs | 768fs | |
| 8.0kHz | - | - | - | - | 4.0960 | 6.1440 | Normal Speed Mode |
| 44.1kHz | - | - | - | - | 22.5792 | 33.8688 | |
| 48.0kHz | - | - | - | - | 24.5760 | 36.8640 | |
| 88.2kHz | - | - | 22.5792 | 33.8688 | - | - | Double Speed Mode |
| 96.0kHz | - | - | 24.5760 | 36.8640 | - | - | |
| 176.4kHz | 22.5792 | 33.8688 | - | - | - | - | Quad Speed Mode |
| 192.0kHz | 24.5760 | 36.8640 | - | - | - | - | |

Table 6. System Clock Example (Auto Setting Mode)

■ Audio Interface Format

TDM1-0 bits, DIF2-0 bits, SDS2-0 bits, TDM1-0 pins and DIF pin settings should not be changed during operation. MSB justified and I²S formats are available but LSB justified format is not available when SYNCE bit = "1" (default).

Normal Mode (TDM1-0 bit="00")

Two channels audio data is shifted in via the SDTI pin using BICK and LRCK inputs. Eight data formats are supported and selected by the DIF2-0 bits as shown in [Table 7](#). In all formats the serial data is MSB first, 2's complement format and is latched on the rising edge of BICK. Input "0" data to unused bits if the data does not use maximum bits when MSB justified, I²S format is selected. (e.g. Mode2 can be used in 16-bit MSB justified by zeroing the unused 8bits LSB).

TDM128 Mode (TDM1-0 bit="01")

Four channels audio data is shifted in via the SDTI pin using BICK and LRCK inputs. Data is selected by SDS1-0 bits. BICK is fixed to 128fs. Six data formats are supported and selected by the DIF2-0 bits as shown in [Table 7](#). In all formats the serial data is MSB first, 2's complement format and is latched on the rising edge of BICK.

TDM256 Mode (TDM1-0 bit="1X")

Eight channels audio data is shifted in via the SDTI pin using BICK and LRCK inputs. Data is selected by SDS1-0 bits. BICK is fixed to 256fs. Six data formats are supported and selected by the DIF2-0 bits as shown in [Table 7](#). In all formats the serial data is MSB first, 2's complement format and is latched on the rising edge of BICK.

| Mode | | TDM1 | TDM0 | DIF2 | DIF1 | DIF0 | SDTI Format | LRCK | BICK |
|---------------------|----|------|------|------------------------------------|------|-------|------------------------------------|------|-------|
| Normal (Note 15) | 0 | 0 | 0 | 0 | 0 | 0 | 16-bit LSB justified | H/L | ≥32fs |
| | 1 | | | 0 | 0 | 1 | 20-bit LSB justified | H/L | ≥40fs |
| | 2 | | | 0 | 1 | 0 | 24-bit MSB justified | H/L | ≥48fs |
| | 3 | | | 0 | 1 | 1 | 16-bit I ² S compatible | L/H | 32fs |
| | | | | 24-bit I ² S compatible | L/H | ≥48fs | | | |
| | 4 | | | 1 | 0 | 0 | 24-bit LSB justified | H/L | ≥48fs |
| | 5 | | | 1 | 0 | 1 | 32-bit LSB justified | H/L | ≥64fs |
| | 6 | | | 1 | 1 | 0 | 32-bit MSB justified | H/L | ≥64fs |
| 7 | 1 | 1 | 1 | 32-bit I ² S compatible | L/H | ≥64fs | | | |
| TDM128 | - | 0 | 1 | 0 | 0 | 0 | N/A | ↑ | 128fs |
| | - | | | 0 | 0 | 1 | N/A | ↑ | 128fs |
| | 8 | | | 0 | 1 | 0 | 24-bit MSB justified | ↑ | 128fs |
| | 9 | | | 0 | 1 | 1 | 24-bit I ² S compatible | ↓ | 128fs |
| | 10 | | | 1 | 0 | 0 | 24-bit LSB justified | ↑ | 128fs |
| | 11 | | | 1 | 0 | 1 | 32-bit LSB justified | ↑ | 128fs |
| | 12 | | | 1 | 1 | 0 | 32-bit MSB justified | ↑ | 128fs |
| | 13 | | | 1 | 1 | 1 | 32-bit I ² S compatible | ↓ | 128fs |
| TDM256 | - | 1 | 0 | 0 | 0 | 0 | N/A | ↑ | 256fs |
| | - | | | 0 | 0 | 1 | N/A | ↑ | 256fs |
| | 14 | | | 0 | 1 | 0 | 24-bit MSB justified | ↑ | 256fs |
| | 15 | | | 0 | 1 | 1 | 24-bit I ² S compatible | ↓ | 256fs |
| | 16 | | | 1 | 0 | 0 | 24-bit LSB justified | ↑ | 256fs |
| | 17 | | | 1 | 0 | 1 | 32-bit LSB justified | ↑ | 256fs |
| | 18 | | | 1 | 1 | 0 | 32-bit MSB justified | ↑ | 256fs |
| | 19 | | | 1 | 1 | 1 | 32-bit I ² S compatible | ↓ | 256fs |

Note 15. BICK that is input to each channel must be longer than the bit length of setting format.

Table 7. Audio Data Format (N/A: Not available)

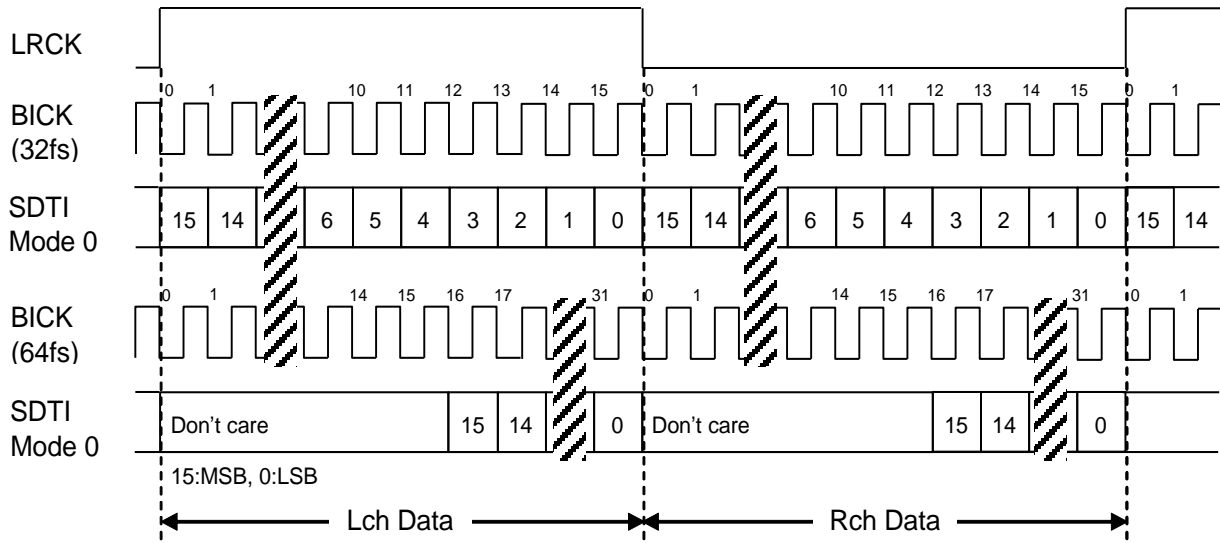


Figure 11. Mode 0 Timing

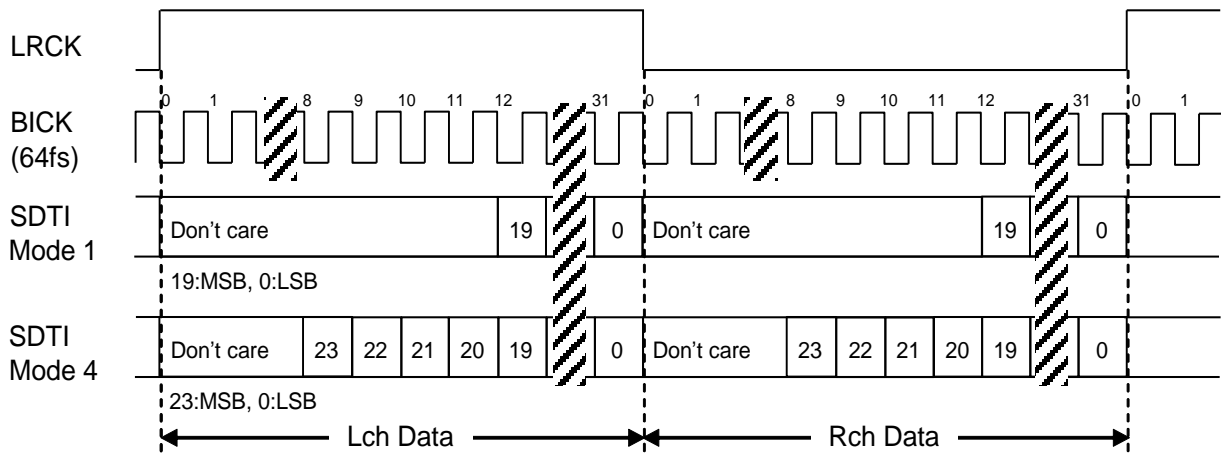


Figure 12. Mode 1/4 Timing

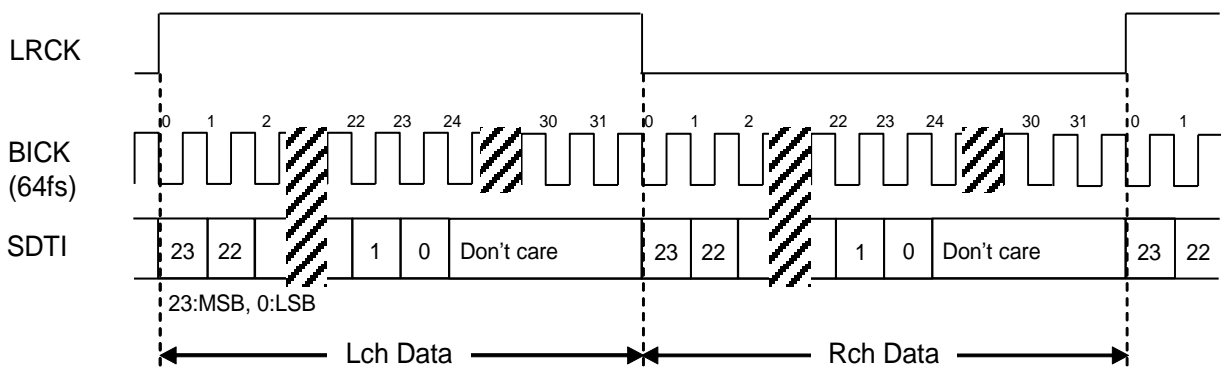
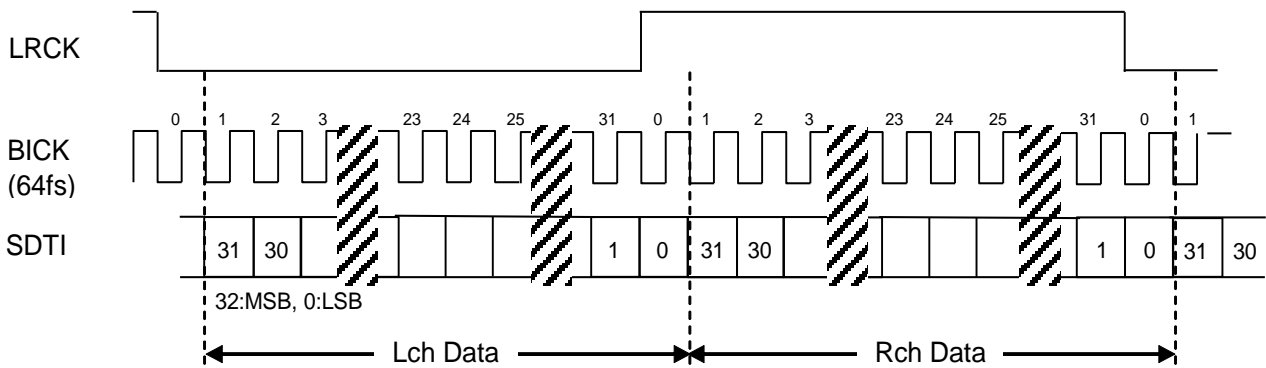
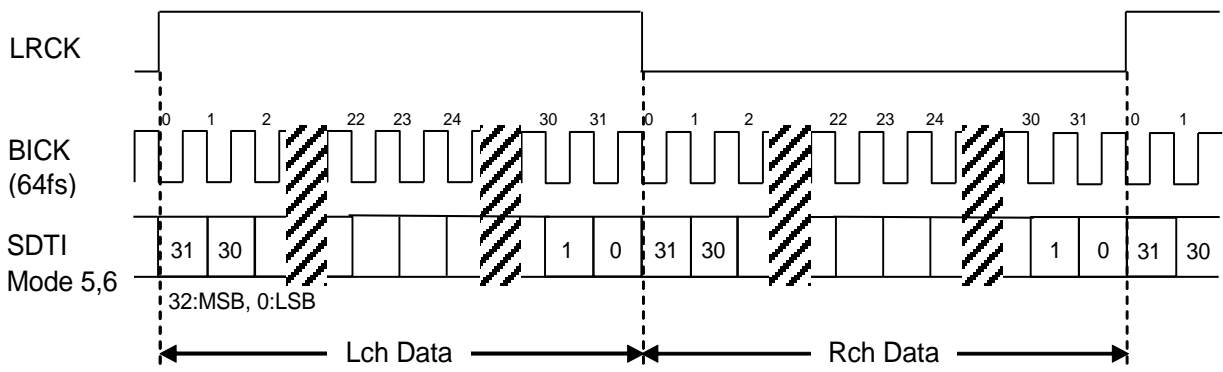
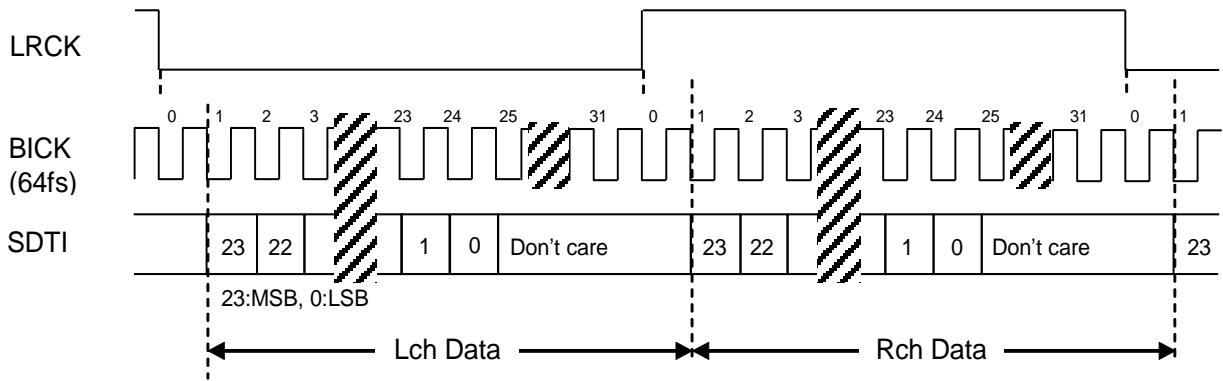


Figure 13. Mode 2 Timing



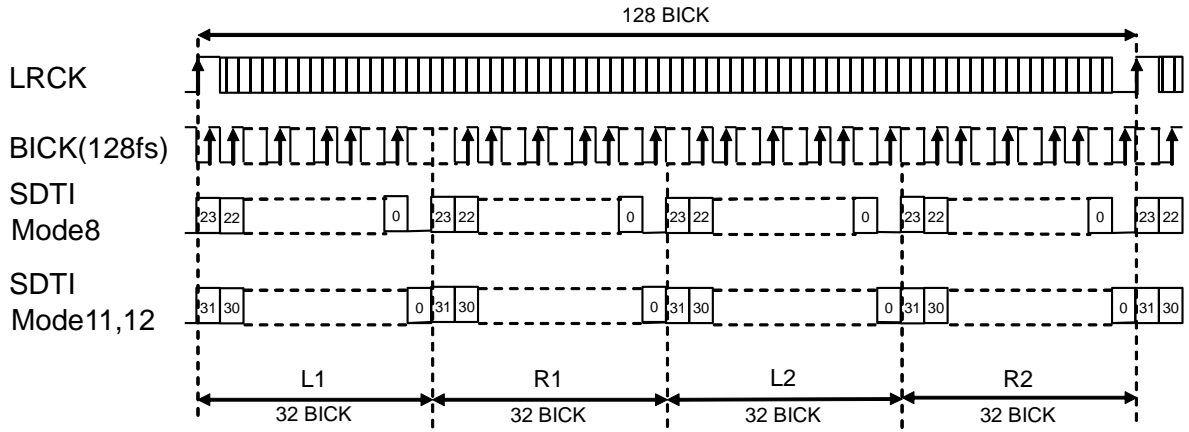


Figure 17. Mode 8/11/12 Timing

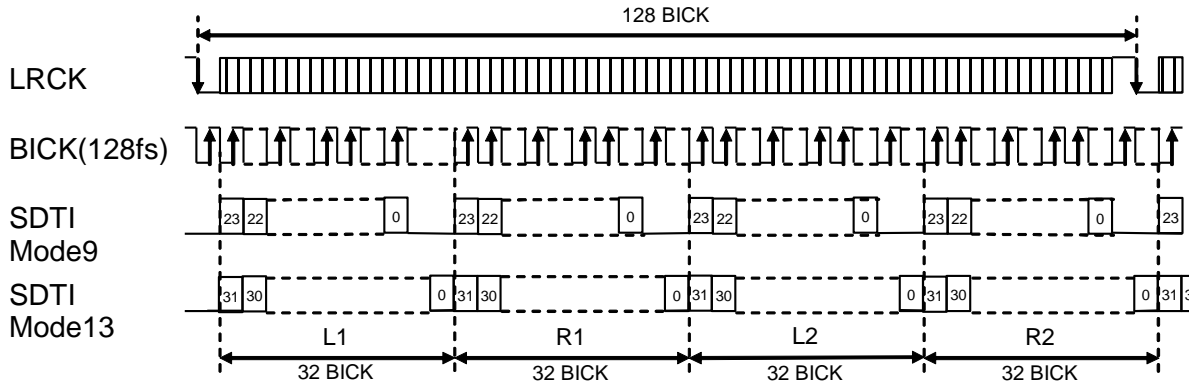


Figure 18. Mode 9/13 Timing

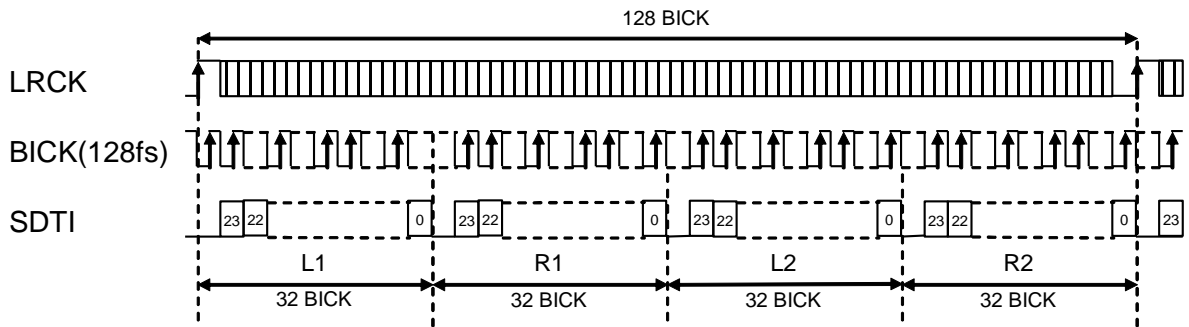


Figure 19. Mode 10 Timing

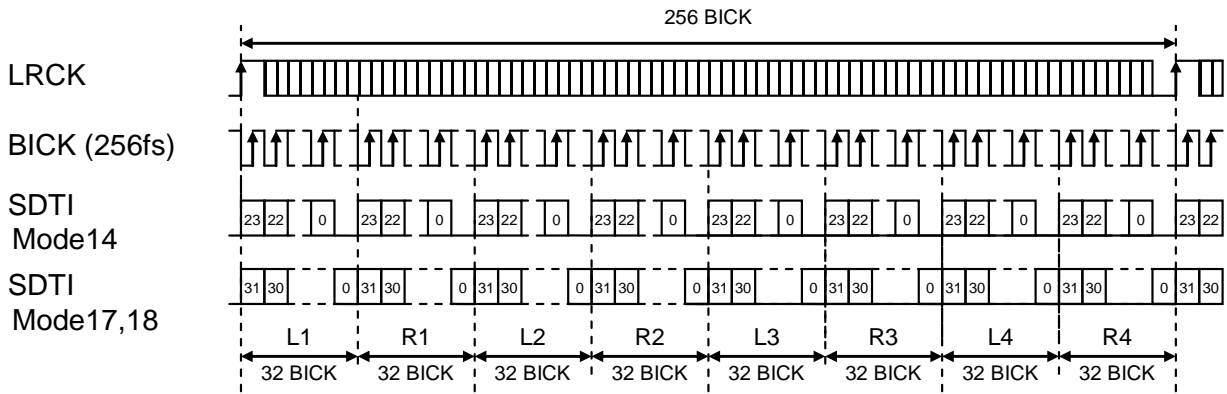


Figure 20. Mode 14/17/18 Timing

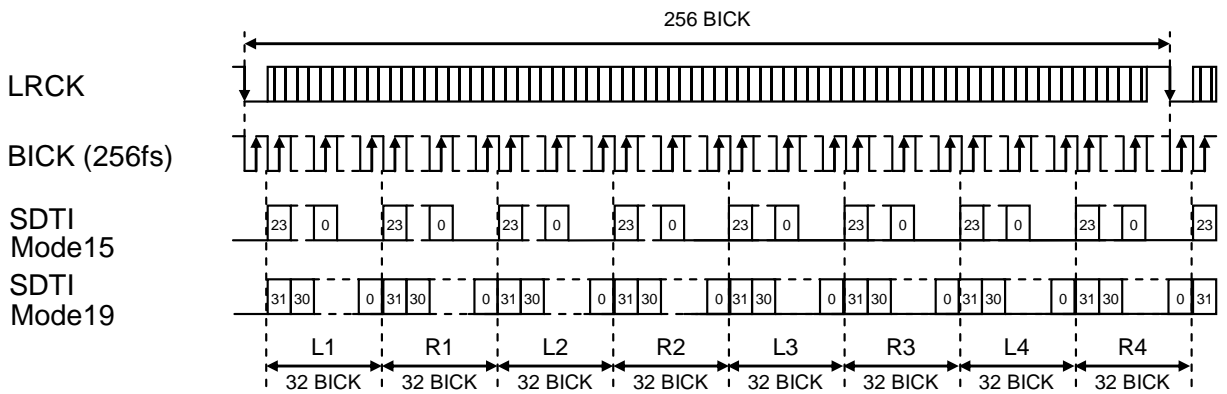


Figure 21. Mode 15/19 Timing

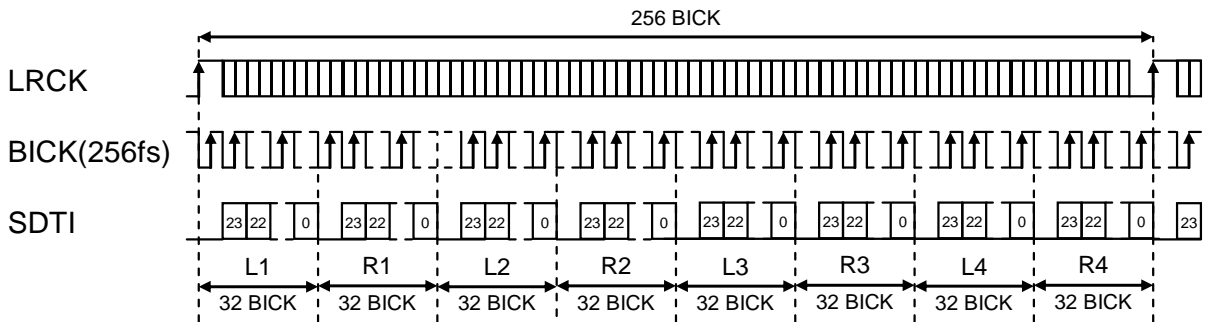


Figure 22. Mode 16 Timing

[2] Data Select

SDS1-0 bits control the playback channel of each DAC.

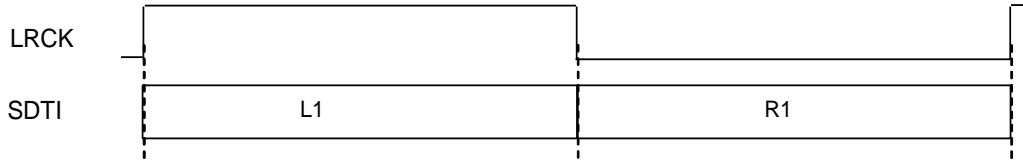


Figure 23. Data Slot in Normal Mode

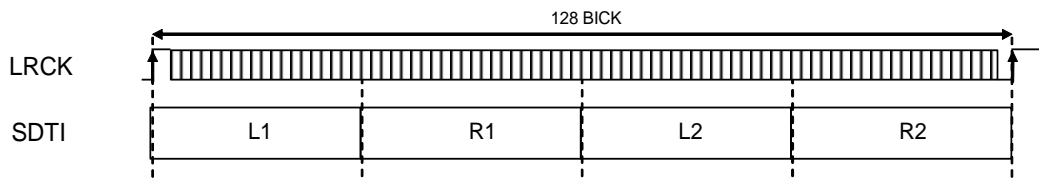


Figure 24. Data Slot in TDM128 Mode

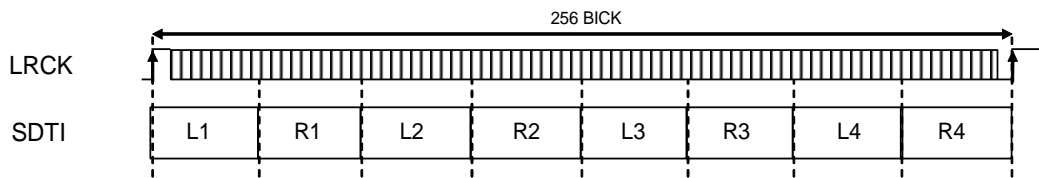


Figure 25. Data Slot in TDM256 Mode

| | SDS1 | SDS0 | DAC1 | |
|--------|------|------|------|-----|
| | | | Lch | Rch |
| Normal | x | x | L1 | R1 |
| TDM128 | x | 0 | L1 | R1 |
| | x | 1 | L2 | R2 |
| TDM256 | 0 | 0 | L1 | R1 |
| | 0 | 1 | L2 | R2 |
| | 1 | 0 | L3 | R3 |
| | 1 | 1 | L4 | R4 |

(x: don't care)

Table 8. Data Select

■ Digital Volume Function

The AK4432 has a channel-independent digital attenuator (256 levels, 0.5dB steps). Attenuation level of each channel of the DAC can be set by ATT7-0 bits (register 04-05H), respectively (Table 9).

| DAC Lch ATTL7-0bits | DAC Rch ATTR7-0bits | Attenuation Level |
|------------------------|------------------------|--------------------|
| 00h | 00h | +12.0dB |
| 01h | 01h | +11.5dB |
| 02h | 02h | +11.0dB |
| : | : | : |
| 17h | 17h | +0.5dB |
| 18h | 18h | 0.0dB |
| 19h | 19h | -0.5dB |
| : | : | : |
| FDh | FDh | -114.5dB |
| FEh | FEh | -115.0dB |
| FFh | FFh | MUTE ($-\infty$) |

(default)

Table 9. Attenuation level of Digital Attenuator

Transition time between set values of ATT7-0 bits can be selected by the ATS bit (Table 10). When changing output levels, transitions are executed via soft changes (0.125dB steps by every 1/4 ATT speed); thus not switching noise occurs during these transitions.

| Mode | ATS | ATT speed(Transition Time) | |
|------|-----|----------------------------|--------------------------|
| | | 1 step(0.5dB) | Soft Transition(0.125dB) |
| 0 | 0 | 4/fs | 1/fs |
| 1 | 1 | 16/fs | 4/fs |

(default)

Table 10. Digital Volume Transition Time

In Mode0, it takes $255\text{step} \cdot 4/\text{fs} + 1/\text{fs}(\text{mute}) = 1020/\text{fs}$ (21.3ms @fs=48kHz) from FFH to 00H and in Mode1, it takes $255\text{step} \cdot 16/\text{fs} + 4/\text{fs}(\text{mute}) = 4084/\text{fs}$ (85.1ms @fs=48kHz).

| Mode | ATS | 00h \leftrightarrow FFh Transition Time | | | |
|------|-----|---|----------|------------|---------|
| | | Transition Time(fs) | fs=48kHz | fs=44.1kHz | fs=8kHz |
| 0 | 0 | 1021/fs | 21.3ms | 23.2ms | 127.6ms |
| 1 | 1 | 4084/fs | 85.1ms | 92.6ms | 510.5ms |

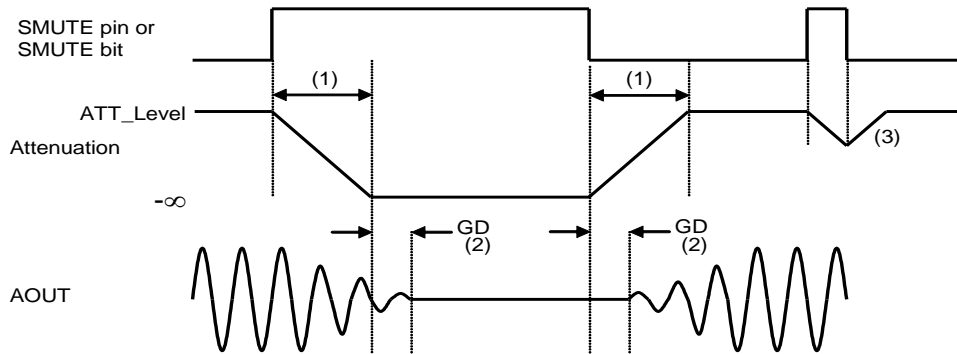
(default)

Table 11. Digital Volume Transition Time 00h \leftrightarrow FFh

Just after power up the DAC, the digital volume level is at MUTE. Then, the volume changes to the value set by registers in soft transition after releasing the power-down state.

■ Soft Mute Operation

The soft mute operation is performed at digital domain. When the SMUTE pin goes to “H” or set SMUTE bit to “1”, the output signal is attenuated by $-\infty$ during $ATT_DATA \times ATT$ transition time from the current ATT level. When the SMUTE pin is returned to “L” or the SMUTE bit is returned to “0”, the mute is cancelled and the output attenuation gradually changes to the ATT level during $ATT_DATA \times ATT$ transition time. If the soft mute is cancelled before attenuating $-\infty$, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Note:

- (1) $ATT_DATA \times ATT$ transition time. For example, this time is 1020LRCK cycles (1020/fs) at $ATT_DATA=255$ in Normal Speed Mode.
- (2) The analog output corresponding to the digital input has group delay (GD).
- (3) If the soft mute is cancelled before attenuating $-\infty$ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

Figure 26. Soft Mute Function and Zero Detection

■ Error Detection

Three types of error can be detected by the AK4432 (Table 12). The internal LDO will be powered down and register access will be disabled when an error is detected. Once an error is detected, the AK4432 will not return to normal operation automatically even if all error conditions are removed. Reset the AK4432 once by bringing the PDN pin = "L" and start up again. In I²C mode, errors can be detected by monitoring Acknowledge. If an error occurs, the AK4432 stops sending Acknowledge.

| No | Error | Error Condition |
|----|----------------------------------|---|
| 1 | Internal Reference Voltage Error | Internal reference voltage is not powered up. |
| 2 | LDO Over Voltage Detection | LDO voltage > 1.6V (Typ) |
| 3 | LDO Over Current Detection | LDO current < 100mA (Typ) |

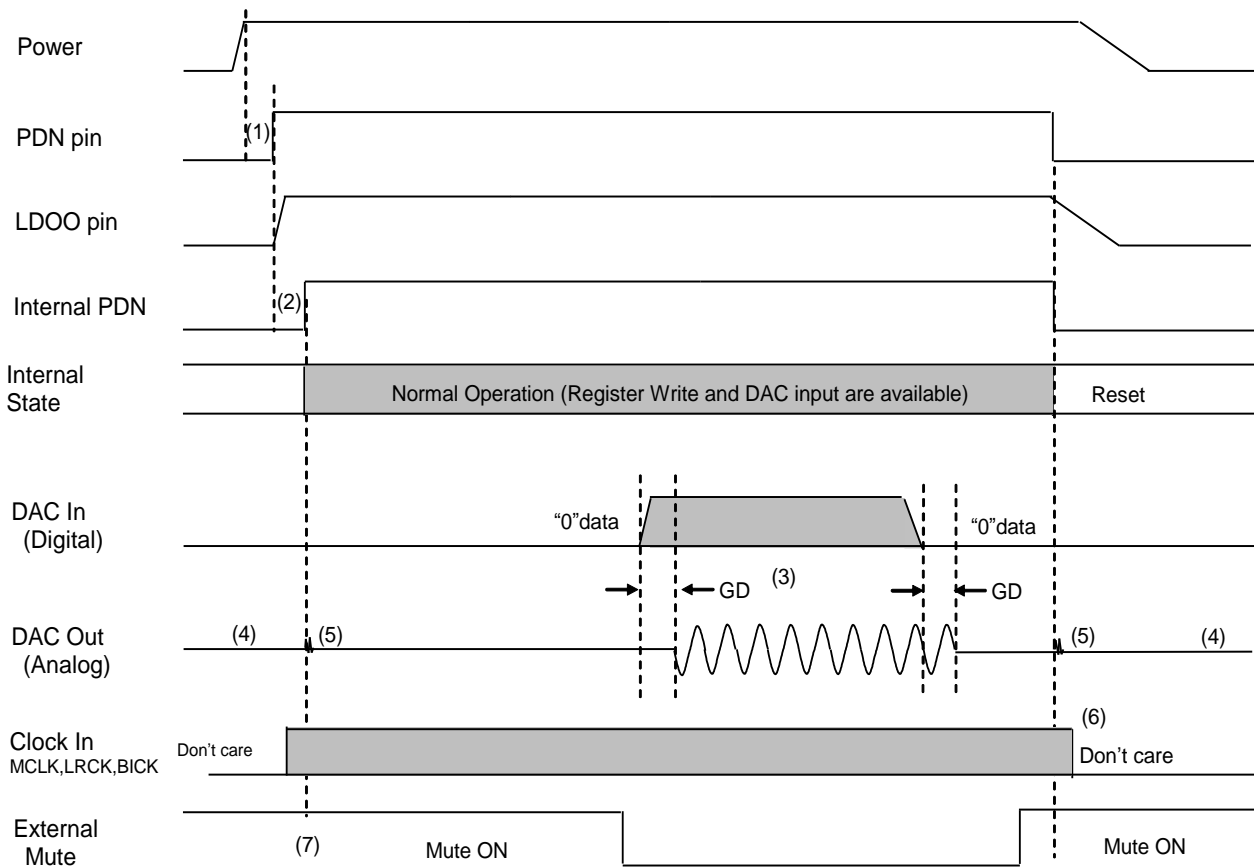
Table 12. ERROR Detection

■ System Reset

The AK4432 should be reset once by bringing the PDN pin = "L" upon power-up. Power-down state of the reference voltage such as LDO and VCOM will be released by the PDN pin = "H", and then after 1ms register writing becomes available. The internal DAC will be powered up after MCLK and LRCK are input. The AK4432 is in power-down state until MCLK and LRCK are input.

■ Power Down Function

The AK4432 is placed in power-down mode by bringing the PDN pin “L” and the analog outputs become floating (Hi-Z) state. Power-up and power-down timings are shown in [Figure 27](#).



Note:

- (1) After AVDD and LVDD are powered-up, the PDN pin should be “L” for 800ns.
- (2) After PDN pin = “H”, the LDO circuit (internal digital block driving power supply) and REF generating circuit (analog reference voltage source) are powered up, and control registers are initialized. Control register settings should be made after 1ms from the PDN pin = “H”.
- (3) The analog output corresponding to digital input has group delay (GD).
- (4) Analog outputs are floating (Hi-Z) in power down mode.
- (5) Click noise occurs at an edge of PDN signal. This noise is output even if “0” data is input.
- (6) MCLK, BICK and LRCK clocks can be stopped in power-down mode (PDN pin= “L”).
- (7) Mute the analog output externally if click noise (5) adversely affect system performance. The timing example is shown in this figure.

Figure 27. Pin Power Down/Up Sequence Example

■ Power Off and Reset Functions

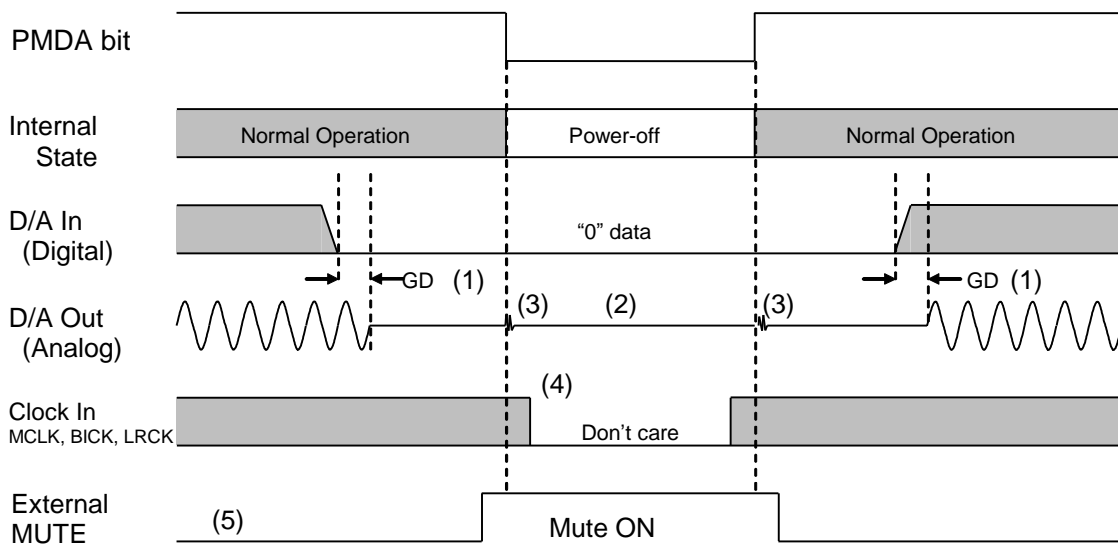
| PMDA | DAC | Register | Digital | Analog Output |
|------|-----|----------|---------|---------------|
| 0 | OFF | Keep | OFF | Hi-Z |
| 1 | ON | Keep | ON | normal |

(default)

Table 13. Power OFF and Reset Function

(1) Power OFF Function (PMDA bit)

All DACs will be powered down immediately by setting PMDA bit to “0”. In this time, all internal circuits except register are powered down and the analog output goes to floating state (Hi-z). Figure 28 shows a timing example of power-on and power-down.



Note:

- (1) The analog output corresponding to digital input has group delay (GD).
- (2) Analog outputs are floating (Hi-Z) in power down mode.
- (3) Click noise occurs at the edges (“↑↓”) of the internal timing of PMDA bit. This noise is output even if “0” data is input.
- (4) Each clock input (MCLK, BICK, LRCK) can be stopped in power down mode (PMDA bit = “0”).
- (5) Mute the analog output externally if the click noise (3) adversely affects system performance.

Figure 28. Power-off/on Sequence Example 1

■ Clock Synchronization

The AK4432 has a reset function of internal counter that keeps the phase difference of the DAC outputs between the AK7738 less than 13/256fs. Clock synchronization function is enabled by SYNCE bit = “1” (default = “1”). SYNCE bit setting must be changed when data is all “0” (no data input). When SYNCE bit = “1” (default) MSB justified and 32-bit I²S compatible formats are available but LSB justified format is not available.

(1) Synchronization with AK7738

In the use cases shown below (Figure 29), the phase difference of DAC output between the AK7738 and the AK4432 can be kept less than 13/256fs by clock synchronization function.

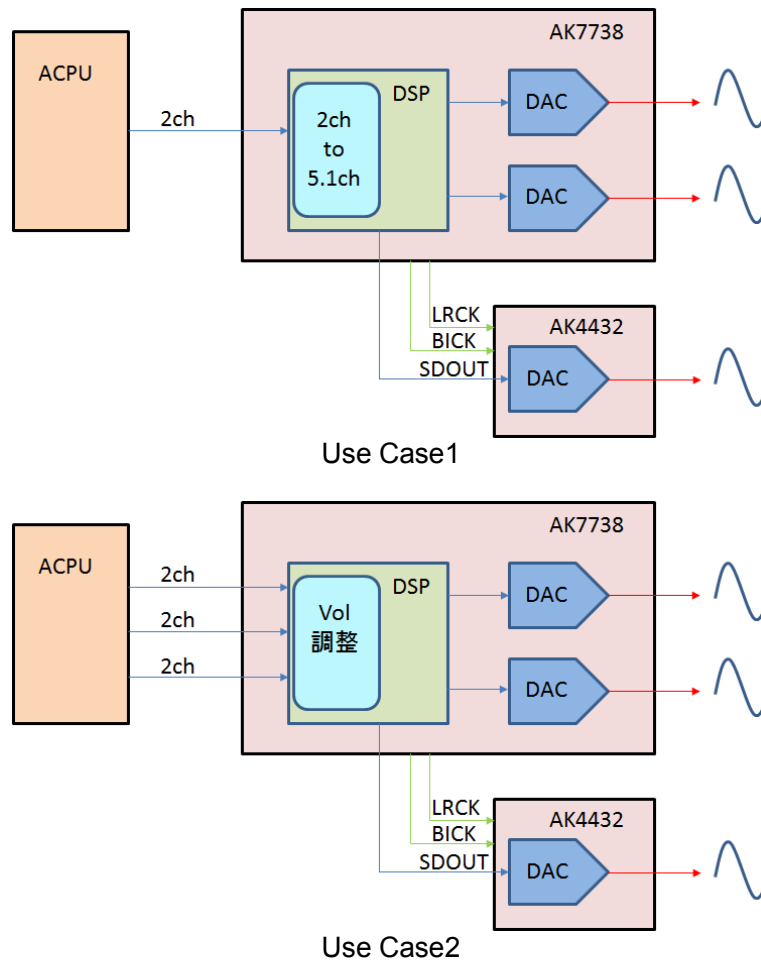


Figure 29. Available Use Cases for Synchronization with the AK7738

Note: When synchronizing with the AK7738, both the AK7738 and the AK4432 should be set as BICK =64fs, 32-bit MSB justified (DIF2-0 bits = “110”).

| | LRCK[kHz] | BICK[fs] | MCLK[fs] | MCLK[MHz] | Phase Diff. [1/MCLK] | Phase Diff. [μs] | Phase Diff. [deg] *1 |
|--------|-----------|----------|----------|-----------|----------------------|------------------|----------------------|
| Normal | 48 | 64 | 256 | 12.288 | 7 ~ 13 | 0.57 ~ 1.06 | 4.1 ~ 7.6 |
| Double | 96 | 64 | 256 | 24.576 | 9 ~ 12 | 0.37 ~ 0.49 | 2.6 ~ 3.5 |
| Quad | 192 | 64 | 128 | 24.576 | 7 ~ 10 | 0.29 ~ 0.41 | 2.1 ~ 2.9 |

Table 14. Phase Difference Relationship between the AK7738 and the AK4432

Note 16. Phase difference to a 20 kHz signal.

■ Parallel Mode

The AK4432 will be in parallel control mode (pin control mode) by bringing the PS pin= "H". In parallel mode, functions that need to set by registers are not available except three followings that can be used by pin settings.

Functions that cannot be controlled by pin settings are operated in their default register settings.

■ Audio Interface

The DIF pin controls audio interface mode (Table 15). Available modes are 32-bit MSB justified (DIF pin = "L") and 32-bit I2C compatible (DIF pin = "H").

| DIF pin | Mode |
|---------|-----------------|
| L | Mode6 (Table 7) |
| H | Mode7 (Table 7) |

Table 15. Audio Interface Forma (Parallel Mode)

■ Soft Mute

Soft mute function can be used by controlling SUMTE signal by the SMUTE pin. (Figure 26)

■ System Clock

Auto setting mode becomes available by setting the ACKS pin to "H". The AK4432 is in Manual setting mode when the ACKS pin is "L". In this case, the sampling speed is fixed to Normal speed mode (Table 16). Input MCKI frequency shown in Table 16.

| ACKS pin | MCKI | Sampling Speed Mode |
|----------|----------------------------|---------------------|
| L | 768fs, 512fs, 384fs, 256fs | Normal Speed Mode |
| H | 512fs, 768fs | Normal Speed Mode |
| H | 256fs, 384fs | Double Speed Mode |
| H | 128fs, 192fs | Quad Speed Mode |

Table 16. System Clock (Parallel Mode)

■ Serial Control Interface

The AK4432 corresponds to both 3-wire serial and I²C bus interfaces. After releasing power-down mode, the AK4432 is in I²C interface mode. 3-wire serial mode will be enabled by writing a dummy command four times continuously following power-up when the CSN pin = "H". (Figure 30)

Input "0cDE → 0xADDA → 0x7A" to the CDTI pin during the CSN pin = "L" is defined as a dummy command. The data format is MSB first. (Figure 30)

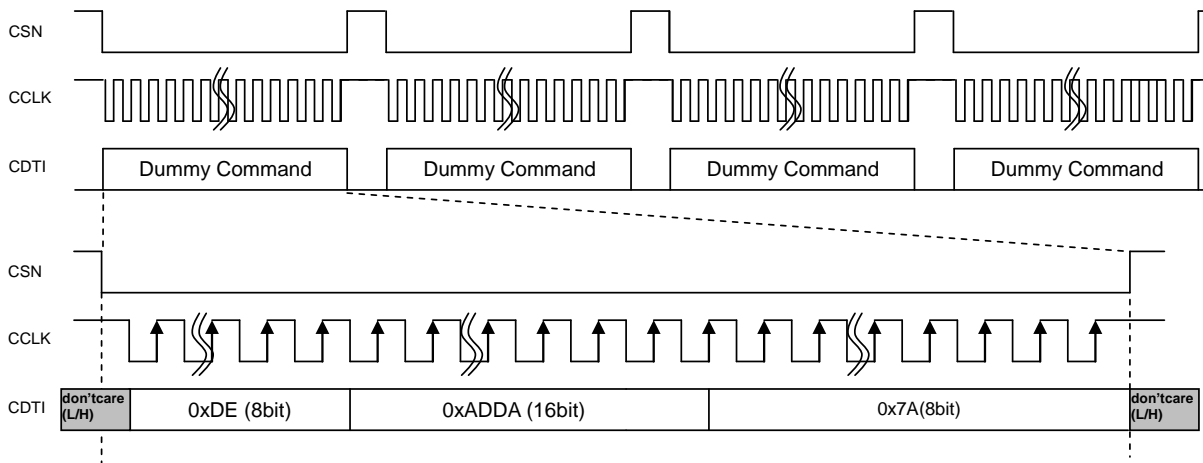


Figure 30. Dummy Comand Format

(1) 3-wire Serial Control Mode (I2C pin = "L")

The internal registers may be written through the 3-wire μ P interface pins (CSN, CCLK and CDTI). The data on this interface consists of a Command code (8bits, the most significant bit is R/W flag and fixed to "1" (write only) and other 7bits are fixed to "1000000"), Register address (MSB first, 16bits) and Control data (MSB first, 8bits) (Figure 31). Address and data are clocked in on the rising edge of CCLK and data is clocked out on the falling edge. For write operations, data is latched on the 8th rising edge of CCLK. The clock speed of CCLK is 7MHz (max).

The AK4432 can perform more than one byte write operation per sequence (Figure 35). The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 16-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 05H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

Internal registers are initialized by setting the PDN pin = "L".

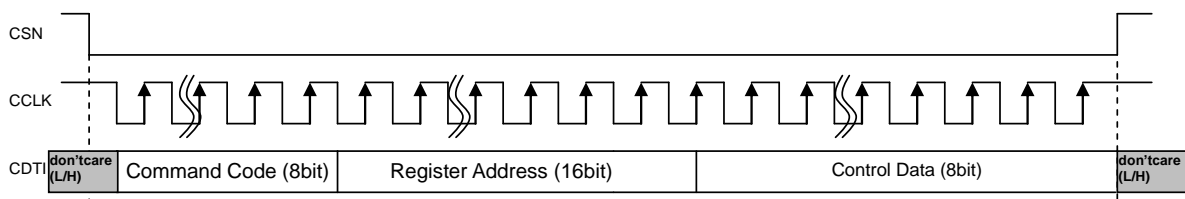
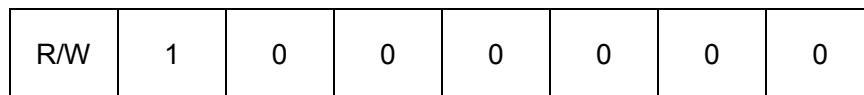


Figure 31. Control I/F Timing



R/W: READ/WRITE (Fixed to "1", Write only)

Figure 32. Command Code

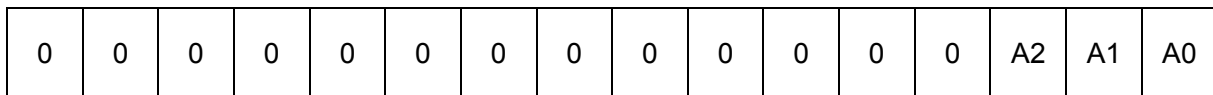


Figure 33. Register Address

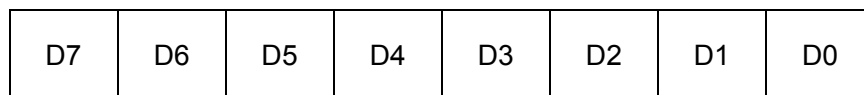


Figure 34. Control Data

- * The AK4432 does not support data read in 3-wire serial mode.
- * Control register write is not possible when the PDN pin = "L".
- * Data will not be written if there are 17times or more CCLK rising edges, or 15times or less CCLK rising edges while the CSN pin is "L".

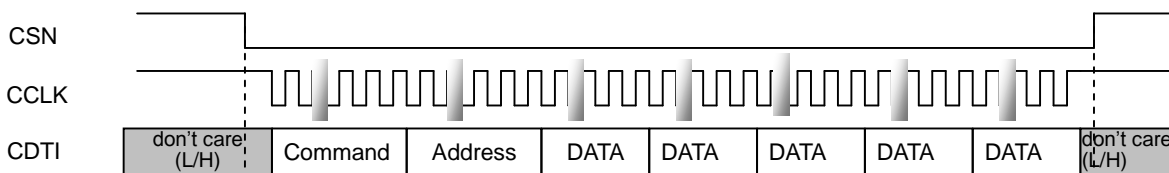


Figure 35. Continuous Write of Control Data

(2) I²C-bus Control Mode

The I²C-bus in the AK4432 can run in fast-mode (max: 400kHz) and fast-mode plus (max: 1MHz) (Table 17). I²C-bus mode should be fixed to either mode during operation. The PDN pin must be “L” when changing the I²C-bus mode.

| SMUTE/CSN/I2CFIL pin | Bus Mode |
|----------------------|----------------|
| L | Fast Mode |
| H | Fast Mode Plus |

Table 17. I²C-Bus Mode Setting

(1) WRITE Operation

Figure 36 shows the data transfer sequence of the I²C-bus mode. All commands are preceded by a START condition. A High to Low transition on the SDA line while SCL is HIGH indicates a START condition (Figure 44). After a START condition, a slave address is sent. This address is 7 bits long followed by the eighth bit that is a data direction bit (R/W). The most significant seven bits of the slave address are fixed as “0011001” (Figure 37). If the slave address matches that of the AK4432, the AK4432 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 45). R/W bit = “1” indicates that the read operation is to be executed. “0” indicates that the write operation is to be executed.

The second byte is an 8-bit command code. The format is MSB first, and it is fixed to “11000000” (Figure 38).

The third byte and fourth byte consist of the control register address of the AK4432. The format is MSB first, the third byte is fixed to zeros and the most significant 5bits of the fourth byte are fixed to zeros (Figure 39, Figure 40). The data after the fifth byte contains control data. The format is MSB first, 8bits (Figure 41). The AK4432 generates an acknowledge after each byte is received. Data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines STOP condition (Figure 44).

The AK4432 can perform more than one byte write operation per sequence. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 16-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds “05H” prior to generating a stop condition, the address counter will “roll over” to “00H” and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only be changed when the clock signal on the SCL line is LOW (Figure 46) except for the START and STOP conditions.

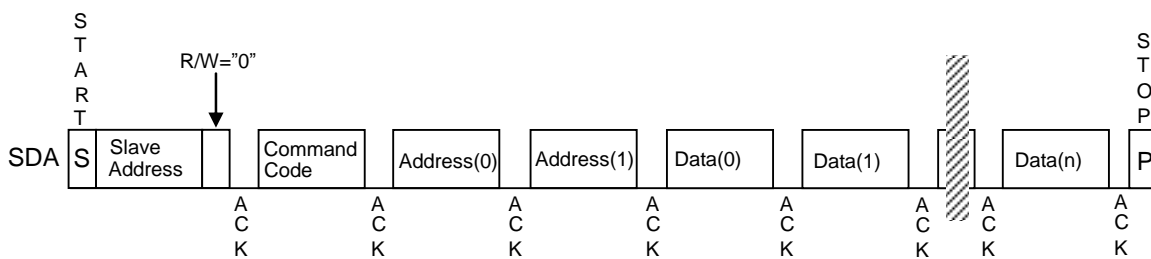
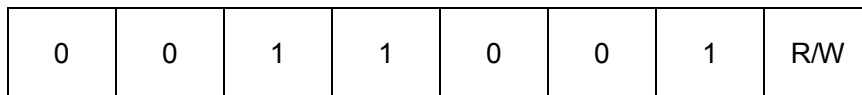


Figure 36. Data Transfer Sequence in I²C-bus Mode



R/W: READ/WRITE ("0": Write, "1": Read)

Figure 37. The First Byte

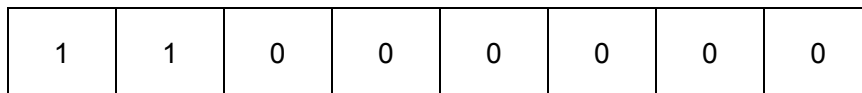


Figure 38. The Second Byte

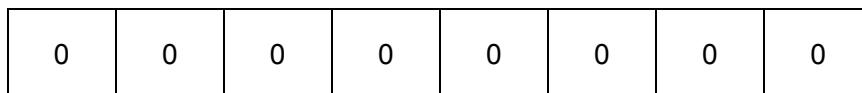


Figure 39. The Third Byte

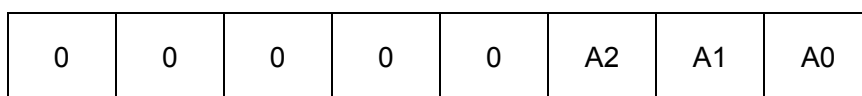


Figure 40. The Fourth Byte

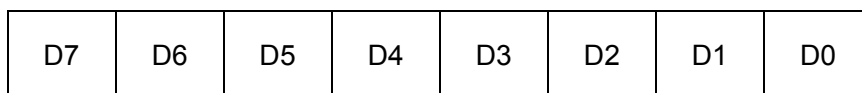


Figure 41. Byte Structure of The Fifth and Succeeding Bytes

(2) READ Operation

In the AK4432, when a “write- slave-address assignment” (R/W bit = “0”) is received at the first byte(Figure 37), the command code “01000000”(Figure 44) at the second byte and the address at the third and fourth bytes are received (Figure 39, Figure 40). When the fourth byte is received and an acknowledgement is transmitted, the read command waits for the next restart condition. After receiving the restart condition, if a “read slave-address assignment” is received at the first byte, data is transferred at the second and succeeding bytes. When the master does not generate an acknowledge but generates a stop condition instead, the AK4432 ceases transmission.

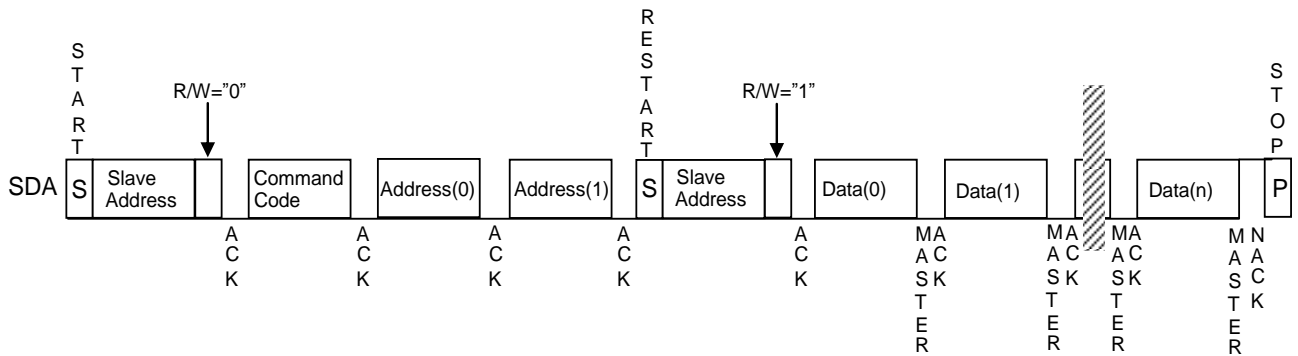


Figure 42. Random Address Read

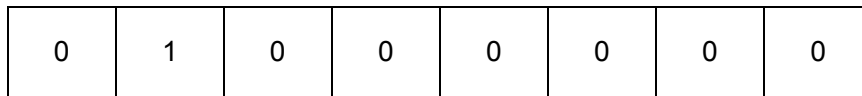


Figure 43. The Second Byte (READ)

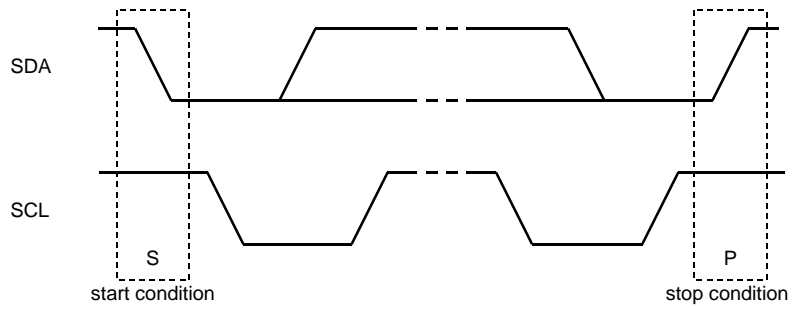


Figure 44. START and STOP Conditions

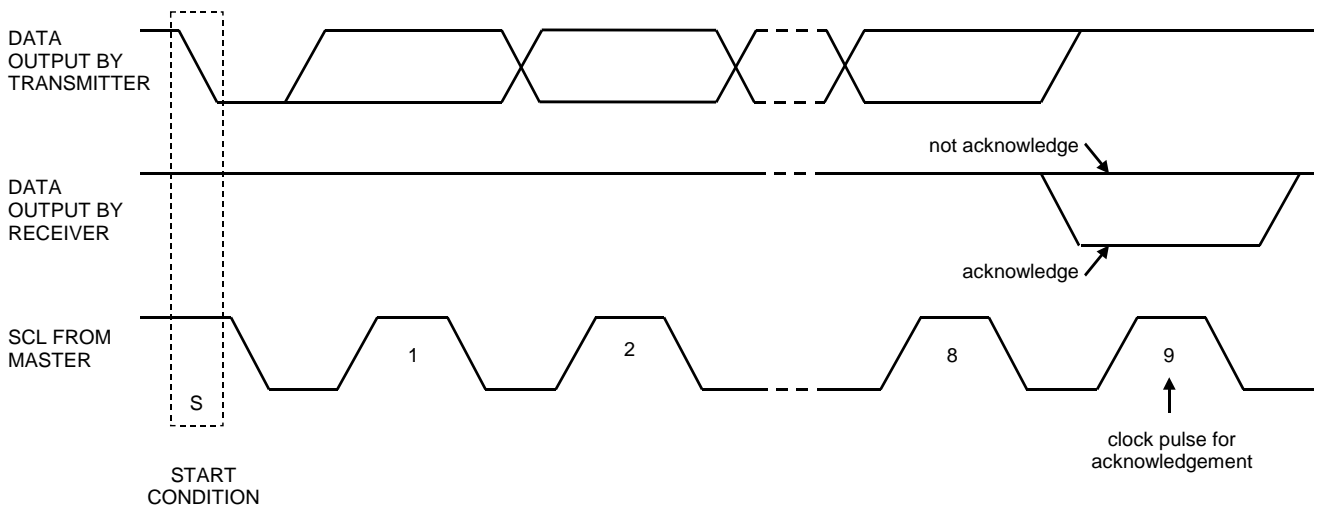


Figure 45. Acknowledge on the I²C-Bus

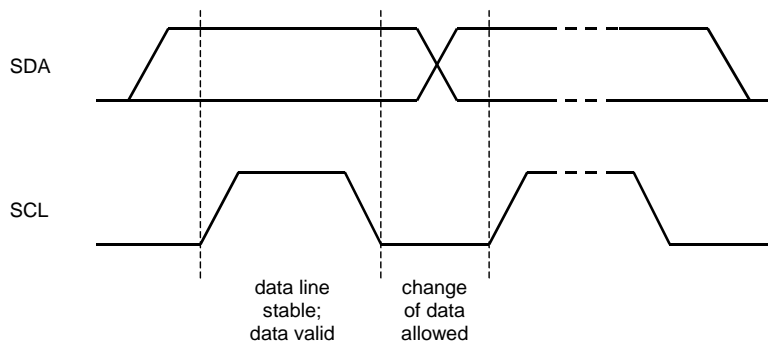


Figure 46. Bit Transfer on the I²C-Bus

■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 00H | Power Management | 0 | 0 | 0 | 0 | 0 | 0 | PMDA | 0 |
| 01H | Control 1 | 0 | 0 | 0 | 0 | 0 | DFS1 | DFS0 | ACKS |
| 02H | Data interface | 0 | SDS1 | SDS0 | TDM1 | TDM0 | DIF2 | DIF1 | DIF0 |
| 03H | Control 2 | 0 | 0 | 0 | DASL | DASD | ATS | SMUTE | SYNCE |
| 04H | AOUTL Volume Control | ATTL7 | ATTL6 | ATTL5 | ATTL4 | ATTL3 | ATTL2 | ATTL1 | ATTLO |
| 05H | AOUTR Volume Control | ATTR7 | ATTR6 | ATTR5 | ATTR4 | ATTR3 | ATTR2 | ATTR1 | ATTR0 |

Note 17. Data must not be written into addresses from 06H to FFH.

Note 18. The bit defined as 0 must contain a "0" value.

Note 19. When the PDN pin goes to "L", the registers are initialized to their default values.

■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|------------------|-----|-----|-----|-----|-----|-----|------|-----|
| 00H | Power Management | 0 | 0 | 0 | 0 | 0 | 0 | PMDA | 0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |

RMDA: DAC Power Management
 0: Power Down
 1: Normal Operation

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|-----|-----|-----|-----|-----|------|------|------|
| 01H | Control 1 | 0 | 0 | 0 | 0 | 0 | DFS1 | DFS0 | ACKS |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

ACKS: Master Clock Frequency Auto Setting Mode Enable
 0: Disable, Manual Setting Mode
 1: Enable, Auto Setting Mode
 When ACKS bit = "1", the MCLK frequency is detected automatically. In this case, the setting of DFS bits is ignored. When this bit is "0", DFS1-0 bits set the sampling speed mode and MCLK frequency for each mode is detected automatically.

DFS1-0: Sampling Speed Mode ([Table 1](#))
 The setting of DFS bits is ignored at ACKS bit = "1".

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------|-----|------|------|------|------|------|------|------|
| 02H | Data interface | 0 | SDS1 | SDS0 | TDM1 | TDM0 | DIF2 | DIF1 | DIF0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

DIF2-0: Audio Interface Mode Select ([Table 7](#))
 Default: "110" (32-bit MSB justified)

TDM1-0: TDM Format Select
 Default: "00" (Stereo Mode)

| Mode | TDM1 | TDM0 | Sampling Speed Mode |
|------|------|------|---|
| 0 | 0 | 0 | Stereo mode (Normal, Double, Quad Speed Mode) |
| 1 | 0 | 1 | TDM128 mode (Normal, Double, Quad Speed Mode) |
| 2 | 1 | 0 | TDM256 mode (Double, Quad Speed Mode) |
| 3 | 1 | 1 | TDM256 mode (Double, Quad Speed Mode) |

SDS1-0: DAC Data Select
 Default: "00" (Stereo Mode)
 0: Normal Operation
 1: Output Other Slot Data ([Table 8](#))

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|-----|-----|-----|------|------|-----|-------|-------|
| 03H | Control 2 | 0 | 0 | 0 | DASL | DASD | ATS | SMUTE | SYNCE |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

SYNCE: SYNC Mode Enable

0: OFF

1: ON (default)

SMUTE: Soft Mute Enable

0: Normal Operation

1: All DAC outputs are soft muted

ATS: Transition Time Setting of Digital Attenuator (Table 10)

Default: "00"

DASD: Digital Filter Setting for DAC Block

0: Sharp roll off filter or Slow roll off filter (default)

1: Short delay Sharp roll off filter or Short delay Slow roll off filter

DASL: Slow Roll-off Filter Enable for DAC Block

0: Sharp Roll-off Filter (default)

1: Slow Roll-off Filter

| DASD bit | DASL bit | Mode |
|----------|----------|-----------------------------------|
| 0 | 0 | Sharp roll-off filter |
| 0 | 1 | Slow roll-off filter |
| 1 | 0 | Short delay Sharp roll-off filter |
| 1 | 1 | Short delay Slow roll-off filter |

(default)

Table 18 Digital Filter setting for DAC Block

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----------------------|-------|-------|-------|-------|-------|-------|-------|-------|
| 04H | AOUTL Volume Control | ATTL7 | ATTL6 | ATTL5 | ATTL4 | ATTL3 | ATTL2 | ATTL1 | ATTL0 |
| 05H | AOUTR Volume Control | ATTR7 | ATTR6 | ATTR5 | ATTR4 | ATTR3 | ATTR2 | ATTR1 | ATTR0 |
| | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| | Default | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 |

ATTL7-0: DAC Lch Attenuation Level

Default:18(0dB)

ATTR7-0: DAC Rch Attenuation Level

Default:18(0dB)

13. Recommended External Circuits

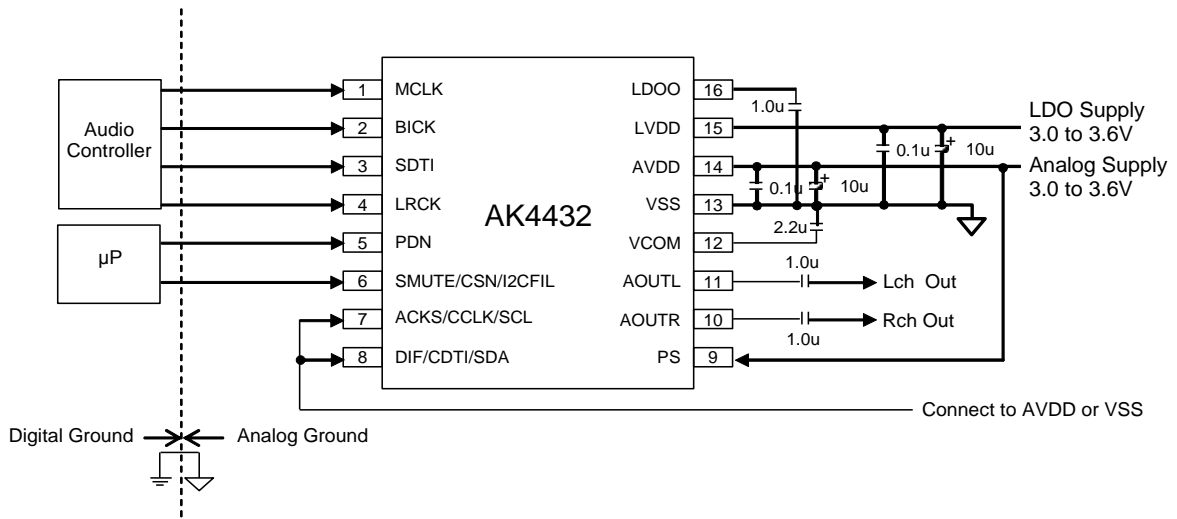


Figure 47. System Connection Diagram (P/S pin = "H")

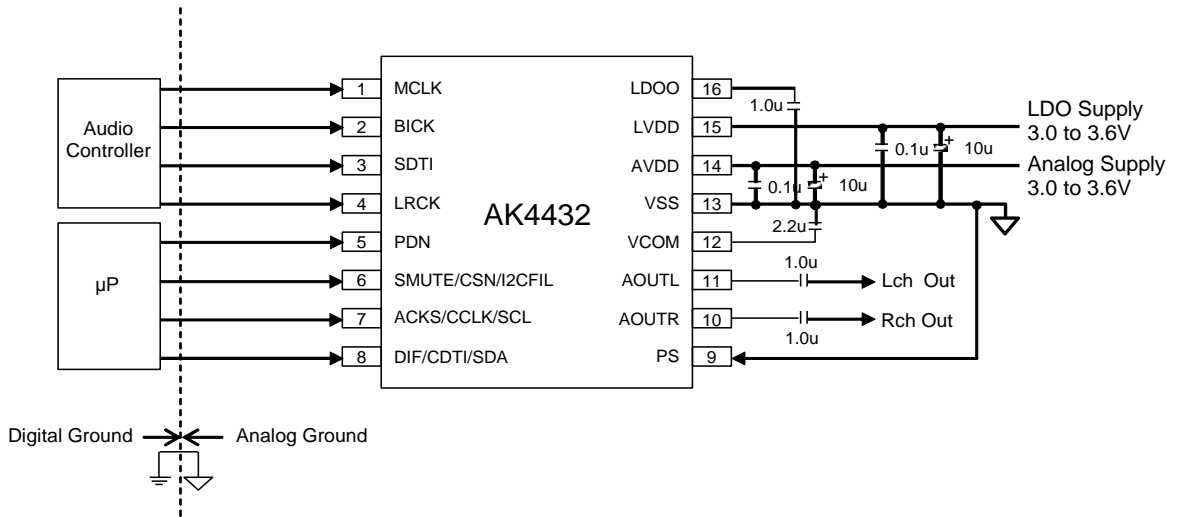


Figure 48. System Connection Diagram (P/S pin = "L")

1. Grounding and Power Supply Decoupling

The AK4432 requires careful attention to power supply and grounding arrangements. **VSS must be connected to the same analog ground plane.** Decoupling capacitors should be as near to the AK4432 as possible.

2. Voltage Reference

VCOM is a signal ground of this chip and output the voltage $AVDD \times 1/2$. A $2.2\mu\text{F}$ ($\pm 50\%$ includes temperature characteristics) ceramic capacitor attached between the VCOM pin and VSS eliminates the effects of high frequency noise. This capacitor should be as close to the pin as possible. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK4432.

The LDOO pin is a power supply for internal digital circuit and outputs 1.2V. A $1\mu\text{F}$ ($\pm 50\%$ includes temperature characteristics) ceramic capacitor attached between the LDOO pin and VSS eliminates the effects of high frequency noise. This capacitor should be connected as close as possible to the pin. No load current may be drawn from the LDOO pin.

3. Analog Output

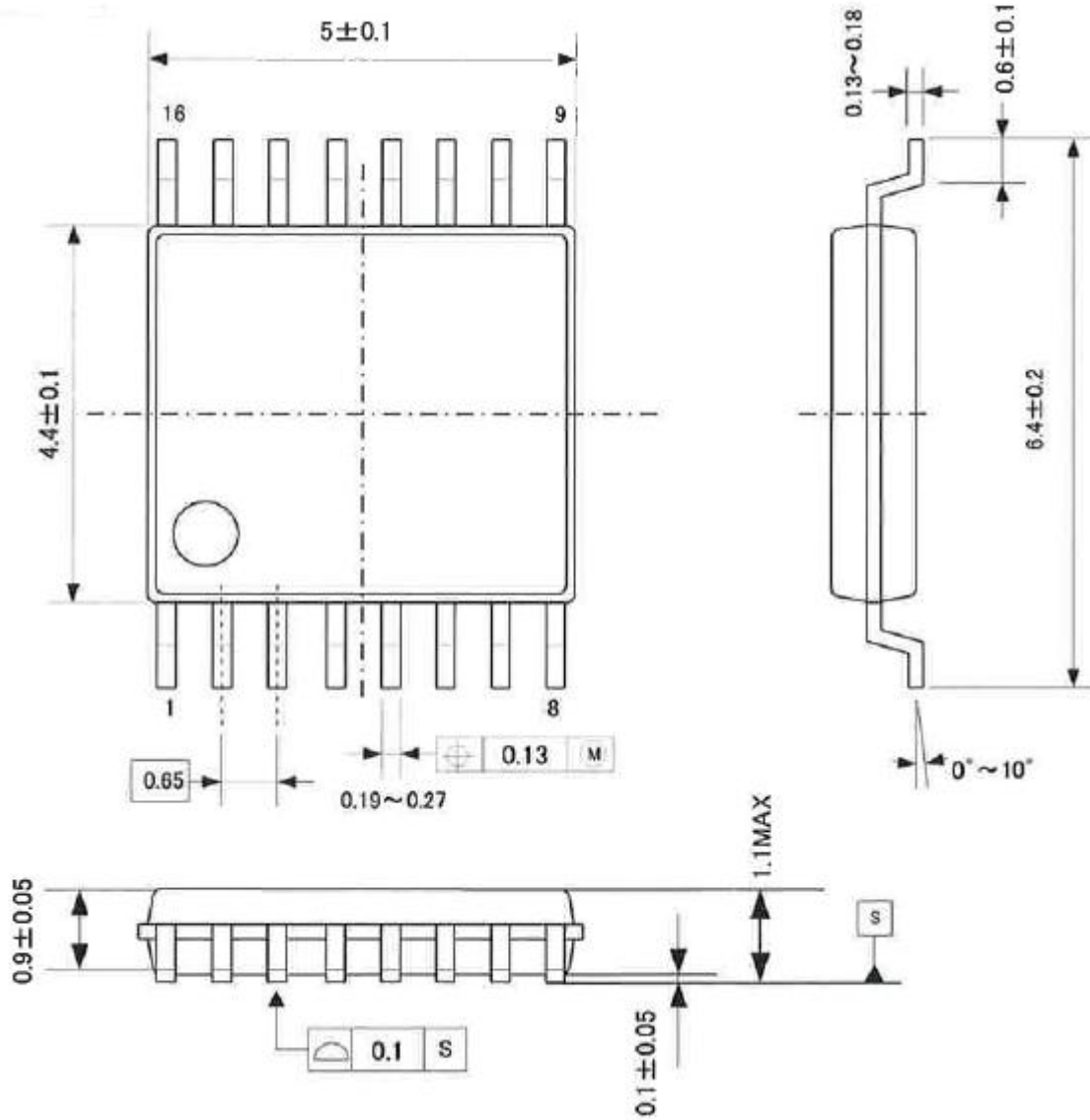
The output signal range is nominally $0.86 \times AVDD V_{pp}$ (typ.) centered around the VCOM voltage. The DAC input data format is 2's complement. The output voltage is a positive full scale for 7FFFFFFH(@32bit) and a negative full scale for 80000000H(@32bit). The ideal output is VCOM voltage for 00000000H(@32bit). The internal analog filters remove most of the noise generated by the delta-sigma modulator of DAC beyond the audio passband, in single-ended input mode.

DC offsets on analog outputs are eliminated by AC coupling since DAC outputs have DC offsets of a few mV.

14. Package

■ Outline Dimensions

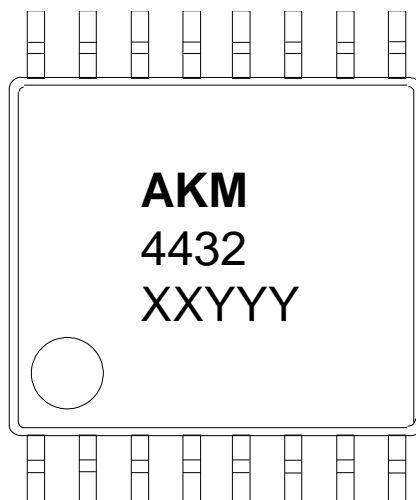
16-pin TSSOP (Unit: mm)



■ Material & Lead Finish

Package molding compound: Epoxy, Halogen (Br and Cl) free
 Lead frame material: Cu
 Lead frame surface treatment: Solder (Pb free) plate

■ **Marking**



- 1) Pin #1 indication
- 2) Date Code: XXXX (4 digits)
- 3) Marking Code: 4432

15. Revision History

| Date (Y/M/D) | Revision | Reason | Page | Contents |
|--------------|----------|---------------|------|----------|
| 15/02/18 | 00 | First Edition | | |

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