WINSOURCE
ELECTRONICS

THE DATASHEET OF

ADUM5400CRWZ

Quad-Channel Isolator with Integrated DC-to-DC Converter

Data Sheet

ADuM5400

FEATURES

- ***iso*Power integrated, isolated dc-to-dc converter**
- **Regulated 5 V output**
- **500 mW output power**
- **Quad dc-to-25 Mbps (NRZ) signal isolation channels**
- **Schmitt trigger inputs**
- **16-lead SOIC package with >7.6 mm creepage**
- **High temperature operation: 105°C maximum**
- **High common-mode transient immunity: >25 kV/μs**
- **Safety and regulatory approvals**
  - **UL recognition**
    - **2500 V rms for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice #5A**
  - **VDE certificate of conformity (pending)**
    - **IEC 60747-5-2 (VDE 0884, Part 2)**
    - **V_{IORM} = 560 V peak**

APPLICATIONS

- **RS-232/RS-422/RS-485 transceivers**
- **Industrial field bus isolation**
- **Power supply start-up bias and gate drives**
- **Isolated sensor interfaces**
- **Industrial PLCs**

GENERAL DESCRIPTION

The ADuM5400[1] device is a quad-channel digital isolator with *iso*Power®, an integrated, isolated dc-to-dc converter. Based on the Analog Devices, Inc., *i*Coupler® technology, the dc-to-dc converter provides up to 500 mW of regulated, isolated power with 5.0 V input and 5.0 V output voltages. This architecture eliminates the need for a separate, isolated dc-to-dc converter in low power, isolated designs. The *i*Coupler chip scale transformer technology is used to isolate the logic signals and the magnetic components of the dc-to-dc converter. The result is a small form factor, total isolation solution.

The ADuM5400 isolator provides four independent isolation channels in two speed grades (see the Ordering Guide for more information).

*iso*Power uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to the AN-0971 Application Note for details on board layout recommendations.

FUNCTIONAL BLOCK DIAGRAM

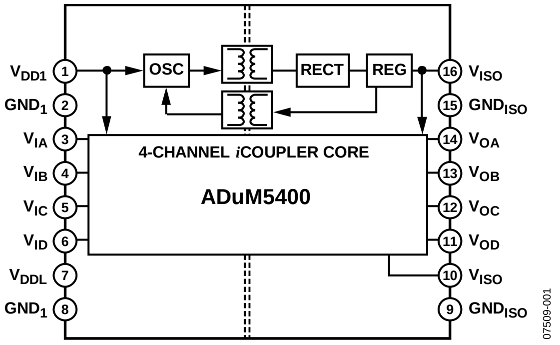

Figure 1.

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[1] Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329.

Rev. B

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REVISION HISTORY

6/12—Rev. A to Rev. B

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9/11—Rev. 0 to Rev. A

Changes to Features Section ... 1
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Added Table 2 and Table 3; Renumbered Sequentially ... 3
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10/08—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

4.5 V ≤ V_{DD1} ≤ 5.5 V; each voltage is relative to its respective ground. All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 5.0 V, V_{ISO} = 5.0 V.

Table 1. DC-to-DC Converter Static Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC-TO-DC CONVERTER SUPPLY						
Setpoint	V_{ISO}	4.7	5.0	5.4	V	I_{ISO} = 0 mA
Line Regulation	$V_{ISO(LINE)}$		1		mV/V	I_{ISO} = 50 mA, V_{DD1} = 4.5 V to 5.5 V
Load Regulation	$V_{ISO(LOAD)}$		1	5	%	I_{ISO} = 10 mA to 90 mA
Output Ripple	$V_{ISO(RIP)}$		75		mV p-p	20 MHz bandwidth, C_{BO}[1] = 0.1 µF||10 µF, I_{ISO} = 90 mA
Output Noise	$V_{ISO(NOISE)}$		200		mV p-p	C_{BO}[1] = 0.1 µF||10 µF, I_{ISO} = 90 mA
Switching Frequency	f_{OSC}		180		MHz	
PWM Frequency	f_{PWM}		625		kHz	
Output Supply Current	$I_{ISO(MAX)}$	100			mA	V_{ISO} > 4.5 V
Efficiency at $I_{ISO(MAX)}$			34		%	I_{ISO} = 100 mA
I_{DD1}, No V_{ISO} Load	$I_{DD1(Q)}$		19	30	mA	
I_{DD1}, Full V_{ISO} Load	$I_{DD1(MAX)}$		290		mA	

[1] C_{BO} = capacitive bypass output. This represents the parallel combination of high frequency bypass capacitors between Pin 15 and Pin 16.

Table 2. DC-to-DC Converter Dynamic Specifications

		1 Mbps—A Grade, C Grade			25 Mbps—C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT									
Input	I_{DD1}		19			64		mA	No V_{ISO} load
Available to Load	$I_{ISO(LOAD)}$		100			89		mA	

Table 3. Switching Specifications

		A Grade			C Grade				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS									
Maximum Data Rate				1			25	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		55	100		45	60	ns	50% input to 50% output
Pulse Width Distortion	PWD			40			6	ns	$\|t_{PLH} - t_{PHL}\|$
Change vs. Temperature						5		ps/°C	
Minimum Pulse Width	PW	1000			40			ns	Within PWD limit
Propagation Delay Skew	t_{PSK}			50			15	ns	Between any two units
Channel-to-Channel Matching	t_{PSKCD}/t_{PSKOD}			50			6	ns	

Table 4. Input and Output Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Logic High Input Threshold	V_{IH}	$0.7 \times V_{DD1}$			V	
Logic Low Input Threshold	V_{IL}			$0.3 \times V_{DD1}$	V	
Logic High Output Voltages	V_{OH}	$V_{ISO} - 0.3$	5.0		V	$I_{Ox} = -20\ \mu A$, $V_{Ix} = V_{IxH}$
		$V_{ISO} - 0.5$	4.8		V	$I_{Ox} = -4\ mA$, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OL}		0.0	0.1	V	$I_{Ox} = 20\ \mu A$, $V_{Ix} = V_{IxL}$
			0.0	0.4	V	$I_{Ox} = 4\ mA$, $V_{Ix} = V_{IxL}$
Undervoltage Lockout	UVLO					V_{DD1}, V_{DDL}, V_{ISO} supplies
Positive Going Threshold	V_{UV+}		2.7		V	
Negative Going Threshold	V_{UV-}		2.4		V	
Hysteresis	V_{UVH}		0.3		V	
Input Currents per Channel	I_I	−20	+0.01	+20	μA	$0\ V \leq V_{Ix} \leq V_{DDx}$
AC SPECIFICATIONS						
Output Rise/Fall Time	t_R/t_F		2.5		ns	10% to 90%
Common-Mode Transient Immunity[1]	|CM|	25	35		kV/μs	$V_{Ix} = V_{DD1}$ or V_{ISO}, $V_{CM} = 1000\ V$, transient magnitude = 800 V
Refresh Rate	f_r		1.0		Mbps	

[1] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.7 \times V_{DD1}$ or $0.7 \times V_{ISO}$ for a high output or $V_O < 0.3 \times V_{DD1}$ or $0.3 \times V_{ISO}$ for a low output. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

PACKAGE CHARACTERISTICS

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
RESISTANCE AND CAPACITANCE						
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2.2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	θ_{JA}		45		°C/W	Thermocouple located at center of package underside; test conducted on 4-layer board with thin traces[3]

[1] This device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.
[3] See the Thermal Analysis section for thermal model definitions.

REGULATORY INFORMATION

The ADuM5400 is approved by the organizations listed in Table 6. Refer to Table 11 and to the Insulation Lifetime section for details regarding the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 6.

UL[1]	CSA	VDE (Pending)[2]
Recognized Under 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to IEC 60747-5-2 (VDE 0884 Part 2):2003-01[2]
Single Protection, 2500 V rms Isolation Voltage	Testing was conducted per CSA 60950-1-07 and IEC 60950-1 2nd Ed. at 2.5 kV rated voltage Basic insulation at 600 V rms (848 V peak) working voltage Reinforced insulation at 250 V rms (353 V peak) working voltage	Basic insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM5400 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 10 µA).
[2] In accordance with IEC 60747-5-2 (VDE 0884 Part 2):2003-01, each ADuM5400 is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates IEC 60747-5-2 (VDE 0884 Part 2):2003-01 approval.

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 7. Critical Safety Related Dimensions and Material Properties

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap	L(I01)	8.0	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Material Group		IIIa		Material group (DIN VDE 0110, 1/89, Table 1)

IEC 60747-5-2 (VDE 0884, PART 2):2003-01 INSULATION CHARACTERISTICS

The ADuM5400 is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking branded on the component denotes IEC 60747-5-2 (VDE 0884, Part 2) approval.

Table 8. VDE Characteristics

Description	Conditions	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V_{PEAK}
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m =$ 1 sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V_{PEAK}
Input-to-Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	840	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	4000	V_{PEAK}
Withstand Isolation Voltage	1 minute withstand rating	V_{ISO}	2500	V_{RMS}
Surge Isolation Voltage	$V_{PEAK} = 6$ kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	6000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 2)			
Case Temperature		T_S	150	°C
Side 1 I_{DD1} Current		I_{S1}	555	mA
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

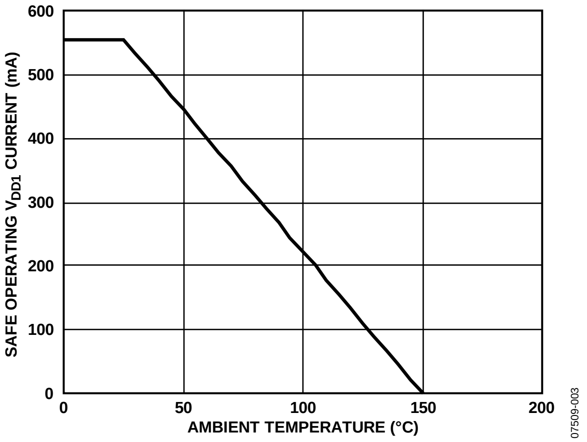


Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN EN 60747-5-2

RECOMMENDED OPERATING CONDITIONS

Table 9.

Parameter	Symbol	Min	Max	Unit
Operating Temperature Range	T_A	−40	+105	°C
Supply Voltages[1]	V_{DD}	4.5	5.5	V

[1] Each voltage is relative to its respective ground.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 10.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Ambient Operating Temperature (T_A)	−40°C to +85°C
Supply Voltages (V_{DD1}, V_{ISO})[1]	−0.5 V to +7.0 V
V_{ISO} Supply Current[2]	
−40°C to +85°C	100 mA
−40°C to +105°C	60 mA
Input Voltage (V_{IA}, V_{IB}, V_{IC}, V_{ID})[1, 3]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage (V_{OA}, V_{OB}, V_{OC}, V_{OD})[1, 3]	−0.5 V to V_{ISO} + 0.5 V
Average Output Current per Data Output Pin[4]	−10 mA to +10 mA
Common-Mode Transients[5]	−100 kV/µs to +100 kV/µs

[1] Each voltage is relative to its respective ground.

[2] V_{ISO} provides current for dc and dynamic loads on the Side 2 I/O channels. This current must be included when determining the total V_{ISO} supply current.

[3] V_{DDI} and V_{ISO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PCB Layout section.

[4] See Figure 2 for maximum rated current values for various temperatures.

[5] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 11. Maximum Continuous Working Voltage Supporting 50-Year Minimum Lifetime[1]

Parameter	Max	Unit	Applicable Certification
AC Voltage, Bipolar Waveform	424	V peak	All certifications, 50 year operation
AC Voltage, Unipolar Waveform			
Basic Insulation	600	V peak	Working voltage per IEC 60950-1
Reinforced Insulation	353	V peak	Working voltage per IEC 60950-1
DC Voltage			
Basic Insulation	600	V peak	Working voltage per IEC 60950-1
Reinforced Insulation	353	V peak	Working voltage per IEC 60950-1

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

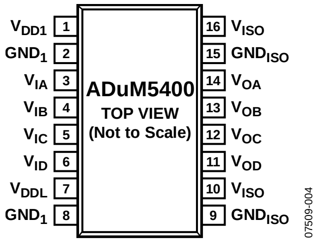


Figure 3. Pin Configuration

Table 12. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Primary Supply Voltage, 4.5 V to 5.5 V.
2, 8	GND_1	Ground 1. Ground reference for isolator primary. Pin 2 and Pin 8 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	V_{DDL}	Logic Power Supply Voltage. This pin must be connected to V_{DD1} and have a dedicated bypass capacitor.
9, 15	GND_{ISO}	Ground Reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected to each other, and it is recommended that both pins be connected to a common ground.
10, 16	V_{ISO}	Secondary Supply Voltage Output for External Loads, 5.0 V. These pins are not tied together internally and must be connected together on the PCB.
11	V_{OD}	Logic Output D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.

Table 13. Truth Table (Positive Logic)

V_{Ix} Input[1]	V_{DD1}/V_{DDL} State	V_{DD1}/V_{DDL} Input (V)	V_{ISO} State	V_{ISO} Output (V)	V_{Ox} Output[1]	Operation
High	Powered	5.0	Powered	5.0	High	Normal operation, data is high
Low	Powered	5.0	Powered	5.0	Low	Normal operation, data is low

[1] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D).

TYPICAL PERFORMANCE CHARACTERISTICS

Each voltage is relative to its respective ground; all typical specifications are at T_A = 25°C.

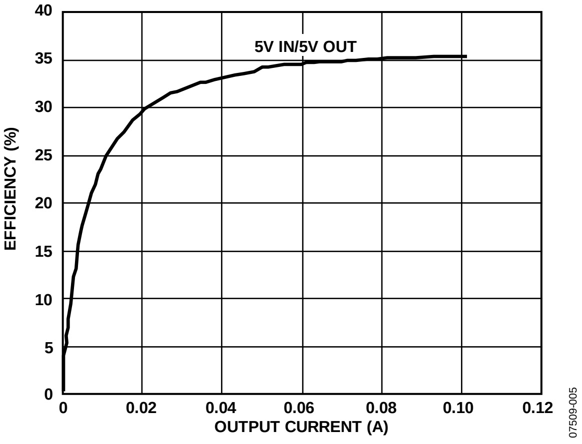


Figure 4. Typical Power Supply Efficiency at 5 V/5 V

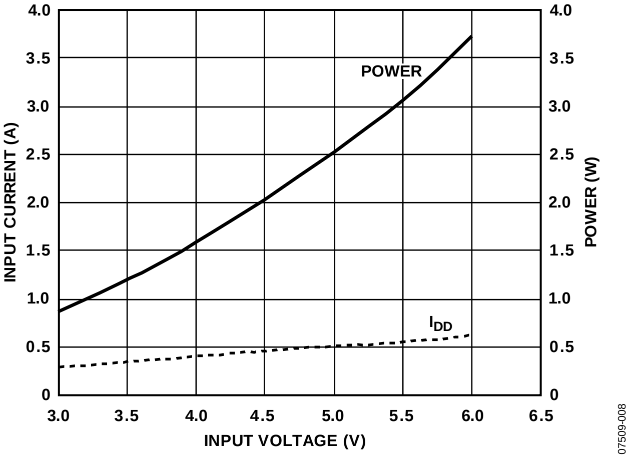


Figure 7. Typical Short-Circuit Input Current and Power vs. V_{DD1} Supply Voltage

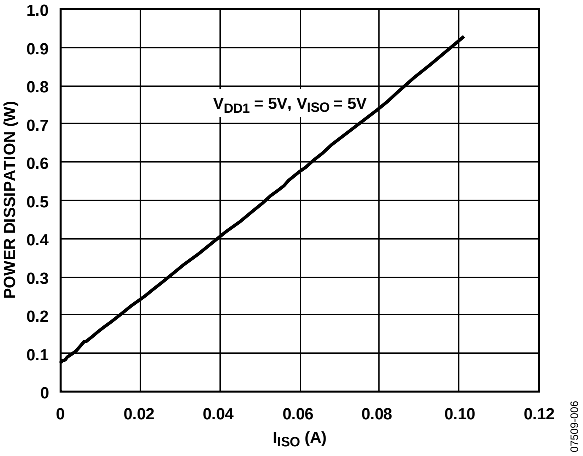


Figure 5. Typical Total Power Dissipation vs. I_{ISO} with Data Channels Idle

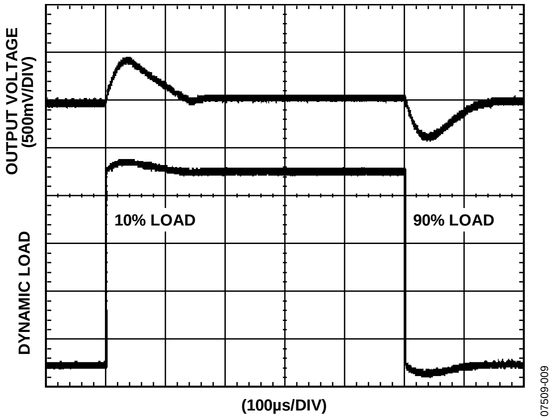


Figure 8. Typical V_{ISO} Transient Load Response, 5 V Output, 10% to 90% Load Step

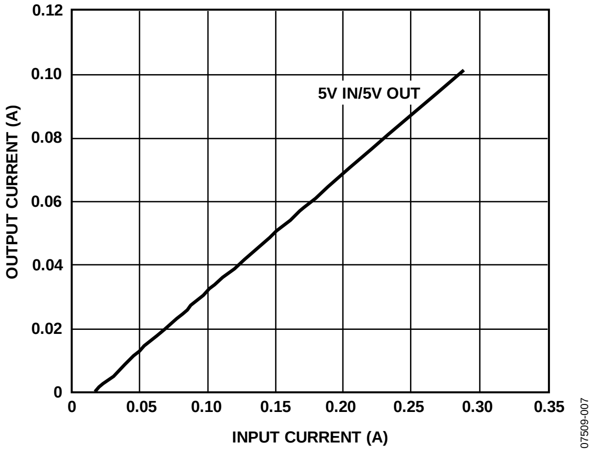


Figure 6. Typical Isolated Output Supply Current, I_{ISO}, as a Function of External Load, No Dynamic Current Draw at 5 V/5 V

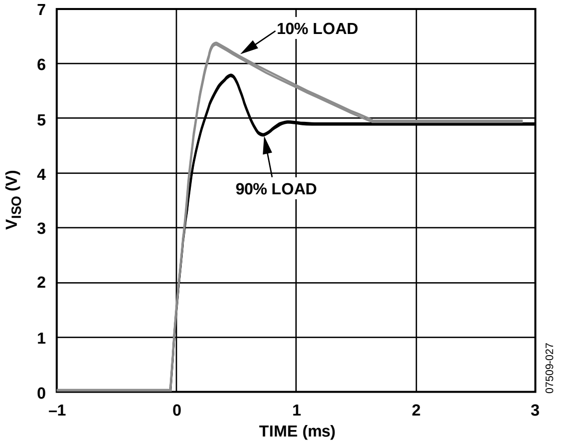


Figure 9. Typical V_{ISO} = 5 V Output Voltage Start-Up Transient at 10% and 90% Load

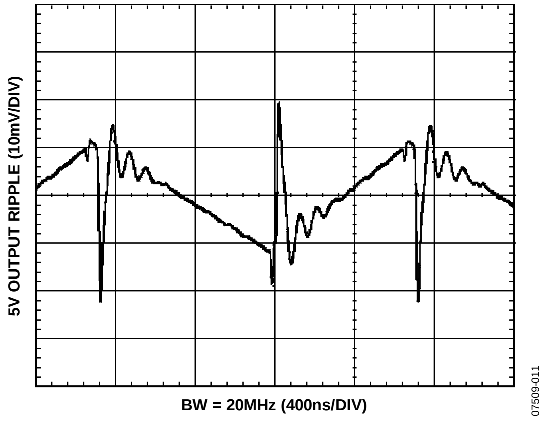


Figure 10. Typical V_{ISO} = 5 V Output Voltage Ripple at 90% Load

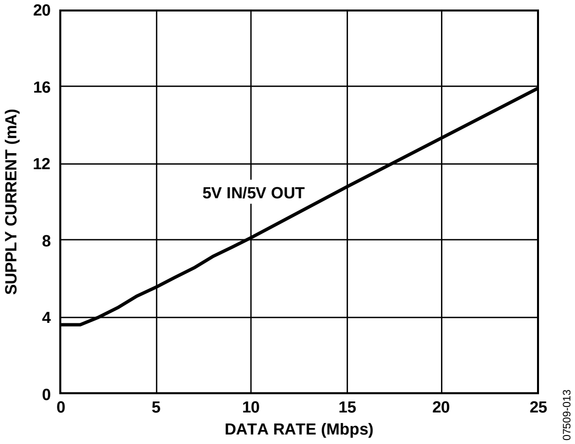


Figure 12. Typical I_{CH} Supply Current per Forward Data Channel (15 pF Output Load)

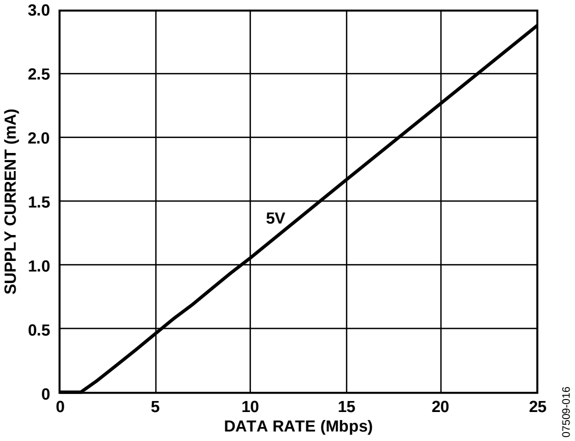


Figure 11. Typical $I_{ISO(D)}$ Dynamic Supply Current per Output (15 pF Output Load)

TERMINOLOGY

$I_{DD1(Q)}$

$I_{DD1(Q)}$ is the minimum operating current drawn at the V_{DD1} pin when there is no external load at V_{ISO} and the I/O pins are operating below 2 Mbps, requiring no additional dynamic supply current.

$I_{DD1(MAX)}$

$I_{DD1(MAX)}$ is the input current under full dynamic and V_{ISO} load conditions.

t_{PHL} Propagation Delay

t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{Ix} signal to the 50% level of the falling edge of the V_{Ox} signal.

t_{PLH} Propagation Delay

t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{Ix} signal to the 50% level of the rising edge of the V_{Ox} signal.

Propagation Delay Skew (t_{PSK})

t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Channel-to-Channel Matching

Channel-to-channel matching is the absolute value of the difference in propagation delays between two channels when operated with identical loads.

Minimum Pulse Width

The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

Maximum Data Rate

The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

APPLICATIONS INFORMATION

The dc-to-dc converter section of the ADuM5400 works on principles that are common to most modern power supplies. It has a secondary side controller architecture with isolated pulse-width modulation (PWM) feedback. V_{DD1} power is supplied to an oscillating circuit that switches current into a chip scale air core transformer. Power transferred to the secondary side is rectified and regulated to 5 V. The secondary (V_{ISO}) side controller regulates the output by creating a PWM control signal that is sent to the primary (V_{DD1}) side by a dedicated *i*Coupler data channel. The PWM modulates the oscillator circuit to control the power being sent to the secondary side. Feedback allows for significantly higher power and efficiency.

The ADuM5400 implements undervoltage lockout (UVLO) with hysteresis on the V_{DD1}, V_{DDL}, and V_{ISO} power supplies. This feature ensures that the converter does not enter oscillation due to noisy input power or slow power-on ramp rates.

PCB LAYOUT

The ADuM5400 digital isolator with integrated 0.5 W *iso*Power dc-to-dc converter requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 13). Note that a low ESR bypass capacitor is required between Pin 1 and Pin 2, within 2 mm of the chip leads.

The power supply section of the ADuM5400 uses a 180 MHz oscillator frequency to efficiently pass power through its chip scale transformers. In addition, normal operation of the data section of the *i*Coupler introduces switching transients on the power supply pins. Bypass capacitors are required and must provide transient suppression at several operating frequencies. Noise suppression requires a low inductance, high frequency capacitor that is effective at 180 MHz and 360 MHz. Ripple suppression and proper regulation require a large value capacitor to provide bulk current at 625 kHz. These are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{ISO}. To suppress noise and reduce ripple, a parallel combination of at least two capacitors is required. The recommended capacitor values are 0.1 µF and 10 µF for V_{DD1}. The smaller capacitor must have low ESR; for example, use of a ceramic capacitor is advised.

Note that the total lead length between the ends of the low ESR capacitor and the input power supply pin must not exceed 2 mm. Installing the bypass capacitor with traces more than 2 mm in length may result in data corruption. Consider a bypass capacitor between Pin 1 and Pin 8 and between Pin 9 and Pin 16 unless both common ground pins are connected together close to the package.

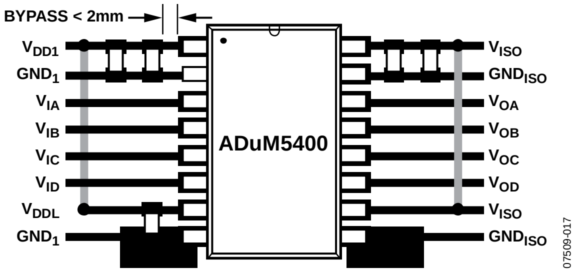


Figure 13. Recommended PCB Layout

In applications involving high common-mode transients, ensure that board capacitive coupling across the isolation barrier is minimized. Furthermore, design the board layout so that any coupling that does occur affects all pins on a given component side equally. Failure to ensure this can cause differential voltages between pins, exceeding the absolute maximum ratings for the device (specified in Table 10) and thereby leading to latch-up and/or permanent damage.

The ADuM5400 is a power device that dissipates about 1 W of power when fully loaded and running at maximum speed. Because it is not possible to apply a heat sink to an isolation device, the device depends primarily on heat dissipation into the PCB through the GND pins. If the device is used at high ambient temperatures, provide a thermal path from the GND pins to the PCB ground plane. The board layout in Figure 13 shows enlarged pads for Pin 8 (GND_1) and Pin 9 (GND_{ISO}). Large diameter vias should be implemented from the pad to the ground, and power planes should be used to reduce inductance. Multiple vias in the thermal pads can significantly reduce temperatures inside the chip. The dimensions of the expanded pads are at the discretion of the designer and depend on the available board space.

EMI CONSIDERATIONS

The dc-to-dc converter section of the ADuM5400 component must operate at a very high frequency to allow efficient power transfer through the small transformers. This creates high frequency currents that can propagate in circuit board ground and power planes, causing edge emissions and dipole radiation between the primary and secondary ground planes. Grounded enclosures are recommended for applications that use these devices. If grounded enclosures are not possible, follow good RF design practices in the layout of the PCB. See the AN-0971 Application Note for board layout recommendations.

PROPAGATION DELAY PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component (see Figure 14). The propagation delay to a logic low output may differ from the propagation delay to a logic high output.

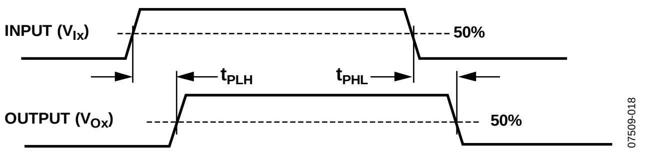


Figure 14. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM5400 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM540x components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than 1 µs, periodic sets of refresh pulses indicative of the correct input state are sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state by the watchdog timer circuit. This situation should occur in the ADuM5400 only during power-up and power-down operations.

The limitation on the ADuM5400 magnetic field immunity is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to falsely set or reset the decoder. The following analysis defines the conditions under which this can occur.

The 3.3 V operating condition of the ADuM5400 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude of >1.0 V. The decoder has a sensing threshold of about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt)\sum \pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
N is the number of turns in the receiving coil.
r_n is the radius of the nth turn in the receiving coil (cm).

Given the geometry of the receiving coil in the ADuM5400 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 15.

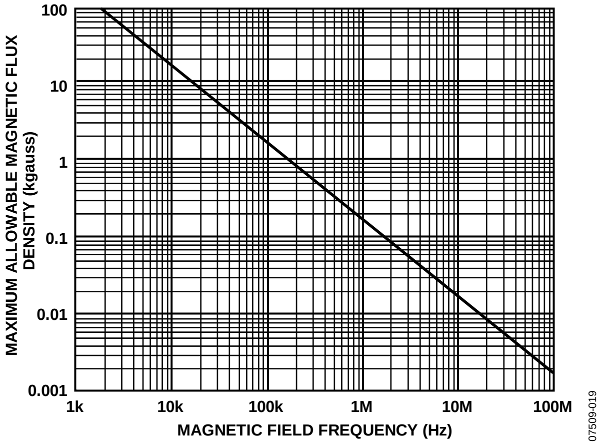


Figure 15. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (and is of the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V, which is still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM5400 transformers. Figure 16 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 16, the ADuM5400 is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For example, at a magnetic field frequency of 1 MHz, a 0.5 kA current placed 5 mm away from the ADuM5400 is required to affect the operation of the component.

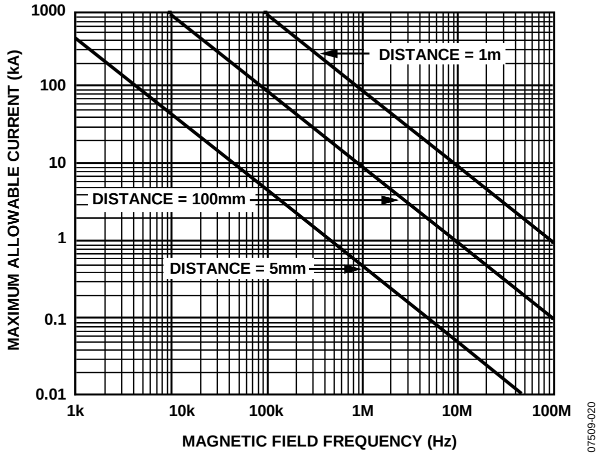


Figure 16. Maximum Allowable Current for Various Current-to-ADuM5400 Spacings

Note that in the presence of strong magnetic fields and high frequencies, any loops formed by PCB traces may induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Exercise care in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The V_{DD1} power supply input provides power to the *i*Coupler data channels, as well as to the power converter. For this reason, the quiescent currents drawn by the data converter and the primary and secondary I/O channels cannot be determined separately. All of these quiescent power demands have been combined into the $I_{DD1(Q)}$ current, as shown in Figure 17. The total I_{DD1} supply current is equal to the sum of the quiescent operating current; the dynamic current due to high data rate, and any external I_{ISO} load.

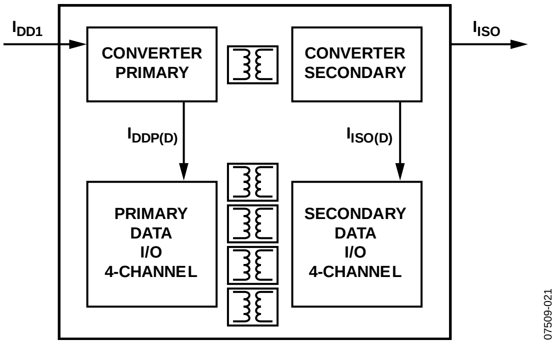


Figure 17. Power Consumption Within the ADuM5400

Dynamic I/O current is consumed only when operating a channel at speeds higher than the refresh rate of f_r. The dynamic current of each channel is determined by its data rate. Figure 12 shows the current for a channel in the forward direction, meaning that the input is on the V_{DD1} side of the part.

The following relationship allows the total I_{DD1} current to be calculated:

$$I_{DD1} = (I_{ISO} \times V_{ISO})/(E \times V_{DD1}) + \Sigma\, I_{CHn};\ n = 1 \text{ to } 4 \qquad (1)$$

where:
I_{DD1} is the total supply input current.
I_{CHn} is the current drawn by a single channel determined from Figure 12.
I_{ISO} is the current drawn by the secondary side external load.
E is the power supply efficiency at 100 mA load from Figure 4 at the V_{ISO} and V_{DD1} condition of interest.

The maximum external load can be calculated by subtracting the dynamic output load from the maximum allowable load.

$$I_{ISO(LOAD)} = I_{ISO(MAX)} - \Sigma\, I_{ISO(D)n};\ n = 1 \text{ to } 4 \qquad (2)$$

where:
$I_{ISO(LOAD)}$ is the current available to supply an external secondary side load.
$I_{ISO(MAX)}$ is the maximum external secondary side load current available at V_{ISO}.
$I_{ISO(D)n}$ is the dynamic load current drawn from V_{ISO} by an output channel, as shown in Figure 11.

The preceding analysis assumes a 15 pF capacitive load on each data output. If the capacitive load is larger than 15 pF, the additional current must be included in the analysis of I_{DD1} and $I_{ISO(LOAD)}$.

POWER CONSIDERATIONS

The ADuM5400 power input, the data input channels on the primary side, and the data output channels on the secondary side are all protected from premature operation by UVLO circuitry. Below the minimum operating voltage, the power converter holds its oscillator inactive, and all input channel drivers and refresh circuits are idle. Outputs are held in a low state to prevent transmission of undefined states during power-up and power-down operations.

During application of power to V_{DD1}, the primary side circuitry is held idle until the UVLO preset voltage is reached.

The primary side input channels sample the input and send a pulse to the inactive secondary output. As the secondary side converter begins to accept power from the primary, the V_{ISO} voltage starts to rise. When the secondary side UVLO is reached, the secondary side outputs are initialized to their default low state until data, either from a logic transition or a dc refresh cycle, is received from the corresponding primary side input. It can take up to 1 µs after the secondary side is initialized for the state of the output to correlate to the primary side input.

The dc-to-dc converter section goes through its own power-up sequence. When UVLO is reached, the primary side oscillator also begins to operate, transferring power to the secondary power circuits. The secondary V_{ISO} voltage is below its UVLO limit at this point; the regulation control signal from the secondary is not being generated. The primary side power oscillator is allowed to free run in this circumstance, supplying the maximum amount of power to the secondary, until the secondary voltage rises to its regulation setpoint. This creates a large inrush current transient at V_{DD1}. When the regulation point is reached, the regulation control circuit produces the regulation control signal that modulates the oscillator on the primary side. The V_{DD1} current is reduced and is then proportional to the load current. The inrush current is less than the short-circuit current shown in Figure 7. The duration of the inrush depends on the V_{ISO} load conditions and the current available at the V_{DD1} pin.

Because the rate of charge of the secondary side is dependent on load conditions, the input voltage, and the output voltage level selected, ensure that the design allows the converter to stabilize before valid data is required.

When power is removed from V_{DD1}, the primary side converter and coupler shut down when the UVLO level is reached. The secondary side stops receiving power and starts to discharge. The outputs on the secondary side hold the last state that they received from the primary until one of these events occurs:

- The UVLO level is reached and the outputs are placed in their high impedance state.
- The outputs detect a lack of activity from the inputs and the outputs transition to their default low state until the secondary power reaches UVLO and the outputs transition to their high impedance state.

THERMAL ANALYSIS

The ADuM5400 consists of four internal die attached to a split lead frame with two die attach paddles. For the purposes of thermal analysis, the die are treated as a thermal unit, with the highest junction temperature reflected in the θ_{JA} from Table 5. The value of θ_{JA} is based on measurements taken with the part mounted on a JEDEC standard 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM5400 operates at full load up to 85°C and at derated load up to 105°C.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends on the characteristics of the voltage waveform applied across the insulation. Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM5400.

Accelerated life testing is performed using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined, allowing calculation of the time to failure at the working voltage of interest. Table 11 summarizes the peak voltages for 50 years of service life in several operating conditions. In many cases, the working voltage approved by agency testing is higher than the 50-year service life voltage. Operation at working voltages higher than the service life voltage listed can lead to premature insulation failure.

The insulation lifetime of the ADuM5400 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates, depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 18, Figure 19, and Figure 20 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. A 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 11 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases.

Any cross-insulation voltage waveform that does not conform to Figure 19 or Figure 20 should be treated as a bipolar ac waveform, and its peak voltage limited to the 50-year lifetime voltage value listed in Table 11.

The voltage presented in Figure 20 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

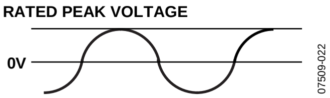


Figure 18. Bipolar AC Waveform

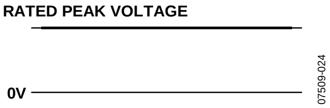


Figure 19. DC Waveform

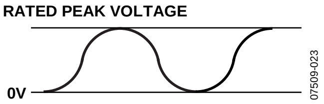
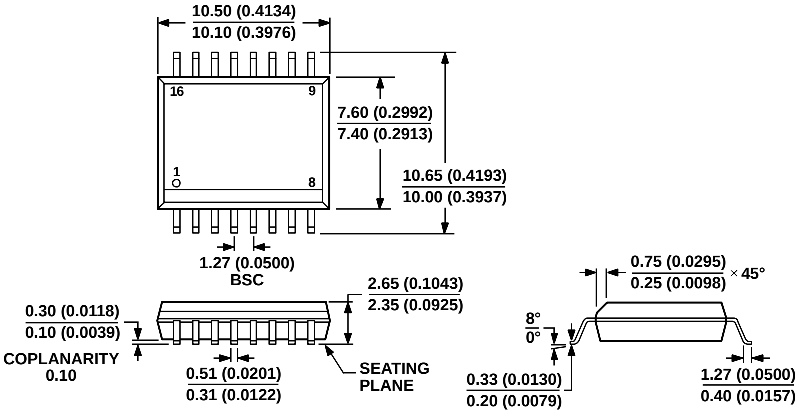


Figure 20. Unipolar AC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 21. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{ISO} Side	Maximum Data Rate (Mbps)	Maximum Propagation Delay, 5 V (ns)	Maximum Pulse Width Distortion (ns)	Temperature Range	Package Description	Package Option
ADuM5400ARWZ	4	0	1	100	40	−40°C to +105°C	16-Lead SOIC_W	RW-16
ADuM5400CRWZ	4	0	25	60	6	−40°C to +105°C	16-Lead SOIC_W	RW-16

[1] Z = RoHS Compliant Part.
[2] Tape and reel are available. The addition of an RL suffix designates a 13” (1,000 units) tape and reel option.