THE DATASHEET OF

ADUM3221WBRZ-RL7

Isolated, 4 A Dual-Channel Gate Driver

Data Sheet

ADuM3220/ADuM3221

FEATURES

- **4 A peak output current**
- **Precise timing characteristics**
  - **60 ns maximum isolator and driver propagation delay**
  - **5 ns maximum channel-to-channel matching**
- **High junction temperature operation: 125°C**
- **3.3 V to 5 V input logic**
- **4.5 V to 18 V output drive**
- **UVLO at 2.5 V V_{DD1}**
  - **ADuM3220A/ADuM3221A UVLO at 4.1 V V_{DD2}**
  - **ADuM3220B/ADuM3221B UVLO at 7.0 V V_{DD2}**
- **Thermal shutdown protection at >150°C**
- **Output shoot-through logic protection on the ADuM3220**
- **Default low output**
- **High frequency operation: dc to 1 MHz**
- **CMOS input logic levels**
- **High common-mode transient immunity: >25 kV/μs**
- **Enhanced system-level ESD performance per IEC 61000-4-x**
- **Safety and regulatory approvals**
  - **UL recognition**
    - **2500 V rms for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice #5A**
  - **VDE certificate of conformity**
    - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
    - **V_{IORM} = 560 V peak**
- **Small footprint and low profile**
  - **Narrow body, RoHS-compliant, 8-lead SOIC**
  - **5 mm × 6 mm × 1.6 mm**
- **Qualified for automotive applications**

APPLICATIONS

- **Isolated synchronous dc-to-dc converters**
- **MOSFET/IGBT gate drivers**

GENERAL DESCRIPTION

The ADuM3220/ADuM3221[1] are isolated, 4 A dual-channel gate drivers based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed CMOS and monolithic transformer technology, these isolation components provide outstanding performance characteristics superior to the alternatives, such as the combination of pulse transformers and gate drivers.

The ADuM3220/ADuM3221 provide digital isolation in two independent isolation channels. They have a maximum propagation delay of 60 ns and 5 ns channel-to-channel matching. In comparison to gate drivers that employ high voltage level translation method-ologies, the ADuM3220/ADuM3221 offer the benefit of true, galvanic isolation between the input and each output, enabling voltage translation across the isolation barrier. The ADuM3220 has shoot-through protection logic, which prevents both outputs from being on at the same time, whereas the ADuM3221 allows both outputs to be on at the same time. Both parts offer a default output low characteristic as required for gate drive applications.

The ADuM3220/ADuM3221 operate with an input supply voltage ranging from 3.0 V to 5.5 V, providing compatibility with lower voltage systems. The outputs of the ADuM3220A/ADuM3221A can be operated at supply voltages from 4.5 V to 18 V. The outputs of the ADuM3220B/ADuM3221B can be operated at supply voltages from 7.6 V to 18 V.

The junction temperature of the ADuM3220/ADuM3221 is specified from −40°C to +125°C.

FUNCTIONAL BLOCK DIAGRAMS

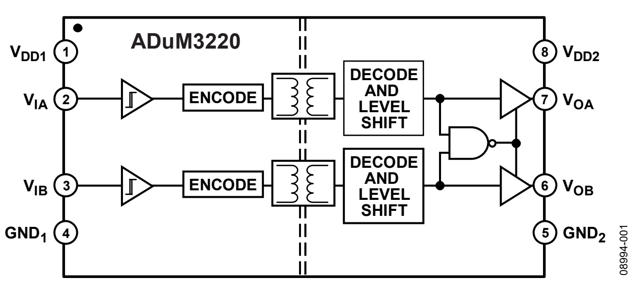

Figure 1.

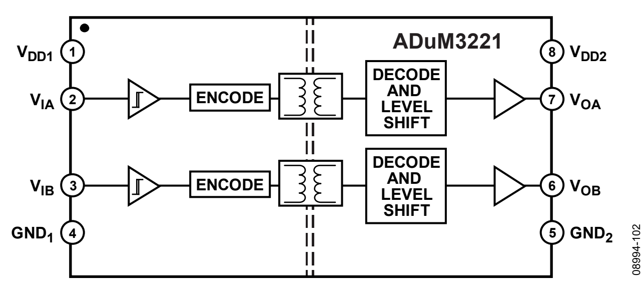

Figure 2.

[1] Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,239.

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4/2010—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

All voltages are relative to their respective ground. 4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 18 V, unless stated otherwise. All minimum/maximum specifications apply over T_J = −40°C to +125°C. All typical specifications are at T_J = 25°C, V_{DD1} = 5 V, V_{DD2} = 10 V. Switching specifications are tested with CMOS signal levels.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current, Two Channels, Quiescent	$I_{DDI(Q)}$		1.2	1.5	mA	
Output Supply Current, Two Channels, Quiescent	$I_{DDO(Q)}$		4.7	10	mA	
Total Supply Current, Two Channels[1]						
DC to 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.4	1.7	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2(Q)}$		11	17	mA	DC to 1 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	0.7 × V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DD2} − 0.1	V_{DD2}		V	I_{Ox} = −20 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	I_{Ox} = +20 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout, V_{DD2} Supply						
ADuM3220A/ADuM3221A						
Positive-Going Threshold	V_{DD2UV+}		4.1	4.4	V	
Negative-Going Threshold	V_{DD2UV-}	3.2	3.7		V	
Hysteresis	V_{DD2UVH}		0.4		V	
ADuM3220B/ADuM3221B						
Positive-Going Threshold	V_{DD2UV+}		7.0	7.5	V	
Negative-Going Threshold	V_{DD2UV-}	6.0	6.5		V	
Hysteresis	V_{DD2UVH}		0.5		V	
Output Short-Circuit Pulsed Current[2]	$I_{OA(SC)}$, $I_{OB(SC)}$	2.0	4.0		A	V_{DD2} = 10 V
Output Pulsed Source Resistance	R_{OA}, R_{OB}	0.3	1.3	3.0	Ω	V_{DD2} = 10 V
Output Pulsed Sink Resistance	R_{OA}, R_{OB}	0.3	0.9	3.0	Ω	V_{DD2} = 10 V
SWITCHING SPECIFICATIONS						
Pulse Width[3]	PW	50			ns	C_L = 2 nF, V_{DD2} = 10 V
Data Rate[4]				1	MHz	C_L = 2 nF, V_{DD2} = 10 V
Propagation Delay[5]	t_{DLH}, t_{DHL}	35	45	60	ns	C_L = 2 nF, V_{DD2} = 10 V; see Figure 20
	t_{DLH}, t_{DHL}	36	50	68	ns	C_L = 2 nF, V_{DD2} = 4.5 V; see Figure 20
Propagation Delay Skew[6]	t_{PSK}			12	ns	C_L = 2 nF, V_{DD2} = 10 V; see Figure 20
Channel-to-Channel Matching[7]	t_{PSKCD}		1	5	ns	C_L = 2 nF, V_{DD2} = 10 V; see Figure 20
	t_{PSKCD}		1	7	ns	C_L = 2 nF, V_{DD2} = 4.5 V; see Figure 20
Output Rise/Fall Time (10% to 90%)	t_R/t_F	14	20	25	ns	C_L = 2 nF, V_{DD2} = 10 V; see Figure 20
	t_R/t_F	14	22	28	ns	C_L = 2 nF, V_{DD2} = 4.5 V; see Figure 20
Dynamic Input Supply Current per Channel	$I_{DDI(D)}$		0.05		mA/Mbps	V_{DD2} = 10 V
Dynamic Output Supply Current per Channel	$I_{DDO(D)}$		1.5		mA/Mbps	V_{DD2} = 10 V
Refresh Rate	f_r		1.2		Mbps	

[1] The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 9 and Figure 10 for total V_{DD1} and V_{DD2} supply currents as a function of frequency.
[2] Short-circuit duration less than 1 µs. Average power must conform to the limit shown in the Absolute Maximum Ratings section.
[3] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.
[4] The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.
[5] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% threshold of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal. See Figure 20 for waveforms of propagation delay parameters.
[6] t_{PSK} is the magnitude of the worst-case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 20 for waveforms of propagation delay parameters.
[7] Channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All voltages are relative to their respective ground. 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 18 V, unless stated otherwise. All minimum/maximum specifications apply over T_J = −40°C to +125°C. All typical specifications are at T_J = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 10 V. Switching specifications are tested with CMOS signal levels.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Supply Current, Two Channels, Quiescent	$I_{DDI(Q)}$		0.7	1.0	mA	
Output Supply Current, Two Channels, Quiescent	$I_{DDO(Q)}$		4.7	10	mA	
Total Supply Current, Two Channels[1]						
DC to 1 MHz						
V_{DD1} Supply Current	$I_{DD1(Q)}$		0.8	1.0	mA	DC to 1 MHz logic signal frequency
V_{DD2} Supply Current	$I_{DD2(Q)}$		11	17	mA	DC to 1 MHz logic signal frequency
Input Currents	I_{IA}, I_{IB}	−10	+0.01	+10	µA	0 V ≤ V_{IA}, V_{IB} ≤ V_{DD1}
Logic High Input Threshold	V_{IH}	0.7 × V_{DD1}			V	
Logic Low Input Threshold	V_{IL}			0.3 × V_{DD1}	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}	V_{DD2} − 0.1	V_{DD2}		V	I_{Ox} = −20 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}		0.0	0.15	V	I_{Ox} = +20 mA, V_{Ix} = V_{IxL}
Undervoltage Lockout, V_{DD2} Supply						
ADuM3220A/ADuM3221A						
Positive-Going Threshold	V_{DD2UV+}		4.1	4.4	V	
Negative-Going Threshold	V_{DD2UV-}	3.2	3.7		V	
Hysteresis	V_{DD2UVH}		0.4		V	
ADuM3220B/ADuM3221B						
Positive-Going Threshold	V_{DD2UV+}		7.0	7.5	V	
Negative-Going Threshold	V_{DD2UV-}	6.0	6.5		V	
Hysteresis	V_{DD2UVH}		0.5		V	
Output Short-Circuit Pulsed Current[2]	$I_{OA(SC)}$, $I_{OB(SC)}$	2.0	4.0		A	V_{DD2} = 10 V
Output Pulsed Source Resistance	R_{OA}, R_{OB}	0.3	1.3	3.0	Ω	V_{DD2} = 10 V
Output Pulsed Sink Resistance	R_{OA}, R_{OB}	0.3	0.9	3.0	Ω	V_{DD2} = 10 V
SWITCHING SPECIFICATIONS						
Pulse Width[3]	PW	50			ns	C_L = 2 nF, V_{DD2} = 10 V
Data Rate[4]				1	MHz	C_L = 2 nF, V_{DD2} = 10 V
Propagation Delay[5]	t_{DLH}, t_{DHL}	36	48	62	ns	C_L = 2 nF, V_{DD2} = 10 V; see Figure 20
	t_{DLH}, t_{DHL}	37	53	72	ns	C_L = 2 nF, V_{DD2} = 4.5 V; see Figure 20
Propagation Delay Skew[6]	t_{PSK}			12	ns	C_L = 2 nF, V_{DD2} = 10 V; see Figure 20
Channel-to-Channel Matching[7]	t_{PSKCD}		1	5	ns	C_L = 2 nF, V_{DD2} = 10 V; see Figure 20
	t_{PSKCD}		1	7	ns	C_L = 2 nF, V_{DD2} = 4.5 V; see Figure 20
Output Rise/Fall Time (10% to 90%)	t_R/t_F	14	20	25	ns	C_L = 2 nF, V_{DD2} = 10 V; see Figure 20
	t_R/t_F	14	22	28	ns	C_L = 2 nF, V_{DD2} = 4.5 V; see Figure 20
Dynamic Input Supply Current per Channel	$I_{DDI(D)}$		0.025		mA/Mbps	V_{DD2} = 10 V
Dynamic Output Supply Current per Channel	$I_{DDO(D)}$		1.5		mA/Mbps	V_{DD2} = 10 V
Refresh Rate	f_r		1.1		Mbps	

[1] The supply current values for both channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 9 and Figure 10 for total V_{DD1} and V_{DD2} supply currents as a function of frequency.
[2] Short-circuit duration less than 1 µs. Average power must conform to the limit shown in the Absolute Maximum Ratings section.
[3] The minimum pulse width is the shortest pulse width at which the specified timing parameter is guaranteed.
[4] The maximum data rate is the fastest data rate at which the specified timing parameter is guaranteed.
[5] t_{DLH} propagation delay is measured from the time of the input rising logic high threshold, V_{IH}, to the output rising 10% threshold of the V_{Ox} signal. t_{DHL} propagation delay is measured from the input falling logic low threshold, V_{IL}, to the output falling 90% threshold of the V_{Ox} signal. See Figure 20 for waveforms of propagation delay parameters.
[6] t_{PSK} is the magnitude of the worst-case difference in t_{DLH} and/or t_{DHL} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions. See Figure 20 for waveforms of propagation delay parameters.
[7] Channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

PACKAGE CHARACTERISTICS

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		1.0		pF	f = 1 MHz
Input Capacitance	C_I		4.0		pF	
IC Junction-to-Case Thermal Resistance, Side 1	$θ_{JCI}$		46		°C/W	Thermocouple located at center of package underside
IC Junction-to-Case Thermal Resistance, Side 2	$θ_{JCO}$		41		°C/W	Thermocouple located at center of package underside
IC Junction-to-Ambient Thermal Resistance	$θ_{JA}$		85		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device; Pin 1 through Pin 4 are shorted together, and Pin 5 through Pin 8 are shorted together.

REGULATORY INFORMATION

The ADuM3220/ADuM3221 are approved by the organizations listed in Table 4.

Table 4.

UL	CSA	VDE
Recognized Under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single/Basic 2500 V rms Isolation Voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage Functional insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage	Reinforced insulation, 560 V peak
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM3220/ADuM3221 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (current leakage detection limit = 5 µA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM3220/ADuM3221 is proof tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). An asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 5.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1 minute duration
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

These isolators are suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval for a 560 V peak working voltage.

Table 6.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V peak
Input-to-Output Test Voltage, Method B1	V_{IORM} × 1.875 = V_{PR}, 100% production test, t_m = 1 sec, partial discharge < 5 pC	V_{PR}	1050	V peak
Input-to-Output Test Voltage, Method A	V_{IORM} × 1.6 = V_{PR}, t_m = 60 sec, partial discharge < 5 pC	V_{PR}		
After Environmental Tests Subgroup 1			896	V peak
After Input and/or Safety Tests Subgroup 2 and Subgroup 3	V_{IORM} × 1.2 = V_{PR}, t_m = 60 sec, partial discharge < 5 pC	V_{PR}	672	V peak
Highest Allowable Overvoltage	Transient overvoltage, t_{TR} = 10 sec	V_{TR}	4000	V peak
Safety-Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Side 1 Current		I_{S1}	160	mA
Side 2 Current		I_{S2}	47	mA
Insulation Resistance at T_S	V_{IO} = 500 V	R_S	$>10^9$	Ω

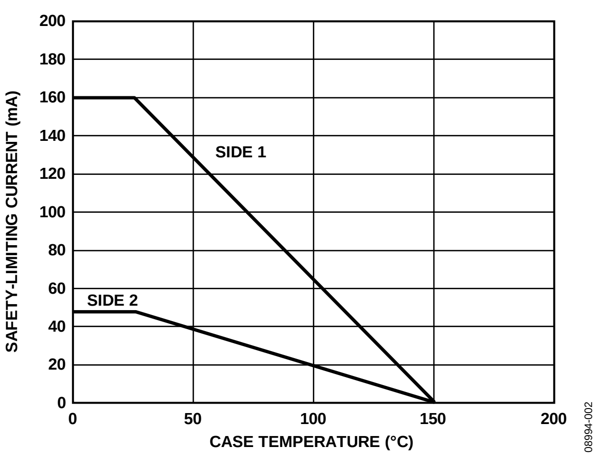


Figure 3. Thermal Derating Curve; Dependence of Safety-Limiting Values on Case Temperature, per DIN V VDE V 0884-10 (Safety-Limiting Current Is Defined as the Average Current at Maximum V_{DD})

RECOMMENDED OPERATING CONDITIONS

Table 7.

Parameter	Symbol	Min	Max	Unit
Operating Junction Temperature	T_J	−40	+125	°C
Supply Voltages[1]	V_{DD1}	3.0	5.5	V
	V_{DD2}	4.5	18	V
V_{DD1} Rise Time	t_{VDD1}		1	V/μs
Common-Mode Transient Immunity, Input to Output		−25	+25	kV/μs
Input Signal Rise and Fall Times			1	ms

[1] All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information about immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 8.

Parameter	Rating
Storage Temperature (T_{ST})	−55°C to +150°C
Operating Temperature (T_J)	−40°C to +150°C
Supply Voltage Ranges[1]	
V_{DD1}	−0.5 V to +7.0 V
V_{DD2}	−0.5 V to +20 V
Input Voltage Range (V_{IA}, V_{IB})[1, 2]	−0.5 V to V_{DDI} + 0.5 V
Output Voltage Range (V_{OA}, V_{OB})[1, 2]	−0.5 V to V_{DDO} + 0.5 V
Average Output Current per Pin (I_O)[3]	−23 mA to +23 mA
V_{OA} to GND_2 Negative Transient[4]	−2 V for 200 ns
V_{OB} to GND_2 Negative Transient[4]	−2 V for 200 ns
Common-Mode Transients, (CM_H, CM_L)[5]	−100 kV/µs to +100 kV/µs

[1] All voltages are relative to their respective ground.
[2] V_{DDI} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively.
[3] See Figure 3 for information about maximum allowable current for various temperatures.
[4] Applies to nonautomotive grade devices only.
[5] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum rating can cause latch-up or permanent damage.

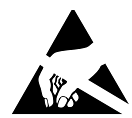
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 9. Maximum Continuous Working Voltage[1]

Parameter	Max	Unit	Constraint
AC Bipolar Voltage[2]	565	V peak	50-year minimum lifetime
AC Unipolar Voltage[3]	1131	V peak	50-year minimum lifetime
DC Voltage[4]	1131	V peak	50-year minimum lifetime

[1] Refers to the continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.
[2] See Figure 24.
[3] See Figure 25.
[4] See Figure 26.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

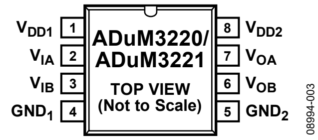


Figure 4. Pin Configuration

Table 10. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1, 3.0 V to 5.5 V.
2	V_{IA}	Logic Input A.
3	V_{IB}	Logic Input B.
4	GND_1	Ground 1. Ground reference for Isolator Side 1.
5	GND_2	Ground 2. Ground reference for Isolator Side 2.
6	V_{OB}	Logic Output B.
7	V_{OA}	Logic Output A.
8	V_{DD2}	Supply Voltage for Isolator Side 2, 4.5 V to 18 V.

Table 11. Truth Table, ADuM3220 (Positive Logic)[1]

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
L	L	Powered	Powered	L	L	
L	H	Powered	Powered	L	H	
H	L	Powered	Powered	H	L	
H	H	Powered	Powered	L	L	
X	X	Unpowered	Powered	L	L	Outputs return to the input state within 1 μs of V_{DD1} power restoration.
X	X	Powered	Unpowered	L	L	Outputs return to the input state within 1 μs of V_{DD2} power restoration.

[1] X = don't care, L = low, H = high.

Table 12. Truth Table, ADuM3221 (Positive Logic)[1]

V_{IA} Input	V_{IB} Input	V_{DD1} State	V_{DD2} State	V_{OA} Output	V_{OB} Output	Notes
L	L	Powered	Powered	L	L	
L	H	Powered	Powered	L	H	
H	L	Powered	Powered	H	L	
H	H	Powered	Powered	H	H	
X	X	Unpowered	Powered	L	L	Outputs return to the input state within 1 μs of V_{DD1} power restoration.
X	X	Powered	Unpowered	L	L	Outputs return to the input state within 1 μs of V_{DD2} power restoration.

[1] X = don't care, L = low, H = high.

TYPICAL PERFORMANCE CHARACTERISTICS

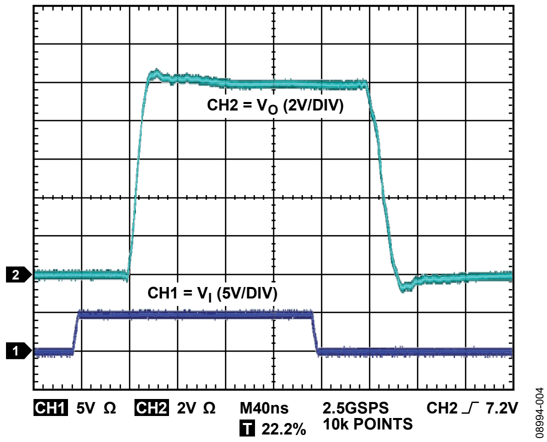


Figure 5. Output Waveform for 2 nF Load with 10 V Output Supply

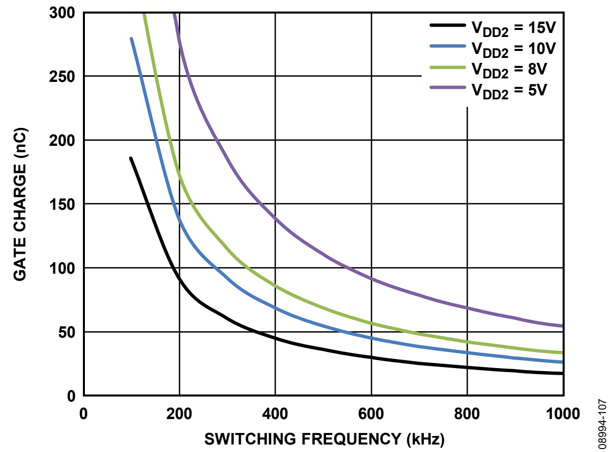


Figure 8. Typical Maximum Load vs. Switching Frequency (R_{GATE} = 1 Ω)

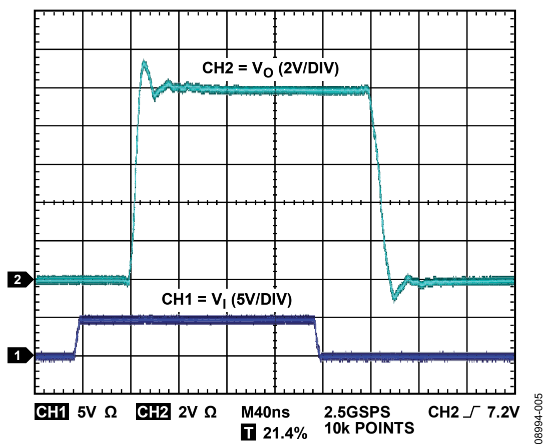


Figure 6. Output Waveform for 1 nF Load with 10 V Output Supply

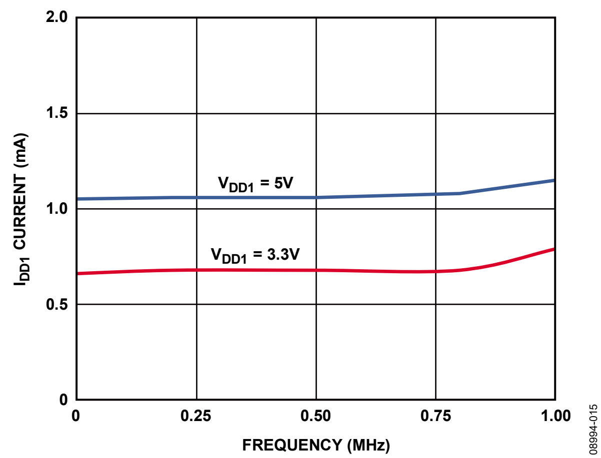


Figure 9. Typical I_{DD1} Supply Current vs. Frequency

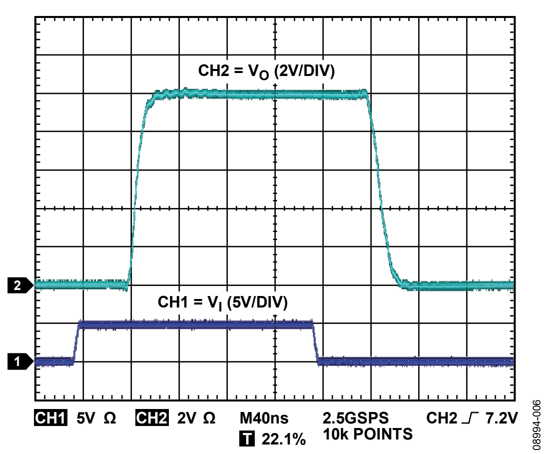


Figure 7. Output Waveform for 1 nF Load with 5 Ω Series Resistance and 10 V Output Supply

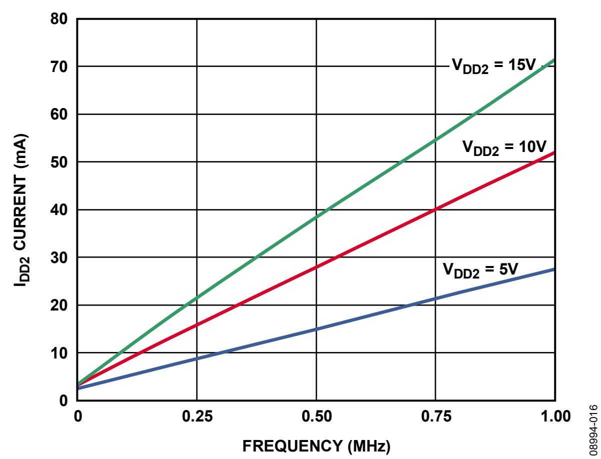


Figure 10. Typical I_{DD2} Supply Current vs. Frequency with 2 nF Load

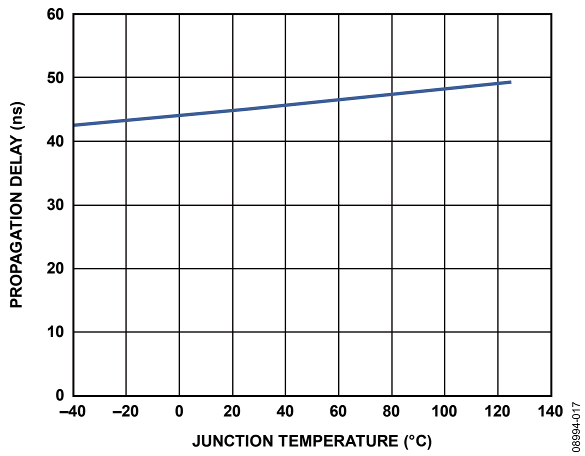


Figure 11. Typical Propagation Delay vs. Temperature

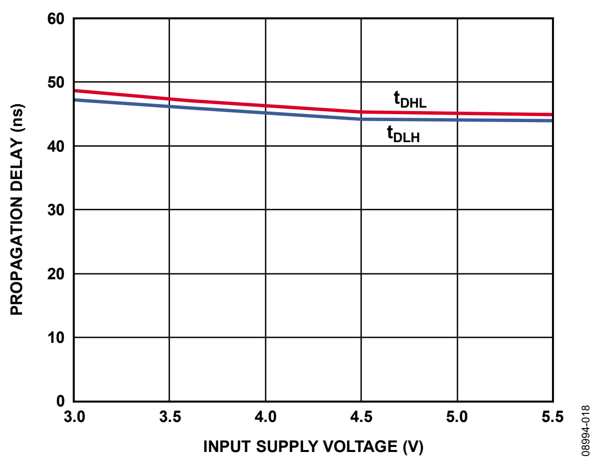


Figure 12. Typical Propagation Delay vs. Input Supply Voltage, V_{DD2} = 10 V

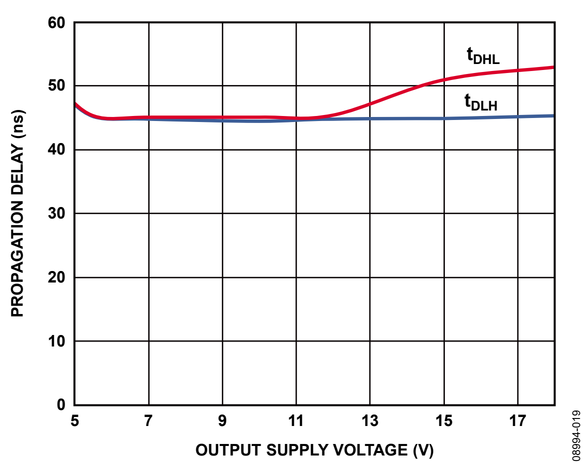


Figure 13. Typical Propagation Delay vs. Output Supply Voltage, V_{DD1} = 5 V

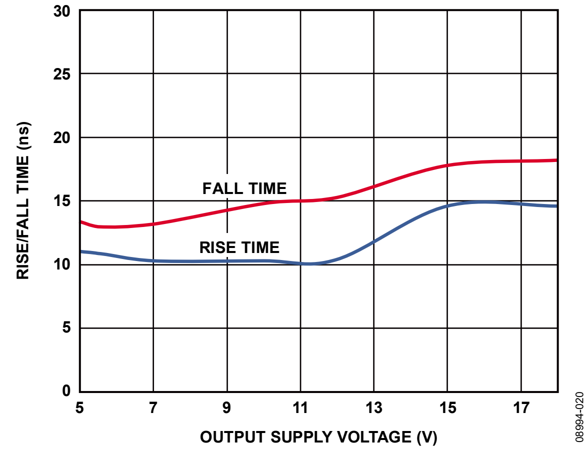


Figure 14. Typical Rise/Fall Time Variation vs. Output Supply Voltage

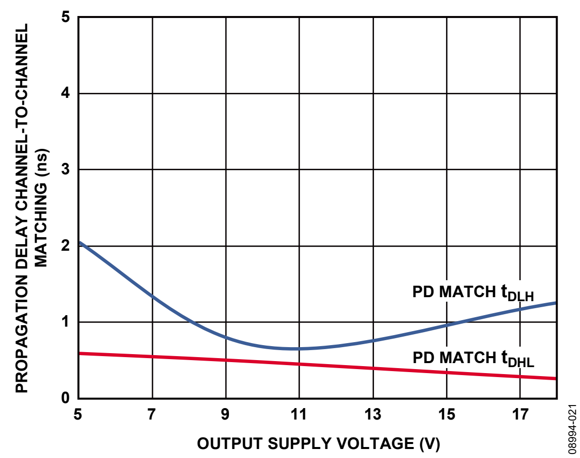


Figure 15. Typical Propagation Delay Channel-to-Channel Matching vs. Output Supply Voltage

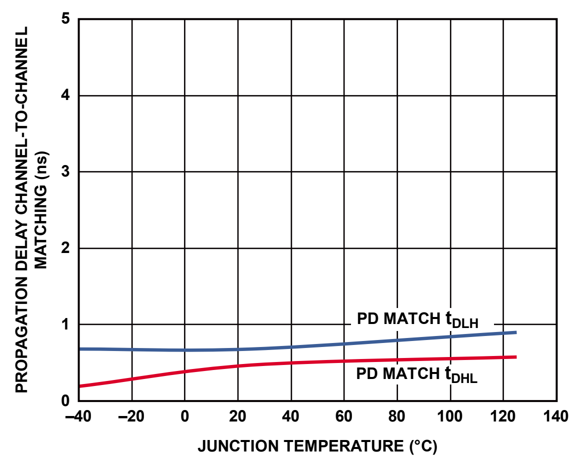


Figure 16. Typical Propagation Delay Channel-to-Channel Matching vs. Temperature, V_{DD2} = 10 V

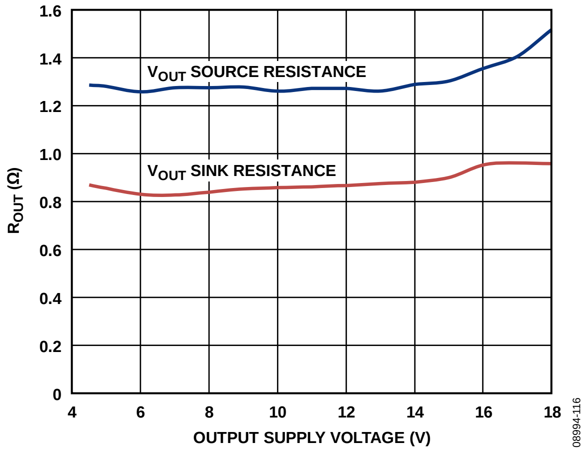


Figure 17. Typical Output Source Resistance vs. Output Supply Voltage

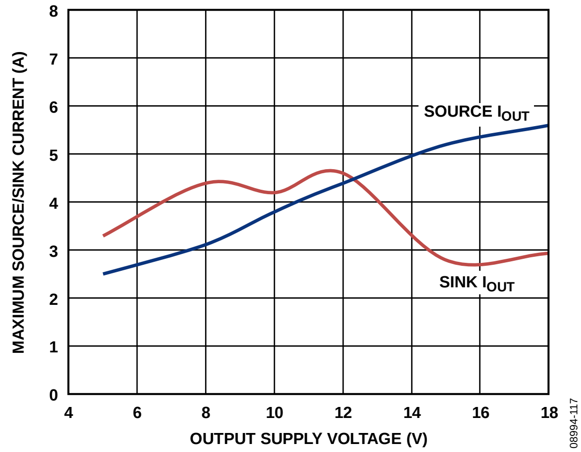


Figure 18. Typical Maximum Source/Sink Current vs. Output Supply Voltage

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM3220/ADuM3221 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins, as shown in Figure 19. Use a small ceramic capacitor with a value from 0.01 µF to 0.1 µF to provide a good high frequency bypass. On the output power supply pin, V_{DD2}, it is recommended that a 10 µF capacitor also be added to provide the charge required to drive the gate capacitance at the ADuM3220/ADuM3221 outputs. On the output supply pin, the use of vias with the bypass capacitor should be avoided, or multiple vias should be used to reduce the inductance in the bypassing. The total lead length between both ends of the smaller capacitor and the input or output power supply pin should not exceed 20 mm.

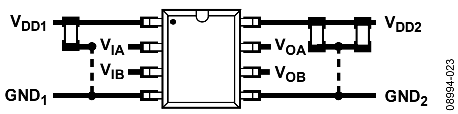


Figure 19. Recommended PCB Layout

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output can differ from the propagation delay to a logic high output. The ADuM3220/ADuM3221 specify t_{DLH} as the time between the input rising high logic threshold, V_{IH}, and the output rising 10% threshold (see Figure 20). Likewise, the falling propagation delay, t_{DHL}, is defined as the time between the input falling logic low threshold, V_{IL}, and the output falling 90% threshold. The rise and fall times are dependent on the loading conditions and are not included in the propagation delay, as is the industry standard for gate drivers.

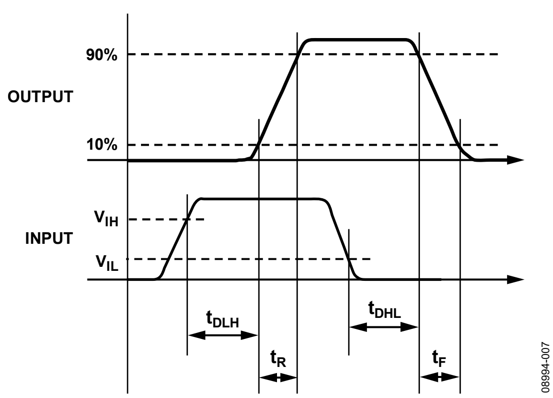


Figure 20. Propagation Delay Parameters

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM3220/ADuM3221 component.

Propagation delay skew refers to the maximum amount that the propagation delay differs between multiple ADuM3220/ADuM3221 components operating under the same conditions.

THERMAL LIMITATIONS AND SWITCH LOAD CHARACTERISTICS

For isolated gate drivers, the necessary separation between the input and output circuits prevents the use of a single thermal pad beneath the part; therefore, heat is dissipated mainly through the package pins.

Package thermal dissipation limits the performance of switching frequency vs. output load, as illustrated in Figure 8, which shows the maximum load capacitance that can be driven with a 1 Ω series gate resistor for different values of output voltage. For example, this curve shows that a typical ADuM3220/ADuM3221 can drive a large MOSFET with 120 nC gate charge at 8 V output (which is equivalent to a 15 nF load) up to a frequency of about 300 kHz.

OUTPUT LOAD CHARACTERISTICS

The ADuM3220/ADuM3221 output signals depend on the characteristics of the output load, which is typically an N-channel MOSFET. The driver output response to an N-channel MOSFET load can be modeled with a switch output resistance (R_{SW}), an inductance due to the printed circuit board trace (L_{TRACE}), a series gate resistor (R_{GATE}), and a gate-to-source capacitance (C_{GS}), as shown in Figure 21.

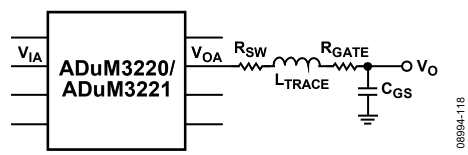


Figure 21. RLC Model of the Gate of an N-Channel MOSFET

R_{SW} is the switch resistance of the internal ADuM3220/ADuM3221 driver output, which is about 1.5 Ω. R_{GATE} is the intrinsic gate resistance of the MOSFET and any external series resistance. A MOSFET that requires a 4 A gate driver has a typical intrinsic gate resistance of about 1 Ω and a gate-to-source capacitance, C_{GS}, from 2 nF to 10 nF. L_{TRACE} is the inductance of the printed circuit board trace, typically a value of 5 nH or less for a well-designed layout with a very short and wide connection from the ADuM3220/ADuM3221 output to the gate of the MOSFET.

The following equation defines the Q factor of the RLC circuit, which indicates how the ADuM3220/ADuM3221 output responds to a step change. For a well-damped output, Q is less than 1. Adding a series gate resistor dampens the output response.

$$Q = \frac{1}{(R_{SW} + R_{GATE})} \times \sqrt{\frac{L_{TRACE}}{C_{GS}}}$$

In Figure 5 and Figure 6, the ADuM3220/ADuM3221 output waveforms for 10 V output are shown for a C_{GS} of 2 nF and 1 nF, respectively. Note the ringing of the output in Figure 6 with C_{GS} of 1 nF and a calculated Q factor of 1.5, where less than 1 is desired for good damping.

Output ringing can be reduced by adding a series gate resistor to dampen the response. For applications that use a load of 1 nF or less, it is recommended that a series gate resistor of about 5 Ω be added. As shown in Figure 7, R_{GATE} is 5 Ω, which yields a calculated Q factor of about 0.3. Figure 7 illustrates a damped response in comparison with Figure 6.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions of more than 1 µs at the input, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output.

If the decoder receives no internal pulses for more than about 3 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default low state by the watchdog timer circuit. In addition, the outputs are in a low default state while the power is rising before the UVLO threshold is crossed.

The ADuM3220/ADuM3221 are immune to external magnetic fields. The limitation on the ADuM3220/ADuM3221 magnetic field immunity is set by the condition in which induced voltage in the transformer receiving coil is sufficiently large to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM3220/ADuM3221 is examined because it represents the most susceptible mode of operation. The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; \; n = 1, 2, \ldots, N$$

where:
β is the magnetic flux density (gauss).
r_n is the radius of the nth turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM3220/ADuM3221 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 22.

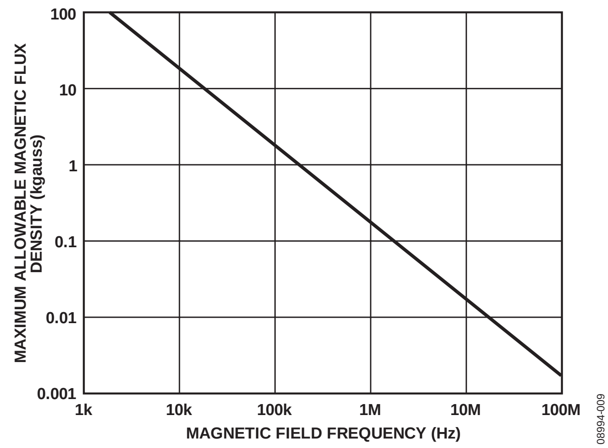


Figure 22. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and had the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM3220/ADuM3221 transformers. Figure 23 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM3220/ADuM3221 are immune and can be affected only by extremely large currents operated at a high frequency very close to the component. For the 1 MHz example, a 0.5 kA current must be placed 5 mm away from the ADuM3220/ADuM3221 to affect the operation of the component.

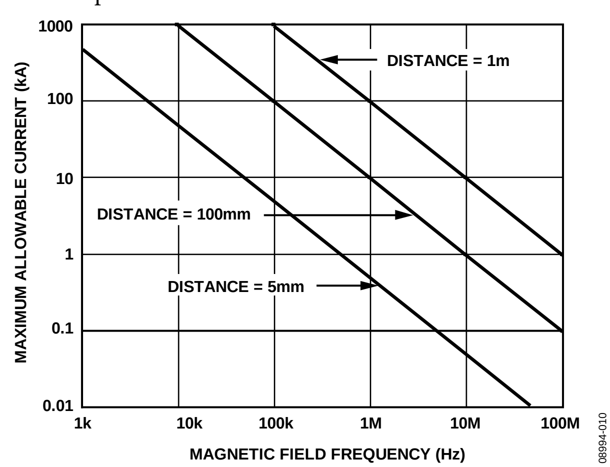


Figure 23. Maximum Allowable Current for Various Current-to-ADuM3220/ADuM3221 Spacings

POWER CONSUMPTION

The supply current at a given channel of the ADuM3220/ADuM3221 isolator is a function of the supply voltage, channel data rate, and channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \qquad f > 0.5f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \qquad f \leq 0.5f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \qquad f > 0.5f_r$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz, half of the input data rate, NRZ signaling).

f_r is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total I_{DD1} and I_{DD2} supply current, the supply currents for each input and output channel corresponding to I_{DD1} and I_{DD2} are calculated and totaled.

Figure 9 provides total input I_{DD1} supply current as a function of frequency for both input channels. Figure 10 provides total I_{DD2} supply current as a function of frequency for both outputs loaded with 2 nF capacitance.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM3220/ADuM3221.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage.

The values shown in Table 9 summarize the peak voltage for 50 years of service life. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM3220/ADuM3221 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 24, Figure 25, and Figure 26 illustrate these different isolation voltage waveforms.

A bipolar ac voltage environment is the worst case for the *i*Coupler products and is the 50-year operating lifetime that Analog Devices recommends for maximum working voltage. In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. Any cross-insulation voltage waveform that does not conform to Figure 25 or Figure 26 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 9.

Note that the voltage presented in Figure 25 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

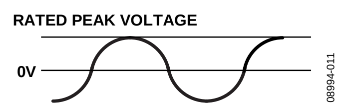


Figure 24. Bipolar AC Waveform

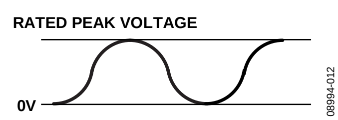


Figure 25. Unipolar AC Waveform

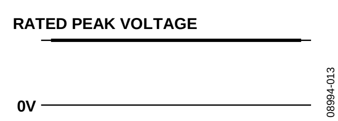


Figure 26. DC Waveform

OUTLINE DIMENSIONS

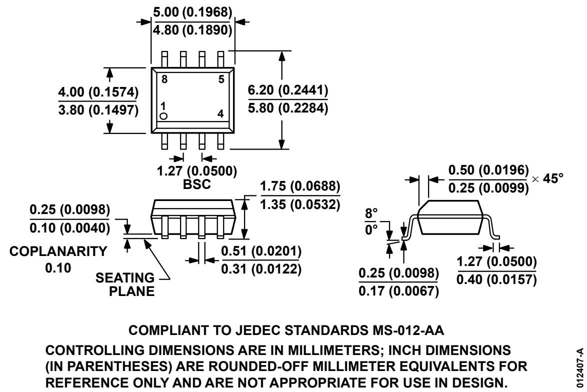


Figure 27. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model[1, 2]	No. of Inputs, V_{DD1} Side	Maximum Data Rate (MHz)	Maximum Propagation Delay, 5 V (ns)	Minimum V_{DD2} Operating Voltage (V)	Output Shoot-Through Protection (Yes/No)	Junction Temperature Range	Package Description	Package Option
ADuM3220ARZ	2	1	60	4.5	Yes	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3220ARZ-RL7	2	1	60	4.5	Yes	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3220BRZ	2	1	60	7.6	Yes	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3220BRZ-RL7	2	1	60	7.6	Yes	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3220WARZ	2	1	60	4.5	Yes	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3220WARZ-RL7	2	1	60	4.5	Yes	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3220WBRZ	2	1	60	7.6	Yes	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3220WBRZ-RL7	2	1	60	7.6	Yes	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3221ARZ	2	1	60	4.5	No	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3221ARZ-RL7	2	1	60	4.5	No	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3221BRZ	2	1	60	7.6	No	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3221BRZ-RL7	2	1	60	7.6	No	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3221WARZ	2	1	60	4.5	No	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3221WARZ-RL7	2	1	60	4.5	No	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3221WBRZ	2	1	60	7.6	No	−40°C to +125°C	8-Lead SOIC_N	R-8
ADuM3221WBRZ-RL7	2	1	60	7.6	No	−40°C to +125°C	8-Lead SOIC_N	R-8

[1] Z = RoHS Compliant Part.
[2] W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADuM3220W and ADuM3221W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES