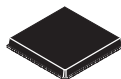




**THE DATASHEET OF  
ADS8410IRGZR**





# 16-BIT, 2-MSPS, LVDS SERIAL INTERFACE, SAR ANALOG-TO-DIGITAL CONVERTER

Check for Samples: [ADS8410](#)

## FEATURES

- 2-MHz Sample Rate
- 16-Bit Resolution
- SNR 87.5 dB at 10 kHz I/P
- THD –98 dB at 10 kHz I/P
- $\pm 1$  LSB Typ,  $\pm 2.5$  LSB INL Max
- $+0.8/-0.5$  LSB Typ,  $+1.5/-1$  LSB DNL Max
- Unipolar Differential Input Range: 0 V to 4 V
- Internal Reference
- Internal Reference Buffer
- 200-Mbps LVDS Serial Interface
- Optional 200-MHz Internal Interface Clock
- 16-/8-Bit Data Frame
- Zero Latency at Full Speed
- Power Dissipation: 290 mW at 2 MSPS
- Nap Mode (125 mW Power Dissipation)
- Power Down (5  $\mu$ W)
- 48-Pin QFN Package

## APPLICATIONS

- Medical Instrumentation
- High-Speed Data Acquisition Systems
- High-Speed Close-Loop Systems
- Communication

## DESCRIPTION

The ADS8410 is a 16-bit, 2-MSPS, analog-to-digital (A/D) converter with 4-V internal reference. The device includes a capacitor based SAR A/D converter with inherent sample and hold.

The ADS8410 also includes a 200-Mbps, LVDS, serial interface. This interface is designed to support daisy chaining or cascading of multiple devices. A selectable 16-/8-bit data frame mode enables the use of a single shift register chip (SN65LVDS152) for converting the data to parallel format.

The ADS8410 unipolar single-ended input range supports a differential input swing of 0 V to  $+V_{ref}$ .

The nap feature provides substantial power saving when used at lower conversion rates.

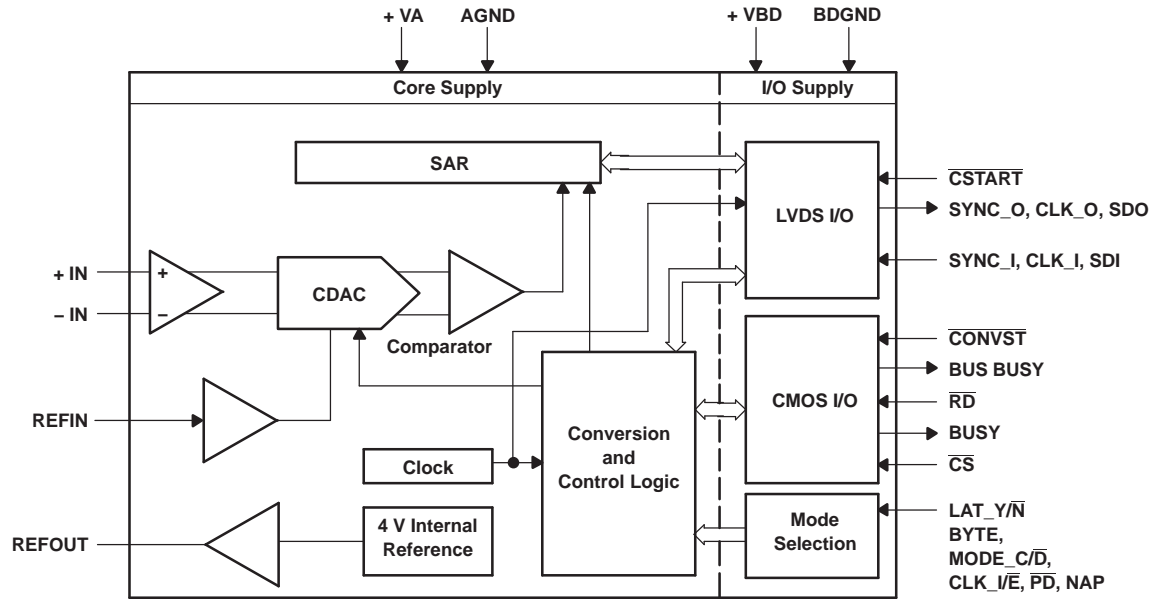
The ADS8410 is available in a 48-pin QFN package.

**Table 1. High-Speed SAR Converter Family**

Type/Speed	500 kHz	~ 600 kHz	750 kHz	1 MHz	1.25 MHz	2 MHz	3 MHz	4 MHz
18-Bit Pseudo-Diff	ADS8383	ADS8381						
		ADS8380 (S)						
18-Bit Pseudo-Bipolar, Fully Diff		ADS8382 (S)						
16-Bit Pseudo-Diff		ADS8370 (S)	ADS8371		ADS8401/05	ADS8411		
						ADS8410 (S-LVDS)		
16-Bit Pseudo-Bipolar, Fully Diff		ADS8372 (S)			ADS8402/06	ADS8412		
						ADS8413 (S-LVDS)		
14-Bit Pseudo-Diff					ADS7890 (S)		ADS7891	
12-Bit Pseudo-Diff								ADS7881



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



**ORDERING INFORMATION<sup>(1)</sup>**

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	NO MISSING CODES AT RESOLUTION (BIT)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA QUANTITY
ADS8410IB	±2.5	1.5/-1	16	48 pin QFN	RGZ	-40°C to 85°C	ADS8410IBRGZT	250
							ADS8410IBRGZR	2000
ADS8410I	±4	3/-1	16	48 pin QFN	RGZ	-40°C to 85°C	ADS8410IRGZT	250
							ADS8410IRGZR	2000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		UNIT
+IN to AGND		-0.3 V to +VA + 0.3 V
-IN to AGND		-0.3 V to +0.3 V
+VA to AGND		-0.3 to 7 V
+VBD to BDGND		-0.3 to 7 V
Digital input voltage to GND		-0.3 V to (+VBD + 0.3 V)
Digital output to GND		-0.3 V to (+VBD + 0.3 V)
Operating temperature range		-40°C to 85°C
Storage temperature range		-65°C to 150°C
Junction temperature (T <sub>J,max</sub> )		150°C
QFN package	Power dissipation	(T <sub>J Max</sub> - T <sub>A</sub> ) / θ <sub>JA</sub>
	θ <sub>JA</sub> Thermal impedance	86°C/W
Lead temperature, soldering	Vapor phase (60 sec)	215°C
	Infrared (15 sec)	220°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## SPECIFICATIONS

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $+V_A = 5\text{ V}$ ,  $+V_{BD} = 5\text{ V}$  or  $3.3\text{ V}$ ,  $V_{ref} = 4.096\text{ V}$ ,  $f_{sample} = 2\text{ MHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>ANALOG INPUT</b>						
Full-scale input voltage span <sup>(1)</sup>		+IN – (–IN)	0		$V_{ref}$	V
Absolute input voltage range		+IN	–0.2		$V_{ref} + 0.2$	V
		–IN	–0.2		+0.2	
$C_i$	Input capacitance			25		pF
	Input leakage current			500		pA
<b>SYSTEM PERFORMANCE</b>						
Resolution				16		Bits
No missing codes		ADS8410IB		16		Bits
		ADS8410I		16		
INL	Integral linearity <sup>(2)</sup>	ADS8410IB	–2.5	$\pm 1$	2.5	LSB <sup>(3)</sup>
		ADS8410I	–4.0	$\pm 2.5$	4.0	
DNL	Differential linearity	ADS8410IB	–1	0.8/–0.5	1.5	LSB <sup>(3)</sup>
		ADS8410I	–1.0	1.5/–0.8	3	
$E_O$	Offset error	ADS8410IB	–0.75	$\pm 0.1$	0.75	mV
		ADS8410I	–1.5	$\pm 0.75$	1.5	
$E_G$	Gain error <sup>(4)</sup>	ADS8410IB	–0.05	$\pm 0.01$	0.05	% of FS
		ADS8410I	–0.15	$\pm 0.05$	0.15	
CMMR	Common-mode rejection ratio	With common mode input signal = 200 mV <sub>p-p</sub> at 1 MHz		60		dB
PSRR	Power supply rejection ratio	At FFF0 <sub>H</sub> output code		80		dB
<b>SAMPLING DYNAMICS</b>						
Conversion time		+VBD = 5 V		360	391	ns
		+VBD = 3 V			391	
Acquisition time		+VBD = 5 V		100		ns
		+VBD = 3 V		100		
Maximum throughput rate with or without latency					2.0	MHz
Aperture delay				20		ns
Aperture jitter				10		psec
Step response				50		ns
Overvoltage recovery				50		ns
<b>DYNAMIC CHARACTERISTICS</b>						
THD	Total harmonic distortion <sup>(5)</sup>	$V_{IN}$ 0.5 dB below FS at 10 kHz		–98		dB
		$V_{IN}$ 0.5 dB below FS at 100 kHz		–92.5		
SNR	Signal-to-noise ratio	$V_{IN}$ 0.5 dB below FS at 10 kHz		87.5		dB
		$V_{IN}$ 0.5 dB below FS at 100 kHz		86		
SINAD	Signal-to-noise and distortion	$V_{IN}$ 0.5 dB below FS at 10 kHz		87		dB
		$V_{IN}$ 0.5 dB below FS at 100 kHz		85		
SFDR	Spurious free dynamic range	$V_{IN}$ 0.5 dB below FS at 10 kHz		–101		dB
		$V_{IN}$ 0.5 dB below FS at 100 kHz		–93		
	–3 dB Small signal bandwidth			37.5		MHz
<b>EXTERNAL REFERENCE INPUT</b>						
Input voltage range, $V_{REF}$			3.9	4.096	4.2	V
Resistance <sup>(6)</sup>		To internal reference voltage		500		k $\Omega$
<b>INTERNAL REFERENCE OUTPUT</b>						

- (1) Ideal input span; does not include gain or offset error.
- (2) This is endpoint INL, not best fit.
- (3) Least significant bit
- (4) Measured relative to actual measured reference.
- (5) Calculated on the first nine harmonics of the input frequency.
- (6) Can vary  $\pm 20\%$

**SPECIFICATIONS (continued)**

T<sub>A</sub> = -40°C to 85°C, +VA = 5 V, +VBD = 5 V or 3.3 V, V<sub>ref</sub> = 4.096 V, f<sub>sample</sub> = 2 MHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start-up time		From 95% (+VA), with 1-μF storage capacitor on REFOUT to AGND			25	ms
Reference voltage range, V <sub>ref</sub>		At room temperature	4.080	4.096	4.112	V
Source current		Static load			10	μA
Line regulation		+VA = 4.75 V to 5.25 V		0.6		mV
Drift		IOUT = 0 V		36		PPM/°C
<b>POWER SUPPLY REQUIREMENTS</b>						
Power supply voltage	+VBD		2.7	3.3	5.25	V
	+VA		4.75	5	5.25	
Supply current, 2-MHz sample rate	+VA			58	64	mA
Power dissipation, 2-MHz sample rate		+VA = 5 V		290	320	mW
<b>NAP MODE</b>						
Supply current	+VA			25		mA
<b>POWER DOWN</b>						
Supply current	+VA			1	2.5	μA
Powerdown time				10		μs
Powerup time		With 1-μF storage capacitor on REFOUT to AGND		25		ms
Invalid conversions after power up or reset				3		Numbers
<b>TEMPERATURE RANGE</b>						
Operating free air			-40		85	°C
<b>LOGIC FAMILY CMOS</b>						
V <sub>IH</sub>	High-level input voltage	I <sub>IH</sub> = 5 μA	+VBD -1		+VBD +0.3	V
V <sub>IL</sub>	Low-level input voltage	I <sub>IL</sub> = 5 μA	-0.3		0.8	V
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = 2 TTL loads	+VBD - 0.6		+VBD	V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 2 TTL loads	0		0.4	V
<b>LOGIC FAMILY LVDS<sup>(7)</sup></b>						
<b>DRIVER</b>						
V <sub>OD(SS)</sub>	Steady-state differential output voltage magnitude	R <sub>L</sub> = 100 Ω, See <a href="#">Figure 52</a> , <a href="#">Figure 53</a>	247	340	454	mV
Δ V <sub>OD(SS)</sub>	Change in steady-state differential output voltage magnitude between logic states		-50		50	
V <sub>OC(SS)</sub>	Steady-state common-mode output voltage	See <a href="#">Figure 54</a>	1.125	1.2	1.375	V
Δ V <sub>OC(SS)</sub>	Change in steady-state common-mode output voltage between logic states		-50		50	mV
V <sub>OC(pp)</sub>	Peak to peak change in common-mode output voltage			50	150	
I <sub>OS</sub>	Short circuit output current	V <sub>OY</sub> or V <sub>OZ</sub> = 0 V		3	10	mA
		V <sub>OD</sub> = 0 V		3	10	
I <sub>OZ</sub>	High impedance output current	V <sub>O</sub> = 0 V or +VBD	-5		5	μA

(7) All min max values ensured by design.

## SPECIFICATIONS (continued)

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $+V_A = 5\text{ V}$ ,  $+V_{BD} = 5\text{ V}$  or  $3.3\text{ V}$ ,  $V_{ref} = 4.096\text{ V}$ ,  $f_{sample} = 2\text{ MHz}$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>RECEIVER</b>						
$V_{ITH+}$	Positive going differential voltage threshold				50	mV
$V_{ITH-}$	Negative going differential voltage threshold			-50		
$V_{IC}$	Common mode input voltage		0.2	1.2	2.2	V
$C_I$	Input capacitance			5		pF

## TIMING REQUIREMENTS

 $T_A = -40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $+V_A = 5\text{ V}$ ,  $+V_{BD} = 5\text{ V}$  or  $3.3\text{ V}$  (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT	REF
<b>SAMPLING AND CONVERSION RELATED</b>						
$t_{acq}$	Acquisition time	100			ns	Figure 1, Figure 2
$t_{cnv}$	Conversion time			391	ns	Figure 1, Figure 2
$t_{w1}$	Pulse duration, $\overline{\text{CONVST}}$ high	100			ns	Figure 1
$t_{w2}$	Pulse duration, $\overline{\text{CONVST}}$ low	40			ns	Figure 1, Figure 2
$t_{d1}$	Delay time, $\overline{\text{CONVST}}$ rising edge to sample start			5	ns	Figure 1
$t_{d2}$	Delay time, $\overline{\text{CONVST}}$ falling edge to conversion start			5	ns	Figure 1, Figure 2
$t_{d3}$	Delay time, $\overline{\text{CONVST}}$ falling edge to busy high	+VBD = 3.3 V		14	ns	Figure 1, Figure 2
		+VBD = 5 V		13		
$t_{d4}$	Delay time, conversion end to busy low	+VBD = 3.3 V		8	ns	Figure 1, Figure 2
		+VBD = 5 V		7		
$t_{w3}$	Pulse duration, $\overline{\text{CSTART}}$ high	100			ns	Figure 1, Table 3
$t_{w4}$	Pulse duration, $\overline{\text{CSTART}}$ low	45			ns	Figure 1, Figure 2, Table 3
$t_{d5}$	Delay time, $\overline{\text{CSTART}}$ rising edge to sample start			7.5	ns	Figure 1, Table 3
$t_{d6}$	Delay time, $\overline{\text{CSTART}}$ falling edge to conversion start			7.5	ns	Figure 1, Figure 2, Table 3
$t_{d7}$	Delay time, $\overline{\text{CSTART}}$ falling edge to busy high	+VBD = 3.3 V		16.5	ns	Figure 1, Figure 2, Table 3
		+VBD = 5 V		15.5		
<b>I/O RELATED</b>						
$t_{d8}$	Delay time, $\overline{\text{RD}}$ falling edge while $\overline{\text{CS}}$ low to BUS_BUSY high			16	ns	Figure 5
$t_{d9}$	Delay time, $\overline{\text{RD}}$ falling edge while $\overline{\text{CS}}$ low to SYNC_O and SDO out of 3-state condition (for device with LAT_Y/ $\overline{\text{N}}$ pulled low)	+VBD = 3.3 V		29	ns	Figure 5
		+VBD = 5 V		28		
$t_{d10}$	Delay time, pre_conversion end (point A) to SYNC_O and SDO out of 3-state condition			22	ns	Figure 6
$t_{d11}$	Delay time, pre_conversion end (point A) to BUS_BUSY high	+VBD = 3.3 V		8	ns	Figure 6
		+VBD = 5 V		7		
$t_{d12}$	Delay time, conversion phase end to SYNC_O high	6		$9 + t_{CLK}$	ns	Figure 6
$t_{d13}$	Delay time, $\overline{\text{RD}}$ falling edge while $\overline{\text{CS}}$ low to SYNC_O high	+VBD = 3.3 V	$5.5 + 4 \cdot t_{CLK}$	$8.5 + 5 \cdot t_{CLK}$	ns	Figure 5
		+VBD = 5 V	$5 + 4 \cdot t_{CLK}$	$8 + 5 \cdot t_{CLK}$		
$t_{w5}$	Pulse duration, $\overline{\text{RD}}$ low for device in no latency mode	5			ns	Figure 11
$t_{d14}$	Delay time, CLK_O rising edge to data valid	+VBD = 3.3 V		1.4	ns	Figure 5, Figure 6
		+VBD = 5 V		1.3		
$t_{d15}$	Delay time, BUS_BUSY low to SYNC_O high in daisy chain mode indicating receiving device to output data	+VBD = 3.3 V	$4 \cdot t_{CLK} - 6.5$	$4 \cdot t_{CLK} - 3$	ns	Figure 7, Figure 12
		+VBD = 5 V	$4 \cdot t_{CLK} - 6$	$4 \cdot t_{CLK} - 2.5$		

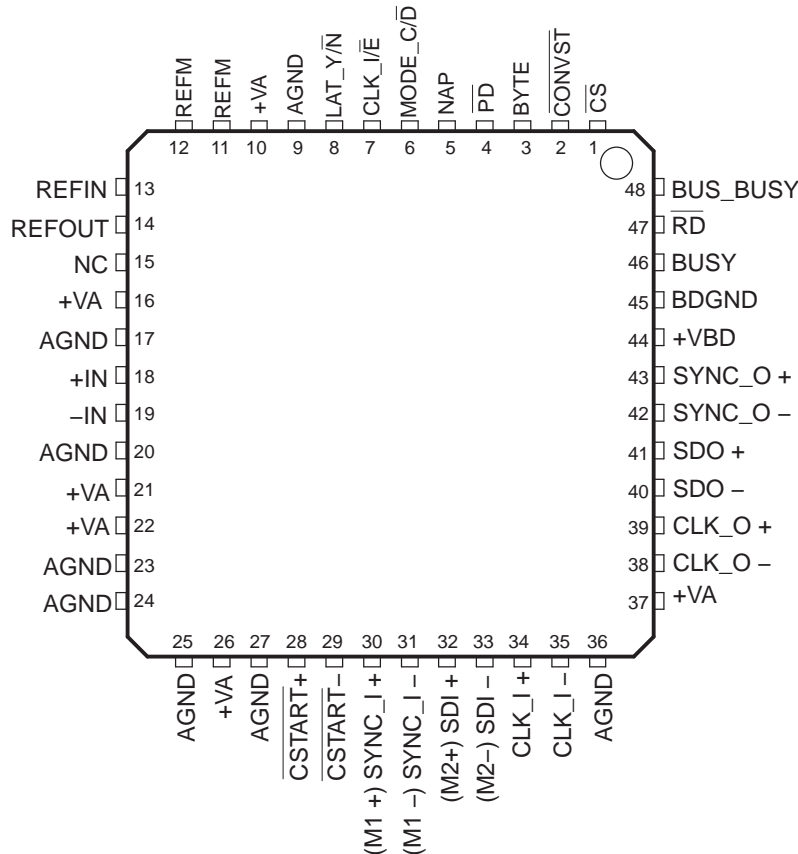
**TIMING REQUIREMENTS (continued)**

T<sub>A</sub> = -40°C to 85°C, +V<sub>A</sub> = 5 V, +V<sub>BD</sub> = 5 V or 3.3 V (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT	REF
t <sub>d16</sub>	Delay time, CLK_O to SDO and SYNC_O 3-state			4	ns	Figure 7, Figure 8, Figure 12, Figure 15
t <sub>pd1</sub>	Propagation delay time, SYNC_I to SYNC_O in daisy chain mode		11 + 0.5*t <sub>CLK</sub>		ns	Figure 12
t <sub>d17</sub>	Delay time, SYNC_O and SDO 3-state to BUS_BUSY low in cascade mode	0		2	ns	Figure 8
t <sub>d18</sub>	Delay time, $\overline{RD}$ rising edge to BUS_BUSY high for device with LAT_Y/ $\overline{N}$ = 1	+V <sub>BD</sub> = 3.3 V		8	ns	Figure 11, Figure 14
		+V <sub>BD</sub> = 5 V		7		
t <sub>d19</sub>	Delay time, point A indicating clear for bus 3-state release to BUSY falling edge	+V <sub>BD</sub> = 3.3 V		40.5	ns	Figure 6
		+V <sub>BD</sub> = 5 V		40		
t <sub>r</sub>	Rise time, differential LVDS output signal			950	ps	Figure 53
t <sub>f</sub>	Fall time, differential LVDS output signal			950	ps	Figure 53
	CLK frequency (serial data rate)	190		210	MHz	
t <sub>d20</sub>	Delay time, from $\overline{PD}$ falling edge to SDO 3-state			10	ns	Figure 22, Figure 23
t <sub>d21</sub>	Delay time, from $\overline{PD}$ falling edge to device powerdown			10	μs	Figure 22, Figure 23
t <sub>d22</sub>	Delay time, from $\overline{PD}$ rising edge to device powerup			25	ms	Figure 22, Figure 23
t <sub>s1</sub>	Settling time, internal reference after first three conversions			4	ms	Figure 22
t <sub>d23</sub>	Delay time, $\overline{CONVST}$ falling edge to start of restricted zone for start of data read cycle	335			ns	Figure 9
t <sub>d24</sub>	Delay time, $\overline{CONVST}$ falling edge to end of restricted zone for start of data read cycle			406	ns	Figure 9

DEVICE INFORMATION

RGZ PACKAGE  
(TOPVIEW)



NC – No internal connection

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
<b>ANALOG PINS</b>			
11, 12	REFM	I	Reference ground. Connect to analog ground plane.
13	REFIN	I	Reference (positive) input. Decouple with REFM pin using 0.1- $\mu$ F bypass capacitor and 1- $\mu$ F storage capacitor.
14	REFOUT	O	Internal reference output. Short to REFIN pin when the internal reference is used. Do not connect to the REFIN pin when an external reference is used. Always decouple with AGND using a 0.1- $\mu$ F bypass capacitor.
18	+IN	I	Noninverting analog input channel
19	-IN	I	Inverting analog input channel (supports $\pm 0.2$ V i/p range)
<b>LVDS I/O PINS<sup>(1)</sup></b>			
28, 29	CSTART+ CSTART-	I	Device sample and convert control input. Device enters sample phase with the rising edge of CSTART and the conversion phase starts with the falling edge of CSTART (provided other conditions are satisfied). Set CSTART = 0 when the CONVST input is used.

(1) All LVDS inputs and outputs are differential with signal+ and signal- lines. Whenever only the 'signal' is mentioned it refers to the signal+ line and the signal- line is the complement. For example CLK\_O refers to CLK\_O+ and CLK\_O- is the complement.

**TERMINAL FUNCTIONS (continued)**

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
30, 31	SYNC_I + SYNC_I-	I Daisy Chain	Connect to previous device SYNC_O with same polarity, while the device is selected to operate in daisy chain mode.
	M1+ M1-	I Cascade	Mode 1 (valid in cascade mode only). CLK_O is available while M1=1 (LVDS) or M1+ is pulled up to +VBD and M1- is grounded (AGND). CLK_O o/p goes to 3-state when M1 = 0 (LVDS) or M1+ is grounded (AGND) and M1- is pulled up to +VBD. Do not allow these pins to float.
32, 33	SDI+ SDI-	I Daisy Chain	Serial data input. Connect to previous device SDO with same polarity, while the device is selected to operate in daisy chain mode.
	M2+ M2-	I Cascade	Mode 2 (valid in cascade mode only). Doubles LVDS o/p current while M2 = 1 (LVDS) or M2+ is pulled up to +VBD and M2- is grounded (AGND). LVDS o/p current is normal (3.4 mA typ) when M2 = 0 (LVDS) or M2+ is grounded (AGND) and M2 - is pulled up to +VBD. Do not allow these pins to float.
34, 35	CLK_I+ CLK_I-	I	Serial external clock input. Set CLK_I/E (pin 7) = 0 to select an external clock source.
38, 39	CLK_O- CLK_O+	O	Serial clock out. Data is latched out on the rising edge of CLK_O and can be captured on the next falling edge.
40, 41	SDO- SDO+	O	Serial data out. Data is latched out on the rising edge of CLK_O with MSB first format.
42, 43	SYNC_O - SYNC_O +	O	Synchronizes the data frame. <sup>(2)</sup>
<b>CMOS I/O PINS</b>			
1	CS	I	Chip select, active low signal. All of the LVDS o/p except CLK_O are 3-state if this pin is high.
2	CONVST	I	CMOS equivalent of CSTART input. So functionality is the same as the CSTART input. Set CONVST = 0 when the CSTART input is used.
3	BYTE	I	Controls the data frame <sup>(3)</sup> duration. The frame duration is 16 CLKs if BYTE = 0 or 8 CLKs if BYTE = 1.
4	PD	I	Active low input, acts as device power down.
5	NAP	I	Selects nap mode while high. Device enters the nap state at conversion end and remains so until the next acquisition phase begins.
6	MODE_C/D	I	Selects cascade (MODE_C/D = 1) or daisy chain mode (MODE_C/D = 0).
7	CLK_I/E	I	Selects the source of the I/O clock. CLK_I/E = 1 selects internally generated clock with 200-MHz typ frequency. CLK_I/E = 0 selects CLK_I as the I/O clock.
8	LAT_Y/N	I	Controls the data read with latency (LAT_Y/N = 1) or without latency ((LAT_Y/N = 0). It is essential to set LAT_Y/N = 0 for the first device in daisy chain or cascade.
46	BUSY	O	Active high signal, indicates a conversion is in progress.
47	RD	I	Data read request to the device, also acts as a handshake signal for daisy chain and cascade operation.
48	BUS_BUSY	O	Status output. Indicates that the bus is being used by the device. Connect to RD of the next device for daisy chain or cascade operation.
<b>POWER SUPPLY PINS</b>			
10, 16, 21, 22, 26, 37	+VA	-	Analog power supply and LVDS input buffer power supply.
9, 17, 20, 23, 24, 25, 27, 36	AGND	-	Analog ground pins. Short to the analog ground plane below the device.
44	+VBD	-	Digital power supply for all CMOS digital inputs and CMOS LVDS outputs.
45	BDGND	-	Digital ground for all digital inputs and outputs. Short to the analog ground plane below the device.

(2) The duration from the first rising edge of SYNC\_O to the second rising edge of SYNC\_O is one data frame. The data frame duration is 16 CLKs if BYTE = 0 or 8 CLKs if BYTE = 1.

(3) The duration from the first rising edge of SYNC\_O to the second rising edge of SYNC\_O is one data frame. The data frame duration is 16 CLKs if BYTE = 0 or 8 CLKs if BYTE = 1.

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O	DESCRIPTION
NO.	NAME		
NOT CONNECTED PINS			
15	NC	–	No connection pins

Table 2. Device Configuration for Various Modes of Operation

OPERATION MODE		DEVICE PINS AND RECOMMENDED LOGIC LEVELS						COMMENTS	REFERENCE FIGURES		
		MODE_C/ $\bar{D}$	CLK_I/ $\bar{E}$	LAT_Y/ $\bar{N}$	M1+	M1–	M2+		M2–	FOR SAMPLING AND CONVERSION	FOR DATA READ
Single device		1	1 or 0	0	+VBD	AGND	AGND	+VBD	Recommended configuration	1 or 2	See Figures 3,4 and 5,6,8 for more details
				or M1 = 1 LVDS		or M2 = 0 LVDS					
		0	1 or 0	0	See comments		See comments		Set SYNC_I and SDI to logic 0 or + terminal to AGND and –ve terminal to +VBD	1 or 2	See Figures 3,4 and 5,6,7 for more details
Multiple devices in daisy chain	1st Device	0	1 or 0	0	See comments		See comments		Set SYNC_I and SDI to logic 0 or + terminal to AGND and –ve terminal to +VBD	1 or 2	See Figures 3,4,11 and 6,12 for more details
	2nd To last device	0	0	1	See comments		See comments		Maximum 4 devices supported at 2 MSPS with 200-MHz CLK	1 or 2	
Multiple devices in cascade	1st Device	1	0	0	+VBD	AGND	AGND	+VBD	Maximum 3 devices supported at 2 MSPS	1 or 2	See Figures 3,4,14 and 6,15 for more details
			or M1 = 1 LVDS		or M2 = 0 LVDS <sup>(1)</sup>						
		1	0	1	+VBD	AGND	AGND	+VBD			
		or M1 = 0 LVDS		or M2 = 0 LVDS <sup>(1)</sup>							

(1) Specified polarity is suitable for a 100-Ω differential load across the LVDS outputs. However, polarity can be reversed to double the output current in order to support two 100-Ω loads on both ends of the transmission lines, resulting in 50-Ω net load.

DETAILED DESCRIPTION

SAMPLE AND CONVERT

The sampling and conversion process is controlled by the  $\overline{CSTART}$  (LVDS) or  $\overline{CONVST}$  (CMOS) signal. Both signals are functionally identical. The following diagrams show control with  $\overline{CONVST}$ . The rising edge of  $\overline{CONVST}$  (or  $\overline{CSTART}$ ) starts the sample phase, if the conversion has completed and the device is in the wait state. Figure 2 shows the case when the device is in the conversion phase at the rising edge of  $\overline{CONVST}$ . In this case, the sample phase starts immediately at the end of the conversion phase and there is no wait state.

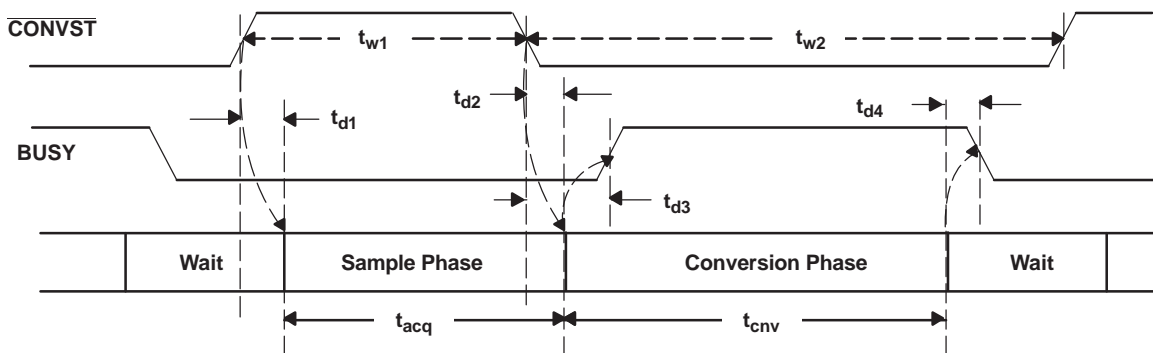
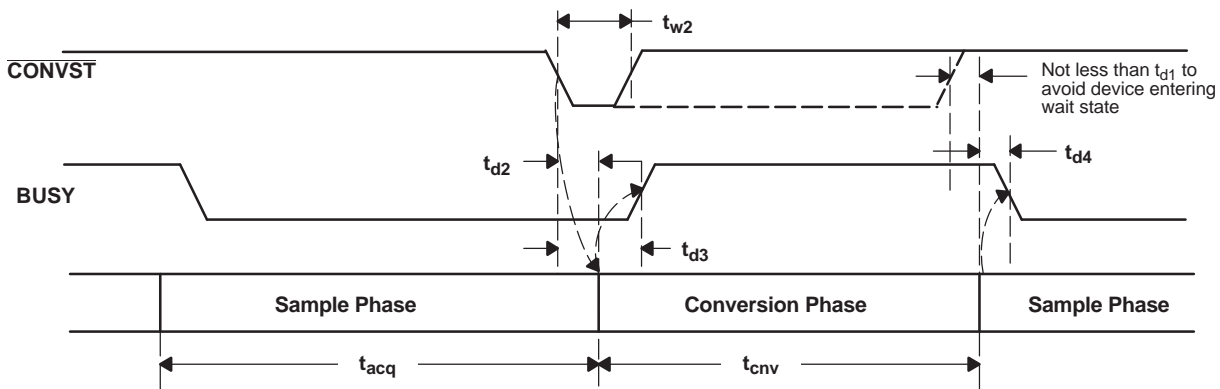


Figure 1. Sample and Convert With Wait (Less Than 2 MSPS Throughput)



**Figure 2. Sample and Convert With No Wait or Back to Back (2 MSPS Throughput)**

The device ends the sample phase and enters the conversion phase on the falling edge of  $\overline{\text{CONVST}}$  ( $\overline{\text{CSTART}}$ ). A high level on the  $\overline{\text{BUSY}}$  output indicates an ongoing conversion. The device conversion time is fixed. The falling edge of  $\overline{\text{CONVST}}$  ( $\overline{\text{CSTART}}$ ) during the conversion phase aborts the ongoing conversion. A data read after a conversion abort fetches invalid data. Valid data is only available after a sample phase and a conversion phase has completed. The timing diagram for control with  $\overline{\text{CSTART}}$  is similar to Figure 1 and Figure 2. Table 3 shows the equivalent timing for control with  $\overline{\text{CONVST}}$  and  $\overline{\text{CSTART}}$ .

**Table 3.  $\overline{\text{CONVST}}$  and  $\overline{\text{CSTART}}$  Timing Control**

TIMING CONTROL WITH $\overline{\text{CONVST}}$	TIMING CONTROL WITH $\overline{\text{CSTART}}$
$t_{w1}$	$t_{w3}$
$t_{w2}$	$t_{w4}$
$t_{d1}$	$t_{d5}$
$t_{d2}$	$t_{d6}$
$t_{d3}$	$t_{d7}$

**DATA READ OPERATION**

The ADS8410 supports a 200-MHz serial LVDS interface for data read operation. The three signal LVDS interface (SDO, CLK\_O, and SYNC\_O) is well suited for high-speed data transfers. An application with a single device or multiple devices can be implemented with a daisy chain or cascade configuration. The following sections discuss data read timing when a single device is used.

**DATA READ FOR A SINGLE DEVICE (See Table 1 for Device Configuration)**

For a single device, there are two possible read cycle starts: a data read cycle start during a wait or sample phase or a data read cycle start at the end of a conversion phase. Read cycle end conditions can change depending on MODE C/D selection. Figure 3 explains the data read cycle. The details of a read frame start with the two previous listed conditions and a read cycle end with MODE C/D selection are explained in Figure 5 and Figure 6 and Figure 7 and Figure 8, respectively.

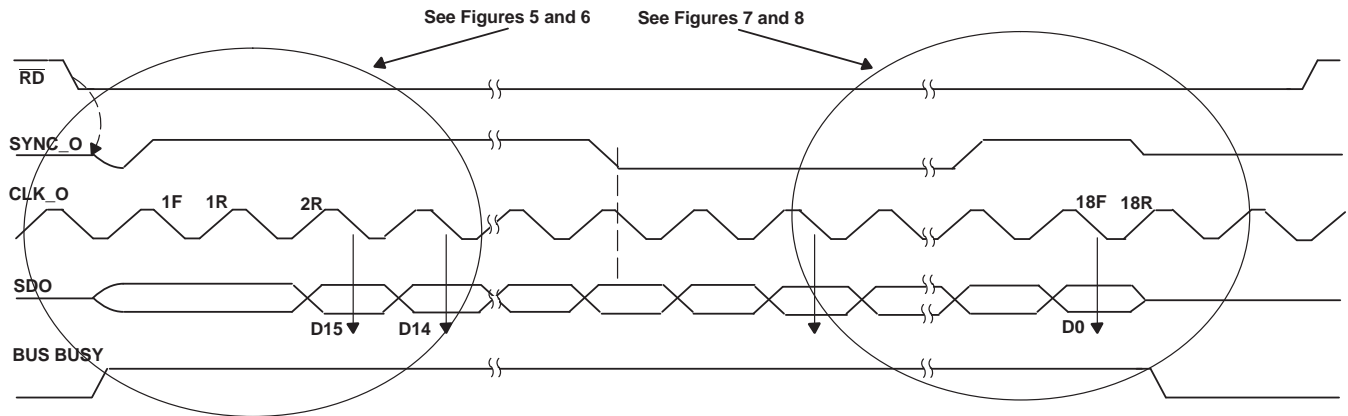


Figure 3. Data Read With  $\overline{CS}$  Low and BYTE = 0

As shown in Figure 3, a new data read cycle is initiated with the falling edge of  $\overline{RD}$ , if  $\overline{CS}$  is low and the device is in a wait or sample phase. The device releases the LVDS o/p (SYNC\_O, SDO) from 3-state and sets BUS\_BUSY high at the start of the read cycle. The SYNC\_O cycle is 16 clocks wide (rising edge to rising edge) if BYTE i/p is held low and can be used to synchronize a data frame. The clock count begins with the first CLK\_O falling edge after a SYNC\_O rising edge. The MSB is latched out on the second rising edge (2R) and each subsequent data bit is latched out on the rising edge of the clock. The receiver can shift data bits on the falling edges of the clock. The next rising edge of SYNC\_O coincides with the 16th rising edge of the clock. D0 is latched out on the 17th rising edge of the clock. The receiver can latch the de-serialized 16-bit word on the 18th rising edge (18R, or the second rising edge after a SYNC\_O rising edge).

$\overline{CS}$  high during a data read 3-states SYNC\_O and SDO. These signals remain in 3-state until the start of the next data read cycle.

### DATA READ IN BYTE MODE

Byte mode is selected by setting BYTE = 1; this mode is allowed for any condition listed in Table 2. Figure 4 shows a data read operation in byte mode.

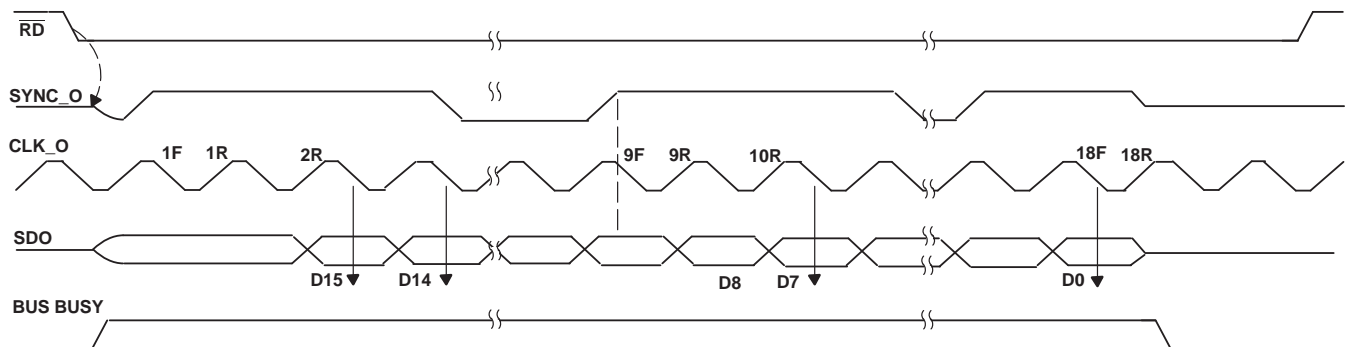


Figure 4. Data Read Timing Diagram with  $\overline{CS}$  Low and BYTE = 1

Similar to Figure 3, a new data read cycle is initiated with the falling edge of  $\overline{RD}$ , if  $\overline{CS}$  is low and the device is in a wait or sample phase. The device releases the LVDS o/p (SYNC\_O, SDO) from 3-state and sets BUS\_BUSY high at the start of the read cycle. The SYNC\_O cycle is 8 clocks wide (rising edge to rising edge) if BYTE i/p is held high and can be used to synchronize a data frame. The clock count begins with the first falling edge of CLK\_O after the rising edge of SYNC\_O. The MSB is latched out on the second rising edge (2R) and each subsequent data bit is latched out on the rising edge of the clock. The receiver can shift data bits on the falling edges of clock. The next rising edge of SYNC\_O coincides with the 8th rising edge of the clock. D8 is latched out on the 9th rising edge of the clock. The receiver can latch the de-serialized higher byte on the 10th rising edge (10R, or second rising edge after a SYNC\_O rising edge). The de-serialized lower byte can be latched on the 18th rising edge (18R).

$\overline{CS}$  high during a data read 3-states SYNC\_O and SDO. These signals remain in 3-state until the start of the next data read cycle.

**DATA READ CYCLE START DURING WAIT OR SAMPLE PHASE**

As shown in Figure 5, the falling edge of  $\overline{RD}$ , with  $\overline{CS}$  low and the device is in a wait or sample phase, triggers the start of a read cycle. The cycle starts when BUS\_BUSY goes high and SYNC\_O and SDO are released from 3-state. SYNC\_O is low at the start and rises to a high level  $t_{d13}$  ns after the falling edge of  $\overline{RD}$ . As shown in Figure 5, the MSB is shifted on the 2nd rising edge of the clock (2R). Other details about the data read cycle are discussed in the previous section (see Figure 3).

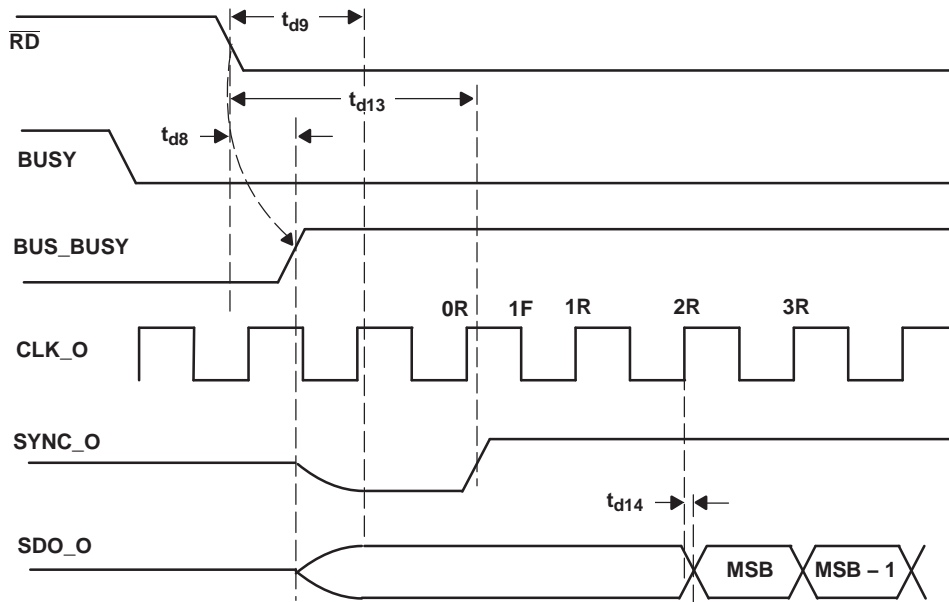


Figure 5. Start of Data Read Cycle with  $\overline{RD}$  with  $\overline{CS}$  Low and Device in Wait or Sample Phase

**DATA READ CYCLE START AT END OF CONVERSION PHASE (Read Without Latency, Back-to-Back)**

This mode is optimized for a data read immediately after the end of a conversion phase and ensures the data read is complete before the sample end while running at 2 MSPS. Point A in Figure 6 indicates a 'pre\_conversion\_end'; it occurs  $t_{d19}$  ns before the falling edge of BUSY or  $[(t_{d2} + t_{cnv} + t_{d4}) - t_{d19}]$  ns after the falling edge of  $\overline{CONVST}$ . A read cycle is initiated at point A if  $\overline{RD}$  is issued before point A while  $\overline{CS}$  is low. Alternately,  $\overline{RD}$  and  $\overline{CS}$  can be held low. At the start of the read cycle, BUS\_BUSY rises to a high level and the LVDS outputs are released from 3-state. The rising edge of SYNC\_O occurs  $t_{d12}$  ns after the conversion end. As shown in Figure 6, the MSB is shifted on the 2nd rising edge of the clock (2R). Other details about the data read cycle are discussed in the previous section (see Figure 3).

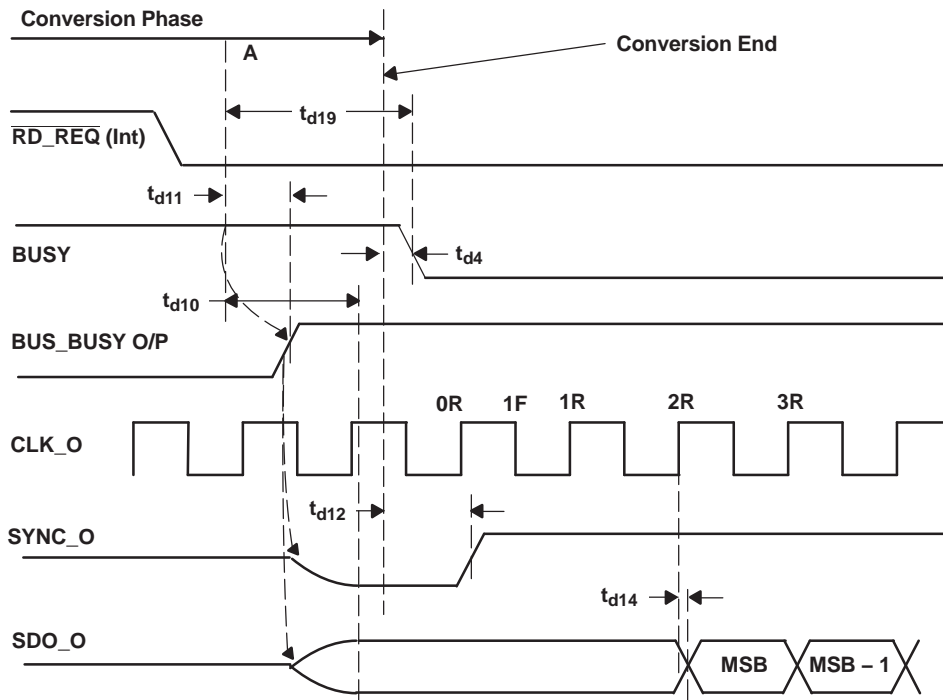


Figure 6. Start of Data Read Cycle with End of Conversion

**DATA READ CYCLE END (With MODE  $C/\bar{D} = 0$ )**

A data read cycle ends after all 16 bits have been serially latched out. Figure 7 shows the timing of the falling edge of BUS\_BUSY and the rising edge of SYNC\_O with respect to SDO. SYNC\_O rises on the 16th rising edge of CLK\_O. As shown in Figure 5 and Figure 6, the MSB is shifted out on the 2nd rising edge of CLK\_O. Therefore, the LSB-1 is shifted out on the 16th rising edge of CLK\_O.

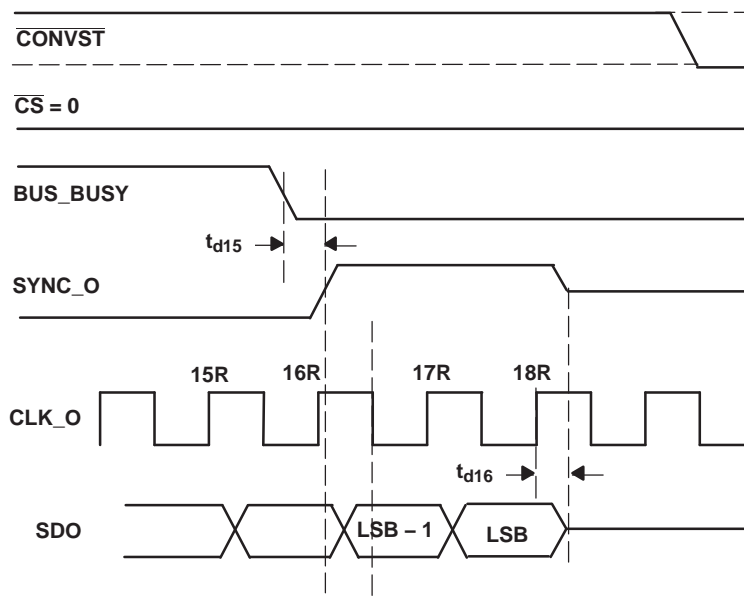
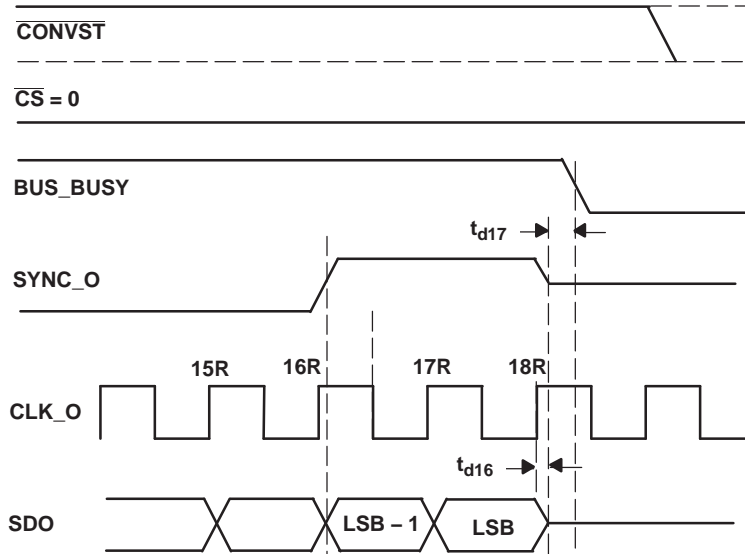


Figure 7. Data Read Cycle End with MODE  $C/\bar{D} = 0$

The next two rising edges of CLK\_O are shown as 17R and 18R in Figure 7. On 17R the LSB is latched out, and on 18R SDO and SYNC\_O go to 3-state. Note that BUS\_BUSY falls  $t_{d15}$  ns before the rising edge of SYNC\_O when MODE C/D = 0. Care must be taken not to allow LVDS bus usage by any other device until the end of the read cycle or  $(t_{d15} + 2/f_{clk} + t_{d16})$  ns after the falling edge of BUS\_BUSY.

**DATA READ CYCLE END (With MODE C/D = 1)**

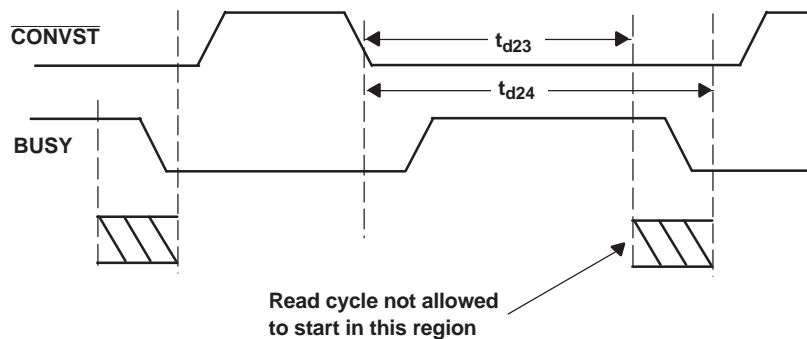
A data read cycle ends after all 16 bits have been serially latched out. Figure 8 shows the timing of the falling edge of BUS\_BUSY and the rising edge of SYNC\_O with respect to SDO. SYNC\_O rises on the 16th rising edge of CLK\_O. As shown in Figure 5 and Figure 6, the MSB is shifted out on the 2nd rising edge of CLK\_O. Therefore, the LSB-1 is shifted out on the 16th rising edge of CLK\_O.



**Figure 8. Data Read Cycle End with MODE C/D = 1**

The next two rising edges of CLK\_O are shown as 17R and 18R in Figure 8. On 17R the LSB is latched out and on 18R SDO and SYNC\_O go to 3-state. In cascade mode (with MODE C/D = 1), unlike daisy chain mode, the falling edge of BUS\_BUSY occurs after the LVDS outputs are 3-stated. One can use the falling edge of BUS\_BUSY to allow LVDS bus usage by any other device.

**RESTRICTIONS ON READ CYCLE START**



**Figure 9. Read Cycle Restriction Region**

The start of a data read cycle is not allowed in the region bound by  $t_{d23}$  and  $t_{d24}$ . Previous conversion results are available for a data read cycle start before this region, and current conversion results are available for a read cycle start after this region.



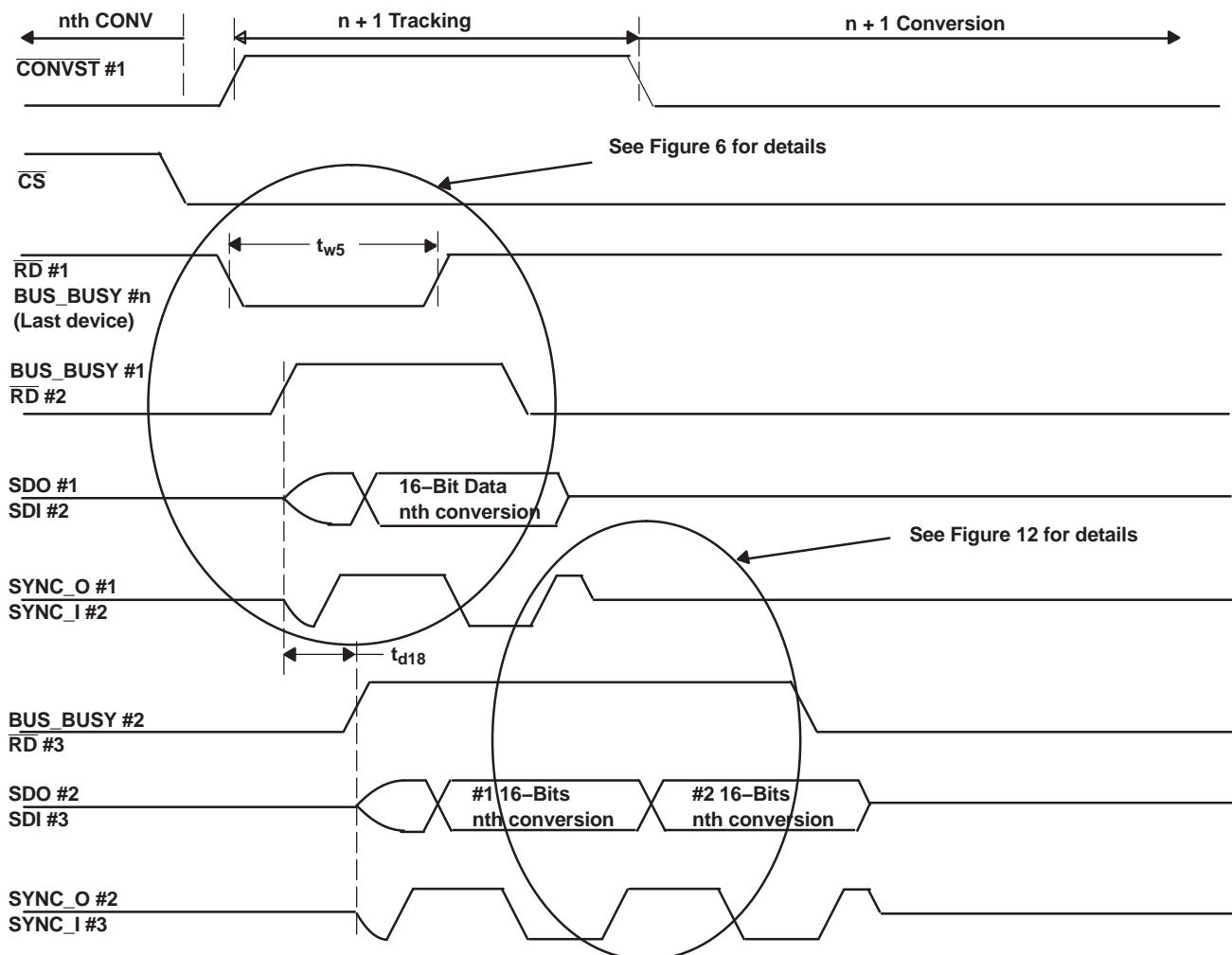


Figure 11. Data Read Operation for Devices in Daisy Chain

**DATA READ OPERATION**

On power up, BUS\_BUSY of all of the devices is low. The devices receive  $\overline{\text{CONVST}}$  or  $\overline{\text{CSTART}}$  to sample and start the conversion. The first device in the chain starts the data read cycle at the end of its conversion. BUS\_BUSY of device 1 (connected to RD of device 2) goes high on the read cycle start. Device 2 BUS\_BUSY goes high on the rising edge of RD. This propagates until the last device in the chain. Device 2 receives CLK\_I, SDI, and SYNC\_I from device 1 and it passes all of these signals to the next device. Device 2 (and every subsequent device in the chain) passes the received signals to its output until it sees the falling edge of RD (same as BUS\_BUSY of the previous device). In daisy chain mode, BUS\_BUSY for any device falls when it has passed all of the previous device data followed by its own data. The falling edge of BUS\_BUSY occurs before the rising edge of SYNC\_O. This indicates to the receiving device that the previous data chain is over and it is its own turn to output the data. The device outputs the data from the last completed conversion. BUS\_BUSY of the last device in the chain is fed back to RD of the first device as shown in Figure 10 (or device 1 RD tied to 0). This makes sure that RD of device 1 is low before its conversion is over. The chain continues with only one external signal ( $\overline{\text{CONVST}}$  or  $\overline{\text{CSTART}}$ ) when CS is held low. Every device LVDS output goes to 3-state once all data transfer through the device has been completed.

CS going high during the data read cycle of any device 3-states its SYNC\_O and SDO. This halts the propagation of data through the chain. To reset this condition it is necessary to assert CS high for all devices. The new read sequence starts only after CS for all devices is low before point A shown in Figure 6. The high pulse on CS must be at least 20 ns wide. It is better to connect CS of all of the devices together to avoid undesired halting of the daisy chain.

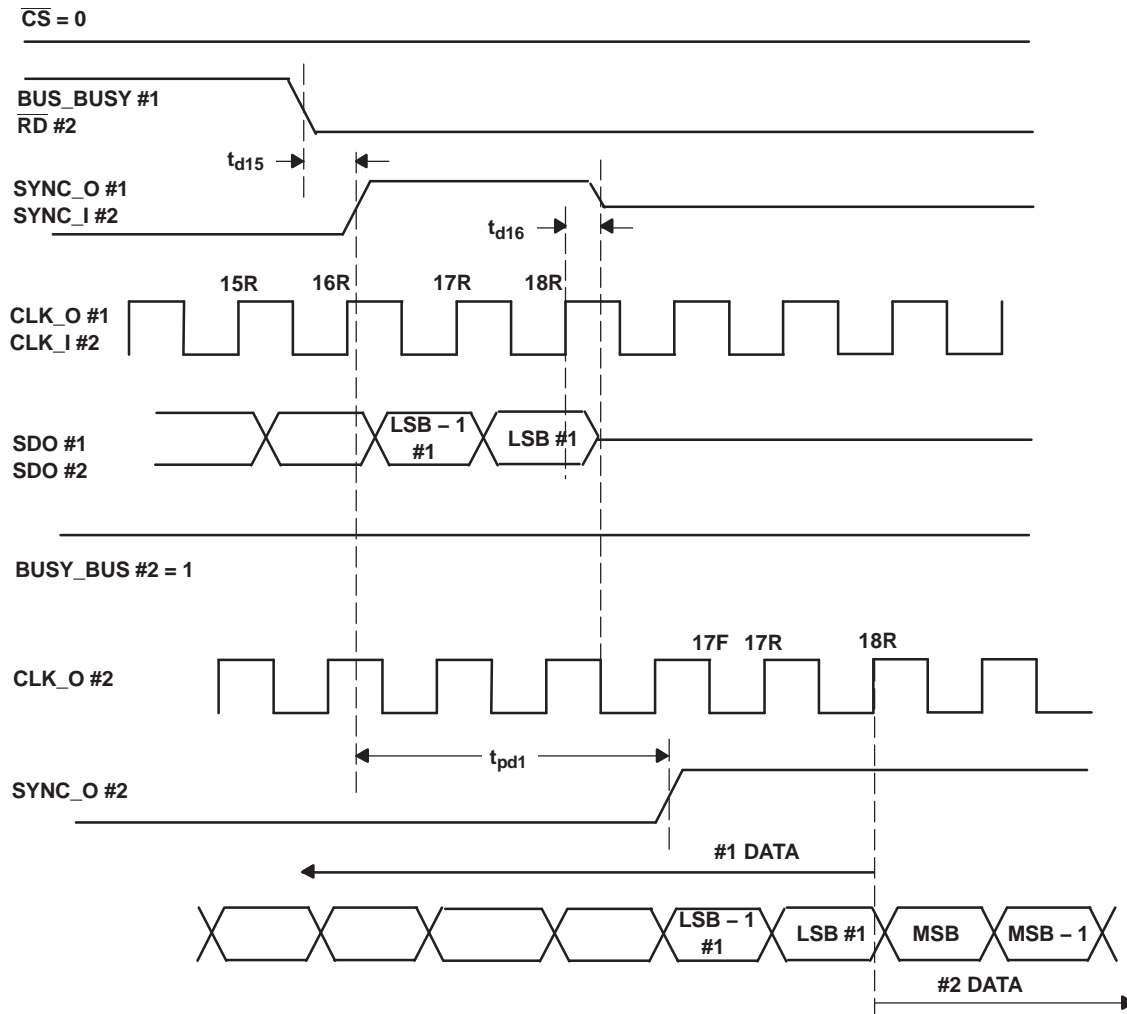


Figure 12. Data Propagation from Device  $n$  to Device  $n+1$  in Daisy Chain Mode

As shown in Figure 12 there is a propagation delay of  $t_{pd1}$  from SYNC\_I to SYNC\_O or SDI to SDO. Note that the data frames of all devices in the chain appear seamless at the last device output. The rising edge of SYNC occurs at an interval of 16 clocks (or 8 clocks in BYTE mode); this can be used as a data frame sync. The deserializer at the output of the last device can shift the data on every falling edge of the clock and it can latch the parallel 16-bit word on the second rising edge of CLK\_O (shown as 18R) after every rising edge of SYNC\_O.

## CASCADE

Figure 13 shows the cascade connection. The signals shown by double lines are LVDS and the others are CMOS. Cascade mode is selected by setting  $MODE\_C/D = 1$ . Similar to daisy chain, the first device in the chain is identified by selecting  $LAT\_Y/\bar{N} = 0$ . For all other devices in the chain  $LAT\_Y/\bar{N} = 1$ . See Table 2 for more details on device configuration. SDO, CLK\_O, and SYNC\_O are connected to the common bus. This means only one device occupies the bus at a time while the LVDS drivers for all other devices 3-state. Unlike SDO and SYNC\_O, the clock cannot be switched out from device to device as the receiver requires a continuous clock. So only device 1 outputs the clock and CLK\_O of all other devices is 3-stated by appropriately setting M1+ and M1- as listed in Table 2.

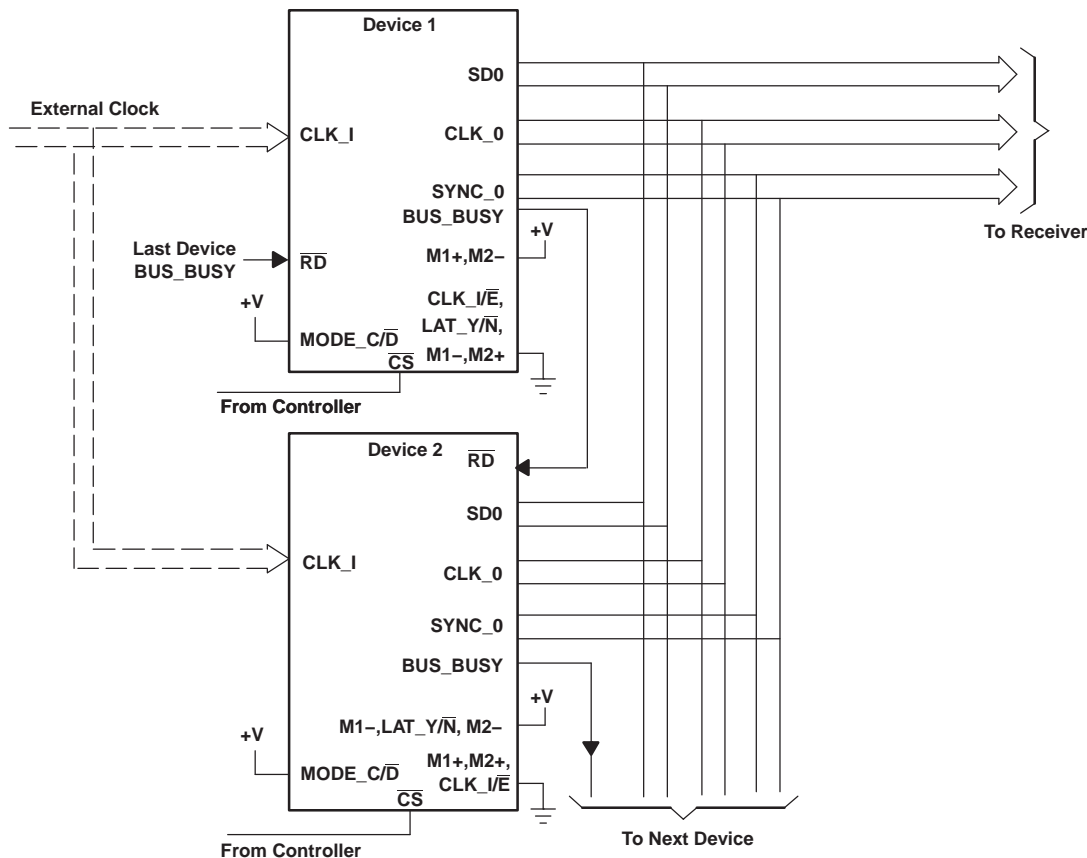


Figure 13. Cascade Connection

**CLOCK SOURCE**

In this mode it is very critical to control the skew between the three LVDS o/p signals. It is recommended to use external clock mode only for all of the devices in cascade. BUS\_BUSY of device *n* is connected to RD of device *n + 1* and so on. Finally BUS\_BUSY of the last device in the chain is to be connected to RD of device 1. This ensures the necessary handshake to control the sequence of data reads for all of the devices in cascade. (It is also allowed to tie RD to 0 for device 1.)

**TIMING DIAGRAMS FOR CASCADE OPERATION**

The conversion rate for *n* devices in cascade must be selected such that:

**1/conversion speed > first device read cycle duration + (n - 1) next device read cycle duration**

**First device read cycle duration = read startup delay<sub>1</sub> + data frame duration + (t<sub>d16</sub> + t<sub>d17</sub>)**

**Next device read cycle duration = read startup delay<sub>n</sub> + data frame duration + (t<sub>d16</sub> + t<sub>d17</sub>)**

**Read startup delay<sub>1</sub> = 10 ns + (t<sub>d19</sub> - t<sub>d4</sub> + t<sub>d12</sub>) + 2/f<sub>clk</sub>**

**Read startup delay<sub>n</sub> = (t<sub>d13</sub> + 2/f<sub>clk</sub>)**

**Data frame duration = 16/f<sub>clk</sub>** Note that it is not necessary that all devices in the chain sample the data simultaneously. But all of the devices must operate with the same exact conversion speed.

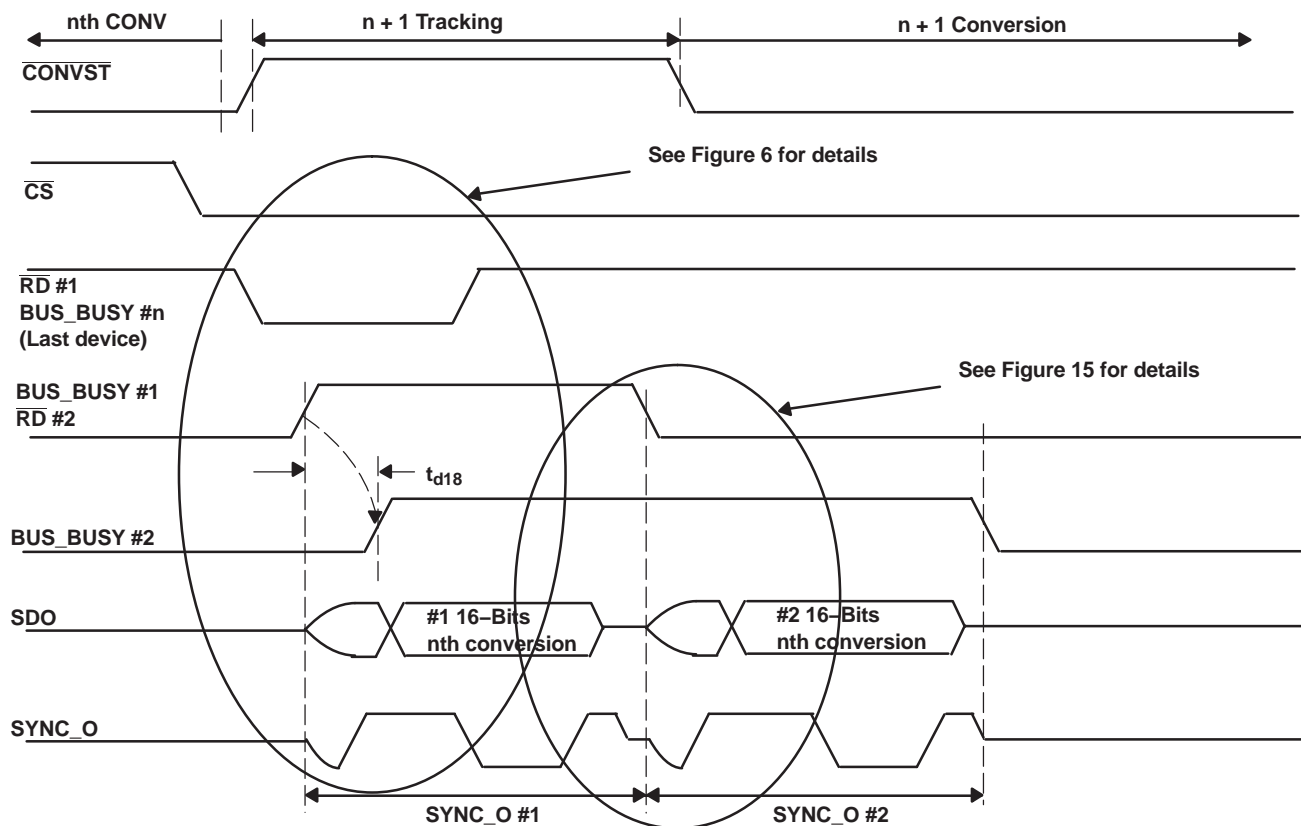


Figure 14. Data Read Operation for Devices in Cascade Mode

### DATA READ OPERATION

On power up, BUS\_BUSY for all of the devices is low. The devices receive  $\overline{\text{CONVST}}$  or  $\overline{\text{CSTART}}$  to sample and start the conversion. The first device starts the data read cycle at the end of its conversion. BUS\_BUSY of device 1 (connected to  $\overline{\text{RD}}$  of device 2) goes high on the read cycle start indicating that it wants to occupy the bus. Device 2 BUS\_BUSY goes high on the rising edge of  $\overline{\text{RD}}$ . This propagates until the last device.

Device 1 BUS\_BUSY goes low after it outputs its data; at this time SDO and SYNC\_O for device 1 go to 3-state. The falling edge of BUS\_BUSY ( $\overline{\text{RD}}$  of the next device) indicates to the next device that it is its turn to output the data. The next device outputs the data from the last completed conversion. BUS\_BUSY of the last device goes low and its SYNC\_O and SDO go to 3-state after it outputs its data. BUS\_BUSY of the last device is fed back to  $\overline{\text{RD}}$  of the first device as shown in Figure 13 ( $\overline{\text{RD}}$  can also be tied to 0 for device 1). This ensures that  $\overline{\text{RD}}$  of device 1 is low before its conversion is over. The data read sequence continues with only one external signal,  $\overline{\text{CONVST}}$  or  $\overline{\text{CSTART}}$ , when CS = 0. For any device, CS high during the data read cycle 3-states SYNC\_O and SDO of the device and halts the data read sequence. To reset this condition it is necessary to assert  $\overline{\text{CS}}$  high for all of the devices. The new read sequence starts only after  $\overline{\text{CS}}$  for all of the devices is low before point A shown in Figure 6. The high pulse on  $\overline{\text{CS}}$  must be at least 20 ns wide. It is better to connect  $\overline{\text{CS}}$  for all of the devices together to avoid undesired halting of the data read sequence.

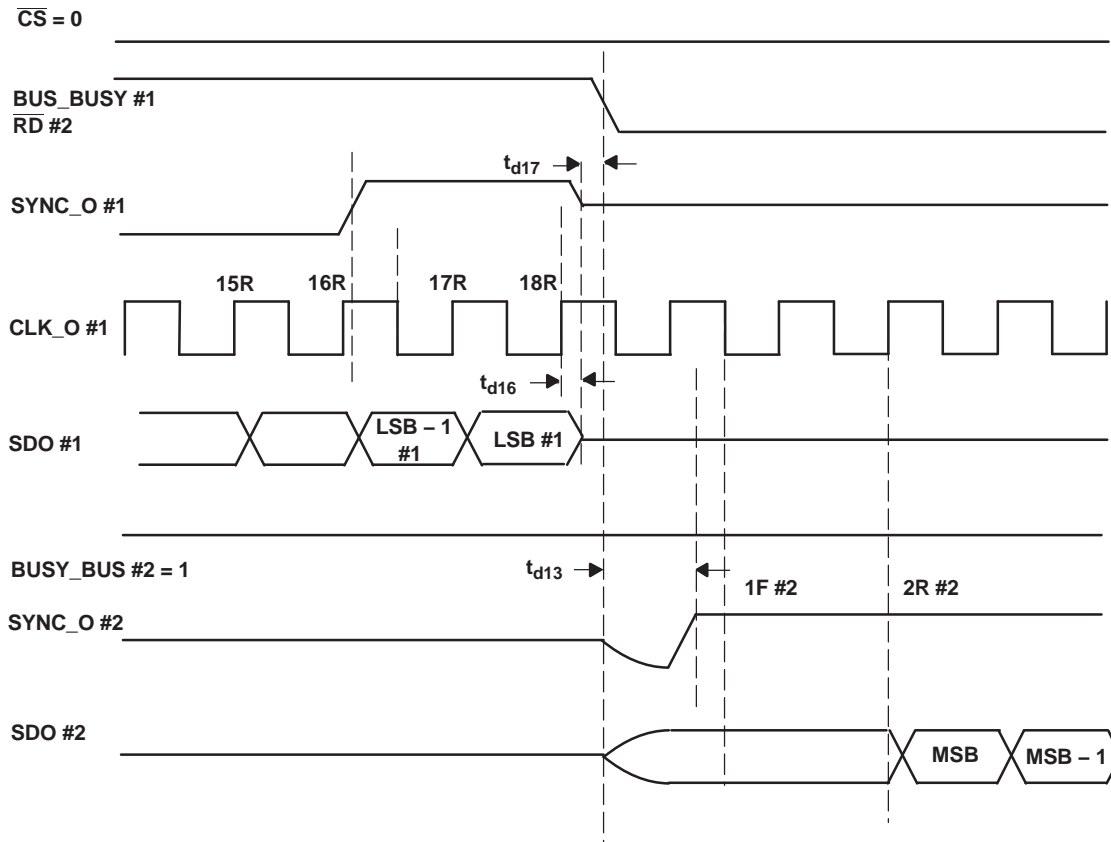


Figure 15. Device n Read Cycle End and Device n+1 Read Cycle Start

Unlike daisy chain, the data frames of all the devices in cascade are not seamless and there is a loss of time between one device 3-state to other device data valid due to wakeup time from 3-state and a two clock phase shift between SYNC and data (see Figure 15 for details). As a result, the number of data frames per second in this mode are less than in daisy chain mode. Also, a maximum of 4 devices can be cascaded on the same bus. But, I/O power per device is considerably lower in cascade as compared to daisy chain as each device LVDS o/p goes to 3-state after its data transfer. The deserializer at the output of the last device can shift the data on every clock falling edge, and it can latch the parallel 16-bit word on the second CLK\_O rising edge (shown as 18R) after every SYNC\_O rising edge.

### THEORY OF OPERATION

The ADS8410 is a member of the high-speed successive approximation register (SAR) analog-to-digital converters family. The architecture is based on charge redistribution, which inherently includes a sample/hold function. The device includes a built-in conversion clock, internal reference, and 200-MHz LVDS serial interface. The device can be operated at maximum throughput of 2 MSPS.

### ANALOG INPUT

An analog input is provided to two input pins: +IN and -IN. When a conversion is initiated, the voltage difference between these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

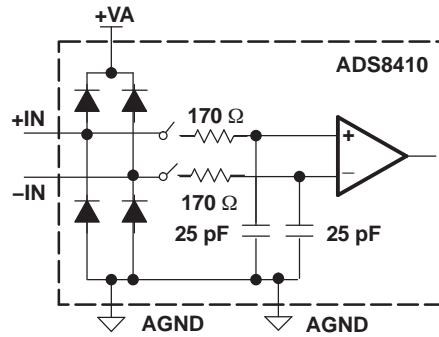


Figure 16. Simplified Input Circuit

When the converter enters hold mode, the voltage difference between the +IN and -IN inputs is captured on the internal capacitor array. The input current on the analog inputs depends upon a number of factors: sample rate, input voltage, signal frequency, and source impedance. Essentially, the current into the ADS8410 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current (this may not happen when the signal is moving continuously). The source of the analog input voltage must be able to charge the input capacitance (25 pF) to better than a 16-bit settling level with a step input within the acquisition time of the device. For calculation, the step size can be selected equal to the maximum voltage difference between two consecutive samples at the maximum signal frequency (see the TYPICAL ANALOG INPUT CIRCUIT section). When the converter goes into hold mode, the input impedance is greater than 1GΩ.

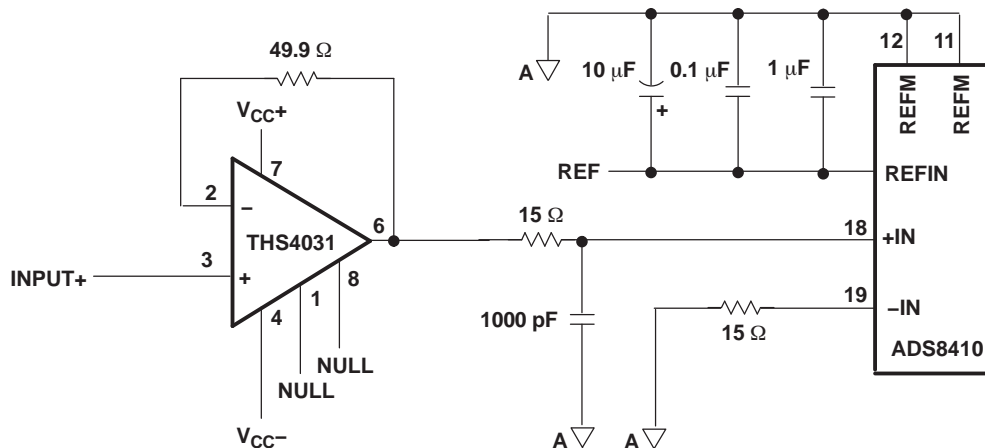


Figure 17. Typical Analog Input Schematic

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, both -IN and +IN inputs should be within the limits specified. Outside of these ranges, the converter linearity may not meet specifications. Care should be taken to ensure that +IN and -IN see the same impedance to the respective sources. If this is not observed, the two inputs could have different settling times. This may result in offset error, gain error, and linearity error which changes with temperature and input voltage.

## REFERENCE

The ADS8410 has a built-in 4.096-V (nominal value) reference. The ADS8410 can also operate with an external reference. When the internal reference is used, pin 14 (REFOUT) should be connected to pin 13 (REFIN), and a 0.1-μF decoupling capacitor and 1-μF storage capacitor must be connected between pin 14 (REFOUT) and pins 11 and 12 (REFM) (see Figure 18). The internal reference of the converter is buffered.

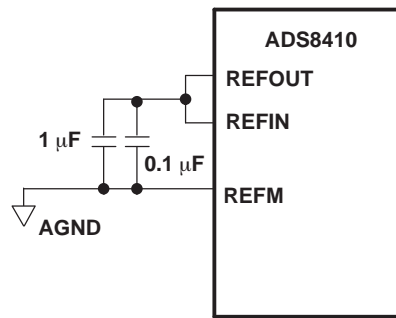


Figure 18. Using Internal Reference

The REFIN pin is also internally buffered. This eliminates the need to put a high bandwidth buffer onboard to drive the ADC reference and saves system area and power. When an external reference is used, the reference must be low noise, which can be achieved by the additional bypass capacitor from the REFIN pin to the REFM pin (see Figure 19). REFM must be connected to the analog ground plane.

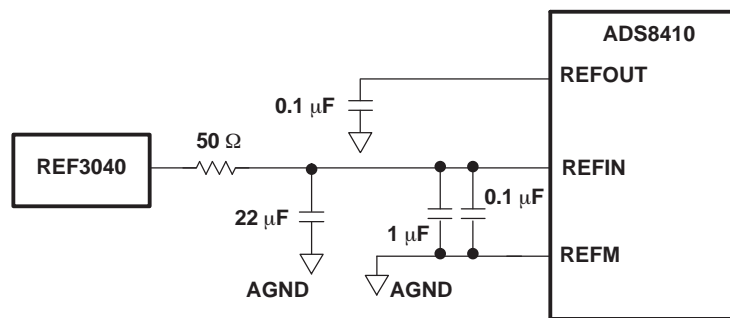


Figure 19. Using External Reference

**DIGITAL INTERFACE**

**TIMING AND CONTROL**

Refer to the timing diagrams and TIMING REQUIREMENTS table for detailed information.

**SAMPLING AND CONVERSION**

Sampling and conversion is controlled by the  $\overline{\text{CONVST}}$  pin. For higher noise performance it is essential to have low jitter on the falling edge of CONVST. The device uses the internally generated clock for conversion, hence it has a fixed conversion time.

**READING DATA**

The ADS8410 includes a high-speed LVDS serial interface. As discussed prior, an external clock (CLK\_I, less than 200 MHz) or an internal 200-MHz clock can be used for a data read. The device outputs data in two's complement format. Table 4 lists the ideal output codes.

Table 4. Ideal Input Voltages and Output Codes

DESCRIPTION	ANALOG VALUE (+IN – (–IN))	HEX CODE
Full-scale range	$+V_{ref}$	–
Least significant bit (LSB)	$+V_{ref}/2^{16}$	–
Full scale	$V_{ref} - 1 \text{ LSB}$	FFFF
Midscale	$+V_{ref}/2$	8000
Midscale – 1 LSB	$V_{ref}/2 - 1 \text{ LSB}$	7FFF

Table 4. Ideal Input Voltages and Output Codes (continued)

DESCRIPTION	ANALOG VALUE (+IN – (-IN))	HEX CODE
Zero	0 V	0000

The restrictions on read cycle start are described in the section RESTRICTIONS ON READ CYCLE START (see Figure 9).

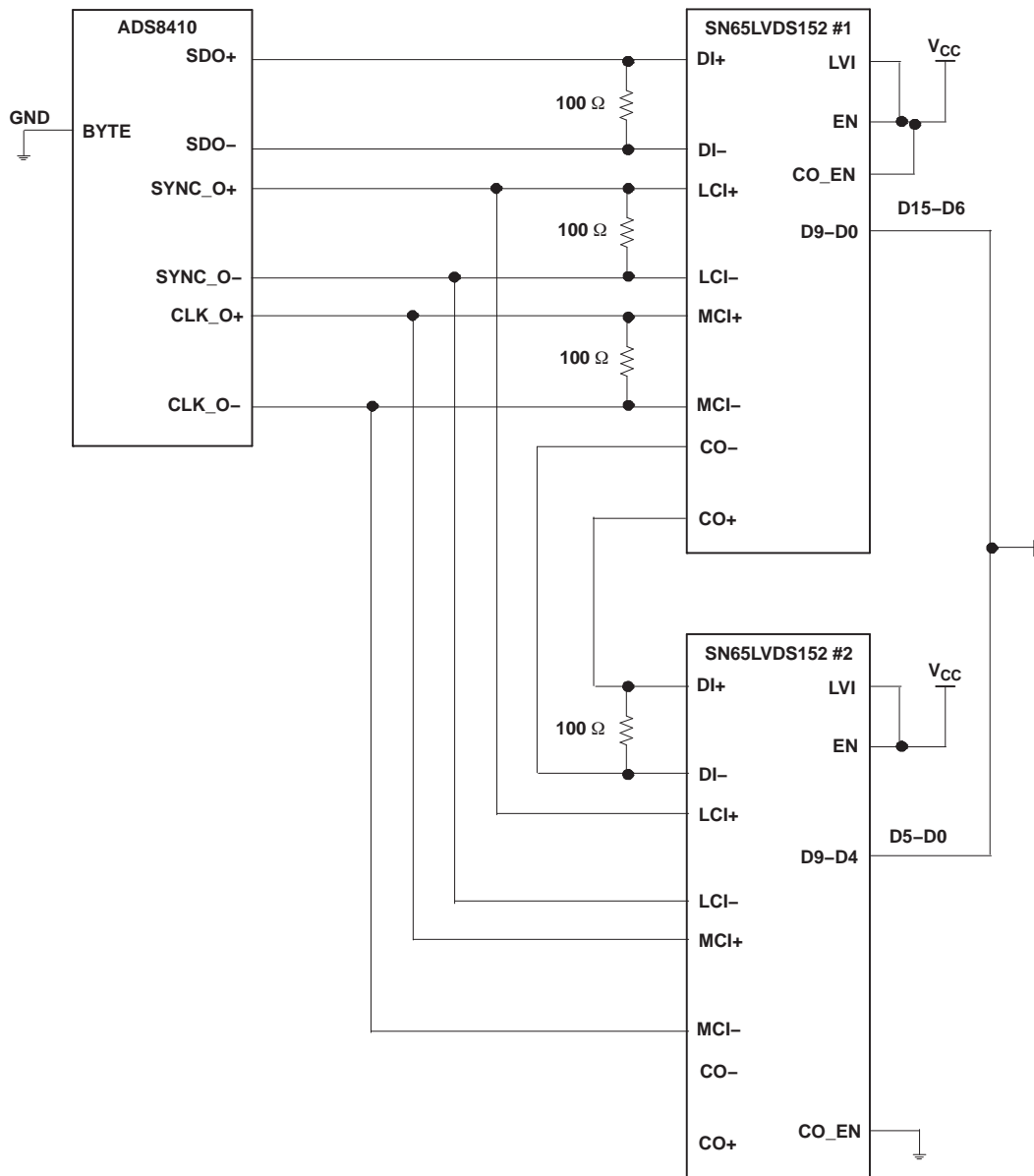


Figure 20. 16-Bit Data De-Serialization While BYTE = 0

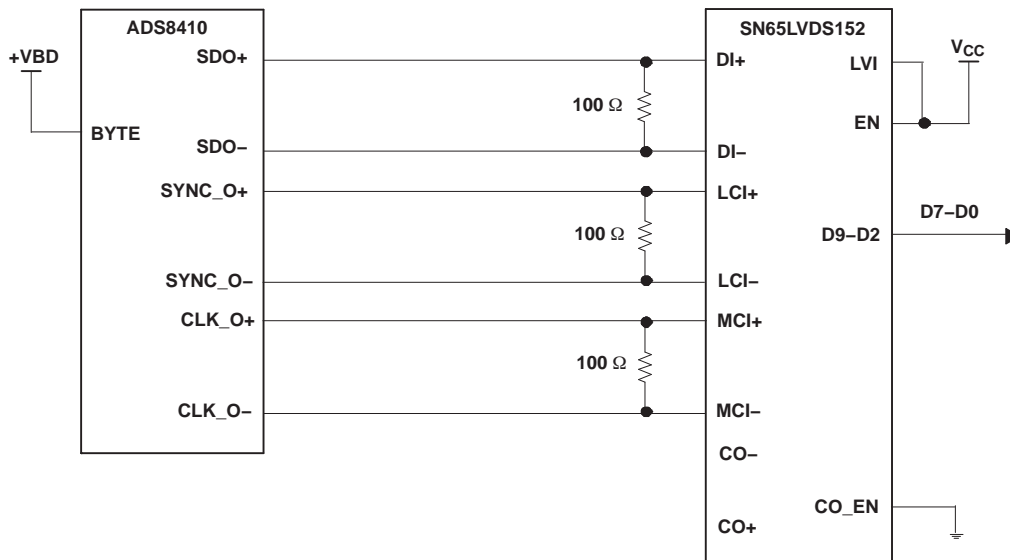


Figure 21. 8-Bit Data De-Serialization While BYTE = 1, Data

**POWER SAVING**

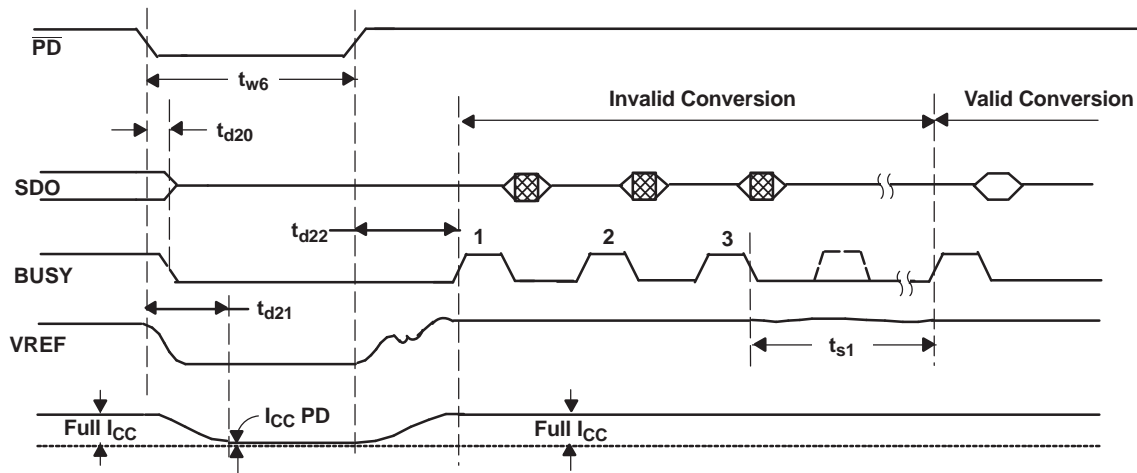
The converter provides two power saving modes, full powerdown and nap. Table 5 lists information on the activation/deactivation and resumption times for both modes.

Table 5. Powerdown Modes

POWERDOWN MODE	SDO	POWER CONSUMPTION	ACTIVATED BY	ACTIVATION TIME	RESUME POWER BY
Normal operation	Refer to DATA READ OPERATION section	58 mA	NA	NA	NA
Full powerdown (internal reference)	3 Stated	1 $\mu$ A	$\overline{\text{PD}} = 0$	$t_{d21}$	$\overline{\text{PD}} = 1$
Full powerdown (external reference)	3 Stated	1 $\mu$ A	$\overline{\text{PD}} = 0$	$t_{d21}$	$\overline{\text{PD}} = 1$
Nap powerdown	Not 3 stated	25 mA	Nap = 1	150 ns	Sample start

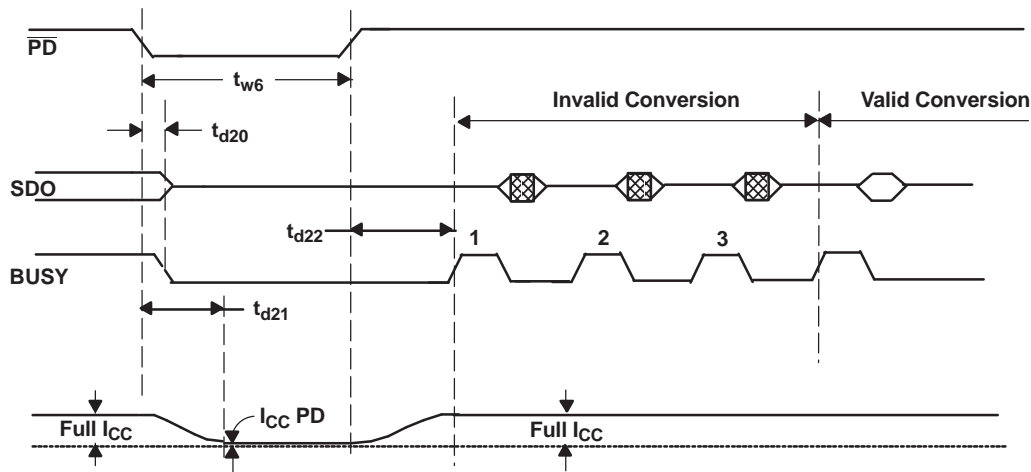
**FULL POWERDOWN MODE**

Full powerdown mode is activated by deasserting  $\overline{\text{PD}} = 0$ ; the device takes  $t_{d21}$  ns to reach the full powerdown state. The device can return to normal mode from full powerdown by asserting  $\overline{\text{PD}} = 1$ . The powerup sequence is different for device operation with an internal reference or external reference as shown in Figure 22 and Figure 23.



**Figure 22. Device Full Powerdown and Powerup Sequence with Device Operation in Internal Reference Mode**

When an internal reference is used, a conversion can be started  $t_{d22}$  ns after asserting  $\overline{PD} = 1$ . After the first three conversions,  $t_{s1}$  ns are required for reference voltage settling to the trimmed value. Any conversions after this provide data at the specified accuracy.



**Figure 23. Device Full Powerdown and Powerup Sequence with Device Operation in External Reference Mode**

When an external reference is used, a conversion can be started  $t_{d22}$  ns after asserting  $\overline{PD} = 1$ . The first three conversions are required for internal circuit stabilization. Any conversions after this provide data at the specified accuracy.

**NAP MODE**

The device automatically enters the nap state if  $nap = 1$  at end of a conversion, and it remains in the nap state until the start of the sampling phase. A minimum of 150 ns is required after a sample start for the device to come out of the nap state and to perform normal sampling. So the minimum sampling time needed for nap mode is  $t_{acq(min)} + 150$  ns, or the maximum conversion speed in nap mode is 1.5 MHz.

## LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8410 circuitry. The device offers single-supply operation, and it is often used in close proximity with digital logic, FPGA, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more difficult it is to achieve good performance from the converter.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to the end of sampling and just prior to latching the output of the analog comparator during the conversion phase. Such glitches might originate from switching power supplies, nearby digital logic, or high power devices. Noise during the end of sampling and the later half of a conversion must be kept to a minimum (the former half of a conversion is not very sensitive since the device uses a proprietary error correction algorithm to correct for transient errors during this period).

The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. On average, the device draws very little current from an external reference as the reference voltage is internally buffered. If the reference voltage is external and originates from an op amp, make sure that it can drive the bypass capacitor or capacitors without oscillation. A 0.1- $\mu\text{F}$  bypass capacitor and 1- $\mu\text{F}$  storage capacitor are recommended from REFIN directly to REFM.

The AGND and BDGND pins should be connected to a clean ground point. In all cases, this should be the analog ground. Avoid connections that are too close to the grounding point of a microcontroller or digital signal processor. If required, run a ground trace directly from the converter to the power supply entry point. The ideal layout consists of an analog ground plane dedicated to the converter and associated analog circuitry.

As with the AGND connections, +VA should be connected to a +5-V power supply plane that is separate from the connection for +VBD and digital logic until they are connected at the power entry point onto the PCB. Power to the ADC should be clean and well bypassed. A 0.1- $\mu\text{F}$  ceramic bypass capacitor should be placed as close to the device as possible. See Table 6 for the placement of the capacitor. In addition to the 0.1- $\mu\text{F}$  capacitor, a 1- $\mu\text{F}$  capacitor is recommended. In some situations, additional bypassing may be required, such as a 100- $\mu\text{F}$  electrolytic capacitor or even a Pi filter made up of inductors and capacitors; all designed to essentially low-pass filter the +5-V supply, thus removing the high frequency noise.

**Table 6. Power Supply Decoupling Capacitor Placement**

POWER SUPPLY PLANE	CONVERTER ANALOG SIDE	CONVERTER DIGITAL SIDE
SUPPLY PINS		
Pair of pins require a shortest path to decoupling capacitors	(9,10) (16,17) (20,21) (22,23) (26,27 or 25,26) (36,37)	(44,45)

## TYPICAL CHARACTERISTICS

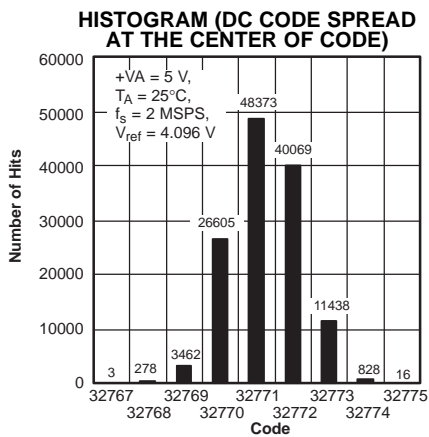


Figure 24.

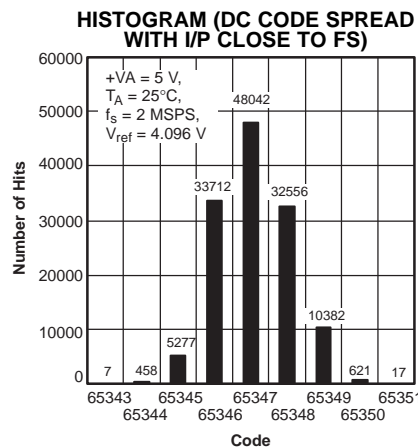


Figure 25.

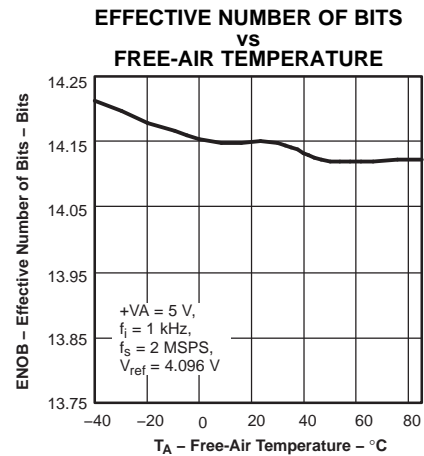


Figure 26.

TYPICAL CHARACTERISTICS (continued)

SIGNAL-TO-NOISE AND DISTORTION  
vs  
FREE-AIR TEMPERATURE

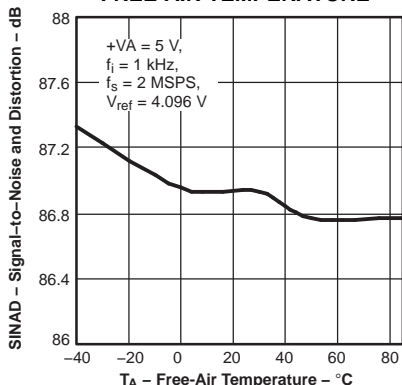


Figure 27.

SIGNAL-TO-NOISE RATIO  
vs  
FREE-AIR TEMPERATURE

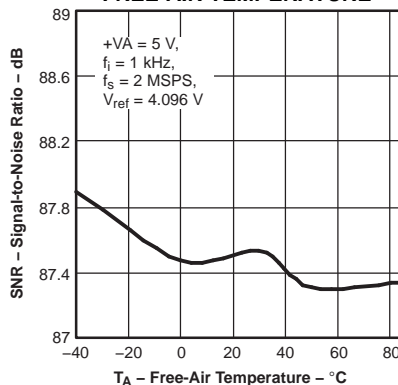


Figure 28.

SPURIOUS FREE DYNAMIC RANGE  
vs  
FREE-AIR TEMPERATURE

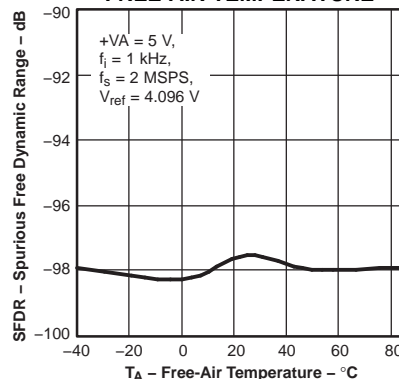


Figure 29.

TOTAL HARMONIC DISTORTION  
vs  
FREE-AIR TEMPERATURE

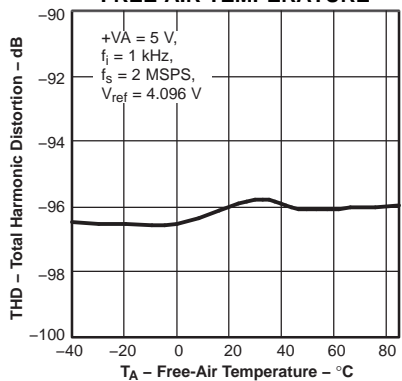


Figure 30.

EFFECTIVE NUMBER OF BITS  
vs  
INPUT FREQUENCY

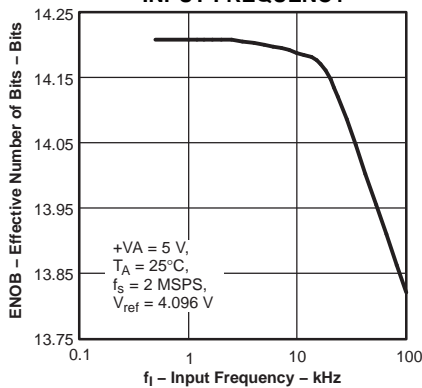


Figure 31.

SIGNAL-TO-NOISE AND DISTORTION  
vs  
INPUT FREQUENCY

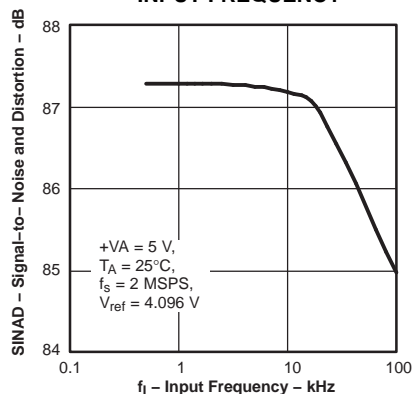


Figure 32.

SIGNAL-TO-NOISE RATIO  
vs  
INPUT FREQUENCY

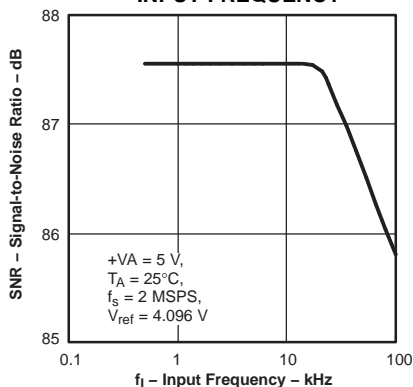


Figure 33.

SPURIOUS FREE DYNAMIC RANGE  
vs  
INPUT FREQUENCY

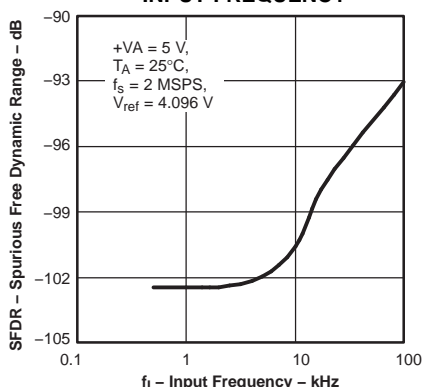


Figure 34.

TOTAL HARMONIC DISTORTION  
vs  
INPUT FREQUENCY

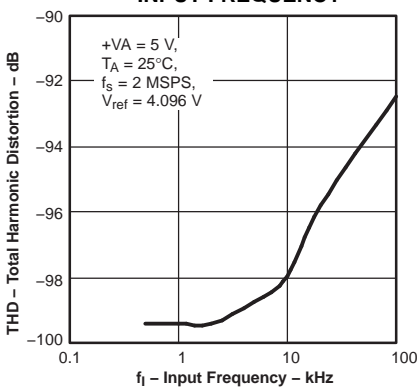


Figure 35.

TYPICAL CHARACTERISTICS (continued)

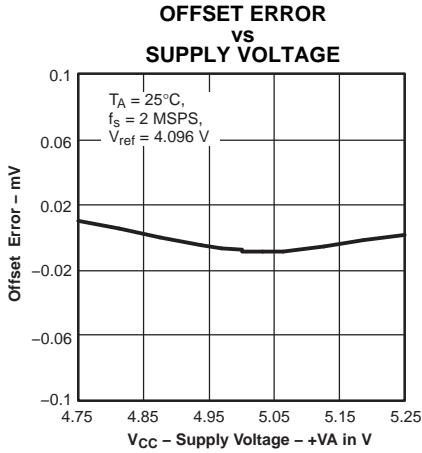


Figure 36.

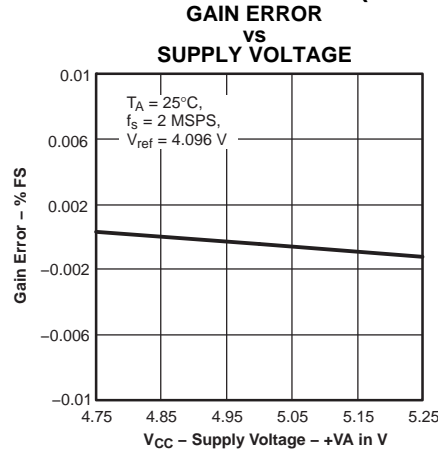


Figure 37.

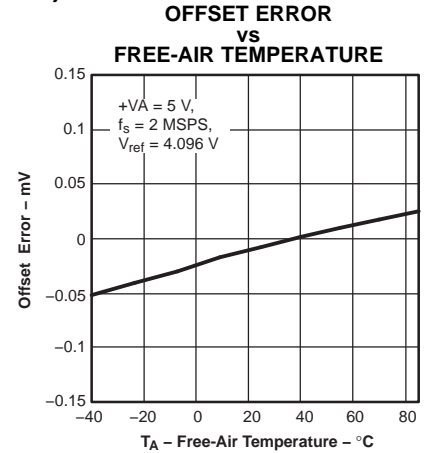


Figure 38.

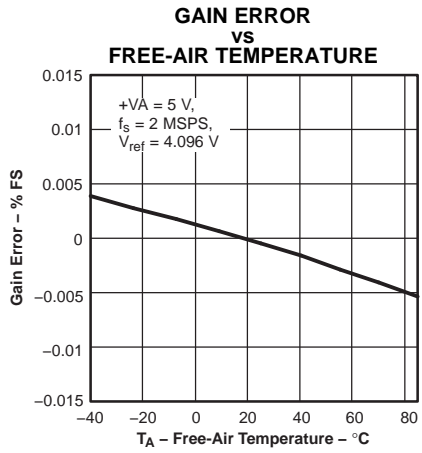


Figure 39.

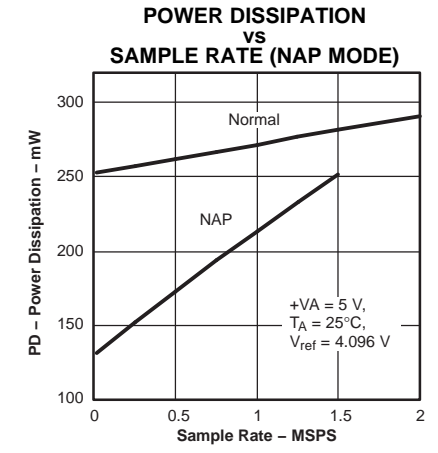


Figure 40.

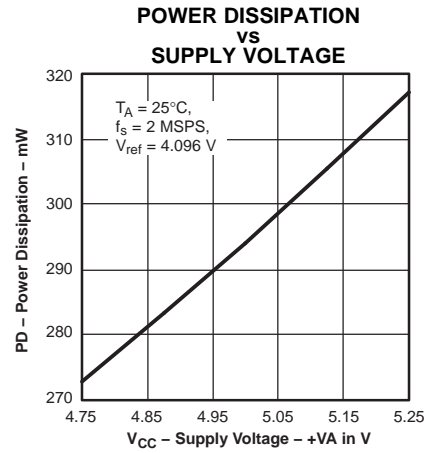


Figure 41.

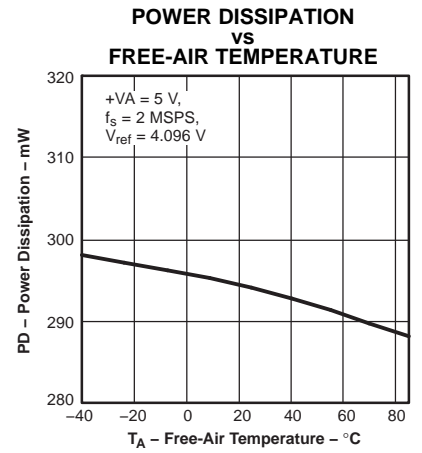


Figure 42.

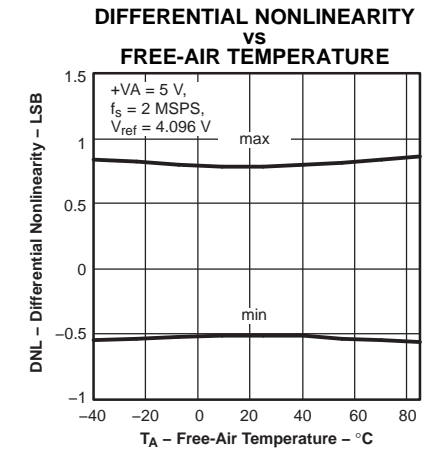


Figure 43.

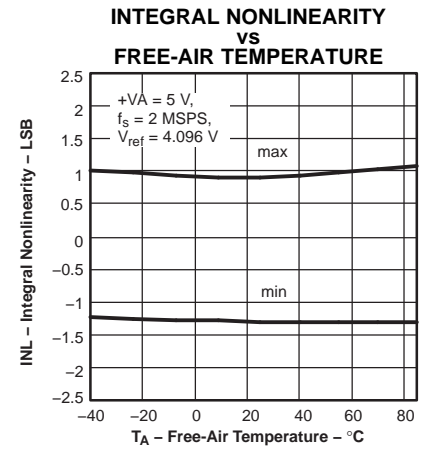


Figure 44.

TYPICAL CHARACTERISTICS (continued)

POSITIVE INTEGRAL NONLINEARITY DISTRIBUTION OVER 25 UNITS

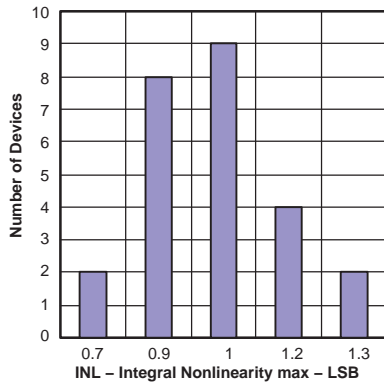


Figure 45.

NEGATIVE INTEGRAL NONLINEARITY DISTRIBUTION OVER 25 UNITS

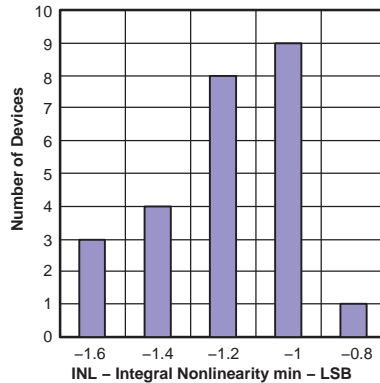


Figure 46.

INTERNAL REFERENCE OUTPUT vs SUPPLY VOLTAGE

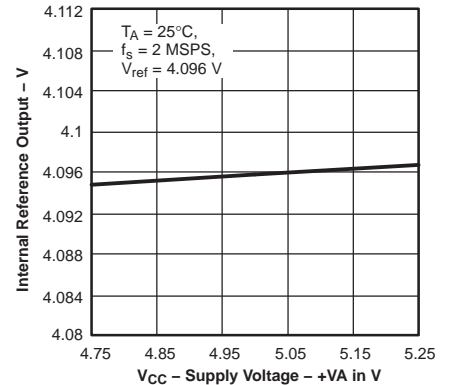


Figure 47.

INTERNAL REFERENCE OUTPUT vs FREE-AIR TEMPERATURE

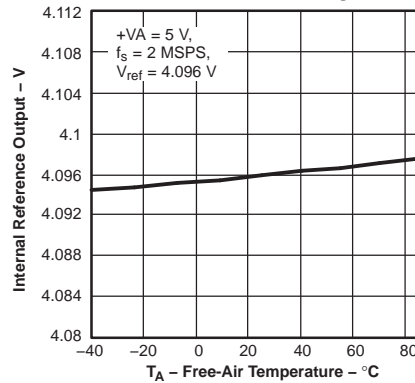


Figure 48.

PARAMETER MEASUREMENT INFORMATION

DRIVER

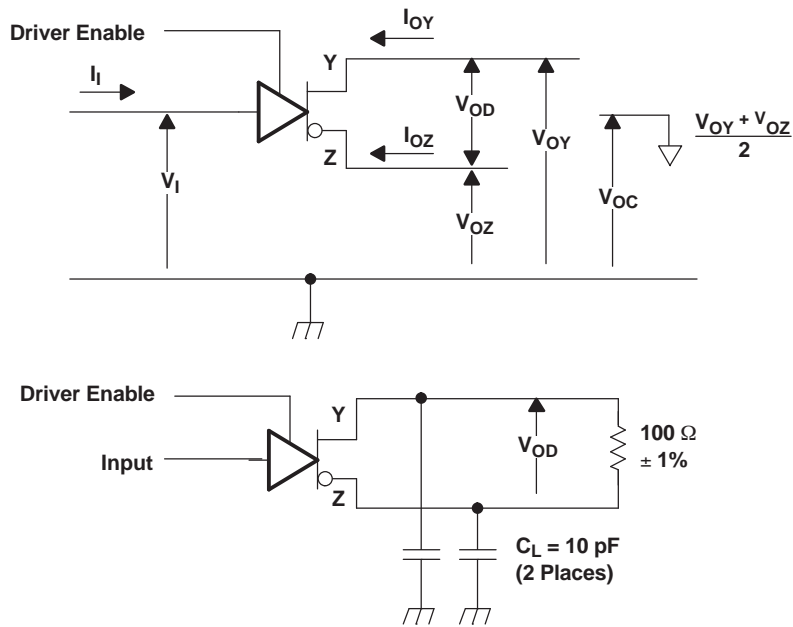


Figure 52. Driver Voltage and Current Definitions

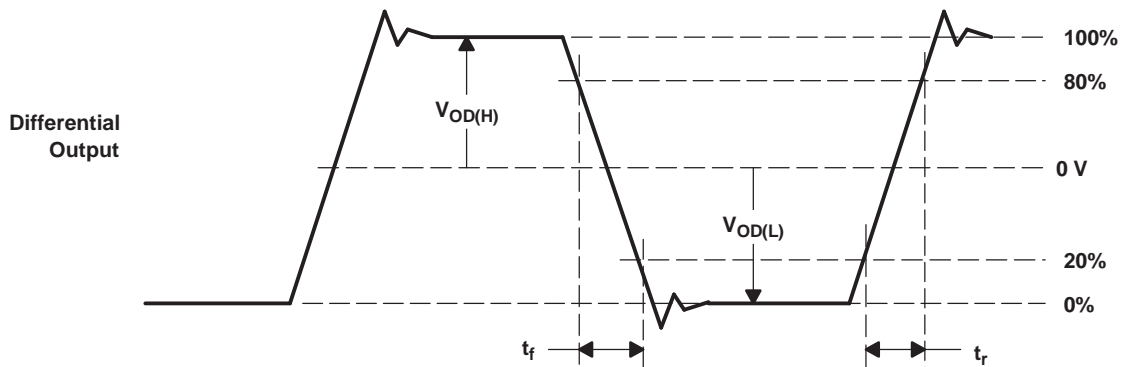


Figure 53. Timing and Voltage Definitions of the Differential Output Signal

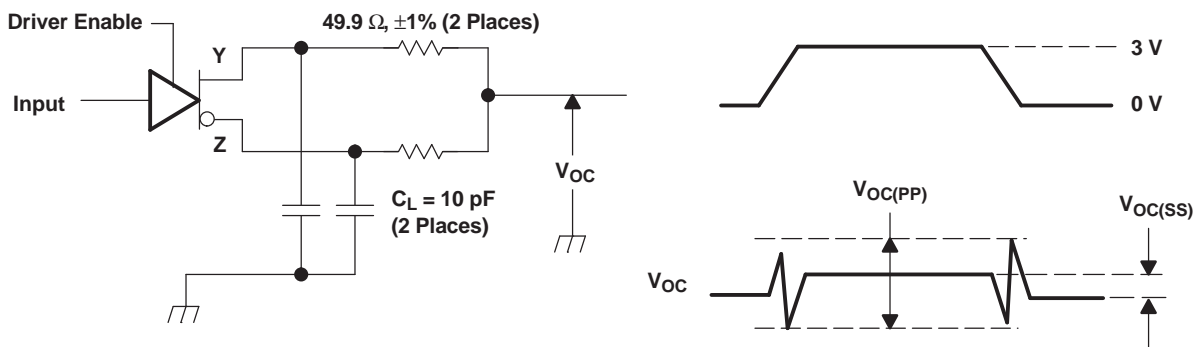


Figure 54. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

PARAMETER MEASUREMENT INFORMATION (continued)

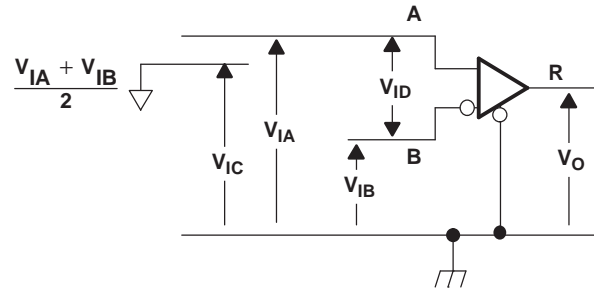


Figure 55. Receiver Voltage Definitions

## REVISION HISTORY

Changes from Original (October 2005) to Revision A	Page
<ul style="list-style-type: none"> <li>• Added min spec for <math>t_{d23}</math> parameter in the <i>Timing Requirements</i> table (used to be max spec for this parameter) .....</li> <li>• Deleted max spec for <math>t_{d23}</math> parameter in the <i>Timing Requirements</i> table (this spec is now the min spec for this parameter) .....</li> </ul>	<p>6</p> <p>6</p>

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8410IRGZT	LIFEBUY	VQFN	RGZ	48	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8410I	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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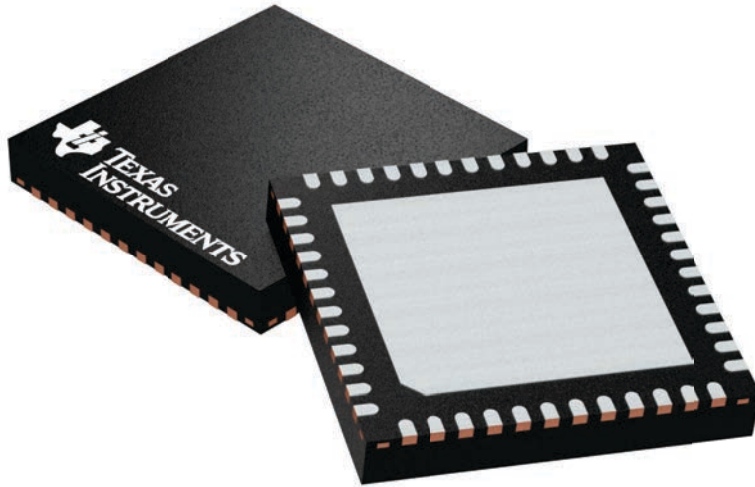
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

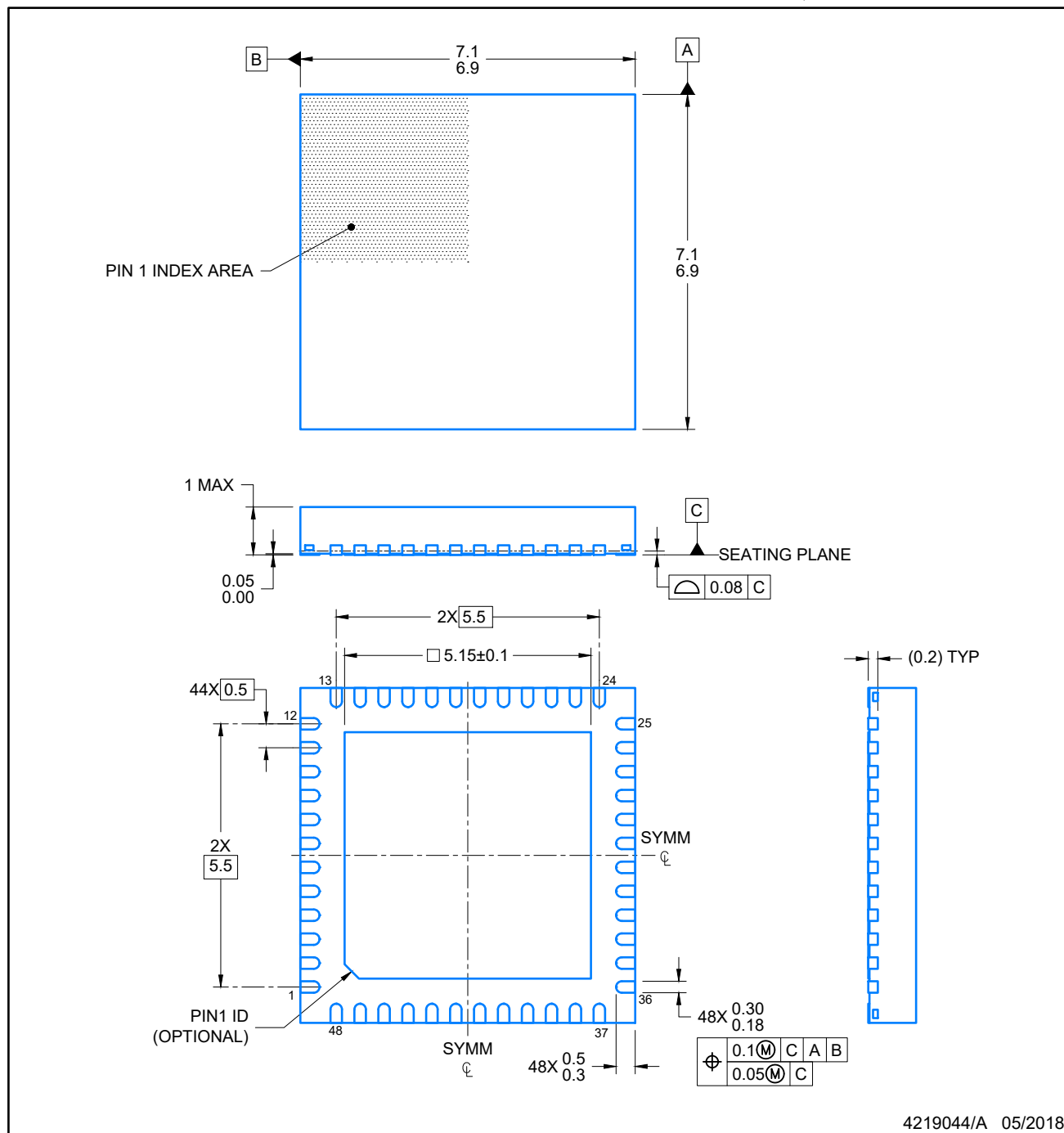
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



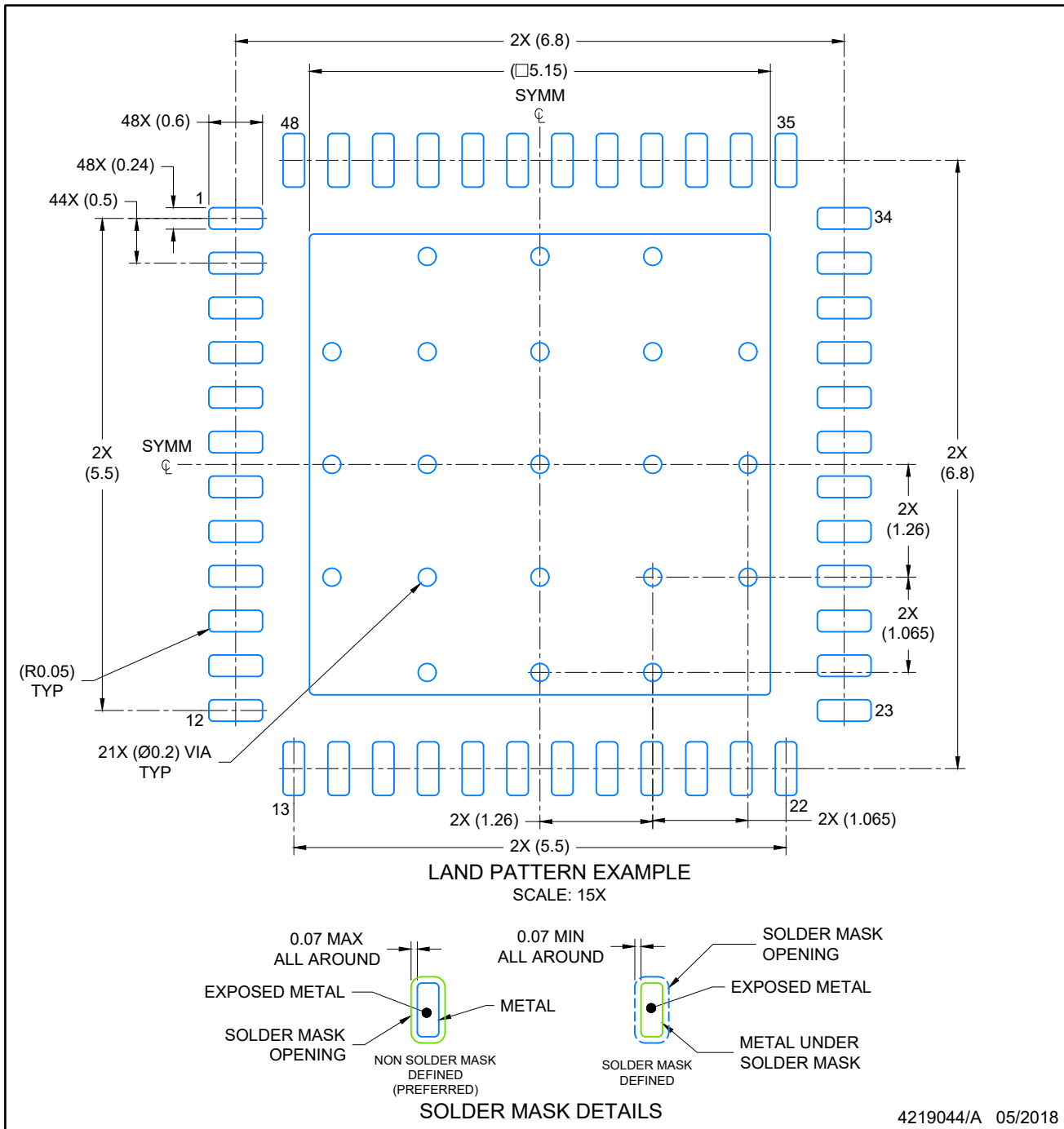
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224671/A



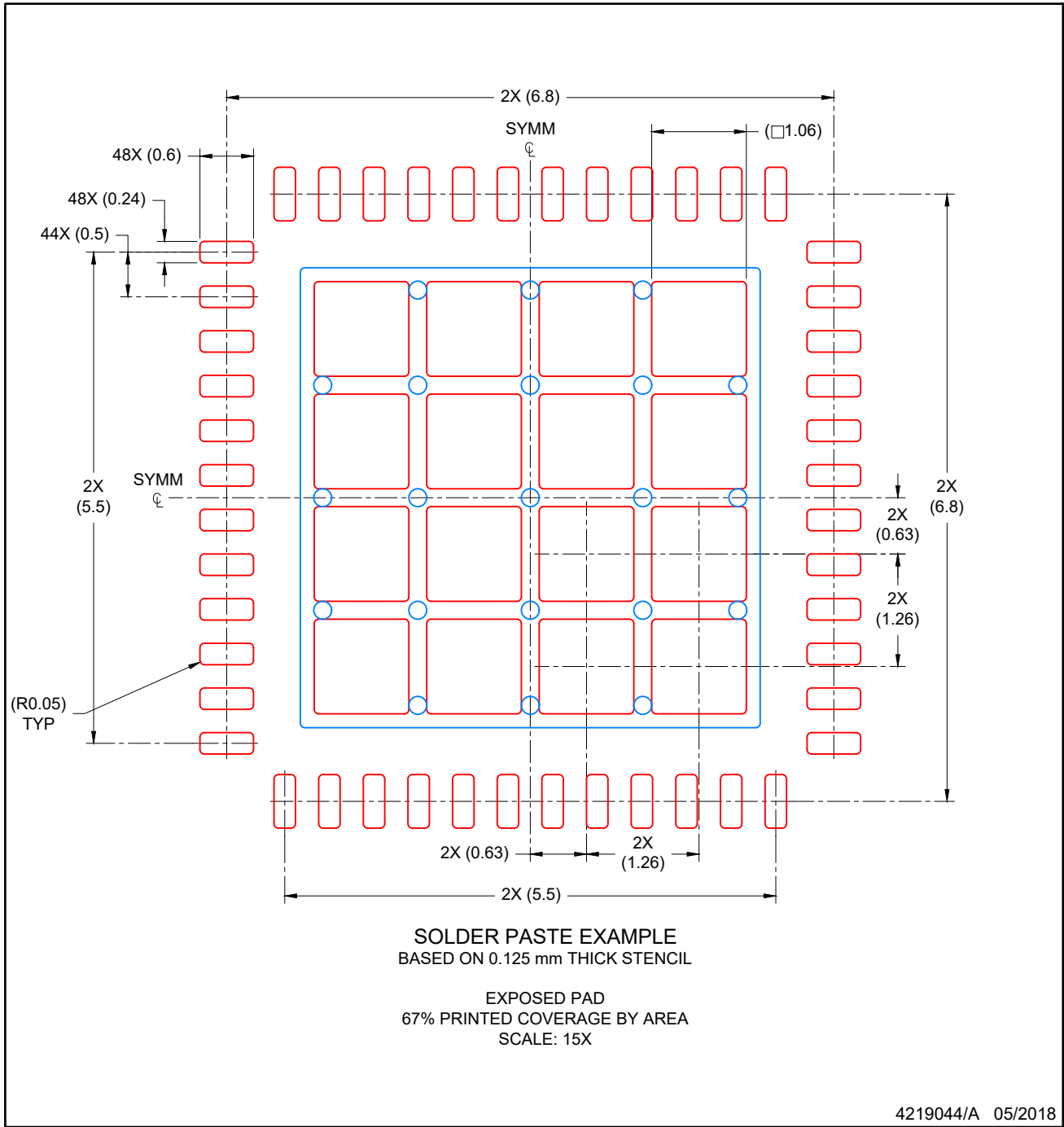
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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