



**THE DATASHEET OF  
ADS7279IRSAT**





## LOW-POWER, 14-BIT, 1MHz, SINGLE/DUAL UNIPOLAR INPUT, ANALOG-TO-DIGITAL CONVERTERS WITH SERIAL INTERFACE

### FEATURES

- 2.7V to 5.5V Analog Supply, Low Power:
  - 13.7mW (1MHz, +VA = 3V, +VBD = 1.8V)
- 1MHz Sampling Rate  $3V \leq +VA \leq 5.5V$ , 900kHz Sampling Rate  $2.7V \leq +VA \leq 3V$
- Excellent DC Performance:
  - $\pm 0.4$ LSB Typ,  $\pm 1.0$ LSB Max INL
  - $\pm 0.4$ LSB Typ,  $\pm 1.0$ LSB Max DNL
  - $\pm 0.8$ mV Max Offset Error at 3V
  - $\pm 1.25$ mV Max Offset Error at 5V
- Excellent AC Performance at  $f_1 = 10$ kHz with 85.9dB SNR, 105.3dB SFDR,  $-100.1$ dB THD
- Built-In Conversion Clock (CCLK)
- 1.65V to 5.5V I/O Supply:
  - SPI™/DSP-Compatible Serial Interface
  - SCLK up to 50MHz
- Comprehensive Power-Down Modes:
  - Deep Power-Down
  - Nap Power-Down
  - Auto Nap Power-Down
- Unipolar Input Range: 0V to  $V_{REF}$
- Software Reset
- Global  $\overline{CONVST}$  (Independent of  $\overline{CS}$ )
- Programmable Status/Polarity EOC/ $\overline{INT}$
- 4 × 4 QFN-16 and TSSOP-16 Packages
- Multi-Chip Daisy-Chain Mode
- Programmable TAG Bit Output
- Auto/Manual Channel Select Mode (ADS7280)

### APPLICATIONS

- Communications
- Transducer Interface
- Medical Instruments
- Magnetometers
- Industrial Process Control
- Data Acquisition Systems
- Automatic Test Equipment

### DESCRIPTION

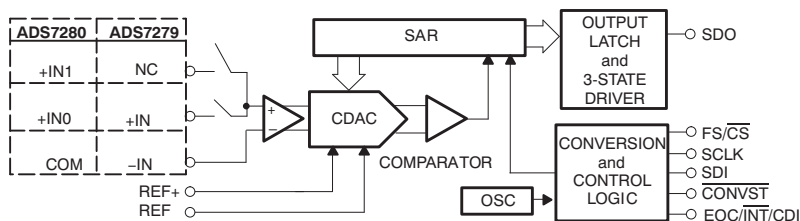
The ADS7279 is a low-power, 14-bit, 1MSPS analog-to-digital converter (ADC) with a unipolar input. The device includes a 14-bit, capacitor-based successive approximation register (SAR) ADC with inherent sample-and-hold.

The ADS7280 is based on the same core and includes a 2-to-1 input MUX with a programmable TAG bit output option. Both the ADS7279 and ADS7280 offer a high-speed, wide voltage serial interface, and are capable of daisy-chain mode operation when multiple converters are used.

These converters are available in 4 × 4 QFN and TSSOP-16 packages, and are fully specified for operation over the industrial  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range.

#### Low Power, High-Speed SAR Converter Family

Type/Speed		500 kSPS	1 MSPS
16-bit single-ended	Single	ADS8327	ADS8329
	Dual	ADS8328	ADS8330
14-bit single-ended	Single		ADS7279
	Dual		ADS7280
12-bit single-ended	Single		ADS7229
	Dual		ADS7230



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### ORDERING INFORMATION<sup>(1)</sup>

MODEL	MAXIMUM INTEGRAL LINEARITY (LSB)	MAXIMUM DIFFERENTIAL LINEARITY (LSB)	MAXIMUM OFFSET ERROR (mV)	PACKAGE TYPE	PACKAGE DESIGNATOR	TEMPERATURE RANGE	ORDERING INFORMATION	TRANSPORT MEDIA, QUANTITY
ADS7279I	±1	±1	±1.25	4 × 4 QFN-16	RSA	–40°C to +85°C	ADS7279IRSAT	Small tape and reel, 250
				TSSOP-16	PW		ADS7279IRSAR	Tape and reel, 3000
							ADS7279IPW	Tube, 90
ADS7280I	±1	±1	±1.25	4 × 4 QFN-16	RSA	–40°C to +85°C	ADS7280IRSAT	Small tape and reel, 250
				TSSOP-16	PW		ADS7280IRSAR	Tape and reel, 3000
							ADS7280IPW	Tube, 90
							ADS7280IPWR	Tape and reel, 2000

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range, unless otherwise noted.

		ADS7279, ADS7280	UNIT
Voltage	+IN to AGND	–0.3 to +VA + 0.3	V
	–IN to AGND	–0.3 to +VA + 0.3	V
Voltage range	+VA to AGND	–0.3 to 7	V
	+REF to AGND	–0.3 to +VA + 0.3	V
	–REF to AGND	–0.3 to 0.3	V
	+VBD to BDGND	–0.3 to 7	V
	AGND to BDGND	–0.3 to 0.3	V
Digital input voltage to BDGND		–0.3 to +VBD + 0.3	V
Digital output voltage to BDGND		–0.3 to +VBD + 0.3	V
T <sub>A</sub>	Operating free-air temperature range	–40 to +85	°C
T <sub>stg</sub>	Storage temperature range	–65 to +150	°C
T <sub>J</sub> max	Junction temperature	+150	°C
4 × 4 QFN-16 package	Power dissipation	(T <sub>J</sub> max – T <sub>A</sub> )/θ <sub>JA</sub>	
	θ <sub>JA</sub> thermal impedance	47	°C/W
TSSOP-16 package	Power dissipation	(T <sub>J</sub> max – T <sub>A</sub> )/θ <sub>JA</sub>	
	θ <sub>JA</sub> thermal impedance	86	°C/W

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $+VA = 4.5\text{V}$  to  $5.5\text{V}$ ,  $+VBD = +1.65\text{V}$  to  $+5.5\text{V}$ ,  $V_{REF} = 5\text{V}$ , and  $f_{SAMPLE} = 1\text{MHz}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7279, ADS7280			UNIT
			MIN	TYP	MAX	
<b>ANALOG INPUT</b>						
FSR	Full-scale input voltage <sup>(1)</sup>	+IN – (–IN) or (+INx – COM)	0		$V_{REF}$	V
	Absolute input voltage	+IN, +IN0, +IN1	AGND – 0.2		+VA + 0.2	V
		–IN or COM	AGND – 0.2		AGND + 0.2	
	Input capacitance				45	pF
	Input leakage current	No ongoing conversion, dc input		50		nA
	Input channel isolation, ADS7280 only	At dc		109		dB
		$V_I = \pm 1.25V_{PP}$ at 50kHz		101		
<b>SYSTEM PERFORMANCE</b>						
	Resolution			14		Bits
NMC	No missing codes		14			Bits
INL	Integral linearity		–1	$\pm 0.4$	1	LSB <sup>(2)</sup>
DNL	Differential linearity		–1	$\pm 0.4$	1	LSB <sup>(2)</sup>
$E_O$	Offset error <sup>(3)</sup>		–1.25	$\pm 0.3$	1.25	mV
	Offset error drift	FSR = 5V		$\pm 0.2$		ppm/ $^\circ\text{C}$
$E_G$	Gain error		–0.25	$\pm 0.05$	0.25	%FSR
	Gain error drift			$\pm 0.5$		ppm/ $^\circ\text{C}$
CMRR	Common-mode rejection ratio	At dc		70		dB
		$V_I = 0.4V_{PP}$ at 1MHz		50		
	Noise			33		$\mu\text{V}_{RMS}$
PSRR	Power-supply rejection ratio	At FFFFh output code <sup>(3)</sup>		78		dB
<b>SAMPLING DYNAMICS</b>						
$t_{CONV}$	Conversion time			18		CCLK
$t_{SAMPLE1}$	Acquisition time	Manual trigger		3		CCLK
		Auto trigger		3		
$t_{SAMPLE2}$	Throughput rate				1	MHz
	Aperture delay			5		ns
	Aperture jitter			10		ps
	Step response			100		ns
	Overvoltage recovery			100		ns

(1) Ideal input span; does not include gain or offset error.

(2) LSB means least significant bit.

(3) Measured relative to an ideal full-scale input [(+IN) – (–IN)] of 4.096V when +VA = 5V.

**ELECTRICAL CHARACTERISTICS (continued)**

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $+VA = 4.5\text{V}$  to  $5.5\text{V}$ ,  $+VBD = +1.65\text{V}$  to  $+5.5\text{V}$ ,  $V_{REF} = 5\text{V}$ , and  $f_{SAMPLE} = 1\text{MHz}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7279, ADS7280			UNIT
			MIN	TYP	MAX	
<b>DYNAMIC CHARACTERISTICS</b>						
THD	Total harmonic distortion <sup>(4)</sup>	$V_{IN} = 5V_{PP}$ at 10kHz	-100.1			dB
		$V_{IN} = 5V_{PP}$ at 100kHz	-89.1			
SNR	Signal-to-noise ratio	$V_{IN} = 5V_{PP}$ at 10kHz	85.9			dB
		$V_{IN} = 5V_{PP}$ at 100kHz	81.0	84.3		
SINAD	Signal-to-noise + distortion	$V_{IN} = 5V_{PP}$ at 10kHz	85.7			dB
		$V_{IN} = 5V_{PP}$ at 100kHz	82.7			
SFDR	Spurious-free dynamic range	$V_{IN} = 5V_{PP}$ at 10kHz	105.3			dB
		$V_{IN} = 5V_{PP}$ at 100kHz	91.3			
	-3dB small-signal bandwidth		30			MHz
<b>CLOCK</b>						
	Internal conversion clock frequency		21	23	24.5	MHz
	SCLK external serial clock	Used as I/O clock only	50			MHz
		As I/O clock and conversion clock	1	42		
<b>EXTERNAL VOLTAGE REFERENCE INPUT</b>						
$V_{REF}$	Input reference range	$V_{REF}[\text{REF+} - (\text{REF-})]$	0.3	+VA		V
		$(\text{REF-}) - \text{AGND}$	-0.1	0.1		
	Resistance <sup>(5)</sup>	Reference input	40			k $\Omega$
<b>DIGITAL INPUT/OUTPUT</b>						
	Logic family—CMOS					
$V_{IH}$	High-level input voltage	$5.5\text{V} \geq +VBD \geq 4.5\text{V}$	$0.65 \times (+VBD)$	$+VBD + 0.3$		V
$V_{IL}$	Low-level input voltage	$5.5\text{V} \geq +VBD \geq 4.5\text{V}$	-0.3	$0.35 \times (+VBD)$		V
$I_i$	Input current	$V_i = +VBD$ or $\text{BDGND}$	-50	50		nA
$C_i$	Input capacitance		5			pF
$V_{OH}$	High-level output voltage	$5.5\text{V} \geq +VBD \geq 4.5\text{V}$ , $I_O = 100\mu\text{A}$	$+VBD - 0.6$	$+VBD$		V
$V_{OL}$	Low-level output voltage	$5.5\text{V} \geq +VBD \geq 4.5\text{V}$ , $I_O = 100\mu\text{A}$	0	0.4		V
$C_O$	Output capacitance		5			pF
$C_L$	Load capacitance		30			pF
	Data format—straight binary					
<b>POWER-SUPPLY REQUIREMENTS</b>						
Power-supply voltage	+VBD		1.65	3.3	5.5	V
	+VA		4.5	5	5.5	V
Supply current	1MHz Sample rate		5.7		7.0	mA
	Nap or Auto Nap mode		0.3		0.5	
	Deep power-down mode		0.004		1	$\mu\text{A}$
Buffer I/O supply current	1MSPS, $\text{BVDD} = 1.8\text{V}$		0.1		0.5	mA
	1MSPS, $\text{BVDD} = 3\text{V}$		0.5		1.2	
Power dissipation	$\text{AVDD} = 5\text{V}$ , $\text{BVDD} = 1.8\text{V}$		28.7		35.9	mW
	$\text{AVDD} = 5\text{V}$ , $\text{BVDD} = 3\text{V}$		30.0		38.6	
<b>TEMPERATURE RANGE</b>						
$T_A$	Operating free-air temperature		-40	+85		$^\circ\text{C}$

(4) Calculated on the first nine harmonics of the input frequency.

(5) Can vary  $\pm 30\%$ .

## ELECTRICAL CHARACTERISTICS

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $+VA = 2.7\text{V}$  to  $3.6\text{V}$ ,  $+VBD = 1.65\text{V}$  to  $1.5x(+VA)$ ,  $V_{REF} = 2.5\text{V}$ ,  $f_{SAMPLE} = 1\text{MHz}$  for  $3\text{V} \leq +VA \leq 3.6\text{V}$ , and  $f_{SAMPLE} = 900\text{kHz}$  for  $3\text{V} < +VA \leq 2.7\text{V}$  using external clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7279, ADS7280			UNIT
			MIN	TYP	MAX	
<b>ANALOG INPUT</b>						
FSR	Full-scale input voltage <sup>(1)</sup>	+IN – (–IN) or (+INx – COM)	0		$V_{REF}$	V
	Absolute input voltage	+IN, +IN0, +IN1	AGND – 0.2		+VA + 0.2	V
		–IN or COM	AGND – 0.2		AGND + 0.2	
	Input capacitance				45	pF
	Input leakage current	No ongoing conversion, dc Input		50		nA
	Input channel isolation, ADS7280 only	At dc		108		dB
		$V_{IN} = \pm 1.25V_{PP}$ at 50kHz		101		
<b>SYSTEM PERFORMANCE</b>						
	Resolution			14		Bits
	No missing codes		14			Bits
INL	Integral linearity		–1	$\pm 0.4$	1	LSB <sup>(2)</sup>
DNL	Differential linearity		–1	$\pm 0.4$	1	LSB <sup>(2)</sup>
$E_O$	Offset error <sup>(3)</sup>		–0.8	$\pm 0.05$	0.8	mV
	Offset error drift	FSR = 2.5V		$\pm 0.1$		ppm/ $^\circ\text{C}$
$E_G$	Gain error		–0.25	$\pm 0.06$	0.25	%FSR
	Gain error drift			$\pm 0.5$		ppm/ $^\circ\text{C}$
CMRR	Common-mode rejection ratio	At dc		70		dB
		$V_{IN} = 0.4V_{PP}$ at 1MHz		50		
	Noise			33		$\mu V_{RMS}$
PSRR	Power-supply rejection ratio	At FFFFh output code <sup>(3)</sup>		78		dB
<b>SAMPLING DYNAMICS</b>						
$t_{CONV}$	Conversion time			18		CCLK
$t_{SAMPLE1}$	Acquisition time	Manual trigger		3		CCLK
		Auto trigger		3		
$t_{SAMPLE2}$	Throughput rate	$2.7\text{V} \leq +VA < 3.0\text{V}$			0.9	MHz
		$3.0\text{V} \leq +VA < 3.64\text{V}$			1	
	Aperture delay			5		ns
	Aperture jitter			10		ps
	Step response			100		ns
	Overvoltage recovery			100		ns

(1) Ideal input span; does not include gain or offset error.

(2) LSB means least significant bit.

(3) Measured relative to an ideal full-scale input [(+IN) – (–IN)] of 2.5V when  $+VA = 3\text{V}$ .

**ELECTRICAL CHARACTERISTICS (continued)**

At  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $+VA = 2.7\text{V}$  to  $3.6\text{V}$ ,  $+VBD = 1.65\text{V}$  to  $1.5 \times (+VA)$ ,  $V_{REF} = 2.5\text{V}$ ,  $f_{SAMPLE} = 1\text{MHz}$  for  $3\text{V} \leq +VA \leq 3.6\text{V}$ , and  $f_{SAMPLE} = 900\text{kHz}$  for  $3\text{V} < +VA \leq 2.7\text{V}$  using external clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7279, ADS7280			UNIT
			MIN	TYP	MAX	
<b>DYNAMIC CHARACTERISTICS</b>						
THD	Total harmonic distortion <sup>(4)</sup>	$V_{IN} = 2.5V_{PP}$ at 10kHz	-100.8			dB
		$V_{IN} = 2.5V_{PP}$ at 100kHz	-88.4			
SNR	Signal-to-noise ratio	$V_{IN} = 2.5V_{PP}$ at 10kHz	81	83.1	dB	
		$V_{IN} = 2.5V_{PP}$ at 100kHz	82			
SINAD	Signal-to-noise + distortion	$V_{IN} = 2.5V_{PP}$ at 10kHz	83			dB
		$V_{IN} = 2.5V_{PP}$ at 100kHz	81.4			
SFDR	Spurious-free dynamic range	$V_{IN} = 2.5V_{PP}$ at 10kHz	102.6			dB
		$V_{IN} = 2.5V_{PP}$ at 100kHz	89.8			
-3dB small-signal bandwidth			30			MHz
<b>CLOCK</b>						
Internal conversion clock frequency			21	22	23.5	MHz
SCLK external serial clock		Used as I/O clock only	42			MHz
		As I/O clock and conversion clock	1	42		
<b>EXTERNAL VOLTAGE REFERENCE INPUT</b>						
$V_{REF}$	Input reference range	$V_{REF} [\text{REF+} - (\text{REF-})]$	$f_{SAMPLE} \leq 500\text{kSPS}$ , $2.7\text{V} \leq +VA < 3\text{V}$	0.3	2.525	V
			$f_{SAMPLE} \leq 500\text{kSPS}$ , $3\text{V} \leq +VA < 3.6\text{V}$	0.3	3	
			$f_{SAMPLE} > 500\text{kSPS}$ , $2.7\text{V} \leq +VA < 3\text{V}$	2.475	2.525	
			$f_{SAMPLE} > 500\text{kSPS}$ , $3\text{V} \leq +VA < 3.6\text{V}$	2.475	3	
		$(\text{REF-}) - \text{AGND}$		-0.1	0.1	
Resistance <sup>(5)</sup>		Reference input	40			k $\Omega$
<b>DIGITAL INPUT/OUTPUT</b>						
Logic family—CMOS						
$V_{IH}$	High-level input voltage	$(+VA \times 1.5)\text{V} \geq +VBD \geq 1.65\text{V}$	$0.65 \times (+VBD)$	$+VBD + 0.3$		V
$V_{IL}$	Low-level input voltage	$(+VA \times 1.5)\text{V} \geq +VBD \geq 1.65\text{V}$	-0.3	$0.35 \times (+VBD)$		V
$I_I$	Input current	$V_I = +VBD$ or $\text{BDGND}$	-50	50		nA
$C_I$	Input capacitance		5			pF
$V_{OH}$	High-level output voltage	$(+VA \times 1.5)\text{V} \geq +VBD \geq 1.65\text{V}$ , $I_O = 100\mu\text{A}$	$+VBD - 0.6$	$+VBD$		V
$V_{OL}$	Low-level output voltage	$(+VA \times 1.5)\text{V} \geq +VBD \geq 1.65\text{V}$ , $I_O = 100\mu\text{A}$	0	0.4		V
$C_O$	Output capacitance		5			pF
$C_L$	Load capacitance		30			pF
Data format—straight binary						

(4) Calculated on the first nine harmonics of the input frequency.

(5) Can vary  $\pm 30\%$ .

**ELECTRICAL CHARACTERISTICS (continued)**

At  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $+VA = 2.7\text{V}$  to  $3.6\text{V}$ ,  $+VBD = 1.65\text{V}$  to  $1.5 \times (+VA)$ ,  $V_{\text{REF}} = 2.5\text{V}$ ,  $f_{\text{SAMPLE}} = 1\text{MHz}$  for  $3\text{V} \leq +VA \leq 3.6\text{V}$ , and  $f_{\text{SAMPLE}} = 900\text{kHz}$  for  $3\text{V} < +VA \leq 2.7\text{V}$  using external clock, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS7279, ADS7280			UNIT
			MIN	TYP	MAX	
<b>POWER-SUPPLY REQUIREMENTS</b>						
Power-supply voltage	+VBD		1.65	+VA	$1.5 \times (+VA)$	V
	+VA	$f_s \leq 1\text{MHz}$	3		3.6	V
		$f_s \leq 900\text{kHz}$	2.7		3.6	
Supply current	1MHz sample rate, $3\text{V} \leq +VA \leq 3.6\text{V}$			4.5	6.0	mA
	900kHz sample rate, $2.7\text{V} \leq +VA \leq 3\text{V}$			4.2		
	Nap or Auto Nap mode			0.25	0.4	
	Deep power-down mode			0.001	1	$\mu\text{A}$
Buffer I/O supply current	1MSPS, BVDD = 1.8V			0.1	0.5	mA
	1MSPS, BVDD = 3V			0.5	1.2	
Power dissipation	AVDD = 3V, BVDD = 1.8V			13.7	18.9	mW
	AVDD = 3V, BVDD = 3V			15.0	21.6	
<b>TEMPERATURE RANGE</b>						
$T_A$	Operating free-air temperature			-40	+85	$^{\circ}\text{C}$

### TIMING CHARACTERISTICS<sup>(1)(2)</sup>: 5V

All specifications typical at –40°C to +85°C and +VA = +VBD = 5V, unless otherwise noted.

PARAMETER			ADS7279, ADS7280			UNIT
			MIN	TYP	MAX	
f <sub>CCLK</sub>	Frequency, conversion clock, CCLK	External, f <sub>CCLK</sub> = 1/2 f <sub>SCLK</sub>	0.5		21	MHz
		Internal, f <sub>CCLK</sub> = 1/2 f <sub>SCLK</sub>	21	23	24.5	
t <sub>1</sub>	Setup time, falling edge of $\overline{CS}$ to EOC		1			CCLK
t <sub>2</sub>	Hold time, falling edge of $\overline{CS}$ to EOC		0			ns
t <sub>CL</sub>	Pulse duration, $\overline{CONVST}$ low		40			ns
t <sub>3</sub>	Hold time, falling edge of $\overline{CS}$ to EOS		20			ns
t <sub>4</sub>	Setup time, rising edge of $\overline{CS}$ to EOS		20			ns
t <sub>5</sub>	Hold time, rising edge of $\overline{CS}$ to EOS		20			ns
t <sub>6</sub>	Setup time, falling edge of $\overline{CS}$ to first falling SCLK		5			ns
t <sub>SCLKL</sub>	Pulse duration, SCLK low		8		t <sub>SCLK</sub> – 8	ns
t <sub>SCLKH</sub>	Pulse duration, SCLK high		8		t <sub>SCLK</sub> – 8	ns
t <sub>SCLK</sub>	Cycle time, SCLK	I/O clock only	20			ns
		I/O and conversion clock	23.8		2000	
		I/O clock, chain mode	20			
		I/O and conversion clock, chain mode	23.8		2000	
t <sub>H2</sub>	Hold time, falling edge of SCLK to SDO invalid	10pF load	2			ns
t <sub>D1</sub>	Delay time, falling edge of SCLK to SDO valid	10pF load			10	ns
t <sub>D2</sub>	Delay time, falling edge of $\overline{CS}$ to SDO valid, SDO MSB output	10pF load			8.5	ns
t <sub>S1</sub>	Setup time, SDI to falling edge of SCLK		8			ns
t <sub>H1</sub>	Hold time, SDI to falling edge of SCLK		4			ns
t <sub>D3</sub>	Delay time, rising edge of $\overline{CS}/FS$ to SDO t <sub>D3</sub> 3-state				5	ns
t <sub>7</sub>	Setup time, 16th falling edge of SCLK before rising edge of $\overline{CS}/FS$		10			ns

- (1) All input signals are specified with t<sub>r</sub> = t<sub>f</sub> = 1.5ns (10% to 90% of VBD) and timed from a voltage level of (V<sub>IL</sub> + V<sub>IH</sub>)/2.  
(2) See timing diagrams.

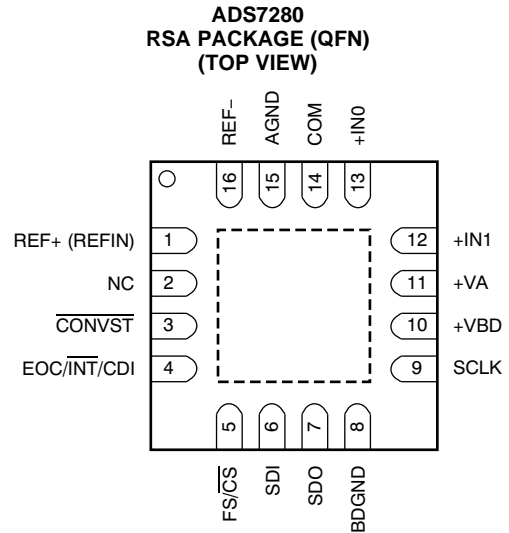
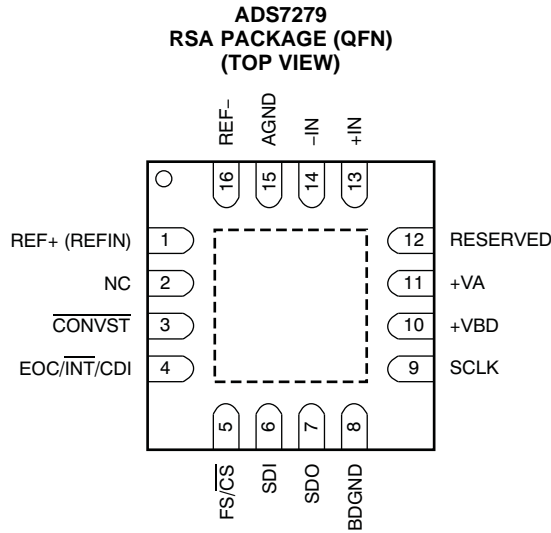
**TIMING CHARACTERISTICS<sup>(1)(2)</sup> : 1.8V**

 All specifications typical at  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ ,  $+V_A = 2.7\text{ V}$ , and  $+V_{BD} = 1.8\text{V}$ , unless otherwise noted.

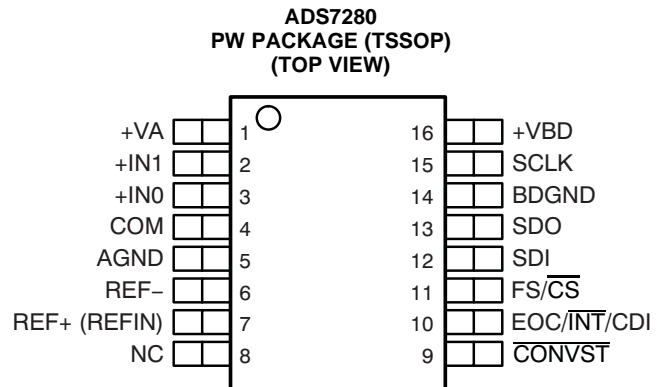
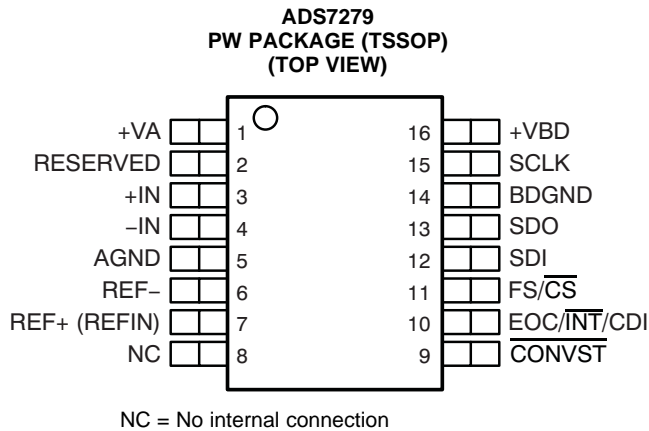
PARAMETER		ADS7279, ADS7280			UNIT	
		MIN	TYP	MAX		
$f_{\text{CCLK}}$	Frequency, conversion clock, CCLK	External, $3\text{V} \leq +V_A \leq 3.6\text{V}$ , $f_{\text{CCLK}} = 1/2 f_{\text{SCLK}}$	0.5		21	MHz
		External, $2.7\text{V} \leq +V_A \leq 3\text{V}$ , $f_{\text{CCLK}} = 1/2 f_{\text{SCLK}}$	0.5		18.9	
		Internal, $f_{\text{CCLK}} = 1/2 f_{\text{SCLK}}$	20	22	23.5	
$t_1$	Setup time, falling edge of $\overline{\text{CS}}$ to EOC		1			CCLK
$t_2$	Hold time, falling edge of $\overline{\text{CS}}$ to EOC		0			ns
$t_{\text{CL}}$	Pulse duration, $\overline{\text{CONVST}}$ low		40			ns
$t_3$	Hold time, falling edge of $\overline{\text{CS}}$ to EOS		20			ns
$t_4$	Setup time, rising edge of $\overline{\text{CS}}$ to EOS		20			ns
$t_5$	Hold time, rising edge of $\overline{\text{CS}}$ to EOS		20			ns
$t_6$	Setup time, falling edge of $\overline{\text{CS}}$ to first $t_6$ falling SCLK		5			ns
$t_{\text{SCLKL}}$	Pulse duration, SCLK low		8	$t_{\text{SCLK}} - 8$		ns
$t_{\text{SCLKH}}$	Pulse duration, SCLK high		8	$t_{\text{SCLK}} - 8$		ns
$t_{\text{SCLK}}$	Cycle time, SCLK	All modes, $3\text{V} \leq +V_A \leq 3.6\text{V}$	23.8		2000	ns
		All modes, $2.7\text{V} \leq +V_A < 3\text{V}$	26.5		2000	
$t_{\text{H2}}$	Hold time, falling edge of SCLK to SDO invalid	10pF load	7.5			ns
$t_{\text{D1}}$	Delay time, falling edge of SCLK to SDO valid	10pF load			16	ns
$t_{\text{D2}}$	Delay time, falling edge of $\overline{\text{CS}}$ to SDO valid, SDO MSB output	10pF load, $2.7\text{V} \leq +V_A \leq 3\text{V}$			13	ns
		10pF load, $3\text{V} \leq +V_A \leq 3.6\text{V}$			11	
$t_{\text{S1}}$	Setup time, SDI to falling edge of SCLK		8			ns
$t_{\text{H1}}$	Hold time, SDI to falling edge of SCLK		4			ns
$t_{\text{D3}}$	Delay time, rising edge of $\overline{\text{CS}}/\text{FS}$ to SDO 3-state				8	ns
$t_7$	Setup time, 16th falling edge of SCLK $t_7$ before rising edge of $\overline{\text{CS}}/\text{FS}$		10			ns

- (1) All input signals are specified with  $t_r = t_f = 1.5\text{ns}$  (10% to 90% of VBD) and timed from a voltage level of  $(V_{\text{IL}} + V_{\text{IH}})/2$ .  
 (2) See timing diagrams.

PIN ASSIGNMENTS



**CAUTION:** The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.



**ADS7279 Terminal Functions**

NAME	NO.		I/O	DESCRIPTION
	QFN	TSSOP		
AGND	15	5	—	Analog ground
BDGND	8	14	—	Interface ground
CONVST	3	9	I	Freezes sample-and-hold, starts conversion with next rising edge of internal clock
EOC/ $\overline{\text{INT}}$ / CDI	4	10	I/O	Status output. If programmed as EOC, this pin is low (default) when a conversion is in progress. If programmed as an interrupt (INT), this pin is low for a preprogrammed duration after the end of conversion and valid data are to be output. The polarity of EOC or INT is programmable. This pin can also be used as a chain data input when the device is operated in daisy-chain mode.
FS/ $\overline{\text{CS}}$	5	11	I	Frame sync signal for TMS320 DSP serial interface or chip select input for SPI interface slave select (SS–).
+IN	13	3	I	Noninverting input
–IN	14	4	I	Inverting input; usually connected to ground
NC	2	8	—	No connection
REF+ (REFIN)	1	7	I	External reference input
REF–	16	6	I	Connect to AGND through individual via
RESERVED	12	2	I	Connect to AGND or +VA
SCLK	9	15	I	Clock for serial interface
SDI	6	12	I	Serial data in
SDO	7	13	O	Serial data out
+VA	11	1		Analog supply, +2.7V to +5.5VDC
+VBD	10	16		Interface supply

**ADS7280 Terminal Functions**

NAME	NO.		I/O	DESCRIPTION
	QFN	TSSOP		
AGND	15	5	—	Analog ground
BDGND	8	14	—	Interface ground
COM	14	4	I	Common inverting input; usually connected to ground
CONVST	3	9	I	Freezes sample-and-hold, starts conversion with next rising edge of internal clock
EOC/ $\overline{\text{INT}}$ / CDI	4	10	I/O	Status output. If programmed as EOC, this pin is low (default) when a conversion is in progress. If programmed as an interrupt (INT), this pin is low for a preprogrammed duration after the end of conversion and valid data are to be output. The polarity of EOC or INT is programmable. This pin can also be used as a chain data input when the device is operated in daisy-chain mode.
FS/ $\overline{\text{CS}}$	5	11	I	Frame sync signal for TMS320 DSP serial interface or chip select input for SPI interface
+IN1	12	2	I	Second noninverting input
+IN0	13	3	I	First noninverting input
NC	2	8	—	No connection.
REF+ (REFIN)	1	7	I	External reference input
REF–	16	6	I	Connect to AGND through individual via
SCLK	9	15	I	Clock for serial interface
SDI	6	12	I	Serial data in (conversion start and reset possible)
SDO	7	13	O	Serial data out
+VA	11	1		Analog supply, +2.7V to +5.5VDC
+VBD	10	16		Interface supply

MANUAL TRIGGER/READ While Sampling  
(use internal CCLK, EOC, and INT polarity programmed as active low)

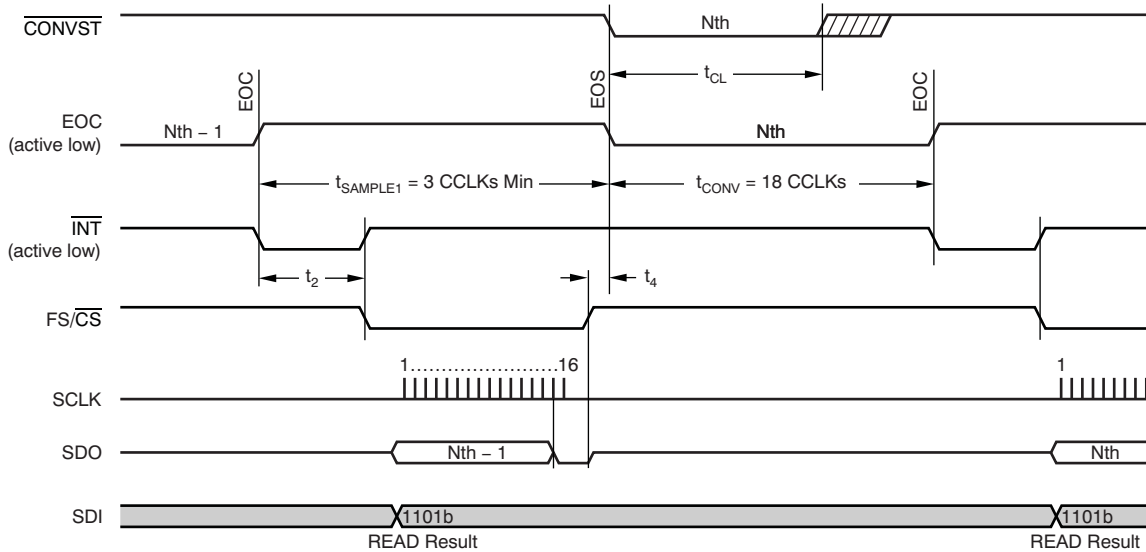


Figure 1. Timing for Conversion and Acquisition Cycles for Manual Trigger (Read While Sampling)

MANUAL TRIGGER/READ While Converting  
(use internal CCLK, EOC, and INT polarity programmed as active low)

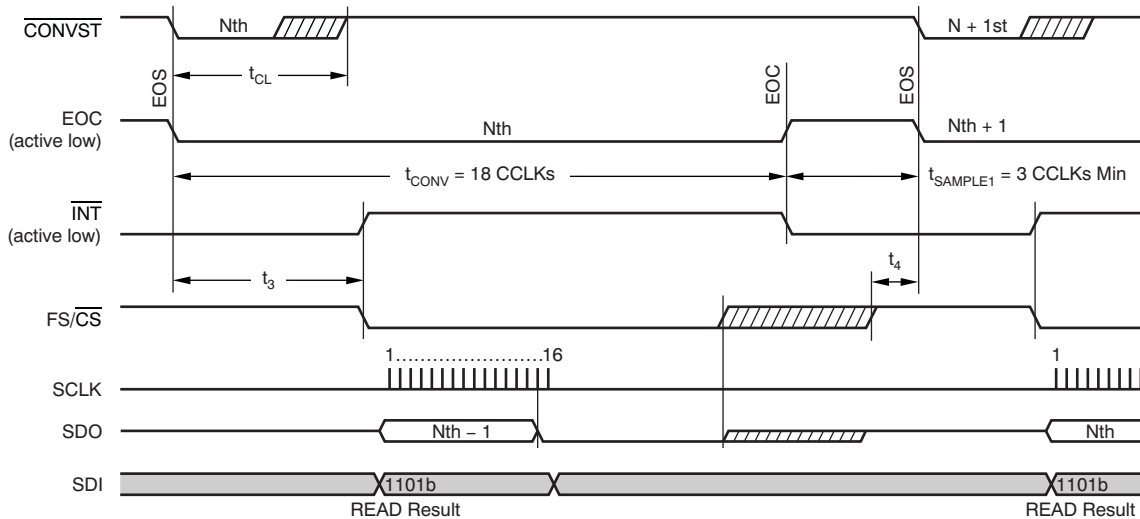


Figure 2. Timing for Conversion and Acquisition Cycles for Manual Trigger (Read While Converting)

AUTO TRIGGER/READ While Converting  
(use internal CCLK, EOC, and INT polarity programmed as active low)

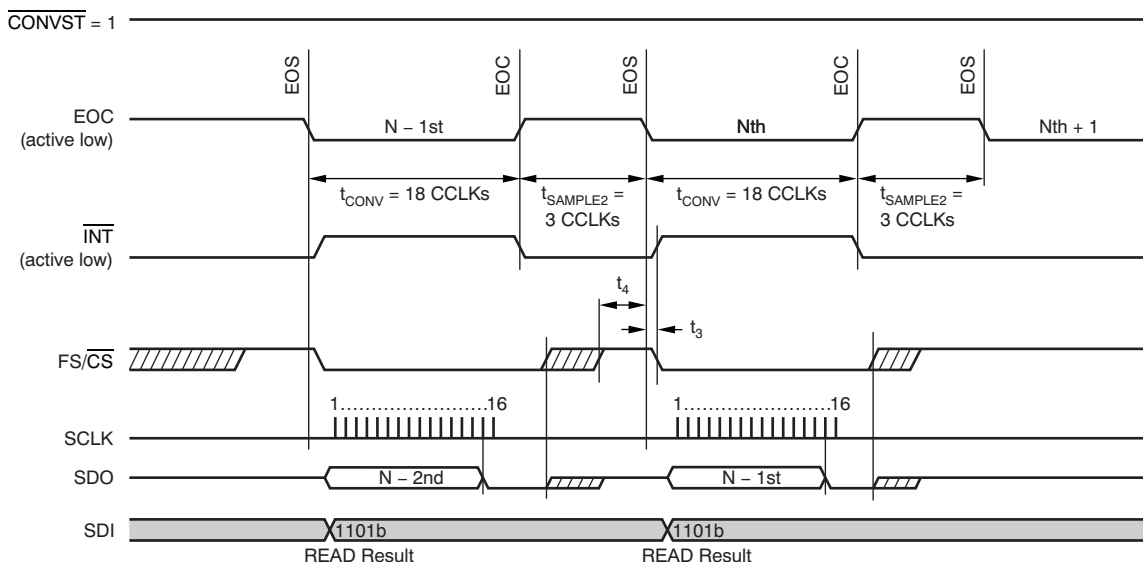


Figure 3. Timing for Conversion and Acquisition Cycles for Autotrigger (Read While Converting)

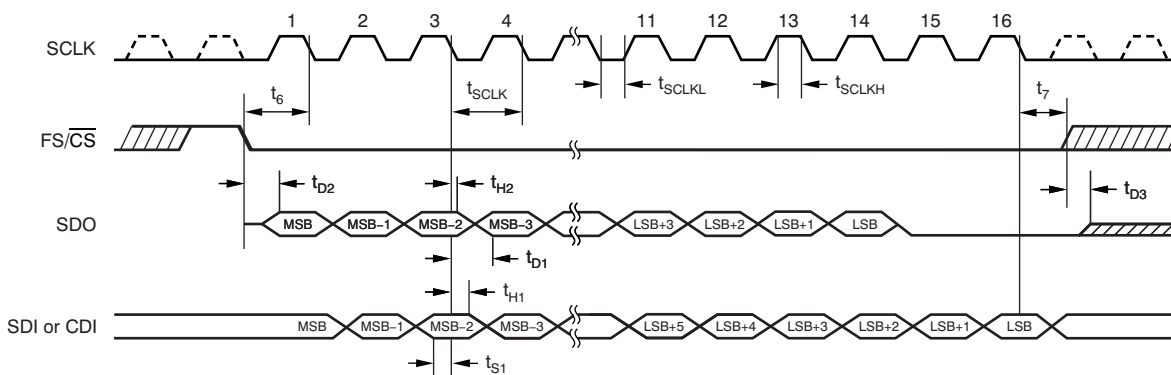


Figure 4. Detailed SPI Transfer Timing

MANUAL TRIGGER/READ While Converting  
(use internal CCLK, EOC, and INT polarity programmed as active low, TAG enabled, auto channel select)

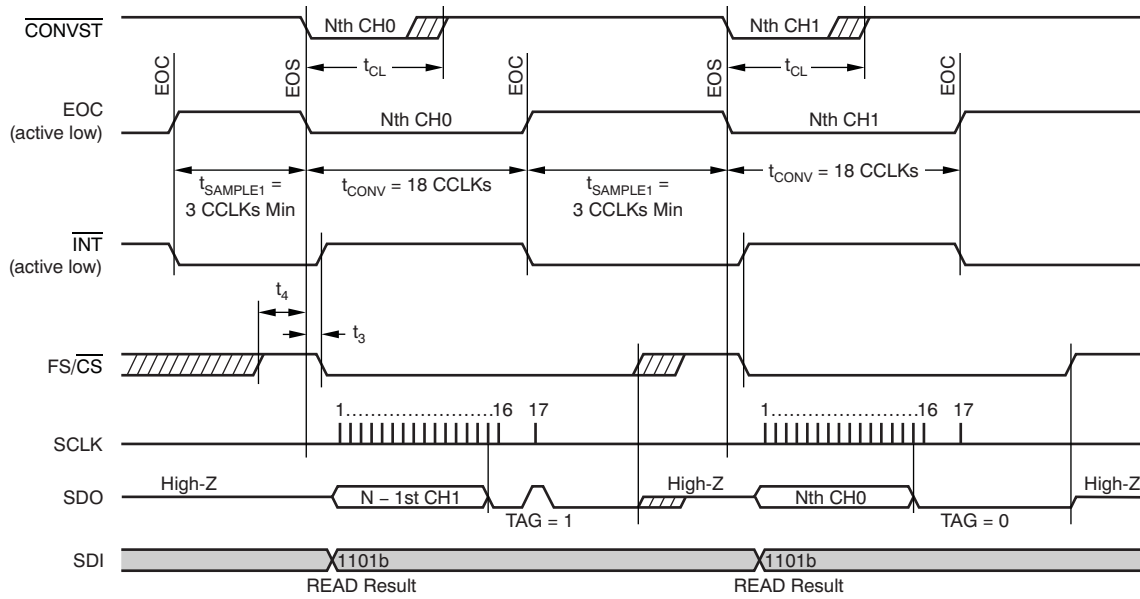


Figure 5. Simplified Dual Channel Timing

**TYPICAL CHARACTERISTICS**

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{REF}} [(\text{REF}+) - (\text{REF}-)] = 5\text{V}$  when  $+VA = +VBD = 5\text{V}$  or  $V_{\text{REF}} [(\text{REF}+) - (\text{REF}-)] = 2.5\text{V}$  when  $+VA = +VBD = 3\text{V}$ ,  $f_{\text{SCLK}} = 42\text{MHz}$ , or  $V_{\text{REF}} = 2.5$  when  $+VA = +VBD = 2.7\text{V}$ ,  $f_{\text{SCLK}} = 37.8\text{MHz}$ ;  $f_1 = \text{dc}$  for dc curves,  $f_1 = 100\text{kHz}$  for ac curves with  $5\text{V}$  supply and  $f_1 = 10\text{kHz}$  for ac curves with  $3\text{V}$  supply, unless otherwise noted.

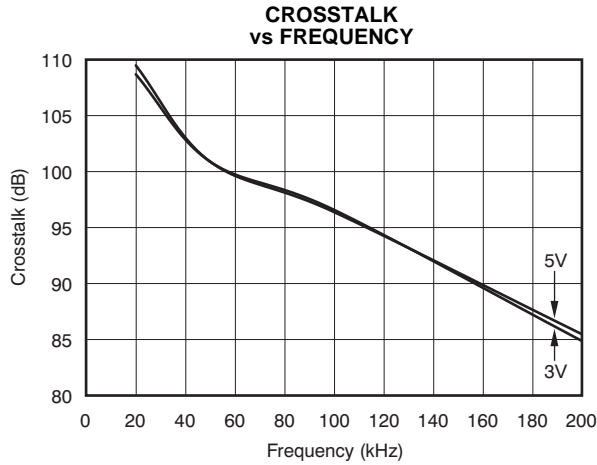


Figure 6.

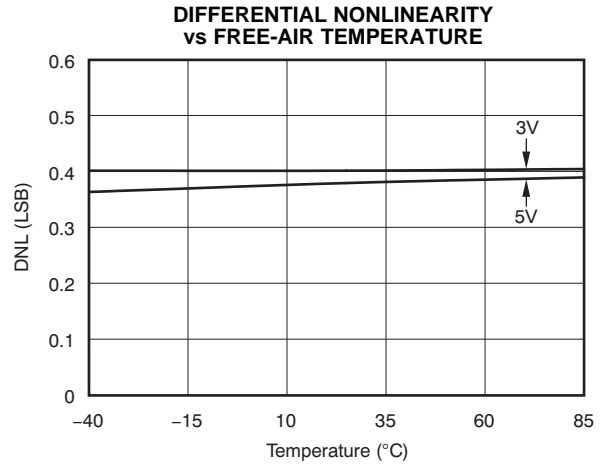


Figure 7.

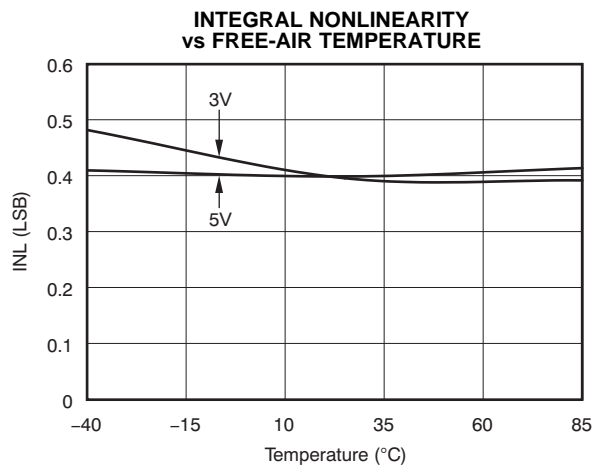


Figure 8.

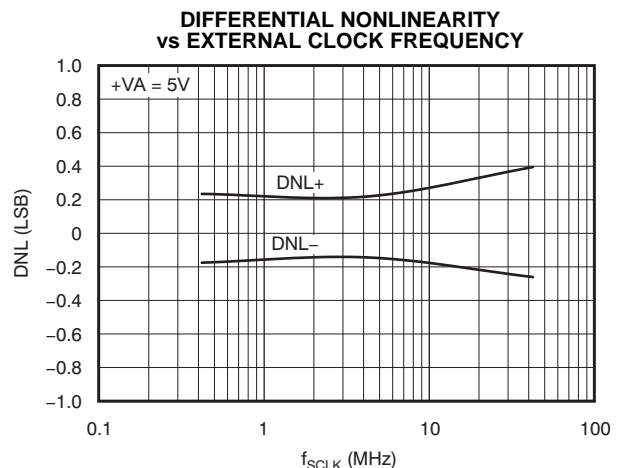


Figure 9.

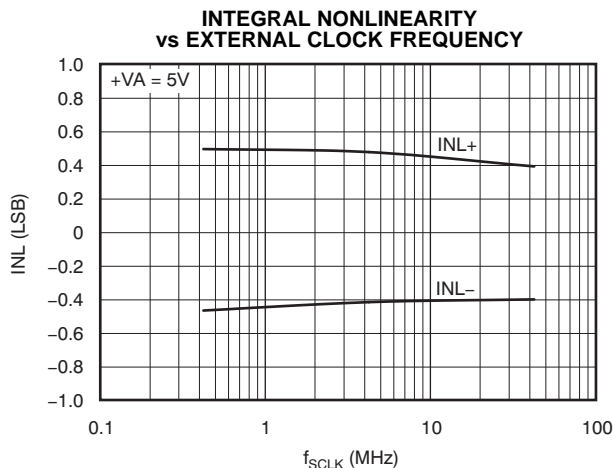


Figure 10.

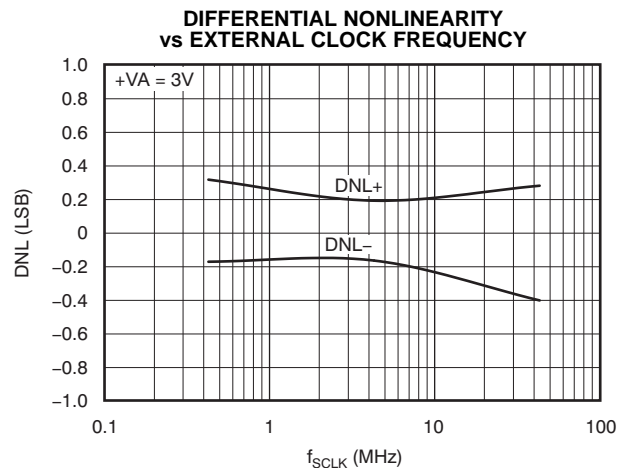


Figure 11.

**TYPICAL CHARACTERISTICS (continued)**

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 5\text{V}$  when  $+VA = +VBD = 5\text{V}$  or  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 2.5\text{V}$  when  $+VA = +VBD = 3\text{V}$ ,  $f_{\text{SCLK}} = 42\text{MHz}$ , or  $V_{\text{REF}} = 2.5$  when  $+VA = +VBD = 2.7\text{V}$ ,  $f_{\text{SCLK}} = 37.8\text{MHz}$ ;  $f_i = \text{dc}$  for dc curves,  $f_i = 100\text{kHz}$  for ac curves with 5V supply and  $f_i = 10\text{kHz}$  for ac curves with 3V supply, unless otherwise noted.

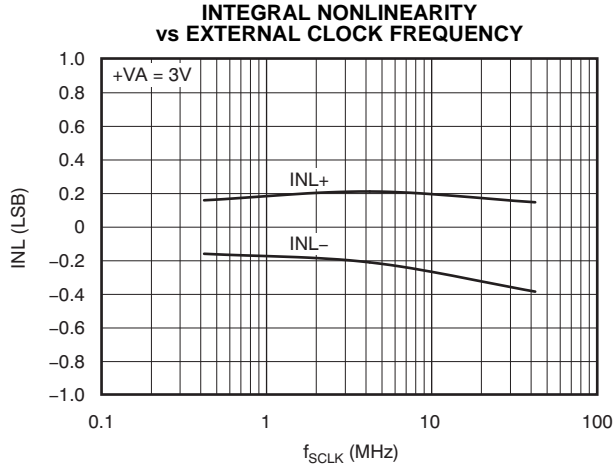


Figure 12.

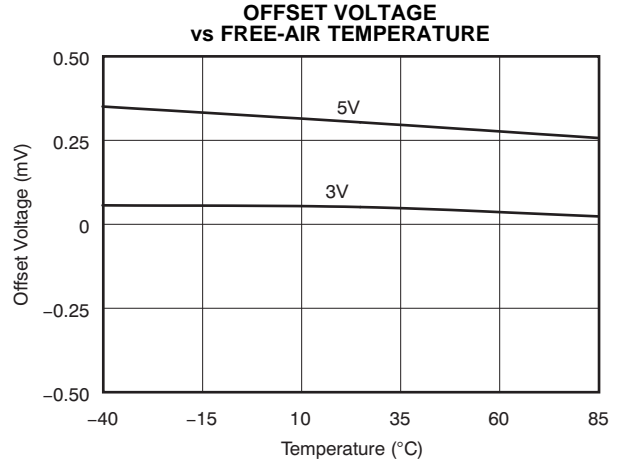


Figure 13.

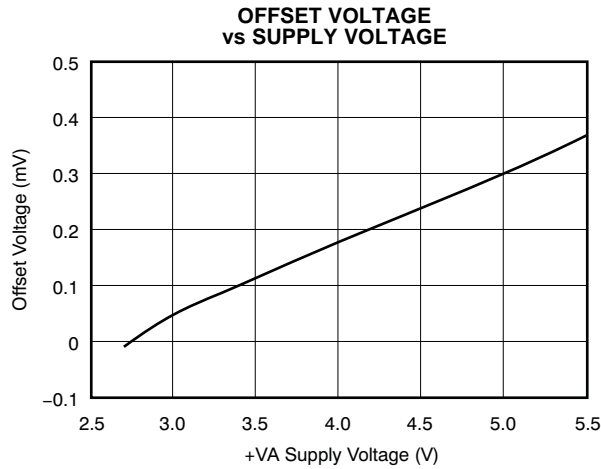


Figure 14.

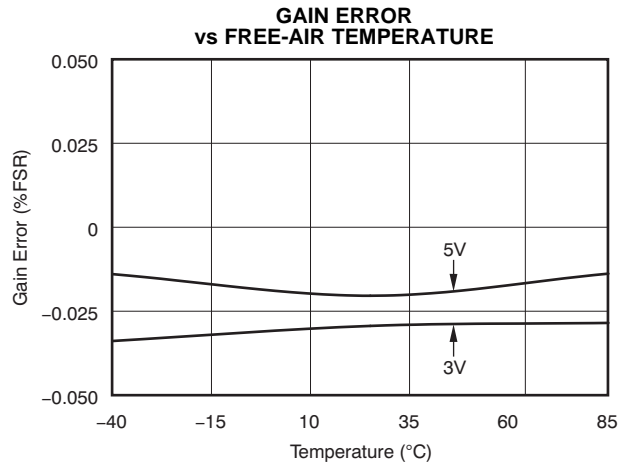


Figure 15.

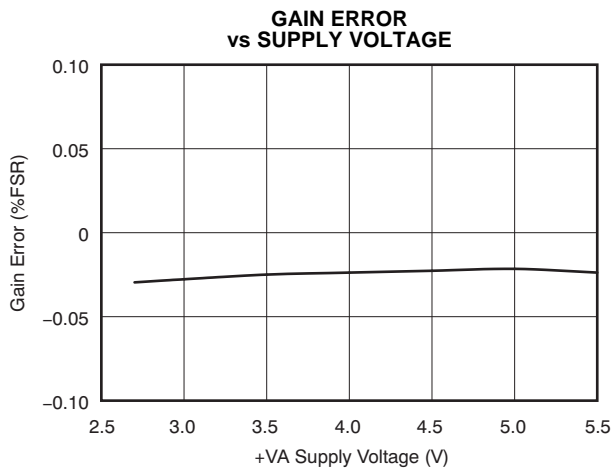


Figure 16.

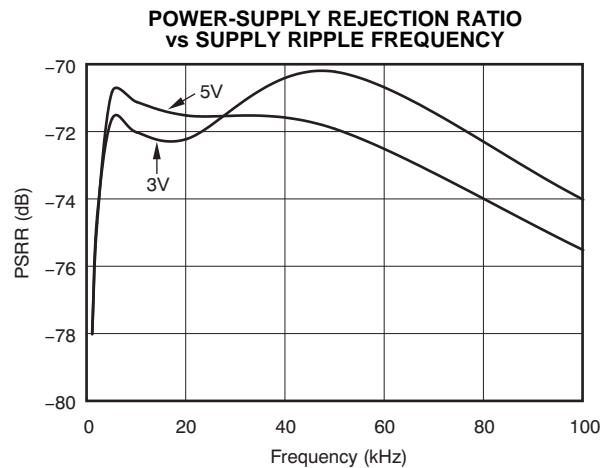


Figure 17.

**TYPICAL CHARACTERISTICS (continued)**

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 5\text{V}$  when  $+V_A = +V_{\text{BD}} = 5\text{V}$  or  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 2.5\text{V}$  when  $+V_A = +V_{\text{BD}} = 3\text{V}$ ,  $f_{\text{SCLK}} = 42\text{MHz}$ , or  $V_{\text{REF}} = 2.5$  when  $+V_A = +V_{\text{BD}} = 2.7\text{V}$ ,  $f_{\text{SCLK}} = 37.8\text{MHz}$ ;  $f_i = \text{dc}$  for dc curves,  $f_i = 100\text{kHz}$  for ac curves with  $5\text{V}$  supply and  $f_i = 10\text{kHz}$  for ac curves with  $3\text{V}$  supply, unless otherwise noted.

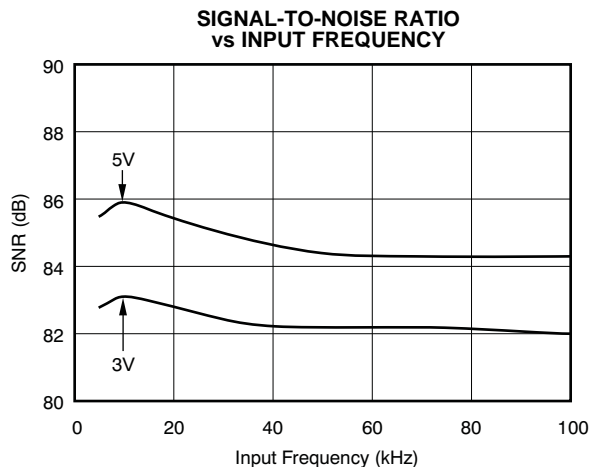


Figure 18.

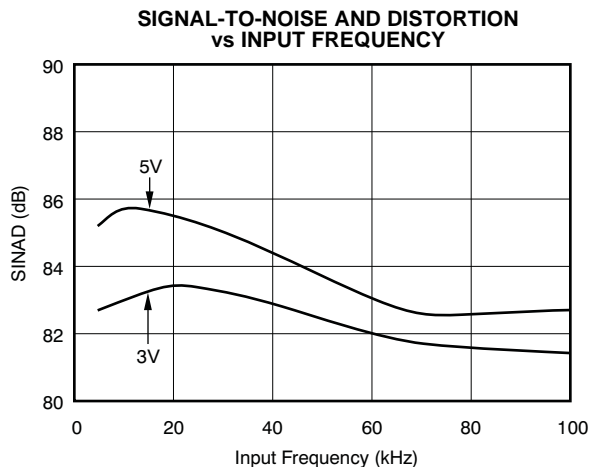


Figure 19.

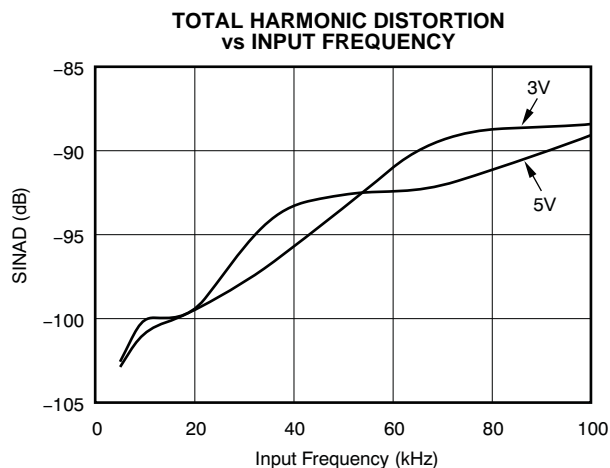


Figure 20.

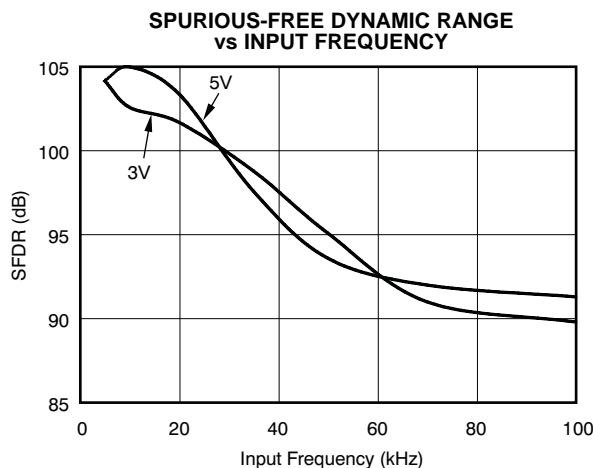


Figure 21.

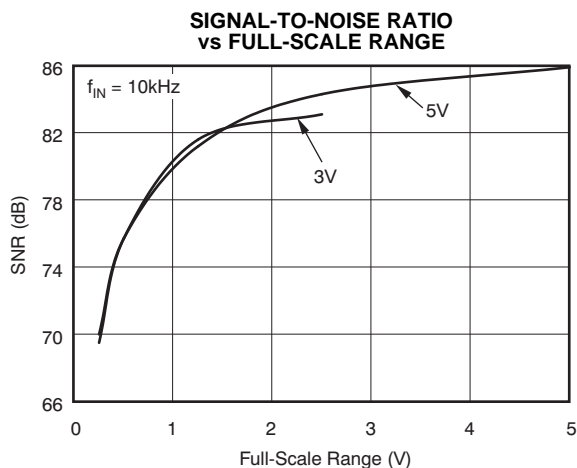


Figure 22.

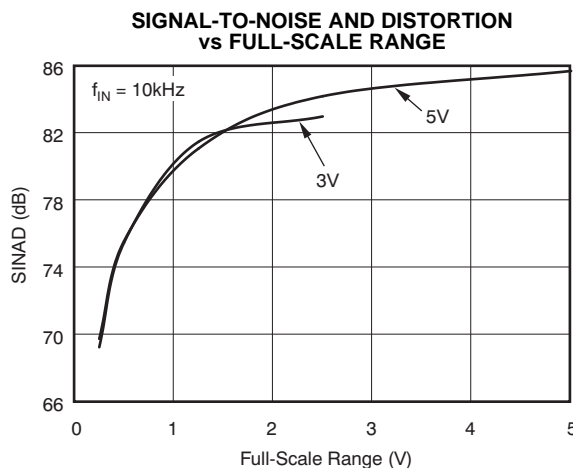


Figure 23.

**TYPICAL CHARACTERISTICS (continued)**

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 5\text{V}$  when  $+V_A = +V_{\text{BD}} = 5\text{V}$  or  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 2.5\text{V}$  when  $+V_A = +V_{\text{BD}} = 3\text{V}$ ,  $f_{\text{SCLK}} = 42\text{MHz}$ , or  $V_{\text{REF}} = 2.5$  when  $+V_A = +V_{\text{BD}} = 2.7\text{V}$ ,  $f_{\text{SCLK}} = 37.8\text{MHz}$ ;  $f_i = \text{dc}$  for dc curves,  $f_i = 100\text{kHz}$  for ac curves with  $5\text{V}$  supply and  $f_i = 10\text{kHz}$  for ac curves with  $3\text{V}$  supply, unless otherwise noted.

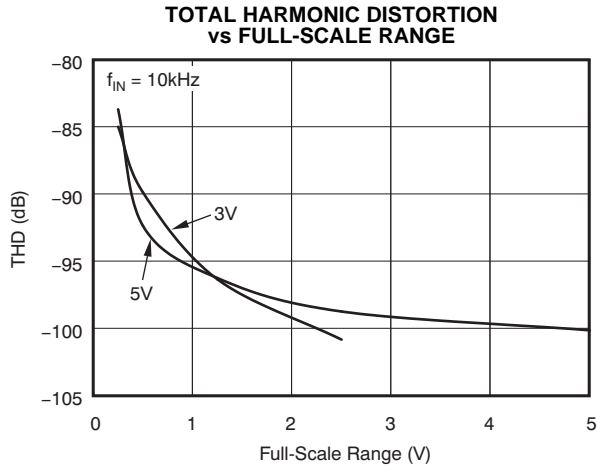


Figure 24.

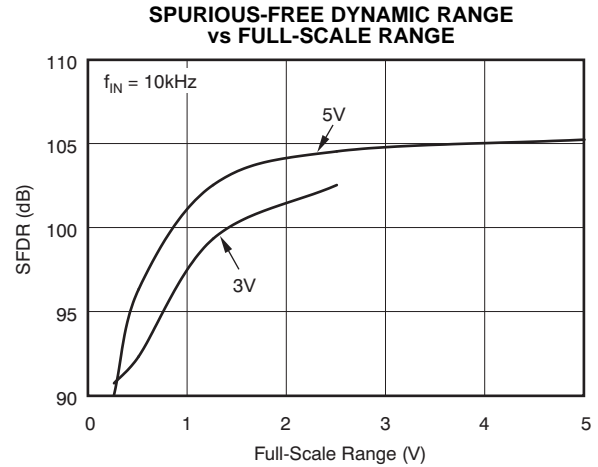


Figure 25.

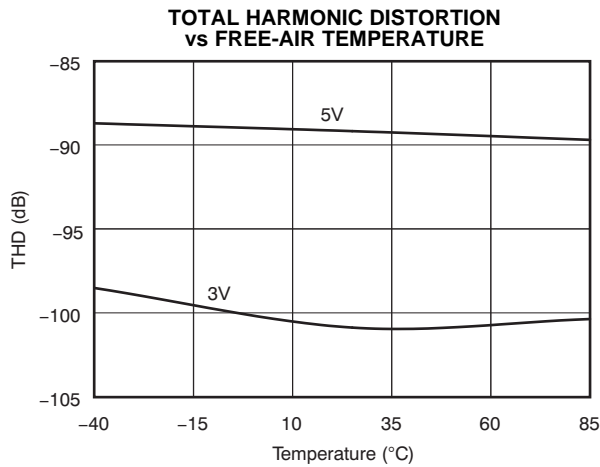


Figure 26.

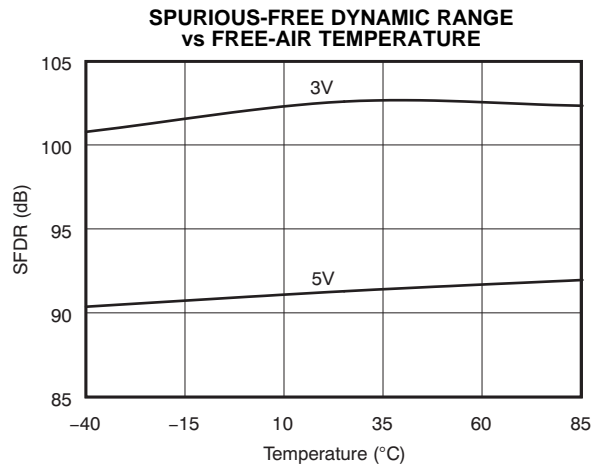


Figure 27.

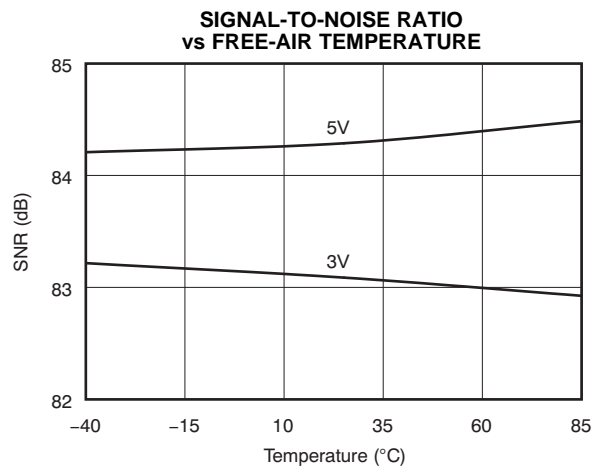


Figure 28.

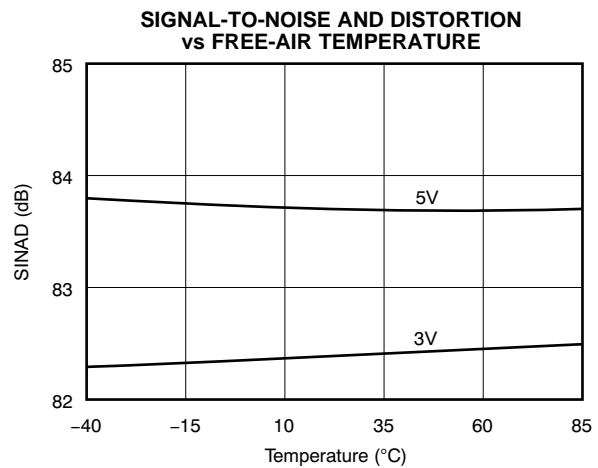


Figure 29.

**TYPICAL CHARACTERISTICS (continued)**

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 5\text{V}$  when  $+VA = +VBD = 5\text{V}$  or  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 2.5\text{V}$  when  $+VA = +VBD = 3\text{V}$ ,  $f_{\text{SCLK}} = 42\text{MHz}$ , or  $V_{\text{REF}} = 2.5$  when  $+VA = +VBD = 2.7\text{V}$ ,  $f_{\text{SCLK}} = 37.8\text{MHz}$ ;  $f_i = \text{dc}$  for dc curves,  $f_i = 100\text{kHz}$  for ac curves with  $5\text{V}$  supply and  $f_i = 10\text{kHz}$  for ac curves with  $3\text{V}$  supply, unless otherwise noted.

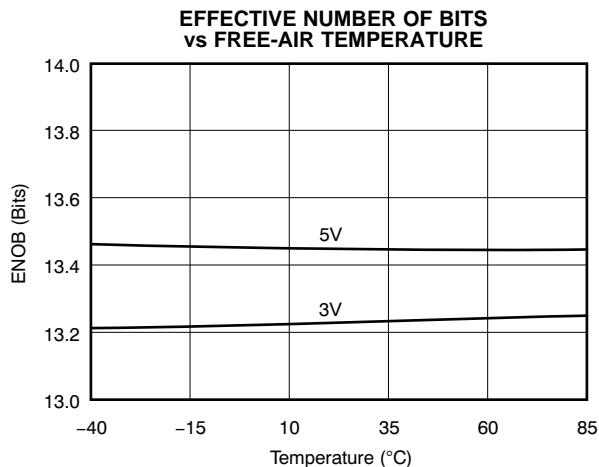


Figure 30.

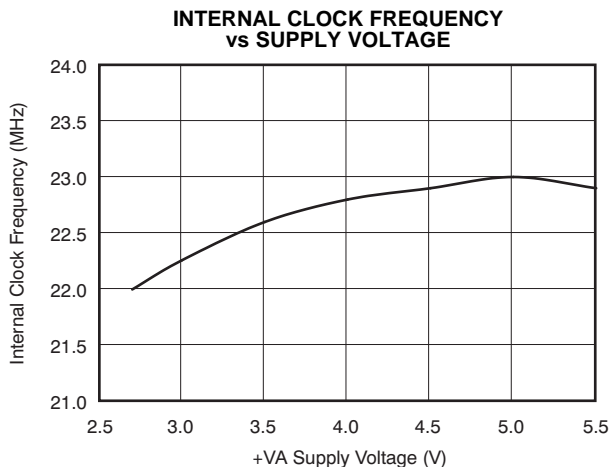


Figure 31.

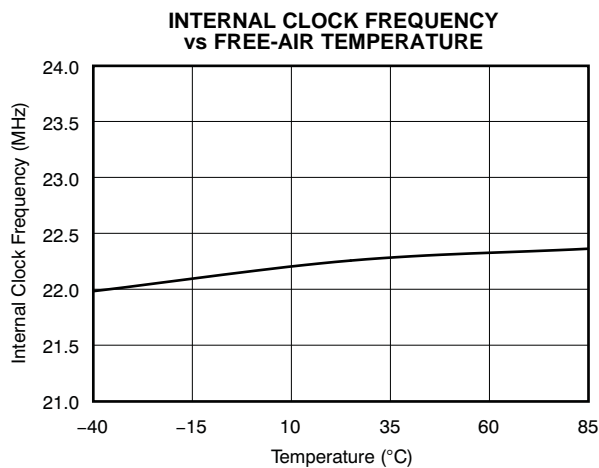


Figure 32.

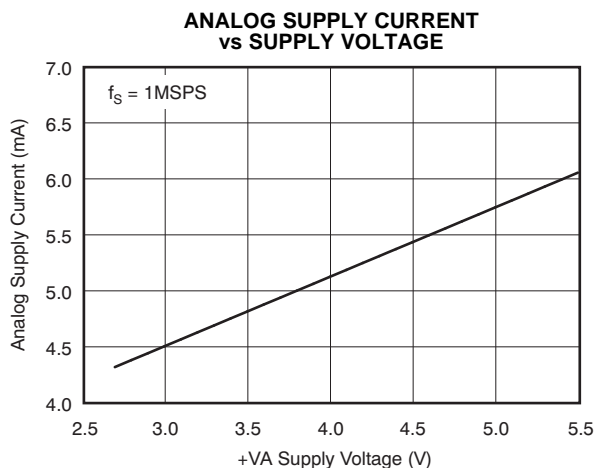


Figure 33.

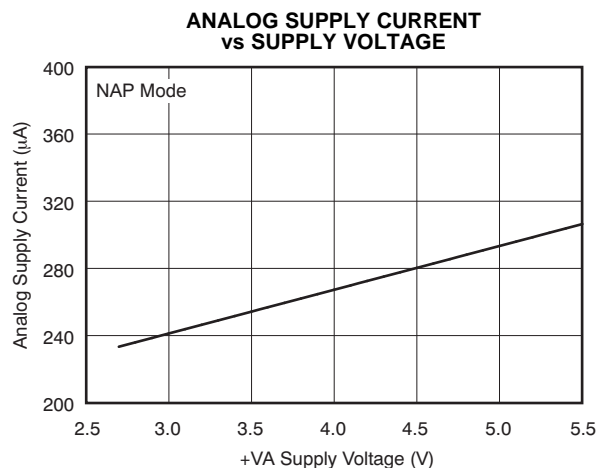


Figure 34.

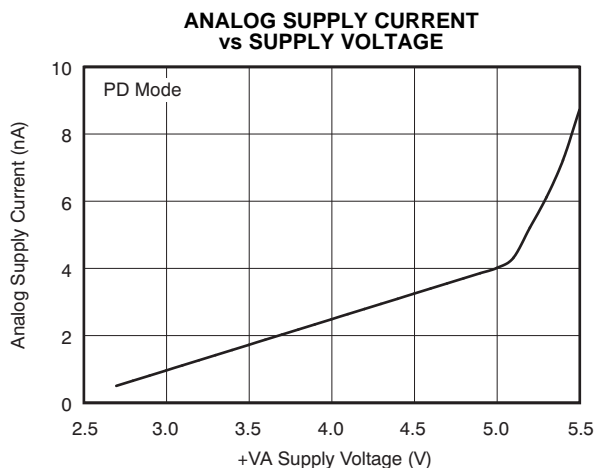


Figure 35.

**TYPICAL CHARACTERISTICS (continued)**

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 5\text{V}$  when  $+VA = +VBD = 5\text{V}$  or  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 2.5\text{V}$  when  $+VA = +VBD = 3\text{V}$ ,  $f_{\text{SCLK}} = 42\text{MHz}$ , or  $V_{\text{REF}} = 2.5$  when  $+VA = +VBD = 2.7\text{V}$ ,  $f_{\text{SCLK}} = 37.8\text{MHz}$ ;  $f_i = \text{dc}$  for dc curves,  $f_i = 100\text{kHz}$  for ac curves with  $5\text{V}$  supply and  $f_i = 10\text{kHz}$  for ac curves with  $3\text{V}$  supply, unless otherwise noted.

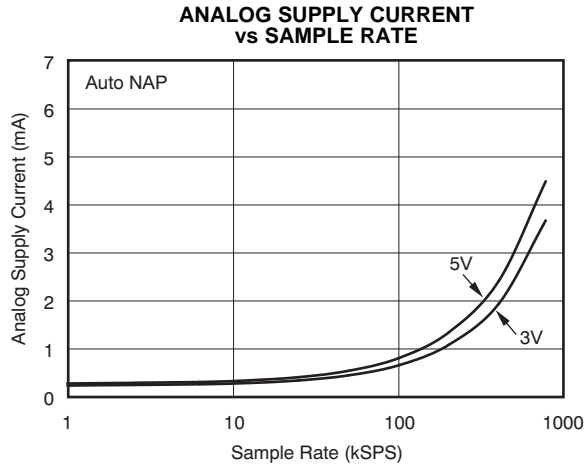


Figure 36.

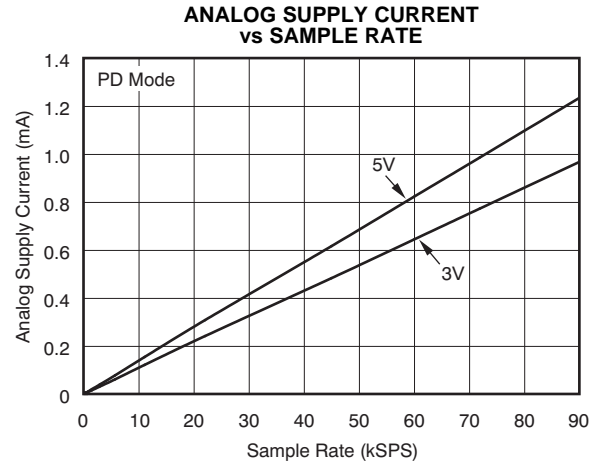


Figure 37.

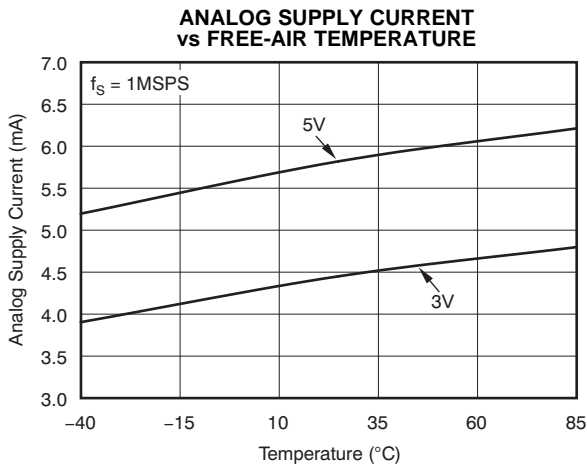


Figure 38.

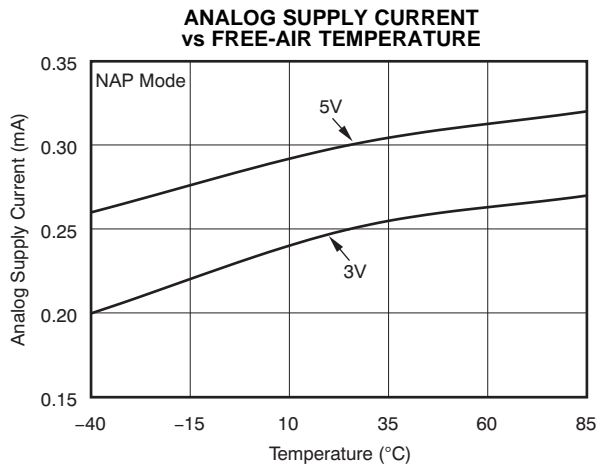


Figure 39.

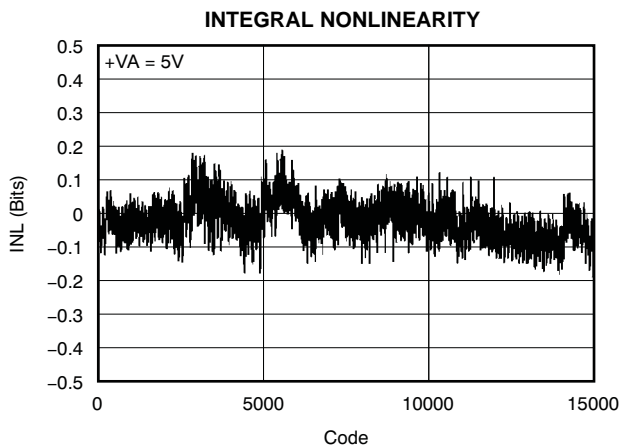


Figure 40.

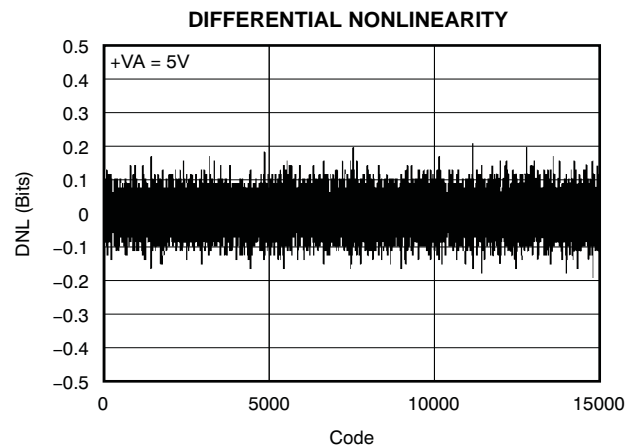


Figure 41.

**TYPICAL CHARACTERISTICS (continued)**

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 5\text{V}$  when  $+VA = +VBD = 5\text{V}$  or  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 2.5\text{V}$  when  $+VA = +VBD = 3\text{V}$ ,  $f_{\text{SCLK}} = 42\text{MHz}$ , or  $V_{\text{REF}} = 2.5$  when  $+VA = +VBD = 2.7\text{V}$ ,  $f_{\text{SCLK}} = 37.8\text{MHz}$ ;  $f_i = \text{dc}$  for dc curves,  $f_i = 100\text{kHz}$  for ac curves with 5V supply and  $f_i = 10\text{kHz}$  for ac curves with 3V supply, unless otherwise noted.

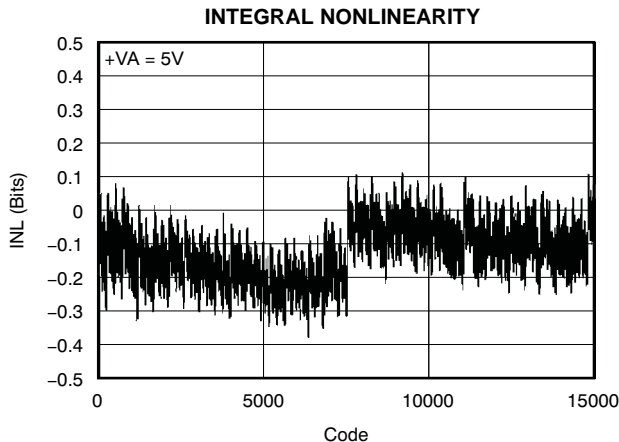


Figure 42.

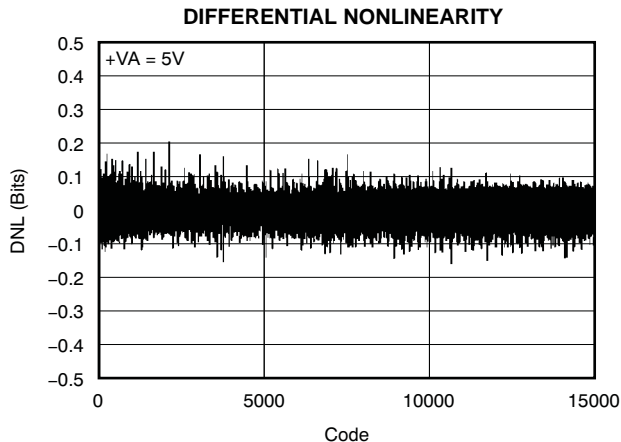


Figure 43.

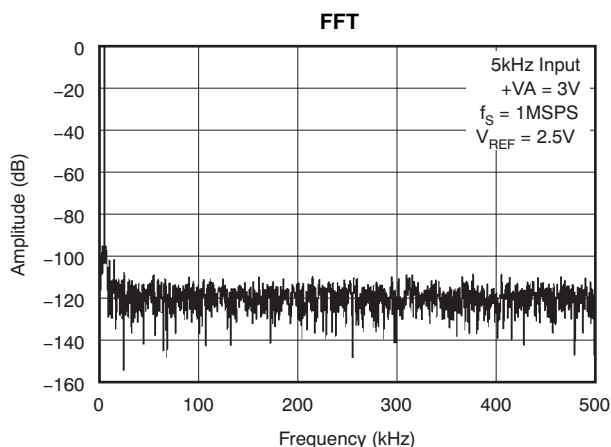


Figure 44.

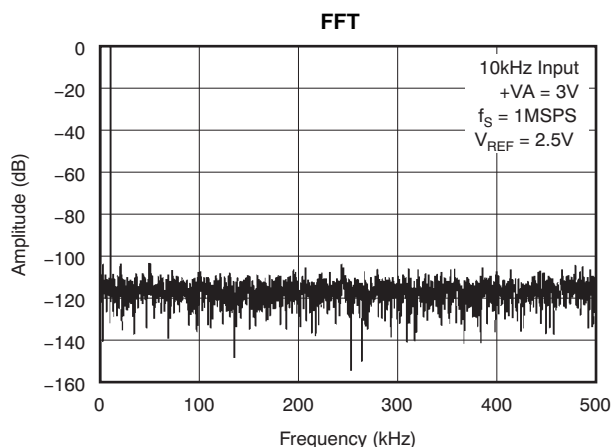


Figure 45.

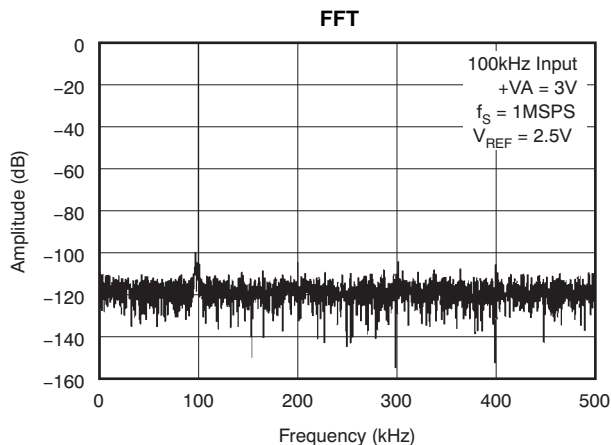


Figure 46.

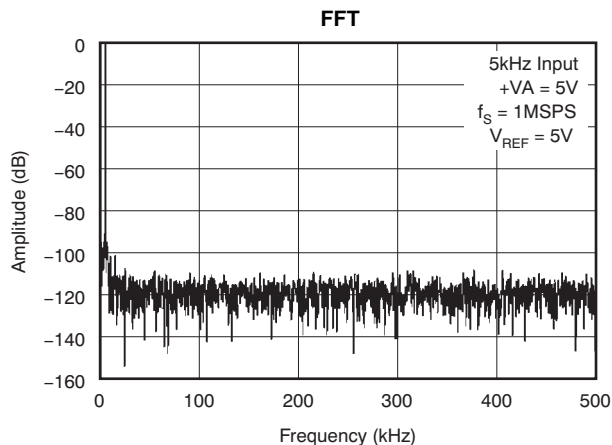


Figure 47.

**TYPICAL CHARACTERISTICS (continued)**

At  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 5\text{V}$  when  $+VA = +VBD = 5\text{V}$  or  $V_{\text{REF}}[(\text{REF}+) - (\text{REF}-)] = 2.5\text{V}$  when  $+VA = +VBD = 3\text{V}$ ,  $f_{\text{SCLK}} = 42\text{MHz}$ , or  $V_{\text{REF}} = 2.5$  when  $+VA = +VBD = 2.7\text{V}$ ,  $f_{\text{SCLK}} = 37.8\text{MHz}$ ;  $f_i = \text{dc}$  for dc curves,  $f_i = 100\text{kHz}$  for ac curves with 5V supply and  $f_i = 10\text{kHz}$  for ac curves with 3V supply, unless otherwise noted.

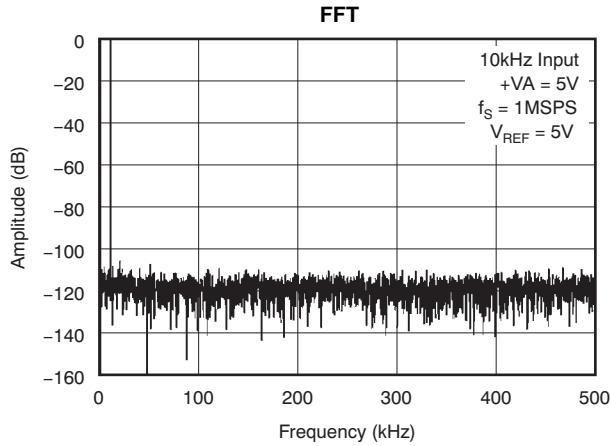


Figure 48.

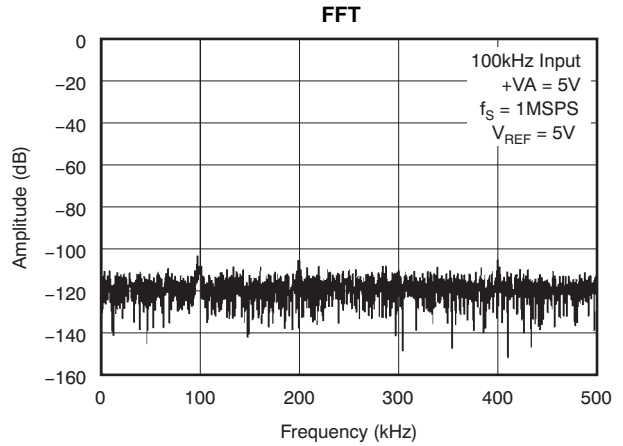


Figure 49.

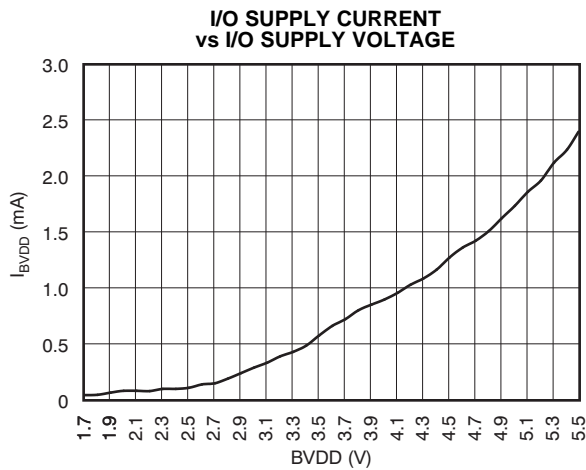


Figure 50.

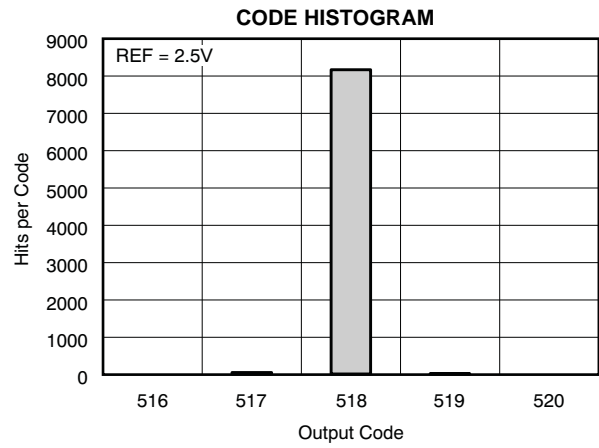


Figure 51.

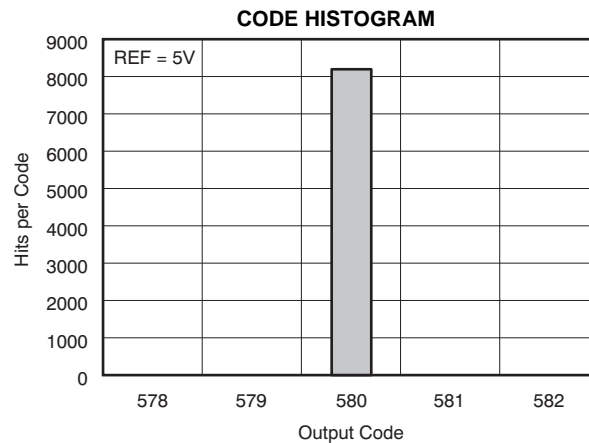


Figure 52.

## THEORY OF OPERATION

The ADS7279 and ADS7280 are two high-speed, low-power, successive approximation register (SAR) analog-to-digital converters (ADCs) that use an external reference. The architecture of each device is based on a charge redistribution model that inherently includes a sample-and-hold function.

These devices have an internal clock that runs the conversion; however, these ADCs can also be programmed to convert data based on an external serial clock, SCLK.

The ADS7279 has one analog input. The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both +IN and –IN inputs are disconnected from any internal function.

The ADS7280 has two inputs. Both inputs share the same common pin, COM. The negative input is the same as the –IN pin for the ADS7279. The ADS7280 can be programmed to select a channel manually, or it can be programmed into the auto channel select mode to sweep between channel 0 and channel 1 automatically.

Throughout this document, the term *ADS7279/80* refers to both devices, unless specifically noted otherwise.

## ANALOG INPUT

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array. The voltage on the –IN input is limited between  $AGND - 0.2V$  and  $AGND + 0.2V$ , allowing the input to reject small signals that are common to both the +IN and –IN inputs. The +IN input has a range of  $-0.2V$  to  $(V_{REF} + 0.2V)$ . The input span  $[(+IN) - (-IN)]$  is limited to  $0V$  to  $V_{REF}$ .

The (peak) input current through the analog inputs depends upon a number of factors: sample rate, input voltage, and source impedance. The current into the ADS7279/80 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (45pF) to a 14-bit settling level within the minimum acquisition time (120ns). When the converter goes into hold mode, the input impedance is greater than  $1G\Omega$ .

Care must be taken regarding the absolute analog input voltage. To maintain converter linearity, the +IN and –IN inputs and the span  $[(+IN) - (-IN)]$  should be within the limits specified. Beyond these ranges, converter linearity may not meet specifications. To minimize noise, low bandwidth input signals with low-pass filters should be used. Care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. If this input matching is not observed, the two inputs could have different settling times. This difference may result in an offset error, gain error, and linearity errors that change with temperature and input voltage.

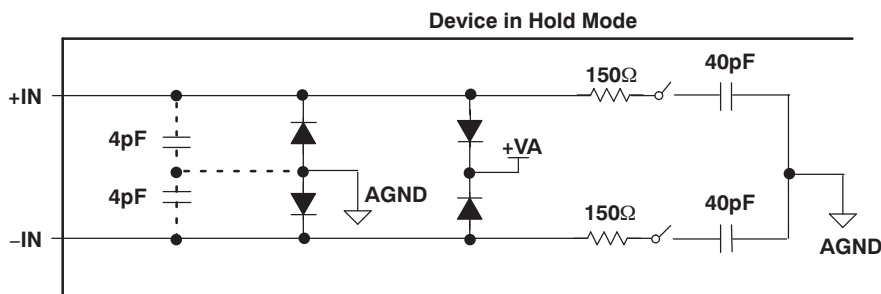


Figure 53. Input Equivalent Circuit

## Driver Amplifier Choice

The analog input to the converter must be driven with a low-noise operational amplifier such as the [THS4031](#) or [OPA365](#). An RC filter is recommended at the input pins to low-pass filter the noise from the source. Two 20Ω resistors and a 470pF capacitor are recommended. The input to the converter is a unipolar input voltage in the range of 0V to  $V_{REF}$ . The minimum -3dB bandwidth of the driving operational amplifier can be calculated as:

$$f_{3db} = (\ln(2) \times (n+1)) / (2\pi \times t_{ACQ})$$

where  $n$  is equal to 14, the resolution of the ADC (in the case of the ADS7279/80). When  $t_{ACQ} = 120\text{ns}$  (minimum acquisition time), the minimum bandwidth of the driving amplifier is 13.8MHz. The bandwidth can be relaxed if the acquisition time is increased by the application. [Figure 54](#) shows the THS4031 used in the source follower configuration to drive the converter in a typical input drive configuration. For the ADS7280, a series resistor of 0Ω should be used on the COM input (or no resistor at all).

## Bipolar to Unipolar Driver

In systems where the input is bipolar, the THS4031 can be used in an inverting configuration with an additional dc bias applied to its positive input to keep the input to the ADS7279/80 within the rated operating voltage range. This configuration is also recommended when the ADS7279/80 is used in signal processing applications where good SNR and THD performance are required. The dc bias can be derived from the [REF5025](#) or the [REF5040](#) reference voltage ICs. The input configuration shown in [Figure 55](#) is capable of delivering better than 85dB SNR and -100dB THD at an input frequency of 10kHz. If bandpass filters are used to filter the input, care should be taken to ensure that the signal swing at the input of the bandpass filter is small, in order to keep the distortion introduced by the filter minimal. In this case, the gain of the circuit shown in [Figure 55](#) can be increased to keep the input to the ADS7279/80 large in order to maintain a high SNR of the system. Note that the gain of the system from the positive input to the output of the THS4031 in such a configuration is a function of the ac signal gain. A resistor divider can be used to scale the output of the [REF5025](#) or [REF5040](#) to reduce the voltage at the dc input to the THS4031 to maintain the voltage at the converter input within its rated operating range.

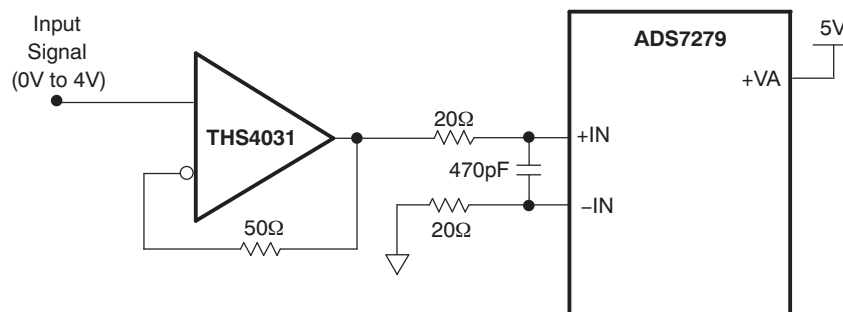


Figure 54. Unipolar Input Drive Configuration

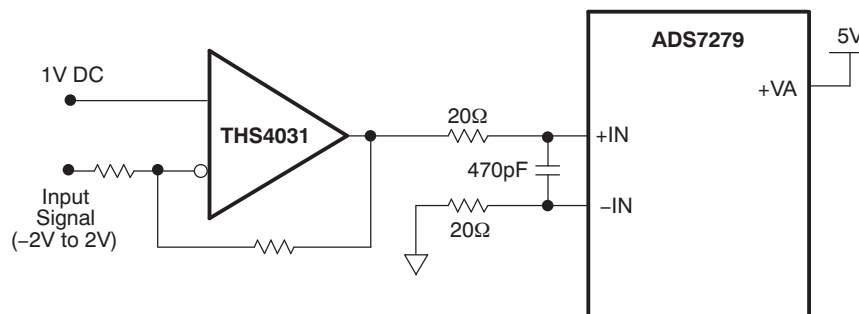


Figure 55. Bipolar Input Drive Configuration

## REFERENCE

The ADS7279/80 must operate with an external reference with a range from 0.3V to 5V. A clean, low-noise, well-decoupled reference voltage on the REF+ pin is required to ensure good converter performance. A low-noise bandgap reference such as the REF5040 can be used to drive this pin. A 22 $\mu$ F ceramic decoupling capacitor is required between the REF+ and REF– pins of the converter. These capacitors should be placed as close as possible to the device pins. REF– should be connected with an own via to the analog ground plane with the shortest possible distance. A series resistor between the reference and the REF50xx is neither required (because the REF50xx is capable of driving a 22 $\mu$ F capacitor while maintaining stability) nor recommended (as a result of additional nonlinearity); see also Figure 68.

## CONVERTER OPERATION

The ADS7279/80 has an oscillator that is used as an internal clock, which controls the conversion rate. The frequency of this clock is 21MHz (minimum). The oscillator is always on, unless the device is in the deep power-down state or the device is programmed for using SCLK as the conversion clock (CCLK). The minimum acquisition (sampling) time takes 3 CCLKs (equivalent to 143ns at 21MHz) and the conversion time takes 18 conversion clocks (CCLK) or approximately 857ns at 21MHz to complete one conversion.

The conversion can also be programmed to run based on an external serial clock, SCLK. This option allows the designer to fully synchronize the converter with the system. The serial clock SCLK is first reduced to 1/2 of its frequency before it is used as the conversion clock (CCLK). For example, with a 42MHz SCLK, this reduction provides a 21MHz clock for conversions. If it is desired to start a conversion at a specific rising edge of SCLK when the external SCLK is programmed as the source of the conversion clock (and manual conversion start is selected), the setup time between  $\overline{\text{CONVST}}$  and that rising SCLK edge should be observed. This configuration ensures that the conversion is complete in 18 CCLKs (or 36 SCLKs). The minimum setup time is 20ns to ensure synchronization between  $\overline{\text{CONVST}}$  and SCLK. In many cases, the conversion can start one SCLK period (or CCLK) later, which results in a conversion length of 19 CCLKs (or 37 SCLKs). The 20ns setup time is not required if the synchronization is not critical to the application.

The duty cycle of SCLK is not critical as long as it meets the minimum high and low time requirements of 8ns. The ADS7279/80 is designed for high-speed applications; therefore, a higher serial clock (SCLK) must be supplied to be able to sustain the high throughput with the serial interface. As a result, the clock period of SCLK must be at most 1 $\mu$ s (when used as the conversion clock, CCLK). The minimum clock frequency is also governed by the parasitic leakage of the capacitive digital-to-analog (CDAC) capacitors internal to the ADS7279/80.

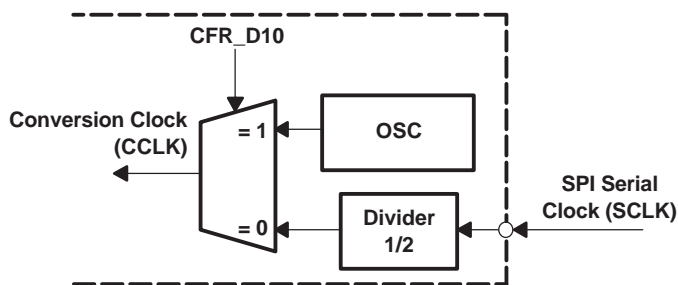


Figure 56. Converter Clock

## Manual Channel Select Mode

The conversion cycle starts with selecting an acquisition channel by writing a channel number to the command register, CMR. The command length can be as short as four SCLKs.

### Auto Channel Select Mode

Channel selection can also be done automatically if auto channel select mode is enabled. This mode is the default channel select mode. The dual channel converter, ADS7280, has a built-in 2-to-1 MUX. If the device is programmed for auto channel select mode, then signals from channel 0 and channel 1 are acquired with a fixed order. Channel 0 is accessed first in the next cycle after the command cycle that configured CFR\_D11 to '1' for auto channel select mode. This automatic access stops the first cycle after the command cycle that sets CFR\_D11 to '0'.

### Start of a Conversion

The end of sampling instance (EOS) or acquisition is the same as the start of a conversion. This event is initiated by bringing the CONVST pin low for a minimum of 40ns. After the minimum requirement has been met, the CONVST pin can be brought high. CONVST acts independently of FS/CS so it is possible to use one common CONVST for applications that require a simultaneous sample/hold with multiple converters. The ADS7279/80 switches from sample to hold mode on the falling edge of the CONVST signal. The ADS7279/80 requires 18 conversion clock (CCLK) edges to complete a conversion. The conversion time is equivalent to 857ns with a 21MHz internal clock. The minimum time between two consecutive CONVST signals is 21 CCLKs.

A conversion can also be initiated without using CONVST if auto-trigger mode is used (CFR\_D9 = 0). When the converter is configured as an auto trigger, the next conversion automatically starts three conversion clocks (CCLK) after the end of a conversion. These three conversion clocks are used as the acquisition time. In this case, the time to complete one acquisition and conversion cycle is 21 CCLKs. Table 1 summarizes the different conversion modes.

**Table 1. Different Types of Conversion**

MODE	SELECT CHANNEL	START CONVERSION
Automatic	<b>Auto Channel Select<sup>(1)</sup></b>	<b>Auto Trigger</b>
	No need to write channel number to the command register (CMR). Use internal sequencer for the ADS7280.	Start a conversion based on the conversion clock CCLK.
Manual	<b>Manual Channel Select</b>	<b>Manual Trigger</b>
	Write the channel number to the CMR.	Start a conversion with CONVST.

(1) Auto channel select should be used with the TAG bit enabled.

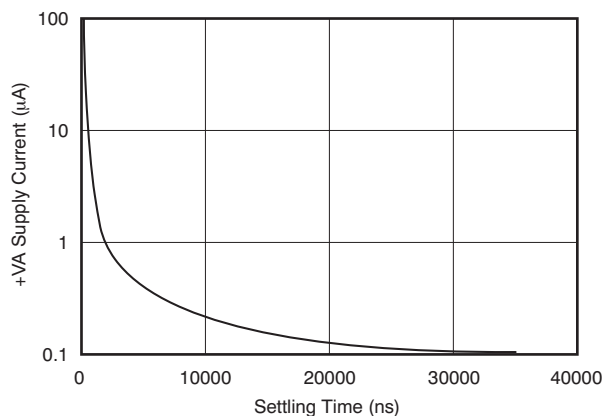
### Status Output EOC/INT

When the status pin is programmed as EOC and the polarity is set as active low, the pin works in the following manner: The EOC output goes low immediately after CONVST goes low when the manual trigger is programmed. EOC stays low throughout the conversion process and returns high when the conversion ends. The EOC output goes low for three conversion clocks after the previous rising edge of EOC, if auto trigger is programmed.

This status pin is programmable. It can be used as an EOC output (CFR\_D[7:6] = 1, 1) where the low time is equal to the conversion time. This status pin can also be used as INT (CFR\_D[7:6] = 1, 0), which is set low as the end of a conversion is brought high (cleared) by the next read cycle. The polarity of this pin, used as either function (that is, EOC or INT), is programmable through CFR\_D7.

## Power-Down Modes

The ADS7279/80 has a comprehensive, built-in power-down feature. There are three power-down modes: Deep power-down mode, Nap power-down mode, and Auto nap power-down mode. All three power-down modes are enabled by setting the related CFR bits. The first two power-down modes are activated when enabled. A wakeup command, 1011b, resumes device operation from a power-down mode. Auto nap power-down mode works slightly differently. When the converter is enabled in Auto nap power-down mode, an end of conversion instance (EOC) puts the device into auto nap power-down. The beginning of sampling resumes converter operation. The contents of the configuration register are not affected by any of the power-down modes. Any ongoing conversion when nap or deep power-down is activated is aborted.



**Figure 57. Typical Analog Supply Current Drop vs Time After Power-Down**

### Deep Power-Down Mode

Deep power-down mode can be activated by writing to configuration register bit CFR\_D2. When the device is in Deep power-down mode, all blocks except the interface are in power-down. The external SCLK is internally blocked. Also, all bias currents and the internal oscillator are turned off. In this mode, supply current falls from 5.7mA to 4nA within 100ns. The wake-up time after a deep power-down is 1µs. When bit D2 in the configuration register is set to '0', the device is in Deep power-down. Setting this bit to '1' or sending a wake-up command resumes the converter operation from the Deep power-down state.

### Nap Mode

In Nap mode, the ADS7279/80 turns off biasing of the comparator and the mid-voltage buffer. In this mode, supply current falls from 5.7mA in normal mode to about 0.3mA within 200ns after the configuration cycle. The wake-up (resume) time from Nap power-down mode is 3 CCLKs (143ns with a 21MHz conversion clock). As soon as the CFR\_D3 bit in the control register is set to '0', the device goes into Nap power-down mode, regardless of the conversion state. Setting this bit to '1' or sending a wake-up command resumes converter operation from the Nap power-down state.

### Auto Nap Mode

Auto nap mode is almost identical to nap mode. The only difference is the time when the device is actually powered down and the method used to wake up the device. Configuration register bit D4 is only used to enable/disable Auto nap mode. If Auto nap mode is enabled, the device turns off the biasing after the conversion has finished; that is, the end of conversion activates Auto nap power-down mode. Supply current falls from 5.7mA in normal mode to about 0.3mA within 200ns. A CONVST command resumes the device and turns on the biasing on again in 3 CCLKs (143ns with a 21MHz conversion clock). The device can also be woken up by disabling auto nap mode when bit D4 of the configuration register is set to '1'. Any channel select command 0XXXb, a wake-up command, or the set default mode command 1111b can also wake up the device from Auto nap power-down. [Table 2](#) compares the various power-down modes.

**NOTE:**

1. This wake-up command is the word *1011b* in the command word. This command sets bits D2 and D3 to '1' in the configuration register, but not D4. A wake-up command removes the device from any of these power-down states, Deep/Nap/Auto nap power-down.
2. Wake-up time is defined as the time between when the host processor tries to wake up the converter and when a conversion start can occur.

**Table 2. Power-Down Mode Comparisons**

TYPE OF POWER-DOWN	SUPPLY CURRENT AT 5V/3V	POWER-DOWN BY	TIME TO POWER-DOWN (ns)	WAKE-UP BY	WAKE-UP TIME	ENABLE
Normal operation	5.7mA/4.5mA	—	—	—	—	—
Deep power-down	4nA/1nA	Setting CFR	100	Woken up by command 1011b	1μs	Set CFR
Nap power-down	0.3mA/0.25mA	Setting CFR	200	Woken up by command 1011b	3 CCLKs	Set CFR
Auto nap power-down	0.3mA/0.25mA	EOC (end of conversion)	200	Woken up by <u>CONVST</u> , any channel select command, default command 1111b, or wake up command 1011b.	3 CCLKs	Set CFR

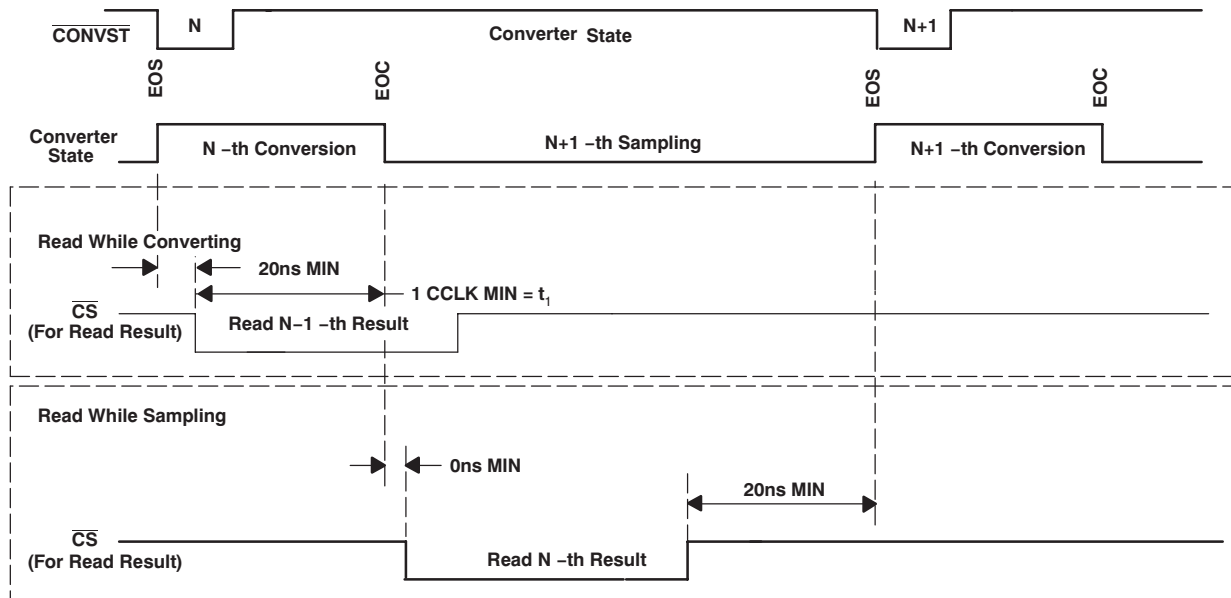


Figure 58. Read While Converting versus Read While Sampling (Manual Trigger)

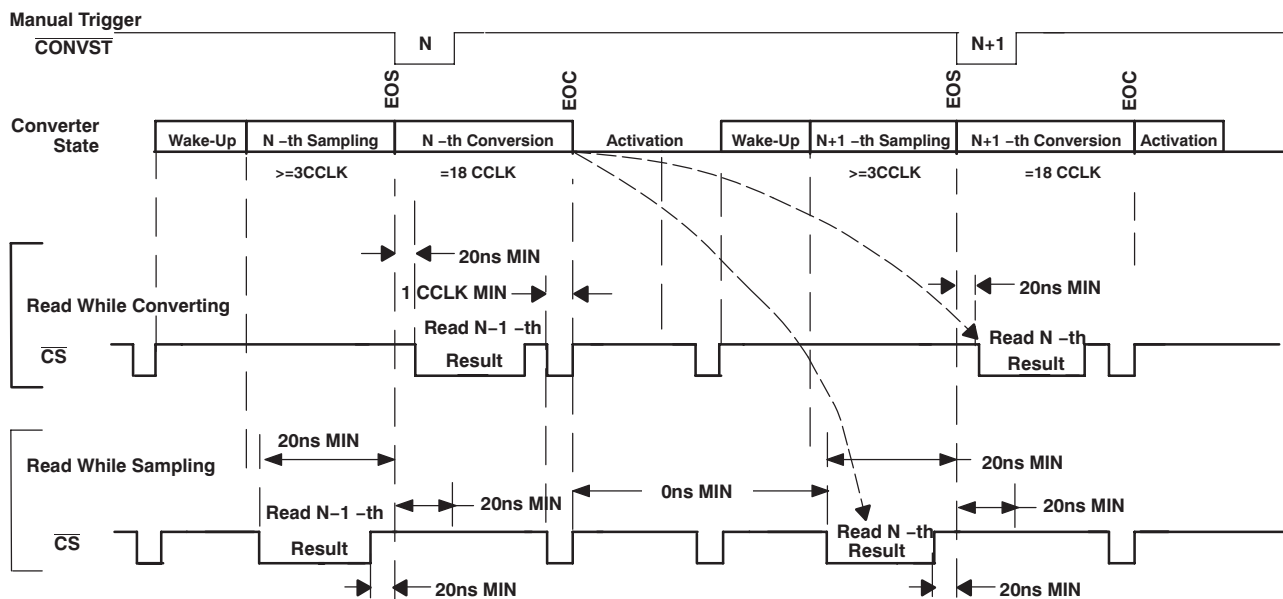


Figure 59. Read While Converting versus Read While Sampling with Deep or Nap Power-Down

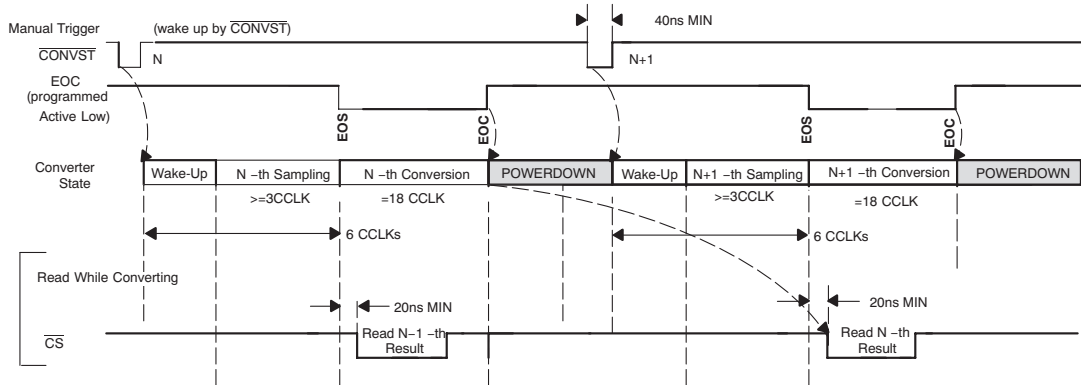


Figure 60. Read While Converting with Auto Nap Power-Down

Total Acquisition + Conversion Cycle Time:

Auto trigger: = 21 CCLKs

Manual:  $\geq 21$  CCLKs

Manual + deep power-down:  $\geq 4$  SCLK +  $100\mu\text{s}$  + 3 CCLK + 18 CCLK + 16 SCLK +  $1\mu\text{s}$

Manual + nap power-down:  $\geq 4$  SCLK + 3 CCLK + 3 CCLK + 18 CCLK + 16 SCLK

Manual + auto nap power-down:  $\geq 1$  CCLK + 3 CCLK + 3 CCLK + 18 CCLK + 16 SCLK (use  $\overline{\text{CONVST}}$  to resume)

Manual + auto nap power-down:  $\geq 4$  SCLK + 3 CCLK + 3 CCLK + 18 CCLK + 16 SCLK (use wake up to resume)

## DIGITAL INTERFACE

The serial clock is designed to accommodate the latest high-speed processors with an SCLK frequency up to 50MHz. Each cycle starts with the falling edge of  $\overline{FS}/\overline{CS}$ . The internal data register content that is made available to the output register at the EOC (presented on the SDO output pin at the falling edge of  $\overline{FS}/\overline{CS}$ ) is the MSB. Output data are valid at the falling edge of SCLK with a  $t_{D1}$  delay so that the host processor can read it at the falling edge. Serial data input is also read at the falling edge of SCLK.

The complete serial I/O cycle starts with the first falling edge of SCLK after the falling edge of  $\overline{FS}/\overline{CS}$  and ends 16 falling edges of SCLK later (see NOTE). The serial interface is very flexible. It works with  $CPOL = 0$ ,  $CPHA = 1$  or  $CPOL = 1$ ,  $CPHA = 0$ . This flexibility means the falling edge of  $\overline{FS}/\overline{CS}$  may fall while SCLK is high. The same relaxation applies to the rising edge of  $\overline{FS}/\overline{CS}$  where SCLK may be high or low as long as the last SCLK falling edge occurs before the rising edge of  $\overline{FS}/\overline{CS}$ .

### NOTE:

There are cases where a cycle is 4 SCLKs or up to 24 SCLKs depending on the read mode combination. See [Table 3](#) and [Table 6](#) for details.

### Internal Register

The internal register consists of two parts: 4 bits for the command register (CMR) and 12 bits for configuration data register (CFR). [Table 3](#) summarizes the command set defined by the CMR.

**Table 3. Command Set Defined by Command Register (CMR)<sup>(1)</sup>**

D[15:12]	HEX	COMMAND	D[11:0]	WAKE-UP FROM AUTO NAP	MINIMUM SCLKs REQUIRED	R/W
0000b	0h	Select analog input channel 0 <sup>(2)</sup>	Don't care	Y	4	W
0001b	1h	Select analog input channel 1 <sup>(2)</sup>	Don't care	Y	4	W
0010b	2h	Don't care	Don't care	–	–	–
0011b	3h	Don't care	Don't care	–	–	–
0100b	4h	Don't care	Don't care	–	–	–
0101b	5h	Don't care	Don't care	–	–	–
0110b	6h	Don't care	Don't care	–	–	–
0111b	7h	Don't care	Don't care	–	–	–
1000b	8h	Reserved for factory test, don't use	Reserved	–	–	–
1001b	9h	Reserved for factory test, don't use	Reserved	–	–	–
1010b	Ah	Reserved for factory test, don't use	Reserved	–	–	–
1011b	Bh	Wake up	Don't care	Y	4	W
1100b	Ch	Read CFR	Don't care	–	16	R
1101b	Dh	Read data	Don't care	–	14	R
1110	Eh	Write CFR	CFR value	–	16	W
1111b	Fh	Default mode (load CFR with default value)	Don't care	Y	4	W

(1) When SDO is not in 3-state mode ( $\overline{FS}/\overline{CS}$  low), the bits from SDO are always part of a conversion result (depending on how many SCLKs are supplied).

(2) These two commands apply to the ADS7280 only.

## WRITING TO THE CONVERTER

There are two different types of writes to the register: a 4-bit write to the CMR and a full 16-bit write to the CMR plus CFR. The command set is listed in [Table 3](#). A simple command requires only 4 SCLKs and the write takes effect at the fourth falling edge of SCLK. A 16-bit write or read takes at least 16 SCLKs (see [Table 6](#) for exceptions that require more than 16 SCLKs).

### Configuring the Converter and Default Mode

The converter can be configured with command 1110b (write to the CFR) or command 1111b (default mode). A write to the CFR requires a 4-bit command followed by 12 bits of data. A 4-bit command takes effect at the fourth falling edge of SCLK. A CFR write takes effect at the 16th falling edge of SCLK.

A default mode command can be achieved by simply tying SDI to +VBD. As soon as the chip is selected, at least four '1's are clocked in by SCLK. The default value of the CFR is loaded into the CFR at the fourth falling edge of SCLK.

CFR default values are all 1s (except for CFR\_D1 on the ADS7279; this bit is ignored by the device and is always read as a '0'). The same default values apply for the CFR after a power-on reset (POR) and software reset.

### READING THE CONFIGURATION REGISTER

The host processor can read back the value programmed in the CFR by issuing command 1100b. The timing is similar to reading a conversion result, except that  $\overline{\text{CONVST}}$  is not used and there is no activity on the EOC/ $\overline{\text{INT}}$  pin. The CFR value read back contains the first four MSBs of conversion data plus valid 12-bit CFR contents. Table 4 shows the Configuration Register Map.

**Table 4. Configuration Register (CFR) Map**

SDI BIT	DEFINITION	
CFR - D[11 - 0]		
D11 default = 1	Channel select mode	
	0: Manual channel select enabled. Use channel select commands to access a different channel.	1: Auto channel select enabled. All channels are sampled and converted sequentially until the cycle after this bit is set to 0.
D10 default = 1	Conversion clock (CCLK) source select	
	0: Conversion clock (CCLK) = SCLK/2	1: Conversion clock (CCLK) = Internal OSC
D9 default = 1	Trigger (conversion start) select: start conversion at the end of sampling (EOS). If D9 = 0, the D4 setting is ignored.	
	0: Auto trigger automatically starts (4 internal clocks after EOC inactive)	1: Manual trigger manually started by falling edge of $\overline{\text{CONVST}}$
D8 default = 1	Don't care	
D7 default = 1	Pin 10 polarity select when used as an output (EOC/ $\overline{\text{INT}}$ )	
	0: EOC Active high / $\overline{\text{INT}}$ active high	1: EOC active low / $\overline{\text{INT}}$ active low
D6 default = 1	Pin 10 function select when used as an output (EOC/ $\overline{\text{INT}}$ )	
	0: Pin used as $\overline{\text{INT}}$	1: Pin used as EOC
D5 default = 1	Pin 10 I/O select for chain mode operation	
	0: Pin 10 is used as CDI input (chain mode enabled)	1: Pin 10 is used as EOC/ $\overline{\text{INT}}$ output
D4 default = 1	Auto nap power-down enable/disable (mid voltage and comparator shut down between cycles). This bit setting is ignored if D9 = 0.	
	0: Auto nap power-down enabled (not activated)	1: Auto nap power-down disabled
D3 default = 1	Nap power-down (mid voltage and comparator shut down between cycles). This bit is set to 1 automatically by wake-up command.	
	0: Enable/activate device in nap power-down	1: Remove device from nap power-down (resume)
D2 default = 1	Deep power-down. This bit is set to 1 automatically by wake-up command.	
	0: Enable/activate device in deep power-down	1: Remove device from deep power-down (resume)
D1 default = 0: ADS7279 1: ADS7280	TAG bit enable. This bit is ignored by the ADS7279 and is always read 0.	
	0: TAG bit disabled.	1: TAG bit output enabled. TAG bit appears at the 17th SCLK.
D0 default = 1	Reset	
	0: System reset	1: Normal operation

## READING CONVERSION RESULT

The conversion result is available to the input of the output data register (ODR) at EOC and presented to the output of the output register at the next falling edge of  $\overline{CS}$  or FS. The host processor can then shift the data out via the SDO pin any time except during the quiet zone. This quiet zone is 20ns before and 20ns after the end of sampling (EOS) period. In the quiet zone the FS/ $\overline{CS}$  should be high, to avoid performance loss when switching from sampling-mode to hold-mode. End of sampling (EOS) is defined as the falling edge of  $\overline{CONVST}$  when manual trigger is used or the end of the third conversion clock (CCLK) after EOC if auto trigger is used.

The falling edge of FS/ $\overline{CS}$  should not be placed at the precise moment of the end of a conversion; otherwise, the data may be corrupt. There must be a minimum of at least one conversion clock (CCLK) delay at the end of a conversion. If FS/ $\overline{CS}$  is placed before the end of a conversion, the previous conversion result is read. If FS/ $\overline{CS}$  is placed after the end of a conversion, the current conversion result is read.

The conversion result is 14-bit data in straight binary format as shown in Table 5. Generally, 14 SCLKs are necessary, but there are exceptions where more than 14 SCLKs are required (see Table 6). Data output from the serial output (SDO) is left-adjusted, MSB first. The 14-bit conversion result is followed by '00', the TAG bit (if enabled), and additional zeros. SDO remains low until FS/ $\overline{CS}$  is brought high again.

**Table 5. Ideal Input Voltages and Output Codes**

DESCRIPTION	ANALOG VALUE	DIGITAL OUTPUT	
		STRAIGHT BINARY	
Full-scale range	$V_{REF}$		
Least significant bit (LSB)	$V_{REF}/16384$	<b>BINARY CODE</b>	<b>HEX CODE</b>
Full-scale	$+V_{REF} - 1LSB$	11 1111 1111 1111	3FFF
Midscale	$V_{REF}/2$	10 0000 0000 0000	2000
Midscale – 1LSB	$V_{REF}/2 - 1LSB$	01 1111 1111 1111	1FFF
Zero	0 V	00 0000 0000 0000	0000

SDO is active when FS/ $\overline{CS}$  is low. The rising edge of FS/ $\overline{CS}$  3-states the SDO output.

### NOTE:

Whenever SDO is not in 3-state mode (that is, when FS/ $\overline{CS}$  is low), a portion of the conversion result is output at the SDO pin. The number of bits depends on how many SCLKs are supplied. For example, a manual select channel command cycle requires 4 SCLKs; therefore, 4MSBs of the conversion result are output at SDO. The exception is that SDO outputs all 1s during the cycle immediately after any reset (POR or software reset).

If SCLK is used as the conversion clock (CCLK) and a continuous SCLK is used, it is not possible to clock out all 14 SDO bits during the sampling time (6 SCLKs) because of the quiet zone requirement. In this case, it is better to read the conversion result during the conversion time (36 SCLKs or 48 SCLKs in Auto nap mode).

### TAG Mode

The ADS7280 includes a feature, TAG, that can be used as a tag to indicate which channel sourced the converted result. An address bit is added after the LSB read out from SDO that indicates which channel the result came from if TAG mode is enabled. This address bit is '0' for channel 0 and '1' for channel 1. The converter requires more than the 16 SCLKs that are required for a 4-bit command plus 12-bit CFR or 14 data bits followed by '00' because of the additional TAG bit.

### Chain Mode

The ADS7279/80 can operate as a single converter or in a system with multiple converters. System designers can take advantage of the simple, high-speed, SPI-compatible serial interface by cascading the devices in a daisy-chain when multiple converters are used. A bit in the CFR is used to reconfigure the EOC/ $\overline{INT}$  status pin as a secondary serial data input, chain data input (CDI), for the conversion result from an upstream converter. This configuration is chain mode operation. A typical connection of three converters is shown in Figure 61.

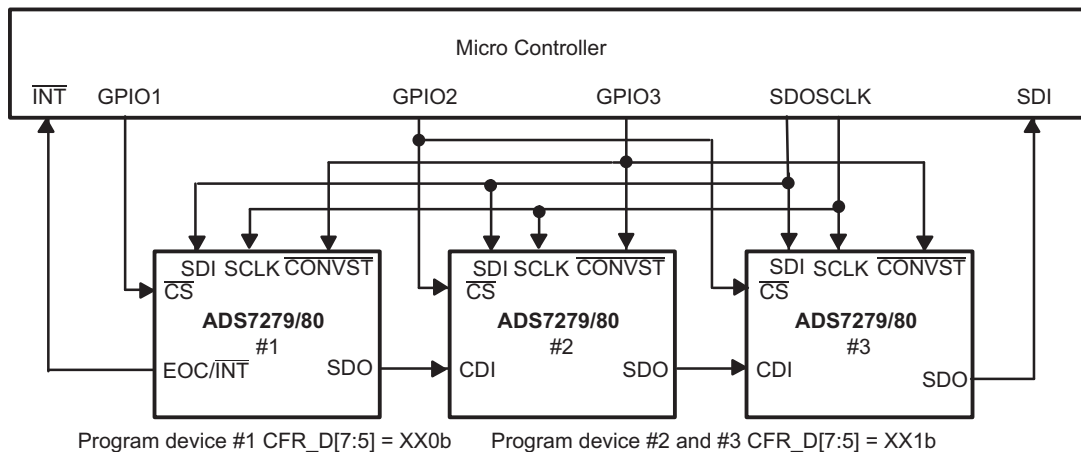


Figure 61. Multiple Converters Connected Using Chain Mode

When multiple converters are used in daisy-chain mode, the first converter is configured in regular mode while the other converters are configured in chain mode. When a converter is configured in chain mode, the CDI input data go straight to the output register; therefore, the serial input data passes through the converter with a 16 SCLK (if the TAG feature is disabled) or a 24 SCLK delay, as long as CS is active. Figure 62 shows a detailed timing diagram. In this timing, the conversions in each converter are performed simultaneously.

Cascaded Manual Trigger/Read While Sampling  
(Use internal CCLK, EOC, and INT programmed as active low)  
CS held low during the N times 16 bits transfer cycle

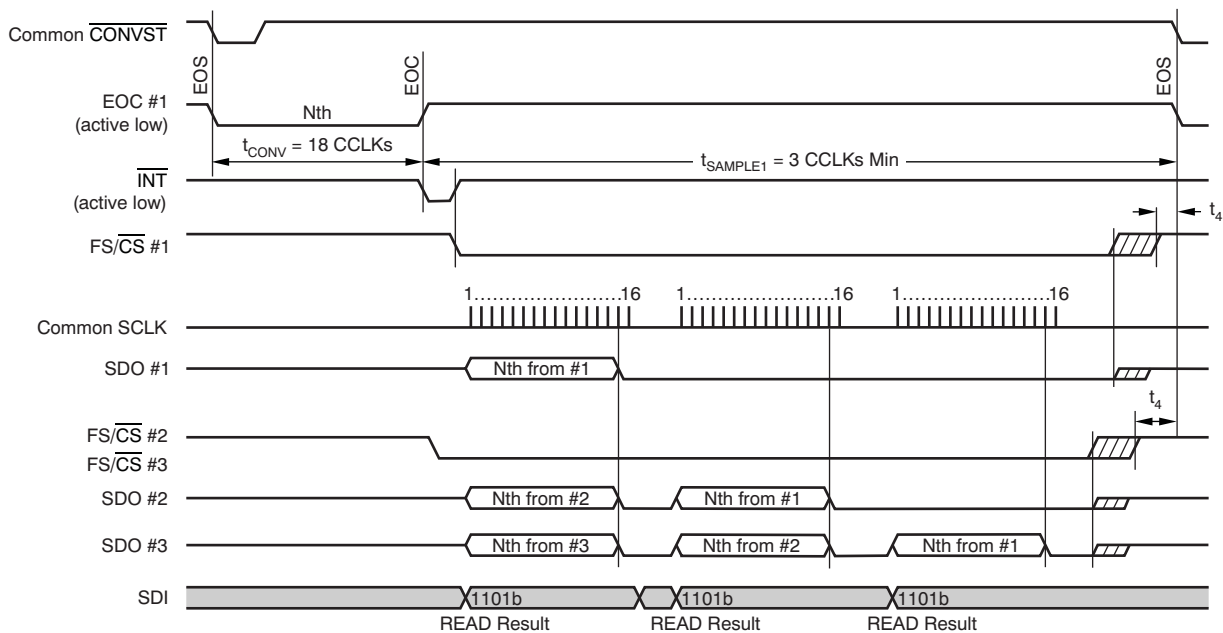


Figure 62. Simplified Cascade Mode Timing with Shared CONVST and Continuous CS

Care must be given to handle the multiple CS signals when the converters operate in daisy-chain mode. The different chip select signals must be low for the entire data transfer (in this example, 48 bits for three converters). The first 16-bit word after the falling chip select is always the data from the chip that received the chip select signal.

Case 1: If chip select is not toggled ( $\overline{CS}$  stays low), the next 16 bits are data from the upstream converter, and so on. This configuration is shown in Figure 62. If there is no upstream converter in the chain, as with converter #1 in the example, the same data from the converter are going to be shown repeatedly.

Case 2: If the chip select is toggled during a chain mode data transfer cycle, as illustrated in Figure 63, the same data from the converter are read out again and again in all three discrete 16-bit cycles. This result is not a desired outcome.

Cascaded Manual Trigger/Read While Sampling  
(Use internal CCLK, EOC, and  $\overline{INT}$  programmed as active low)

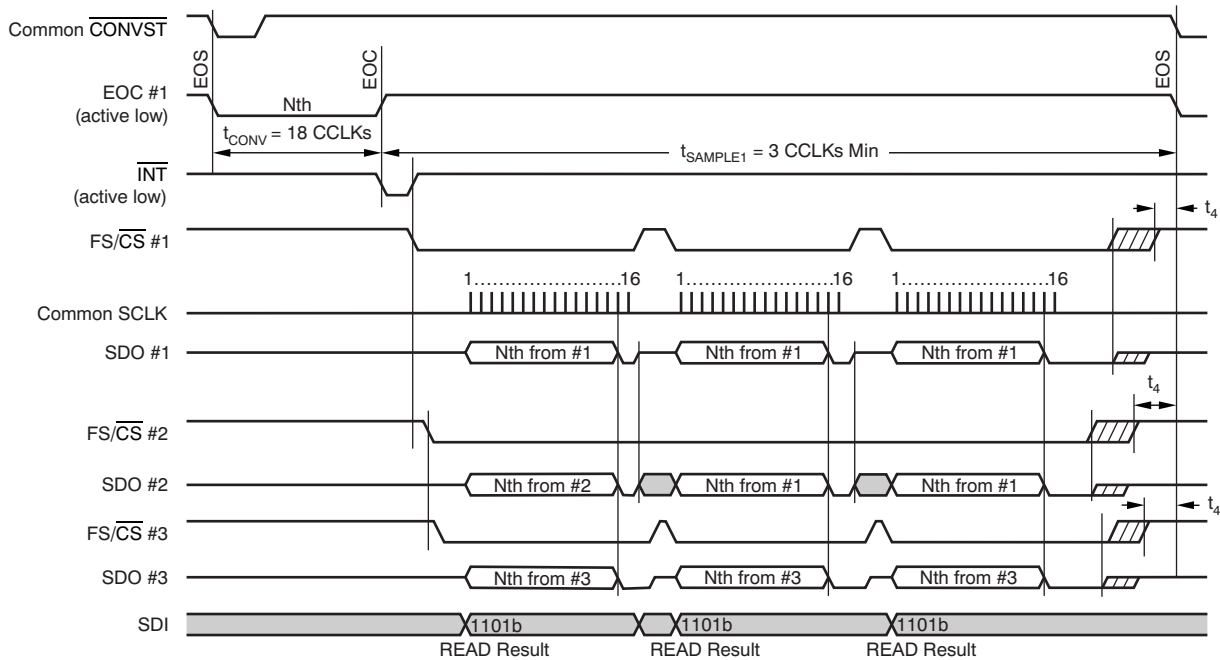


Figure 63. Simplified Cascade Mode Timing with Shared  $\overline{CONVST}$  and Discrete  $\overline{CS}$

Figure 64 shows a slightly different scenario where  $\overline{\text{CONVST}}$  is not shared by the second converter. Converters #1 and #3 have the same  $\overline{\text{CONVST}}$  signal. In this case, converter #2 simply passes the previous conversion data downstream.

Cascaded Manual Trigger/Read While Sampling  
(Use internal CCLK, EOC, and INT programmed as active low)  
CS held low during the N times 16 bits transfer cycle

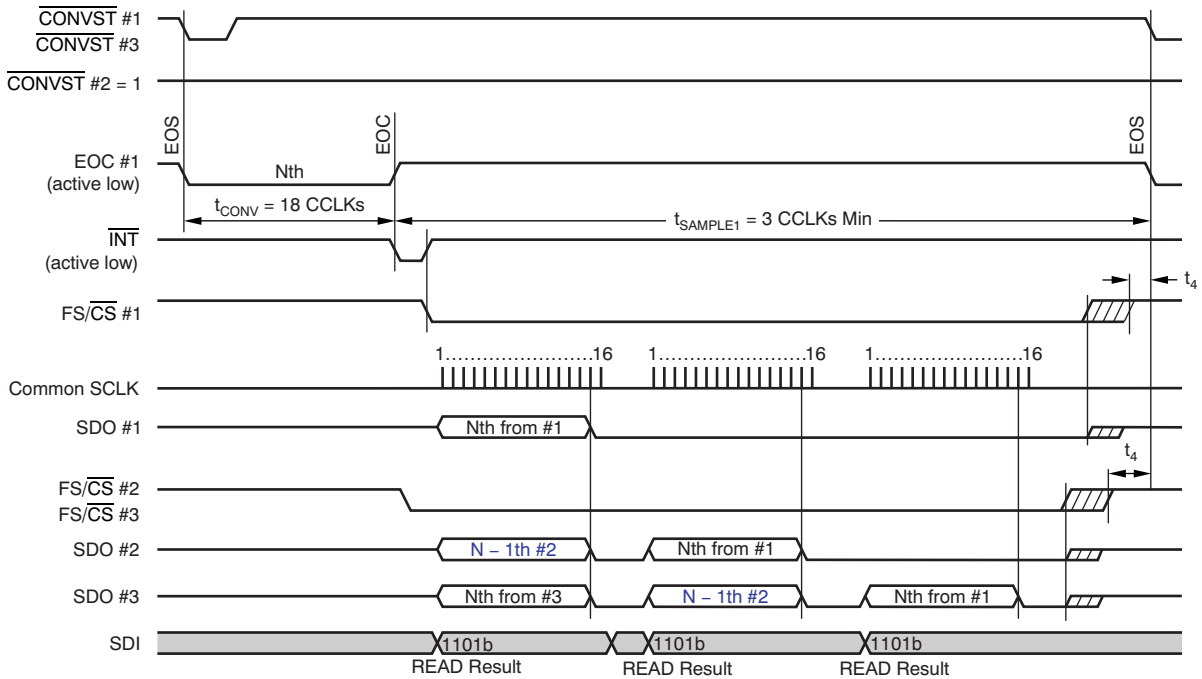


Figure 64. Simplified Cascade Timing (Separate  $\overline{\text{CONVST}}$ )

The number of SCLKs required for a serial read cycle depends on the combination of different read modes, TAG bit, chain mode, and the way a channel is selected (that is, auto channel select). These possible configurations are listed in Table 6.

Table 6. Required SCLKs For Different Read-Out Mode Combinations

CHAIN MODE ENABLED CFR.D5	AUTO CHANNEL SELECT CFR.D11	TAG ENABLED CFR.D1	NUMBER OF SCLK PER SPI READ	TRAILING BITS
0	0	0	14	None
0	0	1	$\geq 17$	MSB is TAG bit plus zero(s)
0	1	0	14	None
0	1	1	$\geq 17$	TAG bit plus seven zeros
1	0	0	16	None
1	0	1	24	TAG bit plus seven zeros
1	1	0	16	None
1	1	1	24	TAG bit plus seven zeros

SCLK skew between converters and data path delay through the converters configured in chain mode can affect the maximum frequency of SCLK. The delay can also be affected by supply voltage and loading. It may be necessary to slow down the SCLK when the devices are configured in chain mode. Figure 65 shows a typical delay process through multiple converters linked in daisy-chain mode.

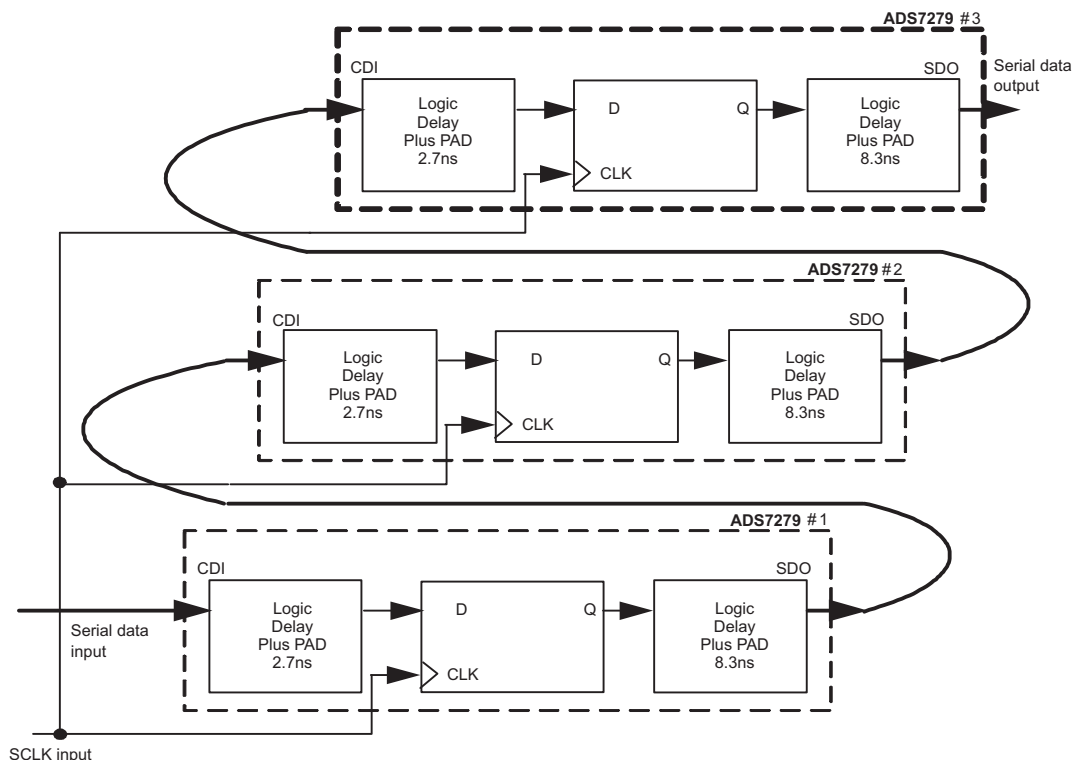


Figure 65. Typical Delay Through Converters Configured in Chain Mode

## RESET

The converter has two reset mechanisms: a power-on reset (POR) and a software reset using CFR\_D0. These two mechanisms are NOR-ed internally. When a reset (software or POR) is issued, all register data are set to the default values (all 1s) and the SDO output (during the cycle immediately after reset) is set to all 1s. The state machine is reset to the power-on state. Figure 66 illustrates the digital output under a reset condition.

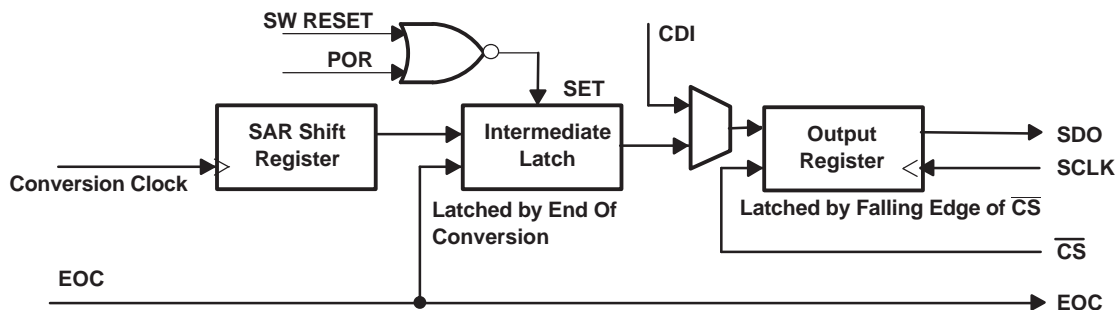


Figure 66. Digital Output Under Reset Condition

When the device is powered up, the POR sets the device to default mode when AVDD reaches 1.5V. When the device is powered down, the POR circuit requires AVDD to remain below 125mV for at least 350ms to ensure proper discharging of internal capacitors and to correct the behavior of the ADC when powered up again. If AVDD drops below 400mV but remains above 125mV, the internal POR capacitor does not discharge fully and the device requires a software reset to perform correctly after the recovery of AVDD (this condition is shown as the *undefined zone* in Figure 67).

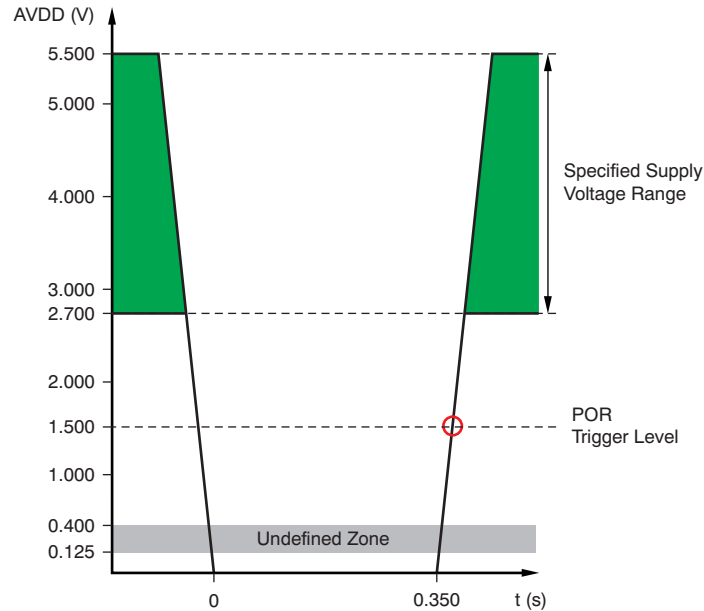


Figure 67. Relevant Voltage Levels for POR

## APPLICATION INFORMATION

### TYPICAL CONNECTION

Figure 68 shows a typical circuit configuration for the device.

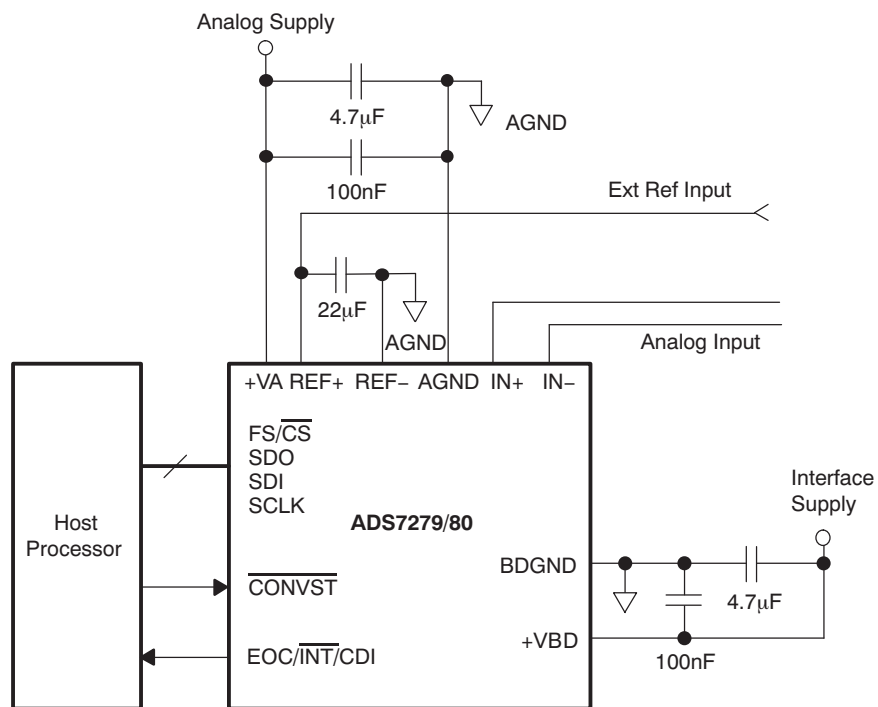


Figure 68. Typical Circuit Configuration

## Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (May 2008) to Revision A	Page
• Added +REF to AGND and –REF to AGND specifications to voltage range section of <i>Absolute Maximum Ratings</i> table..	2
• Changed conditions of the 5V <i>Electrical Characteristics</i> to include +VA = 4.5V to 5.5V .....	3
• Changed conditions of the 5V <i>Electrical Characteristics</i> to include +VA = 4.5V to 5.5V .....	4
• Deleted typical specification for V <sub>REF</sub> [REF+ – (REF–)] input reference range in the External Voltage Reference Input section of the 5V <i>Electrical Characteristics</i> .....	4
• Changed test condition of PD mode, <i>supply current</i> row of the Power-Supply Requirements section of the 5V <i>Electrical Characteristics</i> .....	4
• Changed the V <sub>REF</sub> rows of the External Voltage Reference Input section of the 2.5V <i>Electrical Characteristics</i> .....	6
• Changed test condition of PD mode, <i>supply current</i> row of the Power-Supply Requirements section of the 2.5V <i>Electrical Characteristics</i> .....	7
• Corrected typo in <a href="#">Figure 2</a> .....	12
• Corrected typo in <a href="#">Figure 3</a> .....	13
• Corrected typo in <a href="#">Figure 5</a> .....	14
• Added last sentence to the <i>Driver Amplifier Choice</i> section.....	24
• Updated <a href="#">Figure 54</a> .....	24
• Updated <a href="#">Figure 55</a> .....	24
• Changed fifth sentence of <i>Deep Power-Down Mode</i> section .....	27
• Added supply current value to Auto-nap power-down row of <a href="#">Table 2</a> .....	28
• Added <a href="#">Figure 67</a> and corresponding paragraph to the <i>RESET</i> section .....	37

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS7279IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7279I A	<a href="#">Samples</a>
ADS7279IPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7279I A	<a href="#">Samples</a>
ADS7279IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7279I A	<a href="#">Samples</a>
ADS7279IPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7279I A	<a href="#">Samples</a>
ADS7279IRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7279I A	<a href="#">Samples</a>
ADS7279IRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7279I A	<a href="#">Samples</a>
ADS7280IPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7280I A	<a href="#">Samples</a>
ADS7280IPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7280I A	<a href="#">Samples</a>
ADS7280IRSAR	ACTIVE	QFN	RSA	16	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7280I A	<a href="#">Samples</a>
ADS7280IRSAT	ACTIVE	QFN	RSA	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS 7280I A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

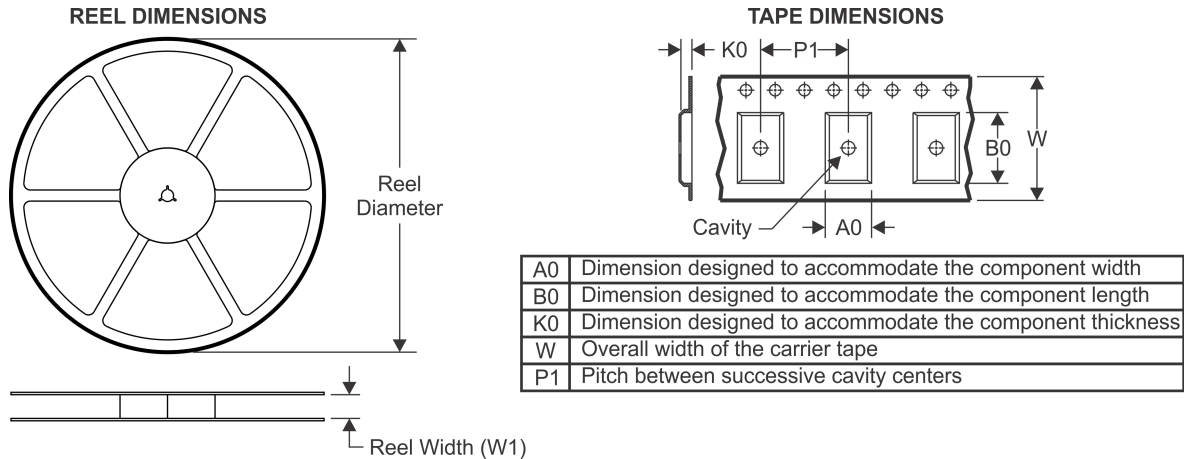
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7279IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS7279IRSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ADS7279IRSAT	QFN	RSA	16	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ADS7280IPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS7280IRSAR	QFN	RSA	16	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
ADS7280IRSAT	QFN	RSA	16	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

## TAPE AND REEL BOX DIMENSIONS

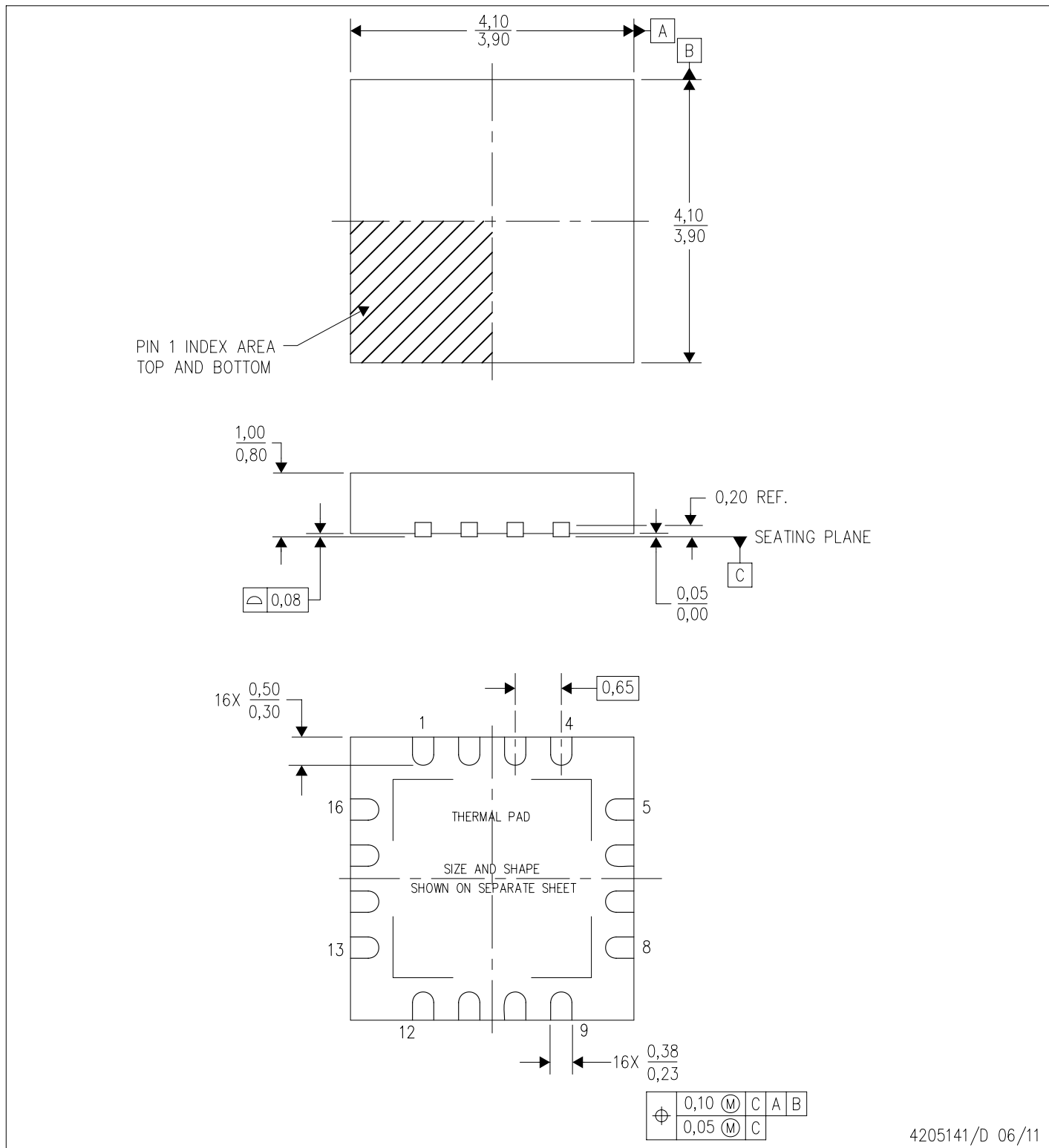


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7279IPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
ADS7279IRSAR	QFN	RSA	16	3000	350.0	350.0	43.0
ADS7279IRSAT	QFN	RSA	16	250	210.0	185.0	35.0
ADS7280IPWR	TSSOP	PW	16	2000	350.0	350.0	43.0
ADS7280IRSAR	QFN	RSA	16	3000	350.0	350.0	43.0
ADS7280IRSAT	QFN	RSA	16	250	210.0	185.0	35.0

RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



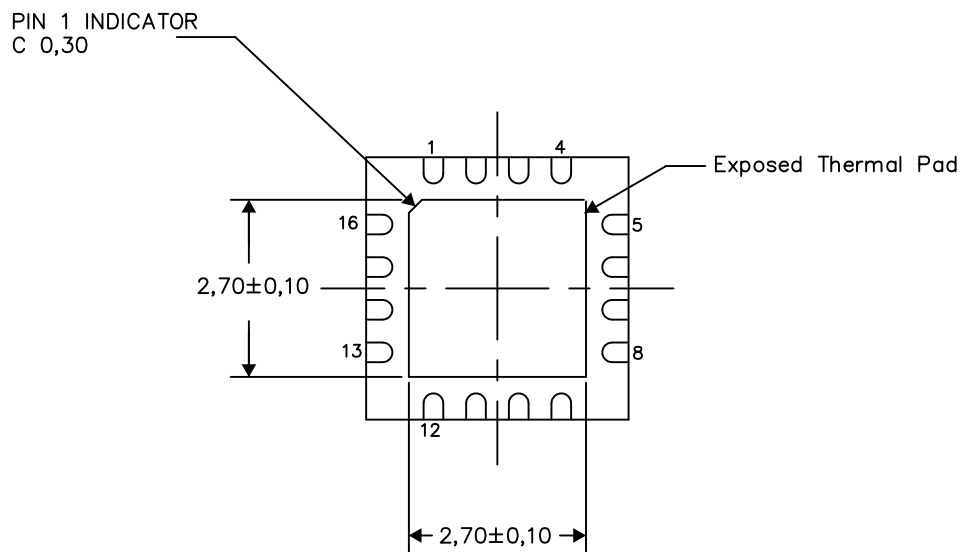
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Quad Flatpack, No-leads (QFN) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Falls within JEDEC MO-220.

## THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

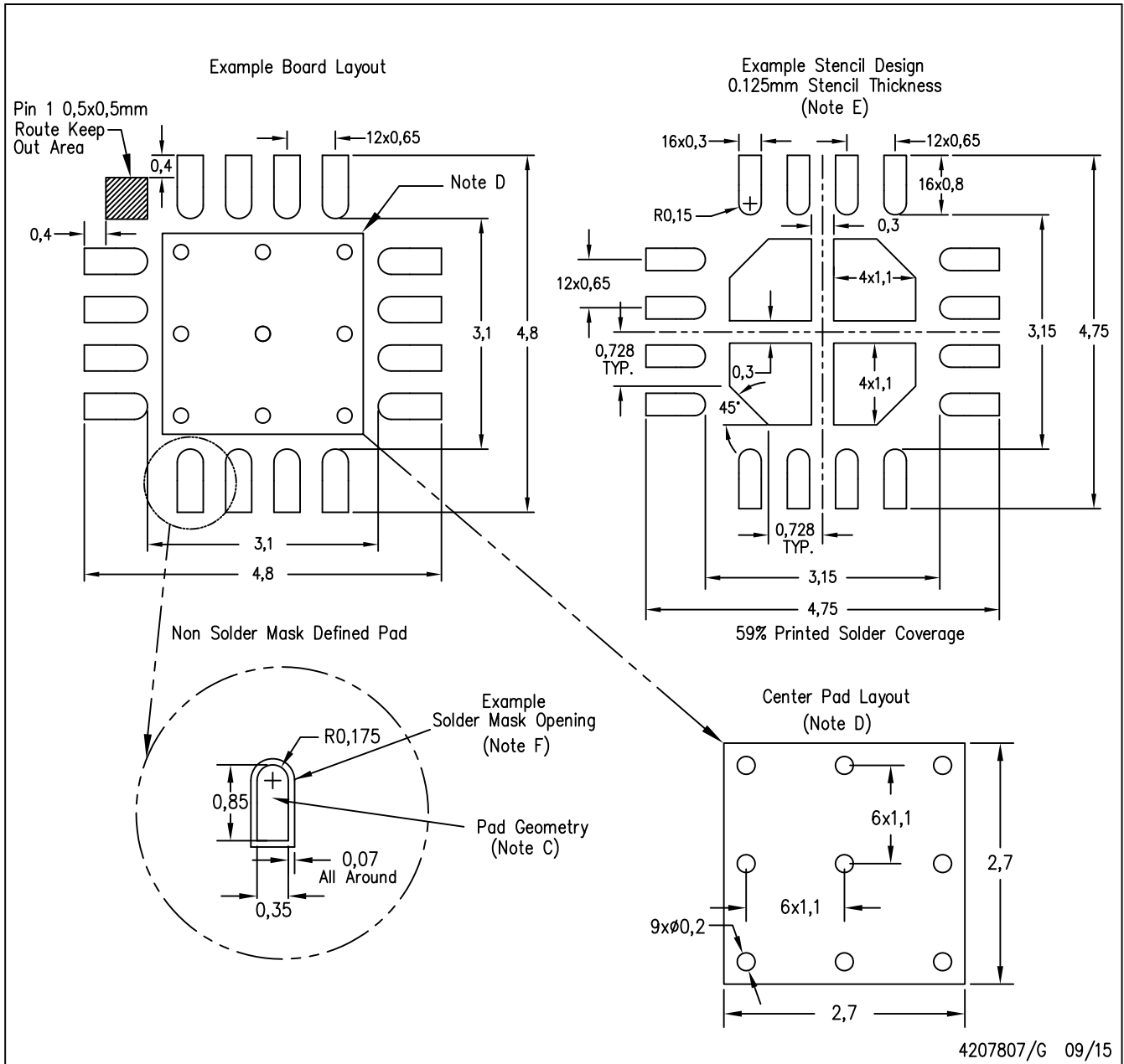
4206364-2/0 09/15

### NOTES:

- A. All linear dimensions are in millimeters

RSA (S-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4207807/G 09/15

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for solder mask tolerances.



# EXAMPLE BOARD LAYOUT

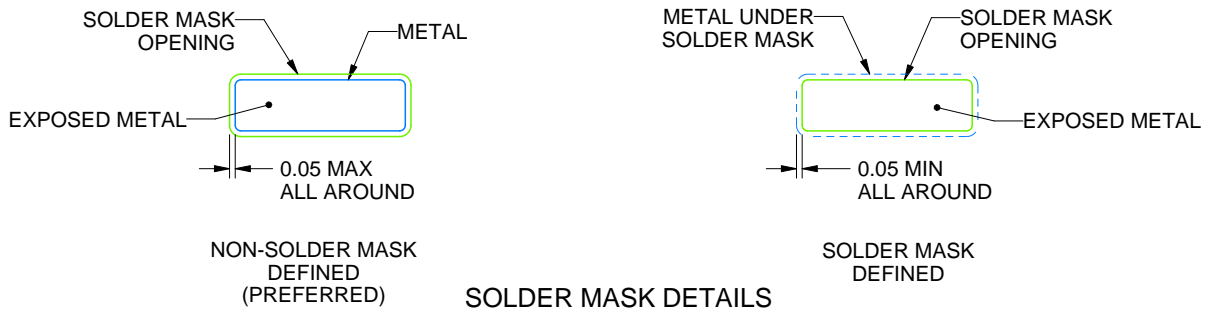
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

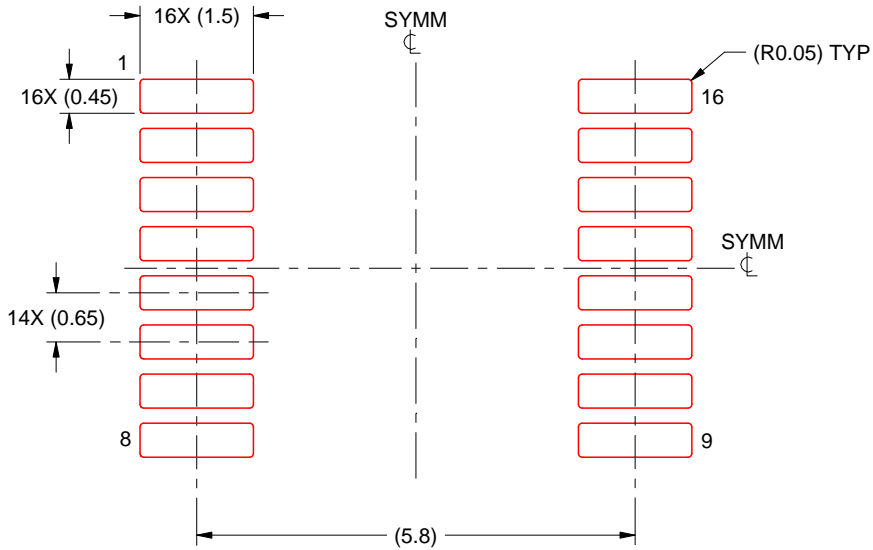
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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