



**THE DATASHEET OF  
ADS6144IRHBT**



## 14-BITS, 125/105/80/65 MSPS ADC WITH DDR LVDS/CMOS OUTPUTS

### FEATURES

- **Maximum Sample Rate: 125 MSPS**
- **14-Bit Resolution with No Missing Codes**
- **3.5 dB Coarse Gain and up to 6 dB Programmable Fine Gain for SNR/SFDR Trade-Off**
- **Parallel CMOS and Double Data Rate (DDR) LVDS Output Options**
- **Supports Sine, LVCMOS, LVPECL, LVDS Clock Inputs, and Clock Amplitude Down to 400 mV<sub>PP</sub>**
- **Clock Duty Cycle Stabilizer**
- **Internal Reference with Support for External Reference**
- **No External Decoupling Required for References**
- **Programmable Output Clock Position and Drive Strength to Ease Data Capture**
- **3.3-V Analog and 1.8-V to 3.3-V Digital Supply**
- **32-QFN Package (5 mm × 5 mm)**
- **Pin Compatible 12-Bit Family (ADS612X)**

### APPLICATIONS

- **Wireless Communications Infrastructure**
- **Software Defined Radio**
- **Power Amplifier Linearization**
- **802.16d/e**
- **Test and Measurement Instrumentation**
- **High Definition Video**
- **Medical Imaging**

- **Radar Systems**

### DESCRIPTION

ADS6145/ADS6144/ADS6143/ADS6142 (ADS614X) are a family of 14-bit A/D converters with sampling frequencies up to 125 MSPS. The high performance and low power consumption of the ADS614X are combined in a compact 32 QFN package. An internal high bandwidth sample and hold and a low jitter clock buffer help to achieve high SNR and high SFDR even at high input frequencies.

The ADS614X feature coarse and fine gain options to improve SFDR performance at lower full-scale analog input ranges.

The digital data outputs are either parallel CMOS or DDR (Double Data Rate) LVDS. Several features exist to ease data capture such as — controls for output clock position and output buffer drive strength, LVDS current, and internal termination programmability.

The output interface type, gain, and other functions are programmed using a 3-wire serial interface. Alternatively, some functions are configured using dedicated parallel pins so the device powers up to the desired state.

The ADS614X include internal references while eliminating traditional reference pins and associated external decoupling. External reference mode is also supported.

The ADS614X are specified over the industrial temperature range (–40°C to 85°C).

**ADS614X Performance Summary**

		<b>ADS6145</b>	<b>ADS6144</b>	<b>ADS6143</b>	<b>ADS6142</b>
<b>SFDR, dBc</b>	$F_{in} = 10$ MHz (0 dB gain)	90	91	93	95
	$F_{in} = 170$ MHz (3.5 dB gain)	78	82	83	84
<b>SINAD, dBFS</b>	$F_{in} = 10$ MHz (0 dB gain)	73.7	74.1	74.5	74.6
	$F_{in} = 170$ MHz (3.5 dB gain)	68.6	70.5	70.6	71.5
<b>Power, mW</b>		417	374	318	285

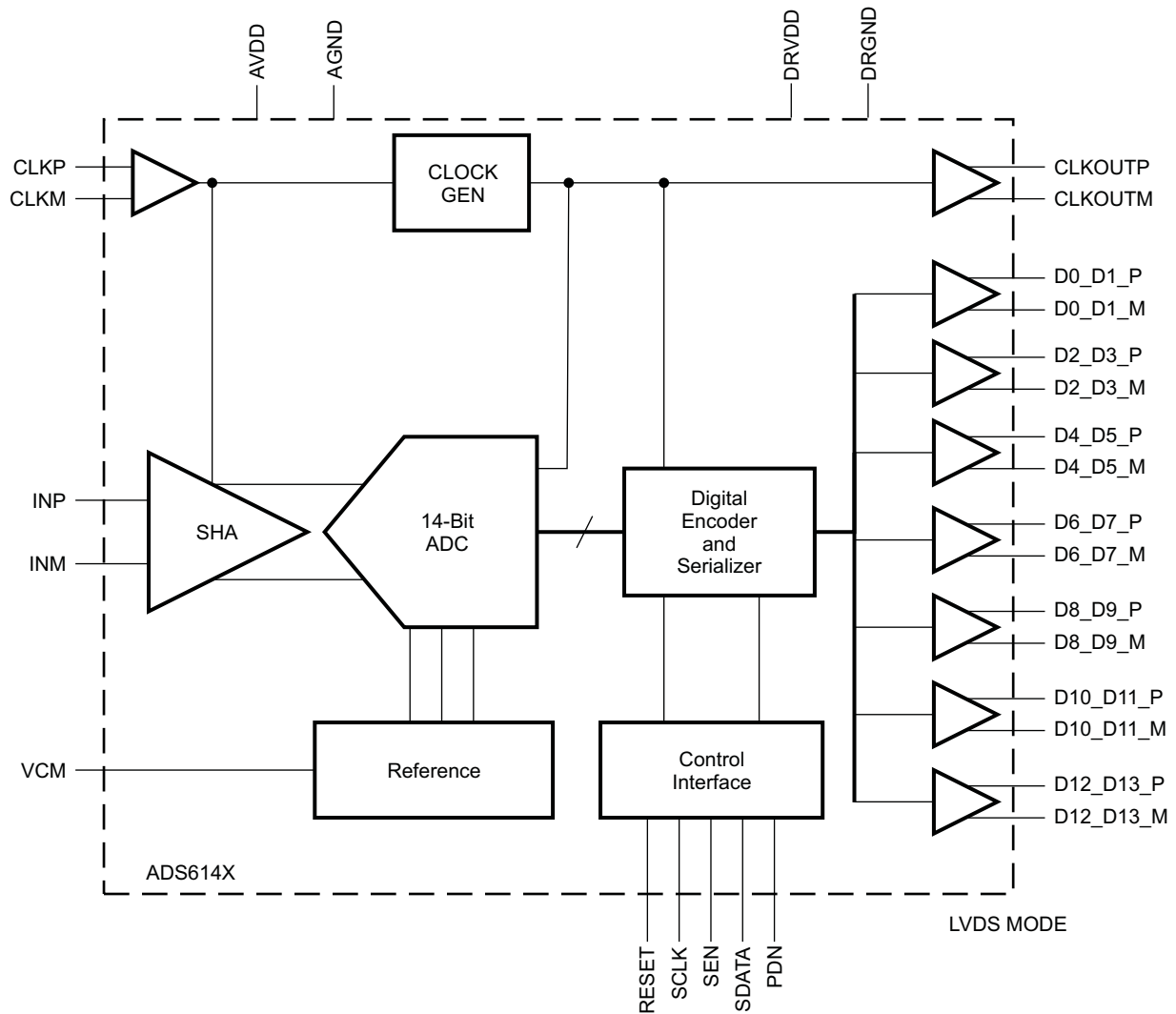


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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.



**ADS61XX FAMILY**

	<b>125 MSPS</b>	<b>105 MSPS</b>	<b>80 MSPS</b>	<b>65 MSPS</b>
<b>ADS614X</b> 14 Bits	ADS6145	ADS6144	ADS6143	ADS6142
<b>ADS612X</b> 12 Bits	ADS6125	ADS6124	ADS6123	ADS6122

**PACKAGE/ORDERING INFORMATION<sup>(1)</sup>**

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA
ADS6145	QFN-32 <sup>(2)</sup>	RHB	–40°C to 85°C	AZ6145	ADS6145IRHBT	Tape and Reel, small
					ADS6145IRHBR	Tape and Reel, large
ADS6144	QFN-32 <sup>(2)</sup>	RHB	–40°C to 85°C	AZ6144	ADS6144IRHBT	Tape and Reel, small
					ADS6144IRHBR	Tape and Reel, large
ADS6143	QFN-32 <sup>(2)</sup>	RHB	–40°C to 85°C	AZ6143	ADS6143IRHBT	Tape and Reel, small
					ADS6143IRHBR	Tape and Reel, large
ADS6142	QFN-32 <sup>(2)</sup>	RHB	–40°C to 85°C	AZ6142	ADS6142IRHBT	Tape and Reel, small
					ADS6142IRHBR	Tape and Reel, large

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at [www.ti.com](http://www.ti.com).
- (2) For thermal pad size on the package, see the mechanical drawings at the end of this data sheet.  $\theta_{JA} = 34 \text{ }^\circ\text{C/W}$  (0 LFM air flow),  $\theta_{JC} = 30 \text{ }^\circ\text{C/W}$  when used with 2 oz. copper trace and pad soldered directly to a JEDEC standard four layer 3 in × 3 in (7.62 cm × 7.62 cm) PCB.

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

		VALUE	UNIT
$V_I$	Supply voltage range, AVDD	–0.3 to 3.9	V
	Supply voltage range, DRVDD	–0.3 to 3.9	V
	Voltage between AGND and DRGND	–0.3 to 0.3	V
	Voltage between AVDD to DRVDD	–0.3 to 3.3	V
	Voltage applied to VCM pin (in external reference mode)	–0.3 to 2	V
	Voltage applied to analog input pins, INP and INM	–0.3 to minimum ( 3.6, AVDD + 0.3)	V
	Voltage applied to analog input pins, CLKP and CLKM	–0.3 to (AVDD + 0.3)	V
$T_A$	Operating free-air temperature range	–40 to 85	°C
$T_J$	Operating junction temperature range	125	°C
$T_{stg}$	Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT		
<b>SUPPLIES</b>							
AVDD	Analog supply voltage	3	3.3	3.6	V		
DRVDD	Output buffer supply voltage <sup>(1)</sup>	CMOS Interface		1.65	1.8 to 3.3	3.6	V
		LVDS Interface		3	3.3	3.6	V
<b>ANALOG INPUTS</b>							
Differential input voltage range		2			V <sub>pp</sub>		
V <sub>IC</sub>	Input common-mode voltage	1.5 ± 0.1			V		
Voltage applied on VCM in external reference mode		1.45	1.5	1.55	V		
<b>CLOCK INPUT</b>							
Input clock sample rate, F <sub>S</sub>	ADS6145	1		125	MSPS		
	ADS6144	1		105			
	ADS6143	1		80			
	ADS6142	1		65			
Input clock amplitude differential (V <sub>CLKP</sub> – V <sub>CLKM</sub> )	Sine wave, ac-coupled	0.4	1.5		V <sub>pp</sub>		
	LVPECL, ac-coupled	± 0.8					
	LVDS, ac-coupled	± 0.35					
	LVC MOS, ac-coupled	3.3					
Input Clock duty cycle		35%	50%	65%			
<b>DIGITAL OUTPUTS</b>							
Output buffer drive strength <sup>(2)</sup>	For C <sub>LOAD</sub> ≤ 5 pF and DRVDD ≥ 2.2 V		DEFAULT strength				
	For C <sub>LOAD</sub> > 5 pF and DRVDD ≥ 2.2 V		MAXIMUM strength				
	For DRVDD < 2.2 V		MAXIMUM strength				
C <sub>LOAD</sub>	Maximum external load capacitance from each output pin to DRGND		CMOS Interface, maximum buffer strength		pF		
			LVDS Interface, without internal termination				
			LVDS Interface, with internal termination				
R <sub>LOAD</sub>	Differential load resistance (external) between the LVDS output pairs		100		Ω		
T <sub>A</sub>	Operating free-air temperature		-40		85 °C		

(1) For easy migration to next generation, higher sampling speed devices (> 125 MSPS), use 1.8V DRVDD supply.

(2) See [Output Buffer Strength Programmability](#) in the application section.

## ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ ,  $AVDD = DRVDD = 3.3\text{ V}$ , maximum rated sampling frequency, 50% clock duty cycle,  $-1\text{ dBFS}$  differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

PARAMETER	ADS6145 $F_S = 125\text{ MSPS}$			ADS6144 $F_S = 105\text{ MSPS}$			ADS6143 $F_S = 80\text{ MSPS}$			ADS6142 $F_S = 65\text{ MSPS}$			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION	14			14			14			14			Bits
<b>ANALOG INPUT</b>													
Differential input voltage range	2			2			2			2			$V_{PP}$
Differential input resistance (dc), see Figure 94	> 1			> 1			> 1			> 1			$M\Omega$
Differential input capacitance, see Figure 95	7			7			7			7			pF
Analog input bandwidth	450			450			450			450			MHz
Analog input common-mode current (per input pin of each ADC)	180			151			114			92			$\mu\text{A}$
<b>REFERENCE VOLTAGES</b>													
VREFB Internal reference bottom voltage	1			1			1			1			V
VREFT Internal reference top voltage	2			2			2			2			V
$\Delta V_{REF}$ Internal reference error (VREFT–VREFB)	-20	$\pm 5$	20	-20	$\pm 5$	20	-20	$\pm 5$	20	-20	$\pm 5$	20	mV
$V_{CM}$ Common-mode output voltage	1.5			1.5			1.5			1.5			V
$V_{CM}$ Output current capability	4			4			4			4			mA
<b>DC ACCURACY</b>													
No missing codes	Specified			Specified			Specified			Specified			
$E_O$ Offset error	-10	$\pm 2$	10	-10	$\pm 2$	10	-10	$\pm 2$	10	-10	$\pm 2$	10	mV
Offset error temperature coefficient	0.05			0.05			0.05			0.05			$\text{mV}/^{\circ}\text{C}$
There are two sources of gain error – internal reference inaccuracy and channel gain error													
$E_{GREF}$ Gain error due to internal reference inaccuracy alone, ( $\Delta V_{REF}/2$ ) %	-1	0.25	1	-1	0.25	1	-1	0.25	1	-1	0.25	1	% FS
$E_{GCHAN}$ Gain error of channel alone <sup>(1)</sup>	-1	$\pm 0.3$	1	-1	$\pm 0.3$	1	-1	$\pm 0.3$	1	-1	$\pm 0.3$	1	% FS
Channel gain error temperature coefficient	0.005			0.005			0.005			0.005			$\Delta\%/^{\circ}\text{C}$
DNL Differential nonlinearity	-0.95	$\pm 0.6$	2	-0.95	$\pm 0.6$	2	-0.95	$\pm 0.5$	2	-0.95	$\pm 0.5$	2	LSB
INL Integral nonlinearity	-4.5	$\pm 2.5$	4.5	-4.5	$\pm 2.5$	4.5	-4	$\pm 2$	4	-4	$\pm 2$	4	LSB
<b>POWER SUPPLY</b>													
$I_{AVDD}$ Analog supply current	123			110			94			84			mA
$I_{DRVDD}$ Digital supply current, CMOS interface, $DRVDD = 1.8\text{ V}$ , No load capacitance, $F_{in} = 2\text{ MHz}$ <sup>(2)</sup>	6.1			5.4			4.5			4.0			mA
$I_{DRVDD}$ Digital supply current, LVDS interface, $DRVDD = 3.3\text{ V}$ , with 100- $\Omega$ external termination	42			42			42			42			mA
Total power, CMOS, $DRVDD = 3.3\text{ V}$ <sup>(3)</sup>	417	625		374	525		318	440		285	400		mW
Global power down	30	60		30	60		30	60		30	60		mW

(1) Specified by design and characterization; not tested in production.

(2) In CMOS mode, the  $DRVDD$  current scales with the sampling frequency and the load capacitance on the output pins (see Figure 87).

(3) The maximum  $DRVDD$  current depends on the actual load capacitance on the digital output lines. Note that the maximum recommended load capacitance is 10 pF.

## ELECTRICAL CHARACTERISTICS

Typical values are at 25°C, min and max values are across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ ,  $AVDD = DRVDD = 3.3\text{ V}$ , maximum rated sampling frequency, 50% clock duty cycle,  $-1\text{ dBFS}$  differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS6145 $F_S = 125\text{ MSPS}$			ADS6144 $F_S = 105\text{ MSPS}$			ADS6143 $F_S = 80\text{ MSPS}$			ADS6142 $F_S = 65\text{ MSPS}$			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
<b>DYNAMIC AC CHARACTERISTICS</b>															
SNR Signal-to-noise ratio, <b>CMOS</b>	$F_{in} = 10\text{ MHz}$	73.9			74.3			74.6			74.7			dBFS	
	$F_{in} = 50\text{ MHz}$	70	73.7		73.7			71	74.2		74.4				
	$F_{in} = 70\text{ MHz}$	73.3			70	73.9		74.1			71	74.4			
	$F_{in} = 170\text{ MHz}$	0 dB Gain	71.1			71.8			72.3			72.7			
		3.5 dB Coarse gain	70.1			70.9			71.4			71.8			
	$F_{in} = 230\text{ MHz}$	0 dB Gain	69.8			70.7			71.3			71.7			
3.5 dB Coarse gain		69			69.9			70.4			70.9				
SNR Signal-to-noise ratio, <b>LVDS</b>	$F_{in} = 10\text{ MHz}$	74.5			74.4			74.9			75			dBFS	
	$F_{in} = 50\text{ MHz}$	70.5	74.4		73.9			71.5	74.4		74.6				
	$F_{in} = 70\text{ MHz}$	74.1			70.5	74.1		74.3			71.5	74.6			
	$F_{in} = 170\text{ MHz}$	0 dB Gain	72.3			72.3			72.8			72.9			
		3.5 dB Coarse gain	71.5			71.5			71.9			72.1			
	$F_{in} = 230\text{ MHz}$	0 dB Gain	71.2			71.2			71.8			72			
3.5 dB Coarse gain		70.5			70.5			71.1			71.2				
RMS output noise	Inputs tied to common-mode	1.05			1.05			1.05			1.05			LSB	
SINAD Signal-to-noise and distortion ratio <b>CMOS</b>	$F_{in} = 10\text{ MHz}$	73.7			74.1			74.5			74.6			dBFS	
	$F_{in} = 50\text{ MHz}$	69	72.3		73			70	74.1		74.1				
	$F_{in} = 70\text{ MHz}$	72.6			69	73.2		73.3			70	74.0			
	$F_{in} = 170\text{ MHz}$	0 dB Gain	68.7			71			71.1			72.2			
		3.5 dB Coarse gain	68.6			70.5			70.6			71.5			
	$F_{in} = 230\text{ MHz}$	0 dB Gain	67.3			69			70.2			70.6			
3.5 dB Coarse gain		67			69			69.9			70.4				
SINAD Signal-to-noise and distortion ratio <b>LVDS</b>	$F_{in} = 10\text{ MHz}$	74.3			74.3			74.8			74.9			dBFS	
	$F_{in} = 50\text{ MHz}$	69.5	72.7		72.9			70.5	74.3		74.4				
	$F_{in} = 70\text{ MHz}$	73.4			69.5	73.5		73.6			70.5	74.4			
	$F_{in} = 170\text{ MHz}$	0 dB Gain	70.6			71.4			72			72.4			
		3.5 dB Coarse gain	70.8			71.1			71.6			71.9			
	$F_{in} = 230\text{ MHz}$	0 dB Gain	69.4			69.2			71			70.5			
3.5 dB Coarse gain		69.4			69.4			70.7			70.5				
ENOB Effective number of bits	$F_{in} = 50\text{ MHz}$	11.1	11.7					11.3	12					Bits	
	$F_{in} = 70\text{ MHz}$				11.1	11.8					11.3	12			
SFDR Spurious free dynamic range	$F_{in} = 10\text{ MHz}$	90			91			93			95			dBc	
	$F_{in} = 50\text{ MHz}$	76	80		83			79	89		89				
	$F_{in} = 70\text{ MHz}$	84			78	84		84			79	86			
	$F_{in} = 170\text{ MHz}$	0 dB Gain	76			80			81			82			
		3.5 dB Coarse gain	78			82			83			84			
	$F_{in} = 230\text{ MHz}$	0 dB Gain	75			77			79			79			
3.5 dB Coarse gain		76			79			81			82				

## ELECTRICAL CHARACTERISTICS (continued)

Typical values are at 25°C, min and max values are across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ ,  $AVDD = DRVDD = 3.3\text{ V}$ , maximum rated sampling frequency, 50% clock duty cycle,  $-1\text{ dBFS}$  differential analog input, internal reference mode, applies to CMOS and LVDS interfaces, unless otherwise noted.

PARAMETER	TEST CONDITIONS	ADS6145 $F_S = 125\text{ MSPS}$			ADS6144 $F_S = 105\text{ MSPS}$			ADS6143 $F_S = 80\text{ MSPS}$			ADS6142 $F_S = 65\text{ MSPS}$			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
THD Total harmonic distortion	$F_{in} = 10\text{ MHz}$	88.5			90			91.5			93			dBc	
	$F_{in} = 50\text{ MHz}$	73	79.5		82.5			76	88		88				
	$F_{in} = 70\text{ MHz}$	82			75	83		83			76	85			
	$F_{in} = 170\text{ MHz}$	0 dB Gain	73.5			79			78			80			
		3.5 dB Coarse gain	75			81			79			82			
	$F_{in} = 230\text{ MHz}$	0 dB Gain	71.5			75.5			76			76			
3.5 dB Coarse gain		72.5			77.5			78			78.5				
HD2 Second harmonic distortion	$F_{in} = 10\text{ MHz}$	96			96			97			98			dBc	
	$F_{in} = 50\text{ MHz}$	76	95		96			79	96		96				
	$F_{in} = 70\text{ MHz}$	91			78	92		93			79	93			
	$F_{in} = 170\text{ MHz}$	0 dB Gain	81			83			83			86			
		3.5 dB Coarse gain	82			84			84			87			
	$F_{in} = 230\text{ MHz}$	0 dB Gain	75			79			80			79			
3.5 dB Coarse gain		76			81			81			81				
HD3 Third harmonic distortion	$F_{in} = 10\text{ MHz}$	90			91			93			95			dBc	
	$F_{in} = 50\text{ MHz}$	76	80		83			79	89		89				
	$F_{in} = 70\text{ MHz}$	84			78	84		84			79	86			
	$F_{in} = 170\text{ MHz}$	0 dB Gain	76			80			81			82			
		3.5 dB Coarse gain	78			82			83			84			
	$F_{in} = 230\text{ MHz}$	0 dB Gain	75			77			79			79			
3.5 dB Coarse gain		76			79			81			82				
Worst spur (other than HD2, HD3)	$F_{in} = 10\text{ MHz}$	93			94			96			97			dBc	
	$F_{in} = 50\text{ MHz}$	92			90			93			96				
	$F_{in} = 70\text{ MHz}$	91			90			92			95				
	$F_{in} = 170\text{ MHz}$	90			89			89			91				
	$F_{in} = 230\text{ MHz}$	90			88			89			90				
IMD 2-Tone intermodulation distortion	$F_1 = 185\text{ MHz}$ , $F_2 = 190\text{ MHz}$ , Each tone at $-7\text{ dBFS}$	83			82			84			88			dBFS	
Input overload recovery	Recovery to within 1% (of final value) for 6-dB overload with sine wave input	1			1			1			1			clock cycles	
PSRR AC Power supply rejection ratio	For 100 mVpp signal on AVDD supply	35			35			35			35			dBc	

## DIGITAL CHARACTERISTICS<sup>(1)</sup>

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1, AVDD = 3.3 V

PARAMETER	TEST CONDITIONS	ADS6145/ADS6144 ADS6143/ADS6142			UNIT
		MIN	TYP	MAX	
<b>DIGITAL INPUTS</b>					
<b>PDN, SCLK, SDATA, and SEN<sup>(2)</sup></b>					
High-level input voltage		2.4			V
Low-level input voltage				0.8	V
High-level input current			33		μA
Low-level input current			-33		μA
Input capacitance			4		pF
<b>DIGITAL OUTPUTS</b>					
<b>CMOS INTERFACE, DRVDD = 1.8 to 3.3 V</b>					
High-level output voltage			DRVDD		V
Low-level output voltage			0		V
Output capacitance	Output capacitance inside the device, from each output to ground		2		pF
<b>DIGITAL OUTPUTS</b>					
<b>LVDS INTERFACE, DRVDD = 3.3 V, I<sub>O</sub> = 3.5 mA, R<sub>L</sub> = 100 Ω<sup>(3)</sup></b>					
High-level output voltage			1375		mV
Low-level output voltage			1025		mV
V <sub>OD</sub>	Output differential voltage		225	350	mV
V <sub>OS</sub>	Output offset voltage, single-ended	Common-mode voltage of OUTP, OUTM	1200		mV
Output capacitance	Output capacitance inside the device, from either output to ground		2		pF

- (1) All LVDS and CMOS specifications are characterized, but not tested at production.  
(2) SCLK and SEN function as digital input pins when they are used for serial interface programming. When used as parallel control pins, analog voltage needs to be applied as per [Table 1](#) & [Table 2](#)  
(3) I<sub>O</sub> Refers to the LVDS buffer current setting, R<sub>L</sub> is the differential load resistance between the LVDS output pair.

## TIMING CHARACTERISTICS – LVDS AND CMOS MODES<sup>(1)</sup>

Typical values are at 25°C, min and max values are across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ ,  $AVDD = DRVDD = 3.3\text{ V}$ , maximum rated sampling frequency, sine wave input clock, 1.5  $V_{PP}$  clock amplitude,  $C_L = 5\text{ pF}^{(2)}$ ,  $I_O = 3.5\text{ mA}$ ,  $R_L = 100\ \Omega$ <sup>(3)</sup>, no internal termination, unless otherwise noted.

For timings at lower sampling frequencies, see section [Output Timings](#) in the APPLICATION INFORMATION of this data sheet.

PARAMETER	TEST CONDITIONS	ADS6145 $F_s = 125\text{ MSPS}$			ADS6144 $F_s = 105\text{ MSPS}$			ADS6143 $F_s = 80\text{ MSPS}$			ADS6142 $F_s = 65\text{ MSPS}$			UNIT			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX				
$t_a$	Aperture delay	0.7	1.5	2.5	0.7	1.5	2.5	0.7	1.5	2.5	0.7	1.5	2.5	ns			
$t_j$	Aperture jitter	150			150			150			150			fs rms			
Wake-up time (to valid data)	From global power down	15 50			15 50			15 50			15 50			$\mu\text{s}$			
	From standby	15 50			15 50			15 50			15 50			$\mu\text{s}$			
	From output buffer disable	CMOS	100 200		100 200		100 200		100 200		100 200		ns				
		LVDS	200 500		200 500		200 500		200 500		200 500		ns				
Latency		9			9			9			9			clock cycles			
<b>DDR LVDS MODE<sup>(4)</sup>, <math>DRVDD = 3.3\text{ V}</math></b>																	
$t_{su}$	Data setup time <sup>(5)</sup>	Data valid <sup>(6)</sup> to zero-cross of CLKOUTP			1.7	2.3		2.5	3.1		3.9	4.5		5.4	6.0	ns	
$t_h$	Data hold time <sup>(5)</sup>	Zero-cross of CLKOUTP to data becoming invalid <sup>(6)</sup>			0.7	1.7		0.7	1.7		0.7	1.7		0.7	1.7	ns	
$t_{PDI}$	Clock propagation delay	Input clock rising edge zero-cross to output clock rising edge zero-cross			4.3	5.8	7.3	4.3	5.8	7.3	4.3	5.8	7.3	4.3	5.8	7.3	ns
	LVDS bit clock duty cycle	Duty cycle of differential clock, (CLKOUTP-CLKOUTM), $10 \leq F_s \leq 125\text{ MSPS}$			40%	47%	55%	40%	47%	55%	40%	47%	55%	40%	47%	55%	
$t_r$ $t_f$	Data rise time, Data fall time	Rise time measured from -50 mV to 50 mV, Fall time measured from 50 mV to -50 mV, $1 \leq F_s \leq 125\text{ MSPS}$			70	100	170	70	100	170	70	100	170	70	100	170	ps
$t_{CLKRI}$ $t_{CLKFA}$ $t_{CLKLL}$	Output clock rise time, Output clock fall time	Rise time measured from -50 mV to 50 mV, Fall time measured from 50 mV to -50 mV, $1 \leq F_s \leq 125\text{ MSPS}$			70	100	170	70	100	170	70	100	170	70	100	170	ps
<b>PARALLEL CMOS MODE, <math>DRVDD = 2.5\text{ V}</math> to <math>3.3\text{ V}</math>, default output buffer drive strength<sup>(7)</sup></b>																	
$t_{su}$	Data setup time <sup>(5)</sup>	Data valid <sup>(8)</sup> to 50% of CLKOUT rising edge			2.9	4.4		3.6	5.1		5.1	6.6		6.5	8.0	ns	
$t_h$	Data hold time <sup>(5)</sup>	50% of CLKOUT rising edge to data becoming invalid <sup>(8)</sup>			1.3	2.7		2.1	3.5		3.6	5.0		5.1	6.5	ns	

(1) Timing parameters are specified by design and characterization and not tested in production.

(2)  $C_L$  is the Effective external single-ended load capacitance between each output pin and ground.

(3)  $I_O$  Refers to the LVDS buffer current setting;  $R_L$  is the differential load resistance between the LVDS output pair.

(4) Measurements are done with a transmission line of 100  $\Omega$  characteristic impedance between the device and the load.

(5) Setup and hold time specifications take into account the effect of jitter on the output data and clock.

(6) Data valid refers to a logic high of +100 mV and logic low of -100 mV.

(7) For  $DRVDD < 2.2\text{ V}$ , it is recommended to use an external clock for data capture and NOT the device output clock signal (CLKOUT).

See [Parallel CMOS interface](#) in the application section.

(8) Data valid refers to a logic high of 2 V (1.7 V) and logic low of 0.8 V (0.7 V) for  $DRVDD = 3.3\text{ V}$  (2.5 V).

**TIMING CHARACTERISTICS – LVDS AND CMOS MODES (continued)**

For timings at lower sampling frequencies, see section [Output Timings](#) in the APPLICATION INFORMATION of this data sheet.

PARAMETER	TEST CONDITIONS	ADS6145 F <sub>s</sub> = 125 MSPS			ADS6144 F <sub>s</sub> = 105 MSPS			ADS6143 F <sub>s</sub> = 80 MSPS			ADS6142 F <sub>s</sub> = 65 MSPS			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
t <sub>PDI</sub>	Clock propagation delay	Input clock rising edge zero-cross to 50% of CLKOUT rising edge												ns
	Output clock duty cycle	Duty cycle of output clock (CLKOUT), 10 ≤ F <sub>s</sub> ≤ 125 MSPS												
t <sub>r</sub> t <sub>f</sub>	Data rise time, Data fall time	Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD, 1 ≤ F <sub>s</sub> ≤ 125 MSPS												ns
t <sub>CLKRISE</sub> t <sub>CLKFALL</sub>	Output clock rise time, Output clock fall time	Rise time measured from 20% to 80% of DRVDD, Fall time measured from 80% to 20% of DRVDD, 1 ≤ F <sub>s</sub> ≤ 125 MSPS												ns

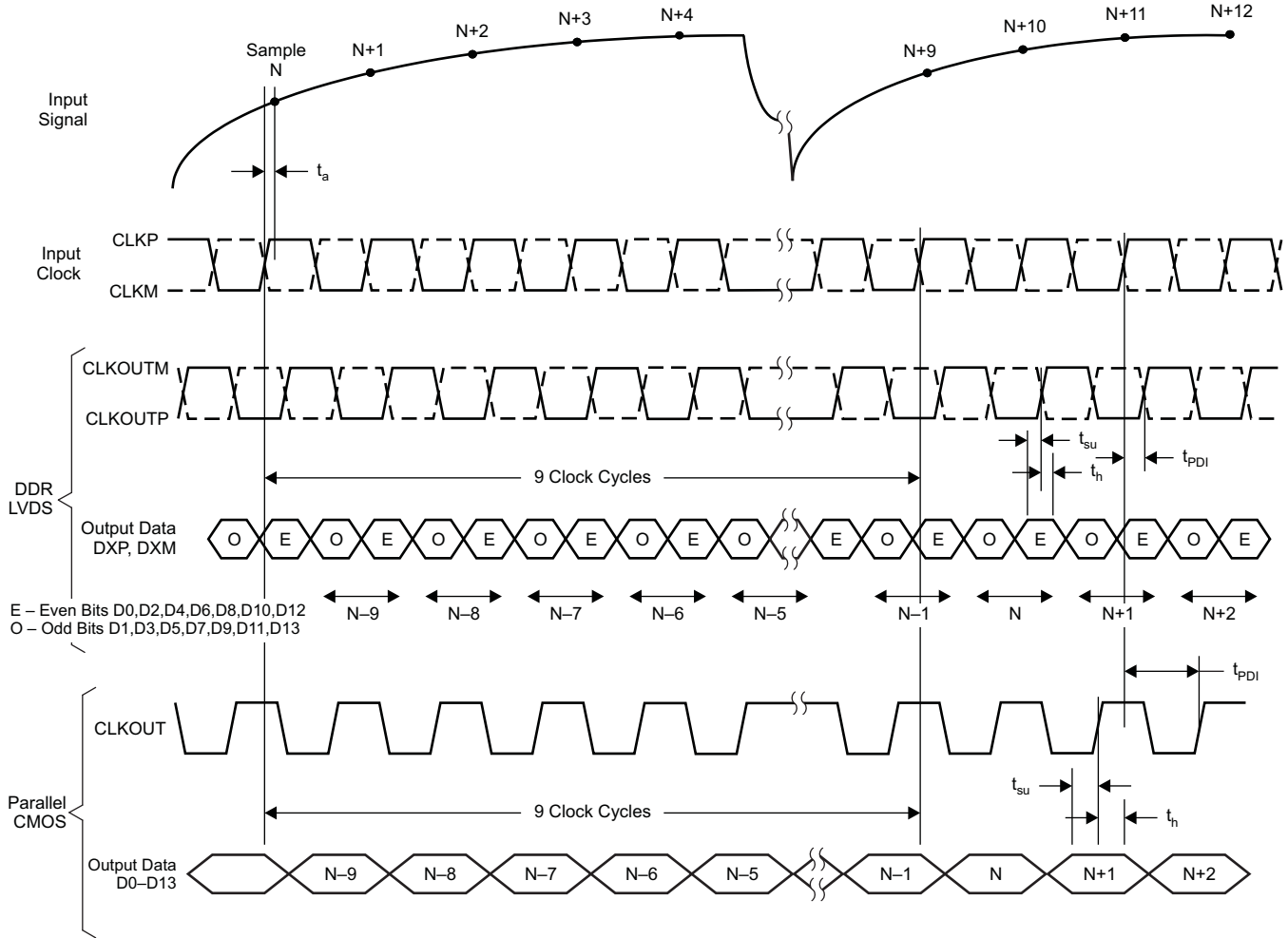
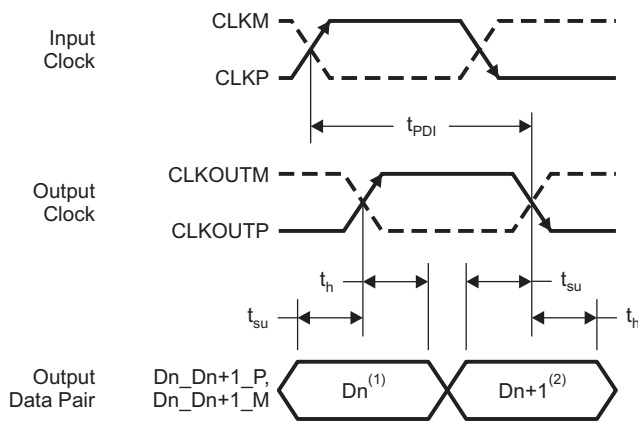


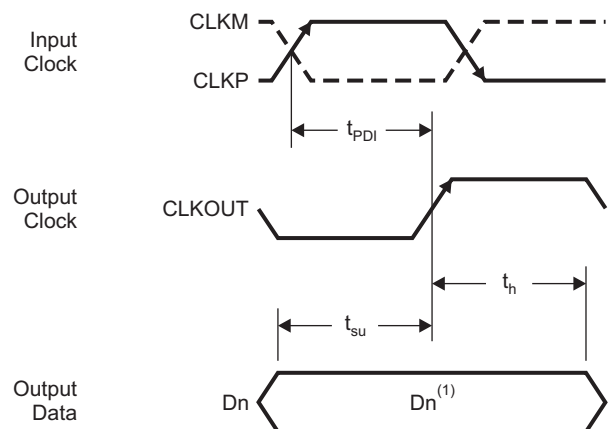
Figure 1. Latency



<sup>(1)</sup> $D_n$  – Bits D0, D2, D4, D6, D8, D10, D12

<sup>(2)</sup> $D_{n+1}$  – Bits D1, D3, D5, D7, D9, D11, D13

Figure 2. LVDS Mode Timing



<sup>(1)</sup> $D_n$  – Bits D0–D13

Figure 3. CMOS Mode Timing

## DEVICE PROGRAMMING MODES

The ADS614X have several features that can be easily configured using either parallel interface control or serial interface programming.

### USING SERIAL INTERFACE PROGRAMMING ONLY

To program using the serial interface, the internal registers must first be reset to their default values, and the RESET pin must be kept **low**. In this mode, SEN, SDATA, and SCLK function as serial interface pins and are used to access the internal registers of the ADC. The registers are reset either by applying a pulse on the RESET pin or by a **high** setting on the <RST> bit (D4 in register 0x00). The [Serial Interface](#) section describes register programming and register reset in more detail.

### USING PARALLEL INTERFACE CONTROL ONLY

To control the device using the parallel interface, keep RESET tied **high** (AVDD). Now SEN, SCLK, SDATA, and PDN function as parallel interface control pins. These pins can be used to directly control certain modes of the ADC by connecting them to the correct voltage levels (as described in [Table 1](#) to [Table 3](#)). There is no need to apply a reset pulse.

Frequently used functions are controlled in this mode — standby, selection between LVDS/CMOS output format, internal/external reference, and 2s complement/straight binary output format.

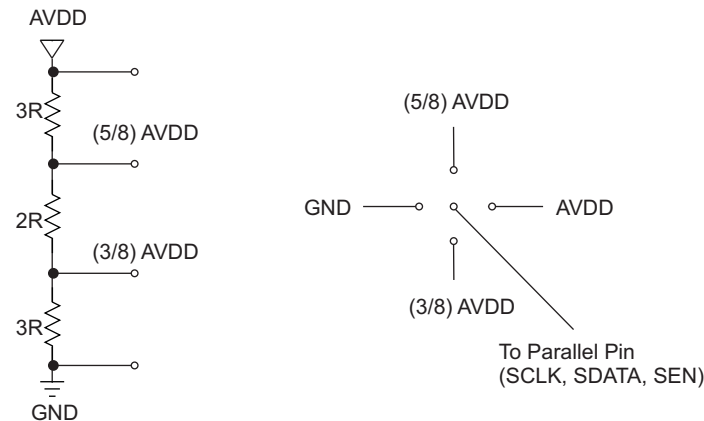


Figure 4. Simple Scheme to Configure Parallel Pins

## DESCRIPTION OF PARALLEL PINS

Table 1. SCLK (Analog Control Pin)

SCLK	DESCRIPTION
0	Internal reference and 0 dB gain (full-scale = 2 V <sub>PP</sub> )
(3/8) AVDD	External reference and 0 dB gain (full-scale = 2 V <sub>PP</sub> )
(5/8) AVDD	External reference and 3.5 dB coarse gain (full-scale = 1.34 V <sub>PP</sub> )
AVDD	Internal reference and 3.5 dB coarse gain (full-scale = 1.34 V <sub>PP</sub> )

Table 2. SEN (Analog Control Pin)

SEN	DESCRIPTION
0	2s Complement format and DDR LVDS interface
(3/8) AVDD	Straight binary format and DDR LVDS interface
(5/8) AVDD	Straight binary and parallel CMOS interface
AVDD	2s Complement format and parallel CMOS interface

**Table 3. SDATA, PDN (Digital Control Pins)**

SDATA	PDN	DESCRIPTION
Low	Low	Normal operation
Low	High (AVDD)	Standby - only the ADC is powered down
High (AVDD)	Low	Output buffers are powered down, fast wake-up time
High (AVDD)	High (AVDD)	Global power down. ADC, internal reference, and output buffers are powered down, slow wake-up time

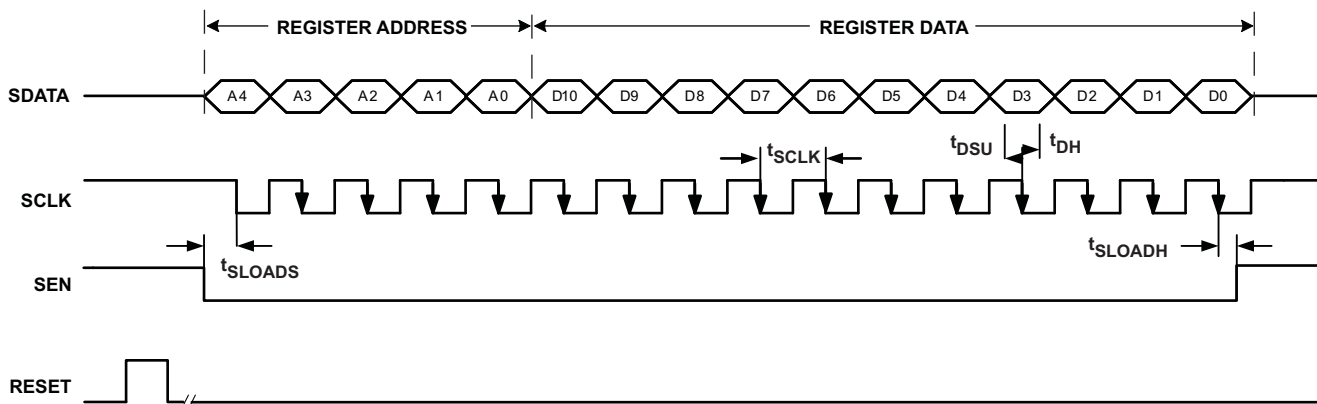
## SERIAL INTERFACE

The ADC has a set of internal registers, which can be accessed through the serial interface formed by pins SEN (Serial interface Enable), SCLK (Serial Interface Clock), SDATA (Serial Interface Data) and RESET. After device power-up, the internal registers must be reset to their default values by applying a high-going pulse on RESET (of width greater than 10 ns).

Serial shift of bits into the device is enabled when SEN is low. Serial data SDATA is latched at every falling edge of SCLK when SEN is active (low). The serial data is loaded into the register at every 16th SCLK falling edge when SEN is low. If the word length exceeds a multiple of 16 bits, the excess bits are ignored. Data is loaded in multiples of 16-bit words within a single active SEN pulse.

The first 5 bits form the register address and the remaining 11 bits form the register data.

The interface can work with a SCLK frequency from 20 MHz down to very low speeds (a few hertz) and also with a non-50% SCLK duty cycle.



**Figure 5. Serial Interface Timing Diagram**

## REGISTER INITIALIZATION

After power-up, the internal registers *must* be reset to their default values. This is done in one of two ways:

1. Either through a hardware reset by applying a high-going pulse on the RESET pin (width greater than 10 ns) as shown in [Figure 5](#).

OR

2. By applying a software reset. Using the serial interface, set the <RST> bit (D4 in register 0x00) to **high**. This initializes the internal registers to their default values and then self-resets the <RST> bit to **low**. In this case the RESET pin is kept **low**.

## SERIAL INTERFACE TIMING

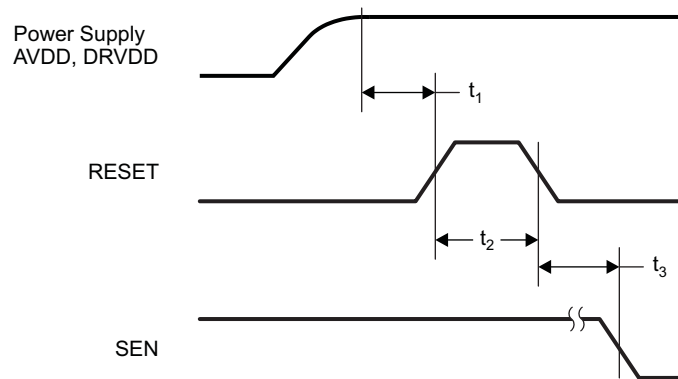
Typical values at 25°C, min and max values across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ ,  
AVDD = DRVDD = 3.3 V (unless otherwise noted)

		MIN	TYP	MAX	UNIT
$f_{SCLK}$	SCLK Frequency = $1/t_{SCLK}$	> DC		20	MHz
$t_{SLOADS}$	SEN to SCLK Setup time	25			ns
$t_{SLOADH}$	SCLK to SEN Hold time	25			ns
$t_{DSU}$	SDATA Setup time	25			ns
$t_{DH}$	SDATA Hold time	25			ns

## RESET TIMING

Typical values at 25°C, min and max values across the full temperature range  $T_{MIN} = -40^{\circ}\text{C}$  to  $T_{MAX} = 85^{\circ}\text{C}$ ,  
AVDD = DRVDD = 3.3 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_1$	Power-on delay	5			ms
$t_2$	Reset pulse width	10			ns
$t_3$	Register write delay	25			ns
$t_{PO}$	Power-up time		6.5		ms



NOTE: A high-going pulse on the RESET pin is required in serial interface mode in the case of initialization through a hardware reset. For parallel interface operation, RESET has to be tied permanently HIGH.

**Figure 6. Reset Timing Diagram**

## SERIAL REGISTER MAP

Table 4 gives a summary of all the modes that can be programmed through the serial interface.

**Table 4. Summary of Functions Supported by Serial Interface<sup>(1)(2)</sup>**

REGISTER ADDRESS IN HEX	REGISTER FUNCTIONS										
	A4 - A0	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1
00	<PDN OBUF> Output buffers powered down	<COARSE GAIN> Coarse gain	<LVDS CMOS> LVDS or CMOS Output interface	0	0	<REF> Internal or external Reference	<RST> Software reset	0	<PDN CLKOUT> Output clock buffer powered down	0	<STBY> ADC Power down
04	<DATAOUT POSN> Output data position control	<CLKOUT EDGE> Output clock edge control	<CLKOUT POSN> Output clock position control	0	0	0	0	0	0	0	0
09	Bit-wise or Byte-wise control	0	0	0	0	0	0	0	0	0	0
0A	<DATA FORMAT> 2s Complement or straight binary	0	0	<TEST PATTERNS>			0	0	0	0	0
0B	<CUSTOM LOW> Custom pattern lower 9 bits									0	0
0C	<FINE GAIN> Fine gain 0 to 6dB			0	0	0	<CUSTOM HIGH> Custom pattern upper 5 bits				
0E	0	LVDS Termination LVDS Internal termination control for output data and clock						<LVDS CURRENT> LVDS Current control		<CURRENT DOUBLE> LVDS current double	
0F	0	0	0	<DRIVE STRENGTH> CMOS output buffer drive strength control			0	0	0	0	

(1) The unused bits in each register (shown by blank cells in above table) must be programmed as '0'.

(2) Multiple functions in a register can be programmed in a single write operation.

## DESCRIPTION OF SERIAL REGISTERS

Each register function is explained in detail.

**Table 5.**

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00	<PDN OBUF> Output buffers powered down	<COARSE GAIN> Coarse gain	<LVDS CMOS> LVDS or CMOS Output interface	0	0	<REF> Internal or external reference	<RST> Software reset	0	<PDN CLKOUT> Output clock buffer powered down	0	<STBY> ADC Power down

### D0 <STBY> [Power down modes](#)

- 0 Normal operation
- 1 Device enters standby mode where only ADC is powered down.

### D2 <PDN CLKOUT> [Power down modes](#)

- 0 Output clock is active (on CLKOUT pin)
- 1 Output clock buffer is powered down and becomes three-stated. Data outputs are unaffected.

### D4 <RST>

- 1 Software reset applied - resets all internal registers and the bit self-clears to 0.

### D5 <REF> [Reference selection](#)

- 0 Internal reference enabled
- 1 External reference enabled

### D8 <LVDS CMOS> [Output Interface selection](#)

- 0 Parallel CMOS interface
- 1 DDR LVDS Interface

### D9 <COARSE GAIN> [Gain programming](#)

- 0 0 dB Coarse gain
- 1 3.5 dB Coarse gain

### D10 <PDN OBUF> [Power down modes](#)

- 0 Output data and clock buffers enabled
- 1 Output data and clock buffers disabled

**Table 6.**

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
04	<DATAOUT POSN> Output data position control	<CLKOUT EDGE> Output Clock edge control	<CLKOUT POSN> Output clock position control	0	0	0	0	0	0	0	0

**D8** <CLKOUT POSN> [Output clock position control](#)

- 0 Default output clock position after reset. The setup/hold timings for this clock position are specified in the timing specifications table.
- 1 Output clock shifted (delayed) by 400 ps

**D9** <CLKOUT EDGE>

- 0 Use rising edge to capture data
- 1 Use falling edge to capture data

**D10** <DATAOUT\_POSN>

- 0 Default position (after reset)
- 1 Data transition delayed by half clock cycle with respect to default position

**Table 7.**

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
09	Bit-wise or Byte-wise control	0	0	0	0	0	0	0	0	0	0

**D10** **Bit-wise or byte-wise selection (DDR LVDS mode only)**

- 0 Bit-wise sequence - Even data bits (D0, D2, D4,..D12) are output at the rising edge of CLKOUTP and odd data bits (D1, D3, D5,..D13) at the falling edge of CLKOUTP
- 1 Byte-wise sequence - Lower 7 data bits (D0-D7) are output at the rising edge of CLKOUTP and upper 7 data bits (D8-D13) at the falling edge of CLKOUTP

**Table 8.**

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0A	<DF> 2s Complement or straight binary	0	0	<TEST PATTERNS>			0	0	0	0	0

**D7-D5 Test patterns**

- 000 Normal operation - <D13:D0> = ADC output
- 001 All zeros - <D13:D0> = 0x0000
- 010 All ones - <D13:D0> = 0x3FFF
- 011 Toggle pattern - <D13:D0> toggles between 0x2AAA and 0x1555
- 100 Digital ramp - <D13:D0> increments from 0x0000 to 0x3FFF by one code every cycle
- 101 Custom pattern - <D13:D0> = contents of CUSTOM PATTERN registers
- 110 Unused
- 111 Unused

**D10 <DATA FORMAT>**

- 0 2s Complement
- 1 Straight binary

**Table 9.**

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0B	<CUSTOM LOW> Lower 9 bits of custom pattern									0	0

**Table 10.**

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0C	<FINE GAIN> Fine gain 0 to 6dB			0	0	0	<CUSTOM HIGH> Upper 5 bits of custom pattern				

Reg 0B <CUSTOM LOW> - Specifies lower 9 bits of custom pattern  
D10-D2

Reg 0C <CUSTOM HIGH> - Specifies upper 5 bits of custom pattern  
D4-D0

**D10-D8 <FINE GAIN> [Gain programming](#)**

- 000 0 dB Gain
- 001 1 dB Gain
- 010 2 dB Gain
- 011 3 dB Gain
- 100 4 dB Gain
- 101 5 dB Gain
- 110 6 dB Gain
- 111 Unused

**Table 11.**

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0E	0	<LVDS TERMINATION> LVDS Internal termination control for output data and clock						<LVDS CURRENT> LVDS Current control		<CURRENT DOUBLE> LVDS Current double	

**D1-D0** <CURRENT DOUBLE> [LVDS current programming](#)

**D0** LVDS Data buffer current control

- 0 Default current, set by <LVDS\_CURR>
- 1 2x LVDS Current set by <LVDS\_CURR>

**D1** LVDS Clock buffer current control

- 0 Default current, set by <LVDS\_CURR>
- 1 2x LVDS Current set by <LVDS\_CURR>

**D3-D2** <LVDS CURRENT> [LVDS current programming](#)

- 00 3.5 mA
- 01 2.5 mA
- 10 4.5 mA
- 11 1.75 mA

**D9-D4** [LVDS internal termination](#)

**D9-D7** <DATA TERM> Internal termination for LVDS output data bits

- 000 No internal termination
- 001 300 Ω
- 010 185 Ω
- 011 115 Ω
- 100 150 Ω
- 101 100 Ω
- 110 80 Ω
- 111 65 Ω

**D6-D4** <CLKOUT TERM> Internal termination for LVDS output clock

- 000 No internal termination
- 001 300 Ω
- 010 185 Ω
- 011 115 Ω
- 100 150 Ω
- 101 100 Ω
- 110 80 Ω
- 111 65 Ω

**Table 12.**

A4–A0 (hex)	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0F	0	0	0	<DRIVE STRENGTH> CMOS Output buffer drive strength control				0	0	0	0

**D7-D4** <DRIVE STRENGTH> [Output buffer drive strength controls](#)

- 0101 WEAKER than default drive
- 0000 DEFAULT drive strength
- 1111 STRONGER than default drive strength (recommended for load capacitances > 5 pF)
- 1010 MAXIMUM drive strength (recommended for load capacitances > 5 pF)
- Other Do not use combinations

## PIN CONFIGURATION (CMOS MODE)

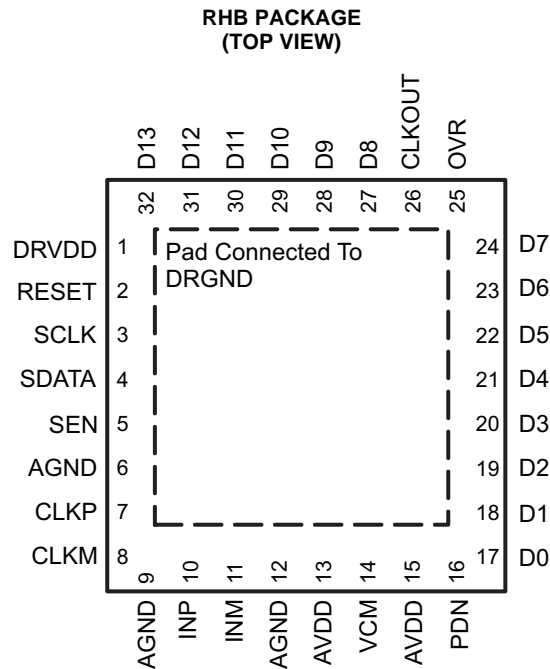


Figure 7. CMOS Mode Pinout

## PIN ASSIGNMENTS – CMOS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	13, 15	2
AGND	Analog ground	I	6, 9, 12	3
CLKP, CLKM	Differential clock inputs	I	7, 8	2
INP, INM	Differential analog inputs	I	10, 11	2
VCM	Internal reference mode – common-mode voltage output. External reference mode – reference input. The voltage forced on this pin sets the internal references.	I/O	14	1
RESET	Serial interface RESET input. When using serial interface mode, the user MUST initialize the internal registers through a hardware RESET by applying a high-going pulse on this pin, or by using the software reset option. See the <i>SERIAL INTERFACE</i> section. In parallel interface mode, the user has to tie the RESET pin permanently HIGH. (SCLK, SDATA, and SEN are used as parallel pin controls in this mode.) The pin has an internal 100-kΩ pull-down resistor.	I	2	1
SCLK	This pin functions as the serial interface clock input when RESET is low. When RESET is tied high, it controls coarse gain and internal/external reference selection. Tie SCLK <b>low</b> for internal reference and 0 dB gain and <b>high</b> for internal reference and 3.5 dB gain. See <a href="#">Table 1</a> . The pin has an internal 100-kΩ pull-down resistor.	I	3	1
SDATA	This pin functions as the serial interface data input when RESET is <b>low</b> . It controls various power down modes along with the PDN pin when RESET is tied <b>high</b> . See <a href="#">Table 3</a> for detailed information. The pin has an internal 100-kΩ pull-down resistor.	I	4	1
SEN	This pin functions as the serial interface enable input when RESET is <b>low</b> . When RESET is high, it controls output interface type and data formats. See <a href="#">Table 2</a> for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	5	1
PDN	Global power-down control pin	I	16	1

**PIN ASSIGNMENTS – CMOS Mode (continued)**

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
CLKOUT	CMOS Output clock	O	26	1
D0	CMOS Output data D0	O	17	1
D1	CMOS Output data D1	O	18	1
D2	CMOS Output data D2	O	19	1
D3	CMOS Output data D3	O	20	1
D4	CMOS Output data D4	O	21	1
D5	CMOS Output data D5	O	22	1
D6	CMOS Output data D6	O	23	1
D7	CMOS Output data D7	O	24	1
D8	CMOS Output data D8	O	27	1
D9	CMOS Output data D9	O	28	1
D10	CMOS Output data D10	O	29	1
D11	CMOS Output data D11	O	30	1
D12	CMOS Output data D12	O	31	1
D13	CMOS Output data D13	O	32	1
OVR	Indicates overvoltage on analog inputs (for differential input greater than full-scale), CMOS level	O	25	1
DRVDD	Digital supply	I	1	1
DRGND	Digital ground. Connect the pad to the ground plane. See <a href="#">Board Design Considerations</a> in the application information section.	I	PAD	1

## PIN CONFIGURATION (LVDS MODE)

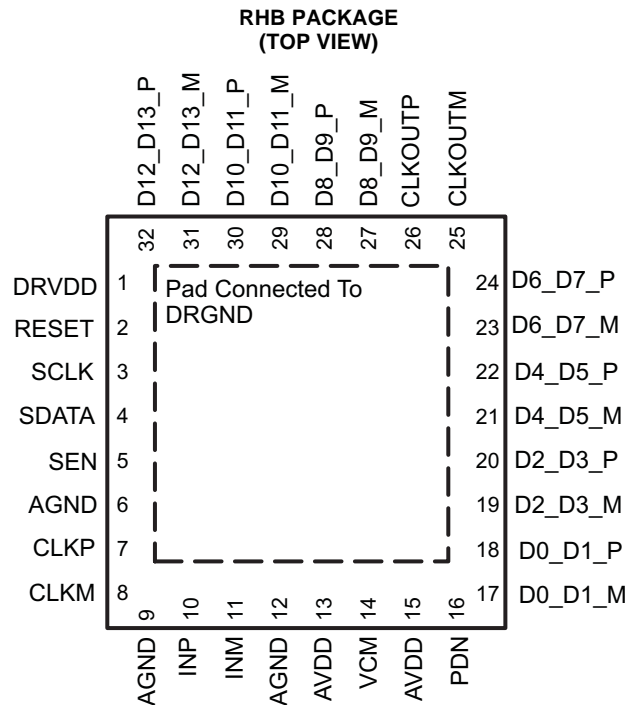


Figure 8. LVDS Mode Pinout

### PIN ASSIGNMENTS – LVDS Mode

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
AVDD	Analog power supply	I	13, 15	2
AGND	Analog ground	I	6, 9, 12	3
CLKP, CLKM	Differential clock inputs	I	7, 8	2
INP, INM	Differential analog inputs	I	10, 11	2
VCM	Internal reference mode – common-mode voltage output. External reference mode – reference input. The voltage forced on this pin sets the internal references.	I/O	14	1
RESET	Serial interface RESET input. When using serial interface mode, the user <b>MUST</b> initialize the internal registers through a hardware RESET by applying a high-going pulse on this pin or by using the software reset option. See the <i>SERIAL INTERFACE</i> section. In parallel interface mode, the user has to tie the RESET pin permanently HIGH. (SCLK, SDATA, and SEN are used as parallel pin controls in this mode.) The pin has an internal 100-kΩ pull-down resistor.	I	2	1
SCLK	This pin functions as the serial interface clock input when RESET is low. When RESET is tied high, it controls coarse gain and internal/external reference selection. Tie SCLK <b>low</b> for internal reference and 0 dB gain and <b>high</b> for internal reference and 3.5 dB gain. See <a href="#">Table 1</a> . The pin has an internal 100-kΩ pull-down resistor.	I	3	1
SDATA	This pin functions as the serial interface data input when RESET is <b>low</b> . It controls various power down modes along with the PDN pin when RESET is tied <b>high</b> . See <a href="#">Table 3</a> for detailed information. The pin has an internal 100 kΩ pull-down resistor.	I	4	1
SEN	The pin functions as the serial interface enable input when RESET is <b>low</b> . When RESET is high, it controls output interface type and data formats. See <a href="#">Table 2</a> for detailed information. The pin has an internal 100-kΩ pull-up resistor to DRVDD.	I	5	1
PDN	Global power-down control pin	I	16	1

**PIN ASSIGNMENTS – LVDS Mode (continued)**

PIN NAME	DESCRIPTION	PIN TYPE	PIN NUMBER	NUMBER OF PINS
CLKOUTP	Differential output clock, true	O	26	1
CLKOUTM	Differential output clock, complement	O	25	1
D0_D1_P	Differential output data D0 and D1 multiplexed, true	O	18	1
D0_D1_M	Differential output data D0 and D1 multiplexed, complement.	O	17	1
D2_D3_P	Differential output data D2 and D3 multiplexed, true	O	20	1
D2_D3_M	Differential output data D2 and D3 multiplexed, complement	O	19	1
D4_D5_P	Differential output data D4 and D5 multiplexed, true	O	22	1
D4_D5_M	Differential output data D4 and D5 multiplexed, complement	O	21	1
D6_D7_P	Differential output data D6 and D7 multiplexed, true	O	24	1
D6_D7_M	Differential output data D6 and D7 multiplexed, complement	O	23	1
D8_D9_P	Differential output data D8 and D9 multiplexed, true	O	28	1
D8_D9_M	Differential output data D8 and D9 multiplexed, complement	O	27	1
D10_D11_P	Differential output data D10 and D11 multiplexed, true	O	30	1
D10_D11_M	Differential output data D10 and D11 multiplexed, complement	O	29	1
D12_D13_P	Differential output data D12 and D13 multiplexed, true	O	32	1
D12_D13_M	Differential output data D12 and D13 multiplexed, complement	O	31	1
DRVDD	Digital supply	I	1	1
DRGND	Digital ground. Connect the pad to the ground plane. See <a href="#">Board Design Considerations</a> in application information section.	I	PAD	1

### TYPICAL CHARACTERISTICS - ADS6145 ( $F_s = 125$ MSPS)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

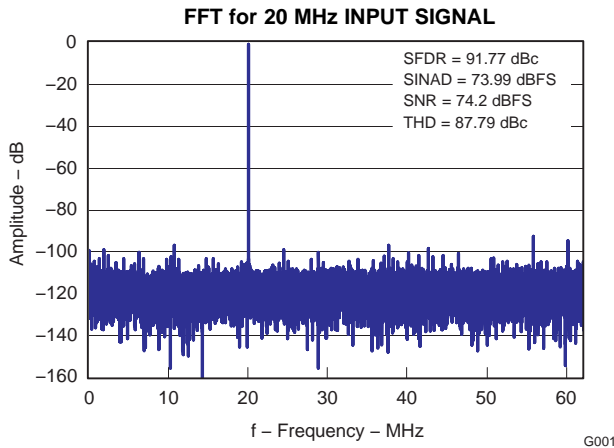


Figure 9.

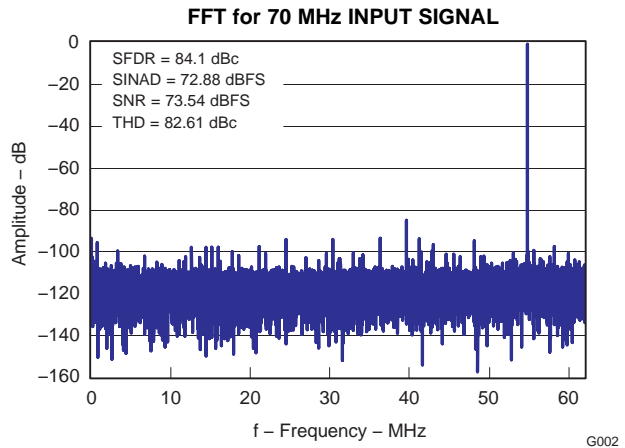


Figure 10.

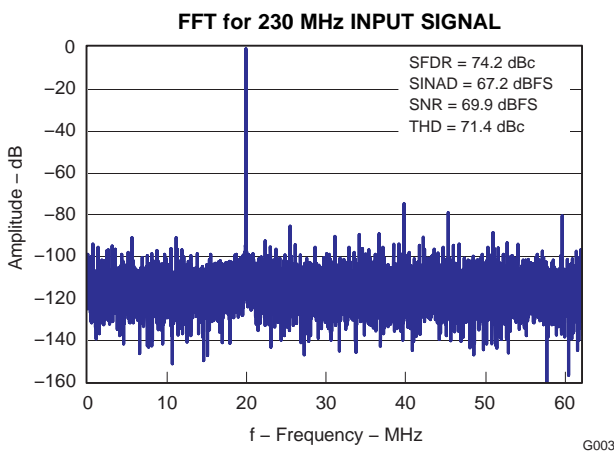


Figure 11.

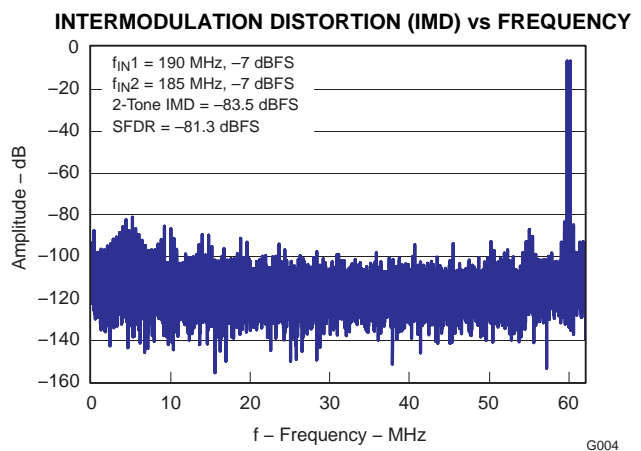


Figure 12.

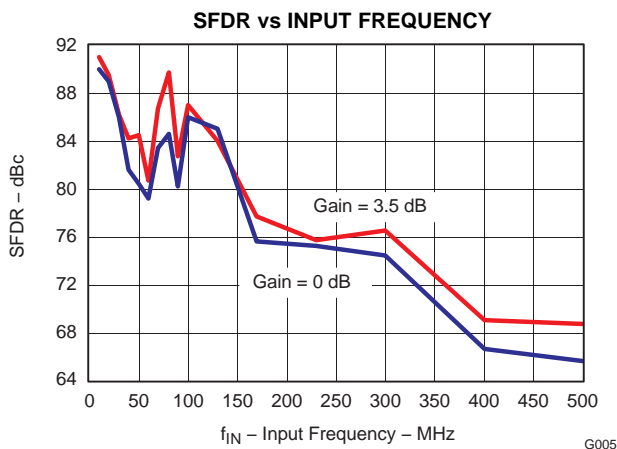


Figure 13.

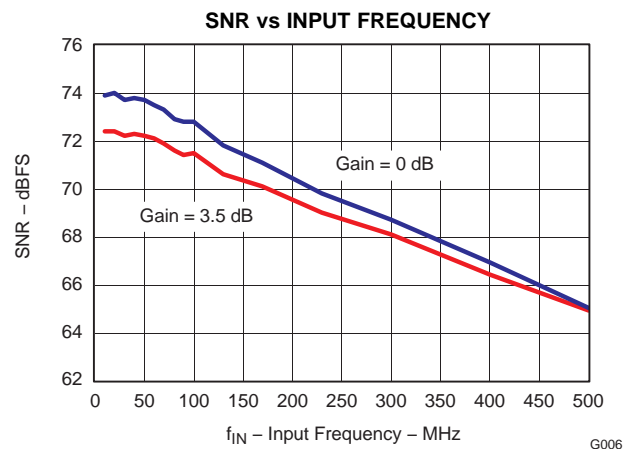


Figure 14.

**TYPICAL CHARACTERISTICS - ADS6145 ( $F_S = 125$  MSPS) (continued)**

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

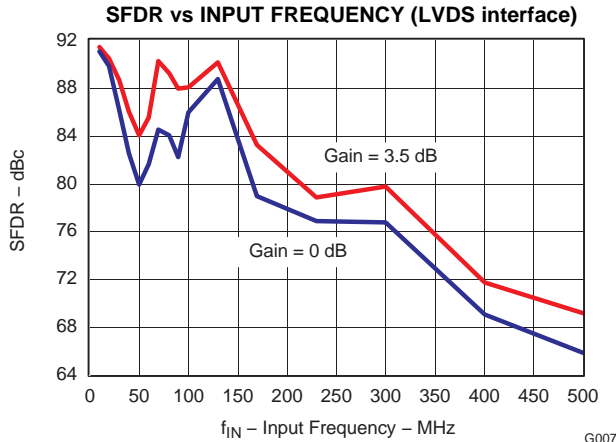


Figure 15.

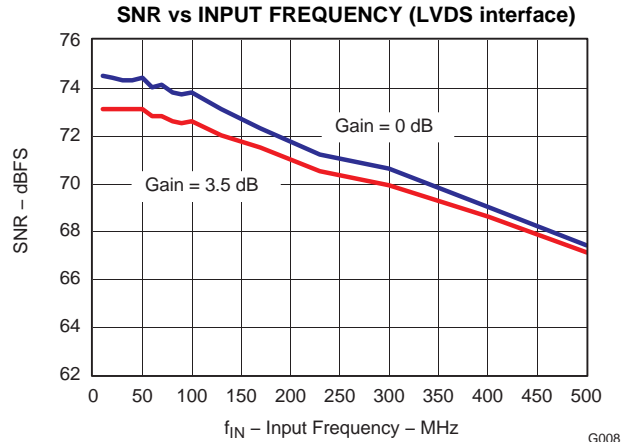


Figure 16.

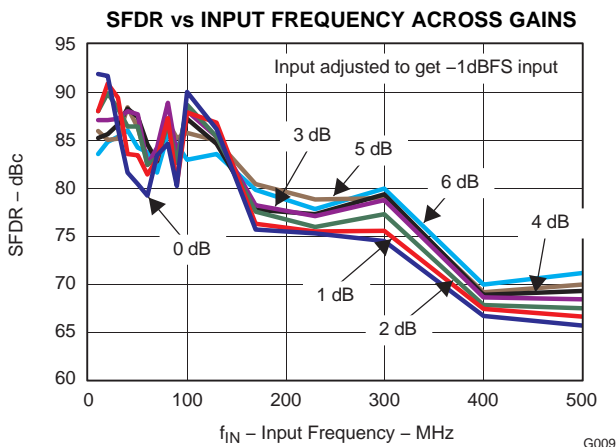


Figure 17.

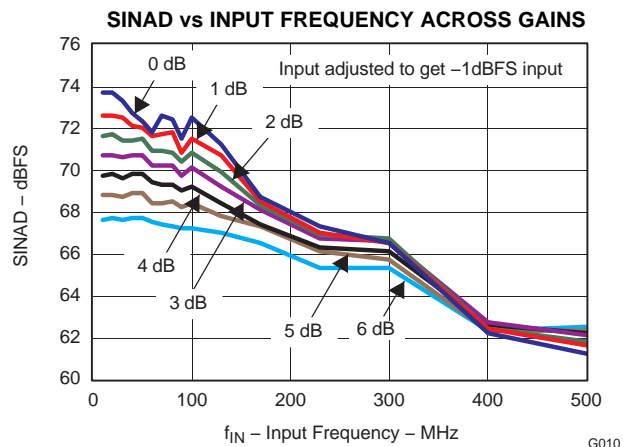


Figure 18.

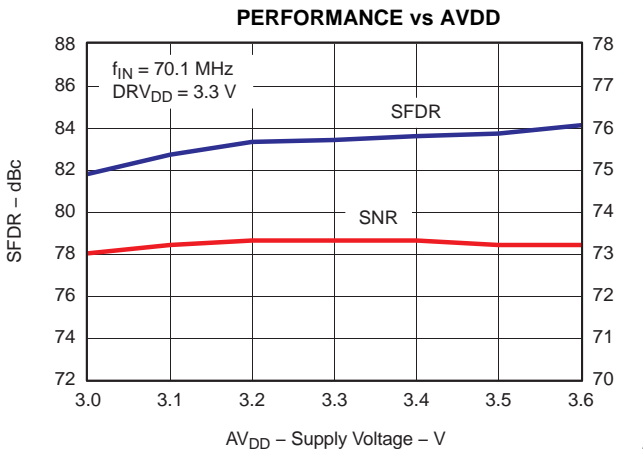


Figure 19.

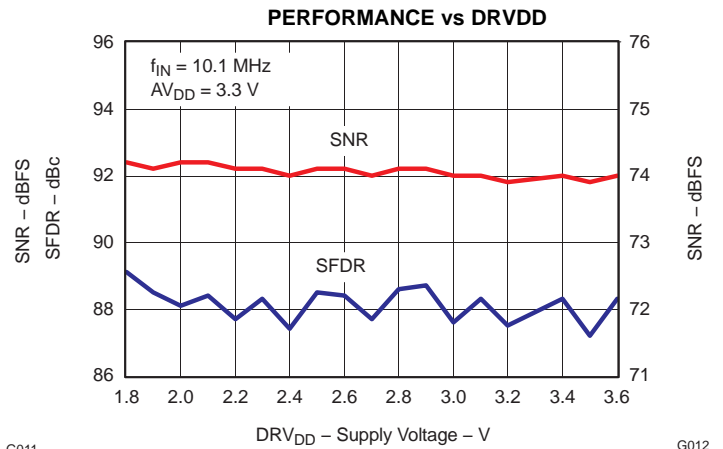


Figure 20.

### TYPICAL CHARACTERISTICS - ADS6145 ( $F_S = 125$ MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

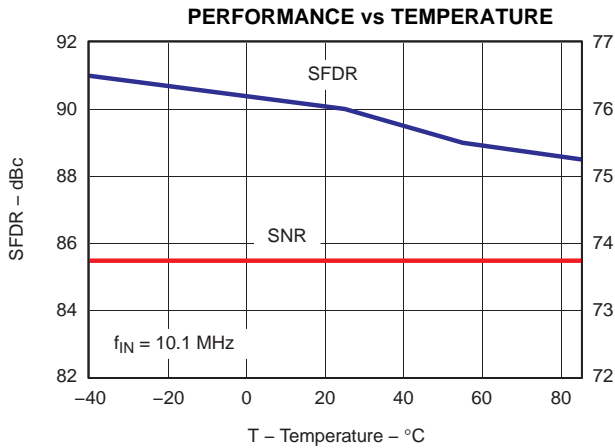


Figure 21.

G013

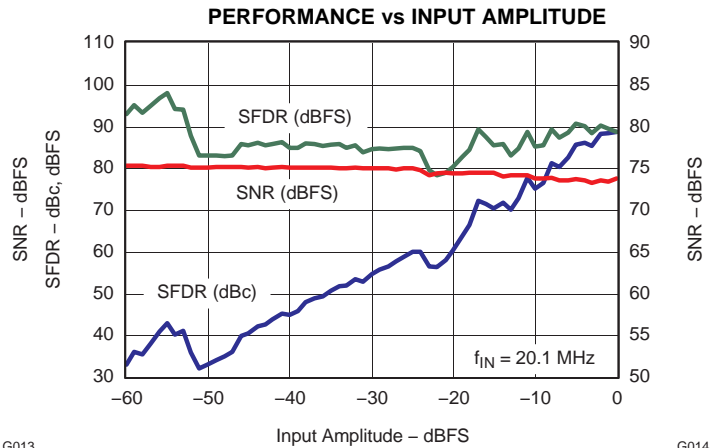


Figure 22.

G014

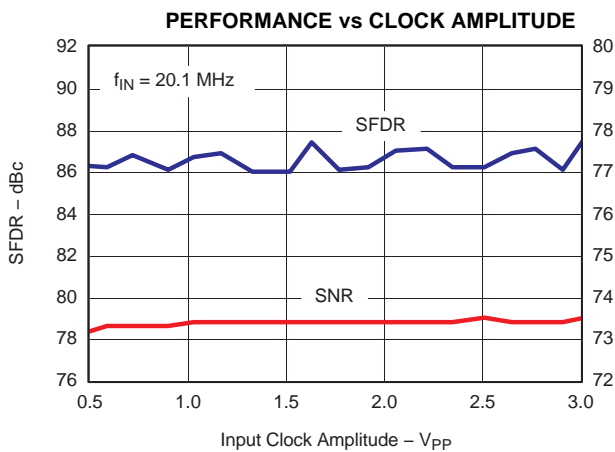


Figure 23.

G015

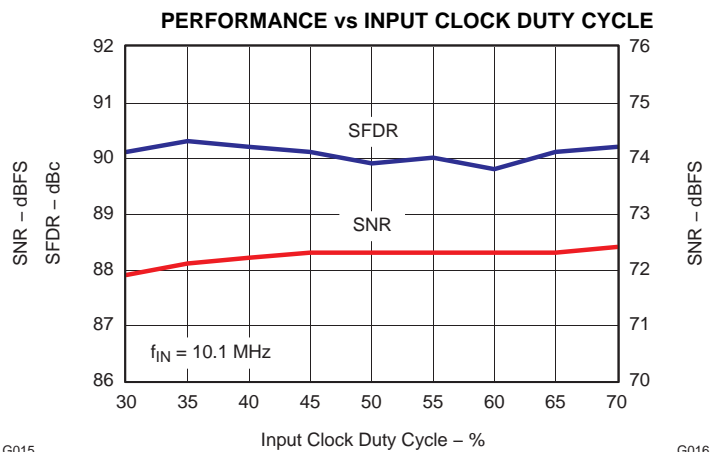


Figure 24.

G016

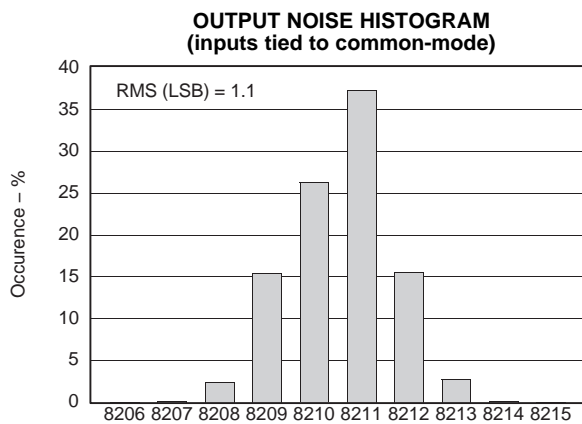


Figure 25.

G017

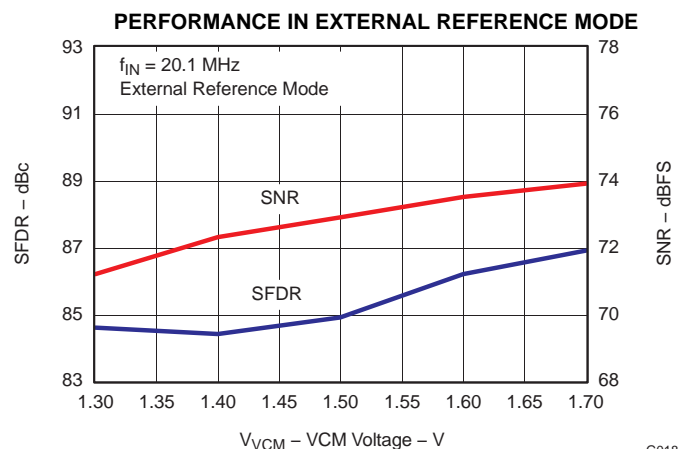


Figure 26.

G018

**TYPICAL CHARACTERISTICS - ADS6144 ( $F_s = 105$  MSPS)**

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>pp</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

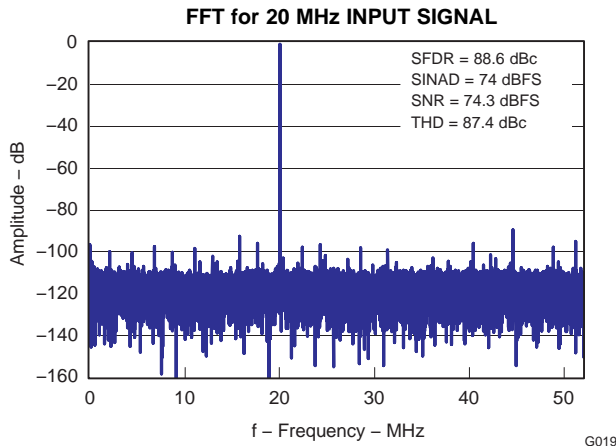


Figure 27.

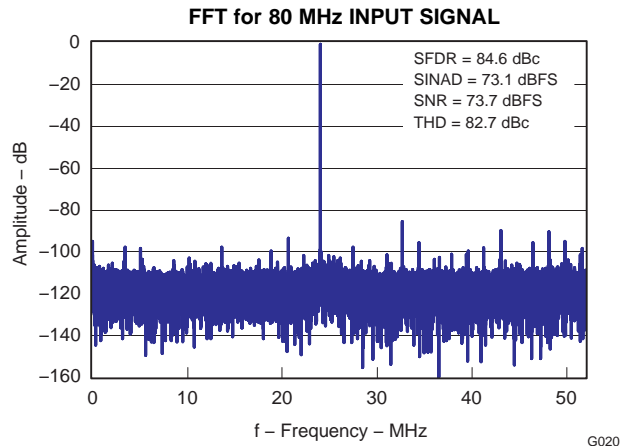


Figure 28.

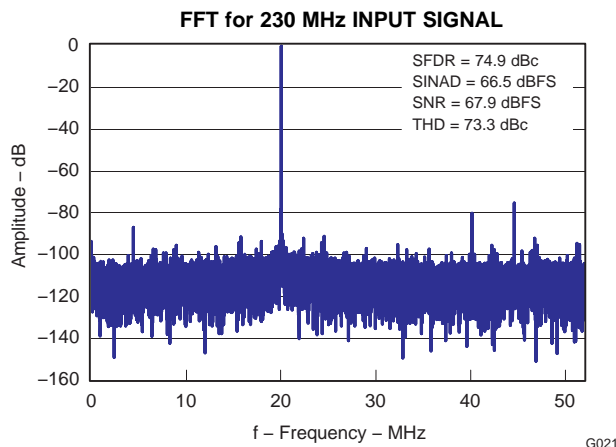


Figure 29.

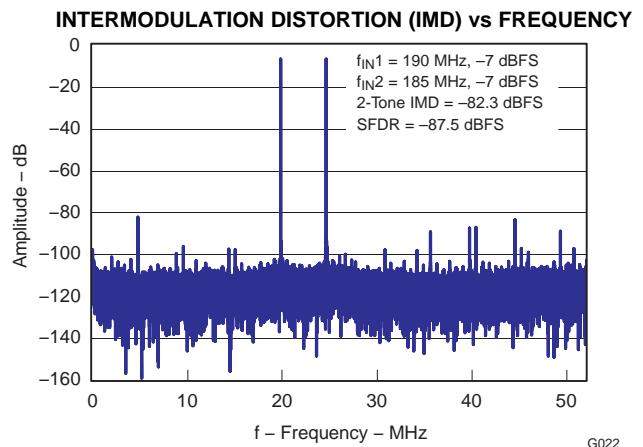


Figure 30.

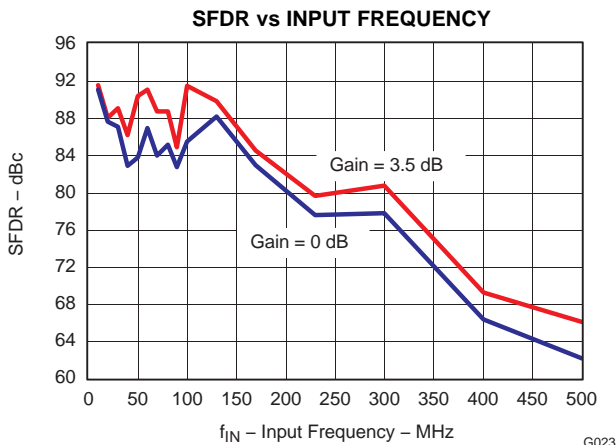


Figure 31.

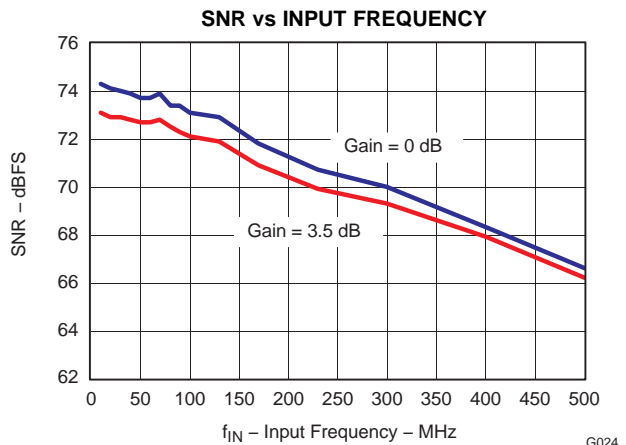


Figure 32.

### TYPICAL CHARACTERISTICS - ADS6144 ( $F_S = 105$ MSPS) (continued)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

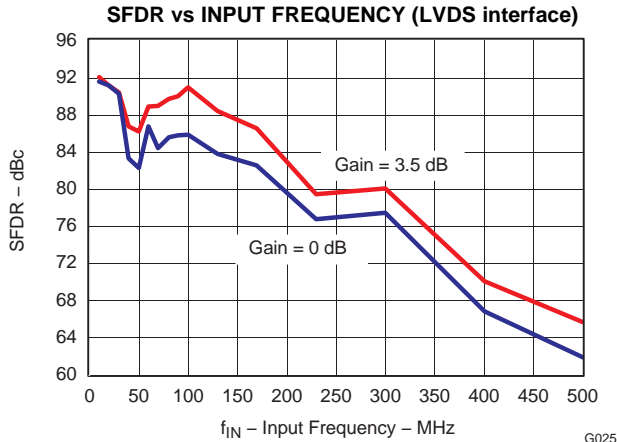


Figure 33.

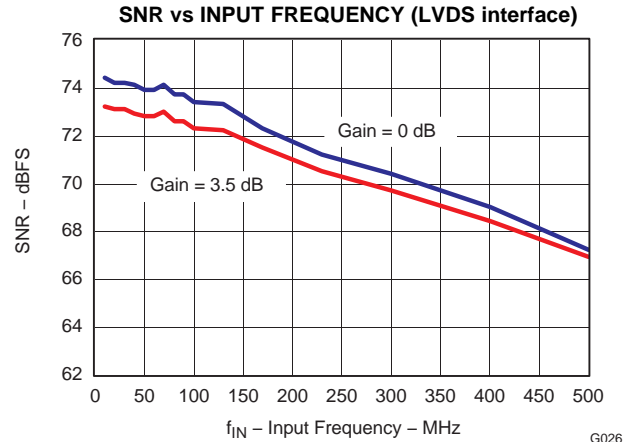


Figure 34.

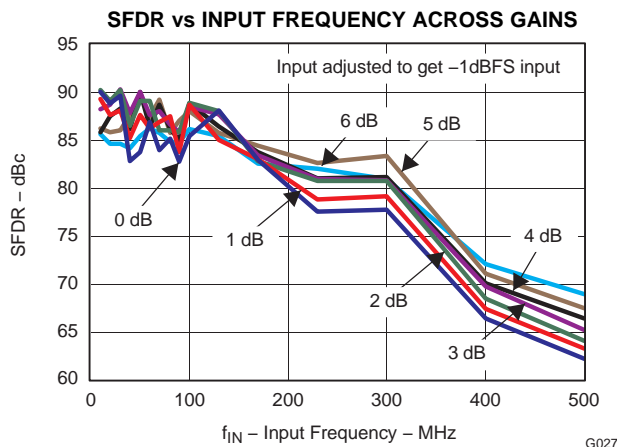


Figure 35.

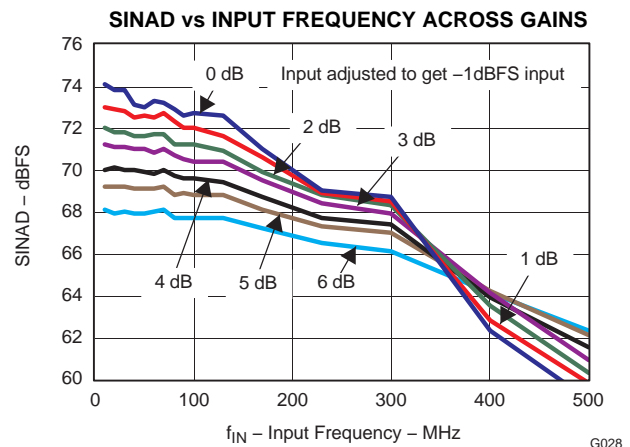


Figure 36.

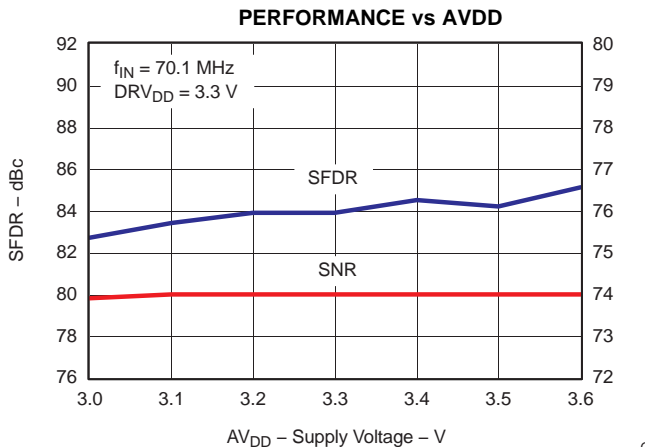


Figure 37.

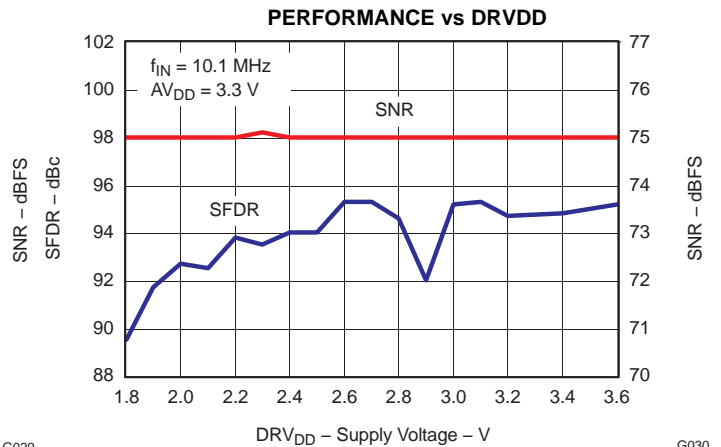


Figure 38.

**TYPICAL CHARACTERISTICS - ADS6144 (F<sub>S</sub>= 105 MSPS) (continued)**

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

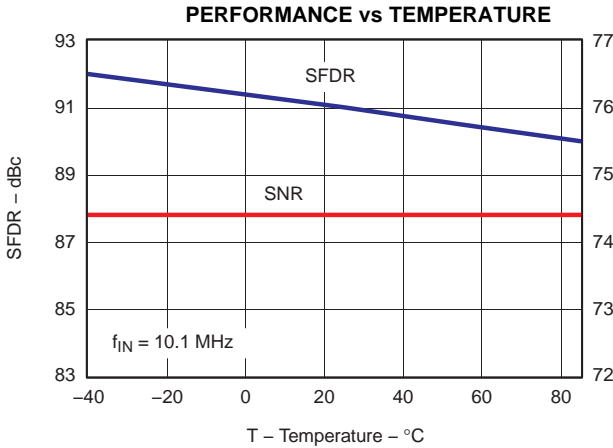


Figure 39.

G031

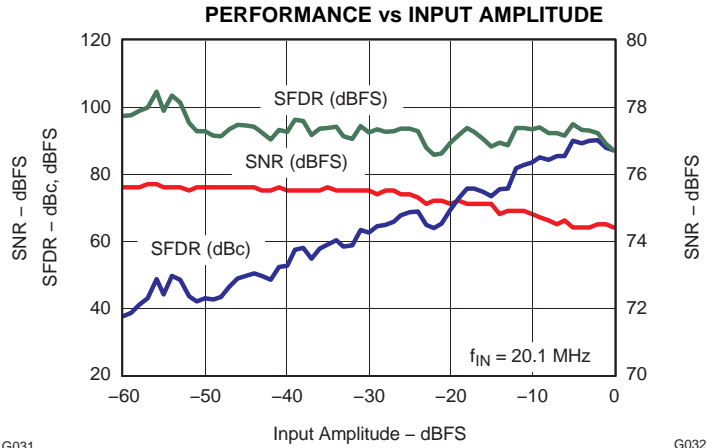


Figure 40.

G032

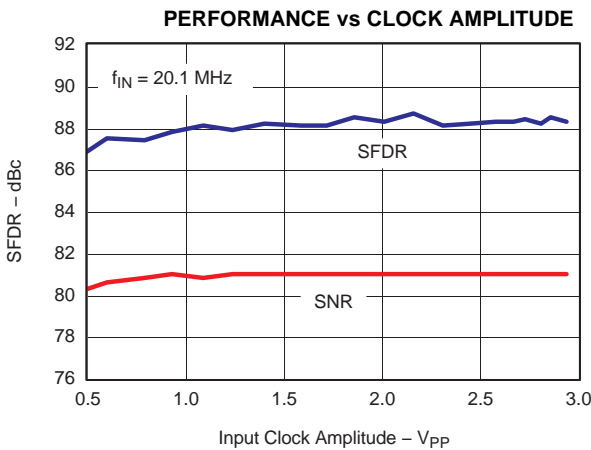


Figure 41.

G033

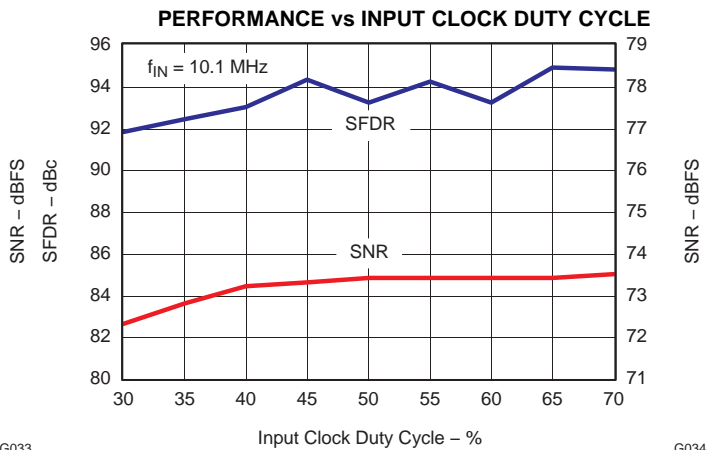


Figure 42.

G034

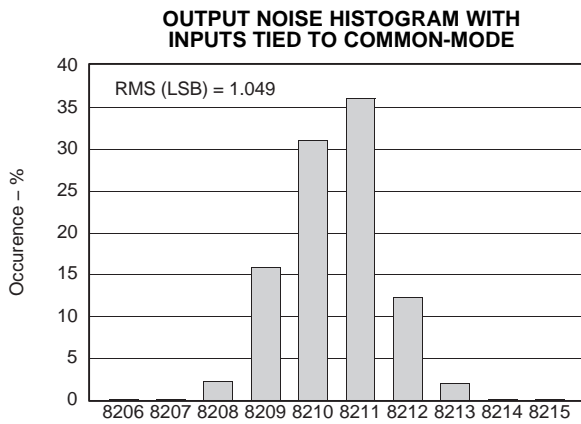


Figure 43.

G035

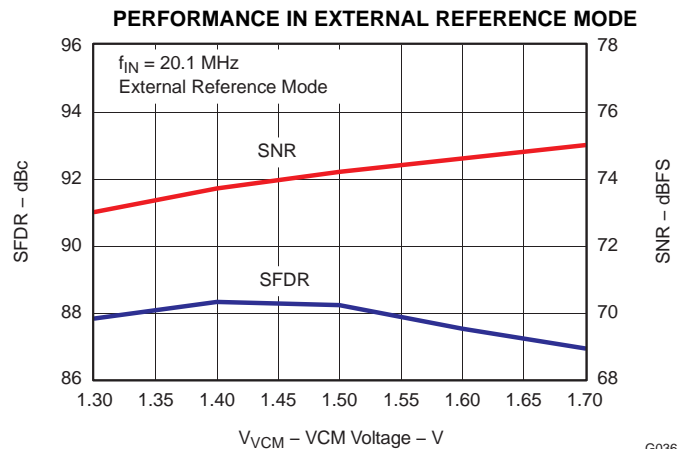


Figure 44.

G036

### TYPICAL CHARACTERISTICS - ADS6143 ( $F_S = 80$ MSPS)

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

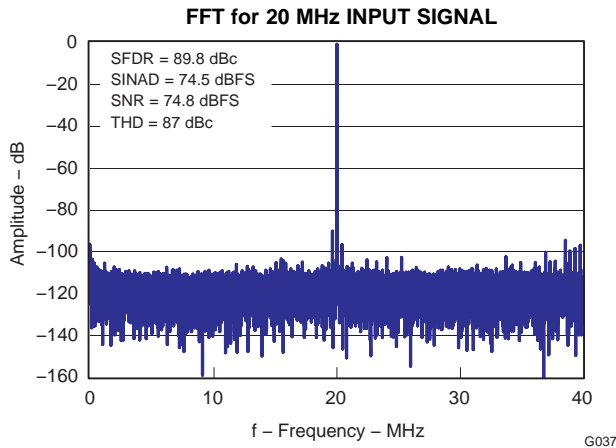


Figure 45.

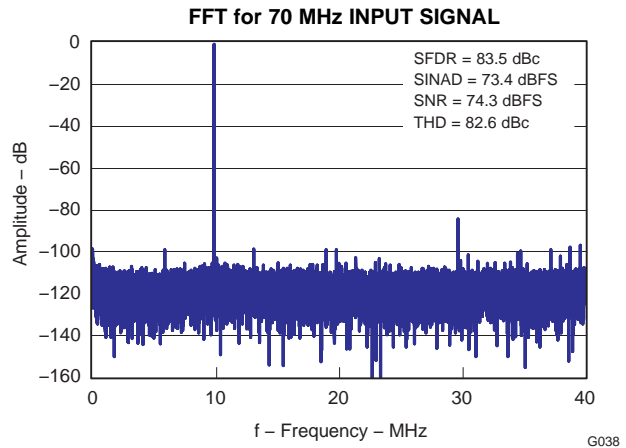


Figure 46.

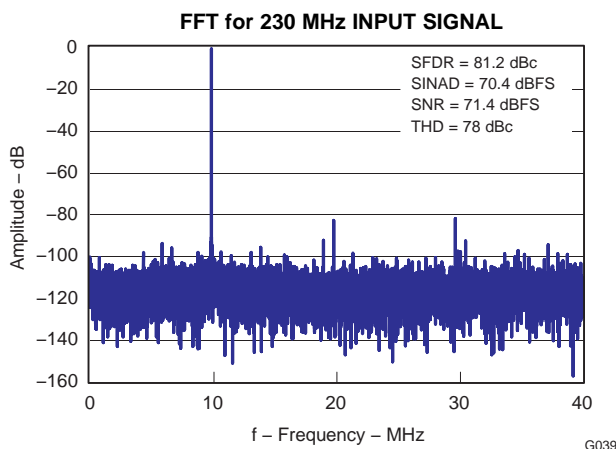


Figure 47.

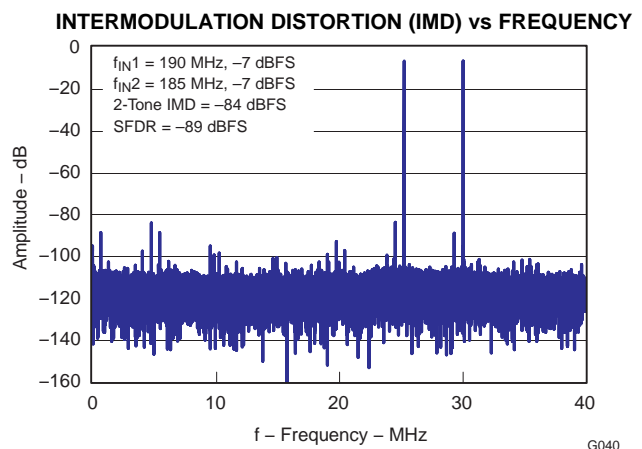


Figure 48.

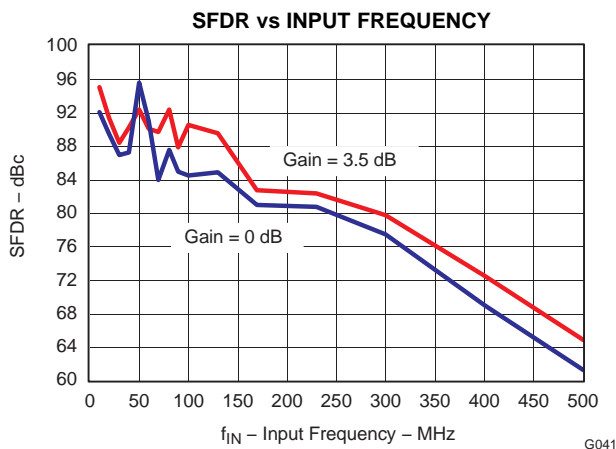


Figure 49.

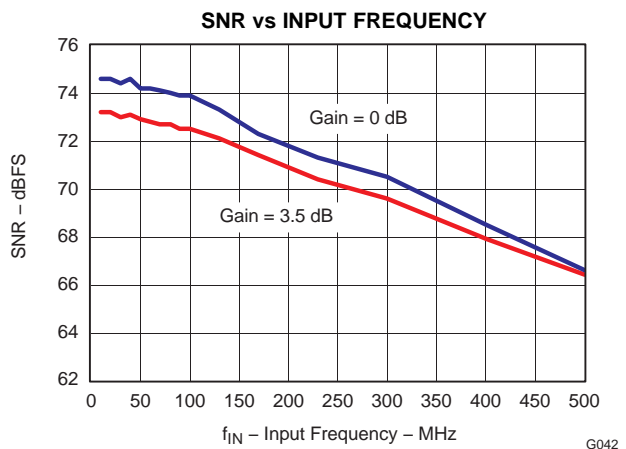


Figure 50.

**TYPICAL CHARACTERISTICS - ADS6143 (F<sub>S</sub>= 80 MSPS) (continued)**

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

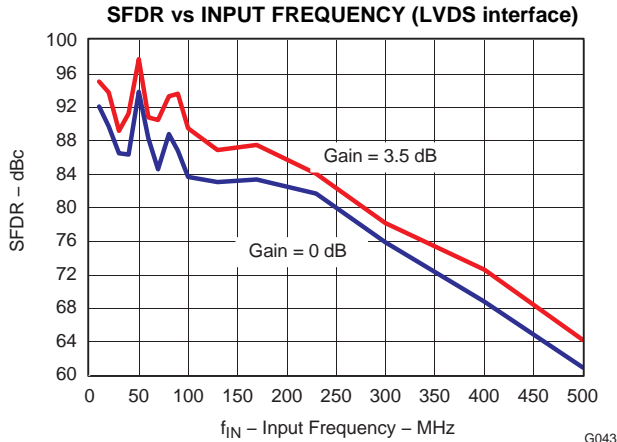


Figure 51.

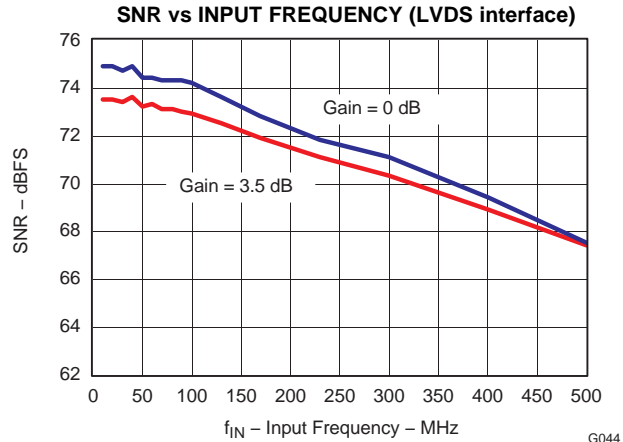


Figure 52.

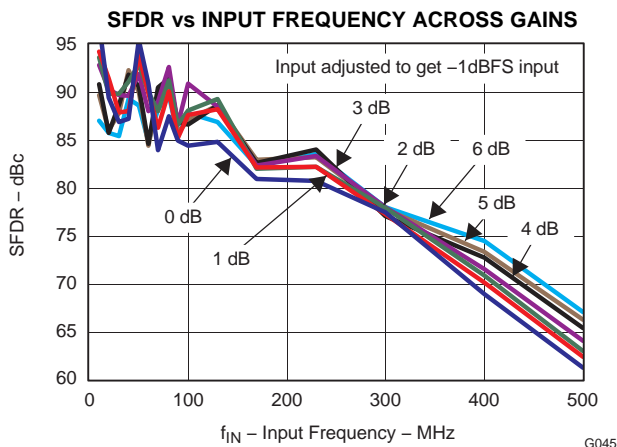


Figure 53.

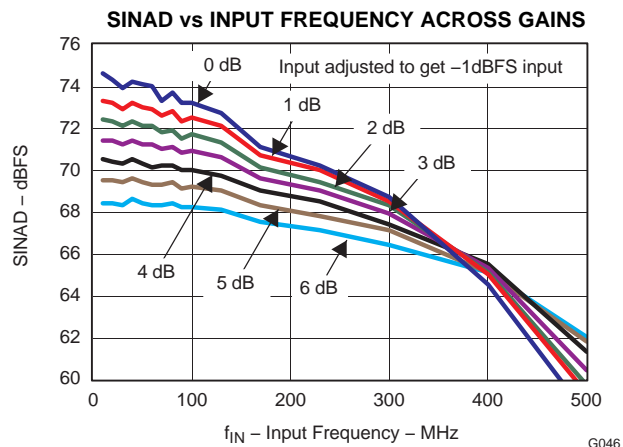


Figure 54.

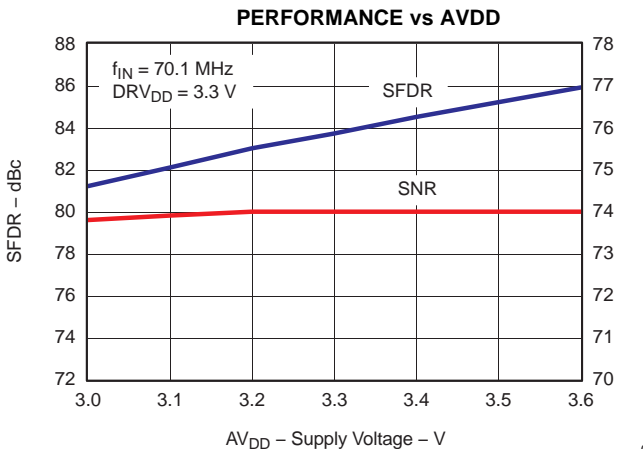


Figure 55.

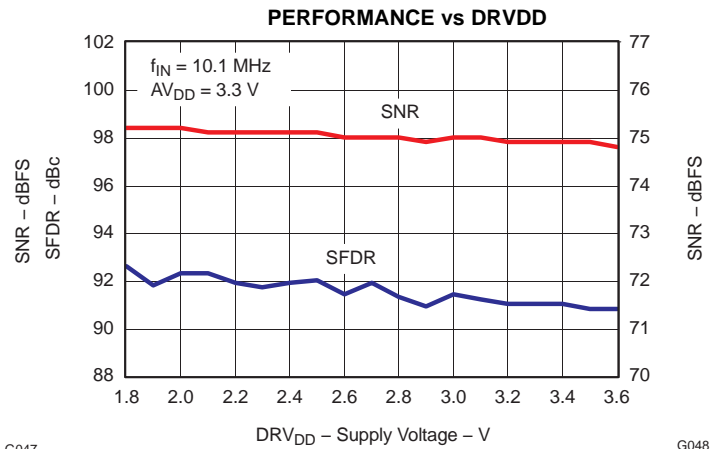


Figure 56.

**TYPICAL CHARACTERISTICS - ADS6143 ( $F_s= 80$  MSPS) (continued)**

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

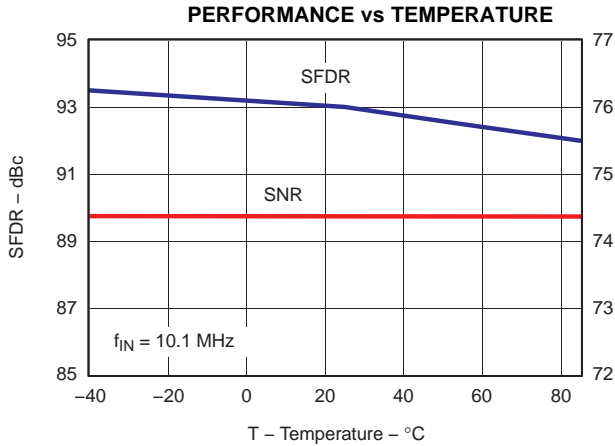


Figure 57.

G049

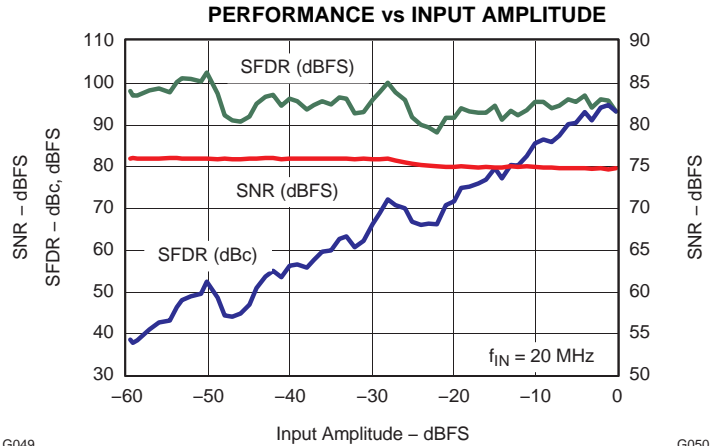


Figure 58.

G050

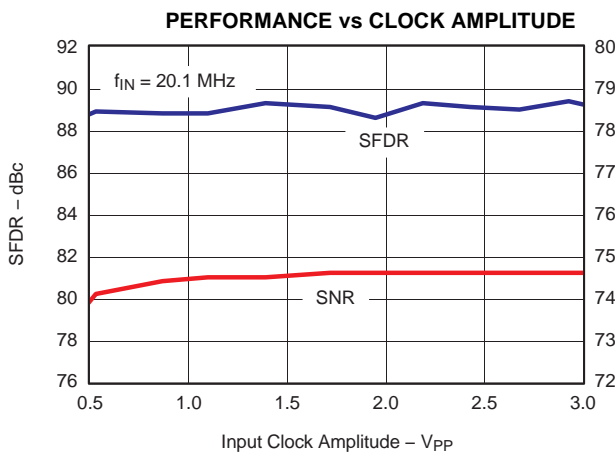


Figure 59.

G051

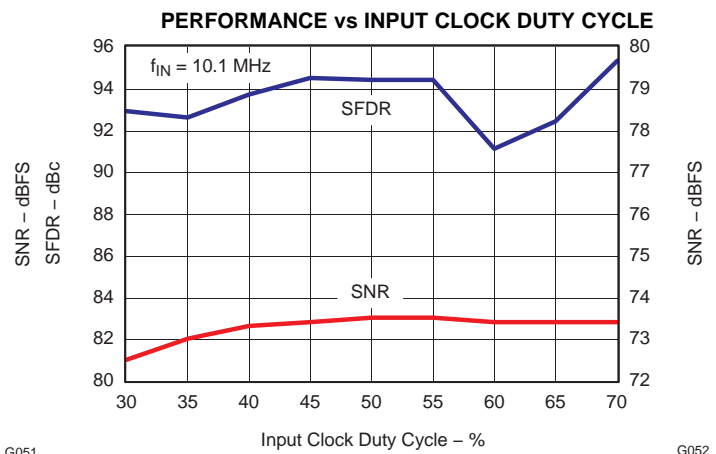


Figure 60.

G052

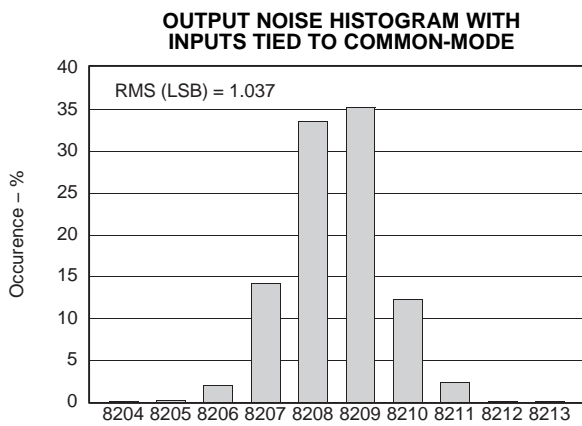


Figure 61.

G053

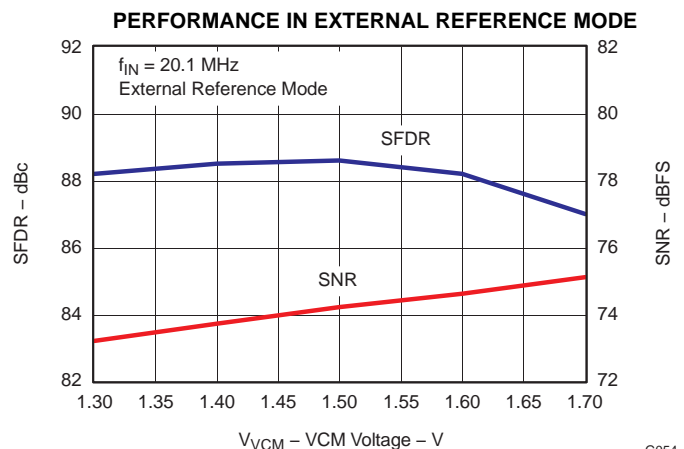


Figure 62.

G054

**TYPICAL CHARACTERISTICS - ADS6142 ( $F_S = 65$  MSPS)**

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

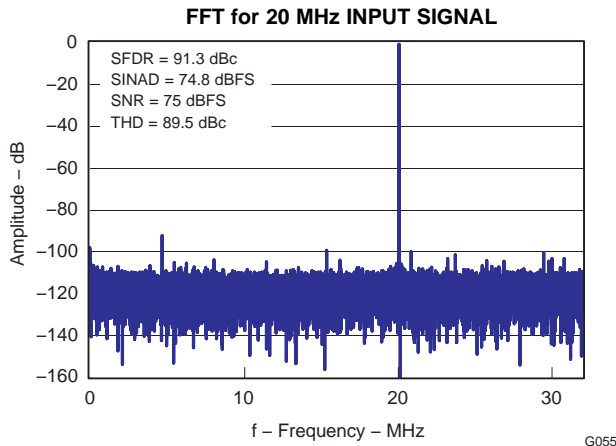


Figure 63.

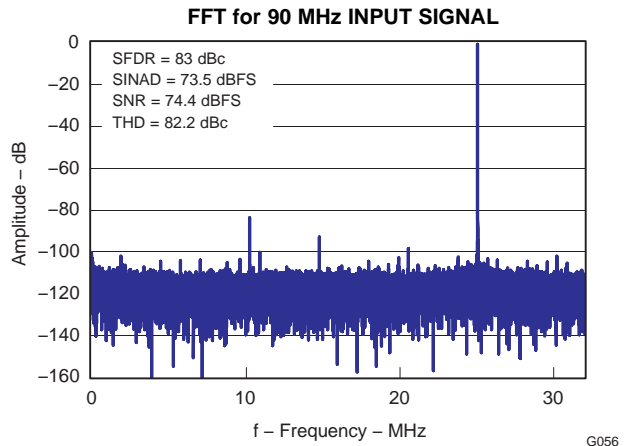


Figure 64.

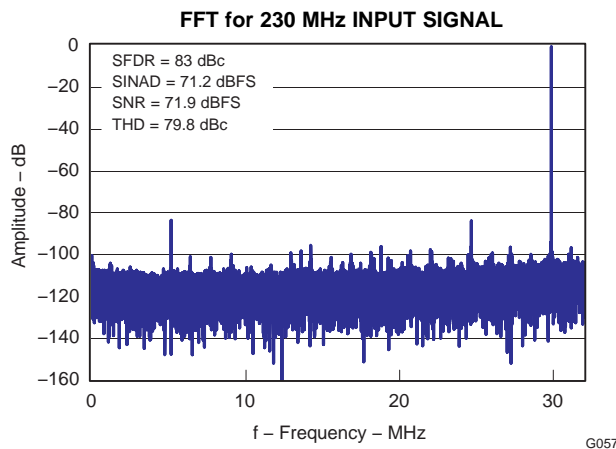


Figure 65.

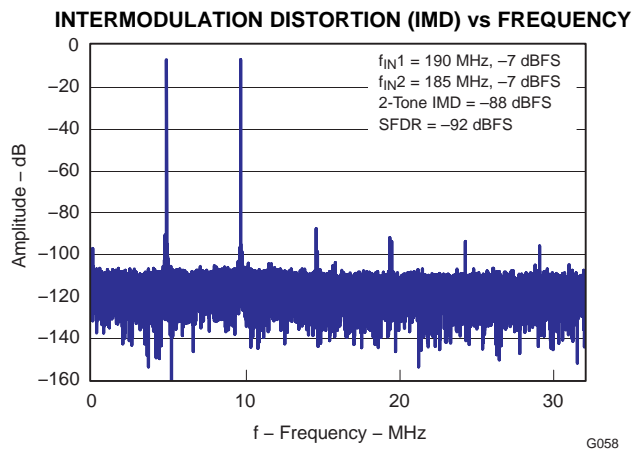


Figure 66.

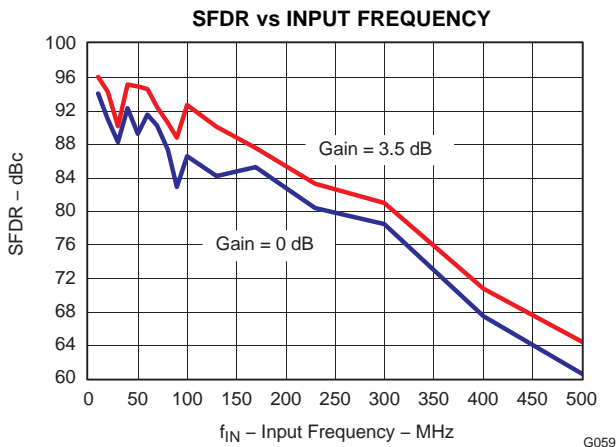


Figure 67.

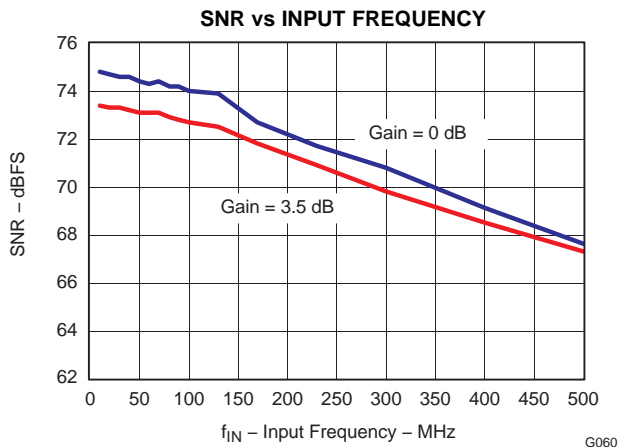


Figure 68.

**TYPICAL CHARACTERISTICS - ADS6142 ( $F_s= 65$  MSPS) (continued)**

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

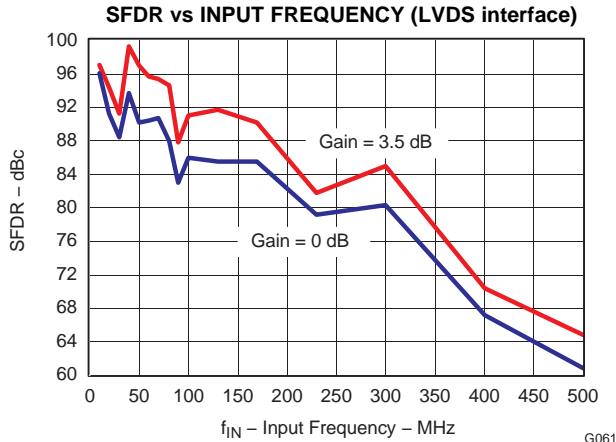


Figure 69.

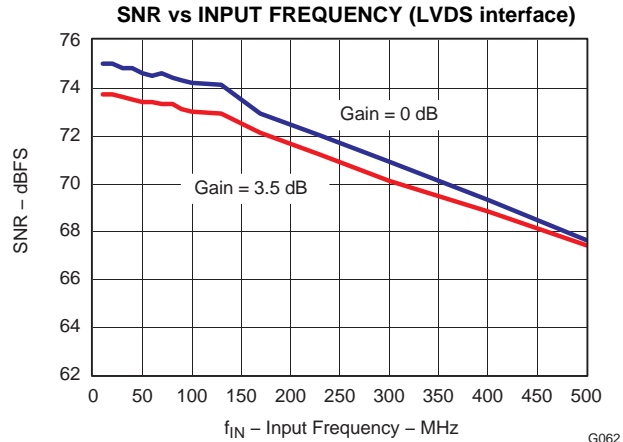


Figure 70.

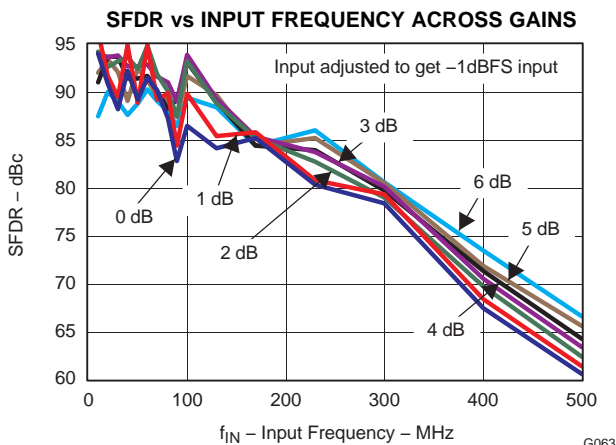


Figure 71.

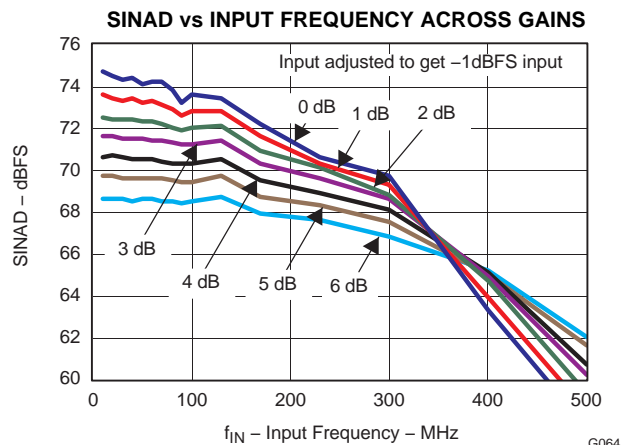


Figure 72.

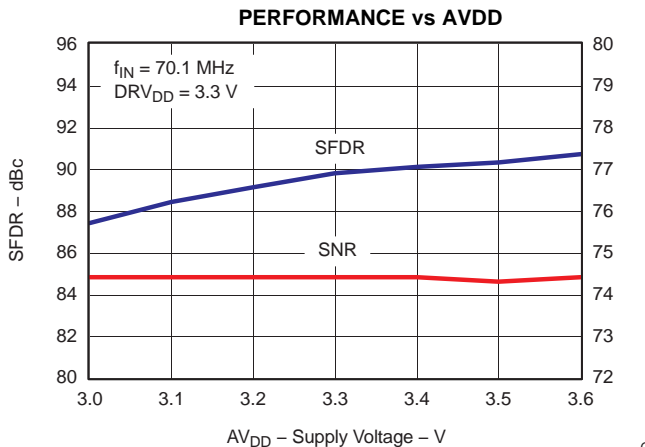


Figure 73.

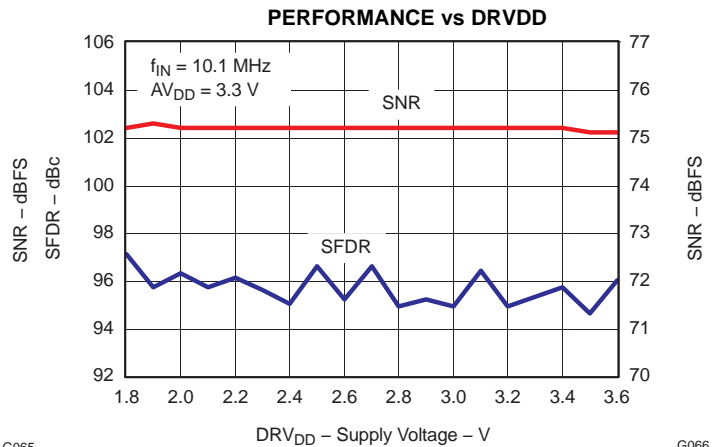


Figure 74.

**TYPICAL CHARACTERISTICS - ADS6142 (F<sub>S</sub>= 65 MSPS) (continued)**

All plots are at 25°C, AVDD = DRVDD = 3.3 V, maximum rated sampling frequency, sine wave input clock, 1.5 V<sub>PP</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

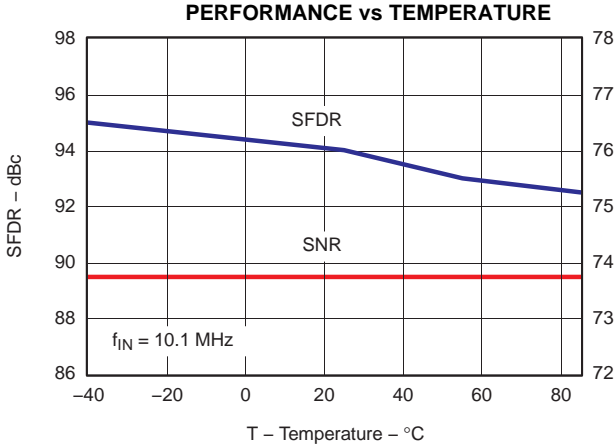


Figure 75.

G067

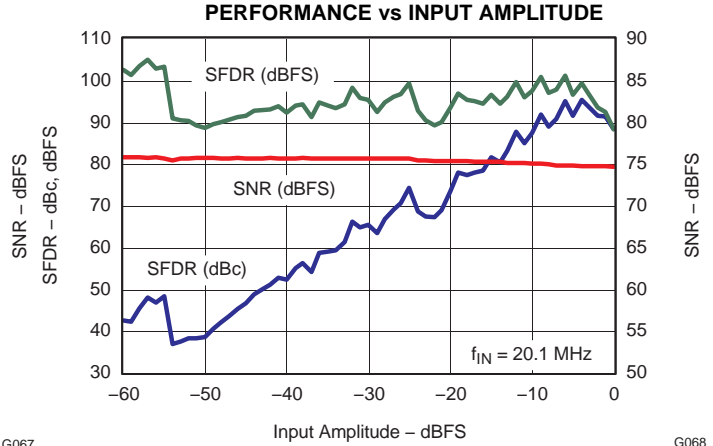


Figure 76.

G068

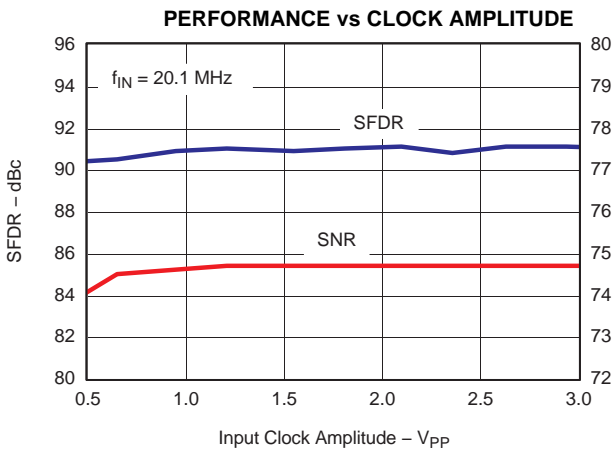


Figure 77.

G069

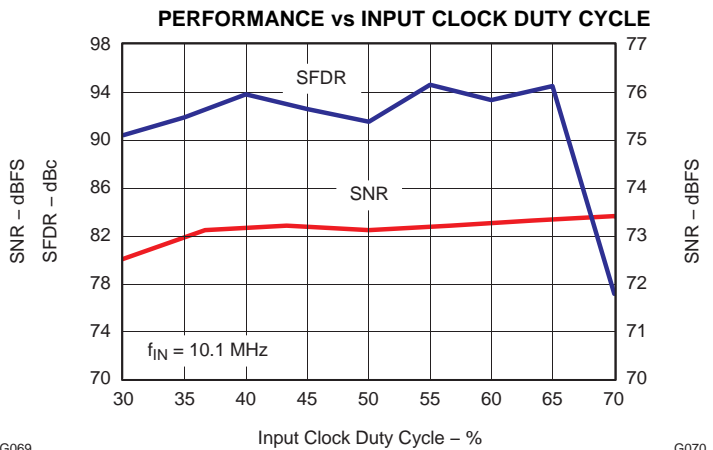


Figure 78.

G070

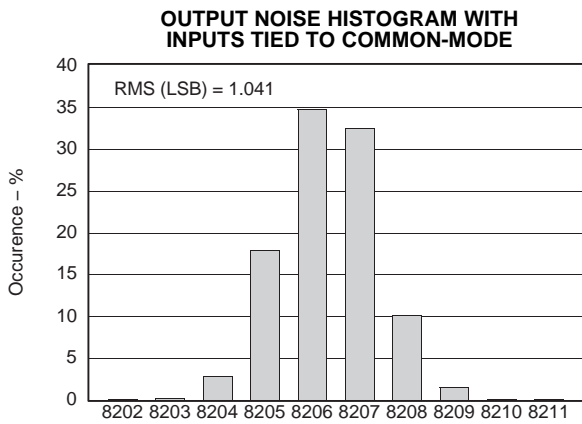


Figure 79.

G071

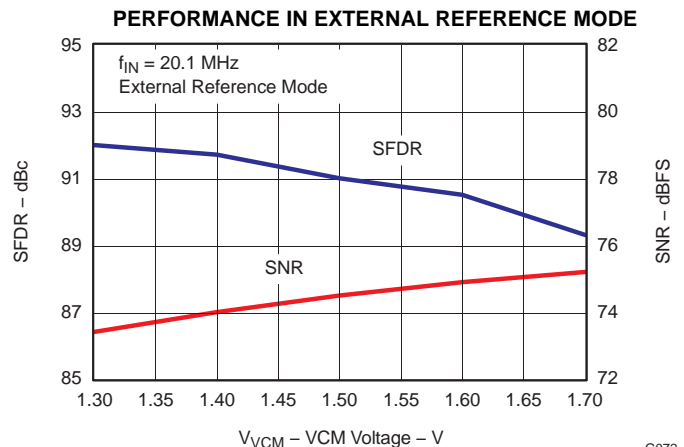


Figure 80.

G072

### TYPICAL CHARACTERISTICS - LOW SAMPLING FREQUENCIES

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sine wave input clock, 1.5 V<sub>pp</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

#### F<sub>S</sub> = 40 MSPS

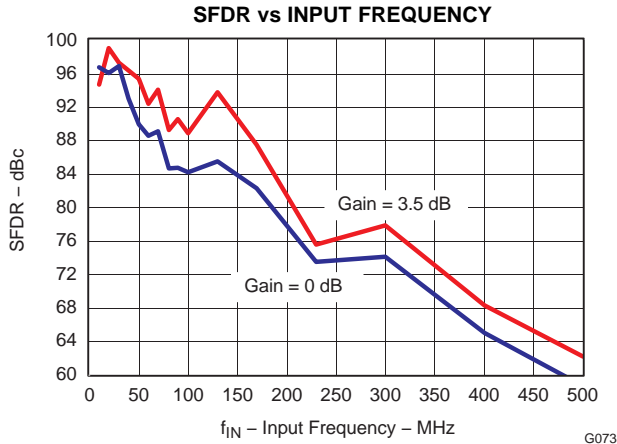


Figure 81.

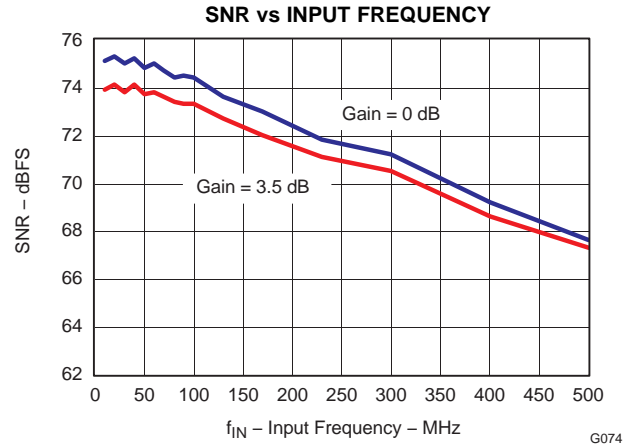


Figure 82.

#### F<sub>S</sub> = 25 MSPS

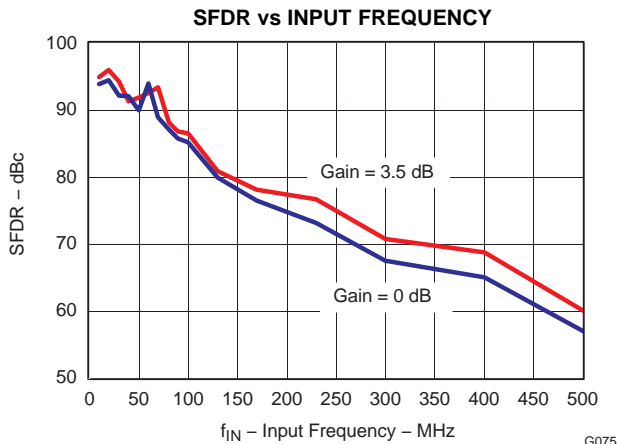


Figure 83.

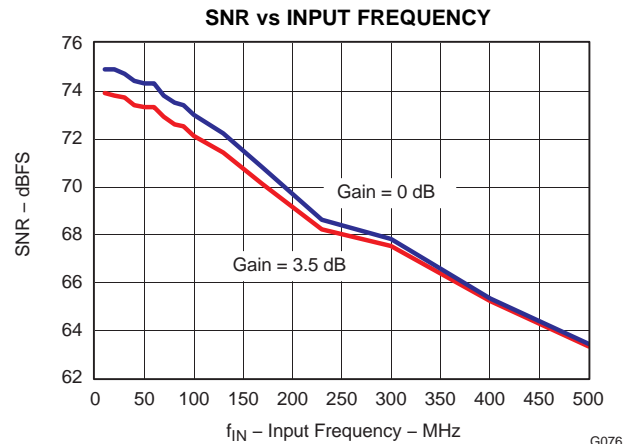


Figure 84.

### COMMON PLOTS

All plots are at 25°C, AVDD = DRVDD = 3.3 V, sine wave input clock, 1.5 V<sub>pp</sub> differential clock amplitude, 50% clock duty cycle, -1 dBFS differential analog input, internal reference mode, 0 dB gain, CMOS output interface (unless otherwise noted)

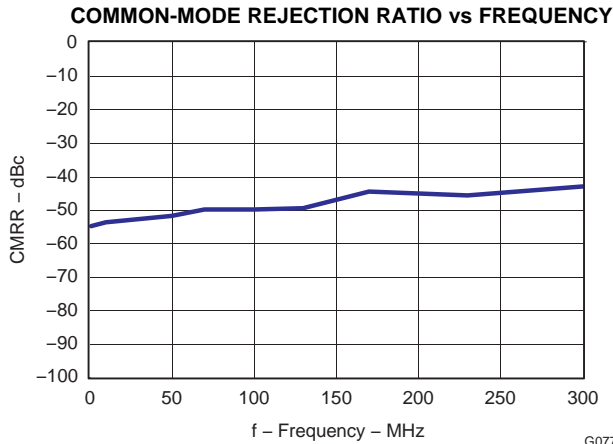


Figure 85.

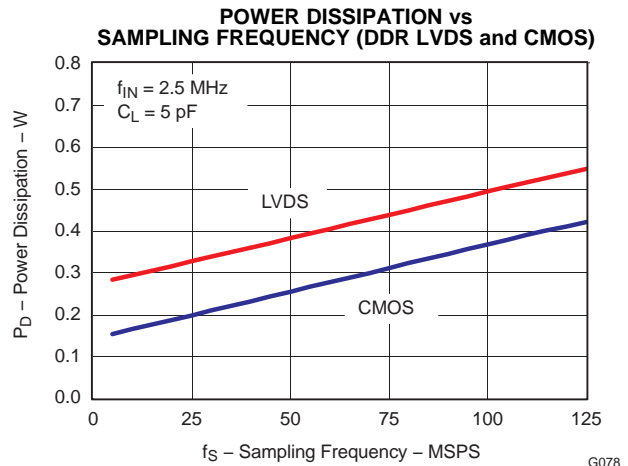


Figure 86.

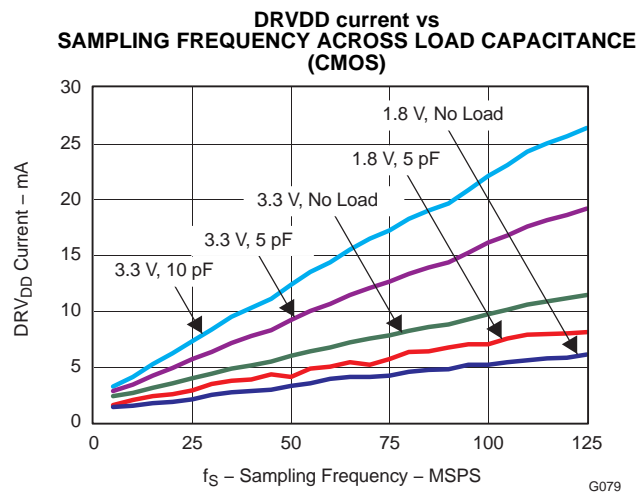
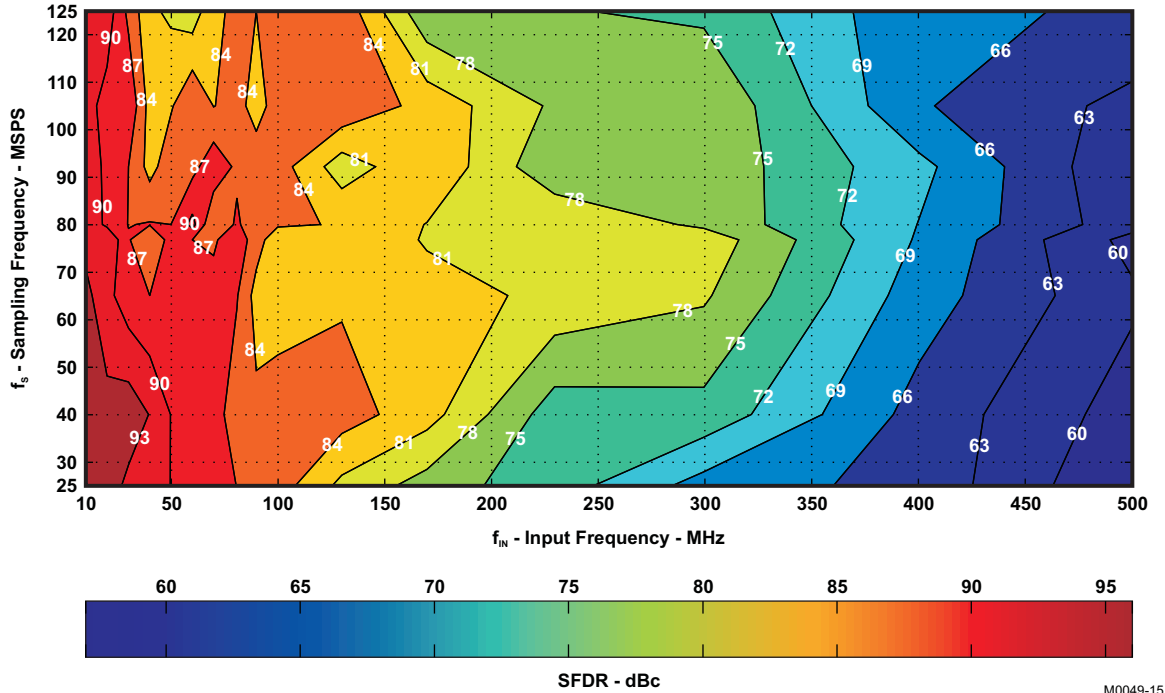


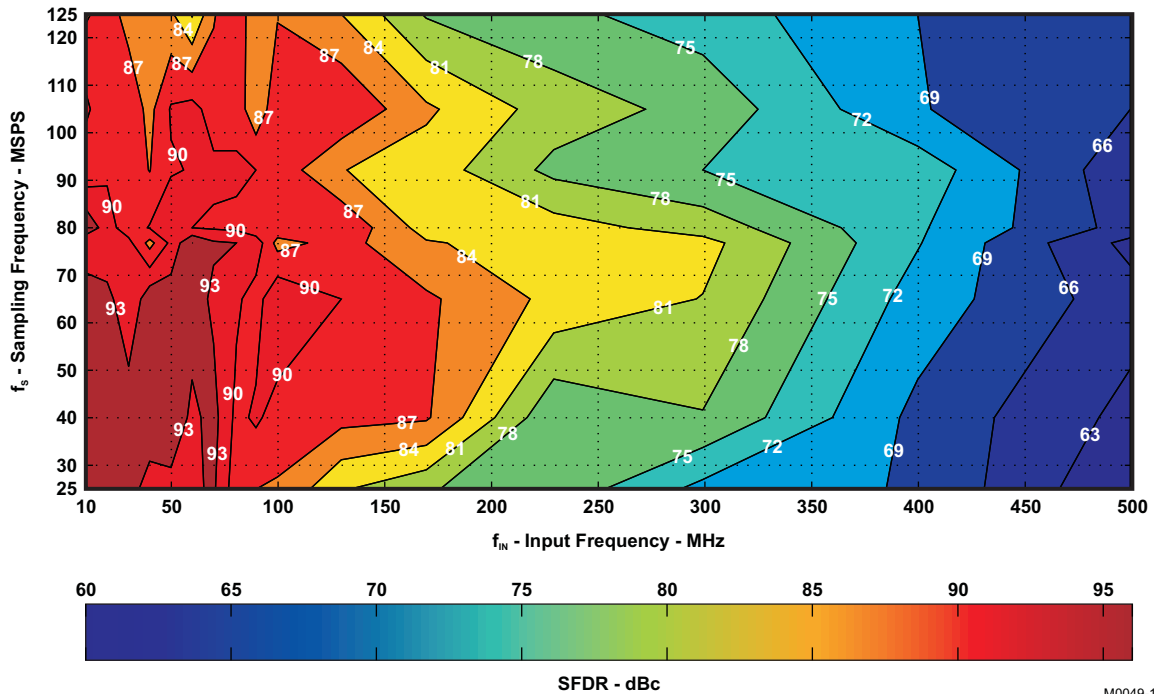
Figure 87.

Contour Plots Across Input and Sampling Frequencies



M0049-15

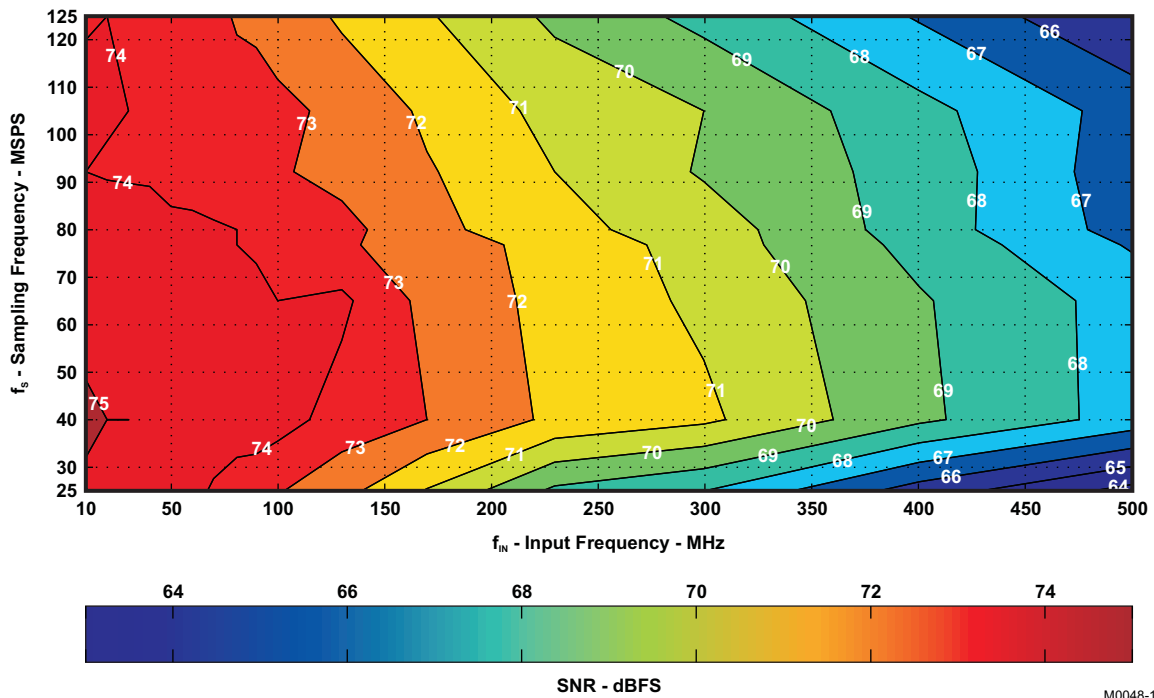
Figure 88. SFDR Contour (no gain,  $F_S = 2 V_{PP}$ )



M0049-16

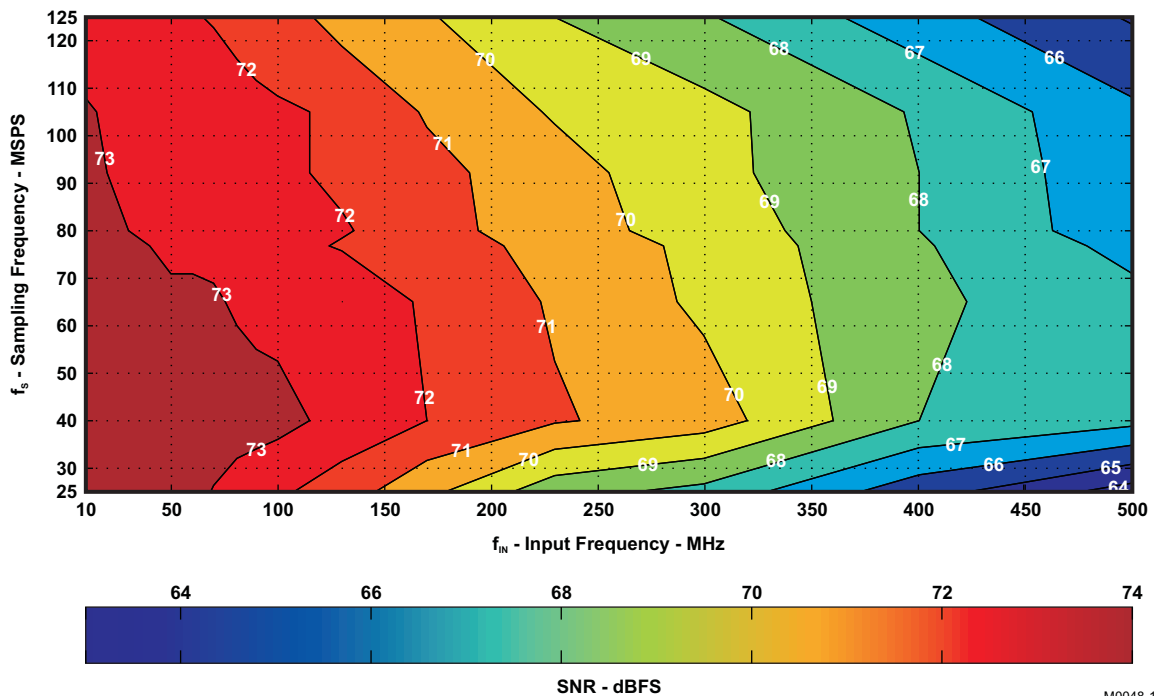
Figure 89. SFDR Contour (with 3.5 dB coarse gain,  $F_S = 1.34 V_{PP}$ )

Contour Plots Across Input and Sampling Frequencies (continued)



M0048-15

Figure 90. SNR Contour (no gain,  $F_S = 2 V_{PP}$ )



M0048-16

Figure 91. SNR Contour (with 3.5 dB coarse gain,  $F_S = 1.34 V_{PP}$ )

## APPLICATION INFORMATION

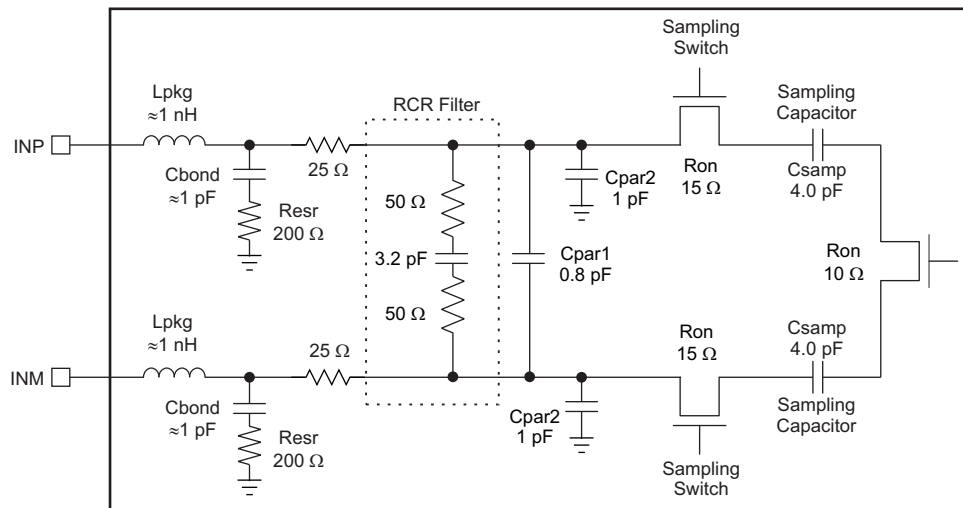
### THEORY OF OPERATION

The ADS614X devices are a family of low power, 14-bit pipeline ADCs in a CMOS process with up to a 125 MSPS sampling frequencies. These devices are based on switched capacitor technology and run off a single 3.3-V supply. The conversion process is initiated by the rising edge of the external input clock. Once the signal is captured by the input sample and hold, the input sample is sequentially converted by a series of lower resolution stages, with the outputs combined in a digital correction logic block. At every clock edge, the sample propagates through the pipeline resulting in a data latency of 9 clock cycles. The output is available as 14-bit data, in DDR LVDS or CMOS and coded in either straight offset binary or binary 2s complement format.

### ANALOG INPUT

The analog input consists of a switched-capacitor based differential sample and hold architecture, shown in Figure 92.

This differential topology results in good ac-performance even for high input frequencies at high sampling rates. The INP and INM pins have to be externally biased around a common-mode voltage of 1.5 V available on the VCM pin. For a full-scale differential input, each input pin (INP, INM) has to swing symmetrically between  $V_{CM} + 0.5$  V and  $V_{CM} - 0.5$  V, resulting in a  $2V_{PP}$  differential input swing. The maximum swing is determined by the internal reference voltages REFP (2.5 V nominal) and REFM (0.5 V, nominal).



**Figure 92. Input Stage**

The input sampling circuit has a high 3dB bandwidth that extends up to 450 MHz (measured from the input pins to the voltage across the sampling capacitors).

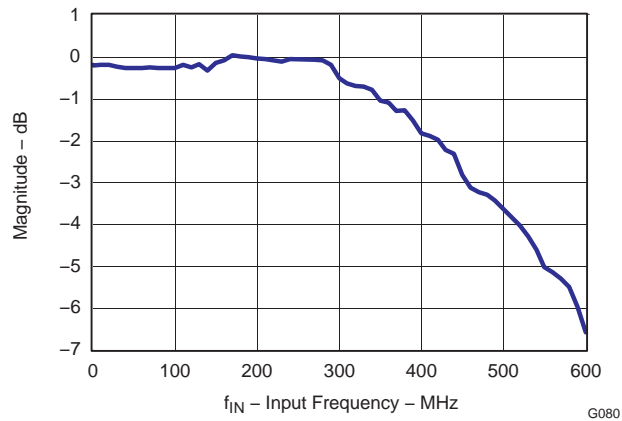


Figure 93. ADC Analog Input Bandwidth

### Drive Circuit Requirements

For optimum performance, the analog inputs must be driven differentially. This improves the common-mode noise immunity and even-order harmonic rejection.

A 5-Ω resistor in series with each input pin is recommended to damp out ringing caused by the package parasitics. It is also necessary to present low impedance (< 50 Ω) for the common-mode switching currents. For example, this is achieved by using two resistors from each input terminated to the common-mode voltage (VCM).

In addition to the above, the drive circuit may have to be designed to provide a low insertion loss over the desired frequency range and matched impedance to the source. While doing this, the ADC input impedance ( $Z_{in}$ ) must be considered. Over a wide frequency range, the input impedance can be approximated by a parallel combination of  $R_{in}$  and  $C_{in}$  ( $Z_{in} = R_{in} || C_{in}$ ).

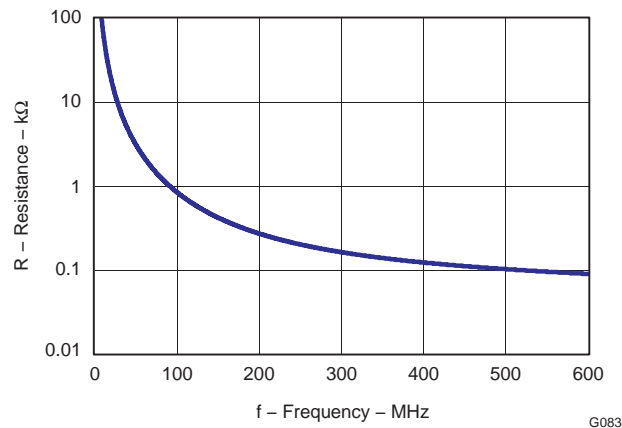


Figure 94. ADC Input Resistance,  $R_{in}$

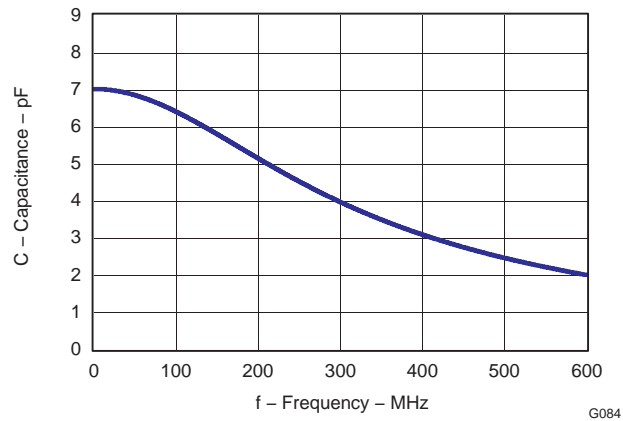


Figure 95. ADC Input Capacitance,  $C_{in}$

### Using RF-Transformer Based Drive Circuits

Figure 96 shows a configuration using a single 1:1 turn ratio transformer (for example, Coilcraft WBC1-1) that can be used for low input frequencies (about 100 MHz).

The single-ended signal is fed to the primary winding of the RF transformer. The transformer is terminated on the secondary side. Putting the termination on the secondary side helps to shield the kickbacks caused by the sampling circuit from the RF transformer's leakage inductances. The termination is accomplished by two resistors connected in series, with the center point connected to the 1.5 V common mode (VCM pin). The value of the termination resistors (connected to common mode) has to be low ( $< 100 \Omega$ ) to provide a low-impedance path for the ADC common-mode switching current.

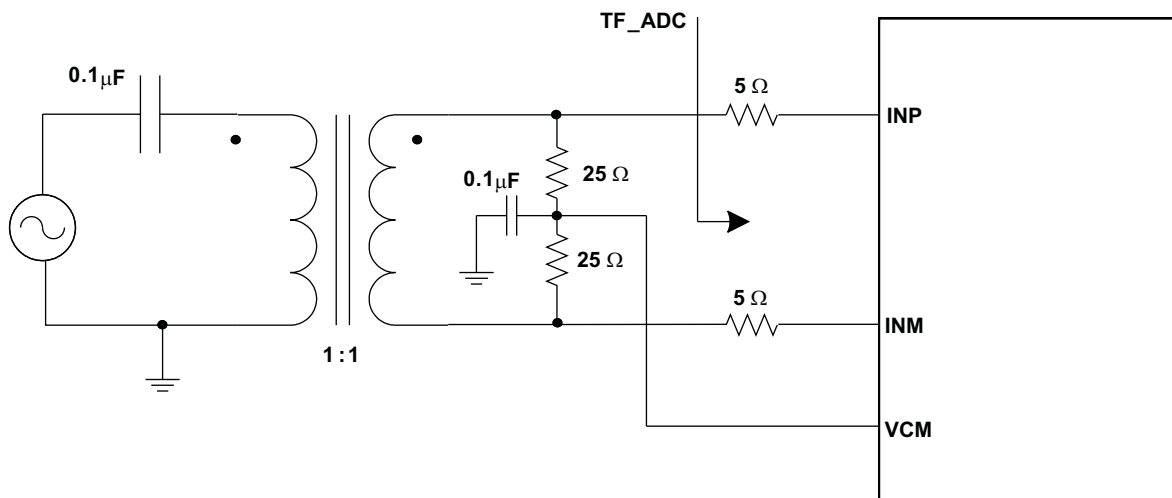


Figure 96. Single Transformer Drive Circuit

At high input frequencies, the mismatch in the transformer parasitic capacitance (between the windings) results in degraded even-order harmonic performance. Connecting two identical RF transformers back-to-back helps minimize this mismatch, and good performance is obtained for high frequency input signals. Figure 97 shows an example using two transformers (Coilcraft WBC1-1). An additional termination resistor pair (enclosed within the dotted box in Figure 97) may be required between the two transformers to improve the balance between the P and M sides. The center point of this termination must be connected to ground.

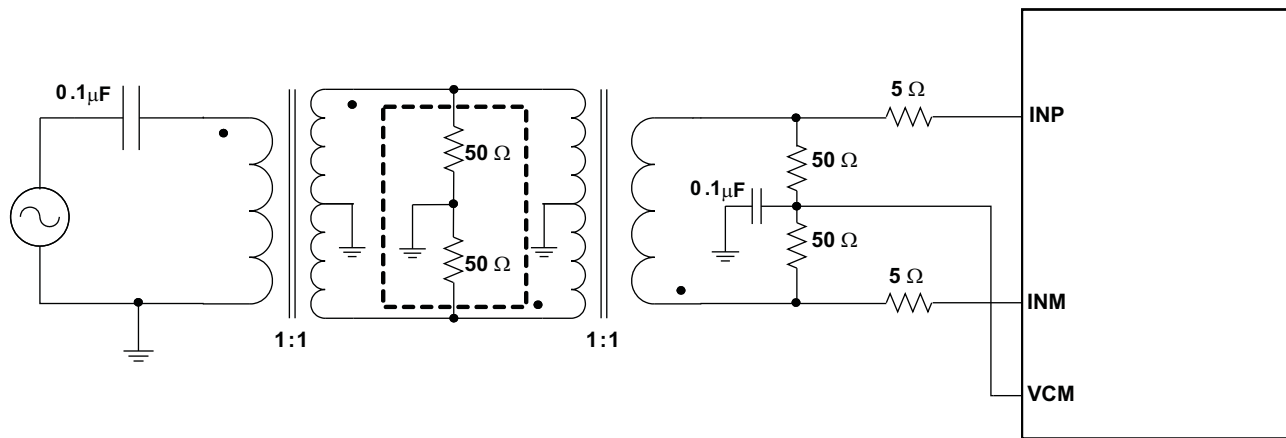


Figure 97. Two Transformer Drive Circuit

### Using Differential Amplifier Drive Circuits

Figure 98 shows a drive circuit using a differential amplifier (TI's THS4509) to convert a single-ended input to a differential output that can be interfaced to the ADC analog input pins. In addition to the single-ended to differential conversion, the amplifier also provides gain (10 dB in Figure 98).  $R_{FIL}$  helps to isolate the amplifier outputs from the switching input of the ADC. Together with  $C_{FIL}$  it also forms a low-pass filter that band-limits the noise (and signal) at the ADC input. As the amplifier output is ac-coupled, the common-mode voltage of the ADC input pins is set using two 200- $\Omega$  resistors connected to VCM.

The amplifier output can also be dc-coupled. Using the output common-mode control of the THS4509, the ADC input pins can be biased to 1.5 V. In this case, use +4-V and –1-V supplies for the THS4509 so that its output common-mode voltage (1.5 V) is at mid-supply.

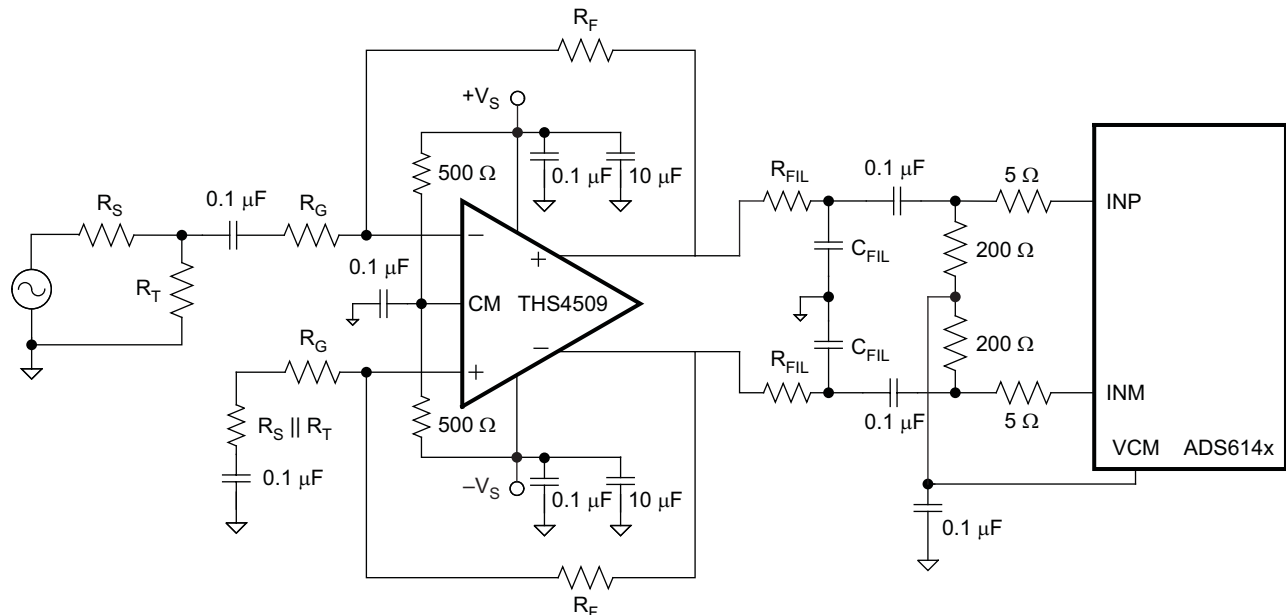


Figure 98. Drive Circuit Using the THS4509

See the EVM User Guide (SLWU028) for more information.

## Input Common Mode

To ensure a low-noise common-mode reference, the VCM pin is filtered with a 0.1- $\mu$ F low-inductance capacitor connected to ground. The VCM pin is designed to directly drive the ADC inputs. The input stage of the ADC sinks a common-mode current in the order of 180  $\mu$ A (at 125 MSPS). Equation 1 describes the dependency of the common-mode current and the sampling frequency.

$$180 \mu\text{A} \times \frac{F_s}{125 \text{ MSPS}} \quad (1)$$

Equation 1 helps to design the output capability and impedance of the CM driving circuit.

## REFERENCE

The ADS614X have built-in internal references REFP and REFM, requiring no external components. Design schemes are used to linearize the converter load seen by the references; this and the integration of the requisite reference capacitors on-chip eliminates the need for external decoupling. The full-scale input range of the converter is controlled in the external reference mode as explained below. The internal or external reference modes can be selected by programming the serial interface register bit <REF> (Table 5).

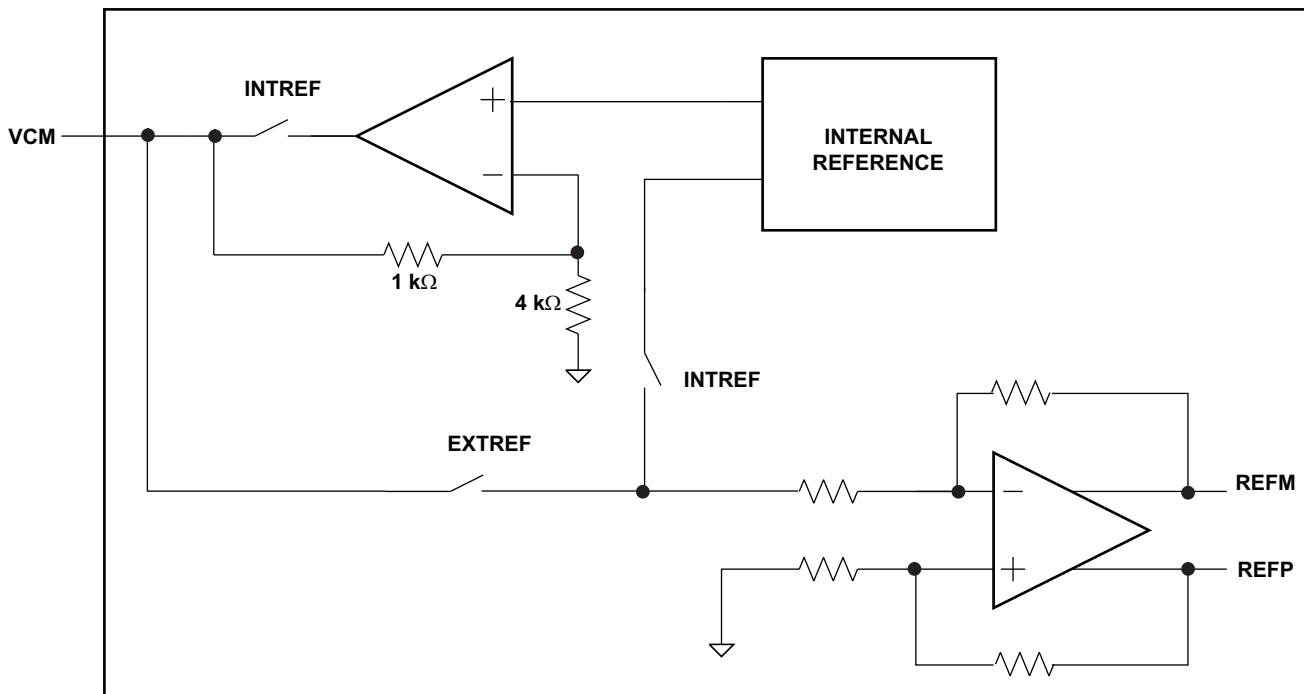


Figure 99. Reference Section

### Internal Reference

When the device is in internal reference mode, the REFP and REFM voltages are generated internally. Common-mode voltage (1.5 V nominal) is output on the VCM pin, which can be used to externally bias the analog input pins.

### External Reference

When the device is in external reference mode, VCM acts as a reference input pin. The voltage forced on the VCM pin is buffered and gained by 1.33 internally, generating the REFP and REFM voltages. The differential input voltage corresponding to full-scale is given by Equation 2.

$$\text{Full-scale differential input pp} = (\text{Voltage forced on VCM}) \times 1.33 \quad (2)$$

In this mode, the 1.5-V common-mode voltage to bias the input pins has to be generated externally. There is no change in performance compared to internal reference mode.

## COARSE GAIN AND PROGRAMMABLE FINE GAIN

The ADS614X include gain settings that can be used to improve SFDR performance (compared to 0 dB gain mode). The gain settings are 3.5 dB coarse gain and 0 dB to 6 dB programmable fine gain. For each gain setting, the analog input full-scale range scales proportionally, as shown in [Table 13](#).

The coarse gain is a fixed setting of 3.5 dB and is designed to improve SFDR with little degradation in SNR (as shown in [Figure 13](#) and [Figure 14](#)). The fine gain is programmable in 1 dB steps from 0 dB to 6 dB. With fine gain, SFDR improvement is also achieved, but at the expense of SNR (there is about 1 dB SNR degradation for every 1 dB of fine gain).

So, the fine gain can be used to trade-off between SFDR and SNR. The coarse gain makes it possible to get the best SFDR but without losing SNR significantly. At high input frequencies, the gains are especially useful as the SFDR improvement is significant with marginal degradation in SINAD. The gains can be programmed using the register bits <COARSE GAIN> (see [Table 5](#)) and <FINE GAIN> (see [Table 10](#)). Note that the default gain after reset is 0 dB.

**Table 13. Full-Scale Range Across Gains**

GAIN, dB	TYPE	FULL-SCALE RANGE, V <sub>PP</sub>
0	Default after reset	2.00
3.5	Coarse setting (fixed)	1.34
1	Fine gain (programmable)	1.78
2		1.59
3		1.42
4		1.26
5		1.12
6		1.00

## CLOCK INPUT

The clock inputs of the ADS614X can be driven differentially (SINE, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between configurations. The common-mode voltage of the clock inputs is set to VCM using internal 5-k $\Omega$  resistors as shown in Figure 100. This allows the use of transformer-coupled drive circuits for the sine wave clock, or ac-coupling for the LVPECL, LVDS clock sources (see Figure 102 and Figure 103).

For best performance, it is recommended to drive the clock inputs differentially, reducing susceptibility to common-mode noise. In this case, it is best to connect both clock inputs to the differential input clock signal with 0.1- $\mu$ F capacitors, as shown in Figure 102. A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1- $\mu$ F capacitor, as shown in Figure 103.

For high input frequency sampling, a clock source with very low jitter is recommended. Band-pass filtering of the clock source can help reduce the effect of jitter. There is no change in performance with a non-50% duty cycle clock input. Figure 24 shows the performance of the ADC versus clock duty cycle.

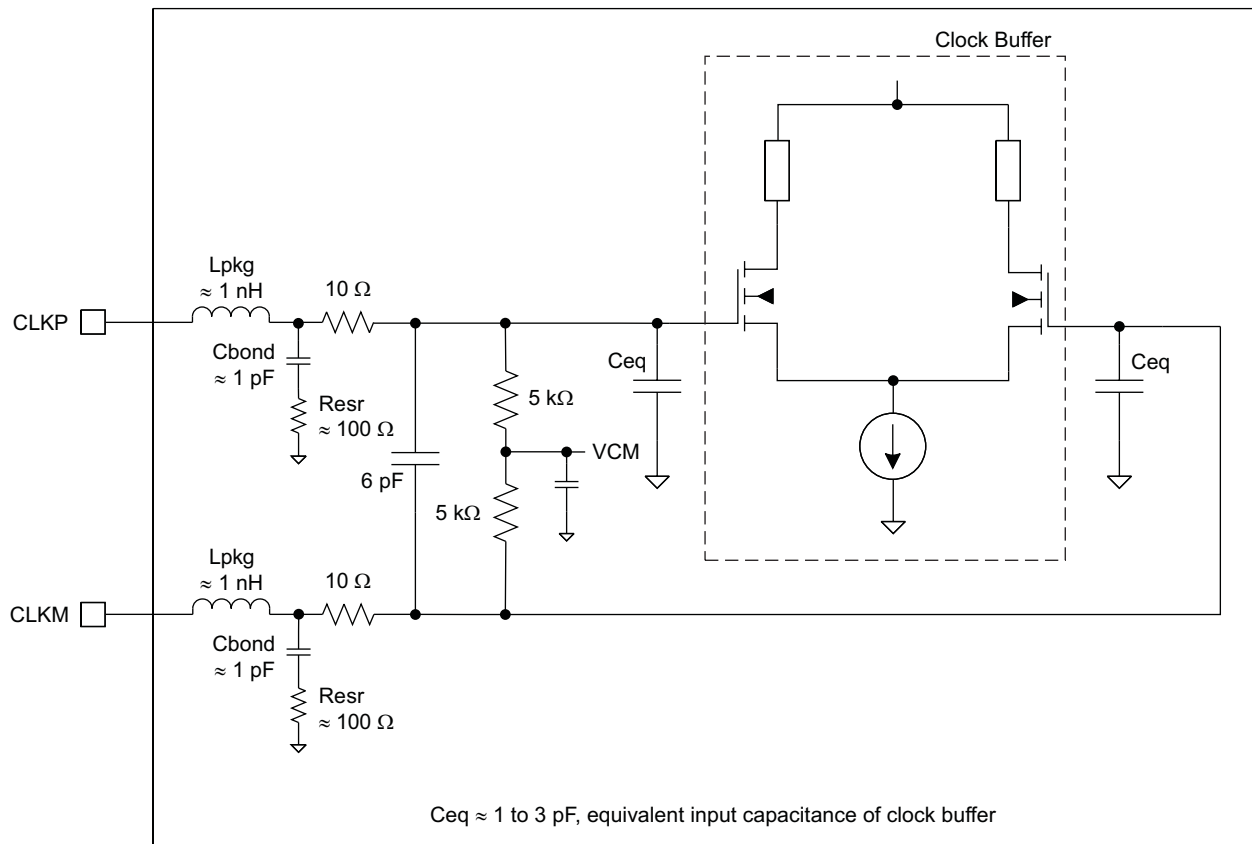


Figure 100. Internal Clock Buffer

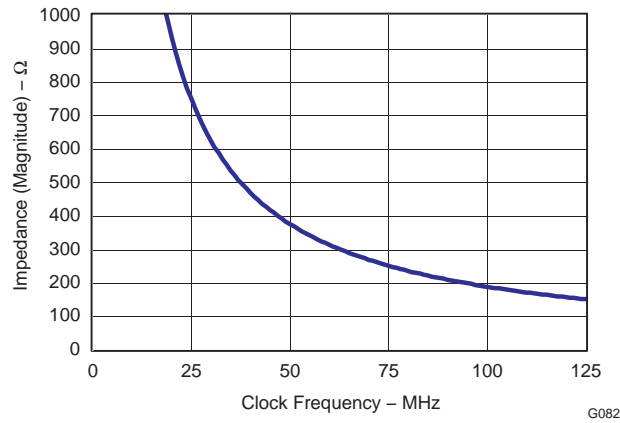


Figure 101. Clock Buffer Input Impedance

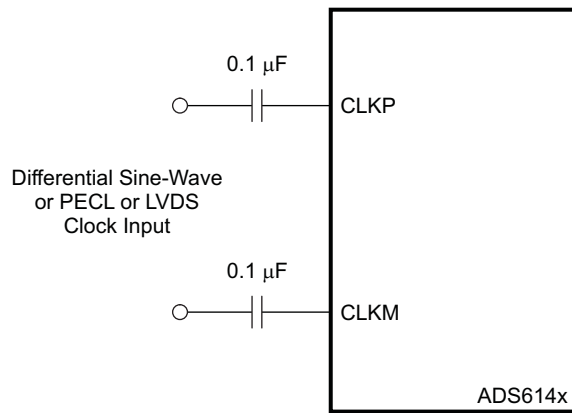


Figure 102. Differential Clock Driving Circuit

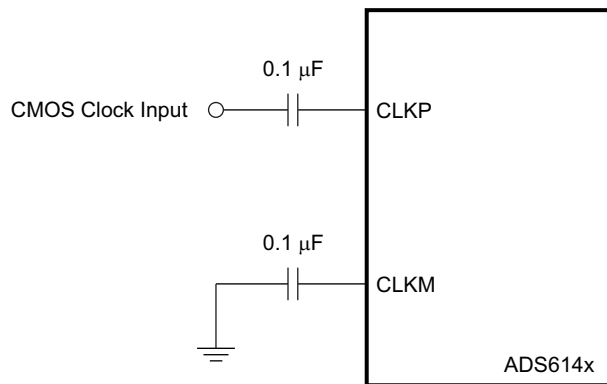


Figure 103. Single-Ended Clock Driving Circuit

## POWER-DOWN MODES

The ADS614X have four power-down modes – global power down, standby, output buffer disable, and input clock stopped. These modes can be set using the serial interface or using the parallel interface (pins SDATA and PDN).

**Table 14. Power-Down Modes**

POWER-DOWN MODES	PARALLEL INTERFACE		SERIAL INTERFACE REGISTER BIT (Table 5)	TOTAL POWER, mW	WAKE-UP TIME (to valid data)
	SDATA	PDN			
Normal operation	Low	Low	<PDN OBUF>=0 and <STBY>=0	417	-
Standby	Low	High	<PDN OBUF>=0 and <STBY>=1	72	Slow (15 $\mu$ s)
Output buffer disable	High	Low	<PDN OBUF>=1 and <STBY>=0	408	Fast (200 ns)
Global power down	High	High	<PDN OBUF>=1 and <STBY>=1	30	Slow (15 $\mu$ s)

### Global Power Down

In this mode, the A/D converter, internal references, and the output buffers are powered down and the total power dissipation reduces to about 30 mW. The output buffers are in a high-impedance state. The wake-up time from the global power down to output data becoming valid in normal mode is a maximum of 50  $\mu$ s. Note that after coming out of global power down, optimum performance is achieved after the internal reference voltages have stabilized (about 1 ms).

### Standby

Only the A/D converter is powered down and total power dissipation is approximately 72 mW. The wake-up time from standby to output data becoming valid is a maximum of 50  $\mu$ s.

### Output Buffer Disable

The data output buffers can be disabled, reducing total power to about 408 mW. With the buffers disabled, the outputs are in a high-impedance state. The wake-up time from this mode to data becoming valid in normal mode is a maximum of 500 ns in LVDS mode and 200 ns in CMOS mode.

### Input Clock Stop

The converter enters this mode when the input clock frequency falls below 1 MSPS. Power dissipation is approximately 120 mW, and the wake-up time from this mode to data becoming valid in normal mode is a maximum of 50  $\mu$ s.

### Power Supply Sequence

During power-up, the AVDD and DRVDD supplies can come up in any sequence. The two supplies are separated inside the device. Externally, they can be driven from separate supplies or from a single supply.

## DIGITAL OUTPUT INTERFACE

The ADS614X output 14 data bits together with an output clock. The output interface is either parallel CMOS or DDR LVDS voltage levels and can be selected using the serial register bit **<LVDS CMOS>** or parallel pin SEN.

### Parallel CMOS Interface

In CMOS mode, the output buffer supply (DRVDD) can be operated over a wide range from 1.8 V to 3.3 V (typical). Each data bit is output on a separate pin as a CMOS voltage level, every clock cycle.

For  $DRVDD \geq 2.2$  V, it is recommended to use the CMOS output clock (CLKOUT) to latch data in the receiving chip. The rising edge of CLKOUT can be used to latch data in the receiver, even at the highest sampling speed (125 MSPS). It is recommended to minimize the load capacitance seen by the data and clock output pins by using short traces to the receiver. Also, match the output data and clock traces to minimize the skew between them.

For  $DRVDD < 2.2$  V, it is recommended to use an external clock (for example, input clock delayed to get desired setup/hold times).

### Output Clock Position Programmability

There is an option to shift (delay) the output clock position so that the setup time increases by 400 ps (typical, with respect to the default timings specified). This may be useful if the receiver needs more setup time, especially at high sampling frequencies. This can be programmed using the serial interface register bit **<CLKOUT\_POSN>** (Table 6).

### Output Buffer Strength Programmability

Switching noise (caused by CMOS output data transitions) can couple into the analog inputs during the instant of sampling and degrade the SNR. The coupling and SNR degradation increases as the output buffer drive is made stronger. To minimize this, the ADS614X CMOS output buffers are designed with a controlled drive strength for the best SNR. The default drive strength also ensures a wide data stable window for load capacitances up to 5 pF and a DRVDD supply voltage  $\geq 2.2$  V.

To ensure a wide data stable window for load capacitances  $> 5$  pF, there is an option to increase the drive strength using the serial interface (**<DRIVE STRENGTH>**, see Table 12). Note that for a DRVDD supply voltage  $< 2.2$  V, it is recommended to use the maximum drive strength (for any value of load capacitance).

### CMOS Mode Power Dissipation

With CMOS outputs, the DRVDD current scales with the sampling frequency and the load capacitance on every output pin. The maximum DRVDD current occurs when each output bit toggles between 0 and 1 every clock cycle. In actual applications, this condition is unlikely to occur. The actual DRVDD current would be determined by the average number of output bits switching, which is a function of the sampling frequency and the nature of the analog input signal.

$$\text{Digital current due to CMOS output switching} = C_L \times DRVDD \times (N \times F_{AVG})$$

where  $C_L$  = load capacitance,  $N \times F_{AVG}$  = average number of output bits switching

Figure 87 shows the current with various load capacitances across sampling frequencies with a 2-MHz analog input frequency.

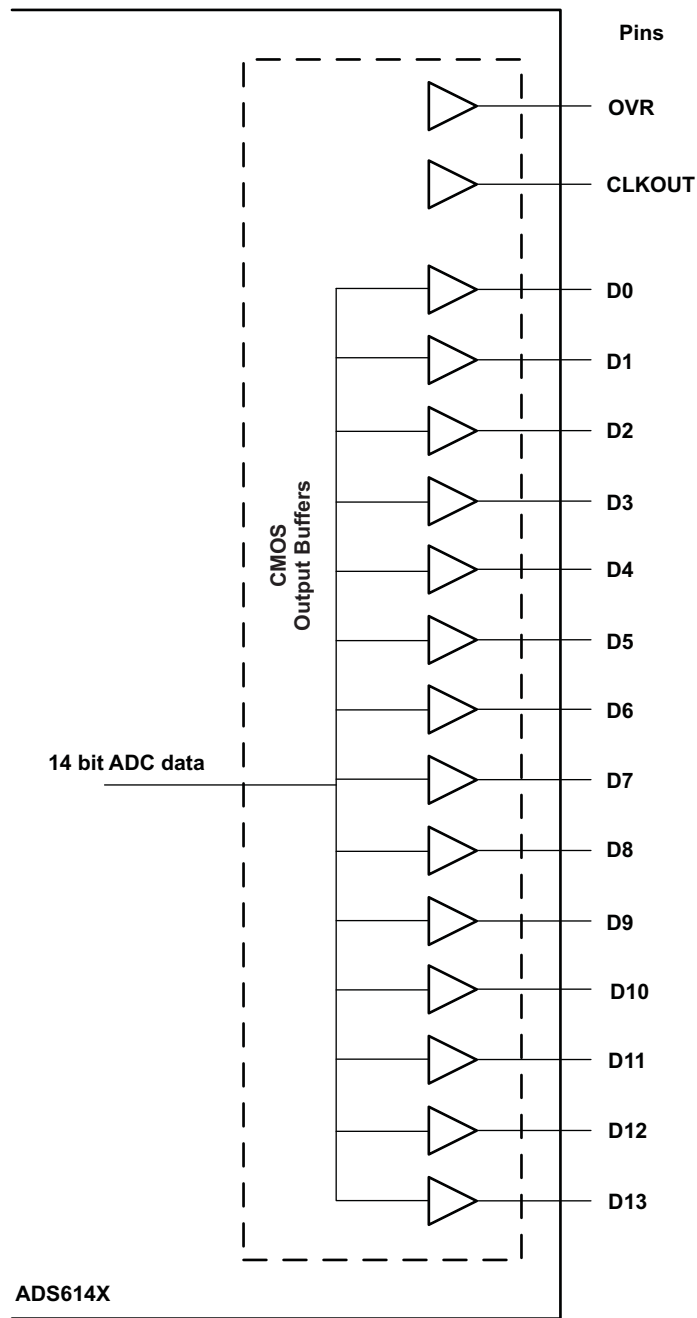


Figure 104. CMOS Output Buffers

## DDR LVDS Interface

The LVDS interface works only with a 3.3-V DRVDD supply. In this mode, the 14 data bits and the output clock are available as LVDS (Low Voltage Differential Signal) levels. Two successive data bits are multiplexed and output on each LVDS differential pair every clock cycle (DDR - Double Data Rate, see [Figure 105](#) ). So, there are 7 LVDS output pairs for the 14 data bits and 1 LVDS output pair for the output clock.

### LVDS Buffer Current Programmability

The default LVDS buffer output current is 3.5 mA. When terminated by 100  $\Omega$ , this results in a 350-mV single-ended voltage swing (700-mV<sub>PP</sub> differential swing). The LVDS buffer currents can also be programmed to 2.5 mA, 4.5 mA, and 1.75 mA (register bits <LVDS CURRENT>, see [Table 11](#)). In addition, there is a current double mode, where this current is doubled for the data and output clock buffers (register bits <CURRENT DOUBLE>, see [Table 11](#)).

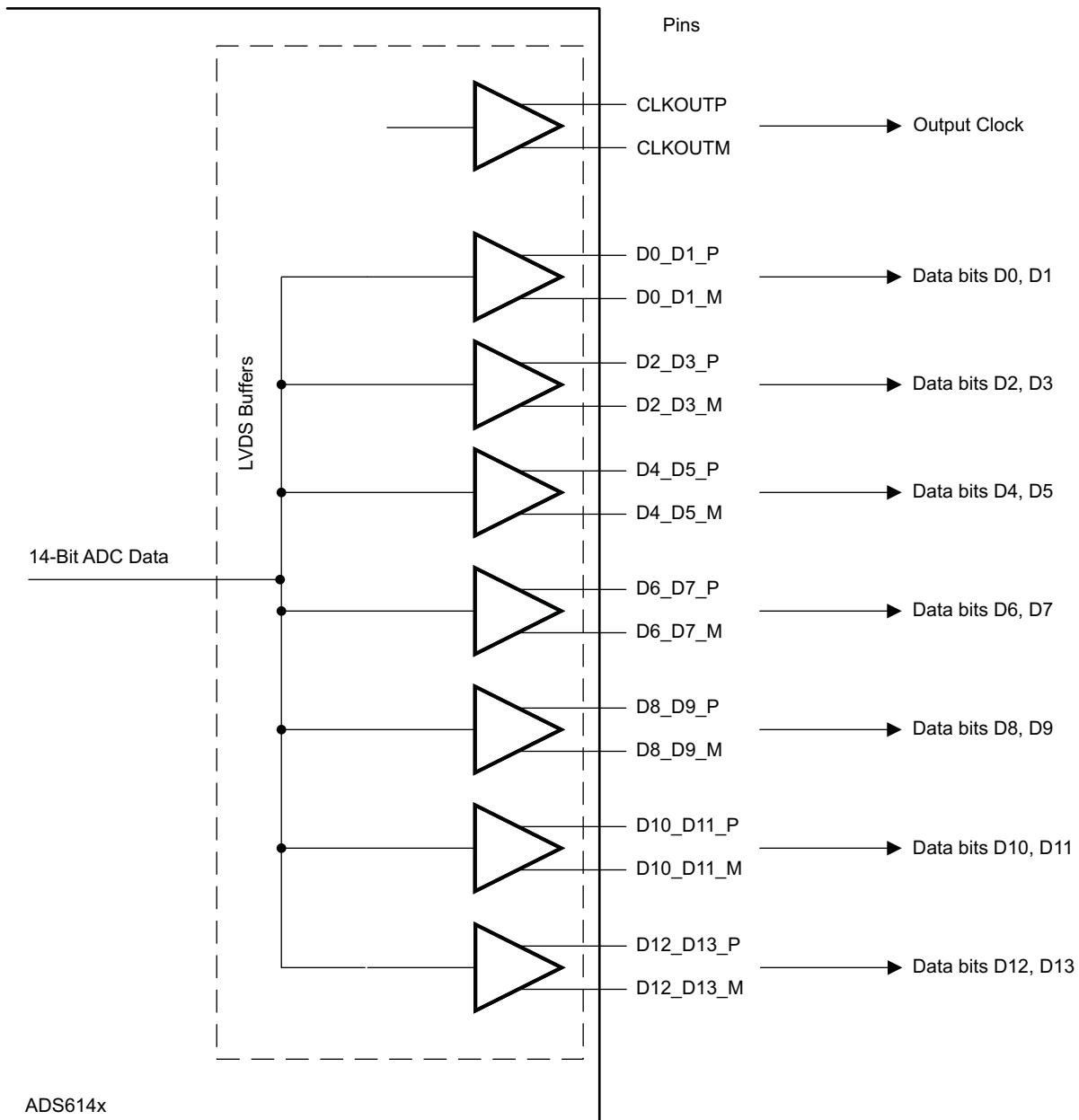
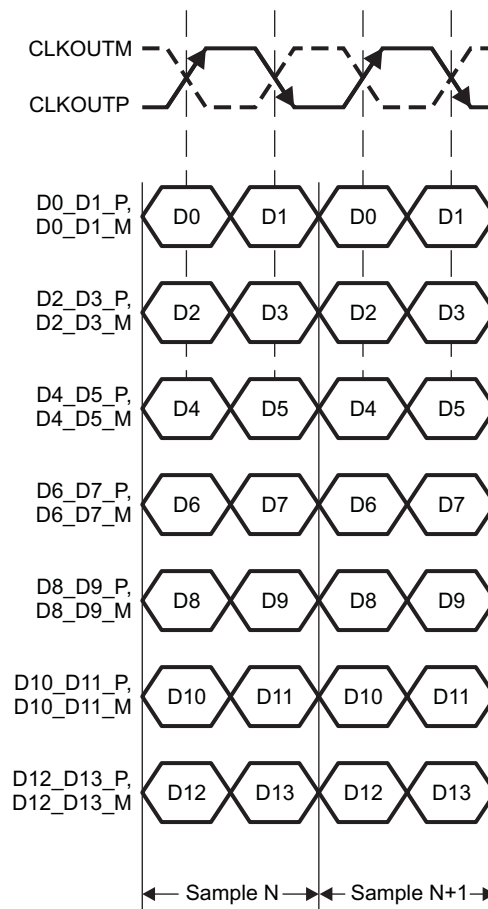


Figure 105. DDR LVDS Outputs

Even data bits D0, D2, D4, D6, D8, D10, and D12 are output at the rising edge of CLKOUTP and the odd data bits D1, D3, D5, D7, D9, D11, and D13 are output at the falling edge of CLKOUTP. Both the rising and falling edges of CLKOUTP must be used to capture all 14 data bits (see [Figure 106](#)).



**Figure 106. DDR LVDS Interface**

### ***LVDS Buffer Internal Termination***

An internal termination option is available (using the serial interface), by which the LVDS buffers are differentially terminated inside the device. The termination resistances available are – 300  $\Omega$ , 185  $\Omega$ , and 150  $\Omega$  (nominal with  $\pm 20\%$  variation). Any combination of these three terminations can be programmed; the effective termination is the parallel combination of the selected resistances. This results in eight effective terminations from open (no termination) to 65  $\Omega$ .

The internal termination helps to absorb any reflections coming from the receiver end, improving the signal integrity. With 100- $\Omega$  internal and 100- $\Omega$  external termination, the voltage swing at the receiver end is halved (compared to no internal termination). The voltage swing can be restored by using the LVDS current double mode. [Figure 107](#) and [Figure 108](#) compare the LVDS eye diagrams without and with internal termination (100  $\Omega$ ). With internal termination, the eye looks clean even with 10-pF load capacitance (from each output pin to ground). The termination is programmed using register bits **<DATA TERM>** and **<CLKOUT TERM>** (see [Table 11](#)).

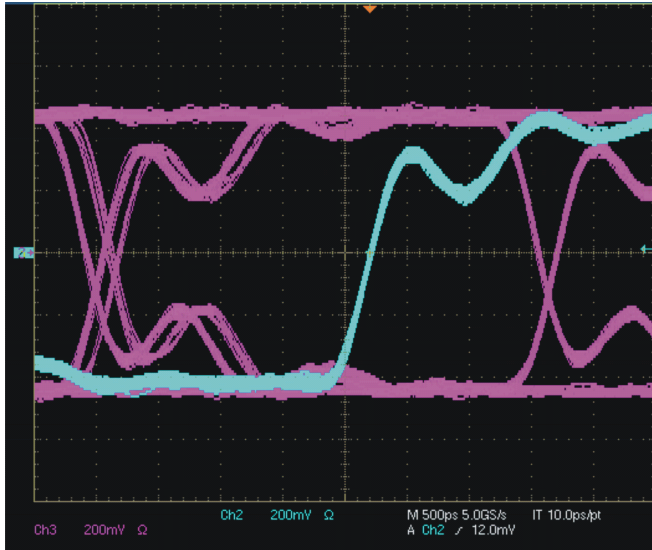


Figure 107. LVDS Eye Diagram - No Internal Termination  
5-pF Load Capacitance  
Blue Trace - Output Clock (CLKOUT)  
Pink Trace - Output Data

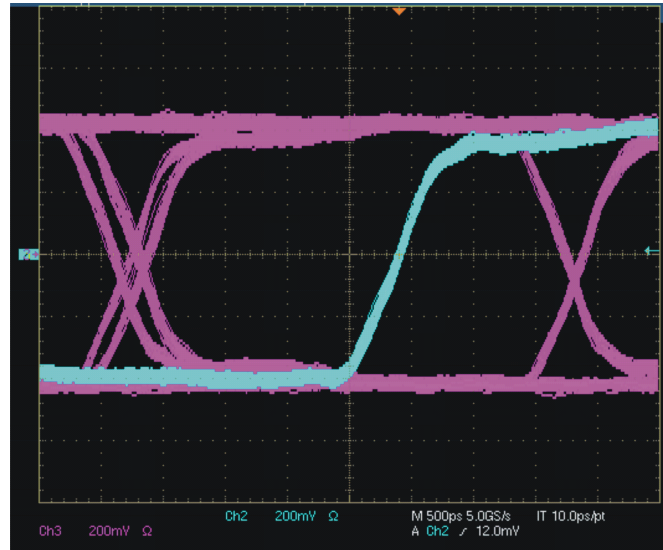


Figure 108. LVDS Eye Diagram with 100-Ω Internal Termination  
10-pF Load Capacitance  
Blue Trace - Output Clock (CLKOUT)  
Pink Trace - Output Data

### Output Data Format

Two output data formats are supported – 2s complement and offset binary. They can be selected using the parallel control pin SEN or the serial interface register bit **<DATA FORMAT>** (see [Table 8](#)).

### Output Timings

The tables below show the timings at lower sampling frequencies.

Table 15. Timing Characteristics at Lower Sampling Frequencies <sup>(1)(2)</sup>

F <sub>s</sub> , MSPS	t <sub>su</sub> DATA SETUP TIME, ns			t <sub>h</sub> DATA HOLD TIME, ns			t <sub>pDI</sub> CLOCK PROPAGATION DELAY, ns		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
<b>CMOS INTERFACE, DRVDD = 2.5 V to 3.3 V</b>									
40	11.3	12.8		10	11.2		5	6.5	7.9
20	23	25		21	23				
10	48	50		46	48				
<b>DDR LVDS INTERFACE, DRVDD = 3.3 V</b>									
40	10.2	10.8		0.7	1.7		4.3	5.8	7.3
20	22	23		0.7	1.7		4.5	6.5	8.5
10	47	48		0.7	1.7		4.5	6.5	8.5

(1) Timing parameters are specified by design and characterization and not tested in production.

(2) Timings are specified with default output buffer drive strength and C<sub>L</sub> = 5 pF.

## BOARD DESIGN CONSIDERATIONS

### Grounding

A single ground plane is sufficient to give good performance, provided the analog, digital, and clock sections of the board are cleanly partitioned. See the EVM User Guide ([SLWU028](#)) for details on layout and grounding.

### Supply Decoupling

As the ADS614X already include internal decoupling, minimal external decoupling can be used without loss in performance. Note that decoupling capacitors can help filter external power supply noise, so the optimum number of capacitors would depend on the actual application. The decoupling capacitors should be placed very close to the converter supply pins.

It is recommended to use separate supplies for the analog and digital supply pins to isolate digital switching noise from sensitive analog circuitry. In case only a single 3.3-V supply is available, it should be routed first to AVDD. It can then be tapped and isolated with a ferrite bead (or inductor) with decoupling capacitor, before being routed to DRVDD.

### Exposed Thermal Pad

It is necessary to solder the exposed pad at the bottom of the package to a ground plane for best thermal performance. For detailed information, see application notes **QFN Layout Guidelines** ([SLOA122](#)) and **QFN/SON PCB Attachment** ([SLUA271](#)).

## DEFINITION OF SPECIFICATIONS

### Analog Bandwidth

The analog input frequency at which the power of the fundamental is reduced by 3 dB with respect to the low frequency value.

### Aperture Delay

The delay in time between the rising edge of the input sampling clock and the actual time at which the sampling occurs.

### Aperture Uncertainty (Jitter)

The sample-to-sample variation in aperture delay.

### Clock Pulse Width/Duty Cycle

The duty cycle of a clock signal is the ratio of the time the clock signal remains at a logic high (clock pulse width) to the period of the clock signal. Duty cycle is typically expressed as a percentage. A perfect differential sine-wave clock results in a 50% duty cycle.

### Maximum Conversion Rate

The maximum sampling rate at which certified operation is given. All parametric testing is performed at this sampling rate unless otherwise noted.

### Minimum Conversion Rate

The minimum sampling rate at which the ADC functions.

### Differential Nonlinearity (DNL)

An ideal ADC exhibits code transitions at analog input values spaced exactly 1 LSB apart. The DNL is the deviation of any single step from this ideal value, measured in units of LSBs.

### Integral Nonlinearity (INL)

The INL is the deviation of the ADC's transfer function from a best fit line determined by a least squares curve fit of that transfer function, measured in units of LSBs.

### Gain Error

The gain error is the deviation of the ADC's actual input full-scale range from its ideal value. The gain error is given as a percentage of the ideal input full-scale range.

### Offset Error

The offset error is the difference, given in number of LSBs, between the ADC's actual average idle channel output code and the ideal average idle channel output code. This quantity is often mapped into mV.

### Temperature Drift

The temperature drift coefficient (with respect to gain error and offset error) specifies the change per degree Celsius of the parameter from  $T_{\text{MIN}}$  to  $T_{\text{MAX}}$ . It is calculated by dividing the maximum deviation of the parameter across the  $T_{\text{MIN}}$  to  $T_{\text{MAX}}$  range by the difference  $T_{\text{MAX}} - T_{\text{MIN}}$ .

### Signal-to-Noise Ratio

SNR is the ratio of the power of the fundamental ( $P_S$ ) to the noise floor power ( $P_N$ ), excluding the power at dc and the first nine harmonics.

$$\text{SNR} = 10\text{Log}_{10} \frac{P_S}{P_N} \quad (4)$$

SNR is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

### Signal-to-Noise and Distortion (SINAD)

SINAD is the ratio of the power of the fundamental ( $P_S$ ) to the power of all the other spectral components including noise ( $P_N$ ) and distortion ( $P_D$ ), but excluding dc.

$$\text{SINAD} = 10\text{Log}_{10} \frac{P_S}{P_N + P_D} \quad (5)$$

SINAD is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

### Effective Number of Bits (ENOB)

The ENOB is a measure of a converter's performance as compared to the theoretical limit based on quantization noise.

$$\text{ENOB} = \frac{\text{SINAD} - 1.76}{6.02} \quad (6)$$

### Total Harmonic Distortion (THD)

THD is the ratio of the power of the fundamental ( $P_S$ ) to the power of the first nine harmonics ( $P_D$ ).

$$\text{THD} = 10\text{Log}_{10} \frac{P_S}{P_D} \quad (7)$$

THD is typically given in units of dBc (dB to carrier).

### Spurious-Free Dynamic Range (SFDR)

The ratio of the power of the fundamental to the highest other spectral component (either spur or harmonic). SFDR is typically given in units of dBc (dB to carrier).

### Two-Tone Intermodulation Distortion

IMD3 is the ratio of the power of the fundamental (at frequencies  $f_1$  and  $f_2$ ) to the power of the worst spectral component at either frequency  $2f_1 - f_2$  or  $2f_2 - f_1$ . IMD3 is either given in units of dBc (dB to carrier) when the absolute power of the fundamental is used as the reference, or dBFS (dB to full scale) when the power of the fundamental is extrapolated to the converter's full-scale range.

### DC Power Supply Rejection Ratio (DC PSRR)

The DC PSRR is the ratio of the change in offset error to a change in analog supply voltage. The DC PSRR is typically given in units of mV/V.

### AC Power Supply Rejection Ratio (AC PSRR)

AC PSRR is the measure of rejection of variations in the supply voltage of the ADC. If  $\Delta V_{SUP}$  is the change in the supply voltage and  $\Delta V_{OUT}$  is the resultant change in the ADC output code (referred to the input), then

$$PSRR = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{SUP}} \quad (\text{Expressed in dBc}) \quad (8)$$

### Common-Mode Rejection Ratio (CMRR)

CMRR is the measure of rejection of variations in the input common-mode voltage of the ADC. If  $\Delta V_{cm}$  is the change in the input common-mode voltage and  $\Delta V_{OUT}$  is the resultant change in the ADC output code (referred to the input), then

$$CMRR = 20\text{Log}^{10} \frac{\Delta V_{OUT}}{\Delta V_{CM}} \quad (\text{Expressed in dBc}) \quad (9)$$

### Voltage Overload Recovery

The number of clock cycles taken to recover to less than 1% error for a 6-dB overload on the analog inputs. A 6-dBFS sine wave at Nyquist frequency is used as the test stimulus.

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## REVISION HISTORY

Changes from Revision A (October 2007) to Revision B	Page
• Added maximum DRVDD current footnote .....	5
• Added SCLK and SEN pin function footnote .....	8
• Changed DDR LVDS output data sequence in <a href="#">Figure 1</a> .....	11
• Changed pin configuration (CMOS mode) information .....	21
• Changed pin configuration (LVDS mode) information .....	23

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**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS6142IRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6142	<a href="#">Samples</a>
ADS6143IRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6143	<a href="#">Samples</a>
ADS6144IRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6144	<a href="#">Samples</a>
ADS6145IRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	AZ6145	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF ADS6142 :**

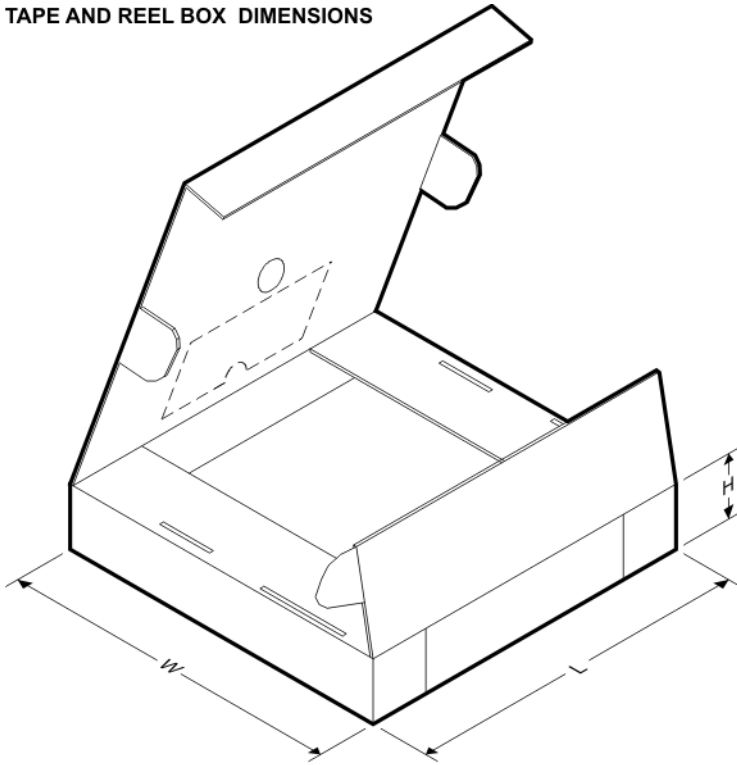
NOTE: Qualified Version Definitions:

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS6142IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS6143IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS6144IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
ADS6145IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS6142IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS6143IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS6144IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
ADS6145IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

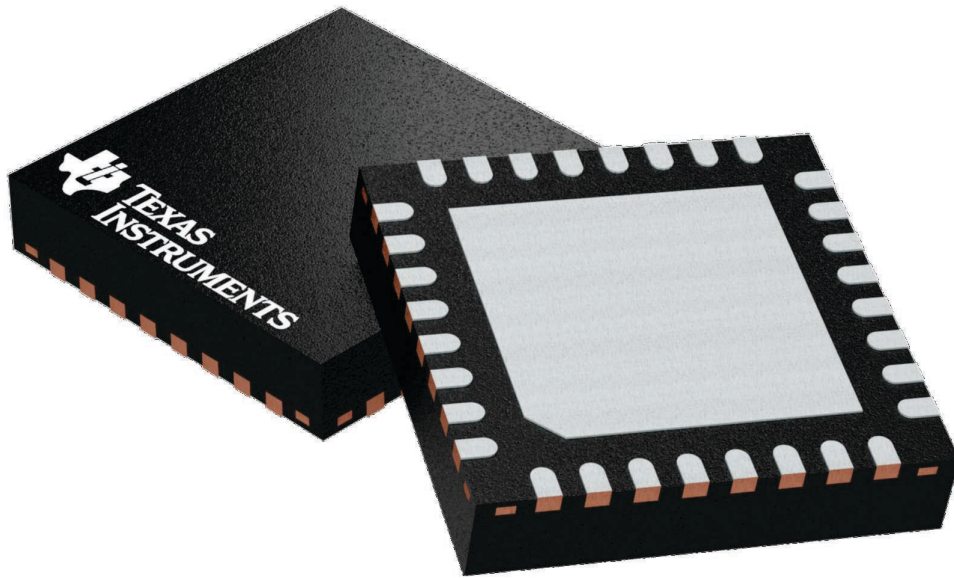
## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

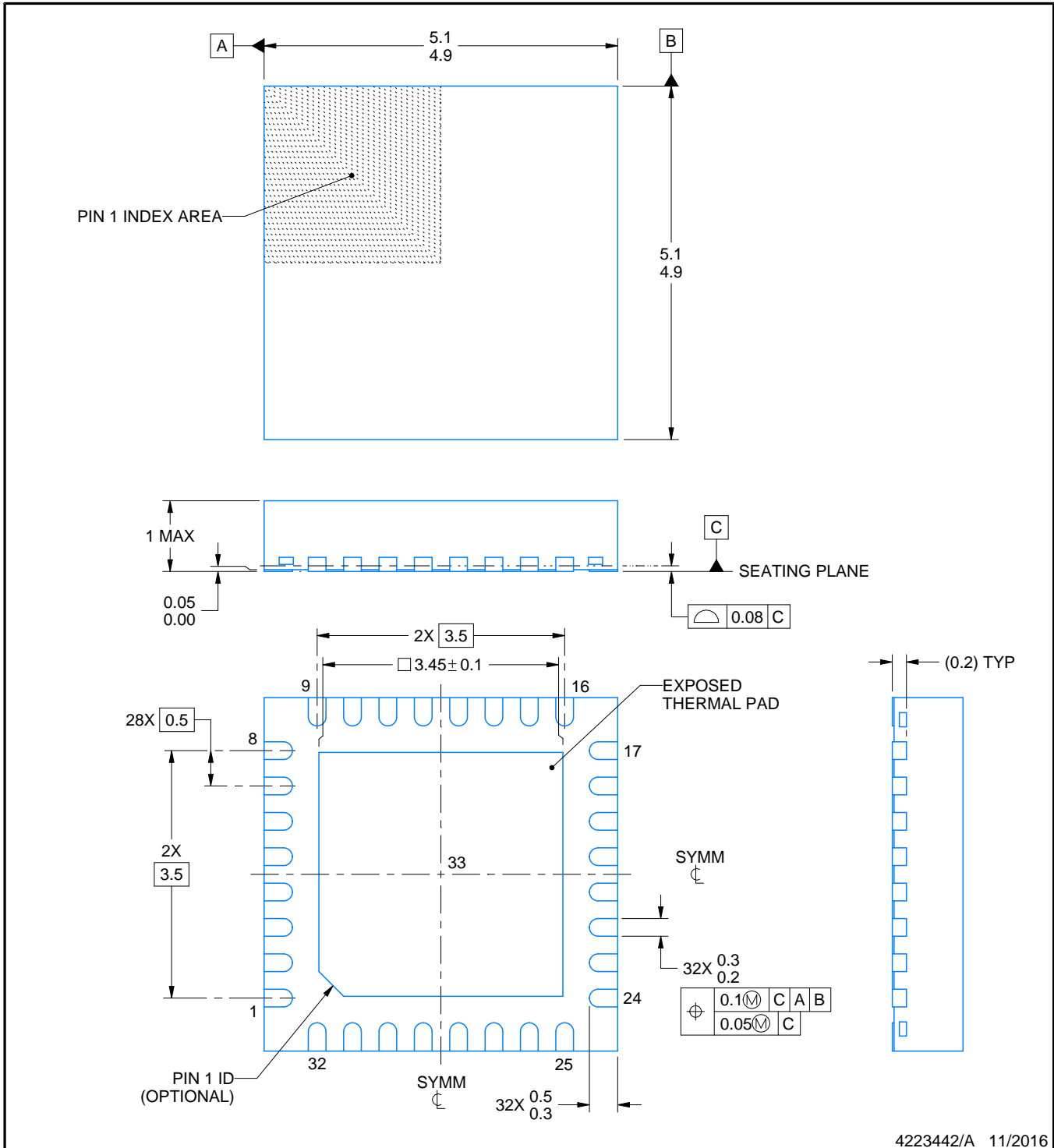
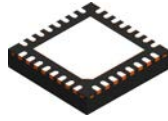
5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

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NOTES:

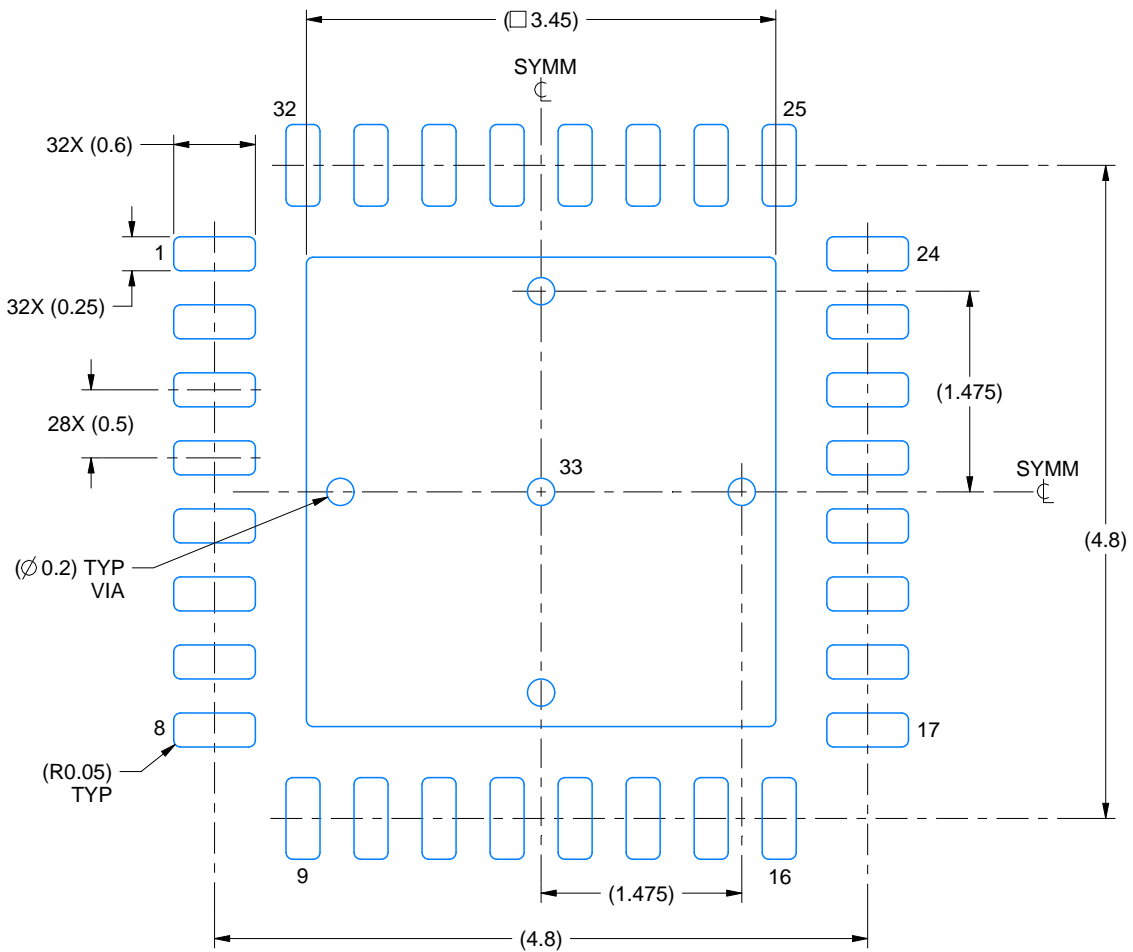
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

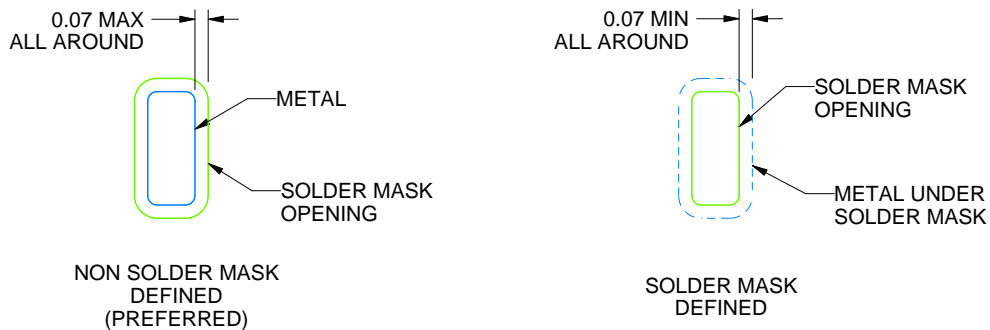
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

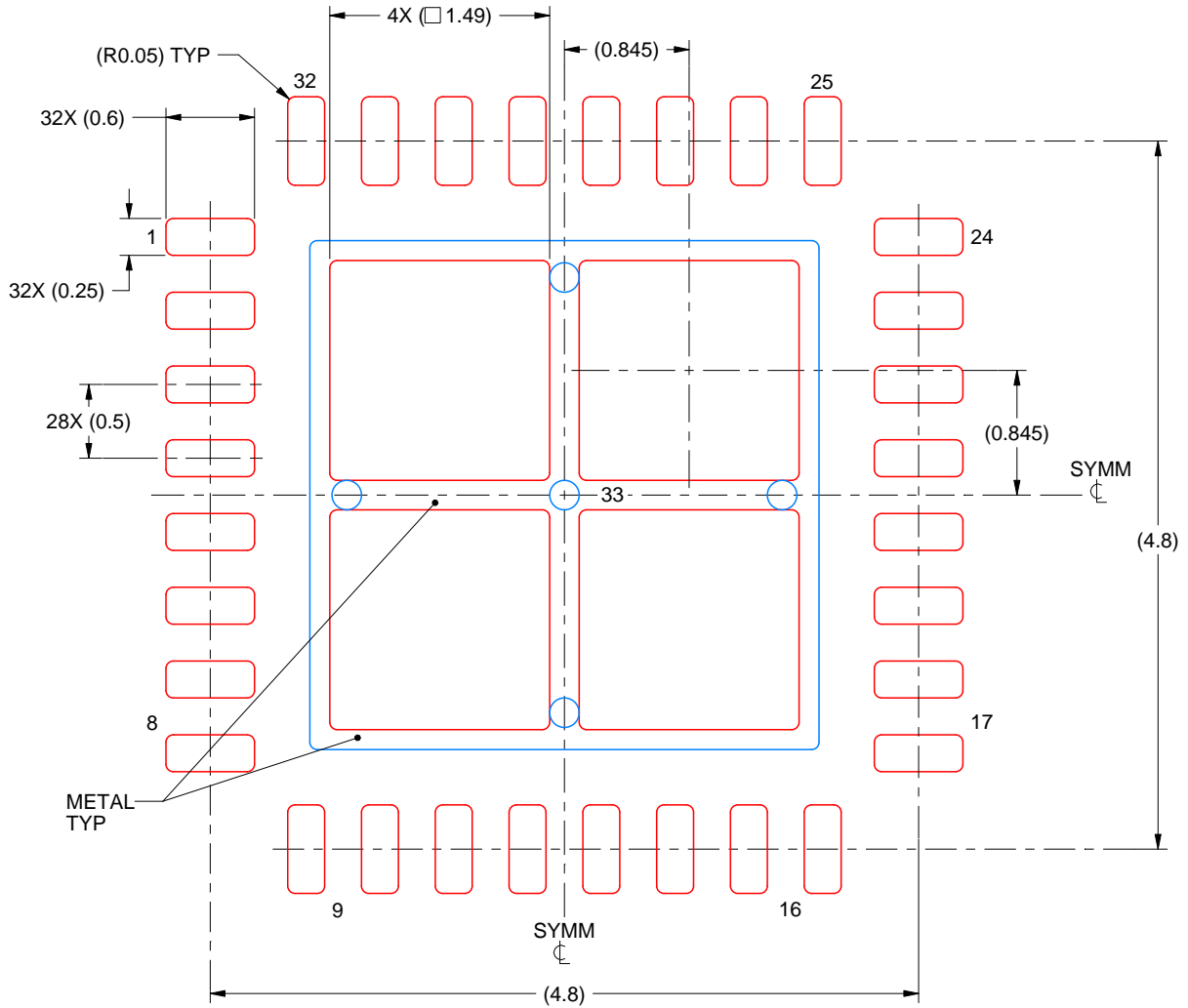
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
 75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
 SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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