



**THE DATASHEET OF
ADRF5040BCPZ**



FEATURES

- Nonreflective 50 Ω design**
- Positive control range: 0 V to 3.3 V**
- Low insertion loss: 0.8 dB at 8.0 GHz**
- High isolation: 34 dB at 8.0 GHz**
- High power handling**
 - 33 dBm through path
 - 27 dBm termination path
- High linearity**
 - 1 dB compression (P1dB): 37 dBm typical
 - Input third-order intercept (IIP3): 58 dBm typical at 8.0 GHz
- ESD rating: 4 kV human body model (HBM)**
- 4 mm \times 4 mm, 24-lead LFCSP package**
- No low frequency spurious**
- RF settling time (0.05 dB margin of final RF_{OUT}): 9 μ s**

APPLICATIONS

- Test instrumentation
- Microwave radios and very small aperture terminals (VSATs)
- Military radios, radars, and electronic counter measures (ECMs)
- Fiber optics and broadband telecommunications

GENERAL DESCRIPTION

The **ADRF5040** is a general-purpose, broadband high isolation, nonreflective single-pole, quad-throw (SP4T) switch in an LFCSP surface-mount package. Covering the 9 kHz to 12.0 GHz range, the switch offers high isolation and low insertion loss. The switch features 34 dB isolation and 0.8 dB insertion loss up to

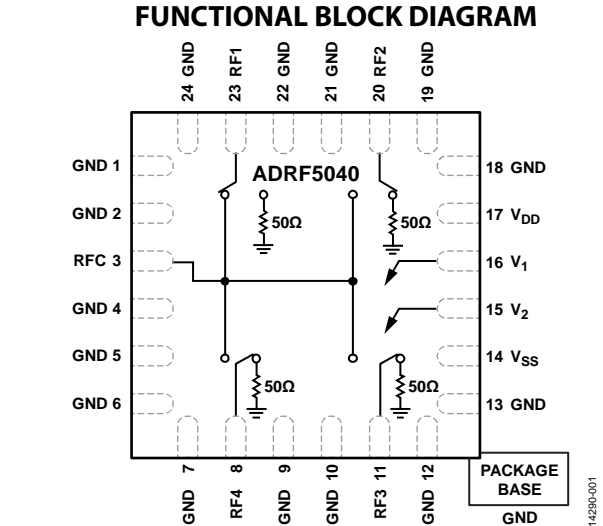


Figure 1.

8.0 GHz, and a 9 μ s settling time of 0.05 dB margin of the final radio frequency output (RF_{OUT}). The switch operates using positive control voltage of 3.3 V and 0 V and requires +3.3 V and -3.3 V supplies. The **ADRF5040** is packaged in a 4 mm \times 4 mm, surface-mount LFCSP package.

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REVISION HISTORY

| | |
|--|----|
| 7/2017—Rev. A to Rev. B | |
| Changes to Figure 2, Figure 3, and Figure 4..... | 5 |
| 2/2017—Rev. 0 to Rev. A | |
| Changes to Ordering Guide | 14 |
| 7/2016—Revision 0: Initial Version | |

SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, V_1 and $V_2 = 0\text{ V}$ or V_{DD} , $T_A = 25^\circ\text{C}$, $50\ \Omega$ system, unless otherwise noted.

Table 1.

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit | |
|---|--|---|-----------------------------|----------|---------------|------------------|
| INSERTION LOSS | 9 kHz to 4.0 GHz | | 0.7 | | dB | |
| | 9 kHz to 8.0 GHz | | 0.8 | | dB | |
| | 9 kHz to 10.0 GHz | | 1.1 | | dB | |
| | 9 kHz to 12.0 GHz | | 2 | | dB | |
| ISOLATION, RFC TO RF1 TO RF4 (WORST CASE) | 9 kHz to 4.0 GHz | | 44 | | dB | |
| | 9 kHz to 8.0 GHz | | 34 | | dB | |
| | 9 kHz to 10.0 GHz | | 29.2 | | dB | |
| | 9 kHz to 12.0 GHz | | 20 | | dB | |
| RETURN LOSS | On State | | 9 kHz to 4.0 GHz | 21 | dB | |
| | | | 9 kHz to 8.0 GHz | 19 | dB | |
| | | | 9 kHz to 10.0 GHz | 13.5 | dB | |
| | | | 9 kHz to 12.0 GHz | 8 | dB | |
| | Off State | | 9 kHz to 4.0 GHz | 25 | dB | |
| | | | 9 kHz to 8.0 GHz | 18.6 | dB | |
| | | | 9 kHz to 10.0 GHz | 15.5 | dB | |
| | | | 9 kHz to 12.0 GHz | 14.5 | dB | |
| RADIO FREQUENCY (RF) SETTling TIME | 50% V_1/V_2 to 0.05 dB margin of final RF_{OUT} 50% V_1/V_2 to 0.1 dB margin of final RF_{OUT} | | 9 | | μs | |
| | | | 7 | | μs | |
| SWITCHING SPEED | 10% to 90% RF_{OUT} 50% V_1/V_2 to 90%/10% RF | | t_{RISE}/t_{FALL} | 1.3 | μs | |
| | | | t_{ON}/t_{OFF} | 3.5 | μs | |
| INPUT POWER | 9 kHz to 12.0 GHz | | 1 dB Compression (P1dB) | 37 | dBm | |
| | | | 0.1 dB Compression (P0.1dB) | 34 | dBm | |
| INPUT THIRD-ORDER INTERCEPT (IIP3) | Two-tone input power = 14 dBm at each tone 1 MHz to 2.0 GHz 1 MHz to 8.0 GHz 1 MHz to 12.0 GHz | | 62 | | dBm | |
| | | | 58 | | dBm | |
| | | | 53 | | dBm | |
| RECOMMENDED OPERATING CONDITIONS | Positive Supply Voltage (V_{DD}) Negative Supply Voltage (V_{SS}) Control Voltage (V_1, V_2) Range | | 3.0 | 3.6 | V | |
| | | | -3.6 | -3.0 | V | |
| | | | 0 | V_{DD} | V | |
| | RF Input Power | $V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $T_A = 85^\circ\text{C}$, frequency = 2 GHz | | | 33 | dBm |
| | | | | | 27 | dBm |
| | Hot Switch Power Level | $V_{DD} = 3.3\text{ V}$, $T_A = 85^\circ\text{C}$, frequency = 2 GHz | | | 27 | dBm |
| | Case Temperature Range (T_{CASE}) | | | -40 | +85 | $^\circ\text{C}$ |

DIGITAL CONTROL VOLTAGE SPECIFICATIONS

$V_{DD} = 3.3 \text{ V} \pm 10\%$, $V_{SS} = -3.3 \text{ V} \pm 10\%$, $T_{CASE} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted.

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Condition/Comments |
|--------------------------------------|----------|-----|-----|----------------|------|--------------------------|
| INPUT CONTROL VOLTAGE (V_1, V_2) | | | | | | <1 μA typical |
| Low | V_{IL} | 0 | | 0.8 | V | |
| High | V_{IH} | 1.4 | | $V_{DD} + 0.3$ | V | |

BIAS AND SUPPLY CURRENT SPECIFICATIONS

$T_{CASE} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, unless otherwise noted.

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit |
|---------------------------|----------|-----|-----|-----|---------------|
| SUPPLY CURRENT | | | | | |
| $V_{DD} = 3.3 \text{ V}$ | I_{DD} | | 20 | 100 | μA |
| $V_{SS} = -3.3 \text{ V}$ | I_{SS} | | 20 | 100 | μA |

ABSOLUTE MAXIMUM RATINGS

Table 4.

| Parameter | Rating |
|--|----------------------------|
| Positive Supply Voltage (V_{DD}) Range | -0.3 V to +3.7 V |
| Negative Supply Voltage (V_{SS}) Range | -3.7 V to +0.3 V |
| Control Voltage (V_1, V_2) Range | -0.3 V to $V_{DD} + 0.3$ V |
| RF Input Power ¹ ($V_{DD}, V_1, V_2 = 3.3$ V, $V_{SS} = -3.3$ V, $T_A = 85^\circ\text{C}$, Frequency = 2 GHz) | |
| Through Path | 34 dBm |
| Termination Path | 28 dBm |
| Hot Switch Power Level ($V_{DD} = 3.3$ V, $T_A = 85^\circ\text{C}$, Frequency = 2 GHz) | 30 dBm |
| Storage Temperature Range | -65°C to +150°C |
| Channel Temperature | 135°C |
| Thermal Resistance (Channel to Package Bottom) | |
| Through Path | 83°C/W |
| Terminated Path | 100°C/W |
| MSL Rating | MSL3 |
| ESD Sensitivity | |
| Human Body Model (HBM) | 4 kV (Class 3) |
| Charged Device Model (CDM) | 1.25 kV |

¹ For the recommended operating conditions, see Table 1.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

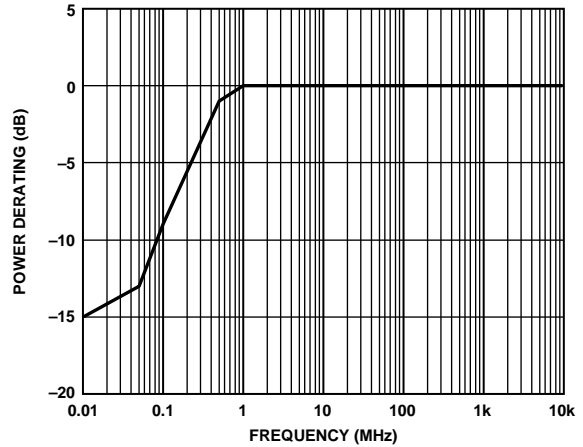


Figure 3. Power Derating for Terminated Path

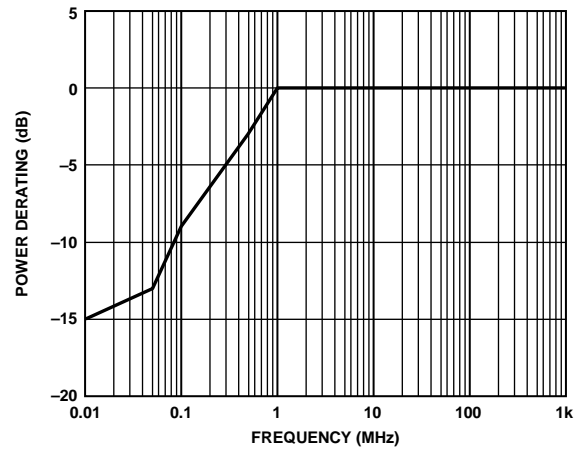


Figure 4. Power Derating for Hot Switching Power

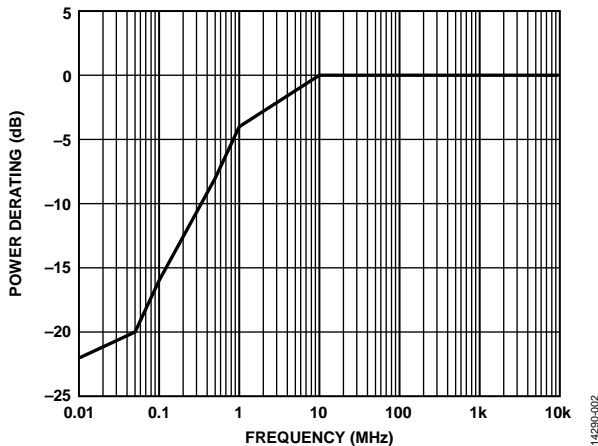


Figure 2. Power Derating for Through Path

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

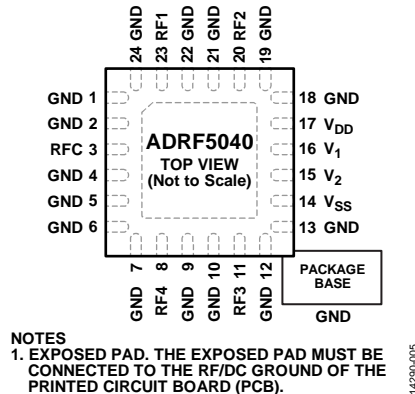


Figure 5. Pin Configuration

Table 5. Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---|-----------------|--|
| 1, 2, 4 to 7, 9, 10, 12, 13, 18, 19, 21, 22, 24 | GND | Ground. The package bottom has an exposed metal pad that must connect to the printed circuit board (PCB) RF/dc ground. See Figure 6 for the GND interface schematic. |
| 3 | RFC | RF Common Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. |
| 8 | RF4 | RF4 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. |
| 11 | RF3 | RF3 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. |
| 14 | V _{SS} | Negative Supply Voltage Pin. |
| 15 | V ₂ | Control Input Pin 2. See Table 2 and Table 6. |
| 16 | V ₁ | Control Input Pin 1. See Table 2 and Table 6. |
| 17 | V _{DD} | Positive Supply Voltage. |
| 20 | RF2 | RF2 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. |
| 23 | RF1 | RF1 Port. This pin is dc-coupled and matched to 50 Ω. A dc blocking capacitor is required if the RF line potential is not equal to 0 V dc. |
| | EPAD | Exposed Pad. The exposed pad must be connected to the RF/dc ground of the PCB. |

Table 6. Truth Table

| Digital Control Inputs | | Signal Path State |
|------------------------|----------------|-------------------|
| V ₁ | V ₂ | |
| Low | Low | RFC to RF1 |
| High | Low | RFC to RF2 |
| Low | High | RFC to RF3 |
| High | High | RFC to RF4 |

INTERFACE SCHEMATICS



Figure 6. GND Interface Schematic

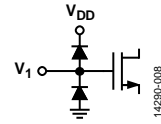


Figure 8. V1 Interface Schematic

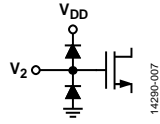


Figure 7. V2 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $T_{CASE} = 25^\circ\text{C}$, unless otherwise specified.

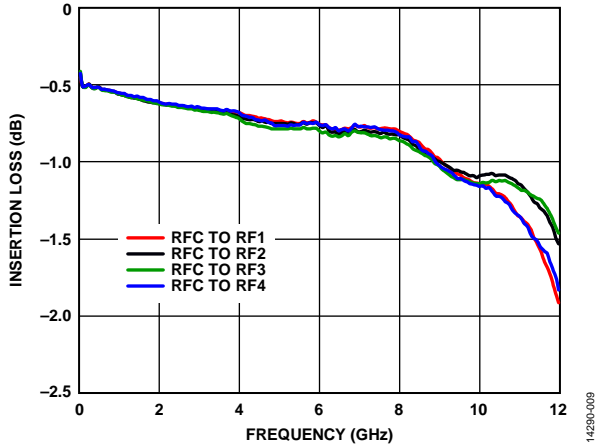


Figure 9. Insertion Loss vs. Frequency

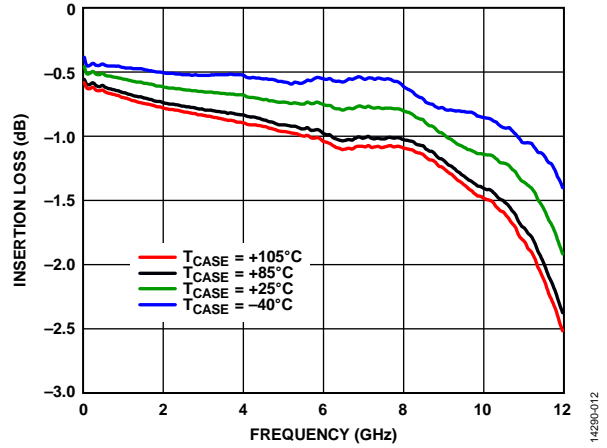


Figure 12. Insertion Loss vs. Frequency, RFC to RF1 On or RFC to RF4 On

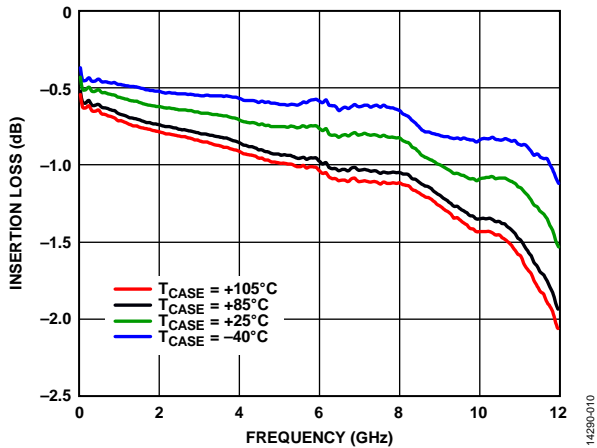


Figure 10. Insertion Loss vs. Frequency, RFC to RF2 On or RFC to RF3 On

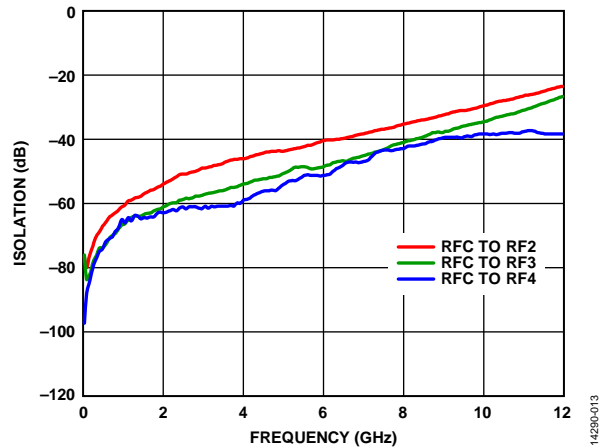


Figure 13. Isolation vs. Frequency, RFC to RF1 On

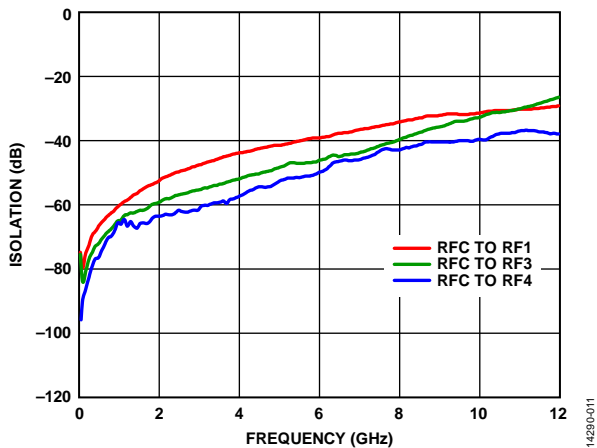


Figure 11. Isolation vs. Frequency, RFC to RF2 On

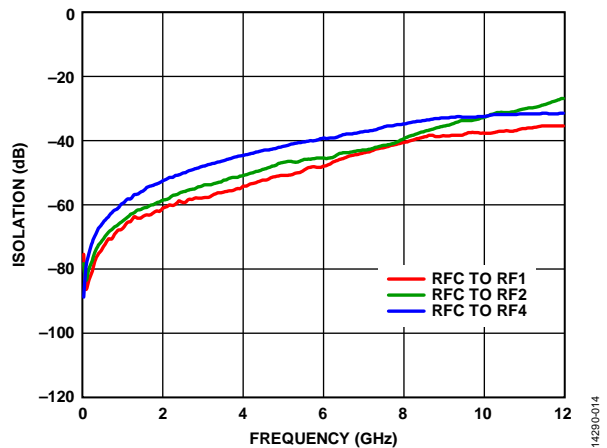


Figure 14. Isolation vs. Frequency, RFC to RF3 On

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $T_{CASE} = 25^\circ\text{C}$, unless otherwise specified.

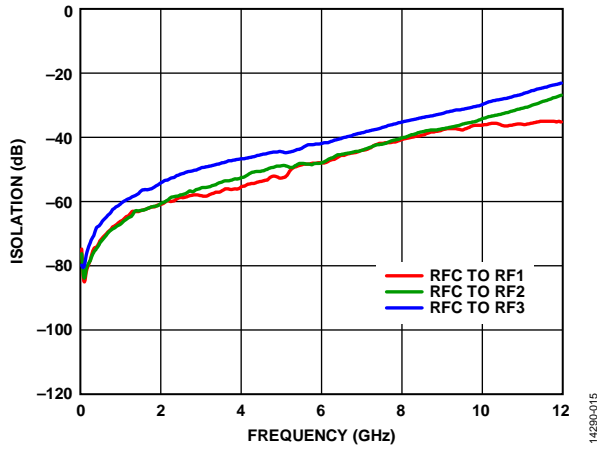


Figure 15. Isolation vs. Frequency, RFC to RF4 On

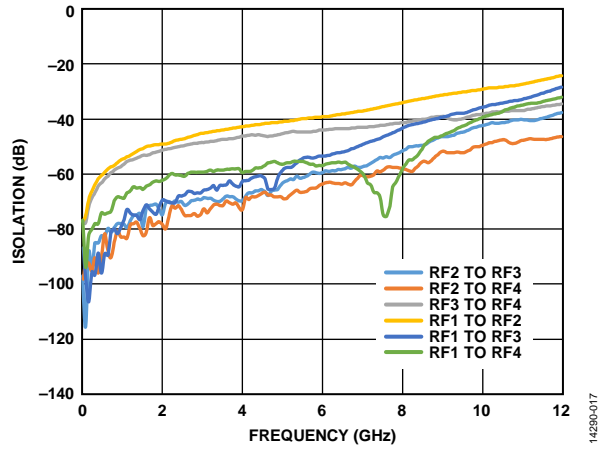


Figure 17. Channel to Channel Isolation vs. Frequency, RFC to RF1 On

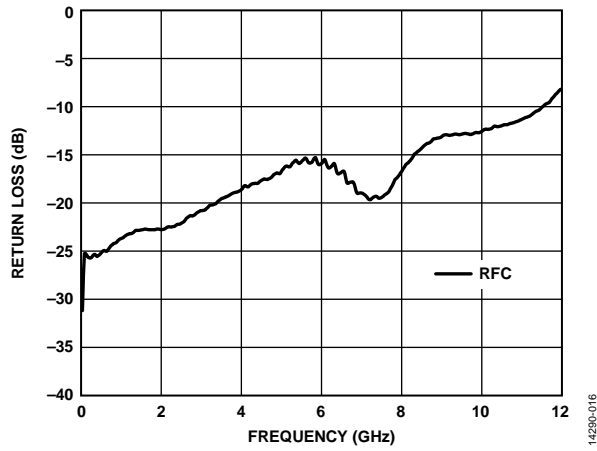


Figure 16. Return Loss vs. Frequency, RFC to RF4 On

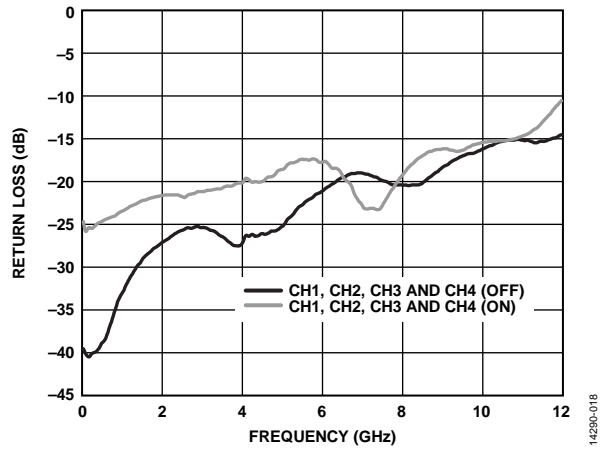


Figure 18. Return Loss vs. Frequency, RFC to RF4 On

INPUT POWER COMPRESSION AND INPUT THIRD-ORDER INTERCEPT

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$, $T_{CASE} = 25^\circ\text{C}$, unless otherwise specified.

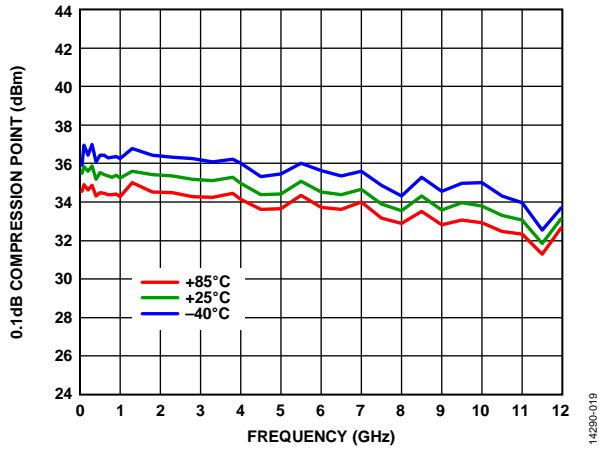


Figure 19. 0.1 dB Compression Point vs. Frequency over Temperature, $V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$

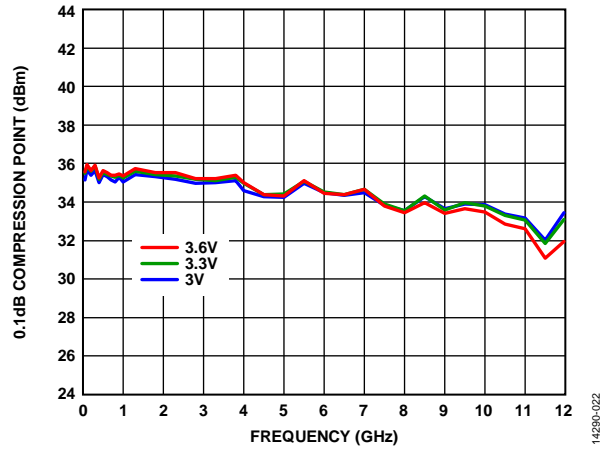


Figure 22. 0.1 dB Compression Point vs. Frequency over Voltage, $T_{CASE} = 25^\circ\text{C}$

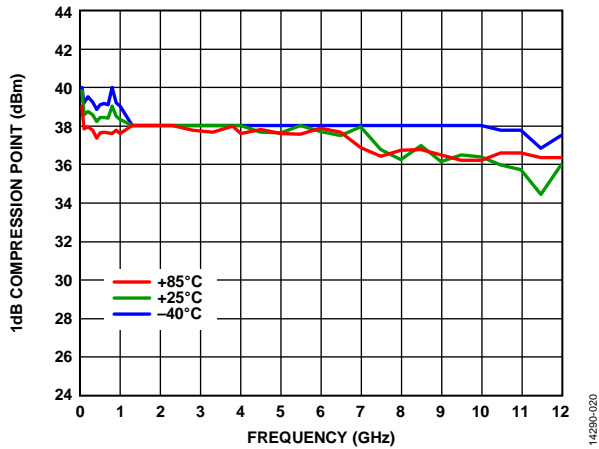


Figure 20. 1 dB Compression Point vs. Frequency over Temperature, $V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$

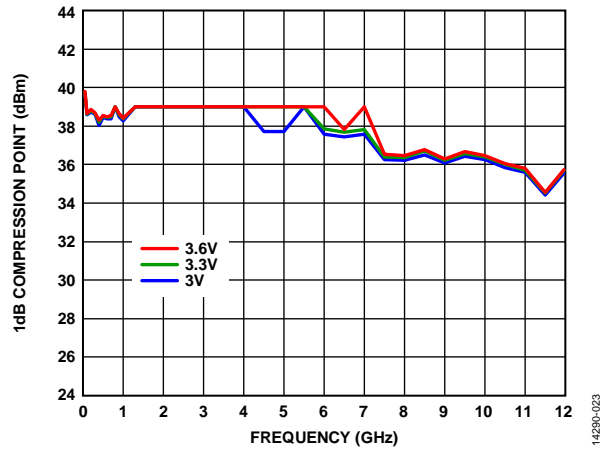


Figure 23. 1 dB Compression Point vs. Frequency over Voltage, $T_{CASE} = 25^\circ\text{C}$

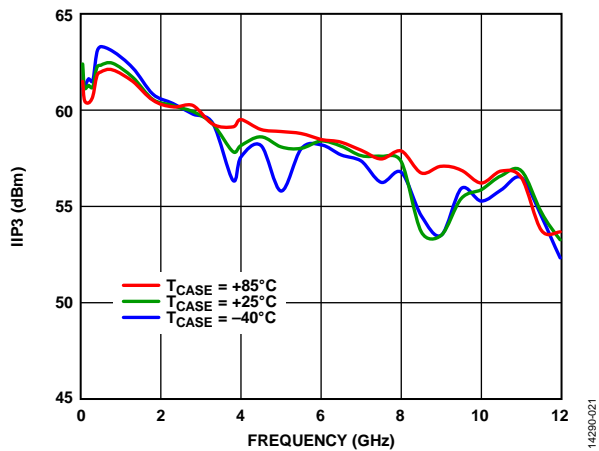


Figure 21. Input Third-Order Intercept (IIP3) vs. Frequency over Temperature, $V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$

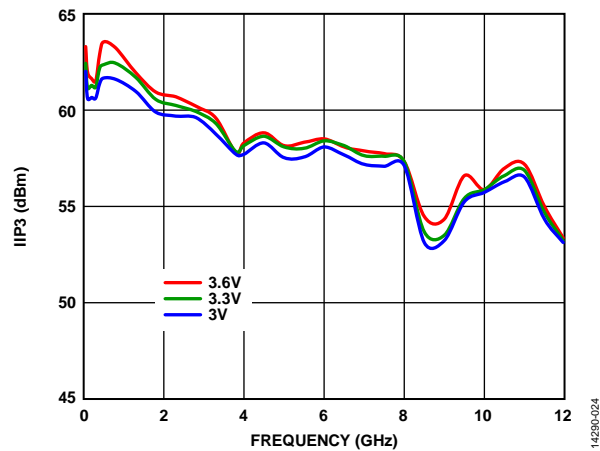


Figure 24. Input Third-Order Intercept (IIP3) vs. Frequency over Voltage, $T_{CASE} = 25^\circ\text{C}$

INPUT POWER COMPRESSION AND INPUT THIRD-ORDER INTERCEPT, 10 kHz TO 1 GHz

$V_{DD} = 3.3\text{ V}$, $V_{SS} = -3.3\text{ V}$ at $T_{CASE} = 25^{\circ}\text{C}$.

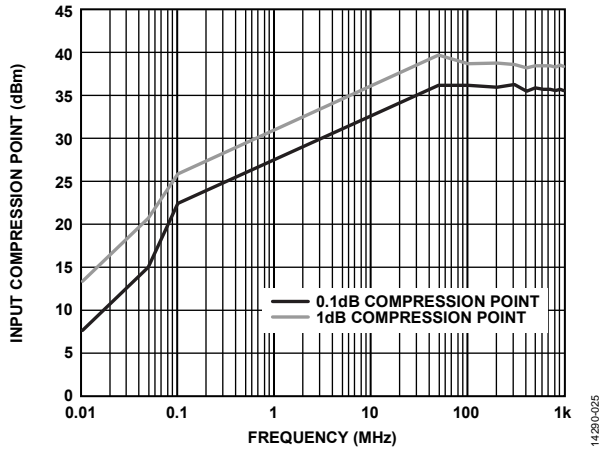


Figure 25. Input Compression Point vs. Frequency

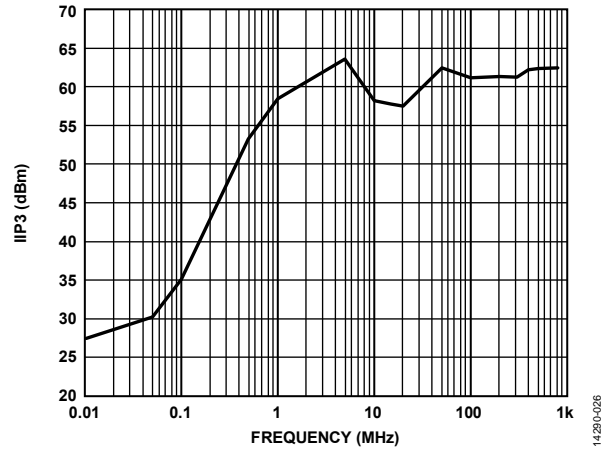


Figure 26. Input Third-Order Intercept (IIP3) vs. Frequency

THEORY OF OPERATION

The [ADRF5040](#) requires a positive supply voltage applied to the V_{DD} pin and a negative voltage supply applied to the V_{SS} pin. Bypassing capacitors are recommended on the supply lines to minimize RF coupling.

The [ADRF5040](#) is controlled via two digital control voltages applied to the V_1 pin and the V_2 pin. A small value bypassing capacitor is recommended on these digital signal lines to improve the RF signal isolation.

The [ADRF5040](#) is internally matched to $50\ \Omega$ at the RF input port (RFC) and the RF output ports (RF1, RF2, RF3, and RF4); therefore, no external matching components are required. The

RF1 through RF4 pins are dc-coupled, and dc blocking capacitors are required on the RF paths. The design is bidirectional; the input and outputs are interchangeable.

The [ADRF5040](#) does not need any special power-up sequencing, and the relative order to power up the V_{DD} and V_{SS} supplies is not important. The V_1 and V_2 control signals can be applied only after V_{DD} is powered up; this sequence avoids forward biasing and causing damage to the internal ESD protection circuits. Turn on the RF signal after the device supply settles to a steady state.

APPLICATIONS INFORMATION

EVALUATION BOARD

The [ADRF5040-EVALZ](#) evaluation board shown in Figure 27 is designed using proper RF circuit design techniques. Signal lines at the RF port have 50 Ω impedance, and the package ground

leads and backside ground slug must be connected directly to the ground plane. The evaluation board is available from Analog Devices, Inc. upon request.

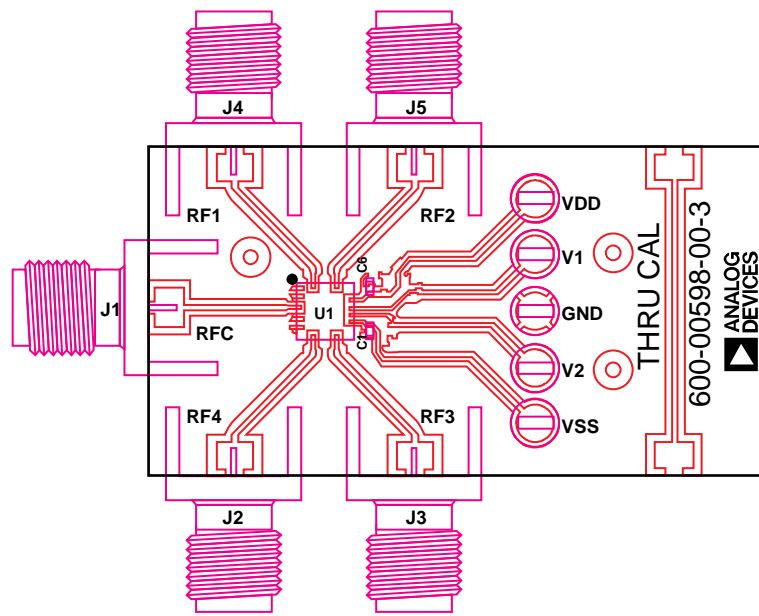


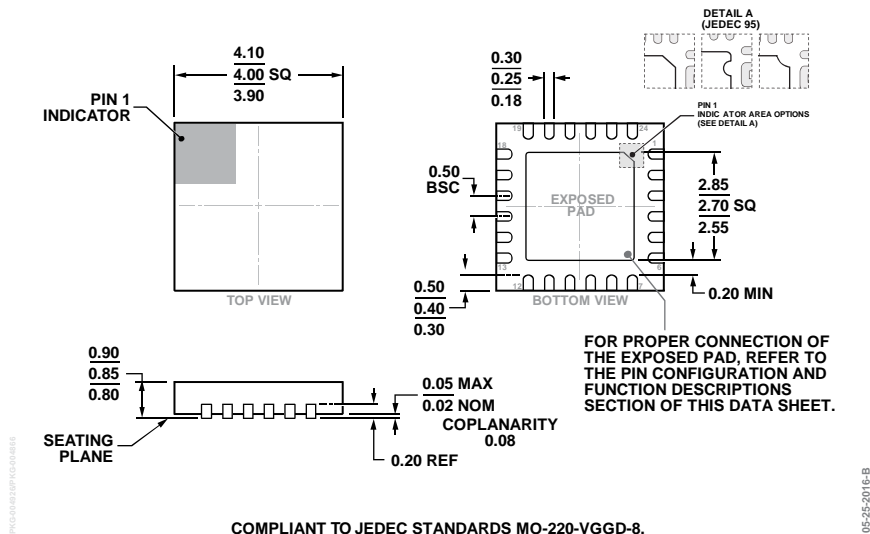
Figure 27. Evaluation PCB

14296-027

Table 7. Bill of Materials for the [ADRF5040-EVALZ](#) Evaluation Board

| Item | Description |
|------------|---|
| J1 to J5 | PC mount SMA RF connectors |
| TP1 to TP5 | Through hole mount test points |
| C1, C6 | 100 pF capacitors, 0402 package |
| U1 | ADRF5040 SP4T switch |
| PCB | 600-00598-00-3 evaluation PCB, Rogers 4350 circuit board material |

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8.
 Figure 28. 24-Lead Lead Frame Chip Scale Package [LFCSP]
 4 mm × 4 mm Body and 0.85 mm Package Height
 (CP-24-16)
 Dimensions shown in millimeters

ORDERING GUIDE

| Model ¹ | Temperature Range | MSL Rating ² | Package Description | Package Option | Branding ³ |
|--------------------|-------------------|-------------------------|---|----------------|------------------------|
| ADRF5040BCPZ | -40°C to +85°C | MSL3 | 24-Lead Lead Frame Chip Scale Package [LFCSP] | CP-24-16 | ADRF 5040 #XXXXX |
| ADRF5040BCPZ-R7 | -40°C to +85°C | MSL3 | 24-Lead Lead Frame Chip Scale Package [LFCSP] | CP-24-16 | ADRF 5040 #XXXXX |
| ADRF5040-EVALZ | | | Evaluation Board | | |

¹ These models are RoHS Compliant Parts.
² See the Absolute Maximum Ratings section.
³ XXXXX is the 5-digit lot number.

Looking for pricing, stock, or lifecycle information?

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