



THE DATASHEET OF ADM7001ACT1



ADM7001/X

Single Ethernet 10/100M PHY

Communications



N e v e r s t o p t h i n k i n g .

Edition 2005-11-25

**Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
81669 München, Germany**

**© Infineon Technologies AG 2005.
All Rights Reserved.**

Attention please!

The information herein is given to describe certain components and shall not be considered as a guarantee of characteristics.

Terms of delivery and rights to technical change reserved.

We hereby disclaim any and all warranties, including but not limited to warranties of non-infringement, regarding circuits, descriptions and charts stated herein.

Information

For further information on technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies Office (www.infineon.com).

Warnings

Due to technical requirements components may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies Office.

Infineon Technologies Components may only be used in life-support devices or systems with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system, or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body, or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

Single Ethernet 10/100M PHY

Revision History: 2005-11-25, Rev. 1.07

Previous Version:

Page/Date	Subjects (major changes since last revision)
2003-03-05	Rev. 1.0: First release of ADM7001
2003-04-08	Rev. 1.01: Register Modifications and Pin updates
2003-07-24	Rev. 1.02: The following sections were updated: 1.2, 1.3, 2.1, 2.2.1, 2.2.5, 2.2.7, 2.2.8, 2.2.8, 4.1, 4.2.3-4, 4.2.11-12, 4.3.4, 4.3.9, 4.3.11, 4.3.12, & 4.3.16
2003-07-30	Rev. 1.03: Updated section 6.2
2003-09-15	Rev. 1.04: Updated Section 2.2.5, 2.2.8, & 4.2.11
2004-02-19	Rev. 1.05: Updated table 5.3
2004-04-16	Rev. 1.06: Removed TQFP packaging
2005-09-12	Rev. 1.07 when changed to the new Infineon format
2005-11-25	Minor change. Included Green package information

Trademarks

ABM[®], ACE[®], AOP[®], ARCOFI[®], ASM[®], ASP[®], DigiTape[®], DuSLIC[®], EPIC[®], ELIC[®], FALC[®], GEMINAX[®], IDEC[®], INCA[®], IOM[®], IPAT[®]-2, ISAC[®], ITAC[®], IWE[®], IWORX[®], MUSAC[®], MuSLIC[®], OCTAT[®], OptiPort[®], POTSWIRE[®], QUAT[®], QuadFALC[®], SCOUT[®], SICAT[®], SICOFI[®], SIDEC[®], SLICOFI[®], SMINT[®], SOCRATES[®], VINETIC[®], 10BaseV[®], 10BaseVX[®] are registered trademarks of Infineon Technologies AG. 10BaseS[™], EasyPort[™], VDSLite[™] are trademarks of Infineon Technologies AG. Microsoft[®] is a registered trademark of Microsoft Corporation, Linux[®] of Linus Torvalds, Visio[®] of Visio Corporation, and FrameMaker[®] of Adobe Systems Incorporated.

Table of Contents

	Table of Contents	4
	List of Figures	6
	List of Tables	7
1	Product Overview	8
1.1	Overview	8
1.1.1	Package Information	8
1.2	Features	8
1.3	Block Diagram	10
2	Interface Description	11
2.1	Pin Diagram	11
2.2	Pin Description	11
2.2.1	Twisted Pair Interface, 5 Pins	13
2.2.2	Digital Ground/Power, 7 Pins	14
2.2.3	Ground and Power, 5 Pins	15
2.2.4	Clock Input, 2 Pins	16
2.2.5	MII/RMII/GPSI Interface, 16 pins	16
2.2.6	Reset Pin	22
2.2.7	Clock Signals, 6 Pins	22
2.2.8	LED Interface, 4 Pins	24
2.2.9	Regulator Control	25
3	Function Description	26
3.1	10/100M PHY Block	26
3.1.1	100Base-X Module	26
3.1.2	100Base-TX Receiver	26
3.1.3	100Base-TX Transmitter	30
3.1.4	100Base-FX Receiver	30
3.1.5	100Base-FX Transmitter	31
3.1.6	10Base-T Module	31
3.1.7	Operation Modes	31
3.1.8	Manchester Encoder/Decoder	31
3.1.9	Transmit Driver and Receiver	31
3.1.10	Smart Squelch	31
3.1.11	Carrier Sense	32
3.1.12	Collision Detection	32
3.1.13	Jabber Function	33
3.1.14	Link Test Function	33
3.1.15	Automatic Link Polarity Detection	33
3.1.16	Clock Synthesizer	33
3.1.17	Auto Negotiation	33
3.1.18	Auto Negotiation and Speed Configuration	34
3.2	MAC Interface	34
3.2.1	Reduced Media Independent Interface (RMII)	34
3.2.2	Receive Path for 100M	35
3.2.3	Receive Path for 10M	36
3.2.4	Transmit Path for 100M	36
3.2.5	Transmit Path for 10M	38
3.2.6	Media Independent Interface (MII)	38

3.2.7	Receive Path for MII	39
3.2.8	Transmit Path for MII	41
3.2.9	General Purpose Serial Interface (GPSI)	41
3.2.10	Receive Path for GPSI	42
3.2.11	Transmit Path for GPSI	42
3.3	LED Display	43
3.4	Management Register Access	44
3.4.1	Preamble Suppression	44
3.4.2	Reset Operation	44
3.5	Power Management	45
3.6	Voltage Regulator	46
4	Registers Description	48
4.1	Register Description	49
5	Electrical Characteristics	74
5.1	DC Characterization	74
5.1.1	Absolute Maximum Rating	74
5.1.2	Recommended Operating Conditions	74
5.1.2.1	DC Characteristics for 2.5 V Operation	74
5.2	AC Characteristics	75
5.2.1	XI/OSCI (Crystal/Oscillator) Timing (In MII Mode)	75
5.3	RMII Timing	76
5.3.1	REFCLK Input Timing (XI in RMII Mode)	76
5.3.2	REFCLK Output Timing (CLKO50 in RMII Mode)	77
5.3.3	RMII Transmit Timing	77
5.3.4	RMII Receive Timing	78
5.4	MII Timing	79
5.4.1	RXCLK Clock Timing	79
5.4.2	MII Receive Timing	81
5.4.3	TXCLK Output Timing	82
5.4.4	MII Transmit Timing	82
5.5	GPSI Timing	83
5.5.1	GPSI Receive Timing	83
5.5.2	GPSI Transmit Timing	84
5.6	Serial Management Interface (MDC/MDIO) Timing	85
5.7	Power On Configuration Timing	86
6	Packaging	87

List of Figures

Figure 1	ADM7001/X Block Diagram	10
Figure 2	Pin Diagram	11
Figure 3	100Base-X Block Diagram and Data Path	27
Figure 4	10Base-T Block Diagram and Data Path	32
Figure 5	RMII Signal Diagram	35
Figure 6	RMII Reception Without Error	35
Figure 7	RMII Reception with False Carrier (100M Only)	36
Figure 8	RMII Reception with Symbol Error	36
Figure 9	10M RMII Receive Diagram	36
Figure 10	100M RMII Transmit Diagram	37
Figure 11	10M RMII Transmit Diagram	38
Figure 12	MII Signal Diagram	39
Figure 13	MII Receive Without Error	39
Figure 14	MII Receive With False Carrier	40
Figure 15	MII Receive With Symbol Error(100M Only)	40
Figure 16	MII Transmission	41
Figure 17	MII Transmit with Collision (Half Duplex Only)	41
Figure 18	GPSI Signal Diagram	42
Figure 19	GPSI Receive Diagram	42
Figure 20	GPSI Transmit Diagram	43
Figure 21	SMII Read Operation	44
Figure 22	SMII Write Operation	45
Figure 23	Medium Detect Power Management Flow Chart	46
Figure 24	Power and Ground Filtering	47
Figure 25	Crystal/Oscillator Timing	75
Figure 26	REFCLK Input Timing	76
Figure 27	REFCLK Output Timing	77
Figure 28	RMII Transmit Timing	78
Figure 29	RMII Receive Timing	78
Figure 30	RXCLK Output Timing	79
Figure 31	MII Receive Timing	81
Figure 32	TXCLK Output Timing	82
Figure 33	MII Transmit Timing	83
Figure 34	GPSI Receive Timing	84
Figure 35	GPSI Transmit Timing	84
Figure 36	Serial Management Interface (MDC/MDIO) Timing	85
Figure 37	Power On Configuration Timing	86
Figure 38	ADM7001/X,Low Profile Quad Flat Package (LQFP)	87

List of Tables

Table 1	Abbreviations for Pin Type	12
Table 2	Abbreviations for Buffer Type	12
Table 3	Twisted Pair Interface, 5 Pins	13
Table 4	Digital Ground/Power, 7 Pins	14
Table 5	Ground and Power, 5 Pins	15
Table 6	Clock Input, 2 Pins	16
Table 7	MII/RMII/GPSI Interface, 16 pins	16
Table 8	Reset Pin	22
Table 9	Clock Signals, 6 pins	22
Table 10	LED Interface, 4 Pins	24
Table 11	Regulator Control	25
Table 12	Look-up Table for Translating 5B Symbols into 4B Nibbles	28
Table 13	Channel Configuration	38
Table 14	Speed LED Display	43
Table 15	Duplex LED Display	43
Table 16	Activity/Link LED Display	43
Table 17	Cable Distance LED Display	44
Table 18	Registers Address Space	48
Table 19	Registers Overview	48
Table 20	Registers Access Types	48
Table 21	Registers Clock Domains	49
Table 22	Reserved Registers	59
Table 23	Absolute Maximum Rating	74
Table 24	Recommended Operating Conditions	74
Table 25	DC Characteristics for 2.5 V Operation	74
Table 26	Crystal/Oscillator Timing	75
Table 27	REFCLK Input Timing	76
Table 28	REFCLK Output Timing	77
Table 29	RMII Transmit Timing	78
Table 30	RMII Receive Timing	79
Table 31	REFCLK Input Timing	80
Table 32	MII Receive Timing	81
Table 33	TXCLK Output Timing	82
Table 34	MII Transmit Timing	83
Table 35	GPSI Receive Timing	84
Table 36	GPSI Transmit Timing	85
Table 37	Serial Management Interface (MDC/MDIO) Timing	85
Table 38	Power On Configuration Timing	86
Table 39	Dimensions for 100 Pin LQFP Package	88

1 Product Overview

Features and Block Diagram.

1.1 Overview

The ADM7001/X is a single chip one port 10/100M PHY, which is designed for today's low cost and low power dual speed application. The ADM7001X is the environmentally friendly "green" package version.

It supports auto sensing 10/100 Mbps ports with on-chip clock recovery and base line wander correction including integrated MLT-3 functionality for 100 Mbps operation, and also supports Manchester Code Converter with on chip clock recovery circuitry for 10 Mbps functionality. Meanwhile, it provides Medium Independent Interface (MII), Reduced Medium Independent Interface (RMII) and General Purpose Serial Interface (GPSI), three different interfaces in different applications.

For today's IA (Information Application), ADM7001/X supports "Auto Cross Over Detection" function to eliminate the technical barrier between networking and end user. With the aid of this auto cross over detection function, Plug-n-Play feature can be easily applied to IA relative products.

The major design target for ADM7001/X is to reduce the power consumption and system radiation for the whole system. With the aid of this low power consumption and low radiation chip, the fan and on-system power supply can be removed to save the total manufacture cost and make SOHO application achievable.

1.1.1 Package Information

Product Name	Product Type	Package	Ordering Number
ADM7001/X	ADM7001/X	LQFP-48-1	Q67801H 2A ¹⁾

1) contact Infineon for the updated ordering information

1.2 Features

Main features:

- IEEE 802.3 compatible 10Base-T and 100Base-T physical layer interface and ANSI X3.263 TP-PMD compatible transceiver.
- Single chip, integrated physical layer and transceivers for 10Base-T and 100BASE-TX function.
- Medium Independent Interface (MII), Reduced MII (RMII) and General Purpose Serial Interface (GPSI) for high port count switch.
- Built-in 10 Mbit transmit filter.
- 10 Mbit PLL, exceeding tolerances for both preamble and data jitter.
- 100 Mbit PLL, combined with the digital adaptive equalizer and performance up to 120 meters for UTP 5.
- 125 MHz Clock Generator and Timing Recovery.
- Integrated Base Line Wander Correction.
- Carrier Integrity Monitor function supported.
- Supports FEFI when Auto Negotiation disabled.
- Supports Auto MDIX function for Plug-and-Play
- IEEE 802.3u Clause 28 compliant auto negotiation for full 10 Mbit/s and 100 Mbit/s control.
- Supports programmable LED for different Switch Application and Power On LED Self Test.
- Supports Cable Length Indication both in MII Register and LED (Programmable)
- Supports PECL interface for fiber connection.
- Supports TP vs. FX Medium Converter function.
- Supports Fault Propagation function for medium converter.
- Supports 10K Bytes Jumbo Packet with Clock Skew 150 ppm.

- Built-in Clock Generator and Power On Reset Signal to save system cost.
- 48 LQFP without regulator.
- Supports Power saving function.
- Supports Parallel LED output.

1.3 Block Diagram

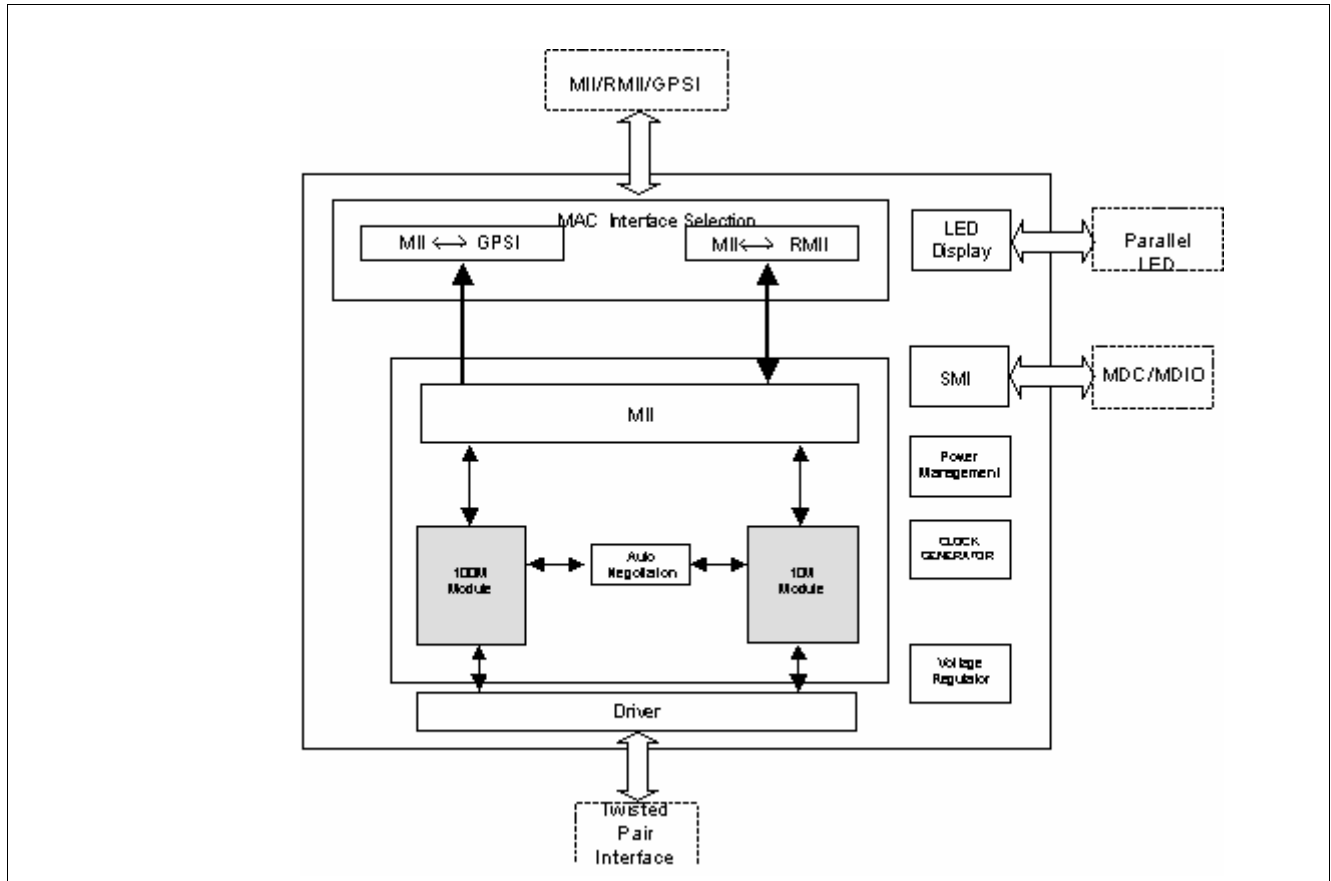


Figure 1 ADM7001/X Block Diagram

2 Interface Description

2.1 Pin Diagram

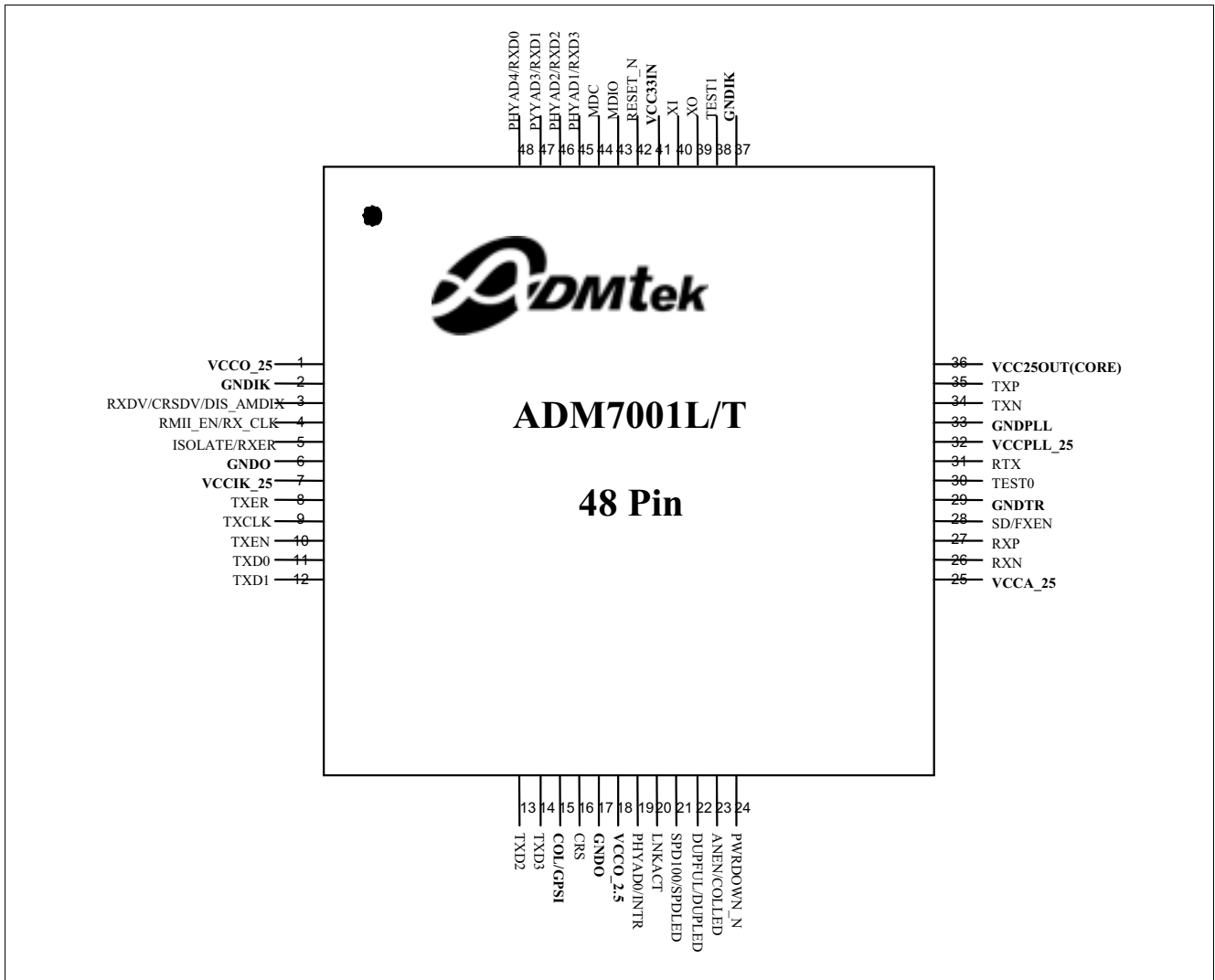


Figure 2 Pin Diagram

2.2 Pin Description

Note: For those pins, which have multiple functions, pin name is separated by slash ("/"). If not specified, all signals are default to digital signals. Please refer to [Table 1](#) Pin Type Descriptions' for an explanation of pin abbreviations.

Table 1 Abbreviations for Pin Type

Abbreviations	Description
I	Standard input-only pin. Digital levels.
O	Output. Digital levels.
I/O	I/O is a bidirectional input/output signal.
AI	Input. Analog levels.
AO	Output. Analog levels.
A/O	Input or Output. Analog levels.
PWR	Power
GND	Ground
MCL	Must be connected to Low (JEDEC Standard)
MCH	Must be connected to High (JEDEC Standard)
NU	Not Usable (JEDEC Standard)
NC	Not Connected (JEDEC Standard)

Table 2 Abbreviations for Buffer Type

Abbreviations	Description
Z	High impedance
PU1	Pull up, 10 k Ω
PD1	Pull down, 10 k Ω
PD2	Pull down, 20 k Ω
TS	Tristate capability: The corresponding pin has 3 operational states: Low, high and high-impedance.
OD	Open Drain. The corresponding pin has 2 operational states, active low and tristate, and allows multiple devices to share as a wire-OR. An external pull-up is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.
OC	Open Collector
PP	Push-Pull. The corresponding pin has 2 operational states: Active-low and active-high (identical to output with no type attribute).
OD/PP	Open-Drain or Push-Pull. The corresponding pin can be configured either as an output with the OD attribute or as an output with the PP attribute.
ST	Schmitt-Trigger characteristics
TTL	TTL characteristics

2.2.1 Twisted Pair Interface, 5 Pins
Table 3 Twisted Pair Interface, 5 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
35	TXP	AI/O		Twisted Pair Transmit Output Positive
34	TXN	AI/O		Twisted Pair Transmit Output Negative
27	RXP	AI/O		Twisted Pair Receive Input Positive
26	RXN	AI/O		Twisted Pair Receive Input Negative
28	Power On Setting FXEN	AI		Fiber Enable Value on this pin will be latched by ADM7001/X/X during power on reset as fiber select signal. 0 _B , Twisted Pair Mode 1 _B , Fiber Optic Mode
	Fiber Mode SDP			100BASE-FX Signal Detect. After power on reset stage, this pin acts as signal detect signal from external fiber optic transceiver in case FXEN is detected as high during power on reset. 0 _B , No signal detected 1 _B , Signal

2.2.2 Digital Ground/Power, 7 Pins

Table 4 Digital Ground/Power, 7 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
6, 17	GND0	D,GND		Ground used by 3.3 V I/O.
2, 37	GNDIK	D,GND		Ground used by Core.
1, 18	VCCO_25	D,PWR		2.5V Power used by Digital I/O Pad.
7	VCCIK_25	D,PWR		2.5 V Power used by Core

2.2.3 Ground and Power, 5 Pins

Table 5 Ground and Power, 5 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
41	VCC3IN	A,PWR		3.3V Power input to ADM7001/X and used by built-in 3.3 V to 2.5 V regulator.
36	VCC25OUT	A,PWR		2.5V Power output by ADM7001/X. Maximum Supply current from this pin is 200 mA
29	GNDTR	A,GND		Analog Ground Pad
25	VCCA_25	A,PWR		Analog 2.5 V Power
32	VCCPLL_25	A,PWR		Analog 2.5 V Power used by Clock Generator module.

2.2.4 Clock Input, 2 Pins
Table 6 Clock Input, 2 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
40	XI/OSCI	I	CTL	Crystal/Oscillator input. 25M Crystal/Oscillator Input in MII mode and 50M Clock input in RMII mode (Also called REFCLK in RMII Mode). <i>Note: CTL: Crystal</i>
39	XO	O	CTL	Crystal output. When 25M Oscillator is used, this pin should left unconnected. Capable of driving one XI input for multiple port application. <i>Note: CTL: Crystal</i>

2.2.5 MII/RMII/GPSI Interface, 16 pins
Table 7 MII/RMII/GPSI Interface, 16 pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
9	MII Mode TXCLK	O	16mA	MII Transmit Clock. 25M Clock output in 100BASE-X mode and 2.5M Clock output for 10BASE-T mode. This clock is continuously driven output and generated from XI. Before Speed is recognized, this pin drives out continuous 25M clock
	RMII Mode TXCLK			N/A
	GPSI Mode TXCLK			GPSI Transmit Clock. 10M Clock output in 10BASE-T mode.

Table 7 MII/RMII/GPSI Interface, 16 pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
14, 13, 12, 11	MII Mode TXD[3:0]	I	TTL PD	Transmit Data. Nibble-wide transmit data stream in MII mode. These four bits are synchronous to the rising edge of TXCLK and TXD[3] is the most significant bit
	RMII Mode TXD[3:0]			Di-bits Transmit Data. TXD0 and TXD1 for the di-bits that are transmitted and are driven synchronously to REFCLK. TXD[1] is the MSB. Note that in 100Mb/s mode, TXD can change once per REFCLK cycle, whereas in 10Mb/s mode, TXD must be held steady for 10 consecutive REFCLK cycles. TXD[3] and TXD[2] are not used in RMII Mode, left unconnected or pull down externally for normal operation.
	GPSI Mode TXD[3:0]			Serial Transmit Data. TXD0 for the designated port inputs the data that is transmitted and is driven synchronously to TXCLK in 10Mb/s mode. When ADM7001/X is programmed into GPSI mode, TXD[3:1] should be left unconnected or pull down externally for normal operation.
10	MII Mode TXEN	I	TTL PD	Transmit Enable. Transmit Enable to indicate that the data on TXD[3:0] is valid.
	RMII Mode TXEN			Transmit Enable. TXEN indicates that the di-bit on TXD is valid and it is driven synchronously to REFCLK.
	GPSI Mode TXEN			Transmit Enable. Transmit Enable to indicate that the data on TXD0 is valid.
8	MII Mode TXER	I	TTL PD	Transmit Error. Active high signal to indicate that there is error condition requested by MAC.
	RMII Mode TXER			Transmit Error. Active high signal to indicate that there is error condition requested by MAC.
	GPSI Mode LOW			Keep Low in GPSI Mode.

Table 7 MII/RMII/GPSI Interface, 16 pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
4	Power On Setting RMII_EN	I	LVTTL PD	RMII Enable. Used to select MII or RMII operation. The default value during power on reset is 0 (Before RMII_EN and GPSI value is determined) <i>Note: LVTTL: Low Voltage TTL Level</i> 0 _B , MII Mode 1 _B , RMII Mode
	MII Mode RX_CLK	O	16mA	MII Receive Clock. 25M Clock output in 100BASE-X mode, 2.5M Clock output for 10BASE-T MII mode. This clock is recovered from the received data on the cable input. Due to recovered from incoming receive data, it is possible that RXCLK starts running yet RXDV keeps low for a while. During power on reset, there is no receiving clock driven by ADM7001/X
	RMII Mode CLKO50			RMII 50M Clock Output. This pin outputs continuous 50M clock in RMII mode. To reduce the BOM cost for system application, user can connect this pin directly to REFCLK to proper RMII operation.
	GPSI Mode RX_CLK			GPSI Receive Clock. 10M clock for 10BASE-T GPSI mode. This clock is recovered from the received data on the cable input. Due to recovered from incoming receive data, it is possible that RXCLK starts running yet CRS keeps low for a while. During power on reset, there is no receiving clock driven by ADM7001/X. <i>Note: That clock on this pin will not be active during power on reset due to power on setting.</i>

Interface Description
Table 7 MII/RMII/GPSI Interface, 16 pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
3	Power On Setting DIS_AMDIX_EN	I	LVTTL PD	Disable Auto Crossover Function Value on this pin will be latched by ADM7001/X to select Auto Cross-Over Function. <i>Note: LVTTL: Low Voltage TTL Level</i> 0 _B , Enable Auto Crossover 1 _B , Disable Auto Crossover
	MII Mode RXDV	O	8mA	MII Receive Data Valid. Active high signal to indicate that the data on RXD[3:0] is valid. Synchronous to the rising edge of RXCLK in MII mode.
	RMII Mode CRSDV			RMII Carrier Sense/Receive Data Valid. Represents Receive Carrier Sense and Data Valid in RMII mode. CRSDV asserts when the receive medium is non-idle. The assertion of CRSDV is asynchronous to REFCLK. At the de-assertion of carrier, CRSDV de-asserts synchronously to REFCLK only on the first di-bit of RXD. If there is still data in the FIFO not yet presented onto RXD, then on the second di-bit of RXD, CRSDV is asserted synchronously to REFCLK. The toggling of CRSDV_P on the first and second di-bit continues until all the data in the FIFO is presented onto RXD. CRSDV is asserted for the duration of carrier activity for a false carrier event.
	GPSI Mode LOW			Keep Low in GPSI Mode.
45, 46, 47, 48	Power On Setting PHYAD[1:4]	I	TTL PD	PHY Address Select Value on these 4 pins combined with PHYAD0 will be stored into ADM7001/X as PHY physical address during power on reset. After power on reset, these 4 pins are output.
	MII Mode RXD[3:0]	O	8mA	MII Receive Data. Nibble-wide receive data stream in MII mode. These four bits are synchronous to the rising edge of RX_CLK and RXD[3] is the most significant bit.
	RMII Mode RXD[1:0]			RMII Receive Data. RXD0 and RXD1 for the di-bits that are received and are driven synchronously to REFCLK. RXD[1] is the MSB. Note that in 100Mb/s mode, RXD can change once per REFCLK cycle, whereas in 10Mb/s mode, RXD must be held steady for 10 consecutive REFCLK cycles. RXD[3:2] have not used in this mode.
	GPSI Mode RXD			GPSI Receive Data. RXD0 for the designated port inputs the data that is transmitted and is driven synchronously to RX_CLK in 10Mb/s mode. RXD[3:1] have not used in this mode.

Table 7 MII/RMII/GPSI Interface, 16 pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
5	Power On Setting ISOLATE	I	TTL PD	ISOLATE Value on this pin will be latched by ADM7001/X during power on reset. 0_B , Normal Operation 1_B , All MII outputs are tri-stated. All MII Inputs(TXD, TXEN, TXER) are ignored
	MII Mode RXER	O	4mA	MII Receive Error. Active high signal to indicate that there is error condition detected by ADM7001/X. When error is detected, RXER will be high and maintains high until RXDV is de-asserted.
	RMII Mode RXER			RMII Receive Error. Active high signal to indicate that there is error condition detected by ADM7001/X. When error is detected, RXER will be high and maintains high until CRSDV is de-asserted.
GPSI Mode N/A	No Operation in GPSI Mode.			
15	Power On Setting GPSI	I	PD	GPSI Mode Select Value on this pin will be sampled by ADM7001/X during power on reset to form GPSI internal control signal. Together with RMII_EN, these two pins form three possible internal supported by ADM7001/X. RMII_EN GPSI Interface 0_B , 0_B MII 0_B , 1_B GPSI(1M8) 1_B , x RMII
	GPSI/MII Mode COL	O	8mA	GPSI/MII Collision In half duplex mode, active high to indicate that there is collision on the medium. In full duplex mode, this pin will keep low all the time.
	RMII Mode N/A			Not Available

Table 7 MII/RMII/GPSI Interface, 16 pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
16	Power On Setting REPEATER	I	LVTTL PD	Repeater Mode. Value on this pin will be latched by ADM7001/X during power on reset as repeater mode <i>Note: LVTTL: Low Voltage TTL Level</i> 0 _B , SW/NIC mode, CRS will be asserted according to RX/TX in half duplex mode. 1 _B , REPEATER mode. CRS will be asserted only in RX mode in half duplex operation.
	MII Mode CRS	O	8mA	MII Carrier Sense. This bit indicates that there is carrier sense presented on the medium. Note that in half duplex mode, this pin will also be asserted high by ADM7001/X under transmit condition. This pin is asynchronous to RX_CLK.
	RMII Mode N/A			Not Available.
GPSI Mode CRS	GPSI Carrier Sense. This bit indicates that there is carrier sense presented on the medium. Note that in half duplex mode, this pin will also be asserted high by ADM7001/X under transmit condition. This pin is asynchronous to RX_CLK.			

Note: LVTTL: Low Voltage TTL Level

2.2.6 Reset Pin

Table 8 Reset Pin

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
42	RESET#	I	ST	Reset Signal Active low to bring ADM7001/X into reset condition. Recommend keeping low for at least 200 ms to ensure the stability of the system after power on reset.

2.2.7 Clock Signals, 6 Pins

Table 9 Clock Signals, 6 pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
43	MDIO	I/O	LVTTTL PU	Management Data. MDIO transfers management data in and out of the device synchronous to MDC. <i>Note: LVTTTL: Low Voltage TTL Level</i>
44	MDC	I	LVTTTL	Management Data Reference Clock. A non-continuous clock input for management usage. ADM7001/X will use this clock to sample data input on MDIO and drive data onto MDIO according to rising edge of this clock. <i>Note: LVTTTL: Low Voltage TTL Level</i>
19	Power On Setting PHYAD0	I	LVTTTL PU	PHY Address bit 0. See RXD[3:0] description. <i>Note: LVTTTL: Low Voltage TTL Level</i>
	MII/RMII/GPSI Mode INTR#			Interrupt Default active low signal to indicate that there is interrupt event in SMI register. Active value of interrupt signal can be configured by register 18.1. Only available when interrupt mode is selected. <i>Note: LVTTTL: Low Voltage TTL Level</i>

Table 9 Clock Signals, 6 pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
24	PWRDOWN#	I	LVTTL PU	Low Power Operation. <i>Note: When RESET# is reset to 0 and PWRDOWN# is set to 0, whole ADM7001/X blocks will be disabled.</i> 0 _B , ADM7001/X in low power mode operation. All blocks except the energy detection and crystal oscillator are deactivated. 1 _B , ADM7001/X in normal mode operation. <i>Note: LVTTL: Low Voltage TTL Level</i>
38, 30	TEST[1:0]	I	LVTTL PD	Industrial Test Pin. Keeps low for normal operation. <i>Note: LVTTL: Low Voltage TTL Level</i>

2.2.8 LED Interface, 4 Pins
Table 10 LED Interface, 4 Pins

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
20	Reserved	I	TTL PU	Reserved.
	LNKACT	O	8mA	Link/Activity LED. Active low (Note) 100ms (blink 100ms) to indicate that there is transmit or receive activity after Link Up. Keeps high all the time when link is failed.
21	Power On Setting SPD100	I	TTL PU	Recommend 100M Operation. This bit is only available in TP mode. Together with ANEN to form speed mode select for ADM7001/X: ANEN SPD100 Mode $0_B, 0_B$ Force 10BASE-T Mode $0_B, 1_B$ Force 100BASE-TX Mode $1_B, 0_B$ 10M Capability $1_B, 1_B$ 10/100M Capability
	Normal Mode SPDLED	O	8mA	Speed LED.(Note) $0_B, 100M$ $1_B, 10M$ Cable Length LED. When FXEN is low and MII register 18.2 DIS_CABLEN_LED is set to 0, this pin together with COLLED and LNKACTLED form cable length information on twisted pair <i>Note: That the following indication assume recommend value on SPDLED, COLLED and LNKACTLED is high, when corresponding bit's power on setting bit is 0, polarity of corresponding bit will be inverted.</i> SPDLED COLLED LNKACTLED Cable Length <i>Note: When recommend value during power on is high, then this signal is active low; if the recommend value is low, then this signal is active high.</i> $110_B,$ >140 meters or Link Failed $110_B,$ 0 - 40 meters $100_B,$ 40 - 80 meters $000_B,$ 80 - 120 meters $xxx_B,$ Flashed Reserved

Table 10 LED Interface, 4 Pins (cont'd)

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
22	Power On Setting DUPFUL	I	TTL PU	Duplex Control This pin is only available when auto negotiation is disabled. ANEN DUPFUL Mode 0 _B , 0 _B Force to Half Duplex Mode 0 _B , 1 _B Force to Full Duplex Mode 1 _B , 0 _B Half Duplex Capability 1 _B , 1 _B Full/Half Duplex Capability
	Normal Mode DUPLED	O	8 mA	Duplex LED.(Note) <i>Note: When recommend value during power on is high, then this signal is active low; if the recommend value is low, then this signal is active high. This rule also applies to Cable Length indication</i> 0 _B , Full Duplex 1 _B , Half Duplex
23	Power On Setting ANEN	I	TTL PU	Auto Negotiation Enable. This bit is only available in TP mode. 0 _B , Disable Auto Negotiation 1 _B , Enable Auto Negotiation
	Normal Mode COLLED	O	8mA	Collision LED. Keep high (Note) when ADM7001/X is in full duplex mode and will blink 100 ms when collision condition is detected in half duplex mode. <i>Note: When recommend value during power on is high, then this signal is active low; if the recommend value is low, then this signal is active high.</i>

2.2.9 Regulator Control

Table 11 Regulator Control

Pin or Ball No.	Name	Pin Type	Buffer Type	Function
31	RTX	AI		Constant Voltage Reference. External 1.1kΩ +/- 1% resistor connection to ground.

3 Function Description

ADM7001/X integrates 100Base-X physical sub layer (PHY), 100Base-TX physical medium dependent (PMD) transceivers, and complete 10Base-T modules into a single chip for both 10 Mbps and 100 Mbps Ethernet operations. It also supports 100Base-FX operation through external fiber-optic transceivers. The device is capable of operating in either full-duplex mode or half-duplex mode in either 10 Mbps or 100 Mbps operation. Operational modes can be selected by hardware configuration pins, software settings of management registers, or determined by the on-chip auto negotiation logic.

The 10Base-T section of the device consists of the 10 Mbps transceiver module with filters and a Manchester ENDEC module.

ADM7001/X consists of seven kinds of major blocks:

- 10/100M PHY Block
- MAC Interface
- LED Display
- SMI
- Power Management
- Clock Generator
- Voltage Regulator

Each 10/100M PHY block contains:

- 10M PHY block
- 100M PHY block
- Auto-negotiation
- Other Digital Control Blocks

3.1 10/100M PHY Block

The 100Base-X section of the device implements the following functional blocks:

- 100Base-X physical coding sub-layer (PCS)
- 100Base-X physical medium attachment (PMA)
- Twisted-pair PMD (TP-PMD) transceiver

The 100Base-X and 10Base-T sections share the following functional blocks:

- Clock synthesizer module
- MII Registers
- IEEE 802.3u auto negotiation

The interface used for communication between PHY block and switch core is MII interface.

3.1.1 100Base-X Module

ADM7001/X implements 100Base-X compliant PCS and PMA, and 100Base-TX compliant TP-PMD as illustrated in [Figure 3](#). Bypass options for each of the major functional blocks within the 100Base-X PCS provide flexibility for various applications. 100 Mbit/s PHY loop back is included for diagnostic purpose.

3.1.2 100Base-TX Receiver

For 100Base-TX operation, the on-chip twisted pair receiver that consists of a differential line receiver, an adaptive equalizer and a base-line wander compensation circuits detects the incoming signal.

ADM7001/X uses an adaptive equalizer that changes filter frequency response in accordance with cable length. The cable length is estimated based on the incoming signal strength. The equalizer tunes itself automatically for any cable length to compensate for the amplitude and phase distortions incurred from the cable.

Function Description

The 100Base-X receiver consists of functional blocks required to recover and condition the 125 Mbps receive data stream. The ADM7001/X implements the 100Base-X receiving state machine diagram as given in ANSI/IEEE Standard 802.3u, Clause 24. The 125 Mbps receive data stream may originate from the on-chip twisted-pair transceiver in a 100Base-TX application. Alternatively, the receive data stream may be generated by an external optical receiver as in a 100Base-FX application.

The receiver block consists of the following functional sub-blocks:

- A/D Converter
- Adaptive Equalizer and Timing Recovery Module
- NRZI/NRZ and Serial/Parallel Decoder
- De-scrambler
- Symbol Alignment Block
- Symbol Decoder
- Collision Detect Block
- Carrier Sense Block
- Stream Decoder Block

A/D Converter

High performance A/D converter with 125M sampling rate converts signals received on RXP/RXN pins to 6-bits data streams; besides it possess auto-gain-control capability that will further improve receive performance especially under long cable or harsh detrimental signal integrity. Due to high pass characteristic on transformer, built in base-line-wander correcting circuit will cancel it out and restore its DC level.

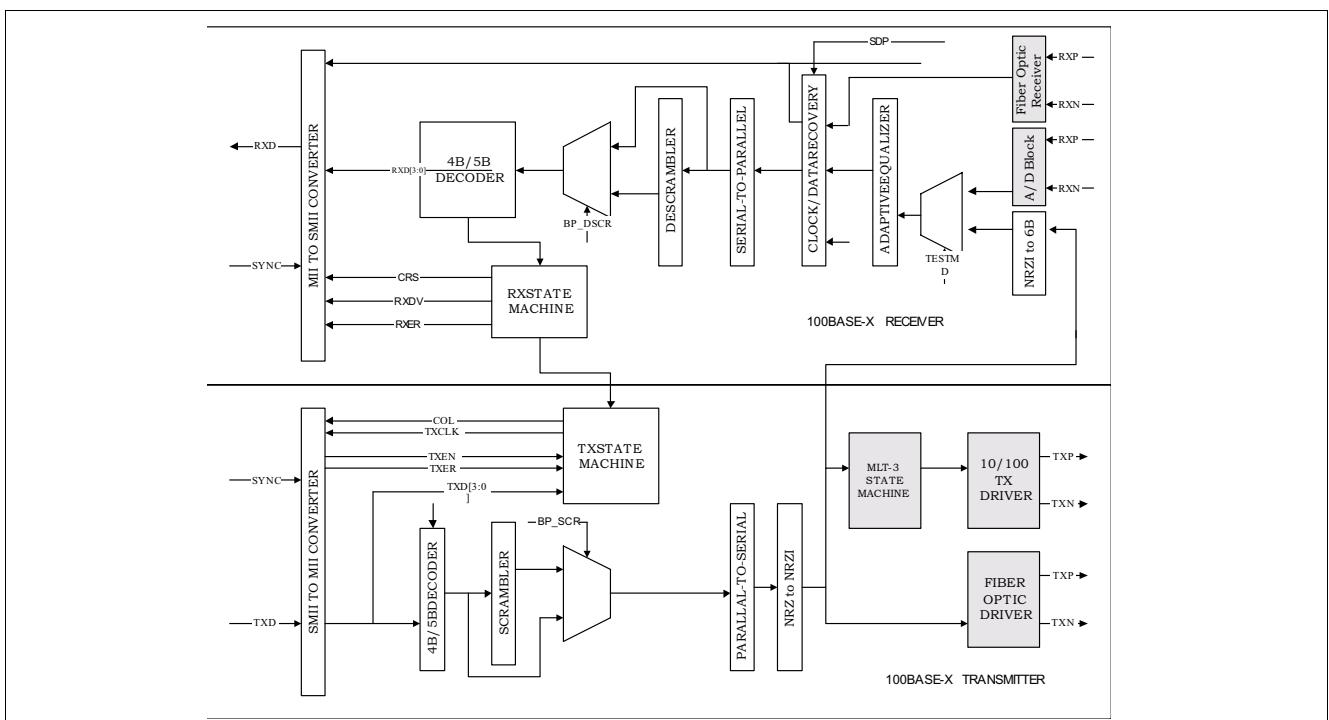


Figure 3 100Base-X Block Diagram and Data Path

Adaptive Equalizer and Timing Recovery Module

All digital design is especially immune from noise environments, and achieves better correlations between production and system testing. Baud rate Adaptive Equalizer/Timing Recovery compensates line loss induced from twisted pair and tracks far end clock at 125M samples per second. Adaptive Equalizer implemented with Feed

forward and Decision Feedback techniques meets the requirement of BER less than 10⁻¹² for transmission on CAT5 twisted pair cable ranging from 0 to 140 meters.

NRZI/NRZ and Serial/Parallel Decoder

The recovered data is converted from NRZI to NRZ. The data is not necessarily aligned to 4B/5B code group's boundary.

Data Descrambling

The descrambler acquires synchronization with the data stream by recognizing idle bursts of 40 or more bits and locking its deciphering Linear Feedback Shift Register (LFSR) to the state of the scrambling LFSR. Upon achieving synchronization, the incoming data is XORed by the deciphering LFSR and descrambled.

In order to maintain synchronization, the descrambler continuously monitors the validity of the unscrambled data that it generates. To ensure this, a link state monitor and a hold timer are used to constantly monitor the synchronization status. Upon synchronization of the descrambler the hold timer starts a 722 μ s countdown. Upon detection of at least 6 idle symbols (30 consecutive 1) within the 722 μ s period, the hold timer will reset and begin a new countdown. This monitoring operation will continue indefinitely to give a properly operating network connection with good signal integrity. If the link state monitor does not recognize at least 6 unscrambled idle symbols within 722 μ s period, the descrambler will be forced out of the current state of synchronization and reset in order to re-acquire synchronization.

Symbol Alignment

The symbol alignment circuit in the ADM7001/X determines code word alignment by recognizing the /J/K delimiter pair. This circuit operates on unaligned data from the descrambler. Once the /J/K symbol pair (11000 10001) is detected, subsequent data is aligned on a fixed boundary.

Symbol Decoding

The symbol decoder functions as a look-up table that translates incoming 5B symbols into 4B nibbles as shown in [Table 12](#). The symbol decoder first detects the /J/K symbol pair preceded by idle symbols and replaces the symbol with MAC preamble. All subsequent 5B symbols are converted to the corresponding 4B nibbles for the duration of the entire packet. This conversion ceases upon the detection of the /T/R symbol pair denoting the end of stream delimiter (ESD). The translated data is presented on the internal RXD[3:0] signal lines with RXD[0] represents the least significant bit of the translated nibble.

Table 12 Look-up Table for Translating 5B Symbols into 4B Nibbles

PCS Code-Group[4:0]	Name	MII (TXD/RXD)<3:0>	Interpretation
11110	0	0000	Data 0
01001	1	0001	Data 1
10100	2	0010	Data 2
10101	3	0011	Data 3
01010	4	0100	Data 4
01011	5	0101	Data 5
01110	6	0110	Data 6
01111	7	0111	Data 7
10010	8	1000	Data 8
10011	9	1001	Data 9
10110	A	1010	Data A
10111	B	1011	Data B

Table 12 Look-up Table for Translating 5B Symbols into 4B Nibbles (cont'd)

PCS Code-Group[4:0]	Name	MII (TXD/RXD)<3:0>	Interpretation
11010	C	1100	Data C
11011	D	1101	Data D
11100	E	1110	Data E
11101	F	1111	Data F
11111	I	Undefined	IDLEUsed as inter-stream fill code
11000	J	0101	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with K
10001	K	0101	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with J
01101	T	Undefined	Start-of-Stream Delimiter, Part 1 of 2; always used in pairs with R
0111	R	Undefined	Start-of-Stream Delimiter, Part 2 of 2; always used in pairs with T
00100	H	Undefined	Transmit Error; used to force signaling errors
00000	V	Undefined	Invalid code
00001	V	Undefined	Invalid code
00010	V	Undefined	Invalid code
00011	V	Undefined	Invalid code
00101	V	Undefined	Invalid code
00110	V	Undefined	Invalid code
01000	V	Undefined	Invalid code
01100	V	Undefined	Invalid code
10000	V	Undefined	Invalid code
11001	V	Undefined	Invalid code

Valid Data Signal

The valid data signal (RXDV) indicates that recovered and decoded nibbles are presented on the internal RXD[3:0] synchronous to receive clock, RXCLK. RXDV is asserted when the first nibble of translated /J/K is ready for transfer over the internal MII. It remains active until either the /T/R delimiter is recognized, link test indicates failure, or no signal is detected. On any of these conditions, RXDV is deasserted.

Receive Errors

The RXER signal is used to communicate with receiver error conditions. While the receiver is in a state of holding RXDV asserted, the RXER will be asserted for each code word which does not map to a valid code-group.

100Base-X Link Monitor

The 100Base-X link monitor function allows the receiver to ensure that reliable data is received. Without reliable data reception, the link monitor will halt both transmit and receive operations until a valid link is detected.

The ADM7001/X performs the link integrity test as outlined in IEEE 100Base-X (Clause 24) link monitor state diagram. The link status is multiplexed with 10 Mbits/s link status to form the reportable link status bit in serial management register 1h, and driven to the LNKACT pin.

When persistent signal energy is detected on the network, the logic moves into a Link-Ready state after approximately 500 μ s, and waits for an enable from the auto negotiation module. When receiving, the link-up state

is entered, and the transmission and reception logic blocks become active. Should auto negotiation be disabled, the link integrity logic moves immediately to the link-up state after entering the link-ready state.

Carrier Sense

Carrier sense (CRS) for 100 Mbits/s operation is asserted upon the detection of two non contiguous zeros occurring within any 10-bit boundary of the received data stream.

The carrier sense function is independent of symbol alignment. In switch mode, CRS is asserted during either packet transmission or reception. For repeater mode, CRS is asserted only during packet reception. When the idle symbol pair is detected in the received data stream, CRS is deasserted. In repeater mode, CRS is only asserted due to receive activity. CRS is intended to encapsulate RXDV.

Bad SSD Detection

A bad start of stream delimiter (Bad SSD) is an error condition that occurs in the 100Base-X receiver if carrier is detected (CRS asserted) and a valid /J/K set of code-group (SSD) is not received.

If this condition is detected, the ADM7001/X will assert RXER and present RXD[3:0] = 1110 to the internal MII for the cycles that correspond to receive 5B code-groups until at least two idle code-groups are detected. Once at least two idle code groups are detected, RXER and CRS become deasserted.

Far-End Fault

Auto negotiation provides a mechanism for transferring information from the Local Station to the link Partner that a remote fault has occurred for 100Base-TX. As auto negotiation is not currently specified for operation over fiber, the far end fault indication function (FEFI) provides this capability for 100Base-FX applications.

A remote fault is an error in the link that one station can detect while the other cannot. An example of this is a disconnected wire at a station's transmitter. This station will receive valid data and detect that the link is good via the link integrity monitor, but will not be able to detect that its transmission is not propagating to the other station.

A 100Base-FX station that detects such a remote fault may modify its transmitted idle stream from all ones to a group of 84 ones followed by a single 0. This is referred to as the FEFI idle pattern.

The FEFI function is controlled by bit 3 of register 11_H. It is initialized to 1 (encoded) if the SELFX pin is at logic high level during power on reset. If the FEFI function is enabled the ADM7001/X will halt all current operations and transmit the FEFI idle pattern when FOSD signal is de-asserted following a good link indication from the link integrity monitor. FOSD signal is generated internally from the internal signal detect circuit. Transmission of the FEFI idle pattern will continue until link up signal is asserted. If three or more FEFI idle patterns are detected by the ADM7001/X, bit 4 of the Basic mode status register (address 1h) is set to one until read by management. Additionally, upon detection of far end fault, all receive and transmit MII activities are disabled/ignored.

3.1.3 100Base-TX Transmitter

ADM7001/X implements a TP-PMD compliant transceiver for 100Base-TX operation. The differential transmit driver is shared by the 10Base-T and 100Base-TX subsystems. This arrangement results in one device that uses the same external magnetics for both the 10Base-T and the 100Base-TX transmission with simple RC component connections. The individually wave-shaped 10Base-T and 100Base-TX transmit signals are multiplexed in the transmission output driver selection.

ADM7001/X 100Base-TX transmission driver implements MLT-3 translation and wave-shaping functions. The rise/fall time of the output signal is closely controlled to conform to the target range specified in the ANSI TP-PMD standard.

3.1.4 100Base-FX Receiver

Signal is received through PECL receiver inputs from fiber transceiver, and directly passed to clock recovery circuit for data/clock recovery. Scrambler/de-scrambler is bypassed in 100Base-FX.

Automatic “Signal_Detect“ Function Block

When DIS_ANASDEN_N in register 18 is set to 0, ADM7001/X doesn't support SDP detection in fiber mode, which is used to connect to fiber transceiver to indicate there is signal on the fiber. Instead, ADM7001/X uses the data on RXP/RXN to detect consecutive 65 “1” on the receive data (Recovered from RXP/RXN) to determine whether “Signal” is detected or not. When the detect condition is true (Consecutive 65 bits “1”), internal signal detect signal will be asserted to inform receive relative blocks to be ready for coming receive activities.

3.1.5 100Base-FX Transmitter

In 100Base FX transmit, the serial data stream is driven out as NRZI PECL signals, which enter fiber transceiver in differential-pairs form. Fiber transceiver should be available working at 3.3 V environment.

3.1.6 10Base-T Module

The 10Base-T Transceiver Module is IEEE 802.3 compliant. It includes the receiver, transmitter, collision, heartbeat, loopback, jabber, waveshaper, and link integrity functions, as defined in the standard. [Figure 4](#) provides an overview for the 10Base-T module.

The ADM7001/X 10Base-T module is comprised of the following functional blocks:

- Manchester encoder and decoder
- Collision detector
- Link test function
- Transmit driver and receiver
- Serial and parallel interface
- Jabber and SQE test functions
- Polarity detection and correction

3.1.7 Operation Modes

The ADM7001/X 10Base-T module is capable of operating in either half-duplex mode or full-duplex mode. In half-duplex mode, the ADM7001/X functions as an IEEE 802.3 compliant transceiver with fully integrated filtering. The COL signal is asserted during collisions or jabber events, and the CRS signal is asserted during transmitting and receiving. In full duplex mode the ADM7001/X can simultaneously transmit and receive data.

3.1.8 Manchester Encoder/Decoder

Data encoding and transmission begin when the transmission enable input (TXEN) goes high and continues as long as the transceiver is in good link state. Transmission ends when the transmission enable input goes low. The last transition occurs at the center of the bit cell if the last bit is 1, or at the boundary of the bit cell if the last bit is 0. A differential input receiver circuit accomplishes decoding and a phase-locked loop that separates the Manchester-encoded data stream into clock signals and NRZ data. The decoder detects the end of a frame when no more mid bit transitions are detected. Within one and half bit times after the last bit, carrier sense is deasserted.

3.1.9 Transmit Driver and Receiver

The ADM7001/X integrates all the required signal conditioning functions in its 10Base-T block such that external filters are not required. Only one isolation transformer and impedance matching resistors are needed for the 10Base-T transmit and receive interface. The internal transmit filtering ensures that all the harmonics in the transmission signal are attenuated properly.

3.1.10 Smart Squelch

The smart squelch circuit is responsible for determining when valid data is present on the differential receives. The ADM7001/X implements an intelligent receive squelch on the RXP/RXN differential inputs to ensure that impulse

Function Description

noise on the receive inputs will not be mistaken for a valid signal. The squelch circuitry employs a combination of amplitude and timing measurements (as specified in the IEEE 802.3 10Base-T standard) to determine the validity of data on the twisted-pair inputs.

The "analog squelch circuit" checks the signal at the start of the packet and any pulses not exceeding the squelch level (either positive or negative, depending upon polarity) will be rejected. Once this first squelch level is overcome correctly, the opposite squelch level must then be exceeded within 150ns. Finally, the signal must exceed the original squelch level within an additional 150ns to ensure that the input waveform will not be rejected.

Only after all these conditions have been satisfied will a control signal be generated to indicate to the remainder of the circuitry that valid data is present.

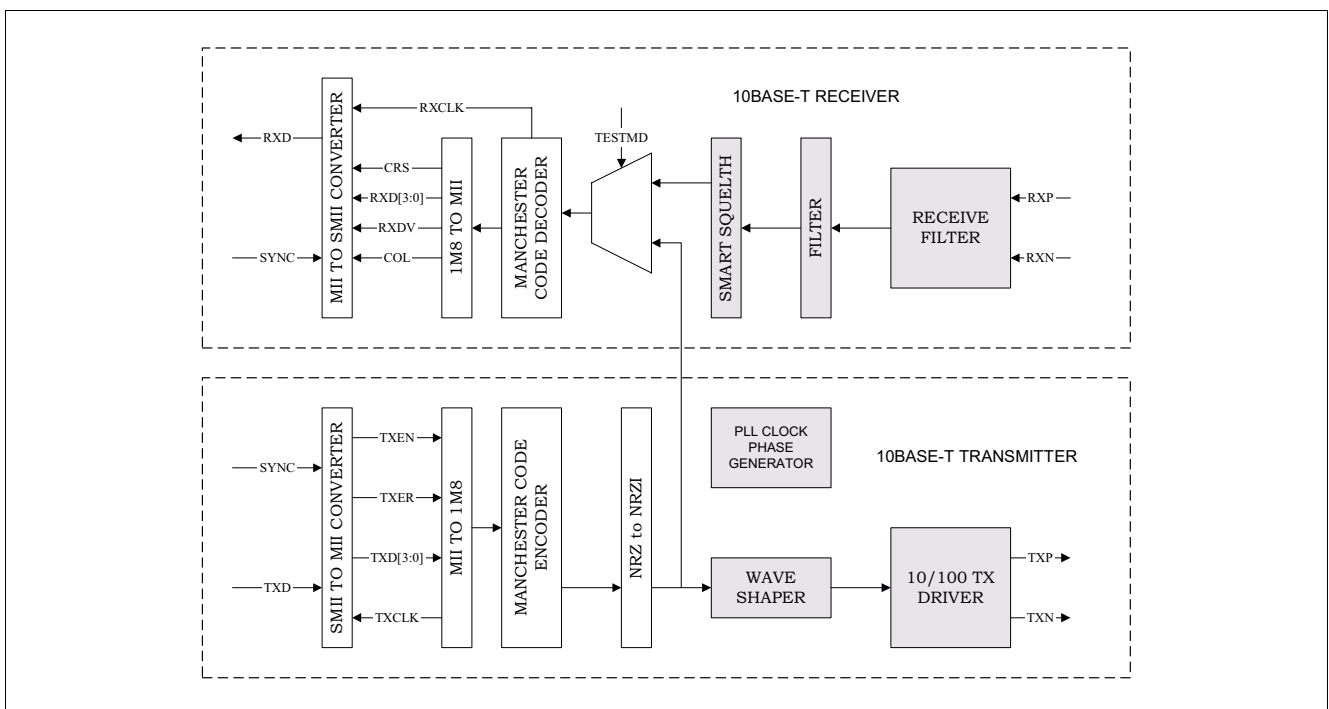


Figure 4 10Base-T Block Diagram and Data Path

Valid data is considered to be present until the squelch level has not been generated for a time longer than 200 ns, indicating end of packet. Once good data has been detected, the squelch levels are reduced to minimize the effect of noise, causing premature end-of-packet detection. The receive squelch threshold level can be lowered for use in longer cable applications. This is achieved by setting bit 7 of register address 10_H.

3.1.11 Carrier Sense

Carrier Sense (CRS) is asserted due to receive activity once valid data is detected via the smart squelch function. For 10 Mbit/s half duplex operation, CRS is asserted during either packet transmission or reception. For 10 Mbit/s full duplex and repeater mode operations, the CRS is asserted only due to receive activity.

3.1.12 Collision Detection

Collision is detected internal to the MAC, which is generated by an AND function of TXEN and RXDV derived from internal timing recovery circuitry. Note should be taken that due to TXEN and RXDV are asynchronous to each other, COL signal outputted by ADM7001/X is irrelevant to either TXCLK or RXCLK.

3.1.13 Jabber Function

The jabber function monitors the ADM7001/X output and disables the transmitter if it attempts to transmit a longer than legal sized packet. If TXEN is high for greater than 24ms, the 10Base-T transmitter will be disabled. Once disabled by the jabber function, the transmitter stays disable for the entire time that the TXEN signal is asserted. This signal has to be de-asserted for approximately 408 ms (The un-jab time) before the jabber function re-enables the transmit outputs. The jabber function can be disabled by programming bit 0 of register address 10_H to high.

3.1.14 Link Test Function

A link pulse is used to check the integrity of the connection with the remote end. If valid link pulses are not received, the link detector disables the 10Base-T twisted-pair transmitter, receiver, and collision detection functions.

The link pulse generator produces pulses as defined in IEEE 802.3 10Base-T standard. Each link pulse is nominally 100 ns in duration and is transmitted every 16 ms, in the absence of transmit data. Setting bit 10 of register 10_H to high can disable link pulse check function.

3.1.15 Automatic Link Polarity Detection

ADM7001/X's 10Base-T transceiver module incorporates an "automatic link polarity detection circuit". The inverted polarity is determined when seven consecutive link pulses of inverted polarity or three consecutive packets are received with inverted end-of-packet pulses. If the input polarity is reversed, the error condition will be automatically corrected and reported in bit 13 of register 11_H.

3.1.16 Clock Synthesizer

The ADM7001/X implements a clock synthesizer that generates all the reference clocks needed from a single external frequency source. The clock source must be a TTL level signal at 25 MHz \pm 50ppm.

3.1.17 Auto Negotiation

The Auto Negotiation function provides a mechanism for exchanging configuration information between two ends of a link segment and automatically selecting the highest performance mode of operation supported by both devices. Fast Link Pulse (FLP) Bursts provides the signaling used to communicate auto negotiation abilities between two devices at each end of a link segment. For further detail regarding auto negotiation, refer to Clause 28 of the IEEE 802.3u specification. The ADM7001/X supports four different Ethernet protocols, so the inclusion of auto negotiation ensures that the highest performance protocol will be selected based on the ability of the link partner.

The auto negotiation function within the ADM7001/X can be controlled either by internal register access or by the use of configuration pins are sampled. If disabled, auto negotiation will not occur until software enables bit 12 in register 0. If auto negotiation is enabled, the negotiation process will commence immediately.

When auto negotiation is enabled, the ADM7001/X transmits the abilities programmed into the auto negotiation advertisement register at address 04_H via FLP bursts. Any combination of 10 Mbps, 100 Mbps, half duplex and full duplex modes may be selected. Auto negotiation controls the exchange of configuration information. Upon successfully auto negotiation, the abilities reported by the link partner are stored in the auto negotiation link partner ability register at address 05_H.

The contents of the "auto negotiation link partner ability register" are used to automatically configure to the highest performance protocol between the local and far-end nodes. Software can determine which mode has been configured by auto negotiation by comparing the contents of register 04_H and 05_H and then selecting the technology whose bit is set in both registers of highest priority relative to the following list.

- 100Base-TX full duplex (highest priority)
- 100Base-TX half duplex
- 10Base-T full duplex

- 10Base-T half duplex (lowest priority)

The basic mode control register at address 0_H provides control of enabling, disabling, and restarting of the auto negotiation function. When auto negotiation is disabled, the speed selection bit (bit 13) controls switching between 10 Mbps or 100 Mbps operation, while the duplex mode bit (bit 8) controls switching between full duplex operation and half duplex operation. The speed selection and duplex mode bits have no effect on the mode of operation when the auto negotiation enable bit (bit 12) is set.

The basic mode status register (BMSR) at address 1_H indicates the set of available abilities for technology types (bit 15 to bit 11), auto negotiation ability (bit 3), and extended register capability (bit 0). These bits are hardwired to indicate the full functionality of the ADM7001/X. The BMSR also provides status on:

- Whether auto negotiation is complete (bit 5)
- Whether the Link Partner is advertising that a remote fault has occurred (bit 4)
- Whether a valid link has been established (bit 2)

The auto negotiation advertisement register at address 4_H indicates the auto negotiation abilities to be advertised by the ADM7001/X. All available abilities are transmitted by default, but writing to this register or configuring external pins can suppress any ability.

The auto negotiation link partner ability register at address 05_H indicates the abilities of the Link Partner as indicated by auto negotiation communication. The contents of this register are considered valid when the auto negotiation complete bits (bit 5, register address 1_H and bit 4, register 17_H) are set.

3.1.18 Auto Negotiation and Speed Configuration

The twelve sets of four pins listed in [Table 13](#) configure the speed capability of each channel of ADM7001/X. The logic state of these pins is latched into the advertisement register (register address 4_H) for auto negotiation purpose. These pins are also used for evaluating the default value in the base mode control register (register 0_H) according to [Table 13](#) Channel Configuration.

3.2 MAC Interface

The ADM7001/X interfaces to 10/100 Media Access Controllers (MAC) via the RMII, MII, or GPSI Interface.

3.2.1 Reduced Media Independent Interface (RMII)

The reduced media Independent interface (RMII) is compliant to the RMII consortium's RMII Rev. 1.2 specification. The REFCLK pin that supplies the 50 MHz reference clock to the ADM7001/X is used as the RMII REFCLK signal. All RMII signals with the exception of the assertion of CRSDV_P are synchronous to REFCLK. See [Figure 5](#)

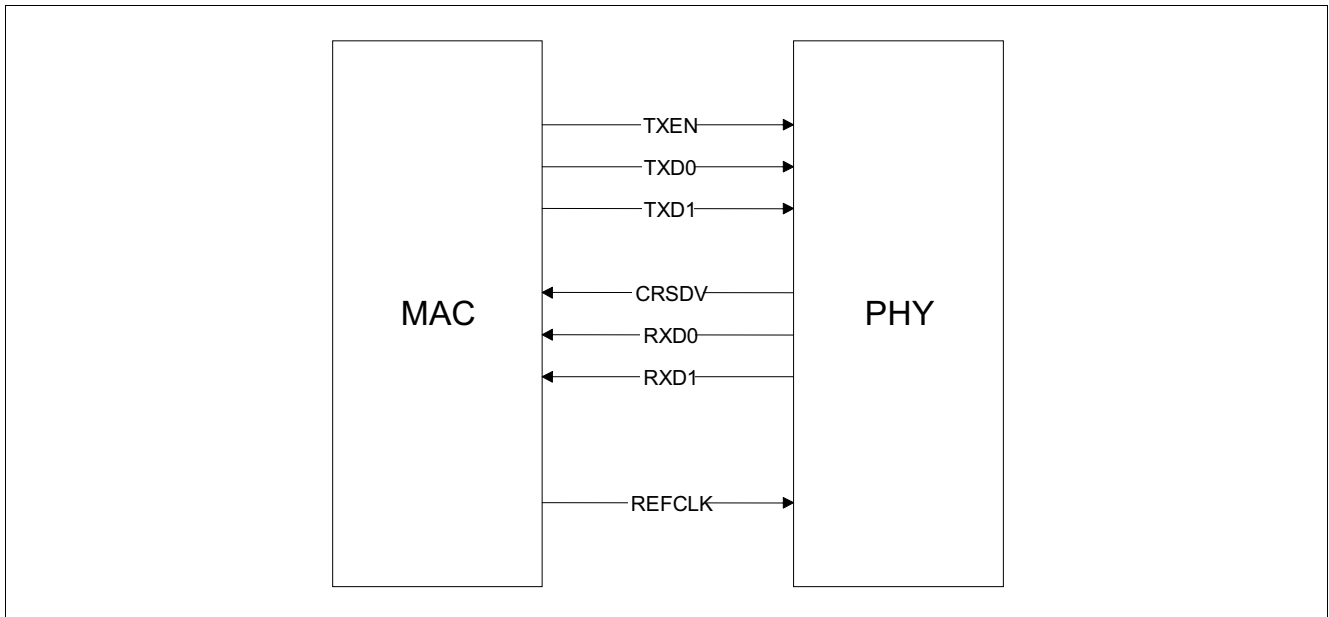


Figure 5 RMII Signal Diagram

3.2.2 Receive Path for 100M

Figure 6 shows the relationship among REFCLK, CRSDV, RXD and RXER while receiving a valid packet. Carrier sense is detected, which causes CRSDV to assert asynchronously to REFCLK. The received data is then placed into the FIFO for resynchronization. After a minimum of 12 bits are placed into the FIFO, the received data is presented onto RXD[1:0] synchronously to REFCLK. Note that while the FIFO is filling up RXD[1:0] is set to 00 until the first received di-bit of preamble (01) is presented onto RXD[1:0]. When carrier sense is de-asserted at the end of a packet, CRSDV is de-asserted when the first di-bit of a nibble is presented onto RXD[1:0] synchronously to REFCLK. If there is still data in the FIFO that has not yet been presented onto RXD[1:0], then on the second di-bit of a nibble, CRSDV reasserts. This pattern of assertion and de-assertion continues until all received data in the FIFO has been presented onto RXD[1:0]. RXER is inactive for the duration of the received valid packet.

Figure 7 shows the relationship among REFCLK, CRSDV and RXD[1:0] during a received false carrier event. CRSDV is asserted asynchronously to REFCLK as in the valid receive case shown in . However, once false carrier is detected, RXD[1:0] is changed to (10) (11) (Value 1110 in MII) and RXER is asserted. Both RXD[1:0] and RXER transition synchronously to REFCLK. After carrier sense is de-asserted, CRSDV is de-asserted synchronously to REFCLK.

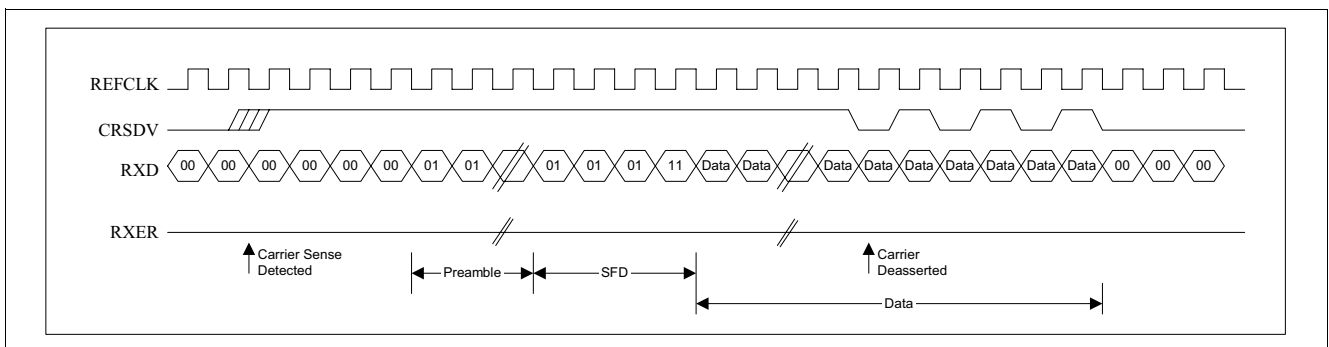


Figure 6 RMII Reception Without Error

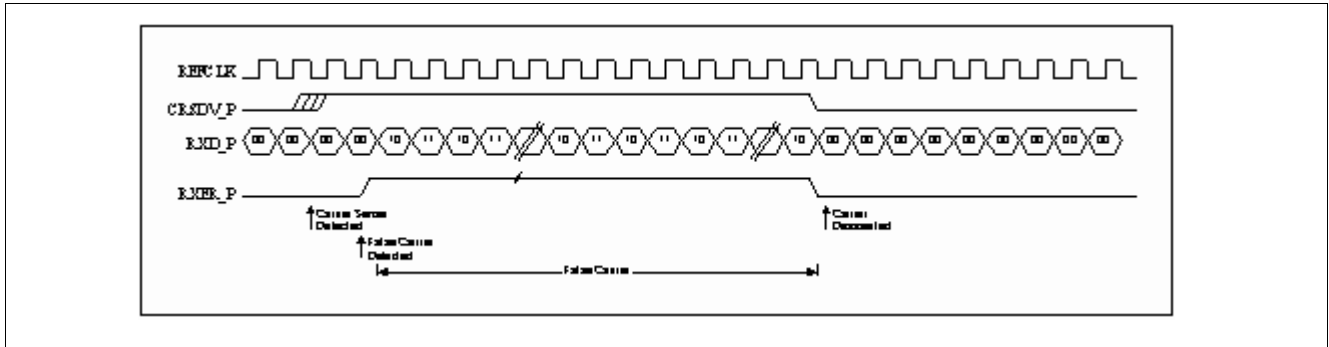


Figure 7 RMI Reception with False Carrier (100M Only)

A receive symbol error event is shown in Figure 8. The packet with the symbol error is treated as if it were a valid packet with the exception that all di-bits are substituted with the (01) pattern.

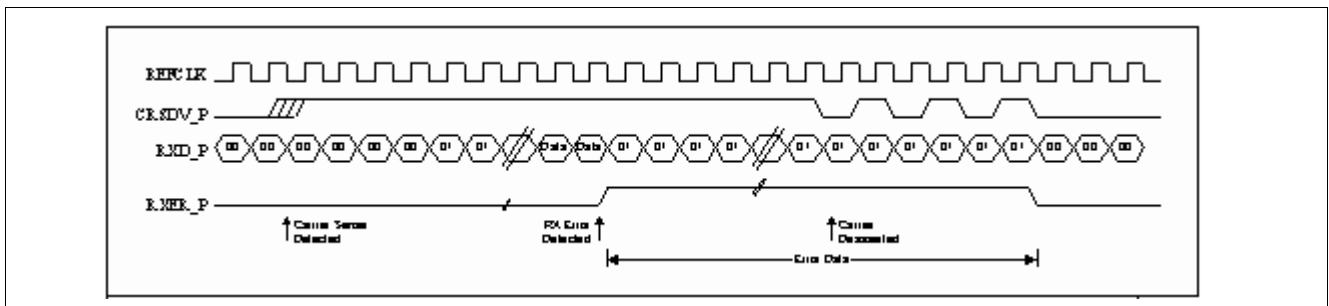


Figure 8 RMI Reception with Symbol Error

3.2.3 Receive Path for 10M

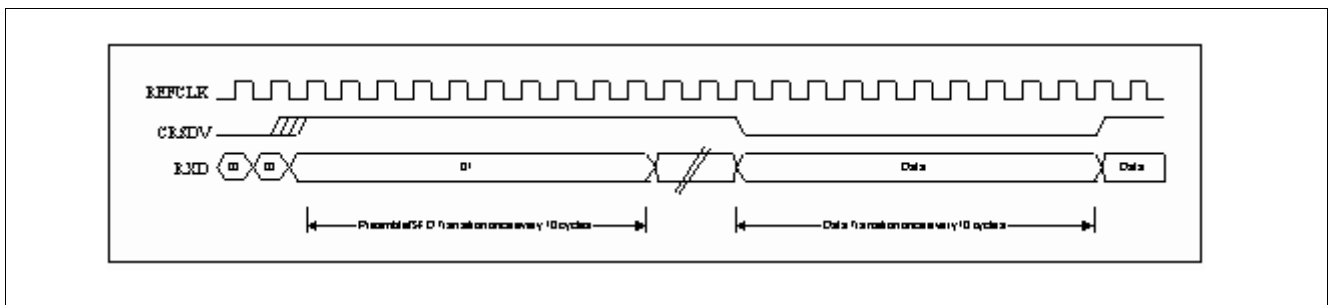


Figure 9 10M RMI Receive Diagram

In 10M Mode, RXER will maintain low all the time due to False Carrier and symbol error is not supported by 10M Mode. Different from 100M mode, RXD and CRSDV can transit once per 10 REFCLK cycles. After carrier sense is de-asserted yet the FIFO data is not fully presented onto RXD, the CRSDV de-assertion and re-assertion also follow this rule.

3.2.4 Transmit Path for 100M

Figure 10 shows the relationship among REFCLK, TXEN and TXD[1:0] during a transmit event. TXEN and TXD[1:0] are synchronous to REFCLK. When TXEN is asserted, it indicates that TXD[1:0] contains valid data to be transmitted. When TXEN is de-asserted, value on TXD[1:0] should be ignored. If an odd number of di-bits are presented onto TXD[1:0] and TXEN, the final di-bit will be discarded by ADM7001/X.

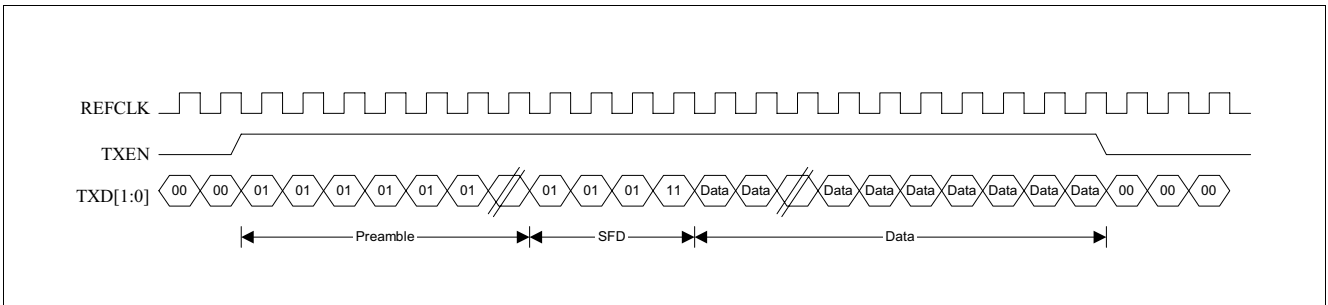


Figure 10 100M RMIITransmit Diagram

3.2.5 Transmit Path for 10M

In 10MBSE-T mode, each di-bit must be repeated 10 times by the MAC, TXEN and TXD[1:0] should be synchronous to REFCLK. When TXEN is asserted, it indicates that data on TXD[1:0] is valid for transmission.

In 10Base-T mode, it is possible that the number of preamble bits and the number of frame bits received are not integer nibbles. The preamble is always padded up such that the SFD appears on the RMII aligned to the nibble boundary. Extra bits at the end of the frame that do not complete a nibble are truncated by AD7001. **Figure 11** shows the timing diagram for 10M Transmission.

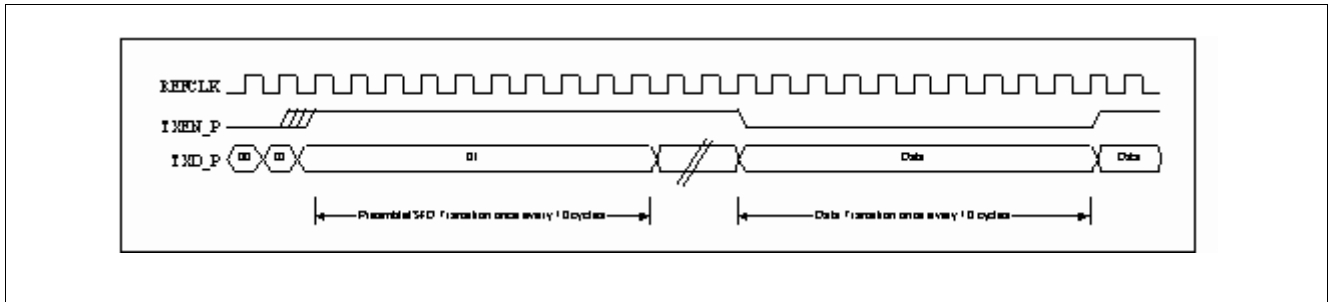


Figure 11 10M RMIITransmit Diagram

Table 13 Channel Configuration

Recommend Value			Auto Negotiation		Capability			
ANENDIS	REC_10M	TP_FULL DUPLEX	Enable	Disable	100 Full	100 Half	10 Full	10 Half
1	1	1	√		√	√	√	√
1	1	0	√			√		√
1	0	1	√				√	√
1	0	0	√					√
0	1	1		√	√			
0	1	0		√		√		
0	0	1		√			√	
0	0	0		√				√

3.2.6 Media Independent Interface (MII)

Signal Diagram for MII interface is shown in **Figure 12**.

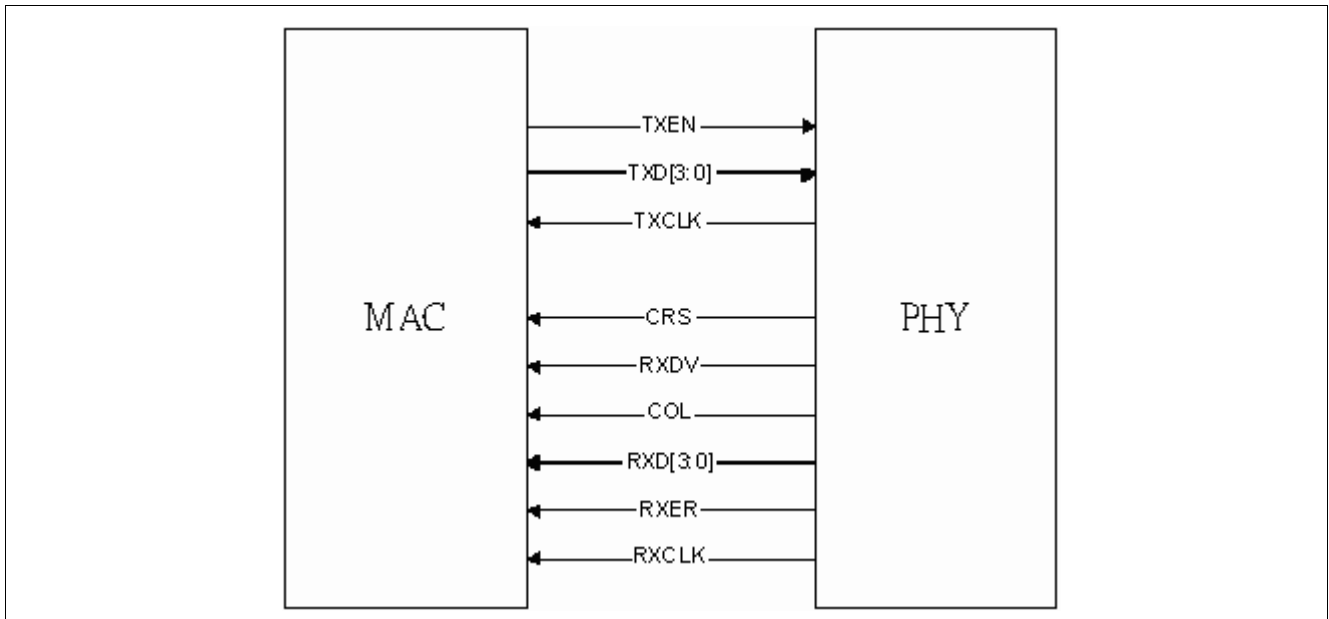


Figure 12 MII Signal Diagram

3.2.7 Receive Path for MII

Figure 13 shows the relationship among RXCLK, RXDV, RXD and CRS during a reception of valid packet. Carrier sense is detected and asserted asynchronously to RXCLK by ADM7001/X. When ADM7001/X detects there is valid data, RXDV and the received data are presented onto RXD[3:0] synchronously to RX_CLK. Whenever received data is not valid anymore, RXDV will be de-asserted by ADM7001/X and "0" will be put on RXD[3:0].

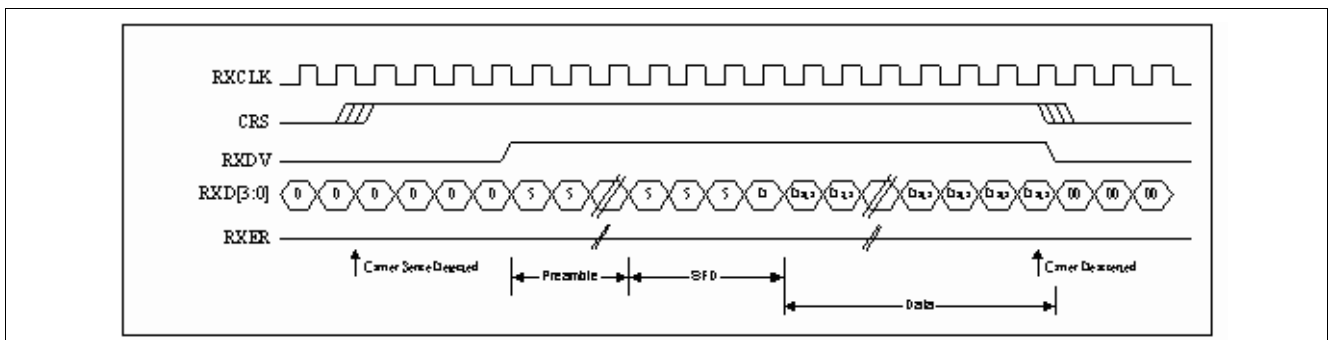


Figure 13 MII Receive Without Error

Figure 14 shows the relationship among RXCLK, RXDV and RXD[3:0] during a received false carrier event. CRS is asserted asynchronously to RXCLK as in the valid receive case shown in Figure 15. However, once false carrier is detected, RXD[3:0] is changed to (1110) and RXER is asserted. Both RXD[3:0] and RXER transit synchronously to RXCLK.

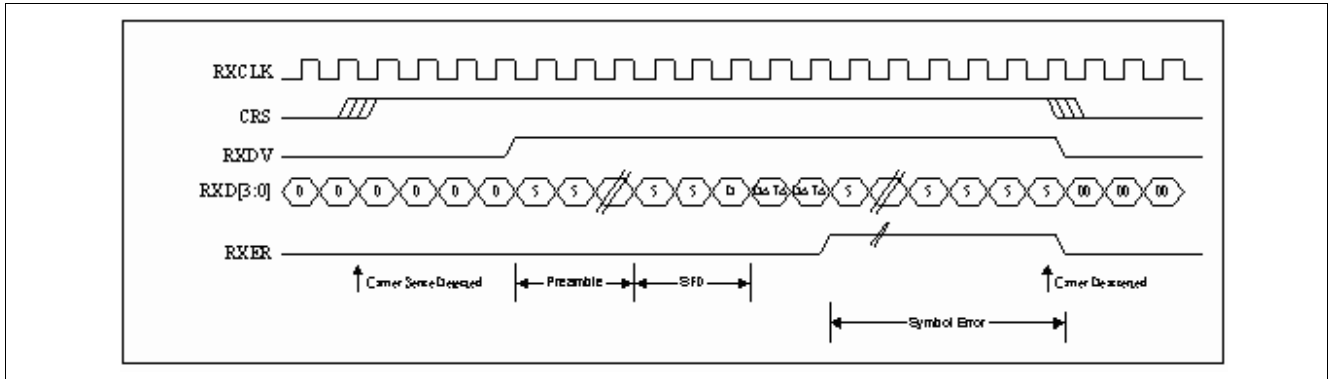


Figure 14 MII Receive With False Carrier

A receive symbol error event is shown in [Figure 15](#). The packet with the symbol error is treated as if it were a valid packet with the exception that all bits are substituted with the (0101) pattern. RXER will keep low in 10M Operation.

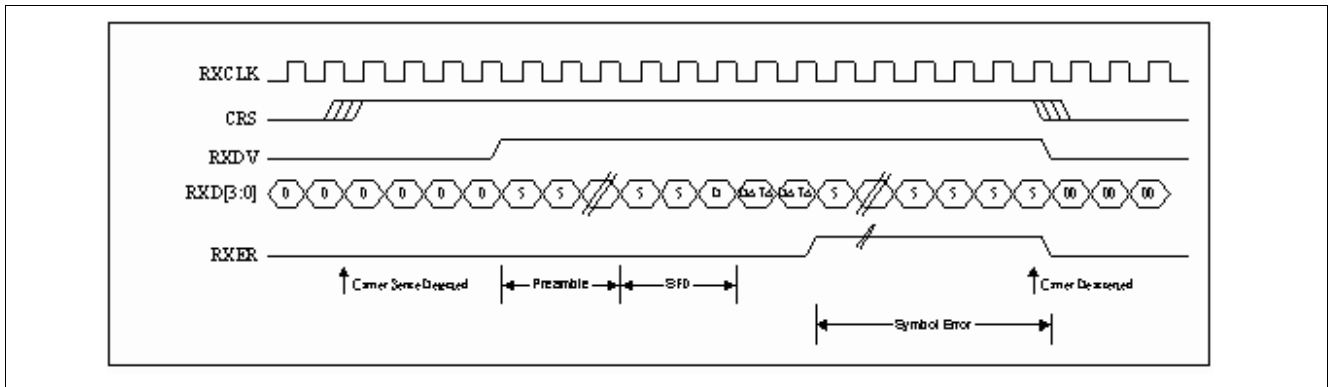


Figure 15 MII Receive With Symbol Error(100M Only)

3.2.8 Transmit Path for MII

Figure 16 shows the relationship among TXCLK, TXEN and TXD[3:0] during a transmit event. TXEN and TXD[3:0] are synchronous to TXCLK, which is generated by MAC. TXCLK is running at 25M in 100M mode and 2.5M in 10M mode. When TXEN is asserted, it indicates that TXD[3:0] contains valid data to be transmitted. When TXEN is de-asserted, value on TXD[1:0] should be ignored.

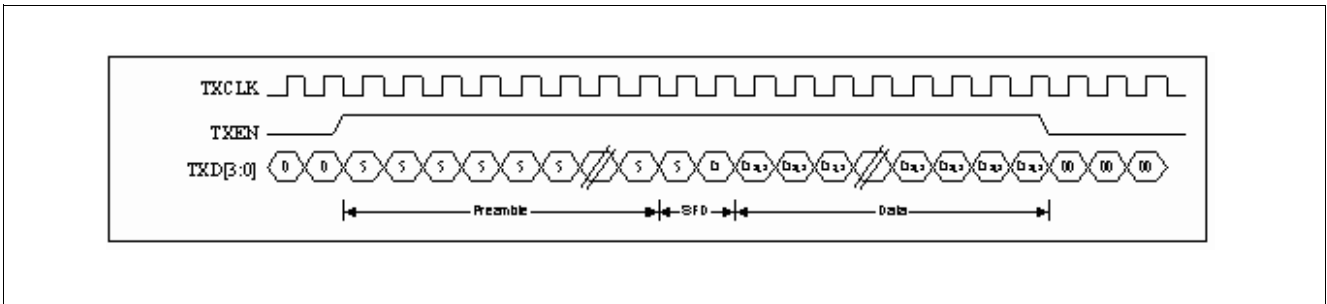


Figure 16 MII Transmission

When ADM7001/X operates in half duplex mode, either 10M or 100M, it will assert COL signal whenever it detects there is collision on the medium. **Figure 17** shows the timing diagram for MII Collision.

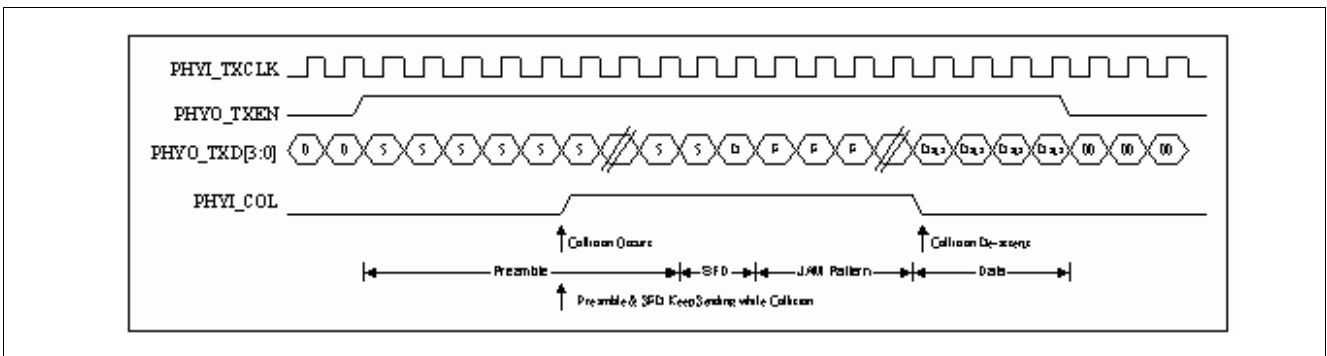


Figure 17 MII Transmit with Collision (Half Duplex Only)

3.2.9 General Purpose Serial Interface (GPSI)

Signal Diagram for MII interface is shown in **Figure 18**.

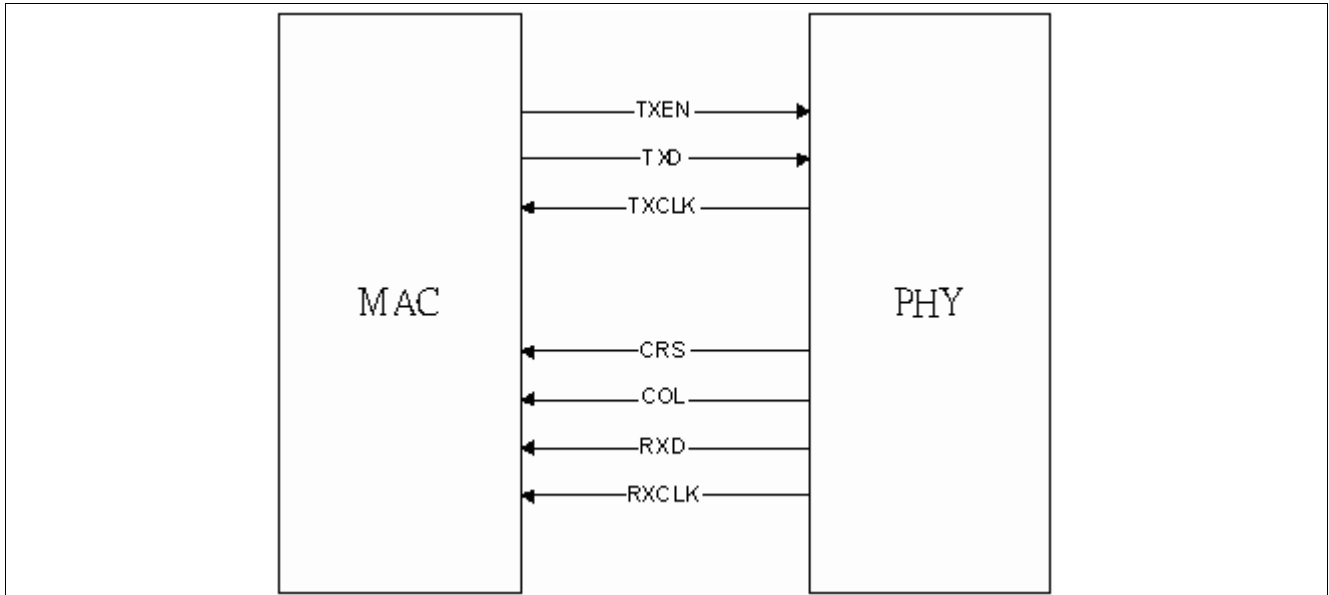


Figure 18 GPSI Signal Diagram

3.2.10 Receive Path for GPSI

Figure 19 shows the relationship among RXCLK, RXD and CRS during a receive of valid packet. Carrier sense is detected and asserted asynchronously to RXCLK by ADM7001/X. When ADM7001/X detects there is valid data, received data is presented onto RXD synchronously to RXCLK. Whenever received data is not valid anymore, CRS will be de-asserted by ADM7001/X and "0" will be put on RXD.

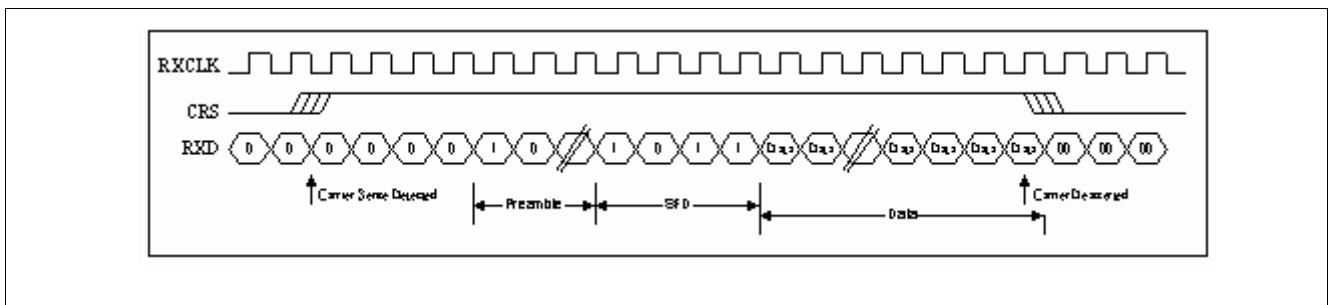
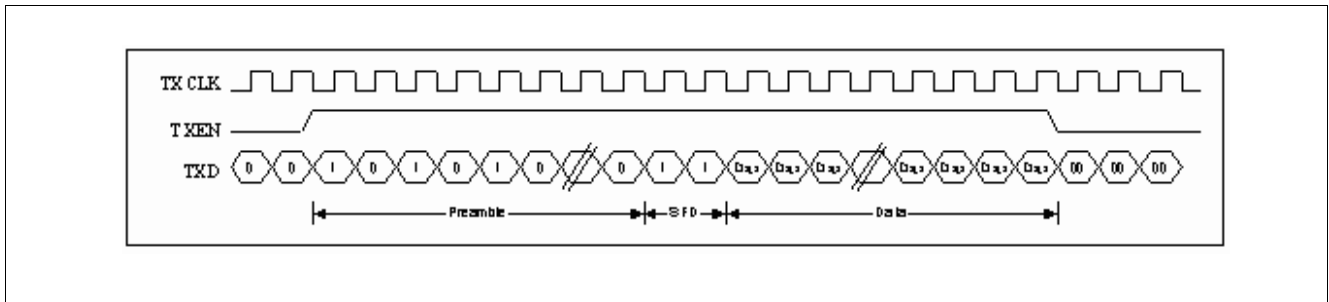


Figure 19 GPSI Receive Diagram

3.2.11 Transmit Path for GPSI

Figure 20 shows the relationship among TXCLK, TXEN and TXD during a transmit event. TXEN and TXD are synchronous to TXCLK, which is generated by MAC. TXCLK is running at 10M in 10M mode. When TXEN is asserted, it indicates that TXD contains valid data to be transmitted. When TXEN is de-asserted, value on TXD should be ignored.


Figure 20 GPSI Transmit Diagram

3.3 LED Display

Register 19 is used for different mode led display. ADM7001/X provides power on LED self test to minimize and ease the system test cost.

All LEDs will be Off during power on reset (Output value same as recommend value on LED pins). After power on reset, all internal parallel LEDs will be On for 2 seconds to ease manufacture overhead

There are three types of LED supported by ADM7001/X internally. The first is LNKACT, which represents the status of Link and Transmit/Receive Activity, the second is LDSPD, which indicates the speed status, and the last is DUPCOL, which shows pure duplex status in full duplex and duplex/collision combined status in half duplex. All these three LED can be controlled by Register 19 to change display contents.

After LED self test, [Table 14](#), [Table 15](#), [Table 16](#) show the On/Off polarity according to different recommended value setting for LDSPD, DUPCOL and LNKACT. When the recommend value is high, ADM7001/X will drive LED LOW; ADM7001/X will drive the LED HIGH when the recommend value is low, instead.

Table 14 Speed LED Display

SPEED	SPDLED
10M	0
100M	1
LINK FAIL	1

Table 15 Duplex LED Display

DUPLEX	DUPCOL	
	HALF	FULL
LINK UP	Blink (HIGH) When Collision	LOW All the Time
LINK FAIL	HIGH All the Time	HIGH All the Time

Table 16 Activity/Link LED Display

SPEED	Link/Activity	
	Link	Activity
LINK UP	LOW	Blink (HIGH) When RX/TX
LINK FAIL	HIGH All the Time	HIGH All the Time

Besides duplex, speed, link and activity status, ADM7001/X also provides cable information that can be shown on LEDs when register 19 is programmed to distance LED display (see [Table 17](#))

Table 17 Cable Distance LED Display

LNKACT	DUPCOL	LEDSPD	Cable Distance
1	1	0	0 to 40 meters
1	0	0	40 to 80 meters
0	0	0	80 to 120 meters
1	1	1	Reserved

3.4 Management Register Access

The SMI consists of two pins, management data clock (MDC) and management data input/output (MDIO). The ADM7001/X is designed to support an MDC frequency specified in the IEEE specification of up to 2.5 MHz. The MDIO line is bi-directional and may be shared by up to 32 devices.

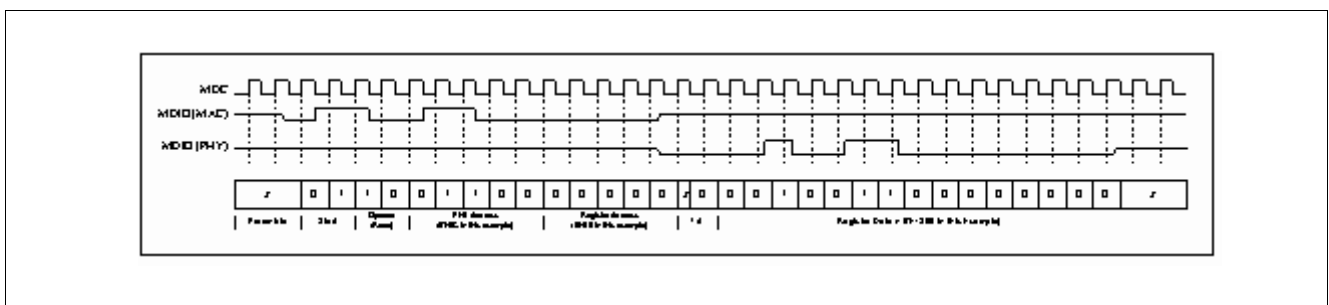
The MDIO pin requires a 1.5 K Ω pull-up which, during idle and turnaround periods, will pull MDIO to a logic one state. Each MII management data frame is 64 bits long. The first 32 bits are preamble consisting of 32 contiguous logic one bits on MDIO and 32 corresponding cycles on MDC. Following preamble is the start-of-frame field indicated by a <01> pattern. The next field signals the operation code (OP): <10> indicates read from MII management register operation, and <01> indicates write to MII management register operation. The next two fields are PHY device address and MII management register address. Both of them are 5 bits wide and the most significant bit is transferred first.

During Read operation, a 2-bit turn around (TA) time spacing between the register address field and data field is provided for the MDIO to avoid contention. Following the turnaround time, a 16-bit data stream is read from or written into the MII management registers of the ADM7001/X

3.4.1 Preamble Suppression

The ADM7001/X supports a preamble suppression mode as indicated by an 1 in bit 6 of the basic mode status register (Register 1h). If the station management entity (i.e. MAC or other management controller) determines that all PHYs in the system support preamble suppression by reading a 1 in this bit, then the station management entity needs not to generate preamble for each management transaction. The ADM7001/X requires a single initialization sequence of 32 bits of preamble following powerup/hardware reset. This requirement is generally met by pulling-up the resistor of MDIO. While the ADM7001/X will respond to management accesses without preamble, a minimum of one idle bit between management transactions is required as specified in IEEE 802.3u.

When ADM7001/X detects that there is physical address match, then it will enable Read/Write capability for external access. When neither physical address nor register address is matched, then ADM7001/X will tristate the MDIO pin.


Figure 21 SMI Read Operation

3.4.2 Reset Operation

The ADM7001/X can be reset either by hardware or software. A hardware reset is accomplished by applying a negative pulse, with duration of at least 200 ms to the RC pin of the ADM7001/X during normal operation to

guarantee internal Power On Reset Circuit is reset well. Setting the reset bit in the Basic Mode Control activates software reset

Register (bit 15, register 0_H). This bit is self-clearing and, when set, will return a value of 1 until the software reset operation has completed, please note that internal SRAM will not be reset during software reset.

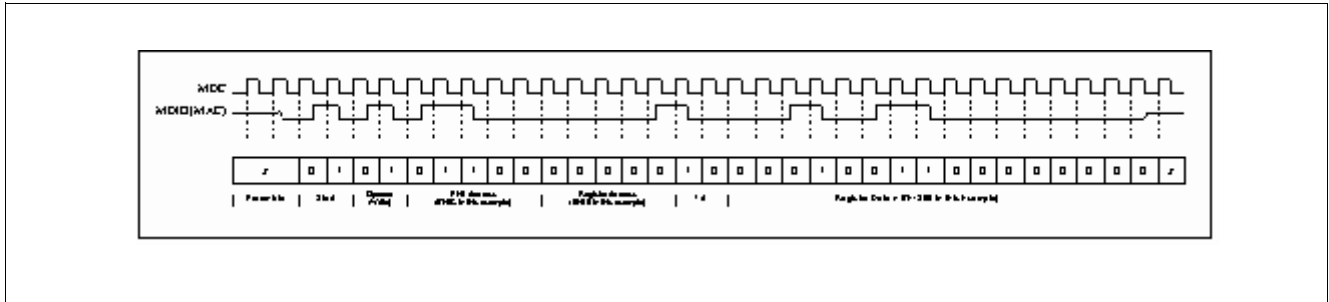


Figure 22 SMI Write Operation

Hardware reset operation samples the pins and initializes all registers to their default values. This process includes re-evaluation of all hardware configurable registers.

A software reset will reset an individual PHY and it does not latch the external pins nor reset the registers to their respective default value.

Logic levels on several I/O pins are detected during a hardware reset to determine the initial functionality of ADM7001/X. Some of these pins are used as output ports after reset operation.

Care must be taken to ensure that the configuration setup will not interfere with normal operation. Dedicated configuration pins can be tied to VCC or Ground directly. Configuration pins multiplexed with logic level output functions should be either weakly pulled up or weakly pulled down through resistors.

3.5 Power Management

An analog block is designed for carrier sense detecting. When there is no carrier sense presented on medium (cable not attached), then "SIGNAL DETECT" will not be ON. Whenever cable is attached to ADM7001/X and the voltage threshold is above +/- 50mV, then SD will be asserted HIGH to indicate that there is cable attached to ADM7001/X. All internal blocks except Management block will be disabled (reset) before SD is asserted.

When SD is asserted, internal Auto Negotiation block will be turned on and the 10M transmit driver will also be turned on for auto negotiation process. Auto negotiation will issue control signals to control 10M receive and 100M A/D block according to different state in arbitration block diagram. During auto negotiation, all digital blocks except management and link monitor blocks will be disabled to reduce power consumption.

Whenever operating speed is determined (Either auto negotiation is On or Off), the non-active speed relative circuit will be disabled all the time to save more power. For example, when corresponding port is operating on 10M, then 100M relative blocks will be disabled and 10M relative blocks will be disabled whenever corresponding port is in 100M mode. Auto negotiation block will be reset when SD signal goes from high to low. See [Figure 23](#) for the state diagram for this algorithm.

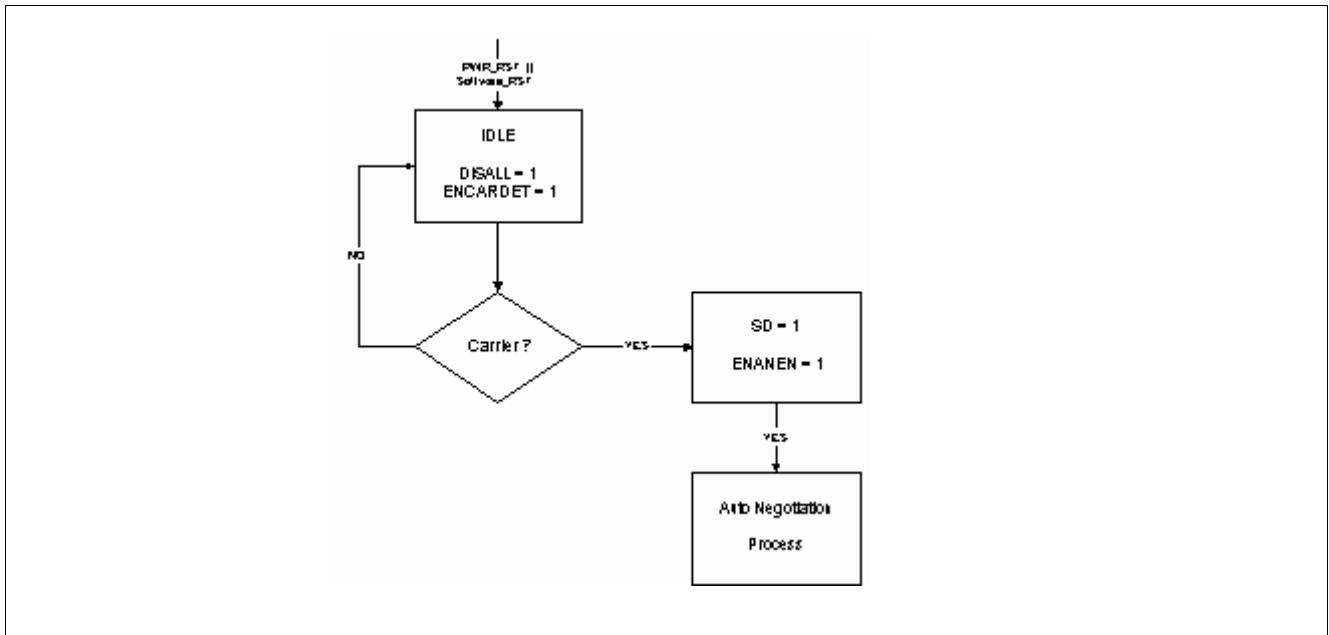


Figure 23 Medium Detect Power Management Flow Chart

Another way to reduce instant power is to separate the LED display period. All 4 LEDs will be divided into 4 time frame and each time frame occupies 1 us. One and only one LED will be driven at each time frame to reduce instant current consumed from LED.

3.6 Voltage Regulator

ADM7001/X requires two different levels, 3.3 V and 2.5 V, of voltage supply to provide the power to different parts of circuitry inside the chip. ADM7001/X has a build-in voltage regulator circuitry to generate the 2.5 V voltage (VCC25OUT) from 3.3 V power source (VCC3IN). External Application Circuitry is shown in [Figure 24](#).

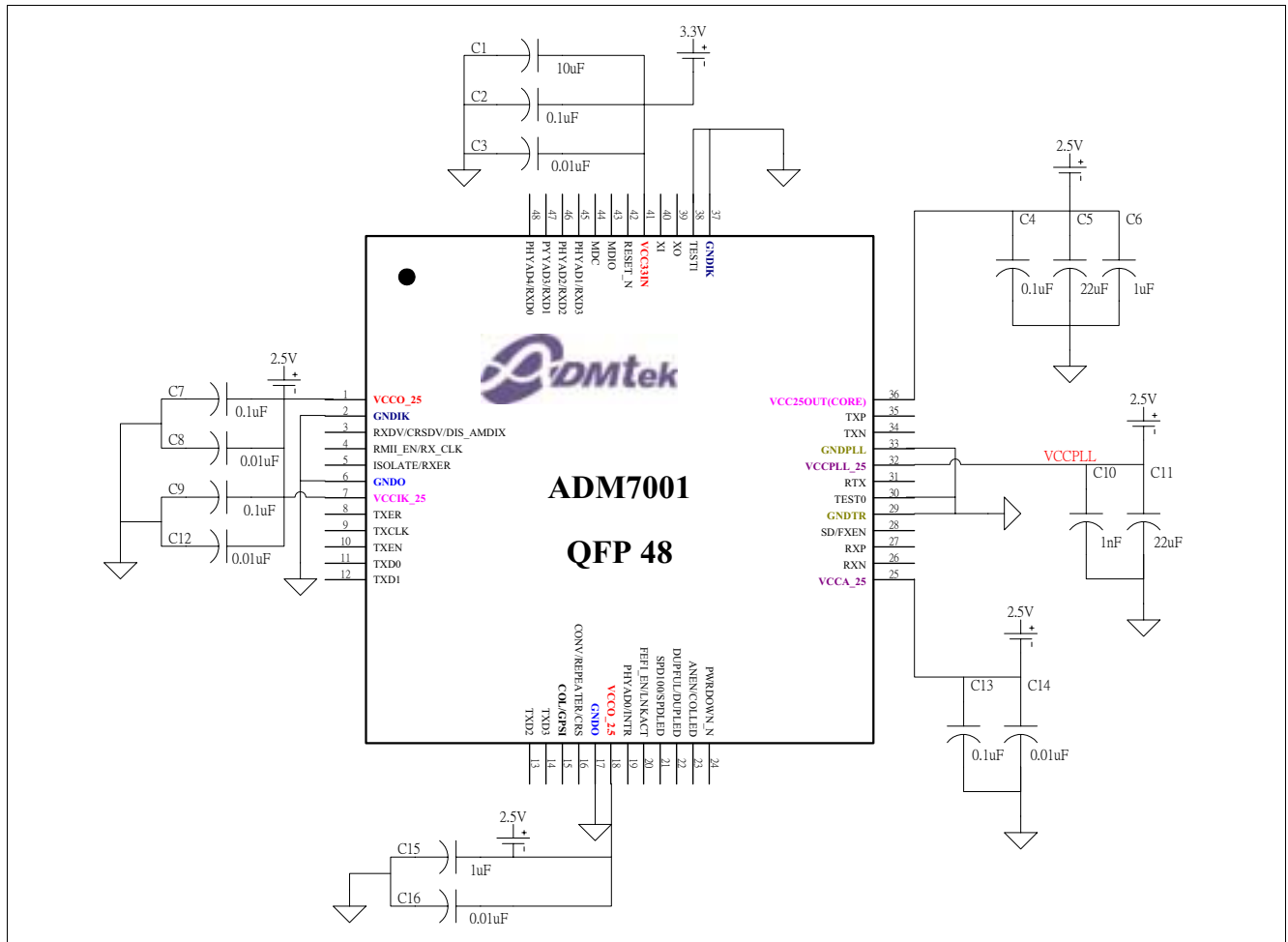


Figure 24 Power and Ground Filtering

4 Registers Description

Table 18 Registers Address Space

Module	Base Address	End Address	Note
PHY	00 _H	1F _H	

Table 19 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
CR	Control Register	00 _H	50
SR	Status Register	01 _H	52
PHY_IR0	PHY Identifier Register 0	02 _H	55
PHY_IR1	PHY Identifier Register 1	03 _H	55
Advertisement	Auto Negotiation Advertisement Register	04 _H	56
ANLPA	Auto Negotiation Link Partner Ability	05 _H	57
ANER	Auto Negotiation Expansion Register	06 _H	58
Res0	Reserved 0	07 _H	59
GPCR	Generic PHY Control/Configuration Register	10 _H	60
P10_MCR	PHY 10M Module Configuration Register	11 _H	62
P100_MCR	PHY 100M Module Control Register	12 _H	64
LCR	LED Configuration Register	13 _H	65
IER	Interrupt Enable Register	14 _H	67
PGSR	PHY Generic Status Register	16 _H	68
PSSR	PHY Specific Status Register	17 _H	69
PRVSR	PHY Recommend Value Status Register	18 _H	70
ISR	Interrupt Status Register	19 _H	71
RECR	Receive Error Counter Register	1D _H	72
CIR	Chip ID Register	1F _H	73

The register is addressed wordwise.

Table 20 Registers Access Types

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
read/write	rw	Register is used as input for the HW	Register is read and writable by SW
read	r	Register is written by HW (register between input and output -> one cycle delay)	Value written by software is ignored by hardware; that is, software may write any value to this field without affecting hardware behavior (= Target for development.)
write	w		Register is writable by SW
read/write hardware affected	rwh	Register can be modified by HW	Register can be modified by HW, but the priority SW versus HW has to be specified
	rwv		

Registers Description
Table 20 Registers Access Types (cont'd)

Mode	Symbol	Description Hardware (HW)	Description Software (SW)
Read only	ro	Register is set by HW (register between input and output -> one cycle delay)	SW can only read this register
Read virtual	rv	Physically, there is no new register, the input of the signal is connected directly to the address multiplexer.	SW can only read this register
Latch high, self clearing	lhsc	Latch high signal at high level, clear on read	SW can read the register
Latch low, self clearing	llsc	Latch high signal at low-level, clear on read	SW can read the register
Latch high, mask clearing	lhmk	Latch high signal at high level, register cleared with written mask	SW can read the register, with write mask the register can be cleared (1 clears)
Latch low, mask clearing	llmk	Latch high signal at low-level, register cleared on read	SW can read the register, with write mask the register can be cleared (1 clears)
Interrupt high, self clearing	ihsc	Differentiate the input signal (low->high) register cleared on read	SW can read the register
Interrupt low, self clearing	ilsc	Differentiate the input signal (high->low) register cleared on read	SW can read the register
Interrupt high, mask clearing	ihmk	Differentiate the input signal (high->low) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt low, mask clearing	ilmk	Differentiate the input signal (low->high) register cleared with written mask	SW can read the register, with write mask the register can be cleared
Interrupt enable register	ien	Enables the interrupt source for interrupt generation	SW can read and write this register
latch_on_reset	lor	rw register, value is latched after first clock cycle after reset	Register is read and writable by SW
Read/write self clearing	rwsc	Register is used as input for the hw, the register will be cleared due to a HW mechanism.	Writing to the register generates a strobe signal for the HW (1 pdi clock cycle) Register is read and writable by SW.

Table 21 Registers Clock Domains

Clock Short Name	Description

4.1 Register Description

Registers Description

Field	Bits	Type	Description
PDN	11	rw	Power Down Enable Ored result with PI_PWRDN pin. Setting this bit high or asserting the PI_PWRDN puts the PHY841F into power down mode. During the power down mode, TXP/TXN and all LED outputs are tristated and the MII/RMII interfaces are isolated. 0 _B PDN_0 , Normal Operation 1 _B PDN_1 , Power Down
ISO	10	rw	Isolate PHY841F from Network Setting this control bit isolates the part from the RMII/MII, with the exception of the serial management interface. When this bit is asserted, the PHY841F does not respond to TXD, TXEN and TXER inputs, and it presents a high impedance on its TXC, RXC, CRSDV, RXER, RXD, COL and CRS outputs. 0 _B ISO_0 , Normal Operation 1 _B ISO_1 , Isolate PHY from MII/RMII
RAN	9	rwsc	Restart Auto Negotiation ANEN_RST. Setting this bit while auto negotiation is enabled forces a new auto negotiation process to start. This bit is self-clearing and returns to 0 after the auto negotiation process has commenced. 0 _B RAN_0 , Normal Operation 1 _B RAN_1 , Restart Auto Negotiation Process
DPLX	8	rw	Duplex Mode If auto negotiation is disabled, this bit determines the duplex mode for the link. 0 _B DPLX_0 , Half Duplex mode 1 _B DPLX_1 , Full Duplex mode
CT	7	rw	Collision Test When set, this bit will cause the COL signal of MII interface to be asserted in response to the assertion of TXEN. 0 _B CT_0 , Disable COL signal test 1 _B CT_1 , Enable COL signal test
SSM	6	ro	Speed Selection MSB SPEED_MSB. Set to 0 all the time indicate that the PHY841F does not support 1000 Mbit/s function.
Res	5:0	ro	Reserved Not Applicable

Status Register

SR		Offset		Reset Value											
Status Register		01 _H		7849 _H											
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T4	TXF	TXH	TF	TH	T2		Res		SUPR	AN_C	RFD	ANEG	LINK	JAB	XTND
ro	ro	ro	ro	ro	ro		ro		ro	ro	ro	ro	ro, ll	ro, lh	ro

Registers Description

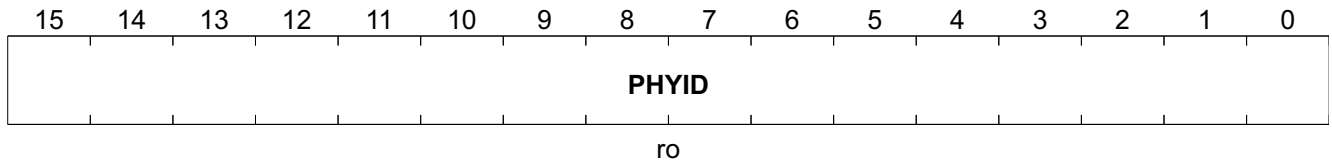
Field	Bits	Type	Description
T4	15	ro	100Base-T4 Capable Set to 0 all the time to indicate that the PHY841F does not support 100Base-T4.
TXF	14		100Base-X Full Duplex Capable Set to 1 all the time to indicate that the PHY841F does support Full Duplex mode.
TXH	13		100Base-X Half Duplex Capable Set to 1 all the time to indicate that the PHY841F does support Half Duplex mode
TF	12		10M Full Duplex Capable TP: Set to 1 all the time to indicate that the PHY841F does support 10M Full Duplex mode. FX: Set to 0 all the time to indicate that the PHY841F does not support 10M Full Duplex mode
TH	11		10M Half Duplex Capable TP: Set to 1 all the time to indicate that the PHY841F does support 10M Half Duplex mode. FX: Set to 0 all the time to indicate that the PHY841F does not support 10M Half Duplex mode
T2	10		100Base-T2 Capable Set to 0 all the time to indicate that the PHY841F does not support 100Base-T2.
Res	9:7		Reserved Not Applicable
SUPR	6		MF Preamble Suppression Capable This bit is hardwired to 1 indicating that the PHY841F accepts management frame without preamble. Minimum 32 preamble bits are required following power-on or hardware reset. One idle bit is required between any two management transactions as per IEEE 802.3u specification.
AN_C	5		Auto Negotiation Complete If auto negotiation is enabled, this bit indicates whether the auto negotiation process has been completed or not. Set to 0 all the time when Fiber Mode is selected. 0 _B AN_C_0 , Auto Negotiation process not completed 1 _B AN_C_1 , Auto Negotiation process completed

Registers Description

Field	Bits	Type	Description
RFD	4	ro	Remote Fault Detect This bit is latched to 1 if the RF bit in the auto negotiation link partner ability register (bit 13, register address 05h) is set or the receive channel meets the far end fault indication function criteria. It is unlatched when this register is read. 0 _B RFD_0 , Remote Fault not detected 1 _B RFD_1 , Remote Fault detected
ANEG	3		Auto Negotiation Ability TP: This bit is set to 1 all the time, indicating that PHY841F is capable of auto negotiation. FX: This bit is set to 0 all the time, indicating that PHY841F is not capable of auto negotiation in Fiber Mode. 0 _B ANEG_0 , Not capable of auto negotiation 1 _B ANEG_1 , Capable of auto negotiation
LINK	2	ro, lhsc	Link Status This bit reflects the current state of the link -test-fail state machine. Loss of a valid link causes a 0 latched into this bit. It remains 0 until this register is read by the serial management interface. Whenever Linkup, this bit should be read twice to get link up status 0 _B LINK_0 , Link is down 1 _B LINK_1 , Link is up
JAB	1	ro, lhsc	Jabber Detect 0 _B JAB_0 , Jabber condition not detected 1 _B JAB_1 , Jabber condition detected
XTND	0	ro	Extended Capability This bit defaults to 1, indicating that the PHY841F implements extended registers. 0 _B XTND_0 , No extended register set 1 _B XTND_1 , Extended register set

PHY Identifier

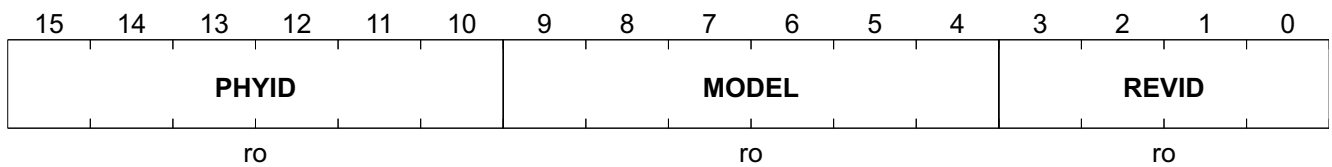
PHY_IR0 **Offset**
PHY Identifier Register 0 **02_H** **Reset Value**
002E_H



Field	Bits	Type	Description
PHYID	15:0	ro	PHY-ID IEEE Address

PHY Identifier Register 1

PHY_IR1 **Offset**
PHY Identifier Register 1 **03_H** **Reset Value**
CC62_H



Field	Bits	Type	Description
PHYID	15:10	ro	PHY-ID 15:0 IEEE Address/Model No./Rev. No.
MODEL	9:4		MODEL 5:0 ADMTEK PHY Revision ID.
REVID	3:0		REV-ID 3:0 ADMTEK PHY Revision ID.

Advertisement

Advertisement	Offset	Reset Value
Auto Negotiation Advertisement Register	04_H	01E1_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NP	Res	RF	Res	APD	PSE	T4	TXF	TXD	TF	TD			Sel		
rw	ro	rw	ro	rw	rw	ro	rw	rw	rw	rw			ro		

Field	Bits	Type	Description
NP	15	rw	Next Page This bit is defaults to 1, indicating that PHY841F is next page capable.
Res	14	ro	Reserved Not Applicable
RF	13	rw	Remote Fault This bit is written by serial management interface for the purpose of communicating the remote fault condition to the auto negotiation link partner. 0 _B NRFD , No remote fault has been detected 1 _B RFD , Remote Fault has been detected
Res	12	ro	Reserved Not Applicable
APD	11	rw	Asymmetric Pause Direction Bit[11:10] Capability 00 _B NP , No Pause 01 _B SP , Symmetric PAUSE 10 _B AP , Asymmetric PAUSE toward Link Partner 11 _B BSP , Both Symmetric PAUSE and Asymmetric PAUSE toward local device
PSE	10	rw	Pause Operation for Full Duplex Value on PAUREC will be stored in this bit during power on reset.
T4	9	ro	Technology Ability for 100Base-T4 Defaults to 0.

Registers Description

Field	Bits	Type	Description
TXF	8	rw	100Base-TX Full Duplex 0_B NCFDO, Not capable of 100M Full duplex operation 1_B CFDO, Capable of 100M Full duplex operation
TXD	7		100Base-TX Half Duplex 0_B TXD_0, Not capable of 100M operation 1_B TXD_1, Capable of 100M operation
TF	6		10Base-T Full Duplex 0_B TF_0, Not capable of 10M full duplex operation 1_B TF_1, Capable of 10M Full Duplex operation
TD	5		10Base-T Half Duplex 0_B TD_0, Not capable of 10M operation 1_B TD_1, Capable of 10M operation
Sel	4:0	ro	Selector Field These 5 bits are hardwired to 00001_B , indicating that the PHY841F supports IEEE 802.3 CSMA/CD.

Auto Negotiation Link Partner Ability

ANLPA **Offset**
Auto Negotiation Link Partner Ability **05_H** **Reset Value**
01E1_H

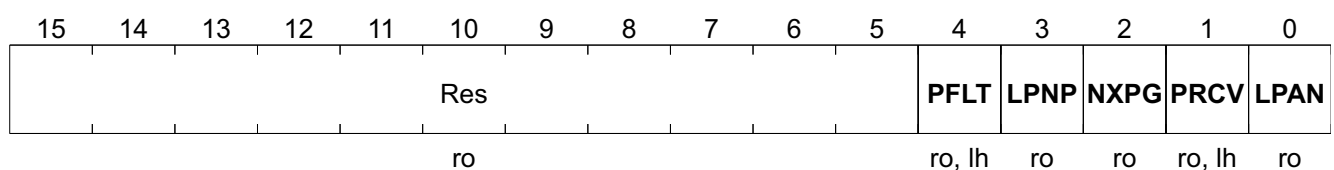
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NPG	ACK	RF	Res	LPAP	LPP	LPTA	TXF	TXD	TF	TD			Sel		
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro			ro		

Registers Description

Field	Bits	Type	Description
NPG	15	ro	Next Page 0 _B NPG_0 , Not capable of next page function 1 _B NPG_1 , Capable of next page function
ACK	14		Acknowledge 0 _B ACK_0 , Not acknowledged 1 _B ACK_1 , Link Partner acknowledges reception of the ability data word
RF	13		Remote Fault 0 _B RF_0 , No remote fault has been detected 1 _B RF_1 , Remote Fault has been detected
Res	12		Reserved Not Applicable
LPAP	11		Link Partner Asymmetric Pause Direction
LPP	10		Link Partner Pause Capability Value on PAUREC will be stored in this bit during power on reset.
LPTA	9		Link Partner Technology Ability for 100Base-T4 Defaults to 0.
TXF	8		100Base-TX Full Duplex 0 _B TXF_0 , Not capable of 100M Full duplex operation 1 _B TXF_1 , Capable of 100M Full duplex operation
TXD	7		100Base-TX Half Duplex 1 _B TXD_1 , Capable of 100M operation 0 _B TXD_2 , Not capable of 100M operation
TF	6		10Base-T Full Duplex 1 _B TF_1 , Capable of 10M Full Duplex operation 0 _B TF_0 , Not capable of 10M full duplex operation
TD	5		10Base-T Half Duplex 1 _B TD_1 , Capable of 10M operation 0 _B TD_0 , Not capable of 10M operation
Sel	4:0		Encoding Definitions

Auto Negotiation Expansion Register

ANER	Offset	Reset Value
Auto Negotiation Expansion Register	06_H	0000_H

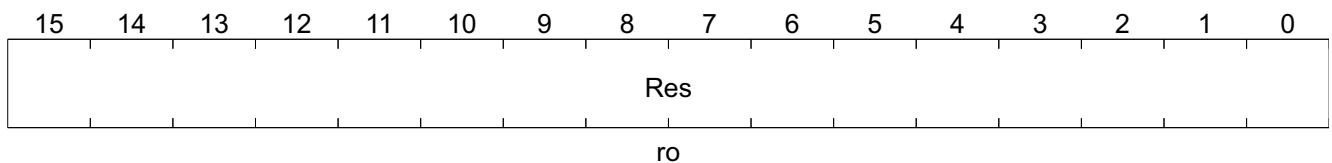


Registers Description

Field	Bits	Type	Description
Res	15:5	ro	Reserved Not Applicable
PFLT	4	ro, lhsc	Parallel Detection Fault 0 _B PFLT_0 , No Fault Detect 1 _B PFLT_1 , Fault has been detected
LPNP	3	ro	Link Partner Next Page Able 0 _B LPNP_0 , Link Partner is not next page capable 1 _B LPNP_1 , Link Partner is next page capable
NXPG	2		Next Page Able 1 _B NXPG_1 , Next page Enable. 0 _B NXPG_0 , Next page Disable
PRCV	1	ro, lhsc	Page Received 0 _B PRCV_0 , No new page has been received 1 _B PRCV_1 , A new page has been received
LPAN	0	ro	Link Partner Auto Negotiation Able 0 _B LPAN_0 , Link Partner is not auto negotiable 1 _B LPAN_1 , Link Partner is auto negotiable

Reserved 0

Res0	Offset	Reset Value
Reserved 0	07 _H	Reserved _H



Field	Bits	Type	Description
Res	15:0	ro	Reserved Not Applicable

Table 22 Reserved Registers

Register Short Name	Register Long Name	Offset Address
Res1	Reserved 1	08 _H
Res2	Reserved 2	09 _H
Res3	Reserved 3	0A _H
Res4	Reserved 4	0B _H
Res5	Reserved 5	0C _H
Res6	Reserved 6	0D _H

Registers Description

Field	Bits	Type	Description
Conv	8	rw	Converter mode (only valid in rmii mode) 0 _B Conv_0 , Normal Mode 1 _B Conv_1 , converter mode
Res	7:5	ro	Reserved Not Applicable
XOVEN	4	rw	Cross Over Auto Detect Enable 0 _B XOVEN_0 , Disable. 1 _B XOVEN_1 , Enable.
Res	3:2	rw	ADMtek reserved bits. Writing value other than 0 to these two bits may cause abnormal operation.
En8	1	rw	Enable Register 8 to Store Next Page Information. 0 _B En8_0 , Store Next Page in Register 5. 1 _B En8_1 , Store Next Page in Register 8
DPMG	0	rw	Disable Power Management Feature 0 _B DPMG_0 , Enable. Enable Medium Detect Function. 1 _B DPMG_1 , Disable. Medium_On is high all the time.

Registers Description

Field	Bits	Type	Description
SMS	14	rw	10BASE-T Serial Mode Select. Only available when AD2106 works in 10M mode. 0 _B SMS_0 , 10M MII or RMI mode (According to RMII_EN) 1 _B SMS_1 , 10M Serial Mode (Seven Wire Mode)
Res	13		ADMtek reserved bits. Writing value other than 1 to this bit may cause abnormal operation.
Res	12:11		ADMtek reserved bits. Writing value other than 0 to these two bits may cause abnormal operation.
ITCE	10		Polarity Interval Timer Check Enable. 0 _B ITCE_0 , Disable 1 _B ITCE_1 , Enable
Res	9		ADMtek reserved bits. Writing value other than 1 to this bit may cause abnormal operation.
Res	8:6		ADMtek reserved bits. Writing value other than 5 to these three bits may cause abnormal operation.
Res	5		ADMtek reserved bits. Writing value other than 1 to this bit may cause abnormal operation.
APD	4		Auto Polarity Disable 0 _B APD_0 , Normal 1 _B APD_1 , Disable
RJM	3		Enable Receive Jabber Monitor 0 _B RJM_0 , Disable 1 _B RJM_1 , Enable
TJD	2		Disable Transmit Jabber 0 _B TJD_0 , Enable Transmit Jabber Function 1 _B TJD_1 , Disable Transmit Jabber Function
NTH	1		Normal Threshold 0 _B NTH_0 , Lower 10BASE-T Receive threshold 1 _B NTH_1 , Normal 10BASE-T Receive threshold
FRL	0		Force 10M Receive Good Link. 0 _B FRL_0 , Normal Operation 1 _B FRL_1 , Force Good Link

PHY 100M Module Control Register

P100_MCR	Offset	Reset Value
PHY 100M Module Control Register	12_H	0022_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res			Res		Res		FxSel	Res		SCR	FEFI	CLE	IAC	Res	
ro			rw		rw		rw	rw		rw	rw	ro	rw	rw	

Field	Bits	Type	Description
Res	15:12	ro	Reserved Not Applicable
Res	11:10	rw	ADMtek reserved bits. Writing value other than 0 to these two bits may cause abnormal operation.
Res	9:8		ADMtek reserved bits. Writing value other than 0 to these two bits may cause abnormal operation.
FxSel	7		Fiber Select. 0 _B SelfX_0 , TP Mode 1 _B SelfX_1 , Fiber Mode
Res	6:5		ADMtek reserved bits. Writing value other than 0 to these two bits may cause abnormal operation.
SCR	4		Disable Scrambler When set to fiber mode, this bit will be forced to 1 automatically. Write 0 to this bit in Fiber Mode has no effect. 0 _B SCR_0 , Enable 1 _B SCR_1 , Disable
FEFI	3		Enable FEFI 0 _B FEFI_0 , Disable 1 _B FEFI_1 , Enable
CLE	2	ro	Disable cable length led indication When this bit is set to 0, SPDLED, COLLED and LNKACTLED are used to represent twisted pair cable length. See SPDLED description for more detail 0 _B CLE_0 , Enable cable length led 1 _B CLE_1 , Disable cable length led
IAC	1	rw	Interrupt active value control 0 _B IAC_0 , Active low 1 _B IAC_1 , Active high
Res	0		ADMtek reserved bits. Writing value other than 0 to this bit may cause abnormal operation.

Registers Description

Field	Bits	Type	Description
SPDCTRL	3:0	ro	Speed LED Control 0000 _B , Collision 0001 _B , All Errors 0010 _B , Duplex 0011 _B , Duplex/Collision 0100 _B , Speed 0101 _B , Link 0110 _B , Transmit Activity 0111 _B , Receive Activity 1000 _B , TX/RX Activity 1001 _B , Link/Receive Activity 1010 _B , Link and TX/RX Activity 1011 _B , 100M False Carrier Error/10M Receive Jabber 1100 _B , 100M Error End of Stream/10M Transmit Jabber 1101 _B , Reserved 1110 _B , Distance (See LED Description for more detail)

Interrupt Enable Register

IER	Offset	Reset Value
Interrupt Enable Register	14_H	03FF_H

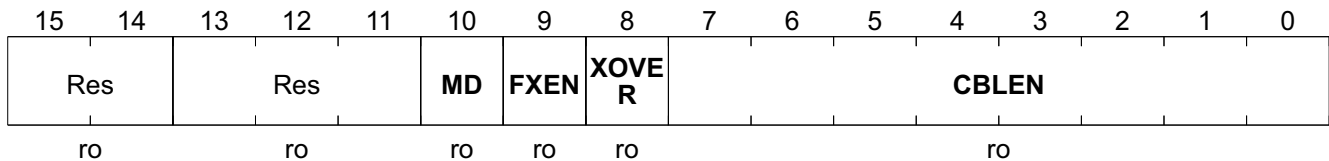
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res						XCHG	SCIE	DCIE	PRIE	LSCE	SEIE	FCAR	TJIE	RJIE	EESE
ro						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
Res	15:10	ro	Reserved Not Applicable
XCHG	9	rw	Cross Over mode Changed Interrupt Enable 0 _B XCHG_0, Interrupt Disable 1 _B XCHG_1, Interrupt Enable
SCIE	8		Speed Changed Interrupt Enable 0 _B SCIE_0, Interrupt Disable 1 _B SCIE_1, Interrupt Enable
DCIE	7		Duplex Changed Interrupt Enable 0 _B DCIE_0, Interrupt Disable 1 _B DCIE_1, Interrupt Enable
PRIE	6		Page Received Interrupt Enable 0 _B PRIE_0, Interrupt Disable 1 _B PRIE_1, Interrupt Enable
LSCE	5		Link Status Changed Interrupt Enable 0 _B LSCE_0, Interrupt Disable 1 _B LSCE_1, Interrupt Enable
SEIE	4		Symbol Error Interrupt Enable 0 _B SEIE_0, Interrupt Disable 1 _B SEIE_1, Interrupt Enable
FCAR	3		False Carrier Interrupt Enable 0 _B FCAR_0, Interrupt Disable 1 _B FCAR_1, Interrupt Enable
TJIE	2		Transmit Jabber Interrupt Enable 0 _B TJIE_0, Interrupt Disable 1 _B TJIE_1, Interrupt Enable
RJIE	1		Receive Jabber Interrupt Enable 0 _B RJIE_0, Interrupt Disable 1 _B RJIE_1, Interrupt Enable
EESE	0		Error End of Stream Enable 0 _B EESE_0, Interrupt Disable 1 _B EESE_1, Interrupt Enable

PHY Generic Status Register

Note: PHY Status Registers start from 22 to 28 (29 to 30 reserves for further use)

PGSR	Offset	Reset Value
PHY Generic Status Register	16_H	0000_H



Field	Bits	Type	Description
Res	15:14	ro	Reserved Not Applicable
Res	13:11		Reserved Not Applicable
MD	10		Medium Detect Real Time Status for Medium Detect Signal. 0 _B MD_0 , Medium_Detect Fail 1 _B MD_1 , Medium_Detect Pass
FXEN	9		Fiber Enable Only Changed when PHY Reset. OR'ed result of PI_SELFX and 17.9 (SELFX) 0 _B FXEN_0 , TX mode 1 _B FXEN_1 , FX mode
XOVER	8		Cross Over Status 0 _B XOVS_0 , MDI mode 1 _B XOVS_1 , MDIX mode
CBLEN	7:0		Cable Length. Only valid for 100M MSB is IC0 1a _H , 40 meters 22 _H , 60 meters 94 _H , 80 meters 9a _H , 100 meters a2 _H , 120 meters ab _H , 140 meters

PHY Specific Status Register

PSSR	Offset	Reset Value
PHY Specific Status Register	17_H	0060_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		Res		JRX	JTX	POL	POUT	PIN	DUP	SPD	LINK	RPAU	RDUP	RSPD	RANV
		ro		ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro

Field	Bits	Type	Description
Res	15:12	ro	Reserved Not Applicable
JRX	11		Real Time 10M Receive Jabber Status 0 _B JRX_0, No jabber 1 _B JRX_1, Jabber
JTX	10		Real Time 10M Transmit Jabber Status 0 _B JTX_0, No Jabber 1 _B JTX_1, Jabber
POL	9		Polarity Only available in 10M. 0 _B POL_0, Normal Polarity 1 _B POL_1, Polarity Reversed
POUT	8		Pause Out Capability Disabled when Half Duplex. 0 _B POUT_0, Lack of Pause Out capability 1 _B POUT_1, Has Pause Out capability
PIN	7		Pause In Capability Disabled when Half Duplex. 0 _B PIN_0, Has Pause In capability 1 _B PIN_1, Lack of Pause In capability
DUP	6		Operating Duplex 0 _B DUP_0, Half Duplex 1 _B DUP_1, Full Duplex
SPD	5		Operating Speed 0 _B SPD_0, 10Mb/s 1 _B SPD_1, 100Mb/s
LINK	4		Real Time Link Status 0 _B LINK_0, Link Down 1 _B LINK_1, Link Up
RPAU	3		Pause Recommend Value Only Changed when PHY Reset. This bit is disabled automatically when RDUP is 0. 0 _B RPAU_0, Pause Disable 1 _B RPAU_1, Pause Enable

Registers Description

Field	Bits	Type	Description
RDUP	2	ro	Duplex Recommended Value Only Changed when PHY Reset. 0 _B RDUP_0 , Half Duplex 1 _B RDUP_1 , Full Duplex
RSPD	1		Speed Recommend Value Only Changed when PHY Reset. 0 _B RSPD_0 , 10M 1 _B RSPD_1 , 100M
RANV	0		Recommended Auto Negotiation Value Only Changed when PHY Reset.

PHY Recommend Value Status Register

PRVSR	Offset	Reset Value
PHY Recommend Value Status Register	18_H	0000_H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res	RANV	FSEL	RSPD	RDUP	PREC	FEFD	XOVR	XOVS	RSII	RM					
ro	ro	ro	ro	ro	ro	ro	ro	ro	ro	ro					ro

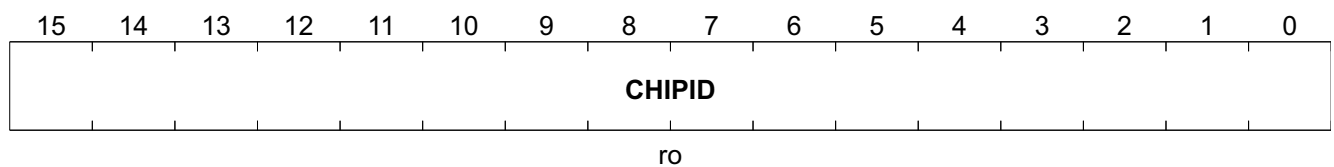
Field	Bits	Type	Description
Res	15	ro	Reserved Not Applicable
RANV	14		Auto Negotiation Recommend Value
FSEL	13		Fiber Select Recommend Value
RSPD	12		Speed Recommend Value 0 _B RSPD_1 , 10M 1 _B RSPD_0 , 100M
RDUP	11		Duplex Recommend Value 0 _B RDUP_0 , Half Duplex 1 _B RDUP_1 , Full Duplex
PREC	10		Pause Capability Recommend Value 0 _B PREC_0 , Pause Disable 1 _B PREC_1 , Pause Enable
FEFD	9		Far End Fault Disable 0 _B FEFD_0 , Enable 1 _B FEFD_1 , Disable
XOVR	8		Cross Over Capability Recommend Value 0 _B XOVR_0 , Disable 1 _B XOVR_1 , Enable
XOVS	7		Cross Over Status 0 _B XOVS_0 , Non-Cross Over 1 _B XOVS_1 , Cross Over

Registers Description

Field	Bits	Type	Description
ERB	15:0	ro	Error Counter Includes. 1 _H 100MFC , 100M False Carrier 2 _H 100MSE , 100M Symbol Error 3 _H 10MTJ , 10M Transmit Jabber 4 _H 10MRJ , 10M Receive Jabber 5 _H ESS , Error Start of Stream 6 _H EES , Error End of Stream

Chip ID Register

CIR	Offset	Reset Value
Chip ID Register	1F _H	8125 _H



Field	Bits	Type	Description
CHIPID	15:0	ro	CHIPID 15:0

5 Electrical Characteristics

5.1 DC Characterization

5.1.1 Absolute Maximum Rating

Table 23 Absolute Maximum Rating

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3 V Power Supply	V_{CC33}	3.0	–	3.6	V	–
2.5 V Power Supply	V_{CC25}	2.25	–	2.75	V	–
Input Voltage	V_{IN}	-0.3	–	$V_{CC33} + 0.3$	V	–
Output Voltage	V_{OUT}	-0.25	–	$V_{CC25} + 0.25$	V	–
Storage Temperature	T_{STG}	-55	–	155	°C	–
Power Consumption	P_C	–	–	0.5	W	–
ESD Rating	V_{ESD}	–	–	2000	V	–

5.1.2 Recommended Operating Conditions

Table 24 Recommended Operating Conditions

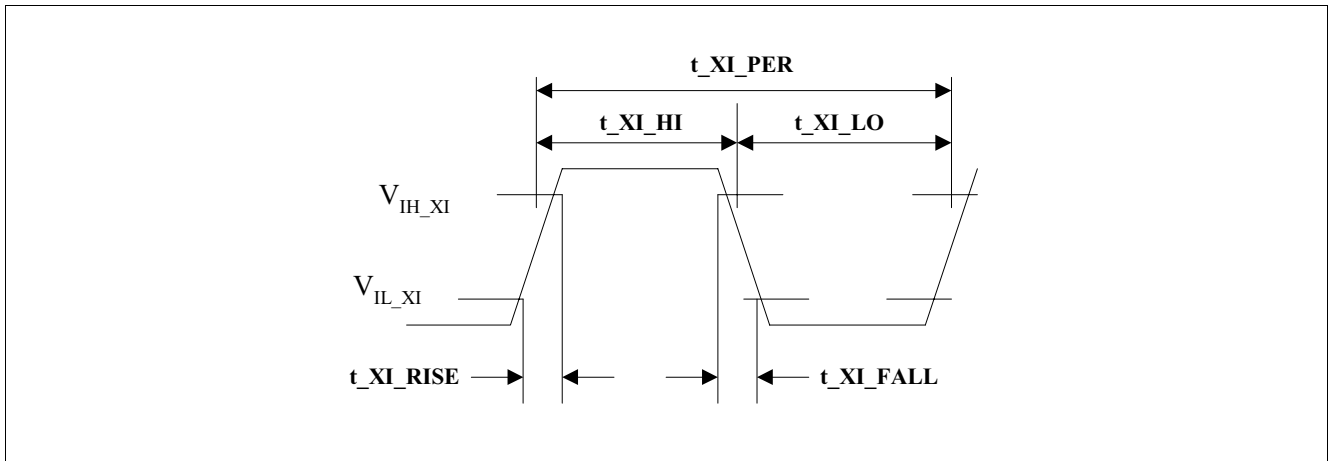
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Power Supply	V_{CC33}	3.135	3.3	3.465	V	–
Input Voltage	V_{IN}	0	–	V_{cc33}	V	–
Junction Operating Temperature	T_j	0	25	115	°C	–

5.1.2.1 DC Characteristics for 2.5 V Operation

Under $V_{cc} = 3.0\text{ V} \sim 3.6\text{ V}$, $T_j = 0^\circ\text{C} \sim 115^\circ\text{C}$

Table 25 DC Characteristics for 2.5 V Operation

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input Low Voltage	V_{IL}	–	–	$0.3 * V_{cc}$	V	CMOS
Input High Voltage	V_{IH}	$0.7 * V_{cc}$	v	–	V	CMOS
Output Low Voltage	V_{OL}	–	–	0.4	V	CMOS
Output High Voltage	V_{OH}	2.0	–	–	V	CMOS
Input Pull-up/down Resistance	R_I	–	75	–	K Ω	$V_{IL} = 0\text{ V}$ or $V_{IH} = V_{cc33}$

5.2 AC Characteristics
5.2.1 XI/OSCI (Crystal/Oscillator) Timing (In MII Mode)

Figure 25 Crystal/Oscillator Timing
Table 26 Crystal/Oscillator Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
XI/OSCI Clock Period ¹⁾	t_{XI_PER}	40.0 - 50 ppm	40.0	40.0 + 50 ppm	ns	–
XI/OSCI Clock High	t_{XI_HI}	14	20.0	–	ns	–
XI/OSCI Clock Low	t_{XI_LO}	14	20.0	–	ns	–
XI/OSCI Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	t_{XI_RISE}	–	–	4	ns	–
XI/OSCI Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	t_{XI_FALL}	–	–	4	ns	–

1) Clock period less than 40ns - 50ppm or greater than 40ns + 50ppm may introduce peer receive CRC due to insufficient receive FIFO depth. Check peer receive FIFO description to confirm.

5.3 RMI Timing

5.3.1 REFCLK Input Timing (XI in RMI Mode)

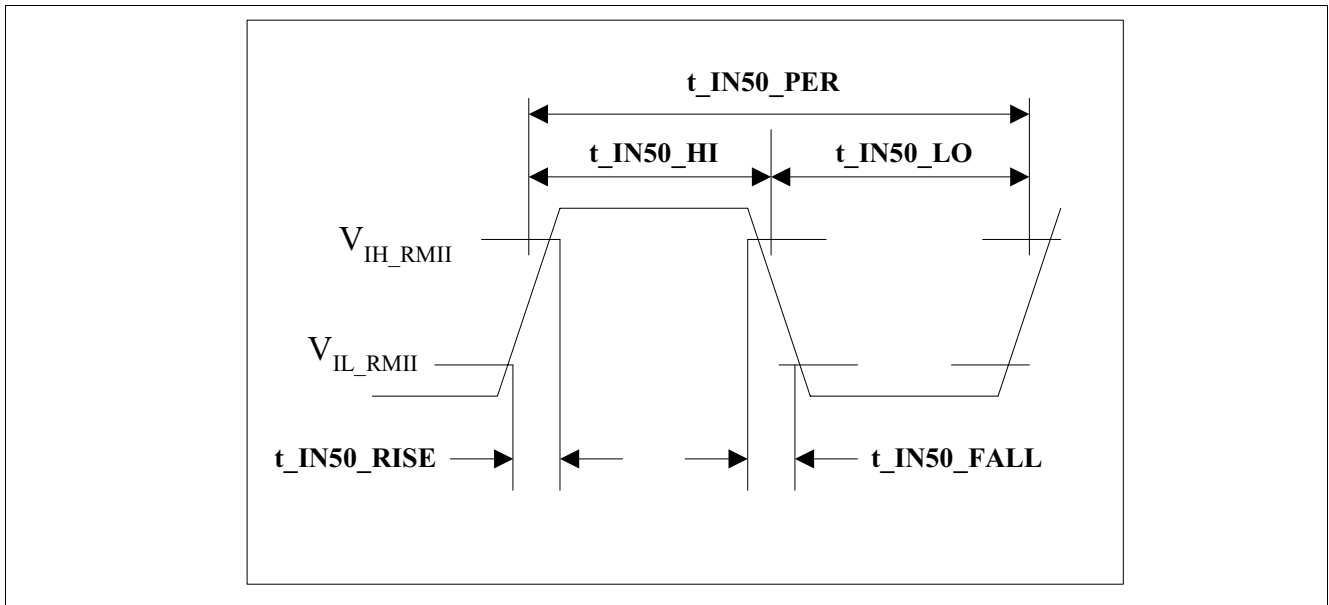
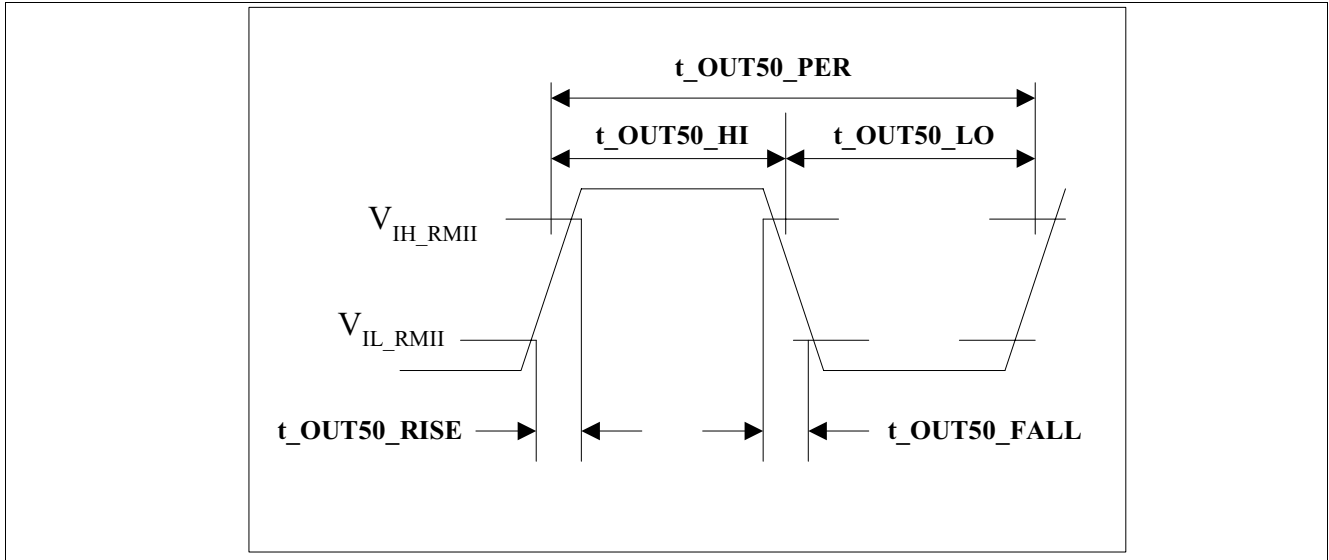


Figure 26 REFCLK Input Timing

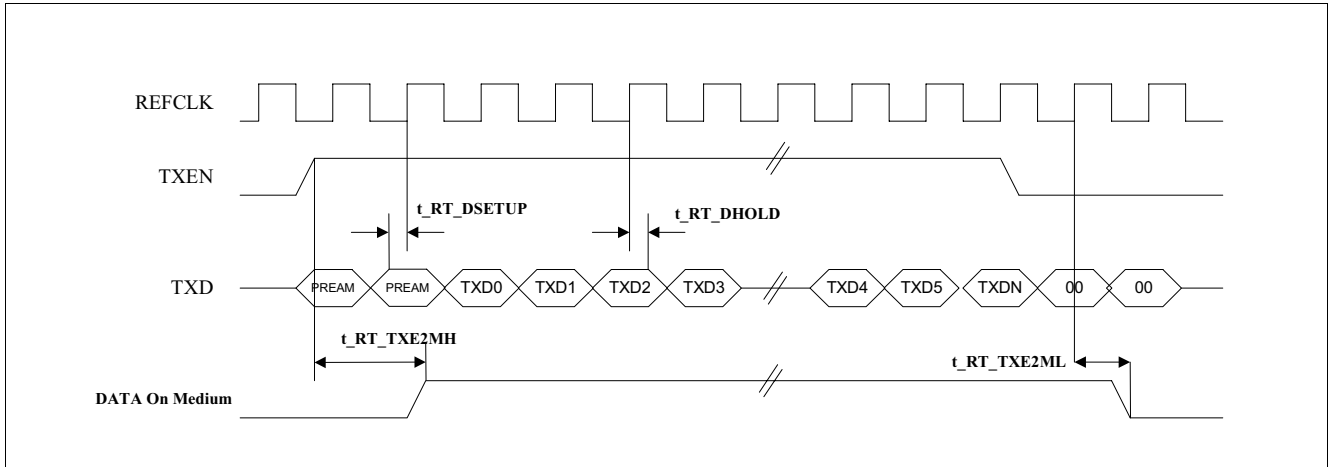
Table 27 REFCLK Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
REFCLK Clock Period	t_{IN50_PER}	20.0 - 50 ppm	20.0	20.0 + 50 ppm	ns	–
REFCLK Clock High	t_{IN50_HI}	8	10.0	–	ns	–
REFCLK Clock Low	t_{IN50_LO}	8	10.0	–	ns	–
REFCLK Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	t_{IN50_RISE}	–	–	2	ns	–
REFCLK Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	t_{IN50_FALL}	–	–	2	ns	–

5.3.2 REFCLK Output Timing (CLKO50 in RMI Mode)

Figure 27 REFCLK Output Timing
Table 28 REFCLK Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
REFCLK Clock Period	t_{OUT50_PER}	20.0 - 50 ppm	20.0	20.0 + 50 ppm	ns	–
REFCLK Clock High	t_{OUT50_HI}	8	10.0	12	ns	–
REFCLK Clock Low	t_{OUT50_LO}	8	10.0	12	ns	–
REFCLK Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	t_{OUT50_RISE}	–	–	2	ns	–
REFCLK Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	t_{OUT50_FALL}	–	–	2	ns	–
REFCLK Clock Jittering (p-p)	t_{OUT50_JIT}	–	0.15	–	ns	v

5.3.3 RMI Transmit Timing


Figure 28 RMI Transmit Timing
Table 29 RMI Transmit Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TXD to REFCLK Rising Setup Time	t_{RT_DSETUP}	2	–	–	ns	–
TXD to REFCLK Rising Hold Time	t_{RT_DHOLD}	2	–	–	ns	–
TXEN asserts to data transmit to medium	$t_{RT_TXE2MH100}$	–	–	235	ns	–
TXEN asserts to data transmit to medium	$t_{RT_TXE2MH10}$	–	–	1550	ns	–
TXEN de-asserts to finish transmitting	$t_{RT_TXE2ML100}$	–	–	260	ns	–
TXEN de-asserts to finish transmitting	$t_{RT_TXE2ML10}$	–	–	1250	ns	–

5.3.4 RMI Receive Timing

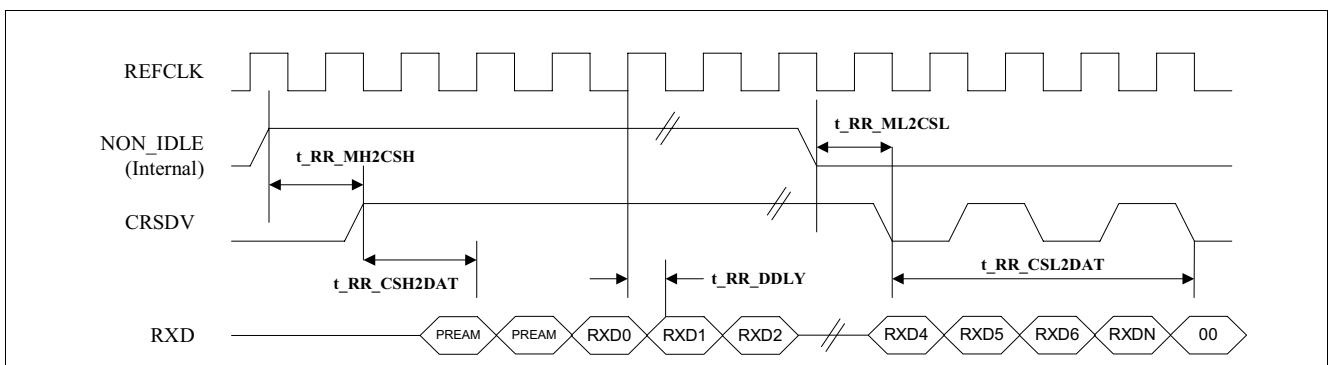

Figure 29 RMI Receive Timing

Table 30 RMI Receive Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Signal Detected on Medium to CRSDV High	$t_{RR_MH2CSH100}$	–	–	265	ns	–
Signal Detected on Medium to CRSDV High	$t_{RR_MH2CSH10}$	–	–	1000	ns	–
IDLE Detected on Medium to CRSDV low	$t_{RR_ML2CSL100}$	–	–	260	ns	–
IDLE Detected on Medium to CRSDV low	$t_{RR_ML2CSL10}$	–	–	570	ns	–
CRSDV High to Receive Data on RXD	$t_{RR_CSH2DAT100}$	–	–	160	ns	–
CRSDV High to Receive Data on RXD	$t_{RR_CSH2DAT10}$	–	–	1600	ns	–
CRSDV Toggle to End of Data Receiving	$t_{RR_CSL2DAT100}$	–	160	–	ns	–
CRSDV Toggle to End of Data Receiving	$t_{RR_CSL2DAT10}$	–	1600	–	ns	–
REFCLK Rising to RXD/CRSDV Delay Time	t_{RR_DDLTY}	–	–	5	ns	–

5.4 MII Timing

5.4.1 RXCLK Clock Timing

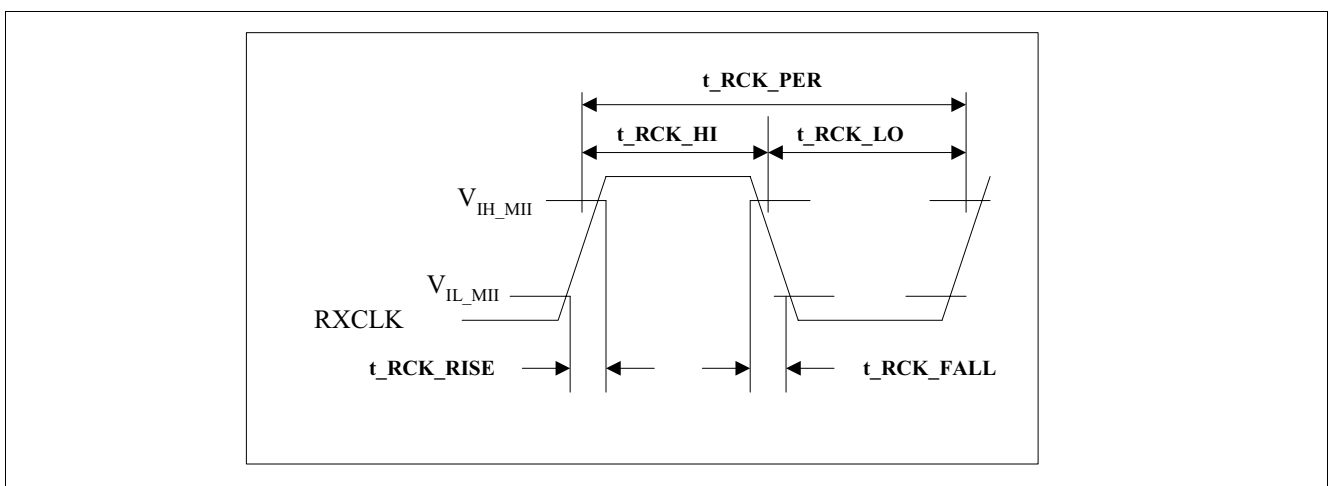
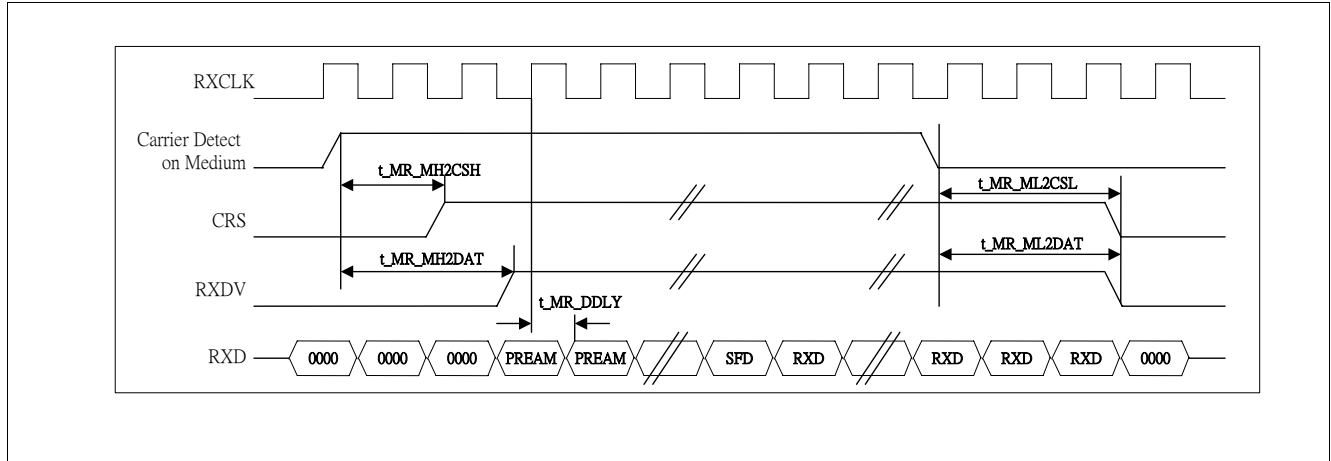

Figure 30 RXCLK Output Timing

Table 31 REFCLK Input Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RXCLK Clock Period(100M) Note ¹⁾	t_{RCK_PER100}	40.0 - 50 ppm	40.0	40.0 + 50 ppm	ns	–
RXCLK Clock Period(10M) Note ²⁾	t_{RCK_PER10}	400.0 - 50 ppm	400.0	400.0 + 50 ppm	ns	–
RXCLK Clock High (100M)	t_{RCK_HI100}	16	–	24		–
RXCLK Clock High (10M)	t_{RCK_HI10}	–	200	–		–
RXCLK Clock Low (100M)	t_{RCK_LO100}	16	–	24	ns	–
RXCLK Clock Low (10M)	t_{RCK_LO10}	–	200	–		–
RXCLK Clock Rise Time, V_{IL} (max) to V_{IH} (min.)	t_{RCK_RISE}	–	–	2	ns	–
RXCLK Clock Fall Time, V_{IH} (min.) to V_{IL} (max)	t_{RCK_FALL}	–	–	2	ns	–
REFCLK Clock Jittering (p-p)	t_{RCK_JIT}	–	0.15	–	ns	–

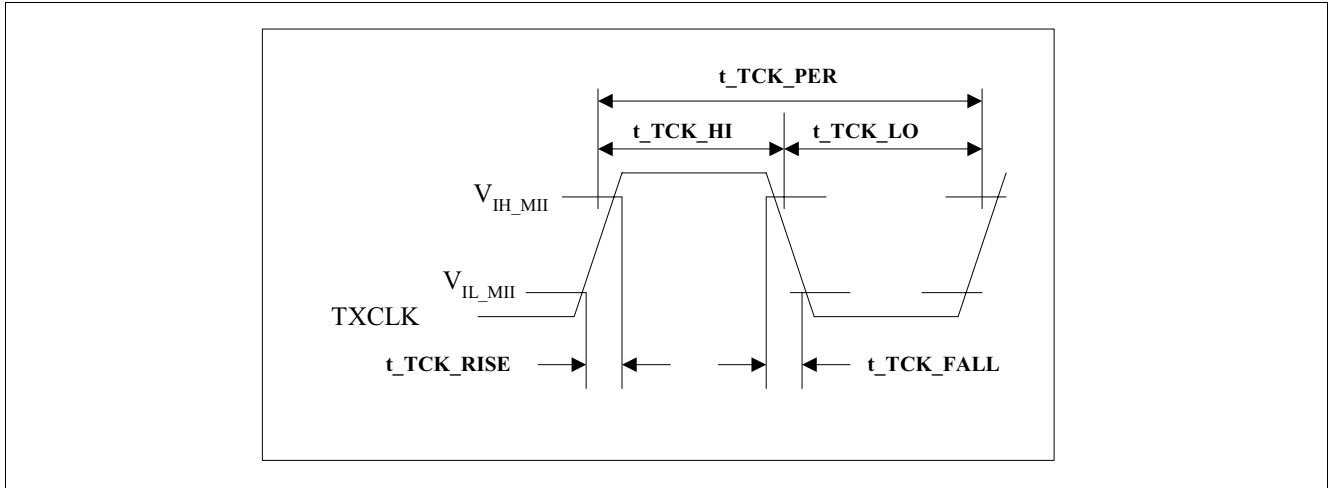
1) Clock period ppm value is highly depended upon peer transmitter clock source skew.

2) Clock period ppm value is highly depended upon peer transmitter clock source skew.

5.4.2 MII Receive Timing

Figure 31 MII Receive Timing
Table 32 MII Receive Timing

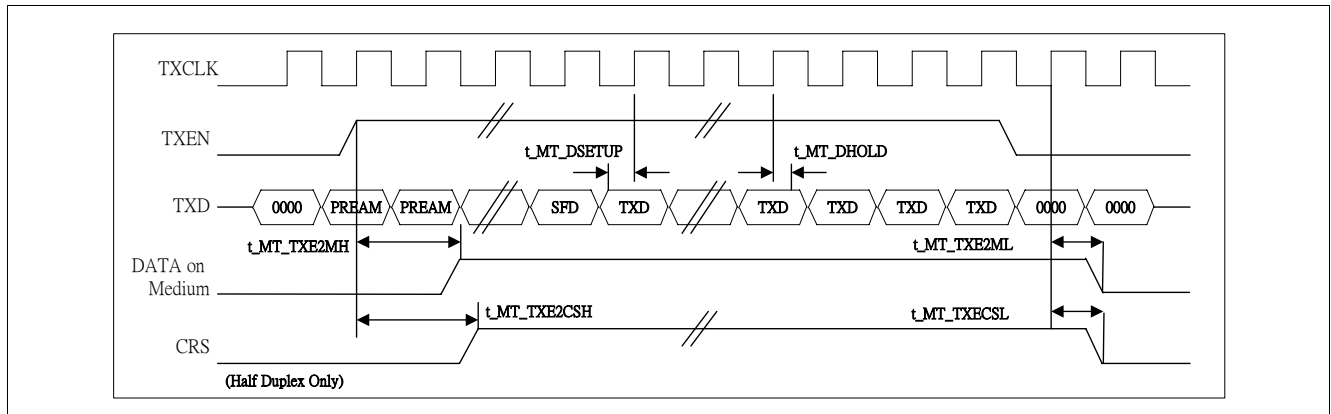
Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Signal Detected on Medium to CRS High	$t_{MR_MH2CSH100}$	–	–	140	ns	–
Signal Detected on Medium to CRS High	$t_{MR_MH2CSH10}$	–	–	1450	ns	–
Signal Detected on Medium to RXDV High	$t_{MR_MH2DAT100}$	–	–	150	ns	–
Signal Detected on Medium to RXDV High	$t_{MR_MH2DAT10}$	–	–	2300	ns	–
RXCLK rising to Data Valid Delay Time	$t_{MR_DDLY100}$	10	–	25	ns	–
RXCLK rising to Data Valid Delay Time	t_{MR_DDLY10}	10	–	25	ns	–
IDLE Detected on Medium to CRS Low	$t_{MR_ML2CSL100}$	–	–	120	ns	–
DLE Detected on Medium to CRS Low	$t_{MR_ML2CSL10}$	–	–	235	ns	–
DLE Detected on Medium to RXDV Low	$t_{MR_ML2DAT100}$	–	–	150	ns	–
DLE Detected on Medium to RXDV Low	$t_{MR_ML2DAT10}$	–	–	1450	ns	–

5.4.3 TXCLK Output Timing


Figure 32 TXCLK Output Timing
Table 33 TXCLK Output Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TXCLK Clock Period (100M)	t_{TCK_PER100}	40.0 - 50 ppm	40.0	40.0 + 50 ppm	ns	–
TXCLK Clock Period (10M)	t_{TCK_PER10}	40.0 - 50 ppm	40.0	40.0 + 50 ppm	ns	–
TXCLK Clock High (100M)	t_{TCK_HI100}	16	–	24	ns	–
TXCLK Clock High (10M)	t_{TCK_HI10}	160	–	240	ns	–
TXCLK Clock Low(100M)	t_{TCK_LO100}	16	–	24	ns	–
TXCLK Clock High (10M)	t_{TCK_LO10}	160	–	240	ns	–
TXCLK Clock Rise Time, VIL (max) to VIH (min)	t_{TCK_RISE}	–	–	2	ns	–
TXCLK Clock Fall Time, VIH (min) to VIL (max)	t_{TCK_FALL}	–	–	2	ns	–
TXCLK Clock Jittering (p-p)	t_{TCK_JIT}	–	0.15	–	ns	–

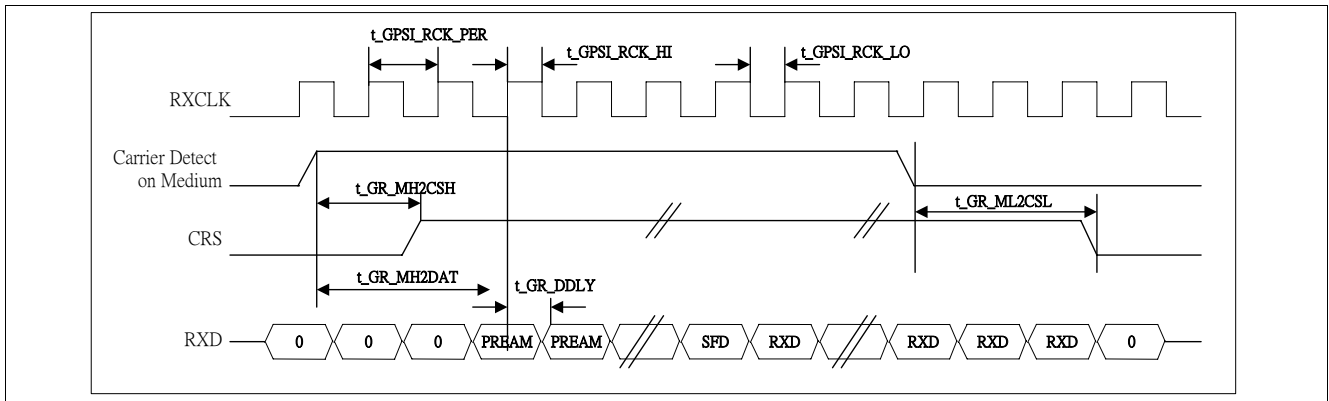
5.4.4 MII Transmit Timing


Figure 33 MII Transmit Timing
Table 34 MII Transmit Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TXD to TXCLK Rising Setup Time	t_{MT_DSETUP}	10	–	25	ns	–
TXD to TXCLK Rising Hold Time	t_{MT_DHOLD}	10	–	25	ns	–
TXEN asserts to data transmit to medium (100M)	$t_{MT_TXE2MH100}$	–	–	75	ns	–
TXEN asserts to data transmit to medium (10M)	$t_{MT_TXE2MH10}$	–	–	350	ns	–
TXEN asserts to CRS Assert (100M Half)	$t_{MT_TXE2CSH100}$	–	–	15	ns	–
TXEN asserts to CRS Assert (10M Half)	$t_{MT_TXE2CSH10}$	–	–	200	ns	–
TXEN de-asserts to finish transmitting (100M)	$t_{MT_TXE2ML100}$	–	–	95	ns	–
TXEN de-asserts to finish transmitting (10M)	$t_{MT_TXE2ML10}$	–	–	660	ns	–
TXEN de-asserts to CRS de-asserts (100M)	$t_{MT_TXE2CSL100}$	–	–	15	ns	–
TXEN de-asserts to CRS de-asserts (10M)	$t_{MT_TXE2CSL10}$	–	–	190	ns	–

5.5 GPSI Timing

5.5.1 GPSI Receive Timing


Figure 34 GPSI Receive Timing
Table 35 GPSI Receive Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
10M Receive Clock Period	$t_{\text{GPSI_RCK_PE}}^{\text{R}}$	100.0 - 50 ppm	100.0	100.0 + 50 ppm	ns	–
10M Receive Clock High	$t_{\text{GPSI_RCK_HI}}$	40	–	–	ns	–
10M Receive Clock Low	$t_{\text{GPSI_RCK_LO}}$	40	–	–	ns	–
Signal Detected on Medium to CRS High	$t_{\text{GR_MH2CSH}}$	–	–	1500	ns	–
Signal Detected on Medium to Data Valid	$t_{\text{GR_MH2DAT}}$	–	–	1600	ns	–
RXCLK rising to Data Valid Delay Time	$t_{\text{GR_DDLY}}$	40	–	60	ns	–
IDLE Detected on Medium to CRS Low	$t_{\text{GR_ML2CSL}}$	–	–	230	ns	–

5.5.2 GPSI Transmit Timing

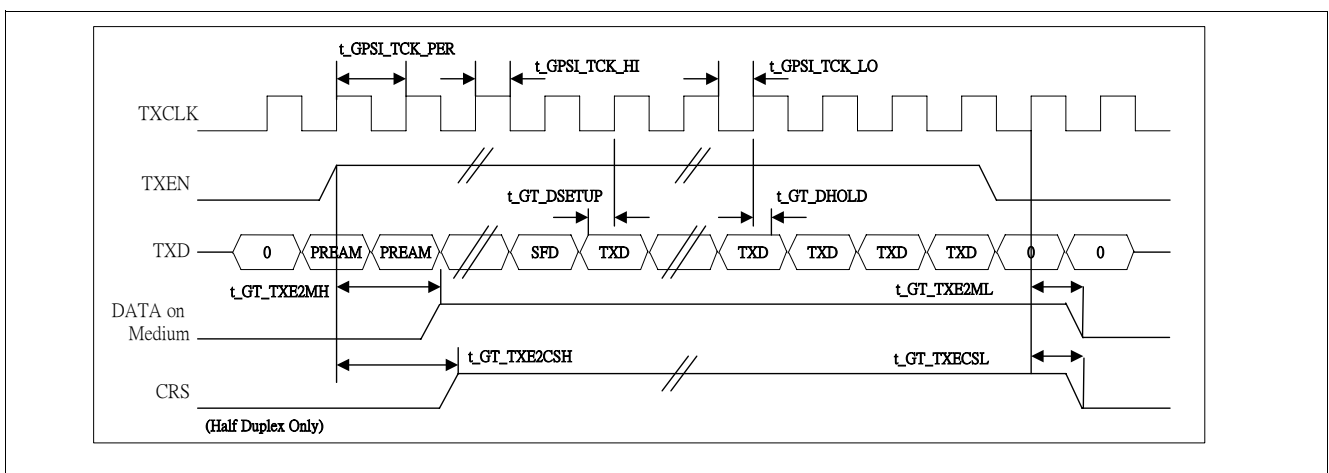
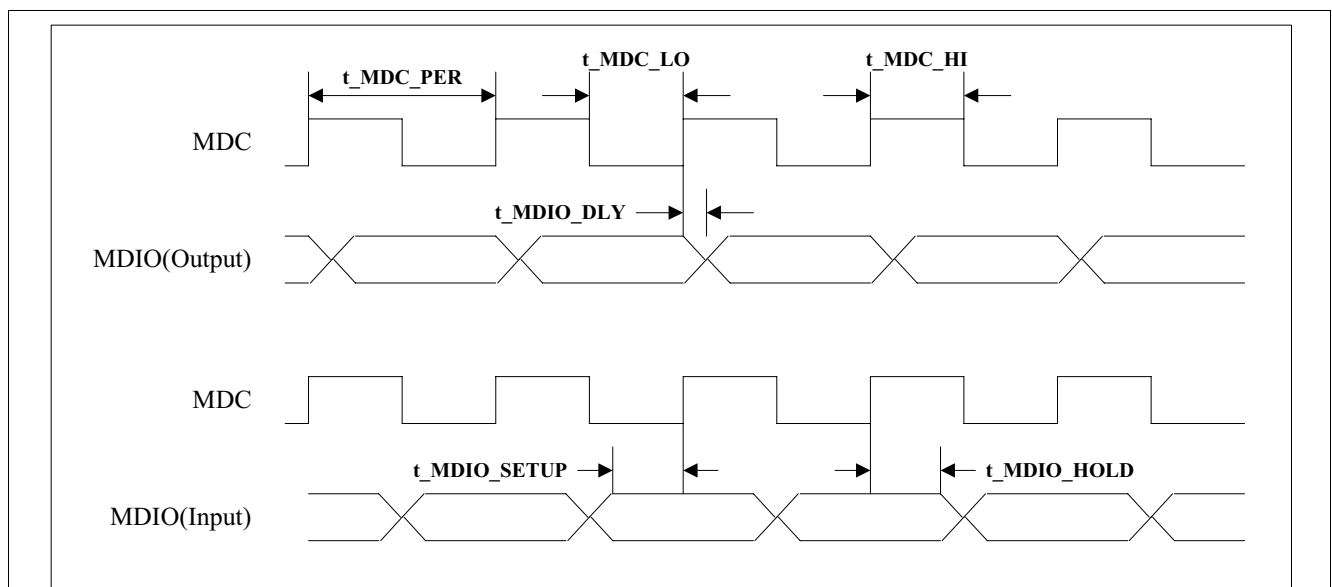

Figure 35 GPSI Transmit Timing

Table 36 GPSI Transmit Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
10M Transmit Clock Period	$t_{\text{GPSI_TCK_PE R}}$	100.0 - 50 ppm	100.0	100.0 + 50 ppm	ns	–
10M Transmit Clock High	$t_{\text{GSPI_TCK_HI}}$	40	–	–	ns	–
10M Transmit Clock Low	$t_{\text{GSPI_TCK_LO}}$	40	–	–	ns	–
TXD to TXCLK Rising Setup Time	$t_{\text{GT_DSETUP}}$	40	–	–	ns	–
TXD to TXCLK Rising Hold Time	$t_{\text{GT_DHOLD}}$	40	–	–	ns	–
TXEN asserts to data transmit to medium	$t_{\text{GT_TXE2MH}}$	–	–	150	ns	–
TXEN asserts to CRS Assert (Half)	$t_{\text{GT_TXE2CSH}}$	–	–	10	ns	–
TXEN de-asserts to finish transmitting	$t_{\text{GT_TXE2ML}}$	–	–	900	ns	–
TXEN de-asserts to CRS de-asserts	$t_{\text{GT_TXECSL}}$	–	–	10	ns	–

5.6 Serial Management Interface (MDC/MDIO) Timing

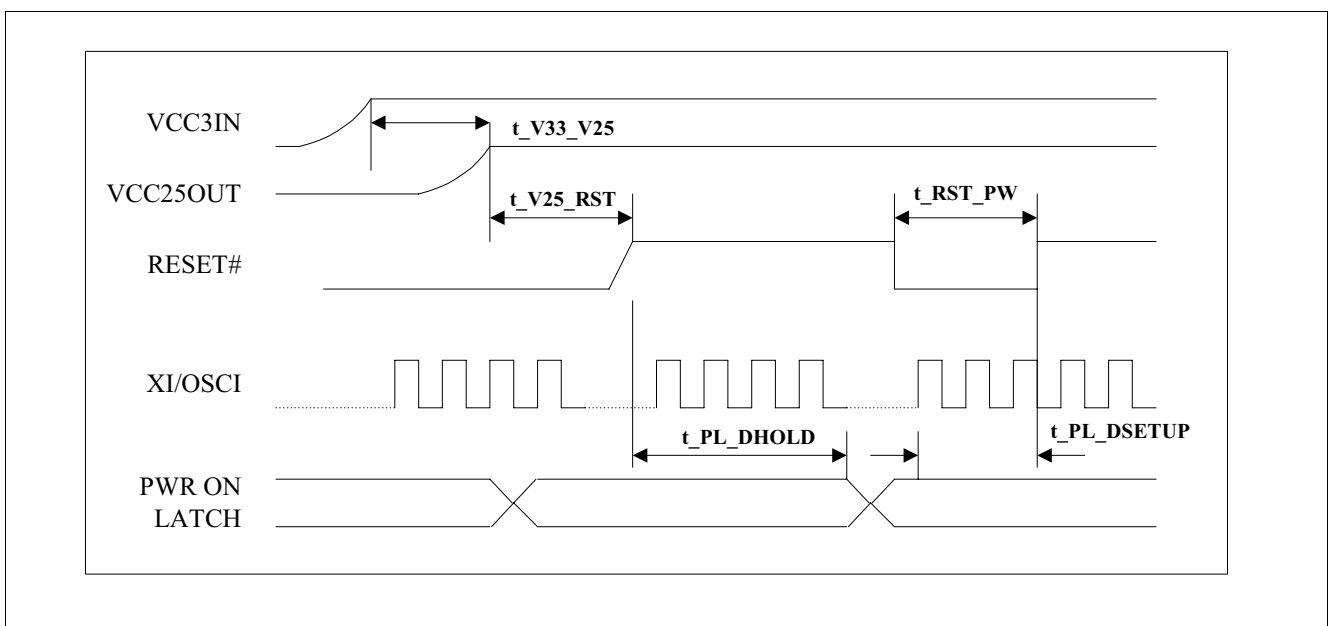

Figure 36 Serial Management Interface (MDC/MDIO) Timing
Table 37 Serial Management Interface (MDC/MDIO) Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC Period	$t_{\text{MDC_PER}}$	100	–	–	ns	–
MDC High	$t_{\text{MDC_HI}}$	40	–	–	ns	–

Table 37 Serial Management Interface (MDC/MDIO) Timing (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
MDC Low	t_{MDC_LO}	40	–	–	ns	–
MDC to MDIO Delay Time	t_{MDIO_DLY}	–	–	20	ns	–
MDIO Input to MDC Setup Time	t_{MDIO_SETUP}	10	–	–	ns	–
MDIO Input to MDC Hold Time	t_{MDIO_HOLD}	10	–	–	ns	–

5.7 Power On Configuration Timing


Figure 37 Power On Configuration Timing
Table 38 Power On Configuration Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
3.3V Power Good to 2.5 V Power Good	t_{V33_V25}	TBD	–	–	ms	–
Hardware Reset With Device Powered up	t_{V25_RST}	200	–	–	ms	–
Hardware Reset With Clock Running	t_{RST_PW}	800	–	–	ns	–
Reset High to Configuration Setup Time	t_{PL_DSETUP}	200	–	–	ns	–
Reset High to Configuration Hold Time	t_{PL_DHOLD}	0	–	–	ns	–

6 Packaging

ADM7001/X, Low Profile Quad Flat Package (LQFP) 48 Pin

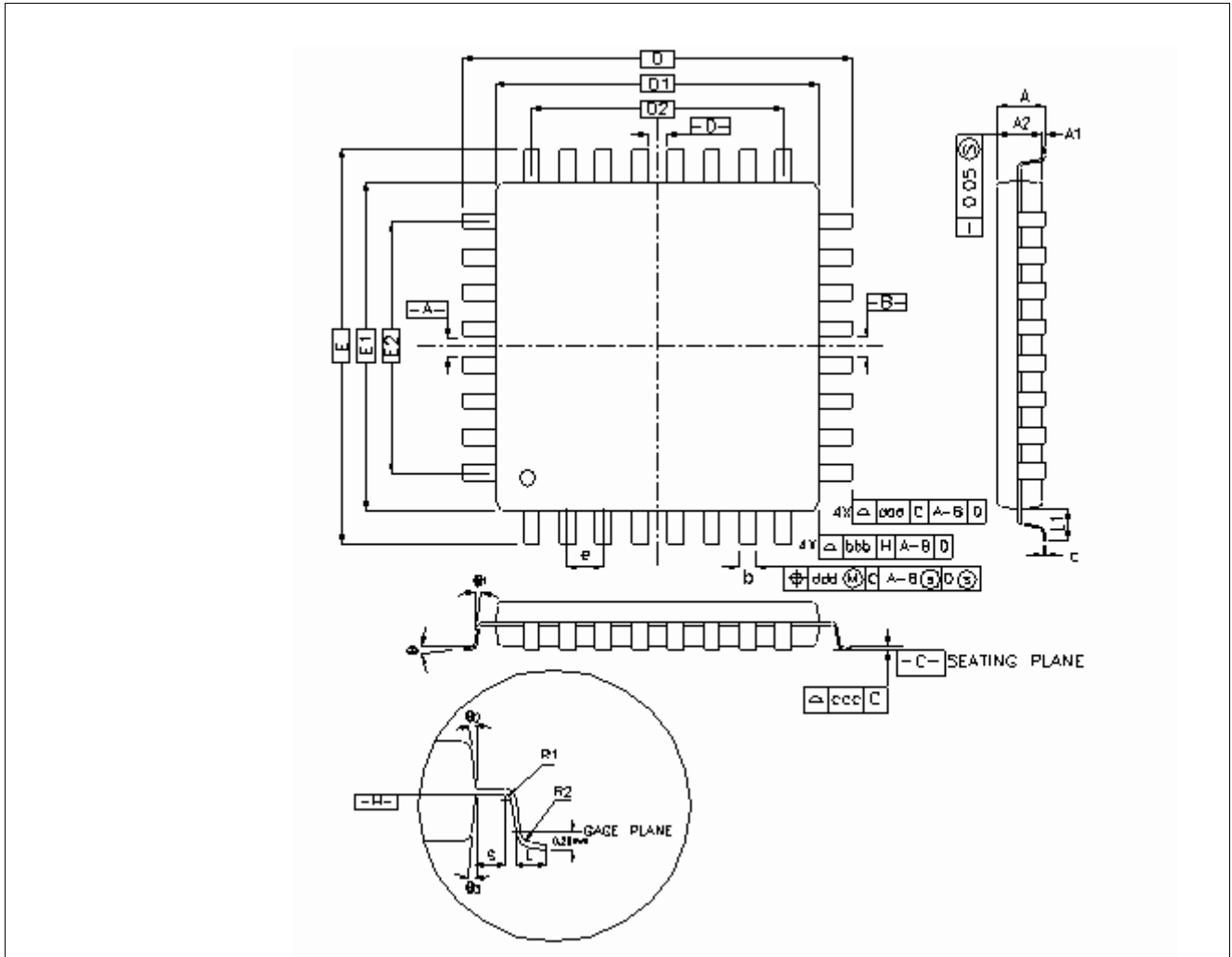


Figure 38 ADM7001/X, Low Profile Quad Flat Package (LQFP)

Table 39 Dimensions for 100 Pin LQFP Package

Symbol	Millimeter (mm)			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	–	–	1.60	–	–	0.063
A ₁	0.05	–	0.15	0.002	–	0.006
A ₂	1.35	1.40	1.45	0.053	0.005	0.057
D	9.00 BSC.			0.354 BSC.		
D ₁	7.00 BSC			0.276 BSC.		
E	9.00 BSC			0.354 BSC.		
E ₁	7.00 BSC			0.276 BSC.		
R ₂	0.08	–	0.20	0.003	–	0.008
R ₁	0.08	–	–	0.003	–	–
Θ	0°	3.5°	7°	0°	3.5°	7°
Θ ₁	0°	–	–	0°	–	–
Θ ₂	11°	12°	13°	11°	12°	13°
Θ ₃	11°	12°	13°	11°	12°	13°
c	0.09	–	0.20	0.004	–	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L ₁	1.00 Ref.			0.039 Ref.		
S	0.20	–	–	0.008	–	–
32L						
b	0.30	0.35	0.45	0.012	0.014	0.018
e	0.80 BSC.			0.031 BSC.		
D ₂	5.60			0.220		
E ₂	5.60			0.220		
Tolerance of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.10			0.003		
ddd	0.20			0.008		
44L						
b	0.17	0.20	0.27	0.007	0.008	0.011
e	0.50 BSC.			0.020 BSC.		
D ₂	5.00			0.197		
E ₂	5.00			0.197		
Tolerance of Form and Position						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.08			0.003		
48L						
b	0.17	0.20	0.27	0.007	0.008	0.011

Table 39 Dimensions for 100 Pin LQFP Package (cont'd)

Symbol	Millimeter (mm)	Inch
e	0.50 BSC.	0.020 BSC.
D ₂	5.50	0.217
E ₂	5.50	0.217
Tolerance of Form and Position		
aaa	0.20	0.008
bbb	0.20	0.008
ccc	0.08	0.003
ddd	0.08	0.003

www.infineon.com

Published by Infineon Technologies AG

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View ADM7001ACT1](#) on WIN SOURCE
- ⊖ [Infineon Technologies](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management