THE DATASHEET OF

ADCS9888CVH-170/NOPB

ADCS9888 205/170/140 MSPS Video Analog Front End

Check for Samples: ADCS9888

FEATURES

- **205 million pixels/s conversion rate**
- **Digitally programmed gain and offset for red, green and blue color balancing**
- **Compatible with RGB and YUV/YPbPr video signals**
- **Output format supports 4:2:2 video pulldown**

KEY SPECIFICATIONS

- **Output data resolution 8 bits x 3 channels**
- **Maximum pixel conversion rate 205 MHz**
- **Analog input bandwidth (typical) 500 MHz**
- **PLL clock jitter (typical) 570 ps p-p**
- **Analog supply voltage 3.0 V to 3.6 V**
- **I/O supply voltage 2.2 V to 3.6 V**
- **Power dissipation (typical) 1.3W**

APPLICATIONS

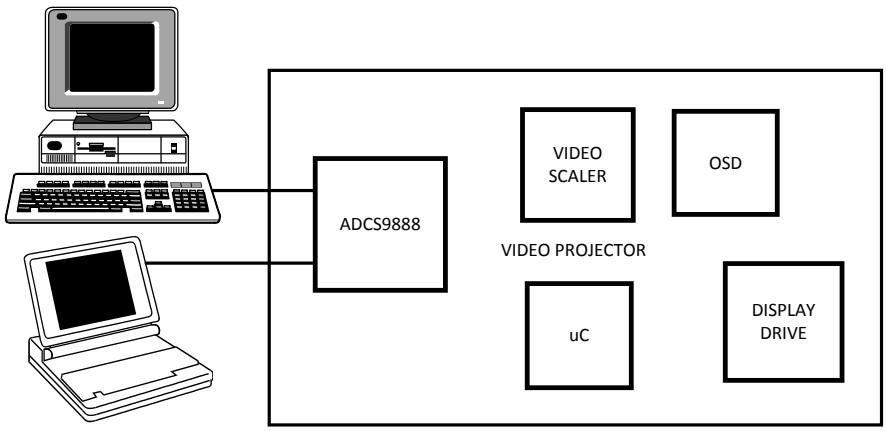
- **LCD flat panel monitors**
- **Video projectors**
- **Plasma display panels**
- **Video capture hardware**
- **RGB and YUV video processing**

DESCRIPTION

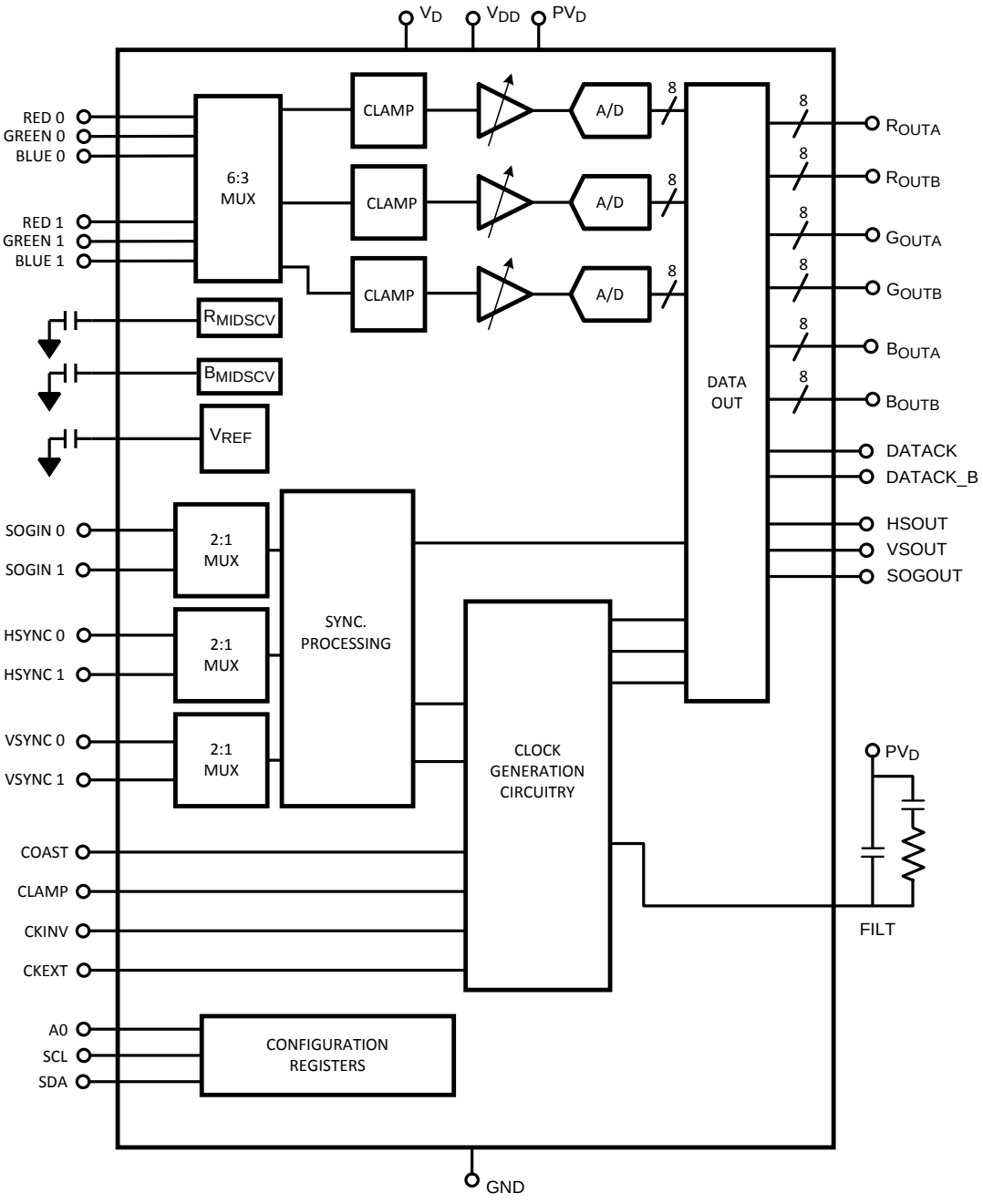
The ADCS9888 is a high performance Analog Front End (AFE) for digital video applications at resolutions up to UXGA. It performs all the analog and mixed signal functions necessary to digitize a variety of computer and component video sources. The ADCS9888 has a 3 channel, 8 bit 205 MHz ADC with full DC restoration and gain/offset compensation. Full processing of synchronization signals is included with on-chip PLL locked to the pixel rate. Digital sync and analog sync-on-green signals are supported. Flexible data output modes support a variety of downstream data capture and processing applications.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

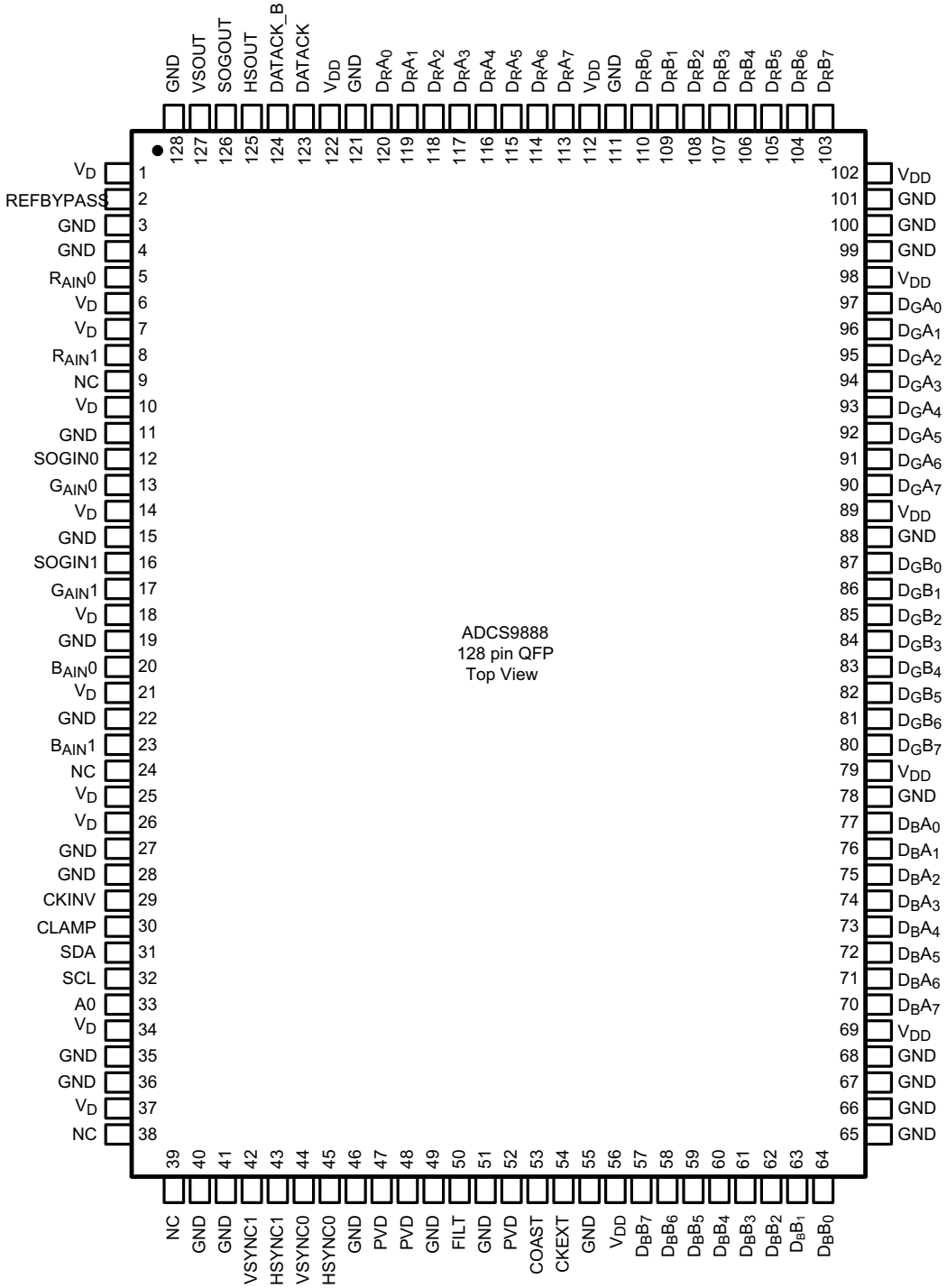
Typical Application



Simplified Block Diagram



Connection Diagram



Pin Descriptions

Pin	Label	Type	Description
Analog Video Inputs			
5	R_{AIN0}	Analog Input	Channel 0 Red (V) Video Input. Input for Red component video channel or V chrominance channel in YUV/YPbPr/YCbCr applications. A high impedance analog input. Input signal should be capacitively coupled to the input using a 0.1 µF capacitor to support clamping and DC restoration. Signal range of 0.5 V_{PP} to 1.0 V_{PP} depending on gain setting.
13	G_{AIN0}	Analog Input	Channel 0 Green (Y) Video Input. Input for Green component video channel or Y luminance channel in YUV/YPbPr/YCbCr applications. A high impedance analog input. Input signal should be capacitively coupled to the input using a 0.1 µF capacitor to support clamping and DC restoration. Signal range of 0.5 V_{PP} to 1.0 V_{PP} depending on gain setting.
20	B_{AIN0}	Analog Input	Channel 0 Blue (U) Video Input. Input for Blue component video channel or U chrominance channel in YUV/YPbPr/YCbCr applications. A high impedance analog input. Input signal should be capacitively coupled to the input using a 0.1 µF capacitor to support clamping and DC restoration. Signal range of 0.5 V_{PP} to 1.0 V_{PP} depending on gain setting.
8	R_{AIN1}	Analog Input	Channel 1 Red (V) Video Input. See R_{AIN0} for more information.
17	G_{AIN1}	Analog Input	Channel 1 Green (Y) Video Input. See G_{AIN0} for more information.
23	B_{AIN1}	Analog Input	Channel 1 Blue (U) Video Input. See B_{AIN0} for more information.
Analog Video Sync			
12	SOGIN0	Analog Input	Channel 0 Sync-On-Green-Input. A high impedance analog input. The video channel containing synchronization information should be capacitively coupled to this input using a 1.0 nF capacitor to support negative peak clamping of the signal. When unused, this input should be left unconnected.
16	SOGIN1	Analog Input	Channel 1 Sync-On-Green-Input. See SOGIN0 for more information.
Sync/Clock Inputs			
45	HSYNC0	Digital Input	Channel 0 Horizontal Sync Input. A logic level synchronization signal at the horizontal line rate is applied to this input. In applications where a composite, logic level sync signal is present, that signal should be connected to the HSYNC input. A Schmitt trigger input is used for improved noise rejection. See the Application Information section for more information.
44	VSYNC0	Digital Input	Channel 0 Vertical Sync Input. A logic level synchronization signal at the vertical frame rate is applied to this input. A Schmitt trigger input is used for improved noise rejection. See the Application Information section for more information.
43	HSYNC1	Digital Input	Channel 1 Horizontal Sync Input. See HSYNC0 for more information.
42	VSYNC1	Digital Input	Channel 1 Vertical Sync Input. See VSYNC0 for more information.
30	CLAMP	Digital Input	External CLAMP Timing Input. When enabled via Register OFh, Bit 7, this input will turn on the clamp circuits in the analog video inputs. This signal should be asserted during the black reference portion of the video waveform. Please refer to the Application Information section for more information.
53	COAST	Digital Input	PLL Clock Generator Coast Input. When enabled via Register 0Fh, Bit 5, this input will cause the clock generator circuit to run open loop and ignore the input reference clock. This is useful when operating with sync signals that contain extra equalization pulses that must be ignored by the PLL. In many cases, the internal VSOUT signal is used to provide the coast control signal, but in some cases it is useful to provide an external COAST control. Please refer to the Application Information section for more information.
54	CKEXT	Digital Input	External Clock Input (Optional). This input can be used to provide an external clock source instead of the internally generated clock. It is enabled via Register 15h, Bit 0. When an external clock is used, most other internal functions operate normally. When unused, this pin can be connected to ground directly, or through a 10 kΩ resistor. The sampling phase adjustment feature is operational when CKEXT is used.
29	CKINV	Digital Input	Sampling clock Inverting Input. This input can be used to invert the pixel sampling clock, with respect to the normal phase of operation. This causes the pixel sampling point to be shifted by 180 degrees in phase. Alternate pixel sampling mode makes use of this feature by sampling at 1/2 the incoming pixel rate, and switching the sampling phase by 180 degree between alternate frames of video. When unused, this input should be grounded. See the Application Information section for more information.
Serial Interface			

Pin Descriptions (continued)

Pin	Label	Type	Description
31	SDA	Digital I/O	Serial Control Interface Data Input/Output. The serial interface is used to access the configuration and status registers in the ADCS9888. Mode and Data information are transferred through the SDA pin from the host or master device. Please refer to the Application Information section of the datasheet under Serial Communications for more information.
32	SCL	Digital Input	Serial Control Interface Clock Input. The clock input is controlled by the host or master device, and is used to load in the data sent by the host, and to clock data out of the ADCS9888. Please refer to the Application Information section of the datasheet under Serial Communications for more information.
33	A0	Digital Input	The least significant bit of the device serial address is selectable as 0 or 1 to allow up to 2 ADCS9888 devices to be connected on the same serial interface. Please refer to the Application Information section of the datasheet under Serial Communications for more information.
Sync. Outputs			
125	HSOUT	Digital Output	Horizontal Sync Output. Internally generated and phase aligned horizontal sync signal. This signal is used as a timing reference for the digital output data stream. Please refer to the section on sync processing for more information.
127	VSOUT	Digital Output	Vertical Sync Output. A delayed version of the input vertical synchronization signal. Please refer to the section on sync processing for more information.
126	SOGOUT	Digital Output	Sync-On-Green Output. A logic level signal that is the output of the Sync-On-Green slicer circuit. Please refer to the section on sync processing for more information.
Data Clock Output			
123	DATACK	Digital Output	Data Output Clock. Complementary data clocks are provided so that output data and HSOUT can be synchronously captured by external logic or memory devices. The clock outputs are synchronous with the internal pixel sample clock. As the sampling phase is adjusted, the DATACK, data, and HSOUT signals all shift together with the sampling interval. When the chip is in power down or seek mode, the DATACK outputs enter a high impedance state.
124	DATACK_B	Digital Output	Data Output Clock Invert. See DATACK description.
Data Outputs			
113-120	D_R_A(7:0)	Digital Output	Red Port A (V or U/V) Output Data. Converted pixel data is presented at the data output port synchronous with the DATACK and HSOUT signals. As the pixel sample phase is adjusted, the HSOUT, DATACK and data outputs all shift together. In single channel mode, all data is presented at the A output ports. In dual channel mode, output data is presented at A and B outputs, either in alternating (interleaved mode) or simultaneous (parallel mode) timing. When 4:2:2 pulldown mode is enabled, only the A ports are used, with U/V data output on Red Port A, and Y data output on Green Port A. When the chip is in seek mode, or low power mode, all data outputs are placed in a high impedance state. See the Application Information section and Configuration Register Descriptions section for more information.
103-110	D_R_B(7:0)	Digital Output	Red Port B (V) Output Data. See D_R_A(7:0).
90-97	D_G_A(7:0)	Digital Output	Green Port A (Y) Output Data. See D_R_A(7:0).
80-87	D_G_B(7:0)	Digital Output	Green Port B (Y) Output Datasheet. See D_R_A(7:0).
70-77	D_B_A(7:0)	Digital Output	Blue Port A (U) Output Data. See D_R_A(7:0).
57-64	D_B_B(7:0)	Digital Output	Blue Port B (U) Output Data. See D_R_A(7:0).
Voltage Reference Bypass			
2	REF BYPASS	Analog Bypass	Internal Reference Bypass. A 0.1 µF capacitor will be connected from this pin to ground, to provide a low impedance decoupling for the internal 1.23V bandgap voltage reference.
9	R_{MIDSC}V (NC)	Analog Bypass	Red (V) Channel midscale Voltage Bypass. No external bypass is required for the midscale voltage. Therefore, this pin is not connected to the internal circuitry. To maintain compatibility with other designs external capacitors can be connected without affecting operation, performance, or reliability.
24	B_{MIDSC}V (NC)	Analog Bypass	Blue (U) Channel midscale Voltage Bypass. No external bypass is required for the midscale voltage. Therefore, this pin is not connected to the internal circuitry. To maintain compatibility with other designs external capacitors can be connected without affecting operation, performance, or reliability.
PLL Loop Filter			

Pin Descriptions (continued)

Pin	Label	Type	Description
50	FILT	PLL VCO Bypass	Phase Locked Loop - Voltage Controlled Oscillator filter connection. An R/C filter circuit is used to maintain the VCO control voltage. This circuit should be isolated from all other circuitry to minimize clock jitter. The circuit is connected to the PV_D bus to provide the maximum isolation from noisy power and ground buses. Refer to the Application Information section for more information.
Power Supply			
1, 6, 7, 10, 14, 18, 21, 25, 26, 34, 37	V_D	Power Supply	Main power supply for analog and digital circuitry inside the IC. The data outputs and PLL are powered from separate buses for additional noise isolation.
56, 69, 79, 89, 98, 102, 112, 122	V_{DD}	Power Supply	Power supply for digital data outputs. This voltage can be operated at voltages below the Main Power Supply, down to 2.5V, to provide convenient interfaces to lower voltage circuitry.
47, 48, 52	PV_D	Power Supply	Phase Locked Loop Power Supply. This input should be well filtered, isolated, and decoupled, to provide a very stable, low noise, voltage source for the PLL and VCO circuitry in the ADCS9888.
3, 4, 11, 15, 19, 22, 27, 28, 35, 36, 40, 41, 46, 49, 51, 55, 65-68, 78, 88, 99-101, 111, 121, 128	GND	Ground	Ground Return. Ground return for all circuitry on the chip. For best performance, the printed circuit board should be designed using a single solid ground plane. Other ICs should be placed to minimize the effects of noisy digital ground returns interfering with the ADCS9888 operation.
39, 39	NC	NC	To ensure compliance with designs using the AD9888, these pins are not connected to the IC die. They may be physically connected to either V_D or PV_D with no effect on operation, performance, or reliability.

Absolute Maximum Ratings[1][2][3]

Positive Supply Voltage ($V^+ = V_D$, PV_D, V_{DD}) With Respect to GND		3.6V
Voltage on Any Input or Output Pin		−0.3V to V^+ +0.3V
Voltage on VSYNC, HSYNC Input Pin		−0.3V to 5.5V
Input Current at any pin[4]		±25 mA
Package Input Current[4]		±50 mA
Package Dissipation at T_A = 25°C		See[5]
ESD Susceptibility[6]	Human Body Model	6500V
	Machine Model	250V
Soldering Information		See[7]
Storage Temperature		−65°C to +150°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(4) When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN} < GND or V_{IN} > V_A or V_D), the current at that pin should be limited to 25 mA. The 50 mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25 mA to two.
(5) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$. T_{JMAX} = 150°C for this device. The typical thermal resistance (θ_{JA}) of this part when board mounted is TBD °C/W for the NND0128A 128 pin QFP package.
(6) Human body model is 100 pF capacitor discharged through a 1.5 kΩ resistor. Machine model is 200 pF discharged through a 0 Ω resistor.
(7) Soldering process must comply with National Semiconductor's reflow temperature profile specifications. Refer to "www.ti.com/packaging".

Operating Ratings[1]

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADCS9888CVH	0°C ≤ T_A ≤ +70°C
V_D Supply Voltage	+3.0V to +3.6V
PV_D Supply Voltage	+3.0V to +3.6V
V_{DD} Supply Voltage	+2.2V to +3.6V
(PV_D or V_{DD})-V_D, V_D-PV_D	≤100 mV
Analog Input Voltage Range	−0.05 to V_D + 0.05V
Digital Input Voltage Range	−0.05 to V_D + 0.05V

(1) All voltages are measured with respect to GND = 0 V, unless otherwise specified.

Electrical Characteristics

The following specifications apply for GND = 0 V, $V_D = V_{DD} = PV_D$ = +3.3 V_{DC}, ADC Clock = 205 MHz, unless otherwise specified. **Boldface limits apply for $T_A = T_{MIN}$ to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min(1)	Typical(2)	Max(1)	Units
ANALOG VIDEO CHANNEL CHARACTERISTICS						
	Resolution			8		Bits
DC ACCURACY						
DNL	Differential Non-Linearity	140 MSPS		+0.5 –0.4	**+1.35** **−1.0**	LSBs
		170 MSPS		+0.6 –0.5	**+1.5** **−1.0**	
		205 MSPS		+0.8 –0.6	**+1.80** **−1.0**	
INL	Integral Non-Linearity Error(3)	140 MSPS		+1.0 −0.7	**+2.0** **–2.0**	LSBs
		170 MSPS		+1.0 −0.9	**+2.25** **–2.25**	
		205 MSPS		+1.2 −1.0	**+2.75** **–2.75**	
CODES	No Missing Codes	25°C	Guaranteed			
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Input Voltage Range Minimum	25°C			0.5	V_{PP}
	Input Voltage Range Maximum		1.0			
	Gain Tempco	25°C		100		ppm/°C
I_{IN}	Input Bias Current	25°C Full Temp. Range(4)			1 **2**	µA
C_{IN}	Input Capacitance	Full Temp. Range		3		pF
R_{IN}	Input Resistance	Full Temp. Range(4)	1			MΩ
V_{OS}	Input Offset Voltage	Full Temp. Range		12	**105**	mV
	Input Full-Scale Matching	Full Temp. Range		1	**9**	%FS
	Offset Adjustment Range	Full Temp. Range	**41**	49	**57**	%FS
INTERNAL VOLTAGE REFERENCE CHARACTERISTICS						
V_{REF}	Output Voltage	Full Temp. Range	**1.15**	1.225	**1.30**	V
	Temperature Coefficient	Full Temp. Range		±50		ppm/°C

(1) Test limits are specified to National's AOQL (Average Outgoing Quality Level).
(2) Typical figures are at $T_J = T_A$ = 25°C, with the ADC Clock at the stated speed, and represent most likely parametric norm.
(3) Full channel integral non-linearity error is defined as the deviation of the analog value, expressed in LSBs from the straight line that best fits the actual transfer function of the AFE.
(4) These values are specified by design and characterization testing.

AC Electrical Characteristics

The following specifications apply for GND = 0 V, V_D = V_{DD} = PV_D = +3.3 V_{DC}, ADC Clock = 205 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_{MIN} to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min(1)	Typical(2)	Max(1)	Units
	Maximum Conversion Rate	Full Temp. Range	**140** **170** **205**			MSPS
	Minimum Conversion Rate	Full Temp. Range(3)			**10**	MSPS
	Data to Clock Skew	Full Temp. Range		0.9		ns
t_{BUFF}		Full Temp. Range	**4.7**			µs
t_{STAH}		Full Temp. Range	**4.0**			µs
t_{DHO}		Full Temp. Range	**0**			µs
t_{DAL}		Full Temp. Range	**4.7**			µs
t_{DAH}		Full Temp. Range	**4.0**			µs
t_{DSU}		Full Temp. Range	**259**			ns
t_{STASU}		Full Temp. Range	**4.7**			µs
t_{STOSU}		Full Temp. Range	**4.0**			µs
	HSYNC Input Frequency	Full Temp. Range	**15**		**110**	kHz
	Maximum PLL Clock Rate	Full Temp. Range	**100/140** **170** **205**			MHz
	Minimum PLL Clock Rate	Full Temp. Range			15	MHz
	PLL Jitter	25°C(3)		570	800	ps p-p
	Sampling Phase Tempco	Full Temp. Range(3)		15		ps/°C

(1) Test limits are specified to National's AOQL (Average Outgoing Quality Level).
(2) Typical figures are at T_J = T_A = 25°C, with the ADC Clock at the stated speed, and represent most likely parametric norm.
(3) These values are specified by design and characterization testing.

DC and Logic Electrical Characteristics

The following specifications apply for GND = 0 V, V_D = V_{DD} = PV_D = +3.3 V_{DC}, ADC Clock = 205 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_{MIN} to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min(1)	Typical(2)	Max(1)	Units
DIGITAL INPUT CHARACTERISTICS						
$V_{IN(1)}$	Logical “1” Output Voltage		**2.5**			V
$V_{IN(0)}$	Logical “0” Output Voltage				**0.8**	V
I_{IH}	Input Leakage Current	See(3)			**−1.0**	µA
I_{IL}	Input Leakage Current	See(3)			**1.0**	µA
C_{IN}	Input Capacitance			3		pF
DIGITAL OUTPUT CHARACTERISTICS						
$V_{OUT(1)}$	Logic “1” Output Voltage		**V_{DD}-0.1**			V
$V_{OUT(0)}$	Logic “0” Output Voltage				**0.1**	V
	Duty Cycle DATACK, DATACK_B	See(3)	**44**	49	**55**	%
	Output Coding		Binary			
POWER SUPPLY CHARACTERISTICS						
	V_D Supply Voltage	See(3)	**3.0**	3.3	**3.6**	V
	V_{DD} Supply Voltage	See(3)	**2.2**	3.3	**3.6**	V
	PV_D Supply Voltage	See(3)	**3.0**	3.3	**3.6**	V

(1) Test limits are specified to National's AOQL (Average Outgoing Quality Level).
(2) Typical figures are at T_J = T_A = 25°C, with the ADC Clock at the stated speed, and represent most likely parametric norm.
(3) These values are specified by design and characterization testing.

DC and Logic Electrical Characteristics (continued)

The following specifications apply for GND = 0 V, V_D = V_{DD} = PV_D = +3.3 V_{DC}, ADC Clock = 205 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_{MIN} to T_{MAX};** all other limits T_A = 25°C.

Symbol	Parameter	Conditions	Min(1)	Typical(2)	Max(1)	Units
I_D	Core Supply Current	25°C - 140 MSPS		259		mA
		25°C - 170 MSPS		275		
		25°C - 205 MSPS		316		
I_{DD}(4)	I/O Supply Current	25°C - 140 MSPS		38		mA
		25°C - 170 MSPS		40		
		25°C - 205 MSPS		57		
IP_{VD}	PLL Supply Current	25°C - 140 MSPS		13		mA
		25°C - 170 MSPS		14		
		25°C - 205 MSPS		18		
	Total Power Dissipation	Full Temp. – 140 MSPS		320	**365**	mA
		Full Temp. – 170 MSPS		330	**375**	
		Full Temp. – 205 MSPS		390	**420**	
	Power Down Supply Current	Full Temp.		8.4	**15**	mA
	Power Down Dissipation	Full Temp.		28	**50**	mW

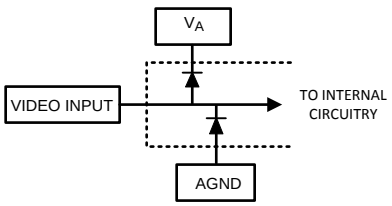
(4) The output supply current (I_{DD}) includes the power required to drive a typical digital bus and load circuit at the stated test frequency. The actual output supply current will depend on the load capacitance of the printed circuit board and connected load device, and the operating frequency and output mode in the application.

Analog Channel Characteristics

The following specifications apply for GND = 0 V, V_D = V_{DD} = PV_D = +3.3 V_{DC}, V_{DD} = +3.3 V_{DC}, ADC Clock = 205 MHz, unless otherwise specified. **Boldface limits apply for T_A = T_{MIN} to T_{MAX};** all other limits T_A = 25°C(1).

Symbol	Parameter	Conditions	Min(2)	Typical(3)	Max(2)	Units
	Analog Bandwidth, Full Power	25°C		500		MHz
	Transient Response	25°C		2		ns
	Overvoltage Recovery Time	25°C		1.5		ns
SNR	Signal to Noise Ratio (Without Harmonics)	25°C – 140 MSPS	40.7	44		dB
		25°C –170 MSPS	40.7	43.5		
		25°C –205 MSPS	40.5	43.5		
SNR	Signal to Noise Ratio (Without Harmonics)	Full temp. – 140 MSPS		44		dB
		Full Temp. – 170 MSPS		43.5		
		Full Temp. – 205 MSPS		43.5		
	Crosstalk	Full Temp.		50		dBc
THERMAL CHARACTERISTICS						
θ_{JC}	Junction to Case Thermal Resistance			12.3		°C/W
θ_{JA}	Junction to Ambient Thermal Resistance			30.2		°C/W

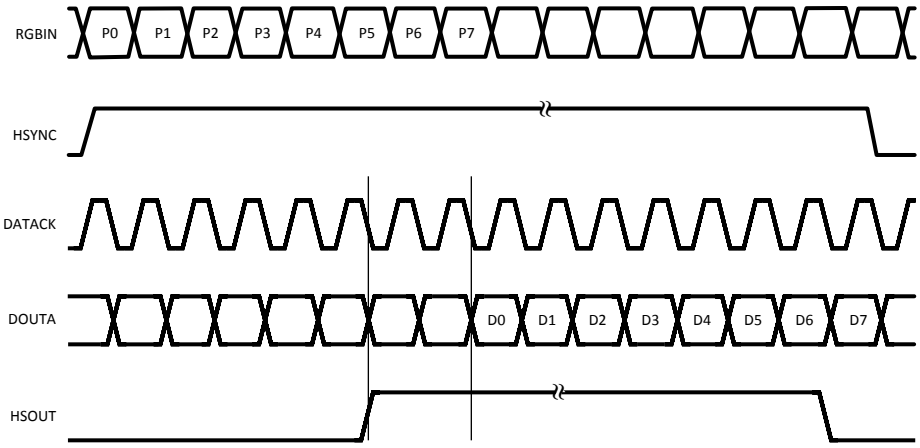
(1) Two diodes clamp the OS analog inputs to AGND and V_A as shown below. This input protection, in combination with the external clamp capacitor and the output impedance of the video source, prevents damage to the ADCS9888 from transients during power-up.



(2) Test limits are specified to National's AOQL (Average Outgoing Quality Level).
(3) Typical figures are at T_J = T_A = 25°C, with the ADC Clock at the stated speed, and represent most likely parametric norm.

TEST CIRCUIT DIAGRAMS

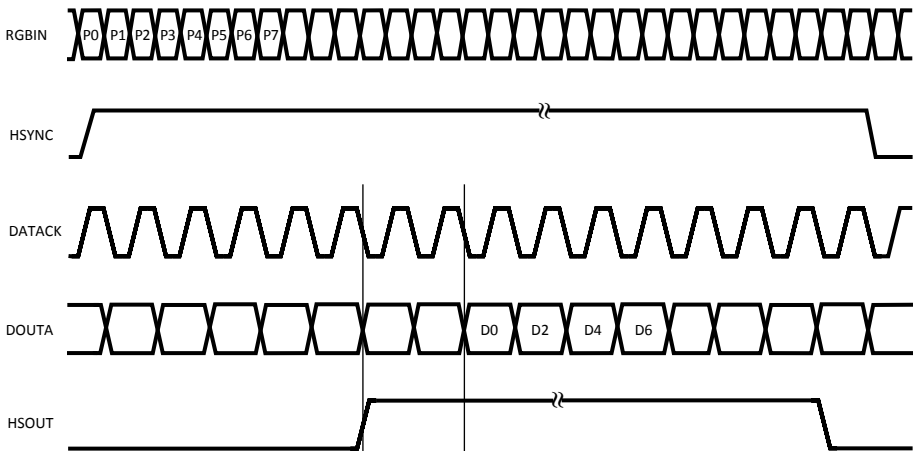
Timing Diagrams



Note 1) Absolute latency from HSYNC to HSOUT is not indicated or implied by this timing diagram. The latency may change by plus or minus one pixel period due to adjustments in the sampling phase register. The latency may also change by plus or minus one pixel period if the input signal is removed and reapplied, or if the ADCS9888 power is removed, and then reapplied, even if the same register settings are loaded.

Note 2) Based upon the relationship of the input HSYNC to P0, the D0 pixel may arrive one pixel earlier or later than shown on the diagram.

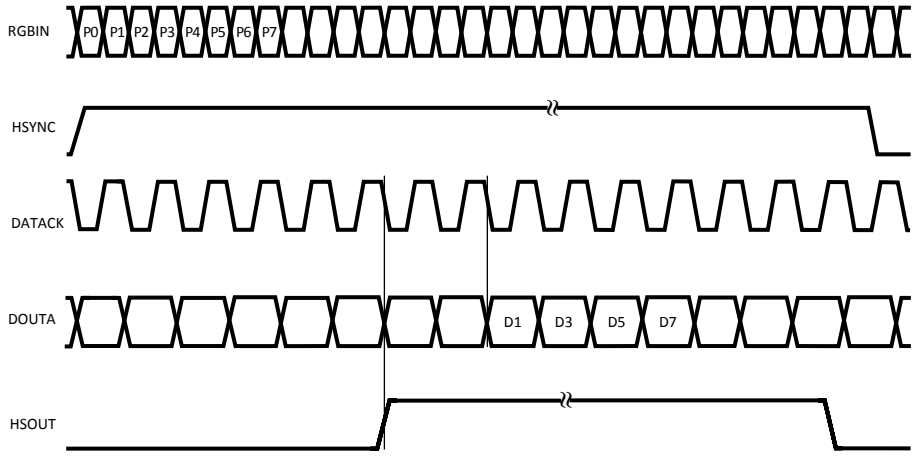
Figure 1. Single Channel Mode



Note 1) Absolute latency from HSYNC to HSOUT is not indicated or implied by this timing diagram. The latency may change by plus or minus one pixel period due to adjustments in the sampling phase register. The latency may also change by plus or minus one pixel period if the input signal is removed and reapplied, or if the ADCS9888 power is removed, and then reapplied, even if the same register settings are loaded.

Note 2) Based upon the relationship of the input HSYNC to P0, the D0 pixel may arrive one pixel earlier or later than shown on the diagram.

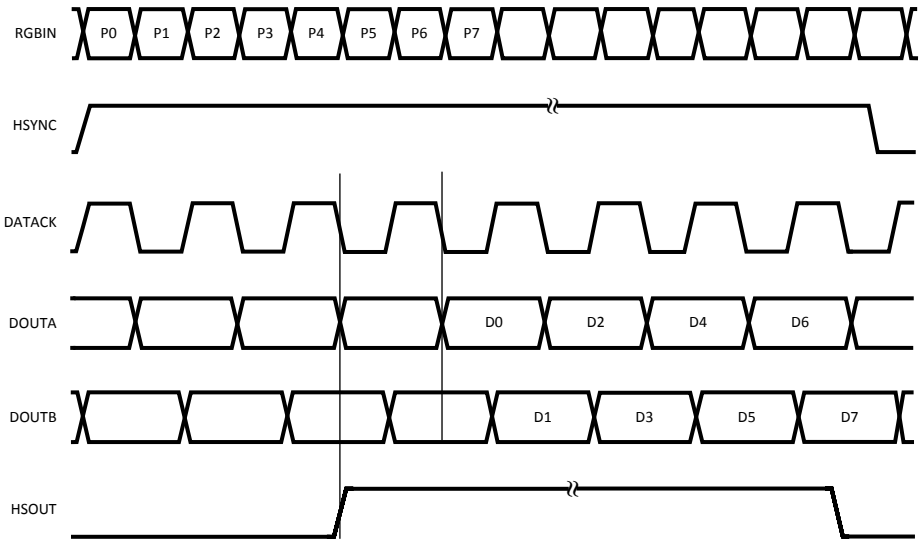
Figure 2. Single Channel Mode - 2 Pixels per Clock (Even Pixels)



Note 1) Absolute latency from HSYNC to HSOUT is not indicated or implied by this timing diagram. The latency may change by plus or minus one pixel period due to adjustments in the sampling phase register. The latency may also change by plus or minus one pixel period if the input signal is removed and reapplied, or if the ADCS9888 power is removed, and then reapplied, even if the same register settings are loaded.

Note 2) Based upon the relationship of the input HSYNC to P0, the D0 pixel may arrive one pixel earlier or later than shown on the diagram.

Figure 3. Single Channel Mode - 2 Pixels per Clock (Odd Pixels)

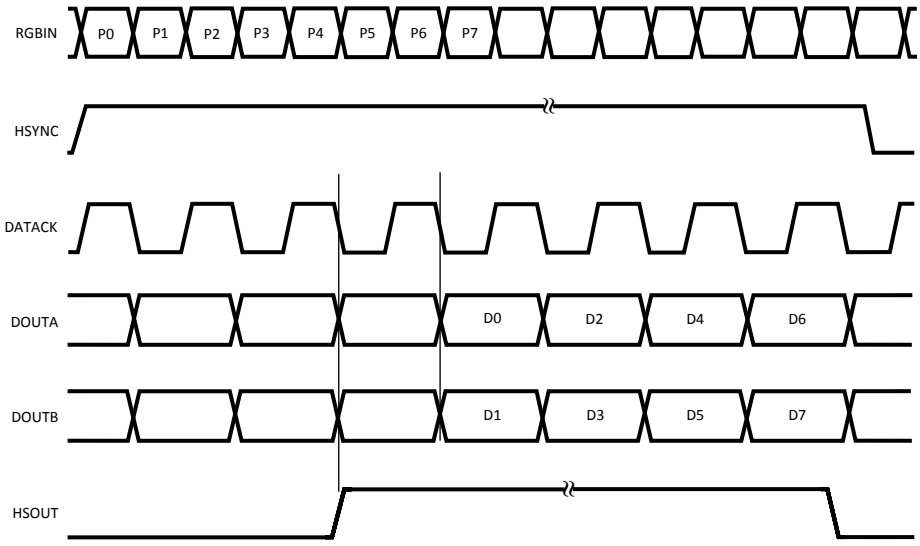


Note 1) Absolute latency from HSYNC to HSOUT is not indicated or implied by this timing diagram. The latency may change by plus or minus one pixel period due to adjustments in the sampling phase register. The latency may also change by plus or minus one pixel period if the input signal is removed and reapplied, or if the ADCS9888 power is removed, and then reapplied, even if the same register settings are loaded.

Note 2) Based upon the relationship of the input HSYNC to P0, the D0 pixel may arrive one pixel earlier or later than shown on the diagram.

Note 3) If Register 15H, Bit 5 is set to 1, HSOUT transitions on the rising edge of DATACK instead of the falling edge.

Figure 4. Dual Channel Mode - Interleaved Outputs

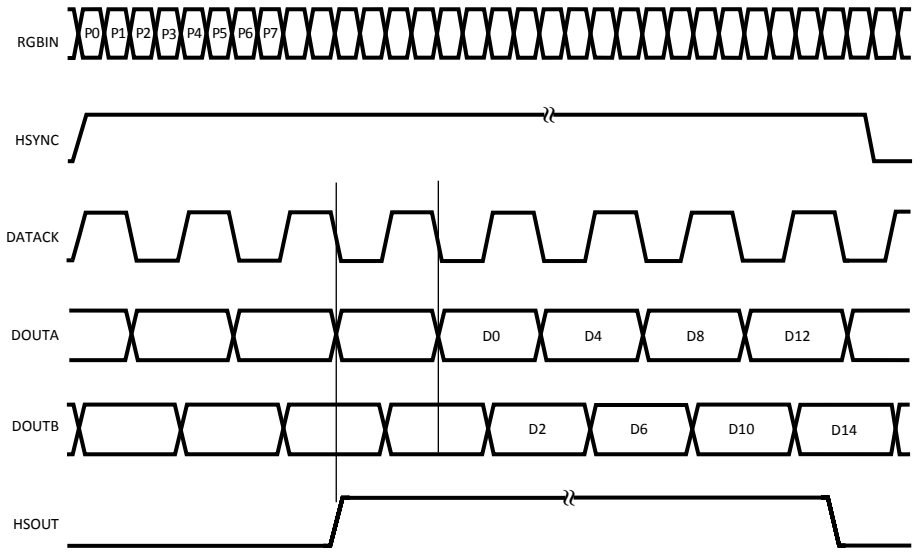


Note 1) Absolute latency from HSYNC to HSOUT is not indicated or implied by this timing diagram. The latency may change by plus or minus one pixel period due to adjustments in the sampling phase register. The latency may also change by plus or minus one pixel period if the input signal is removed and reapplied, or if the ADCS9888 power is removed, and then reapplied, even if the same register settings are loaded.

Note 2) Based upon the relationship of the input HSYNC to P0, the D0 pixel may arrive one pixel earlier or later than shown on the diagram.

Note 3) If Register 15H, Bit 5 is set to 1, HSOUT transitions on the rising edge of DATACK instead of the falling edge.

Figure 5. Dual Channel Mode - Parallel Outputs

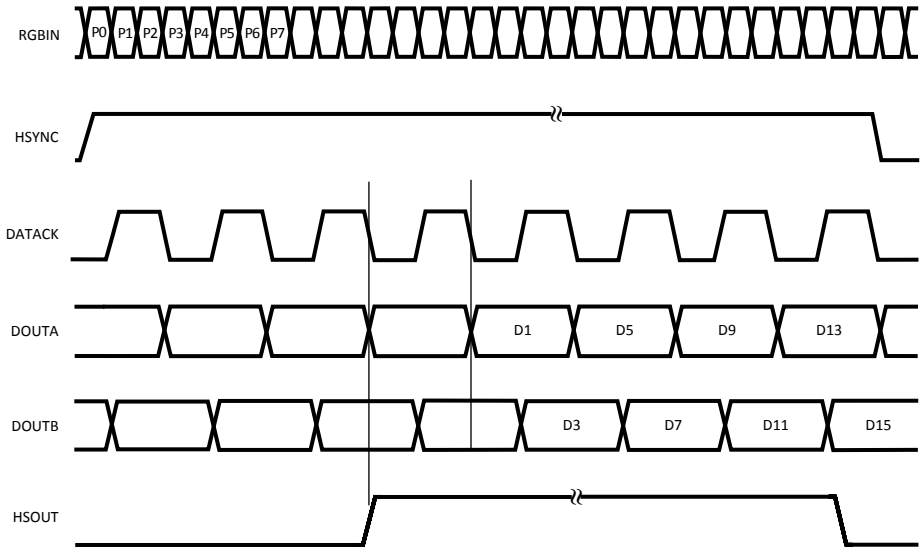


Note 1) Absolute latency from HSYNC to HSOUT is not indicated or implied by this timing diagram. The latency may change by plus or minus one pixel period due to adjustments in the sampling phase register. The latency may also change by plus or minus one pixel period if the input signal is removed and reapplied, or if the ADCS9888 power is removed, and then reapplied, even if the same register settings are loaded.

Note 2) Based upon the relationship of the input HSYNC to P0, the D0 pixel may arrive one pixel earlier or later than shown on the diagram.

Note 3) If Register 15H, Bit 5 is set to 1, HSOUT transitions on the rising edge of DATACK instead of the falling edge.

Figure 6. Dual Channel Mode - Interleaved Outputs - 2 Pixels/Clock - Even Pixels

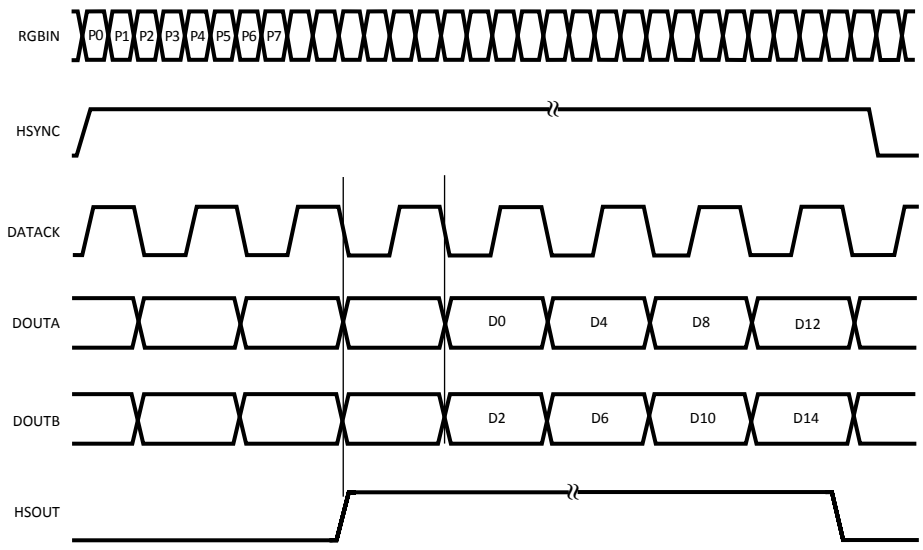


Note 1) Absolute latency from HSYNC to HSOUT is not indicated or implied by this timing diagram. The latency may change by plus or minus one pixel period due to adjustments in the sampling phase register. The latency may also change by plus or minus one pixel period if the input signal is removed and reapplied, or if the ADCS9888 power is removed, and then reapplied, even if the same register settings are loaded.

Note 2) Based upon the relationship of the input HSYNC to P0, the D0 pixel may arrive one pixel earlier or later than shown on the diagram.

Note 3) If Register 15H, Bit 5 is set to 1, HSOUT transitions on the rising edge of DATACK instead of the falling edge.

Figure 7. Dual Channel Mode - Interleaved Outputs - 2 Pixels/Clock - Odd Pixels

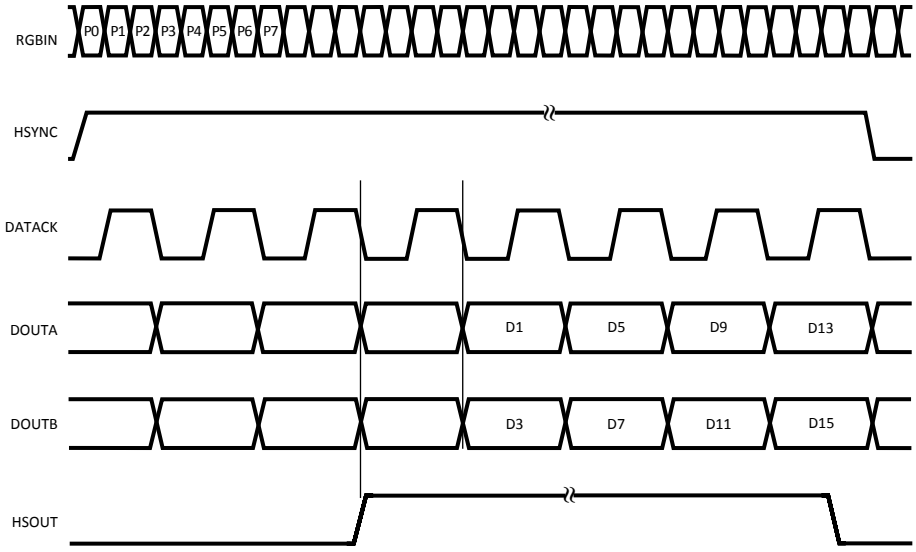


Note 1) Absolute latency from HSYNC to HSOUT is not indicated or implied by this timing diagram. The latency may change by plus or minus one pixel period due to adjustments in the sampling phase register. The latency may also change by plus or minus one pixel period if the input signal is removed and reapplied, or if the ADCS9888 power is removed, and then reapplied, even if the same register settings are loaded.

Note 2) Based upon the relationship of the input HSYNC to P0, the D0 pixel may arrive one pixel earlier or later than shown on the diagram.

Note 3) If Register 15H, Bit 5 is set to 1, HSOUT transitions on the rising edge of DATACK instead of the falling edge.

Figure 8. Dual Channel Mode - Parallel Outputs - 2 Pixels/Clock - Even Pixels

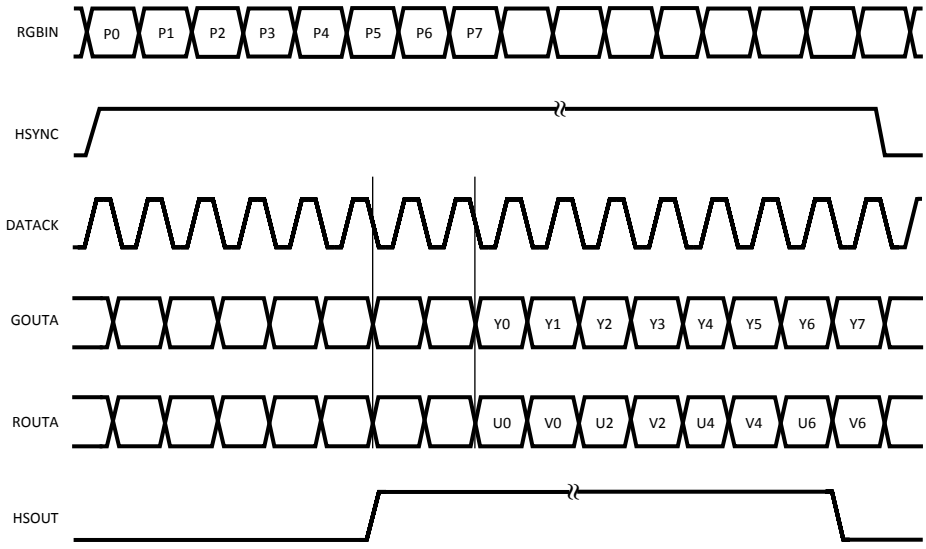


Note 1) Absolute latency from HSYNC to HSOUT is not indicated or implied by this timing diagram. The latency may change by plus or minus one pixel period due to adjustments in the sampling phase register. The latency may also change by plus or minus one pixel period if the input signal is removed and reapplied, or if the ADCS9888 power is removed, and then reapplied, even if the same register settings are loaded.

Note 2) Based upon the relationship of the input HSYNC to P0, the D0 pixel may arrive one pixel earlier or later than shown on the diagram.

Note 3) If Register 15H, Bit 5 is set to 1, HSOUT transitions on the rising edge of DATACK instead of the falling edge.

Figure 9. Dual Channel Mode - Parallel Outputs - 2 Pixels/Clock - Odd Pixels



Note 1) Absolute latency from HSYNC to HSOUT is not indicated or implied by this timing diagram. The latency may change by plus or minus one pixel period due to adjustments in the sampling phase register. The latency may also change by plus or minus one pixel period if the input signal is removed and reapplied, or if the ADCS9888 power is removed, and then reapplied, even if the same register settings are loaded.

Note 2) Based upon the relationship of the input HSYNC to P0, the D0 pixel may arrive one pixel earlier or later than shown on the diagram.

Figure 10. 4:2:2 Output Mode

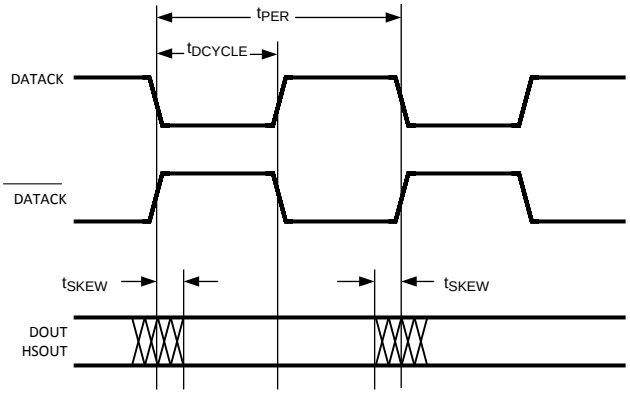


Figure 11. Data Output Timing

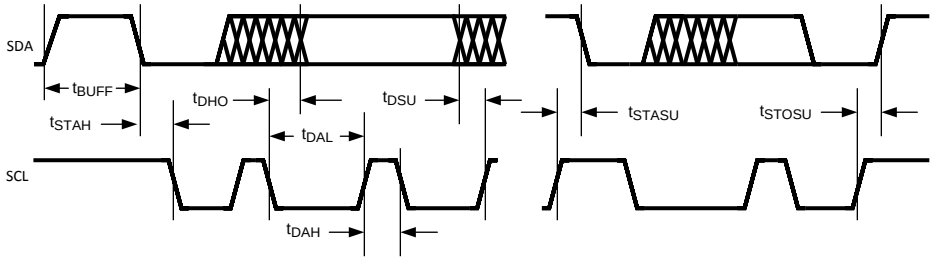


Figure 12. Configuration Register Serial Timing

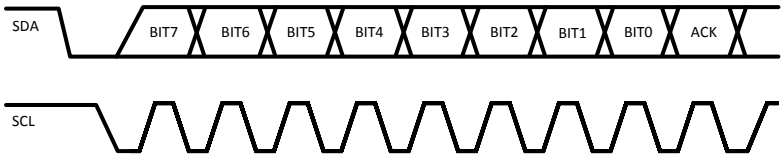


Figure 13. Serial Interface Protocol

Configuration Register Descriptions

Address (Hex)	Write/Read or Read Only	Bits	POR Value	Name	Bit Name/Description
00H	RO	7:0	Revision	Chip Revision	8 bit value that indicates the silicon version. 00000000 = Rev. 0
01H	W/R	7:0	01101001	PLL Divisor MSB	The upper 8 MSBs of the 12 bit PLL divider value. Larger divisors cause the PLL to generate a higher frequency clock. This register should be loaded first, then register 02H, whenever the divider is changed. The PLL divider value is only updated when the LSB value in register 02H is updated. The actual PLL divider value = (PLL register value + 1), so setting a value of 1055d in registers 01H and 02H will result in a divide value of 1056.
02H	W/R	7:4	1101****	PLL Divisor LSB	Lower 4 LSBs of the 12 bit PLL divisor value. See register 01H.

Address (Hex)	Write/Read or Read Only	Bits	POR Value	Name	Bit Name/Description
03H	W/R	7:6	01******	VCO RNG/CPMP	Sets the VCO frequency range for the desired pixel rate. 00 = 15 - 41 MHz 01 = 41 - 82 MHz 10 = 82 - 150 MHz 11 = 150+ MHz
		5:3	**001***		Sets the VCO charge pump current for the desired pixel rate. 000 = 50 µA 001 = 100 µA 010 = 150 µA 011 = 250 µA 100 = 350 µA 101 = 500 µA 110 = 750 µA 111 = 1500 µA
04H	W/R	7:3	10000***	Sample Phase Adjust	5 bit value that adjusts the ADC sample timing relative to HSYNC. LSB = 1/32 of one pixel period or 11.25 degrees of phase. The power up default value is 16D.
05H	W/R	7:0	00001000	Clamp Placement	Sets the Clamp starting point N pixel periods after the trailing edge of the Hsync signal. Settings from 1 to 255 are legal values for Clamp Placement. DO NOT SET = 0.
06H	W/R	7:0	00010100	Clamp Duration	Sets the Clamp duration to N pixel periods. Settings from 1 to 255 are legal values. DO NOT SET = 0.
07H	W/R	7:0	00100000	HSOUT Pulsewidth	Sets the number of pixel periods that HSOUT is active. The leading edge of HSOUT is set by an internally generated phase-adjusted PLL output. The chip then counts the number of pixel periods set by HSOUT Pulsewidth and triggers the trailing edge of HSOUT.
08H	W/R	7:0	10000000	Red Gain	Controls the ADC input range for the RGB video inputs. Default setting provides a nominal signal range of 0.7 V_{PP}. Higher settings increase the signal range up to 1.0 V_{PP} typ. Lower settings reduce the signal range to a minimum of 0.5 V_{PP} typ.
09H	W/R	7:0	10000000	Green Gain	
0AH	W/R	7:0	10000000	Blue Gain	
0BH	W/R	7:1	1000000*	Red Offset	Controls the DC offset correction prior to analog to digital conversion. Default setting is for no offset. Settings higher than 10H make resulting image less bright, settings lower than 10H makes image more bright. Absolute offset amount is also dependent on setting of corresponding gain channel. See description of Offset/Gain functions for more information.
OCH	W/R	7:1	1000000*	Green Offset	
ODH	W/R	7:1	1000000*	Blue Offset	
OEH	W/R	7	0*******	Sync Control	Hsync Polarity Override. 0 = polarity determined by chip, 1 = polarity set by Register 0EH, bit 6.
		6	*1******		Hsync Input Polarity. 0 = active low, 1 = active high.
		5	**0*****		Hsync Output Polarity. 0 = logic high HSOUT, 1 = logic low HSOUT.
		4	***0****		Active Hsync Override. 1 = Hsync source determined by user setting in Register 0EH, bit 3. 0 = determined by chip results in Register 14H, bit 6.
		3	****0***		Active Hsync Select. 0 = HSYNC input is Hsync source. 1 = output of SOGIN sync slicer is Hsync source. This bit only takes effect if Register 0EH bit 4 is 1, or if both Hsync sources are active.
		2	*****0**		Vsync Output Invert. 0 = inverted. 1 = not inverted.
		1	******0*		Active Vsync Override. 1 = source determined by user setting in Register 0EH, bit 0. 0 = source determined by chip results in Register 14H, bit 3.
		0	*******0		Active Vsync Select. 0 = VSYNC input is Vsync source. 1 = Sync separator output is Vsync source. This bit only has effect if Register 0EH, bit 1 = 1.

Address (Hex)	Write/Read or Read Only	Bits	POR Value	Name	Bit Name/Description
0FH	W/R	7	0*******	Clamp Control	Clamp Select. 0 = clamp timing determined by internal chip counters derived from hsync. 1 = clamp timing determined by external CLAMP signal.
		6	*1******		CLAMP Polarity. 0 active high, 1 = active low. This bit only has effect if Register 0FH, bit 7 = 1.
		5	**0*****	COAST Control	COAST Select. 0 = COAST input pin is PLL coast source. 1 = VSYNC is PLL coast source.
		4	***0****		COAST Polarity Override. 0 = determined by chip. 1 = determined by Register 0FH, bit 3.
		3	****1***		COAST Polarity. 0 = active low, 1 = active high. This bit only has an effect when Register 0FH, bit 5 = 0, and Register 0FH bit 4 = 1.
		2	*****1**	Seek Override	Seek Mode Override. 0 = don't allow low power mode. 1 = allow low power mode when sync inputs inactive. In seek mode operation the HSOUT, VSOUT, DATACK and $\overline{\text{DATACK}}$, and all 48 data outputs are placed in a high impedance state. The SOGOUT pin is still active. The voltage references, sync detection and processing, and serial register sub-system (for obvious reasons) are maintained in an active state to provide a rapid transition to normal operation.
		1	******1*	$\overline{\text{PWRDN}}$	Full chip power down. 0 = power down. 1 = normal operation. In power down mode, the HSOUT, VSOUT, DATACK, $\overline{\text{DATACK}}$, and all 48 data outputs are placed in a high impedance state. The SOGOUT pin is still active. The voltage reference, sync detection and processing, and serial register sub-system (for obvious reasons) are maintained in an active state to provide a rapid transition to normal operation.
10H	W/R	7:3	01111***	Sync-On-Green Threshold	Set the voltage of the sync slicer threshold. 00H to 1FH. LSB size is 10 mV. Setting of 00h gives a nominal threshold of 10 mV, while maximum setting of 1FH gives a nominal threshold of 330 mV. Optimal settings will be lower than those used with the Analog Devices AD9888.
		2	*****0**	Red Clamp Select	0 = clamp to ground. 1 = clamp to $R_{MIDSC}V$.
		1	******0*	Blue Clamp Select	0 = clamp to ground. 1 = clamp to $B_{MIDSC}V$.
11H	W/R	7:0	00100000	Sync Separator Threshold	Sets how many internal 5 MHz clock periods the sync separator will count to before toggling high or low. This value should be set to some amount greater than the widest expected hsync or equalization pulse width.
12H	W/R	7:0	00000000	Pre-coast	Sets the number of Hsync periods that the PLL coast becomes active prior to Vsync. This setting is only valid when Vsync is used as the PLL coast source.
13H	W/R	7:0	00000000	Post-Coast	Sets the number of Hsync periods that the PLL coast stays active after Vsync becomes inactive. This setting is only valid when Vsync is used as the PLL coast source.

Address (Hex)	Write/Read or Read Only	Bits	POR Value	Name	Bit Name/Description
14H	RO	7		Sync Detect Status	Hsync Detect. 1 = activity is detected on the HSYNC input pin. 0 = no activity detected.
		6			AHS - Active Hsync Select. The bit indicates which Hsync source will automatically be used by the chip. 0 = HSYNC input pin. 1 = output of sync slicer. This can be overridden by asserting the Active Hsync Override bit at Register 0EH, bit 4 and setting the Hsync source at Register 0EH, bit 3.
		5			Input Hsync Polarity Detect. 0 = active low. 1 = active high.
		4			Vsync Detect. 1 = activity is detected on the VSYNC input pin. 0 = no activity detected.
		3			AVS - Active Vsync Select. This bit indicates which Vsync source will automatically be used by the chip. 0 = VSYNC input pin. 1 = output of sync separator. This can be overridden by asserting the Active Vsync Override bit at Register 0EH, bit 1 and setting the Vsync source at Register 0EH, bit 0.
		2			VSOUT Polarity Detect. 0 = active high, 1 = active low.
		1			SOGIN Activity Detect. This bit indicates if there is activity at the output of the sync slicer. 0 = no activity. 1 = activity detected.
		0			Coast Polarity Detect. This bit indicates the polarity of the signal being applied to the PLL coast function. 0 = active low, 1 = active high.
15H	W/R	7	1*******	Channel Mode	Sets the channel mode of the data outputs. 0 = single channel mode. 1 = dual channel mode. In dual channel mode, the DATACK output clocks operate at 1/2 of the pixel conversion rate, and pixel data is updated on the A and B output ports. See also Register 15H, bit 6.
		6	*1******	Output Mode	Sets the output mode of the data outputs. 0 = interleaved mode, 1 = parallel mode. In interleaved mode, one output port is updated on the rising edge of DATACK, the other output port is updated on the falling edge of DATACK.
		5	**0*****	A/B Even/Odd	When this bit is set to 1, HSOUT transitions on the rising edge of DATACK. (Instead of the falling edge as shown in the timing diagrams).
		4	***0****	4:2:2 Output Mode	Selects 4:2:2 subsampled output formatting mode, for use with YUV type video signals. 0 = normal output formatting, 1 = 4:2:2 output formatting. In YUV 4:2:2 mode, the channel connections and data output are as follows:
					Channel / **Input Signal** / **Output** Red / V / U/V Green / Y / Y Blue / U / High Z
		3	****0***	Input Mux	Selects which video input source is used. 0 = port 0, 1 = port 1.
		2:1	*****11*	Input Bandwidth	Sets the analog input bandwidth. 11 = 500 MHz 10 = 300 MHz 01 = 150 MHz 00 = 75 MHz
		0	*******0	External Clock	Determines whether the internal Hsync referenced PLL is used as the clock source, or the CKEXT source is used. 0 = internal PLL. 1 = CKEXT is used.
16H	W/R	7:0	11111111	Test Register	
17H	W/R	7:0	00000000	Test Register	
18H	RO	7:0		Test Register	
19H	RO	7:0		Test Register	

Application Information

1.0 INTRODUCTION

The ADCS9888 is a complete 8 bit, 205 MSPS monolithic analog front end for capturing analog component video in digital video applications. The high sampling rate allows it to support video capture at full frame rate at resolutions up to 1600 by 1200 at 75 Hz. Higher resolution (and therefore pixel rate) video can be captured by subsampling even and odd columns (pixels) of video on alternating frames.

This highly integrated solution incorporates all of the functions necessary to convert standard computer video signals into digital output data suitable for acquisition by video scaler and similar processing systems. Included components are a 2 channel mux to allow 2 independent video sources to be selected. A full sync processing and clock generation system is included to generate the sampling pixel clock based on the horizontal synchronization signal. 3 inputs with 500 MHz bandwidth are used to capture component RGB or YUV video data. Video clamp circuitry is included to provide the proper AC coupling and black level restoration required in this application. Video is captured at up to 205 MSPS by 8 bit analog to digital converters, and output to a highly flexible output interface. Data can be output on a single 8 bit parallel output per channel, or on dual 8 bit parallel interfaces for each color channel for the higher pixel rate settings. A variety of different output formats are supported to ensure flexible interfacing to a variety of video processing solutions.

2.0 VIDEO SIGNAL PATH

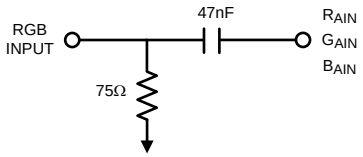
2.1 Input Muxes

The ADCS9888 supports two complete video input channels #0 and #1. This allows two sources of video input to be used for dual input panels, monitors and projectors. All analog video signals and sync signals are muxed.

2.2 Input Termination

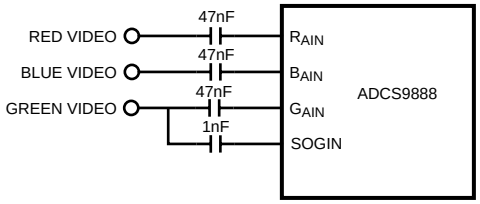
Video input signals are normally received from 75Ω sources. In this case, the signal path should be properly impedance matched through the incoming connectors, and across the printed circuit board up to the video inputs on the ADCS9888. The signal traces should be designed for the proper characteristic impedance, and should be continuous traces that stay on the same side of the printed circuit board, avoiding vias and sharp bends in the trace that can introduce impedance discontinuities.

The 75Ω/47 nF termination network shown should be located as close as possible to the video input pins to minimize unmatched stub impedances and resulting signal distortion. The 75Ω termination resistance should be connected to the system ground plane using a via directly to the plane.



2.3 Video Input Clamp

The analog video inputs will be AC coupled using 47 nF capacitors. Clamping on the inputs is done to ensure the proper DC level of the converted signals. Red, Green and Blue channels will normally be clamped to the zero scale level of the ADC when a black level signal is present on the inputs. This normally happens during the back porch period of the horizontal blanking interval. Register controlled options allow the Red and Blue channels to be clamped to the ADC mid scale point. This allows YUV signal processing where the U and V channels are at a mid scale voltage during “Black”.



2.4 Gain/Offset Adjustment

Gain and Offset adjustment is provided to support video signal ranges of 0.5 Vp-p to 1.0 Vp-p.

When the 8 bit Gain registers are set to the maximum value, the signal range is largest at 1.0 Vp-p typical. When the Gain registers are set to the minimum values of 00h, the signal range is smallest at 0.5 Vp-p. This means that for a given video input signal, maximum settings of Gain will reduce the contrast or range of the converted data, while minimum settings of Gain will increase the contrast or range of the converted data. The "power on defalt" values for Gain are 80h which give a nominal input range of 0.7 Vp-p.

The 7 bit Offset registers provide a ±63 step adjustment. High values of Offset will lower the value of the converted output data, low values of Offset setting will increase the value of the converted output data.

As the Gain and Offset adjustments cause the ADC reference voltages to change, they also cause shifts in the RMIDSCV and BMIDSCV voltages.

2.5 Analog To Digital Converter

Three 8 bit, 205 MSPS analog to digital converters are included. One for each video input channel.

2.6 Output Data Ports

Two 8 bit data ports are provided at the output of each video color channel. This allows a variety of different video output formats for ease of processing by the attached video scaler/processor used in different applications.

Supported modes include:

- Single channel mode, where all data is present on the A output port for each color channel.
- Parallel Dual Channel mode, where data is presented on A and B outputs simultaneously, updated at one half the pixel conversion rate.
- Interleaved Dual Channel mode, where data is presented alternately on A and B outputs one new sample with each incoming pixel clock.
- In both Dual Channel modes, the output data sequence can be altered to provide all Odd pixels on Port B or on Port A, controlled by Bit 5 of Register 15h.

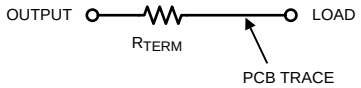
The timing relationship between the data outputs, output clocks, and HSOUT are all synchronized. When the sample phase is adjusted, all of these digital outputs will be shifted together with respect to the source Hsync signal.

In dual channel output modes, if Register 15H, Bit 5 is set to one, then HSOUT will transition on the rising edge of DATACK instead of the falling edge as shown in the timing diagrams.

All DATA and DATACK outputs are placed in high impedance tri-state mode when the chip is in power down. No pull-up or pull-down features are present in the high impedance state. Refer to the specific sections regarding the other logic outputs for their configuration during power down or low power modes of chip operation.

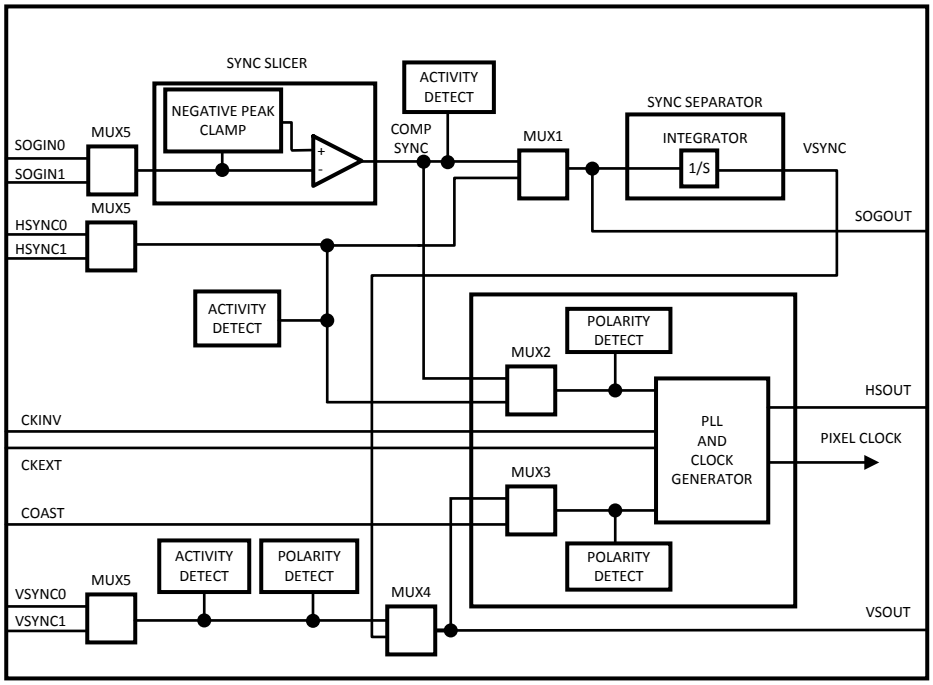
2.6.1 Output Termination

All data and timing outputs are high speed CMOS drivers and should be properly terminated to reduce EMI and optimize signal integrity. Each output should have a series terminating resistor located as close to the output pin as possible. The value of the terminating resistor is dependant on the printed circuit board trace impedance. The optimum performance will be when the output impedance of the chip plus the terminating resistor is equal to the characteristic impedance of the printed circuit board trace. Typical output impedance of the ADCS9888 SOGOUT, DATACK and DATACKB is around 30Ω, while the HSOUT, VSOUT and DATA are 90Ω. So for a 150Ω trace impedance, the optimum terminating resistor values would be 120Ω and 60Ω respectively.



$$Z_{OUTPUT} + R_{TERM} = Z_{TRACE}$$

3.0 SYNC INPUTS AND PROCESSING



3.1 SYNC On Green Input

The Sync-On-Green input is provided to support applications where separate TTL Hsync and Vsync inputs are not provided. In these applications, the composite sync information is provided on the Green video signal. The SOG input accepts an AC coupled version of the green input signal. This signal is clamped, and then further processed to extract the horizontal and vertical sync signals.

3.1.1 Sync Slicer

The Sync Slicer is an adjustable clamp/comparator. First the input is clamped so that the most negative voltage is set to equal an internal reference voltage. This clamped signal is then fed into a 5 bit adjustable comparator to provide a logic level signal with the analog video data removed and only the sync signals remaining. The default comparator setting is 160 mV above the reference voltage. Adjustment increments are in 10 mV intervals with a resulting comparator range from 10 mV to 330 mV.

Optimal settings will be lower than those used with the Analog Devices AD9888. The recommended starting value is a setting of 01111b, but the best setting is dependent on amplitude of the input video signal and synchronizing pulse.

The Sync Slicer output has the same polarity as the input signal. “Normal” video with white positive and black negative will produce sync pulses that are active low. Normal synchronization signals will be mainly high with pulses going low.

The Sync Slicer circuit will provide an active logic output from many signals which do not have sync on green present. Video with no Sync On Green signal present will still cause the output of the Sync Slicer circuit to toggle. The timing of this output will be much different than that caused by a signal where Sync On Green information is included. In addition, when no Sync On Green information is present, timing will always be provided on the VSYNC and/or HSYNC timing inputs.

3.1.2 Sync on Green Activity Detect

The SOGIN activity detect circuit detects the absence or presence of a signal at the output of the Sync Slicer. The result of this detection is sent to Register 14h, Bit 1. (1 = Active, 0 = Inactive)

3.2 HSYNC Input

In most computer video applications, a TTL horizontal sync pulse is output by the graphics card. This TTL signal is connected to the ADCS9888 HSYNC input. In other applications a TTL composite sync signal may be used. To support this, the composite sync signal from the HSYNC input can be processed by the Sync Separator circuit to generate a Vsync signal. Either Hsync signal (from HSYNC input or from SOGIN via the Sync Slicer) can be used as the reference clock for the PLL in the clock generation block.

3.2.1 HSYNC Activity Detect

The HSYNC activity detect circuit detects the absence or presence of an HSYNC input signal. The result of this detection is sent to Register 14h, Bit 7. (1 = Active, 0 = Inactive)

3.2.2 AHS - Active HSYNC Selection

The Clock Generator will use either the HSYNC input, or the output from the Sync Slicer as the reference for the PLL. The AHS performs an automatic selection of the PLL reference source based on the following table:

Reg. 14h Bit 7 Hsync Detect	Reg. 14h Bit 1 SOG Detect	Reb. 0Eh Bit 4 Override	AHS Output
0	0	0	0 – use HSYNC
0	1	0	1 – use SOG
1	0	0	0 – use HSYNC
1	1	0	0Eh, Bit 3
X	X	1	0Eh, Bit 3

3.2.3 Hsync Polarity Detection

The Hsync signal input to the Clock Generator can be an active high or active low signal. A polarity detection circuit is used to detect the state of the Hsync signal. Signals that are mostly low with pulses high will be reported as active high or positive, while signals that are mostly high with pulses low will be reported as active low or negative. The results of this detection are reported in Register 14h, Bit 5. (0 = Negative, 1 = Positive).

Regardless of the polarity of the Hsync signal at the detector, an automatic polarity correction circuit is used to ensure that the proper polarity signal is used to drive the PLL reference clock input.

3.3 SYNC Separator

Either the SOGIN or HSYNC signals can have a composite sync signal as the input. MUX1 is used to feed this composite sync from either source into the sync separator. The sync separator is a digital low pass filter that has an adjustable number of clock ticks from 0 to 255. The default setting is 32 ticks. This filter rejects changes in the composite sync signal that are shorter than the period set. Thus, only long duration changes in the digital composite sync signal, i.e. the vertical sync pulse, are allowed to pass through. The separator uses an internal clock with a nominal frequency of 5 MHz as the filter timebase.

3.4 VSYNC Input

The VSYNC input accepts a TTL vertical sync pulse provided by the video source. This signal or the vertical sync signal output by the Sync Separator can be used to control the Coast function in the clock generation circuitry.

3.4.1 Vsync Activity Detect

The Vsync activity detect circuit detects the absence or presence of a Vsync input signal. The result of this detection is sent to Register 14h, Bit 4. (1 = Active, 0 = Inactive).

3.4.2 Vsync Polarity Detect

The Vsync signal can be an active high or active low signal. A polarity detection circuit is used to detect the active state. The polarity is determined by observing the high/low duty cycle of the VSOUT signal to determine whether the signal is mostly high or mostly low. If the signal is mostly low, then the polarity is set as Positive. If the signal is mostly high, then the polarity is set to Negative. (0 = Negative, 1 = Positive) The results of this detection are sent to Register 14h, Bit 2.

3.4.3 AVS - Active Vsync Detection

There are two possible signal sources for VSOUT. The Vsync input can be used, or the output of the SYNC SEPARATOR can be used. The AVS automatically selects the source for VSOUT based on the results and settings described in the following table.

Reg. 14h Bit 4 Vsync Detect	Reg. 14h Bit 1 SOG Detect	Reg. 0Eh Bit 1 Override	AHS Output
0	0	0	Reg 0Eh, Bit 0
0	1	0	1 – use SOG
1	0	0	0 – use VSYNC
1	1	0	0 – use VSYNC
X	X	1	Reg 0Eh, Bit 0

4.0 CLOCK GENERATION

The PLL clock generator provides a high frequency pixel clock that is phase aligned to the horizontal sync signal. The horizontal sync signal can be provided by the HSYNC input, or the output of the sync slicer circuit. The pixel clock is used as the timing source for the analog to digital conversion and data output processing in the IC.

4.1 PLL

The PLL generates a high frequency pixel clock that is frequency locked and phase aligned to the horizontal sync signal.

The main controls for the PLL are as described in the following subsections.

4.1.1 PLL Divider

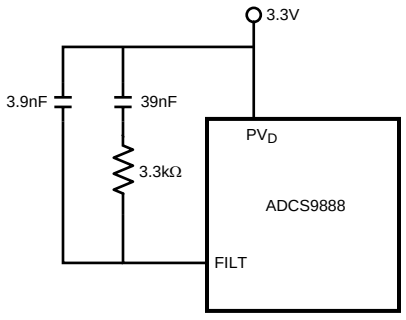
The PLL divider is a 12 bit counter with an adjustment range of 17 to 4096. The divider setting is configured in registers 01h, and 02h. The actual divider value used is the divider register setting + 1, so loading a value of 1055 decimal results in a divider of 1056. The PLL divider value sets the number of pixel periods per line. This value consists of the active video pixels, plus the horizontal blanking overhead. The overhead is typically 20 to 30% of the total line time.

VESA (Video Equipment Standards Association) has established a series of standards for the different computer video settings (resolution and frame rate). These can be used to determine the proper settings of the PLL divider for many applications. Some applications will use non-standard video timings. In these cases, more advanced methods will be required to determine the proper divider setting to use.

The power up default value of the PLL divide registers is 1693d for a real divider setting of 1694d.

4.1.2 VCO Filter Circuit

The Voltage Controlled Oscillator uses an external filter circuit to smooth the charge pump current pulses, and optimize the VCO performance. This circuit connects between the FILT pin and PVD power bus. The filter circuit, and the PVD power must be well isolated from other circuitry to achieve the best PLL performance and low jitter.



4.1.3 VCO Frequency Range Control

The VCO frequency range setting selects the gain of the VCO. By optimizing the gain, the VCO performance can be optimized for different operating frequency ranges. The value is set via the two most significant bits of register 03h.

PV1	PV0	Pixel Clock Range (MHz)	K_{VCO} Gain (MHz/V)
0	0	15-41	31
0	1	41-82	61
1	0	82-150	122
1	1	>150	200

4.1.4 VCO Charge Pump Current Control

The PLL charge pump current can be set to different values to help optimize the performance for different frequency ranges of operation. The value is set via bits 5:3 of Register 03h.

IP2	IP1	IP0	Charge Pump Current (µA)
0	0	0	50
0	0	1	100
0	1	0	150
0	1	1	250
1	0	0	350
1	0	1	500
1	1	0	750
1	1	1	1500

The VCO charge pump current can be calculated using the following equation, and the values for Kvco from the table in the previous section.

Ip = [(HsyncFreq x 2 x π)/19.2]^2 x [(Ct x N)/Kvco)]

where

- Ip = Target Charge Pump current. Round this value up to the next highest available setting
- HsyncFreq = Frequency of Hsync reference clock
- π = 3.1415927 (approximately)
- 19.2 = The PLL stability ratio for the ADCS9888
- Ct = Loop filter capacitance
- N = PLL divider value (register setting in 04h, 05h +1)
- Kvco = VCO gain in MHz/V (1)

4.1.5 PLL Coast

The PLL clock generator provides a high frequency pixel clock that is phase aligned to the horizontal sync signal. During portions of the video signal, this horizontal sync signal may be absent or may have a frequency that is different than the "normal" frequency. During these times, application of the coast signal to the PLL causes it to maintain its current operating frequency and phase (according to the voltage held on the VCO filter capacitor) and “coast”, without attempting to synchronize with the horizontal sync waveform. When the coast signal is de-asserted, the PLL will again try to phase lock with the horizontal sync input.

In most applications, the coast signal is derived from the vertical synchronization pulse from the VSYNC input or from one of the composite sync sources (either SOGIN or HSYNC) after being processed in the sync separator.

The COAST input allows the user to provide a separate external coast control signal. Register 0Fh, bit 5 is used to select which source is used.

4.1.6 Pre-Coast and Post-Coast

When Vsync is used as the coast source, the coast signal can be extended earlier and later by setting the Pre-Coast and Post-Coast settings in Registers 12h and 13h. This feature requires the chip to calculate the number of Hsync pulses (lines) per Vsync (frame). An 11 bit counter is provided to support frame sizes up to 2048 lines (active lines plus vertical blanking overhead).

Once the frame size has been calculated, the chip will anticipate when the next VSYNC begins, and the coast signal can be generated up to 255 lines earlier than the anticipated Vsync. Similarly, the Post-coast setting allows the PLL coast signal to be maintained as many as 255 lines following the de-assertion of Vsync.

4.1.7 Coast Polarity Detection

The coast signal input to the Clock Generator can be an active high or active low signal. A polarity detection circuit determines the polarity of the Coast signal. The polarity is determined by observing the high/low duty cycle of the COAST signal to determine whether the signal is mostly high or mostly low. If the signal is mostly low, then the polarity is set as Positive. If the signal is mostly high, then the polarity is set to Negative. (0 = Negative, 1 = Positive) The results of this detection are sent to Register 14h, Bit 0.

Table 1. Clock Generation Setting

Mode	Resolution (Pixel/Lines)	Refresh Rate Hz	HSYNC Frequency kHz	Pixel Rate MHz	VCO RNGE	VCO CPMP	PLL DIV Setting
VGA	640 x 480	60	31.5	25.175	00	010	799
		72	37.7	31.500	00	011	831
		75	37.5	31.500	00	011	839
		85	43.3	36.000	00	011	831
SVGA	800 x 600	56	35.1	36.000	00	011	1023
		60	37.9	40.000	00	011	1055
		72	48.1	50.000	01	011	1039
		75	46.9	49.500	01	011	1055
		85	53.7	56.250	01	011	1047
XGA	1024 x 768	60	48.4	65.000	01	011	1343
		70	56.5	75.000	01	100	1327
		75	60.0	78.750	01	100	1311
		80	64.0	85.500	10	011	1335
		85	68.3	94.500	10	011	1375
SXGA	1280 x 1024	60	64.0	108.000	10	011	1687
		75	80.0	135.000	10	101	1687
		85	91.1	157.500	11	100	1727
UXGA	1600 x 1200	60	75.0	162.000	11	100	2159
		65	81.3	175.500	11	100	2159
		70	87.5	189.000	11	100	2159
		75	93.8	202.500	11	101	2159
		85	106.3	229.500 *	10	101	1079

NOTE

* Alternate pixel sampling mode. See 4.2.1 CKINV Input

4.2 Pixel Clock Generation And Timing AdjustmenT

Several features are provided that are related to the pixel clock timing. These include:

- Clock Phase Adjust
- CKINV - This is discussed in more detail in the next section, “CKINV Input”.
- Clamp Placement setting

- Clamp Duration setting

Please refer to Configuration Register Descriptions for more details on these adjustments.

4.2.1 CKINV Input

This is a digital input that causes the ADC sampling clock to be inverted. In effect, this causes an additional 180 degrees of phase shift in the ADC sampling point. This input is used in support of Alternate Pixel Sampling mode, which allows higher frequency video signals to be captured. In this mode, only every second pixel is sampled and converted. This is easily achieved by setting the PLL divider value to achieve one half of the true video pixel rate. On one video frame, all odd video pixels will be converted and sent to the video processor. On the next video frame, the state of CKINV will be inverted, and all even pixels will be converted and output. Frame re-assembly and display will be performed by the video scaler or other video processing system.

This input should only change state during the vertical blanking interval, as it may produce several samples of corrupted ADC data during the phase shift. This input should be connected to ground when not in use.

4.2.2 CKEXT Input

While most applications will use the built in PLL to generate a pixel clock, in some cases, the user will drive the CKEXT input with an external pixel clock source. In these applications, the PLL is not used and will be placed in a minimum power state.

The ADC Sample Phase adjustment is available when CKEXT is used.

5.0 TIMING OUTPUTS

5.1 SOGOUT

This pin outputs either the output from the sync slicer, or a delayed but unprocessed version of the HSYNC input. The signal at SOGOUT is the same polarity as the input signal.

5.2 HSOUT

This pin outputs a reconstructed and phase aligned version of the HSYNC input. Both the polarity and duration of this signal are controlled via register settings.

5.3 VSOUT

This pin outputs a delayed but unprocessed (except for selectable inversion via register 0Eh, bit 3) version of the vertical sync signal. This signal can be selected from either the VSYNC input, or the output of the Sync Separator.

5.4 DATACK/DATACKB

These pins provide a complementary output pixel clock that will be used to capture the digital data and HSOUT into the connected digital logic. The output frequency of the clock is dependent on the data output mode being used. Refer to the description for register 15h.

6.0 CONFIGURATION REGISTERS

All device settings are controlled via the configuration registers. These registers are accessed via a serial control bus which consists of 3 inputs/outputs (Serial Data, Serial Clock and A0).

6.1 Serial Control Interface

The serial control interface consists of a bi-directional Data line and an input only Clock line. All clock information is controlled by the Master or Host device, which will usually be a microcontroller or microprocessor. The data line will be driven by the Master or Host during the control/address portions of the protocol. Data portions of the transfer can be driven by either the Master or the ADCS9888, depending on the direction of data flow. The two bus lines will have pullup resistors to a power supply bus, and all devices connected to the bus will use open-drain drivers to activate the clock and data lines. This allows multiple Master and Slave devices to coexist on the same serial interface without bus contention.

6.2 Serial Protocol

The serial protocol is made up of a number of basic protocol elements. A typical transaction will consist of:

- Start Signal
- (Slave Address + Read/Write Bit) Byte
- Base Register Address Byte
- Data Byte
- Stop Signal

6.2.1 Start Signal

Initially, when the bus is inactive, both SCL and SDA will be in a high logic state. A start signal consists of the SDA line transitioning from high to low, while the SCL line remains high.

6.2.2 Stop Signal

When the bus is active, the data line will normally be high or low, and the clock will transition from low, to high, then return to low, to register the next bit in the sequence. A stop signal consists of the SDA line transitioning to a low state, followed by the SCL line transitioning to a high state, followed by the SDA line transitioning to the high state.

6.2.3 Repeat Start Signal

A repeat start occurs in a sequence where a slave address and base address have already been transferred, but the mode of communications will be changing from Write to Read. This occurs during Read operations, since any Read operation first begins with a Write to specify the base register address.

6.2.4 Slave Address BYTE

The slave address byte is used to distinguish between the different devices that may be connected to a common serial bus. Devices have a 7 bit address, with many devices having some bits configurable via external pin connections. The ADCS9888 address byte is configured as follows:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	1	1	0	A0 Pin	0

6.2.5 Register Address BYTE

ADCS9888 register addresses are an 8 bit value. Please refer to the Register Address table at the beginning of the datasheet for more detailed information.

6.2.6 Serial Interface Timeout

The serial interface incorporates a timeout feature. This is present to ensure that the bus cannot become ‘locked’ if the master and slave become out of sync due to noise or other system issues.

An internal timer is used to ensure that the interface is reset if the SCL line is held low. This is used to prevent problems in the case where the ADCS9888 is driving a low on the SDA line and the master device is reset. This allows the master to reset the state of the serial interface on the ADCS9888 by simply driving a low on SCL for more than 50 ms.

The serial bus interface circuitry will be reset to the idle state if the SCL line is held low for more than 50 ms. The bus may be reset to idle if the SCL line is held low from 25 to 50 ms. The bus will not be reset if the SCL line is held low for less than 25 ms.

6.3 Specific Types Of Transfers

6.3.1 Write to Single Register

- Start Signal
- Slave Address Byte (R/W Bit = 0)
- Register Address Byte

- Data Byte to Register
- Stop Signal

6.3.2 Burst Write to Multiple (3) Registers

- Start Signal
- Slave Address Byte (R/W Bit = 0)
- Register Address Byte
- Data Byte to Register
- Data Byte to Register+1
- Data Byte to Register+2
- Stop Signal

6.3.3 Read from Single Register

- Start Signal
- Slave Address Byte (R/W Bit = 0)
- Register Address Byte
- Start Signal
- Slave Address Byte (R/W Bit = 1)
- Data Byte to Register
- Stop Signal

6.3.4 Read from Multiple (3) Registers

- Start Signal
- Slave Address Byte (R/W Bit = 0)
- Register Address Byte
- Start Signal
- Slave Address Byte (R/W Bit = 1)
- Data Byte to Register
- Data Byte to Register+1
- Data Byte to Register+2
- Stop Signal

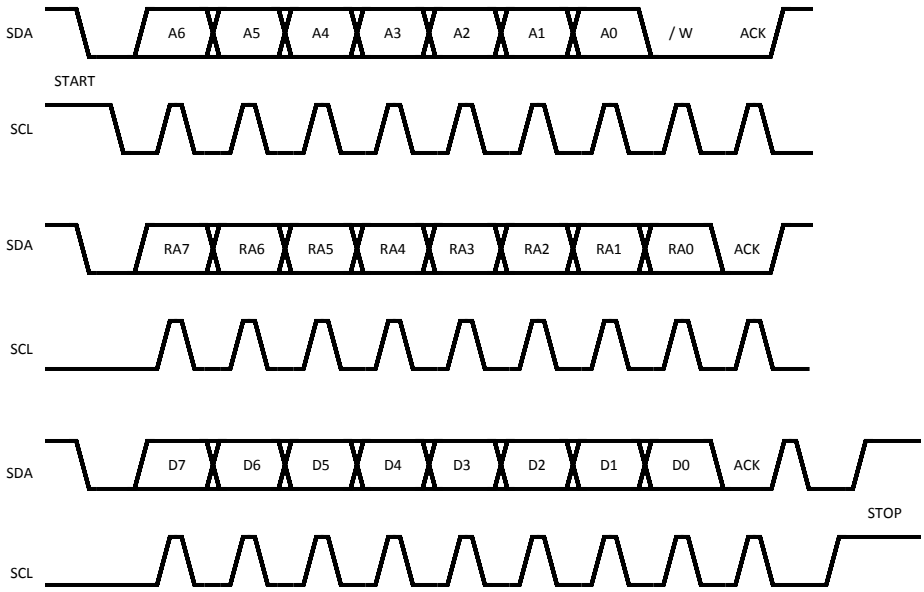


Figure 14. Write to Single Register

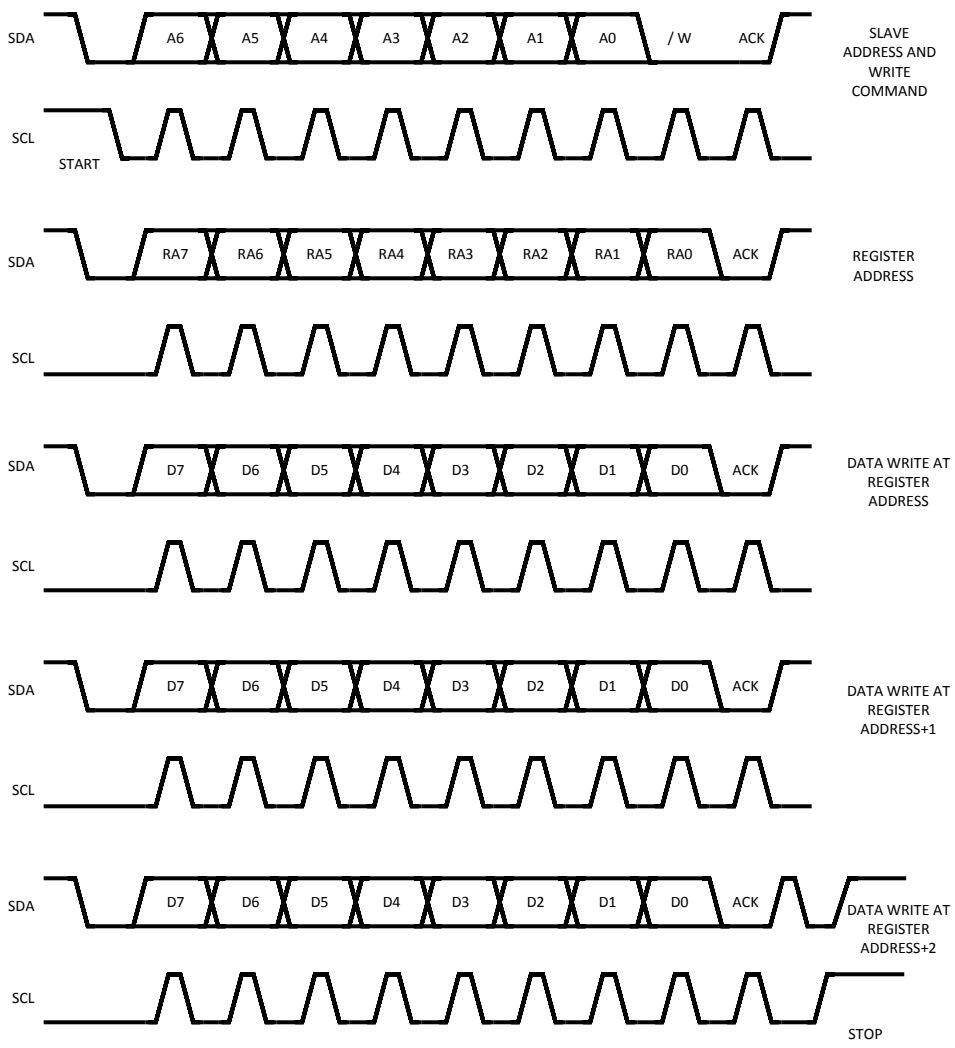


Figure 15. Write to Multiple (3) Registers

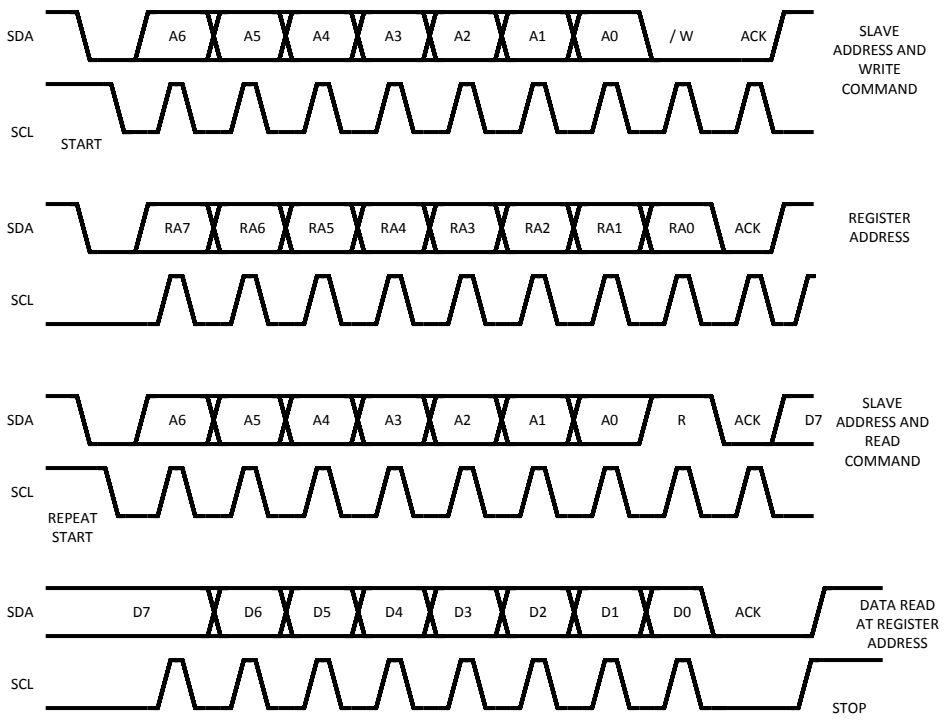


Figure 16. Read from Single Register

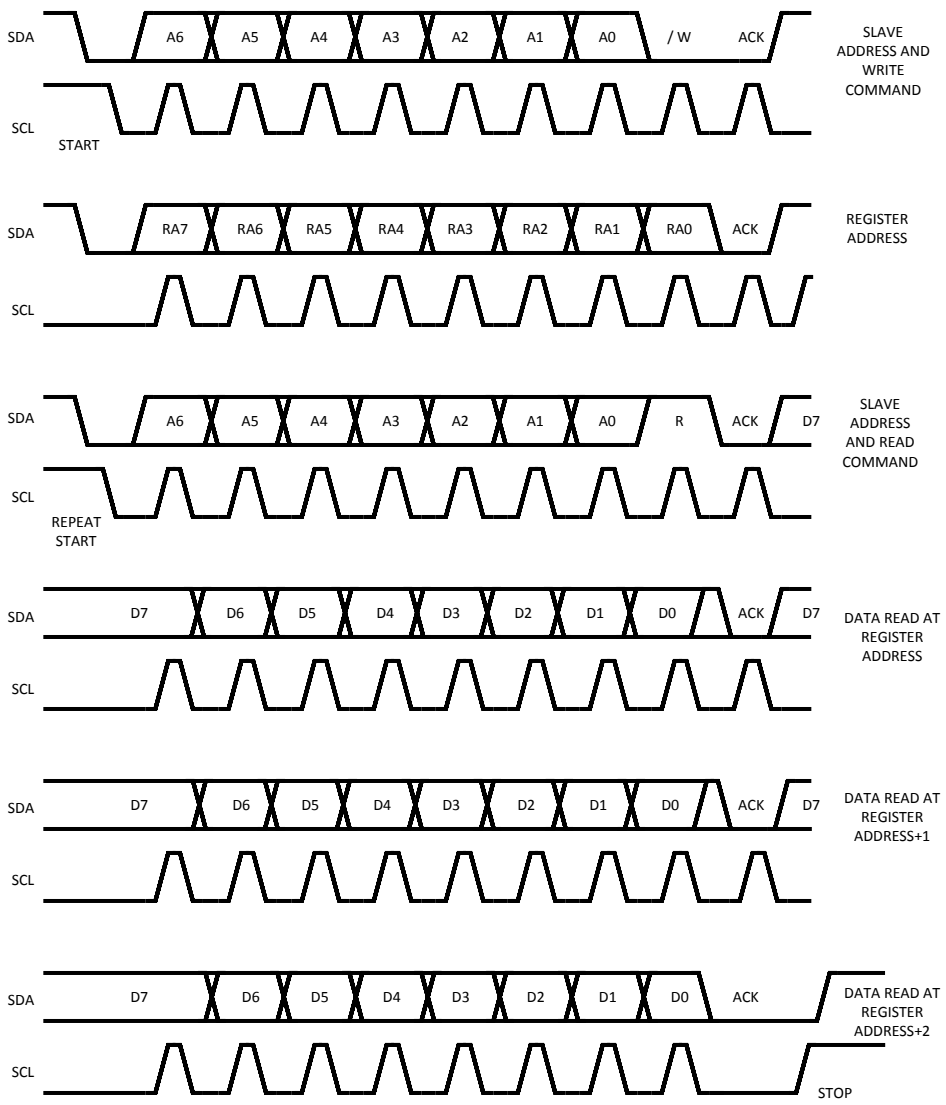


Figure 17. Read from Multiple (3) Registers

6.3.5 Serial Clock Input Noise Filter

Because the serial clock and data lines are resistively pulled up to a power bus, there is a possibility that noise will be coupled into the clock or data lines when all devices have released the line. Noise on the clock line can have serious negative effects, by desynchronizing the Master and Slave. To help prevent these problems, a filter is included on the clock input, to prevent higher frequency noise pulses from being recognized by the serial interface.

REVISION HISTORY

Changes from Revision B (April 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	33

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