



**THE DATASHEET OF  
AD8574TRU-EP-RL**



## FEATURES

**Low offset voltage: 1  $\mu$ V**  
**Input offset drift: 0.005  $\mu$ V/ $^{\circ}$ C**  
**Rail-to-rail input and output swing**  
**5 V/2.7 V single-supply operation**  
**High gain: 145 dB typical**  
**CMRR: 140 dB typical**  
**PSRR: 130 dB typical**  
**Ultralow input bias current: 10 pA typical**  
**Low supply current: 750  $\mu$ A per op amp**  
**Overload recovery time: 50  $\mu$ s**  
**No external capacitors required**

## ENHANCED PRODUCT FEATURES

**Supports defense and aerospace applications (AQEC standard)**  
**Military temperature range ( $-55^{\circ}$ C to  $+125^{\circ}$ C)**  
**Controlled manufacturing baseline**  
**One assembly/test site**  
**One fabrication site**  
**Product change notification**  
**Qualification data available on request**

## APPLICATIONS

**Temperature sensors**  
**Pressure sensors**  
**Precision current sensing**  
**Strain gage amplifiers**

## PIN CONFIGURATION

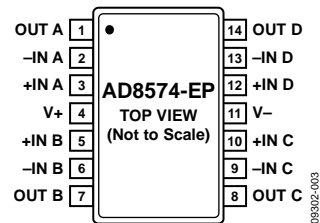


Figure 1. 14-Lead TSSOP

## GENERAL DESCRIPTION

This amplifier has ultralow offset, drift, and bias current. The AD8574-EP is a quad amplifier, featuring rail-to-rail input and output swings. It is guaranteed to operate from 2.7 V to 5 V single supply.

The AD8574-EP provides benefits previously found only in expensive auto-zeroing or chopper stabilized amplifiers. Using a patented spread spectrum, auto-zero technique, the AD8574 eliminates the intermodulation effects from interaction of the chopping function with the signal frequency in ac applications.

With an offset voltage of only 1  $\mu$ V and drift of 0.005  $\mu$ V/ $^{\circ}$ C, the AD8574-EP is perfectly suited for applications where error sources must be minimized.

The AD8574-EP is specified for the military temperature range ( $-55^{\circ}$ C to  $+125^{\circ}$ C). The AD8574-EP quad amplifier is available in a 14-lead TSSOP package.

Additional applications and technical information is available in the [AD8571/AD8572/AD8574](#) data sheets.

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**REVISION HISTORY**

**4/2018—Rev. 0 to Rev. A**

Changes to Features Section.....	1
Added Enhanced Product Features Section.....	1
Changes to Ordering Guide .....	14

**8/2010—Revision 0: Initial Version**

**SPECIFICATIONS****5 V ELECTRICAL CHARACTERISTICS**

$V_S = 5\text{ V}$ ,  $V_{CM} = 2.5\text{ V}$ ,  $V_O = 2.5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	5	$\mu\text{V}$
Input Bias Current	$I_B$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10	50	$\text{pA}$
Input Offset Current	$I_{OS}$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.0	1.5	$\text{nA}$
Input Voltage Range		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	70	$\text{pA}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0 120	140	5	$\text{dB}$
Large Signal Voltage Gain <sup>1</sup>	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $V_O = 0.3\text{ V to } 4.7\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	115	130		$\text{dB}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		120	135	$\text{dB}$
				0.005	0.04	$\mu\text{V}/^\circ\text{C}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega$ to GND $R_L = 100\text{ k}\Omega$ to GND at $-55^\circ\text{C}$ to $+125^\circ\text{C}$ $R_L = 10\text{ k}\Omega$ to GND $R_L = 10\text{ k}\Omega$ to GND at $-55^\circ\text{C}$ to $+125^\circ\text{C}$	4.99 4.99 4.95 4.95	4.998 4.997 4.98 4.975		$\text{V}$ $\text{V}$ $\text{V}$ $\text{V}$
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega$ to V+ $R_L = 100\text{ k}\Omega$ to V+ at $-55^\circ\text{C}$ to $+125^\circ\text{C}$		1	10	$\text{mV}$
		$R_L = 10\text{ k}\Omega$ to V+ $R_L = 10\text{ k}\Omega$ to V+ at $-55^\circ\text{C}$ to $+125^\circ\text{C}$		2	10	$\text{mV}$
Short-Circuit Limit	$I_{SC}$	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	$\pm 25$	$\pm 50$		$\text{mA}$
Output Current	$I_O$	$-55^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 40$		$\text{mA}$
				$\pm 30$		$\text{mA}$
				$\pm 15$		$\text{mA}$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	120	130		$\text{dB}$
Supply Current per Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	115	130		$\text{dB}$
				850	975	$\mu\text{A}$
				1000	1075	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.4		$\text{V}/\mu\text{s}$
Overload Recovery Time				0.05	0.3	$\text{ms}$
Gain Bandwidth Product	GBP			1.5		$\text{MHz}$
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n$ p-p	0 Hz to 10 Hz 0 Hz to 1 Hz		1.3		$\mu\text{V p-p}$ $\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		0.41		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 10\text{ Hz}$		51		$\text{fA}/\sqrt{\text{Hz}}$
				2		$\text{fA}/\sqrt{\text{Hz}}$

<sup>1</sup> Gain testing is dependent upon test bandwidth.

**2.7 V ELECTRICAL CHARACTERISTICS**

$V_S = 2.7\text{ V}$ ,  $V_{CM} = 1.35\text{ V}$ ,  $V_O = 1.35\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Table 2.**

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	5	$\mu\text{V}$
Input Bias Current	$I_B$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10	50	$\mu\text{A}$
Input Offset Current	$I_{OS}$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.0	1.5	$\text{nA}$
Input Voltage Range		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10	50	$\mu\text{A}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.7\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0	115	130	$\text{dB}$
Large Signal Voltage Gain <sup>1</sup>	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $V_O = 0.3\text{ V to } 2.4\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	110	130	$\text{dB}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		105	130	$\text{dB}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 100\text{ k}\Omega$ to GND $R_L = 100\text{ k}\Omega$ to GND at $-55^\circ\text{C}$ to $+125^\circ\text{C}$ $R_L = 10\text{ k}\Omega$ to GND $R_L = 10\text{ k}\Omega$ to GND at $-55^\circ\text{C}$ to $+125^\circ\text{C}$	2.685	2.697		$\text{V}$
Output Voltage Low	$V_{OL}$	$R_L = 100\text{ k}\Omega$ to $V_+$ $R_L = 100\text{ k}\Omega$ to $V_+$ at $-55^\circ\text{C}$ to $+125^\circ\text{C}$ $R_L = 10\text{ k}\Omega$ to $V_+$ $R_L = 10\text{ k}\Omega$ to $V_+$ at $-55^\circ\text{C}$ to $+125^\circ\text{C}$	2.67	2.68		$\text{V}$
Short-Circuit Limit	$I_{SC}$	$-55^\circ\text{C}$ to $+125^\circ\text{C}$	$\pm 10$	$\pm 15$		$\text{mA}$
Output Current	$I_O$	$-55^\circ\text{C}$ to $+125^\circ\text{C}$		$\pm 10$		$\text{mA}$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.5\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	120	130		$\text{dB}$
Supply Current per Amplifier	$I_{SY}$	$V_O = 0\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		750	900	$\mu\text{A}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		0.5		$\text{V}/\mu\text{s}$
Overload Recovery Time				0.05		$\text{ms}$
Gain Bandwidth Product	GBP			1		$\text{MHz}$
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n$ p-p	0 Hz to 10 Hz		2.0		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		94		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 10\text{ Hz}$		2		$\text{fA}/\sqrt{\text{Hz}}$

<sup>1</sup> Gain testing is dependent upon test bandwidth.

## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND to $V_S + 0.3$ V
Differential Input Voltage <sup>1</sup>	$\pm 5.0$ V
ESD (Human Body Model)	2000 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Operating Temperature Range	$-55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
Junction Temperature Range	$-65^{\circ}\text{C}$ to $+150^{\circ}\text{C}$
Lead Temperature (Soldering, 60 sec)	$300^{\circ}\text{C}$

<sup>1</sup> Differential input voltage is limited to  $\pm 5.0$  V or the supply voltage, whichever is less.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL CHARACTERISTICS

$\theta_{JA}$  is specified for the worst case conditions, that is,  $\theta_{JA}$  is specified for a device soldered in a circuit board for TSSOP packages.

Table 4. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
14-Lead TSSOP (RU)	180	36	$^{\circ}\text{C}/\text{W}$

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

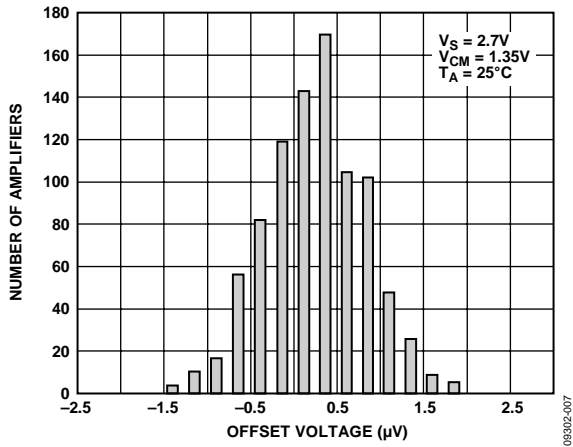


Figure 2. Input Offset Voltage Distribution

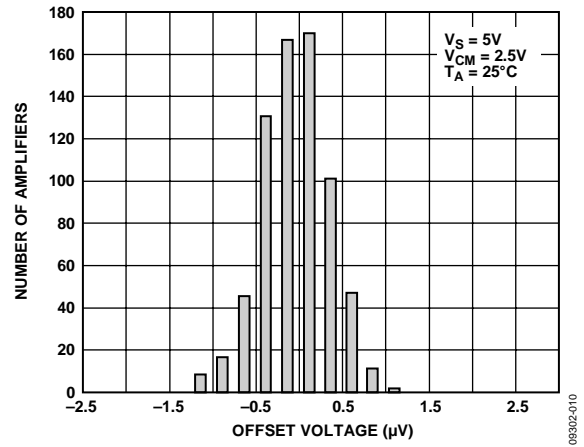


Figure 5. Input Offset Voltage Distribution

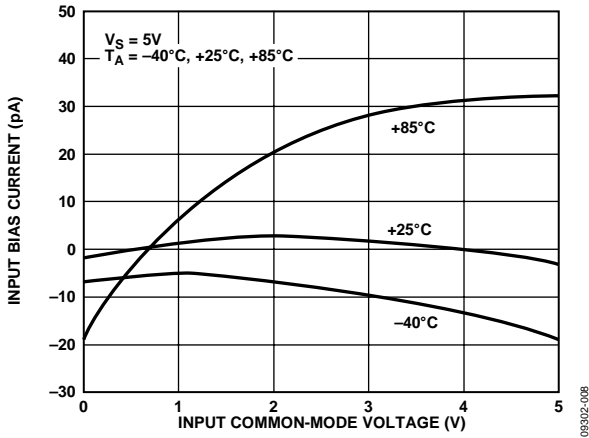


Figure 3. Input Bias Current vs. Input Common-Mode Voltage

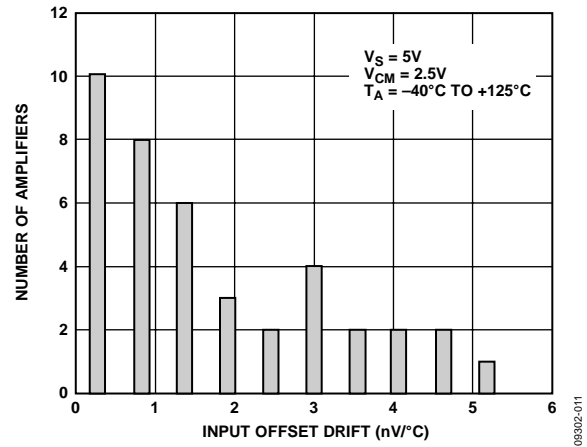


Figure 6. Input Offset Voltage Drift Distribution

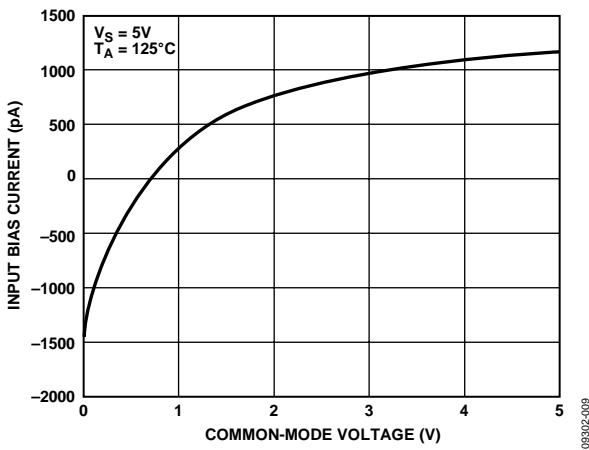


Figure 4. Input Bias Current vs. Common-Mode Voltage

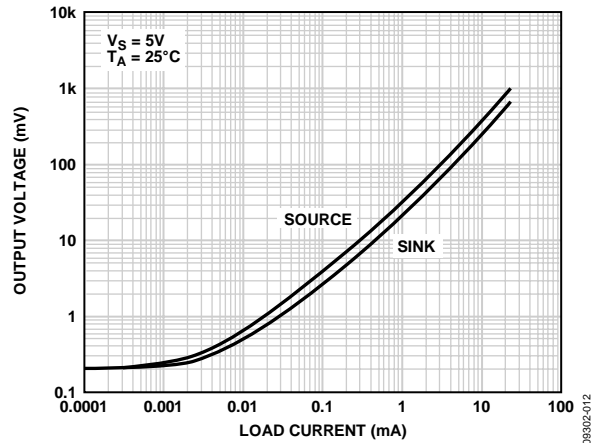


Figure 7. Output Voltage to Supply Rail vs. Load Current

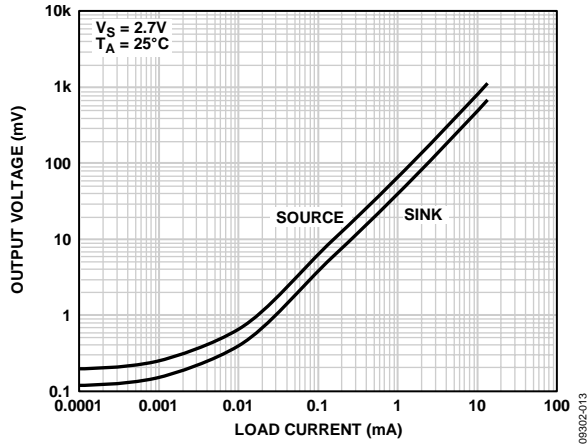


Figure 8. Output Voltage to Supply Rail vs. Load Current

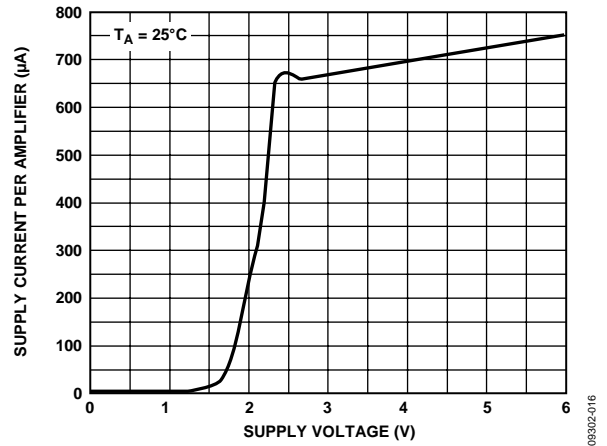


Figure 11. Supply Current per Amplifier vs. Supply Voltage

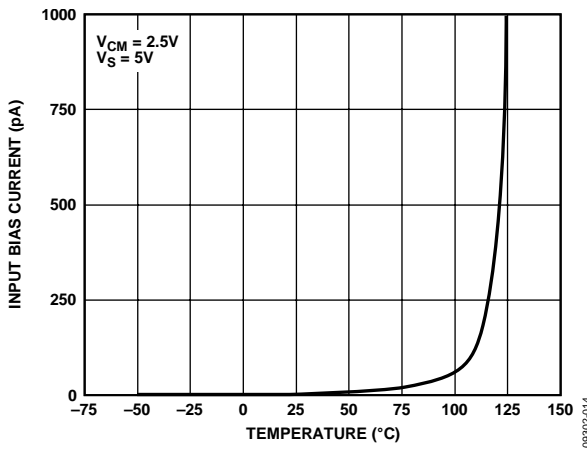


Figure 9. Input Bias Current vs. Temperature

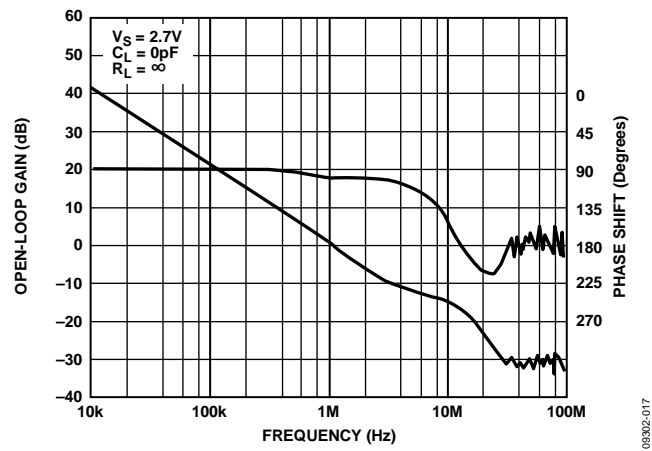


Figure 12. Open-Loop Gain and Phase Shift vs. Frequency

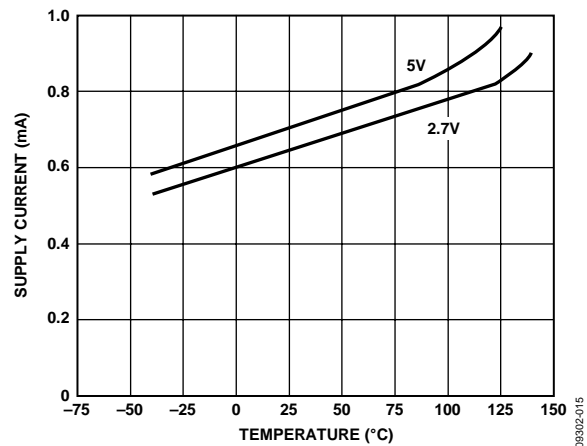


Figure 10. Supply Current vs. Temperature

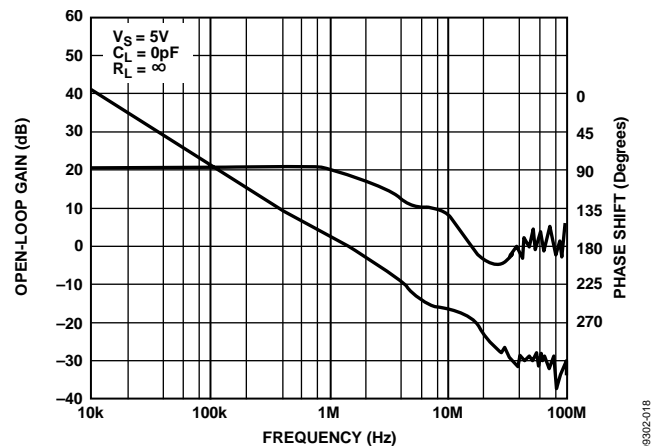


Figure 13. Open-Loop Gain and Phase Shift vs. Frequency

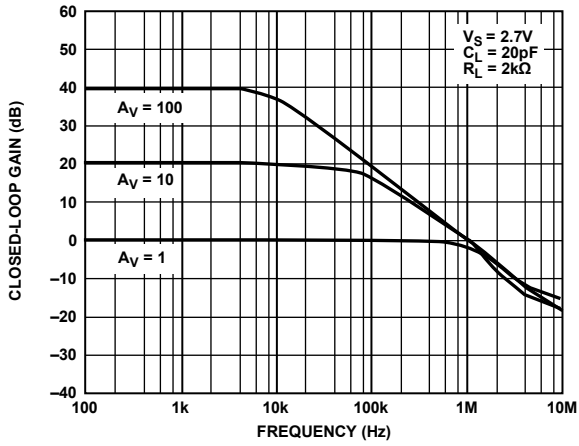


Figure 14. Closed-Loop Gain vs. Frequency

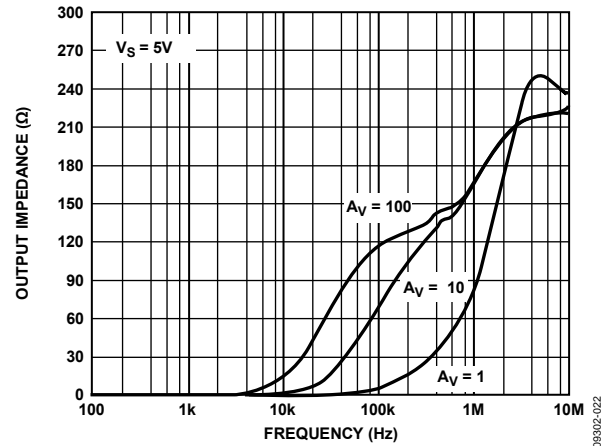


Figure 17. Output Impedance vs. Frequency

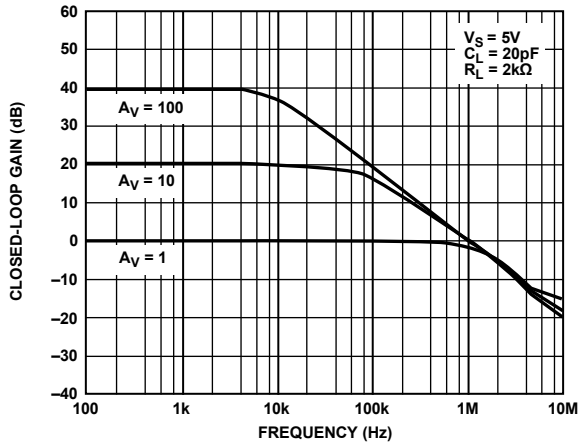


Figure 15. Closed-Loop Gain vs. Frequency

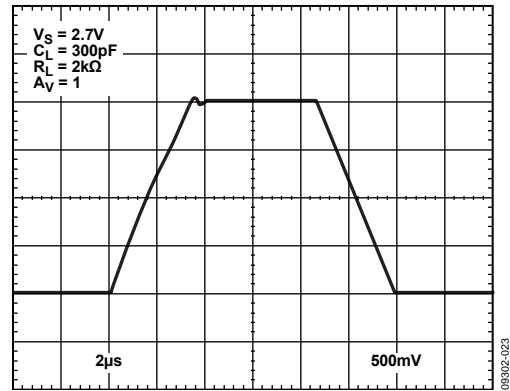


Figure 18. Large Signal Transient Response

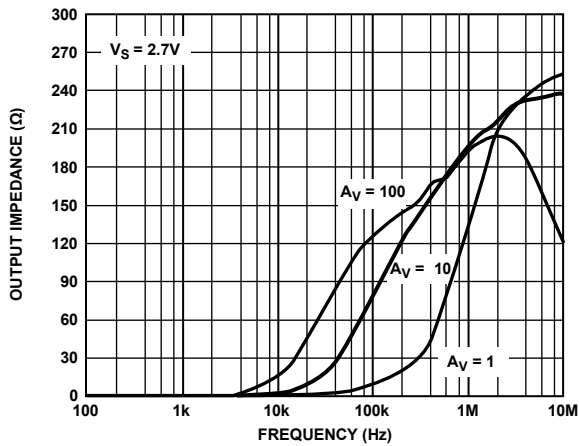


Figure 16. Output Impedance vs. Frequency

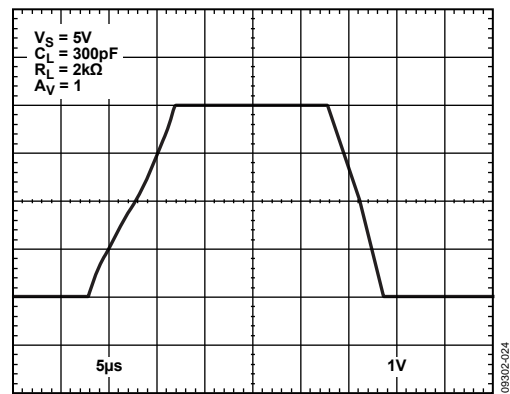


Figure 19. Large Signal Transient Response

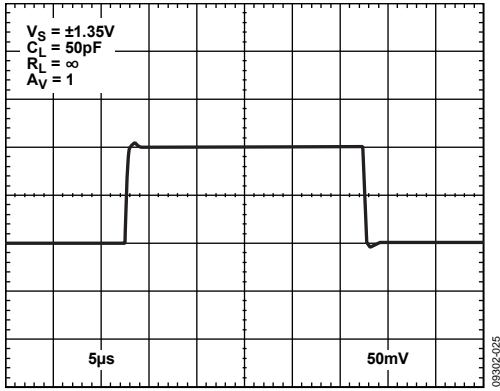


Figure 20. Small Signal Transient Response

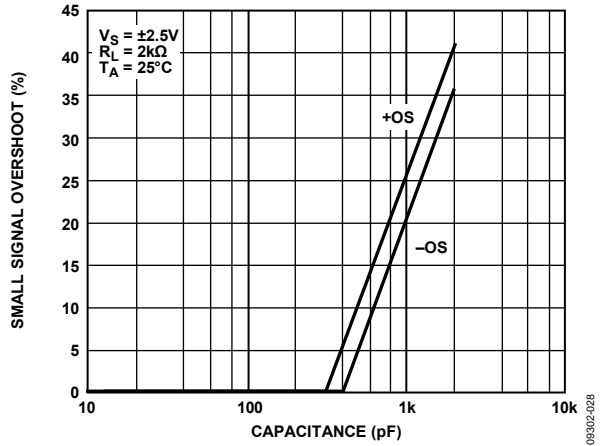


Figure 23. Small Signal Overshoot vs. Load Capacitance

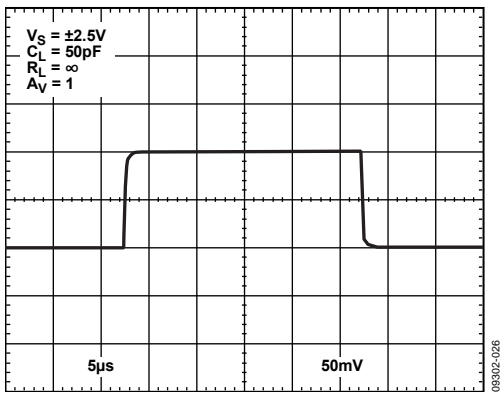


Figure 21. Small Signal Transient Response

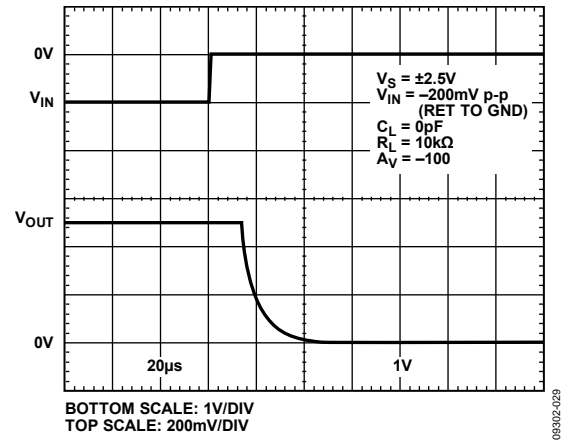


Figure 24. Positive Overvoltage Recovery

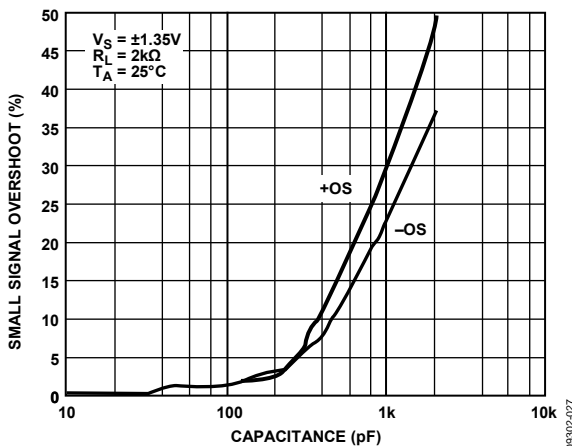


Figure 22. Small Signal Overshoot vs. Load Capacitance

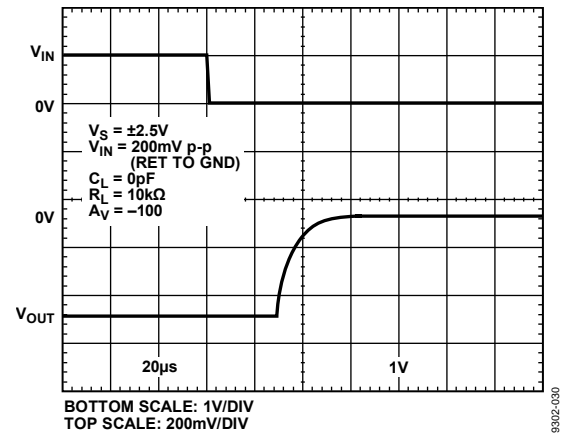


Figure 25. Negative Overvoltage Recovery

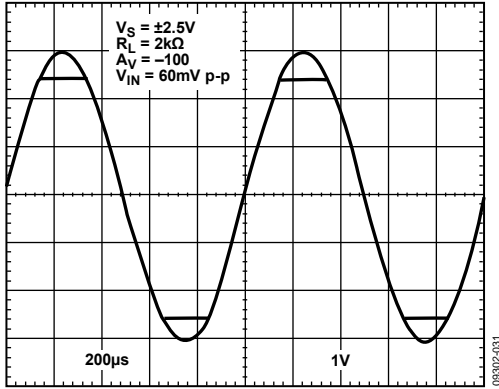


Figure 26. No Phase Reversal

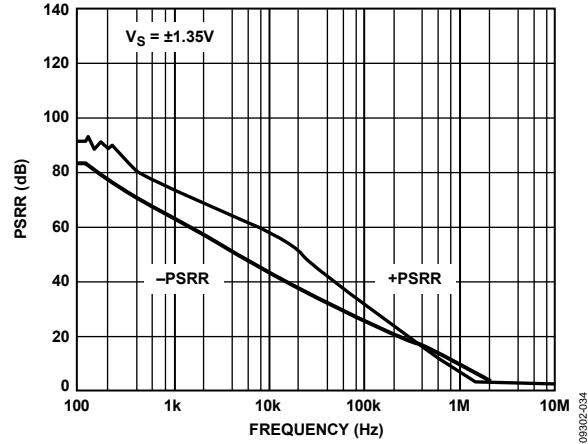


Figure 29. PSRR vs. Frequency

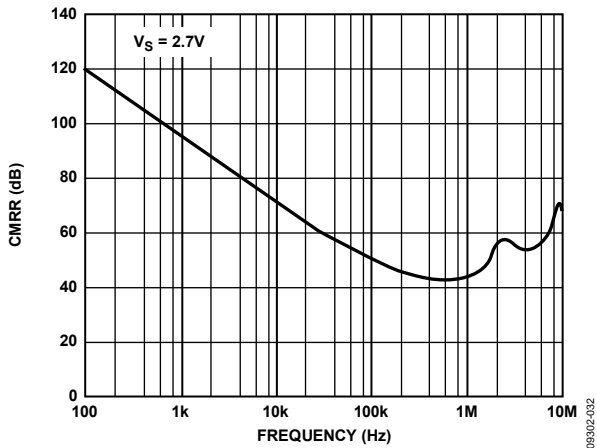


Figure 27. CMRR vs. Frequency

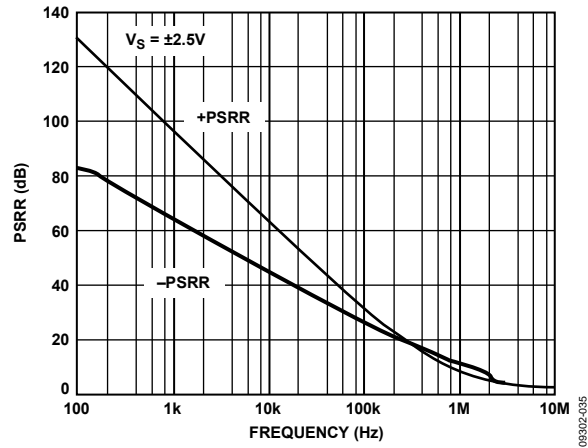


Figure 30. PSRR vs. Frequency

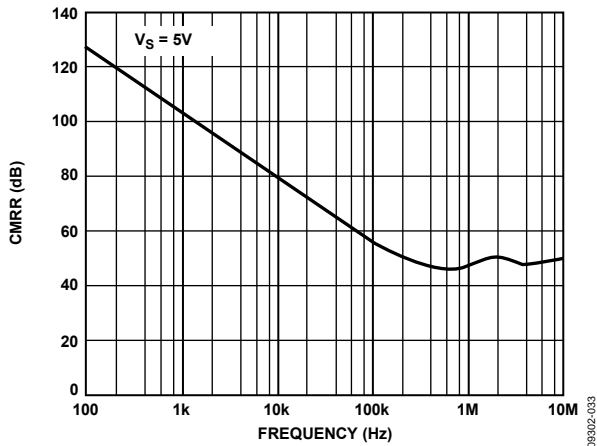


Figure 28. CMRR vs. Frequency

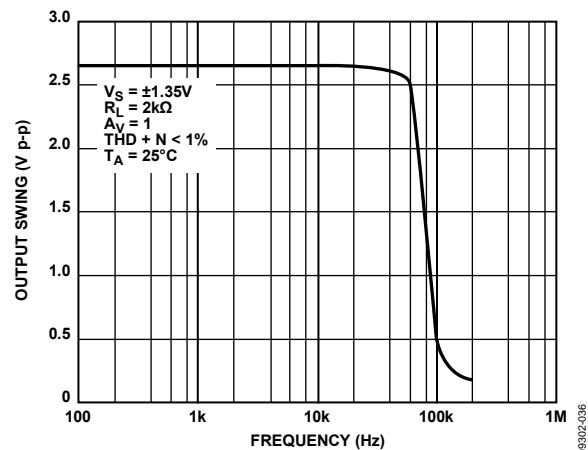


Figure 31. Maximum Output Swing vs. Frequency

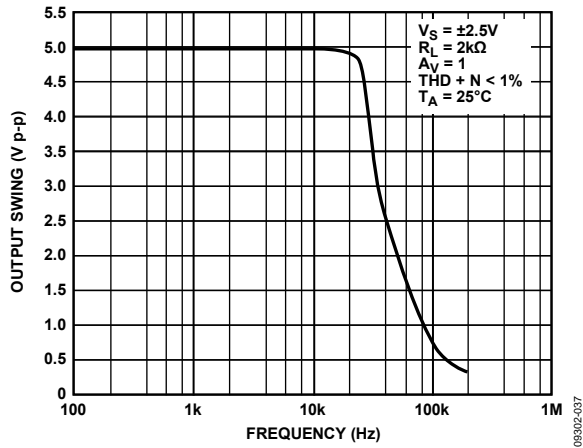


Figure 32. Maximum Output Swing vs. Frequency

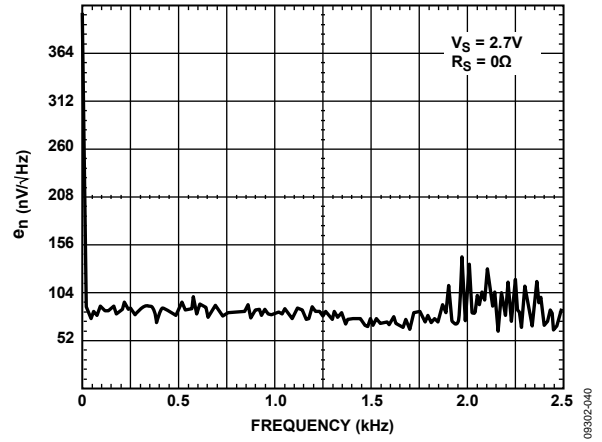


Figure 35. Voltage Noise Density from 0 Hz to 2.5 kHz

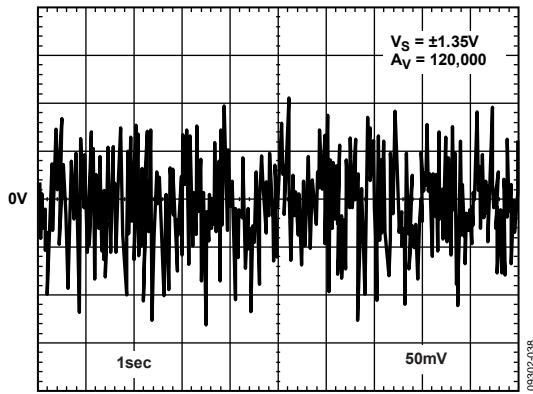


Figure 33. 0.1 Hz to 10 Hz Noise

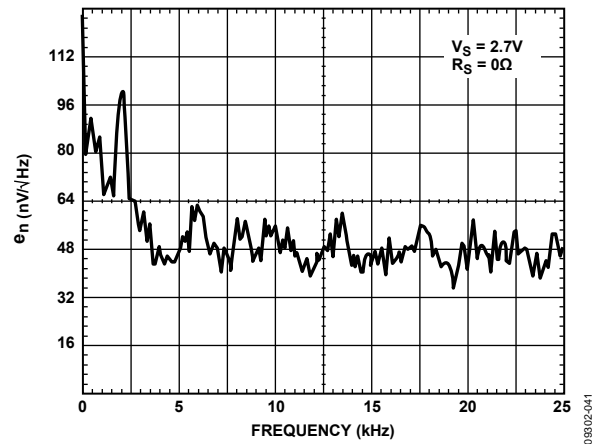


Figure 36. Voltage Noise Density from 0 Hz to 25 kHz

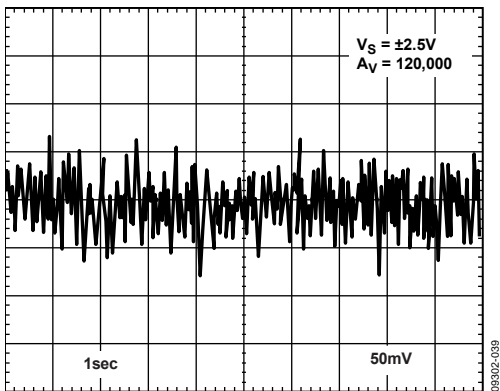


Figure 34. 0.1 Hz to 10 Hz Noise

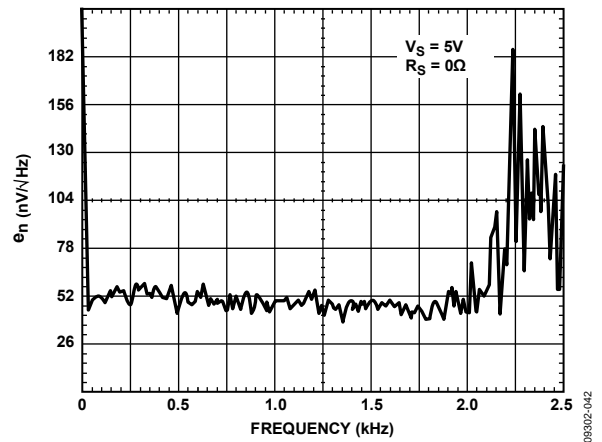


Figure 37. Voltage Noise Density from 0 Hz to 2.5 kHz

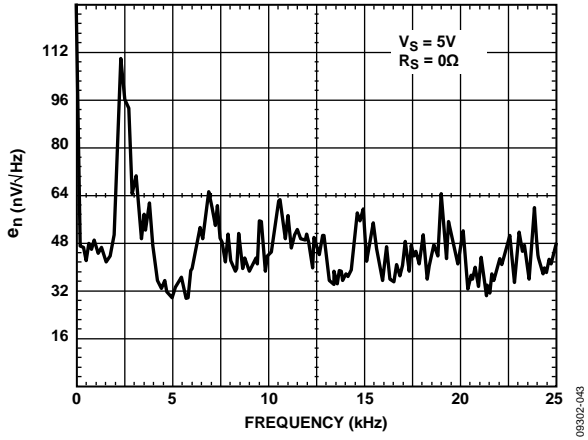


Figure 38. Voltage Noise Density from 0 Hz to 25 kHz

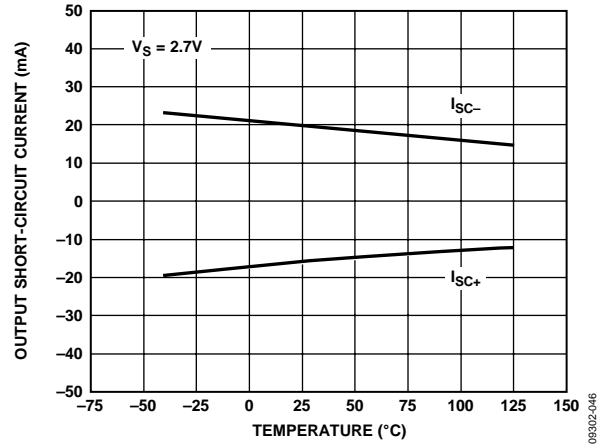


Figure 41. Output Short-Circuit Current vs. Temperature

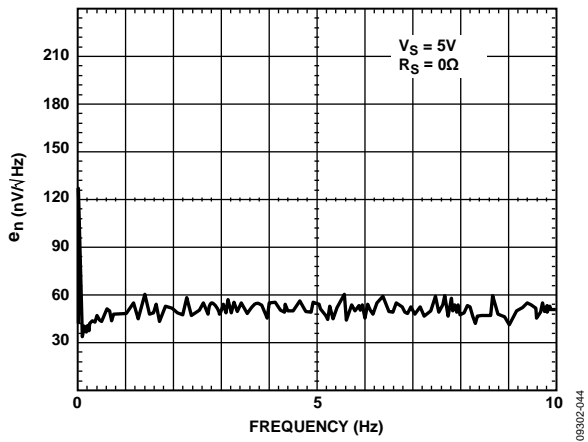


Figure 39. Voltage Noise Density from 0 Hz to 10 Hz

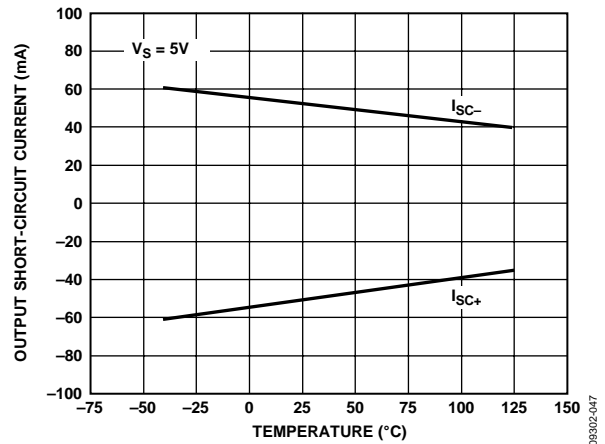


Figure 42. Output Short-Circuit Current vs. Temperature

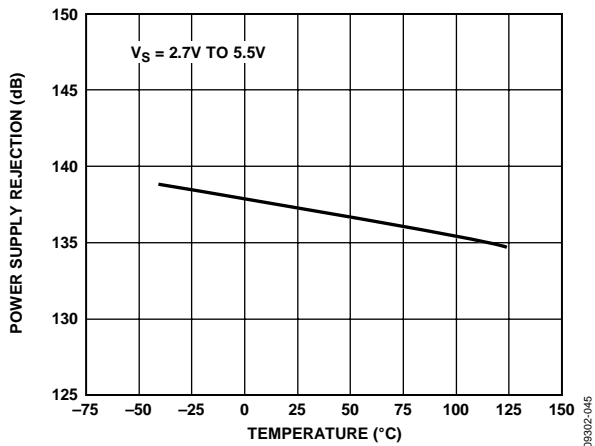


Figure 40. Power Supply Rejection vs. Temperature

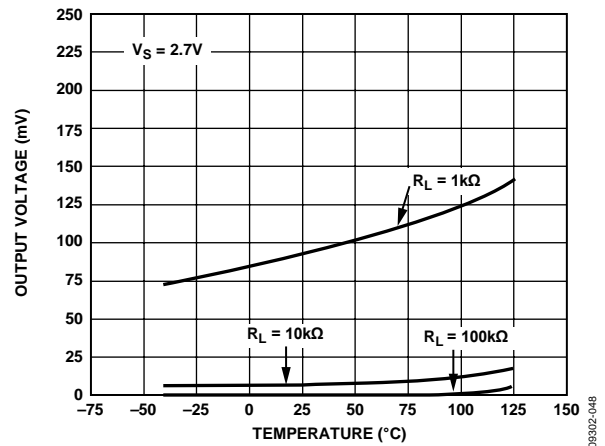


Figure 43. Output Voltage to Supply Rail vs. Temperature

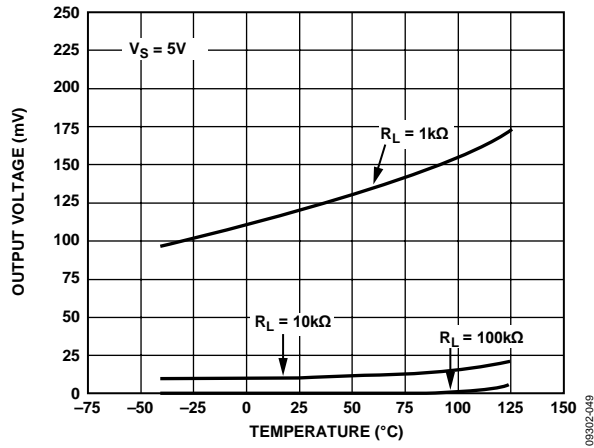
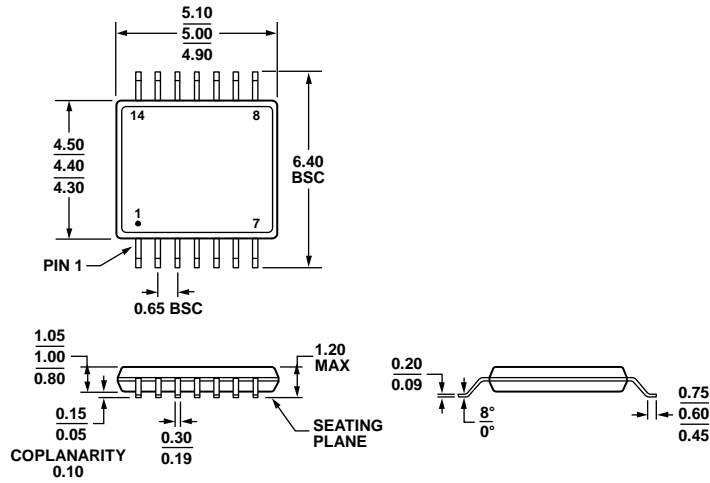


Figure 44. Output Voltage to Supply Rail vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB-1

Figure 45. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)

Dimensions shown in millimeters

061908-A

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option
AD8574TRU-EP	-55°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
AD8574TRU-EP-RL	-55°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
AD8574TRUZ-EP	-55°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14
AD8574TRUZ-EP-RL	-55°C to +125°C	14-Lead Thin Shrink Small Outline Package [TSSOP]	RU-14

<sup>1</sup> Z = RoHS Compliant Part

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View AD8574TRU-EP-RL on WIN SOURCE](#)
- ⊖ [Analog Devices Inc. Information](#)

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- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management