THE DATASHEET OF

AD8008ARMZ

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Ultralow Distortion, High Speed Amplifiers

AD8007/AD8008

FEATURES

Extremely low distortion
- **Second harmonic**
  - **−88 dBc @ 5 MHz**
  - **−83 dBc @ 20 MHz (AD8007)**
  - **−77 dBc @ 20 MHz (AD8008)**
- **Third harmonic**
  - **−101 dBc @ 5 MHz**
  - **−92 dBc @ 20 MHz (AD8007)**
  - **−98 dBc @ 20 MHz (AD8008)**

High speed
- **650 MHz, −3 dB bandwidth (G = +1)**
- **1000 V/µs slew rate**

Low noise
- **2.7 nV/√Hz input voltage noise**
- **22.5 pA/√Hz input inverting current noise**

Low power: 9 mA/amplifier typical supply current
Wide supply voltage range: 5 V to 12 V
0.5 mV typical input offset voltage
Small packaging: 8-lead SOIC, 8-lead MSOP, and 5-lead SC70

APPLICATIONS

Instrumentation
IF and baseband amplifiers
Filters
A/D drivers
DAC buffers

GENERAL DESCRIPTION

The AD8007 (single) and AD8008 (dual) are high performance current feedback amplifiers with ultralow distortion and noise. Unlike other high performance amplifiers, the low price and low quiescent current allow these amplifiers to be used in a wide range of applications. Analog Devices, Inc., proprietary second-generation eXtra-Fast Complementary Bipolar (XFCB) process enables such high performance amplifiers with low power consumption.

The AD8007/AD8008 have 650 MHz bandwidth, 2.7 nV/√Hz voltage noise, −83 dB SFDR at 20 MHz (AD8007), and −77 dBc SFDR at 20 MHz (AD8008).

With the wide supply voltage range (5 V to 12 V) and wide bandwidth, the AD8007/AD8008 are designed to work in a variety of applications. The AD8007/AD8008 amplifiers have a low power supply current of 9 mA/amplifier.

CONNECTION DIAGRAMS

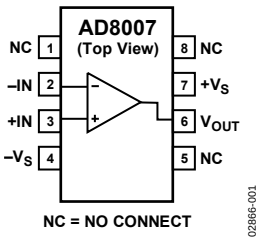

Figure 1. 8-Lead SOIC (R)

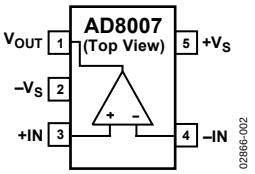

Figure 2. 5-Lead SC70 (KS)

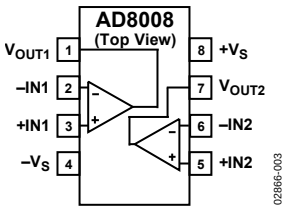

Figure 3. 8-Lead SOIC (R) and 8-Lead MSOP (RM)

The AD8007 is available in a tiny SC70 package as well as a standard 8-lead SOIC. The dual AD8008 is available in both an 8-lead SOIC and an 8-lead MSOP. These amplifiers are rated to work over the industrial temperature range of −40°C to +85°C.

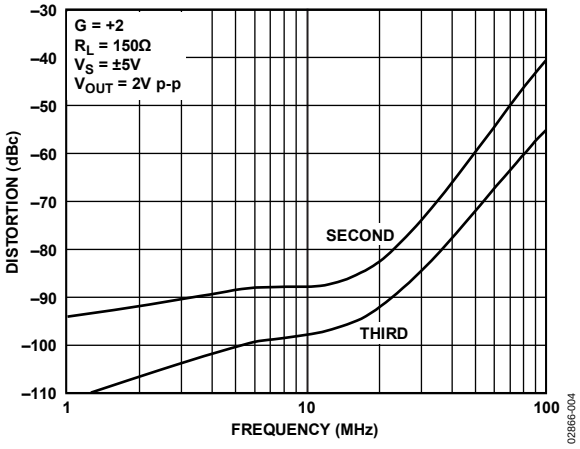

Figure 4. AD8007 Second and Third Harmonic Distortion vs. Frequency

Rev. E
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REVISION HISTORY

11/09—Rev. D to Rev. E

Change to Output Capacitance Section 17
Updated Outline Dimensions 18
Changes to Ordering Guide 19

6/03—Rev. C to Rev. D

Change to Layout Considerations Section 15
Deleted Figure 7 16
Deleted Evaluation Board Section 16
Updated Outline Dimensions 16

10/02—Rev. B to Rev. C

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Updated Outline Dimensions 19

9/02—Rev. A to Rev. B

Updated Outline Dimensions 19

8/02—Rev. 0 to Rev. A

Added AD8008 ..... Universal
Added SOIC-8 (RN) and MSOP-8 (RM) 1
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Changes to General Description 1
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New TPCs 19 to 24 and TPCs 27, 29, 30, and 35 9
Changes to Evaluation Board Section 16
MSOP-8 (RM) Added 19

SPECIFICATIONS

V_S = ±5 V

T_A = 25°C, R_S = 200 Ω, R_L = 150 Ω, R_F = 499 Ω, Gain = +2, unless otherwise noted.

Table 1.

		AD8007/AD8008			
Parameter	**Conditions**	**Min**	**Typ**	**Max**	**Unit**
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p, R_L = 1 kΩ	540	650		MHz
	G = +1, V_O = 0.2 V p-p, R_L = 150 Ω	250	500		MHz
	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω	180	230		MHz
	G = +1, V_O = 2 V p-p, R_L = 1 kΩ	200	235		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p, G = +2, R_L = 150 Ω	50	90		MHz
Overdrive Recovery Time	±2.5 V input step, G = +2, R_L = 1 kΩ		30		ns
Slew Rate	G = +1, V_O = 2 V step	900	1000		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		18		ns
Settling Time to 0.01%	G = +2, V_O = 2 V step		35		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	f_C = 5 MHz, V_O = 2 V p-p		−88		dBc
	f_C = 20 MHz, V_O = 2 V p-p		−83/−77		dBc
Third Harmonic	f_C = 5 MHz, V_O = 2 V p-p		−101		dBc
IMD	f_C = 20 MHz, V_O = 2 V p-p		−92/−98		dBc
	f_C = 19.5 MHz to 20.5 MHz, R_L = 1 kΩ, V_O = 2 V p-p		−77		dBc
Third-Order Intercept	f_C = 5 MHz, R_L = 1 kΩ		43.0/42.5		dBm
	f_C = 20 MHz, R_L = 1 kΩ		42.5		dBm
Crosstalk (AD8008)	f = 5 MHz, G = +2		−68		dB
Input Voltage Noise	f = 100 kHz		2.7		nV/√Hz
Input Current Noise	−Input, f = 100 kHz		22.5		pA/√Hz
	+Input, f = 100 kHz		2		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.015		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.010		Degree
DC PERFORMANCE					
Input Offset Voltage			0.5	4	mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current	+Input		4	8	µA
	−Input		0.4	6	µA
Input Bias Current Drift	+Input		16		nA/°C
	−Input		9		nA/°C
Transimpedance	V_O = ±2.5 V, R_L = 1 kΩ	1.0	1.5		MΩ
	R_L = 150 Ω	0.4	0.8		MΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		4		MΩ
Input Capacitance	+Input		1		pF
Input Common-Mode Voltage Range			−3.9 to +3.9		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	56	59		dB
OUTPUT CHARACTERISTICS					
Output Saturation Voltage	V_{CC} − V_{OH}, V_{OL} − V_{EE}, R_L = 1 kΩ		1.1	1.2	V
Short-Circuit Current, Source			130		mA
Short-Circuit Current, Sink			90		mA
Capacitive Load Drive	30% overshoot		8		pF

Parameter	Conditions	AD8007/AD8008 Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range		5		12	V
Quiescent Current per Amplifier			9	10.2	mA
Power Supply Rejection Ratio					
+PSRR		59	64		dB
−PSRR		59	65		dB

V_S = 5 V

T_A = 25°C, R_S = 200 Ω, R_L = 150 Ω, R_F = 499 Ω, Gain = +2, unless otherwise noted.

Table 2.

Parameter	Conditions	AD8007/AD8008 Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p, R_L = 1 kΩ	520	580		MHz
	G = +1, V_O = 0.2 V p-p, R_L = 150 Ω	350	490		MHz
	G = +2, V_O = 0.2 V p-p, R_L = 150 Ω	190	260		MHz
	G = +1, V_O = 1 V p-p, R_L = 1 kΩ	270	320		MHz
Bandwidth for 0.1 dB Flatness	V_O = 0.2 V p-p, G = +2, R_L = 150 Ω	72	120		MHz
Overdrive Recovery Time	2.5 V input step, G = +2, R_L = 1 kΩ		30		ns
Slew Rate	G = +1, V_O = 2 V step	665	740		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V step		18		ns
Settling Time to 0.01%	G = +2, V_O = 2 V step		35		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	f_C = 5 MHz, V_O = 1 V p-p		−96/−95		dBc
	f_C = 20 MHz, V_O = 1 V p-p		−83/−80		dBc
Third Harmonic	f_C = 5 MHz, V_O = 1 V p-p		−100		dBc
	f_C = 20 MHz, V_O = 1 V p-p		−85/−88		dBc
IMD	f_C = 19.5 MHz to 20.5 MHz, R_L = 1 kΩ, V_O = 1 V p-p		−89/−87		dBc
Third-Order Intercept	f_C = 5 MHz, R_L = 1 kΩ		43.0		dBm
	f_C = 20 MHz, R_L = 1 kΩ		42.5/41.5		dBm
Crosstalk (AD8008)	Output-to-output, f = 5 MHz, G = +2		−68		dB
Input Voltage Noise	f = 100 kHz		2.7		nV/√Hz
Input Current Noise	−Input, f = 100 kHz		22.5		pA/√Hz
	+Input, f = 100 kHz		2		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			0.5	4	mV
Input Offset Voltage Drift			3		µV/°C
Input Bias Current	+Input		4	8	µA
	−Input		0.7	6	µA
Input Bias Current Drift	+Input		15		nA/°C
	−Input		8		nA/°C
Transimpedance	V_O = 1.5 V to 3.5 V, R_L = 1 kΩ	0.5	1.3		MΩ
	R_L = 150 Ω	0.4	0.6		MΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		4		MΩ
Input Capacitance	+Input		1		pF
Input Common-Mode Voltage Range			1.1 to 3.9		V
Common-Mode Rejection Ratio	V_{CM} = 1.75 V to 3.25 V	54	56		dB

Parameter	Conditions	AD8007/AD8008 Min	Typ	Max	Unit
OUTPUT CHARACTERISTICS					
Output Saturation Voltage	$V_{CC} - V_{OH}$, $V_{OL} - V_{EE}$, R_L = 1 kΩ		1.05	1.15	V
Short-Circuit Current, Source			70		mA
Short-Circuit Current, Sink			50		mA
Capacitive Load Drive	30% overshoot		8		pF
POWER SUPPLY					
Operating Range		5		12	V
Quiescent Current per Amplifier			8.1	9	mA
Power Supply Rejection Ratio					
+PSRR		59	62		dB
−PSRR		59	63		dB

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 5
Common-Mode Input Voltage	$\pm V_S$
Differential Input Voltage	±1.0 V
Output Short-Circuit Duration	See Figure 5
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +85°C
Lead Temperature (Soldering, 10 sec)	300°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

MAXIMUM POWER DISSIPATION

The maximum safe power dissipation in the AD8007/AD8008 packages is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die locally reaches the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8007/AD8008. Exceeding a junction temperature of 175°C for an extended time can result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = \textit{Quiescent Power} + (\textit{Total Drive Power} - \textit{Load Power})$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to V_S, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, then consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply

$$P_D = (V_S \times I_S) + \frac{\left(\frac{V_S}{4}\right)^2}{R_L}$$

In single-supply operation, with R_L referenced to V_S, worst case is $V_{OUT} = V_S/2$.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads from metal traces, through-holes, ground, and power planes reduces the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps, see the Layout Considerations section.

Figure 5 shows the maximum safe power dissipation in the package vs. the ambient temperature for the SOIC-8 (125°C/W), MSOP-8 (150°C/W), and SC70-5 (210°C/W) packages on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

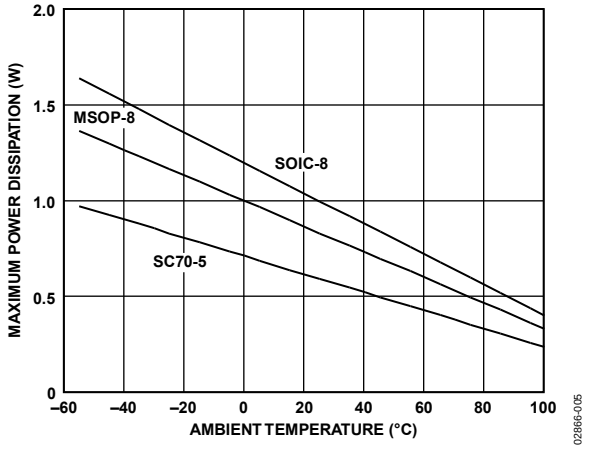


Figure 5. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

OUTPUT SHORT CIRCUIT

Shorting the output to ground or drawing excessive current for the AD8007/AD8008 will likely cause catastrophic failure.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

V_S = ±5 V, R_L = 150 Ω, R_S = 200 Ω, R_F = 499 Ω, unless otherwise noted.

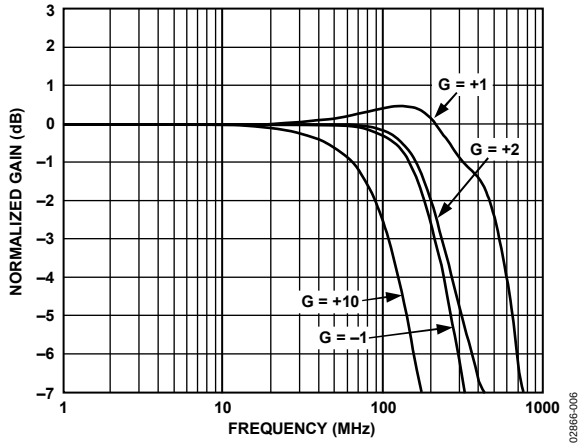


Figure 6. Small Signal Frequency Response for Various Gains

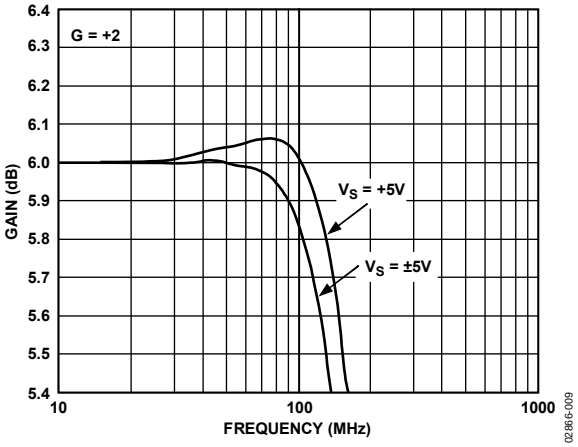


Figure 9. 0.1 dB Gain Flatness; V_S = +5, V_S = ±5 V

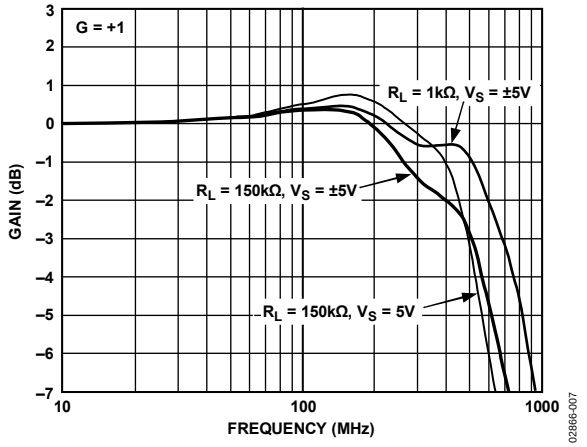


Figure 7. Small Signal Frequency Response for V_S and R_L

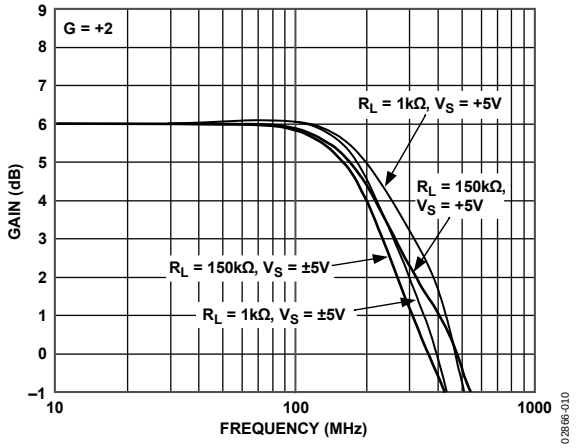


Figure 10. Small Signal Frequency Response for V_S and R_L

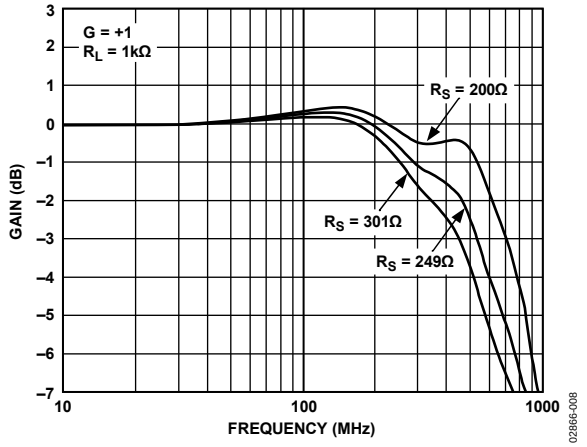


Figure 8. Small Signal Frequency Response for Various R_S Values

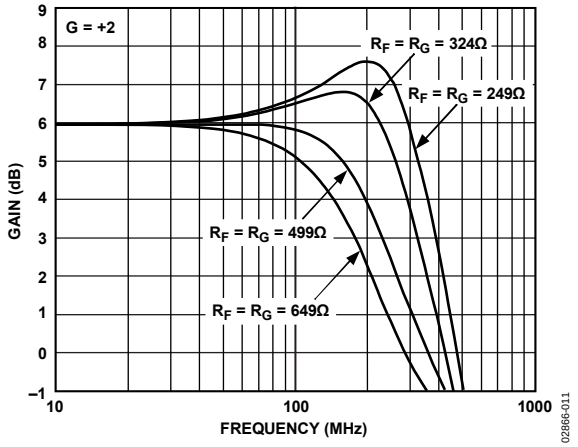


Figure 11. Small Signal Frequency Response for Various Feedback Resistors, $R_F = R_G$

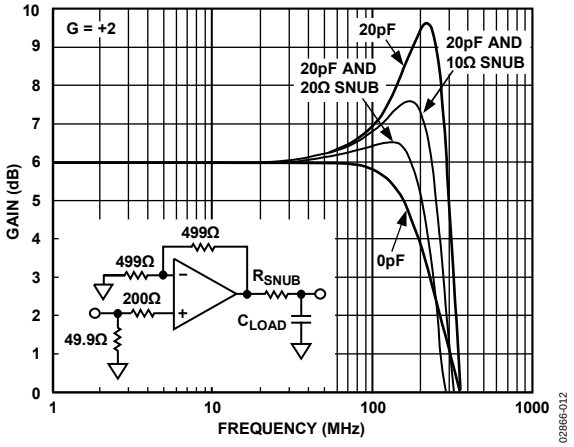


Figure 12. Small Signal Frequency Response for Capacitive Load and Snub Resistor

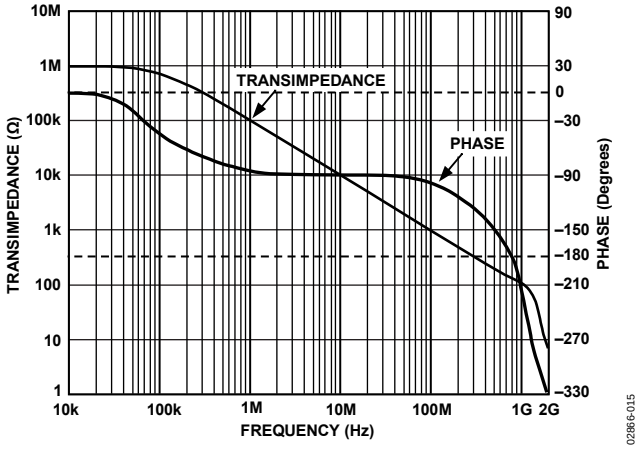


Figure 15. Transimpedance and Phase vs. Frequency

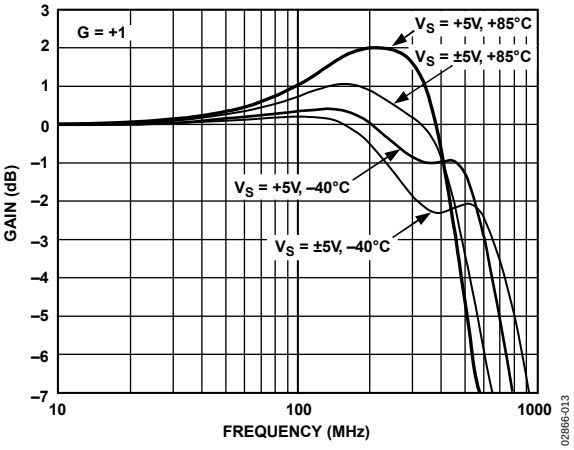


Figure 13. Small Signal Frequency Response over Temperature, V_S = +5 V, V_S = ±5 V

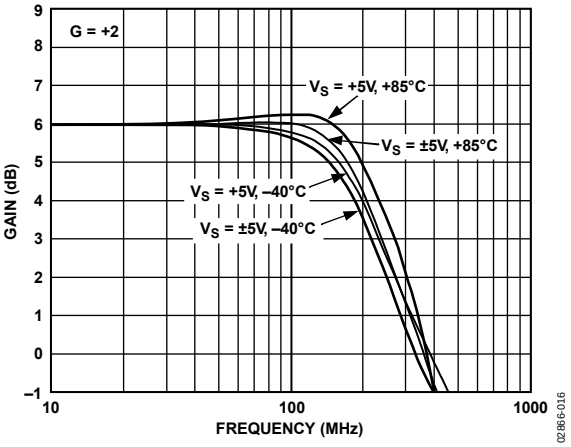


Figure 16. Small Signal Frequency Response over Temperature, V_S = +5 V, V_S = ±5 V

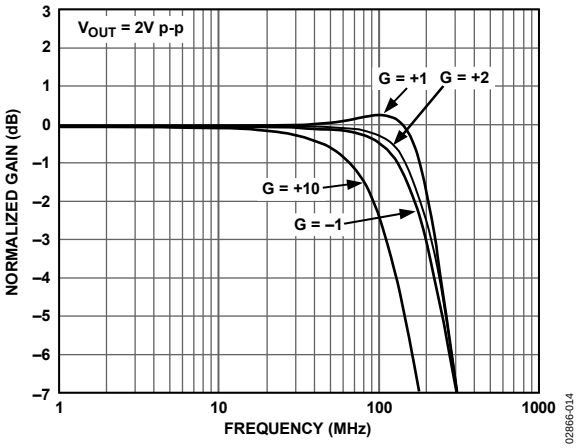


Figure 14. Large Signal Frequency Response for Various Gains

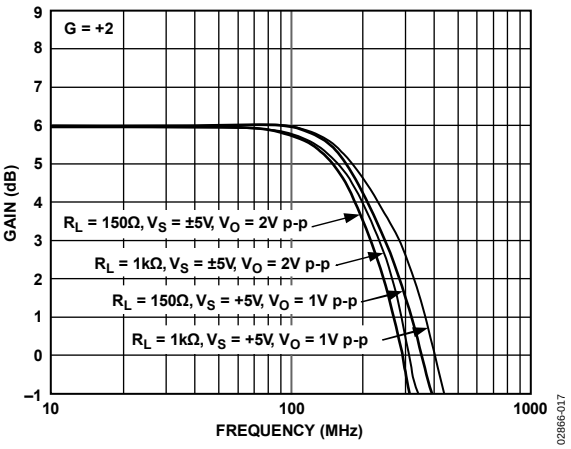


Figure 17. Large Signal Frequency Response for V_S and R_L

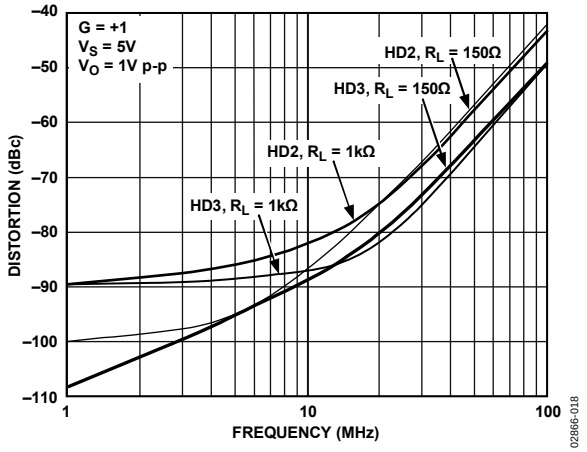


Figure 18. AD8007 Second and Third Harmonic Distortion vs. Frequency and R_L

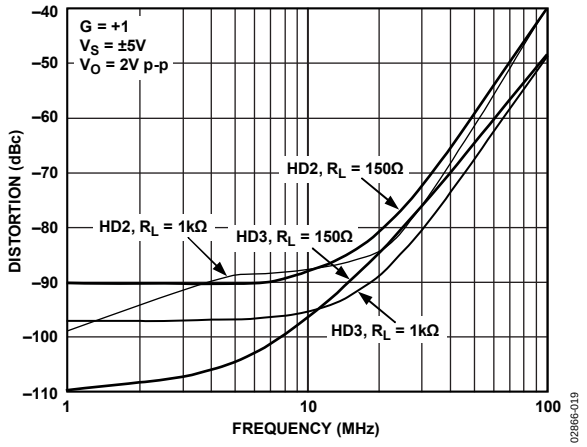


Figure 19. AD8007 Second and Third Harmonic Distortion vs. Frequency and R_L

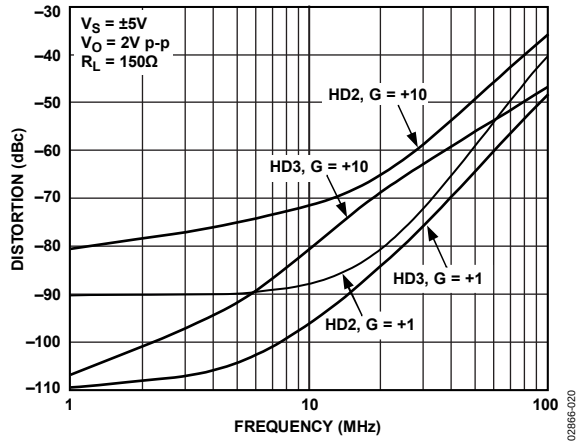


Figure 20. AD8007 Second and Third Harmonic Distortion vs. Frequency and Gain

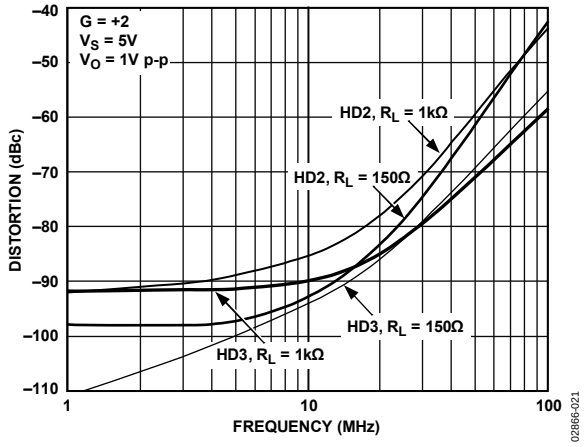


Figure 21. AD8007 Second and Third Harmonic Distortion vs. Frequency and R_L

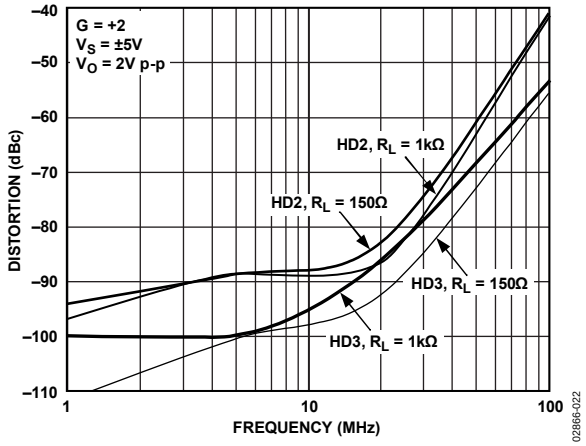


Figure 22. AD8007 Second and Third Harmonic Distortion vs. Frequency and R_L

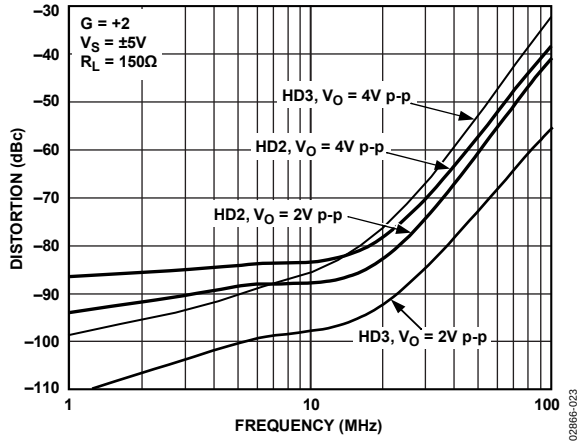


Figure 23. AD8007 Second and Third Harmonic Distortion vs. Frequency and V_O

V_S = ±5 V, R_S = 200 Ω, R_F = 499 Ω, R_L = 150 Ω, @ 25°C, unless otherwise noted.

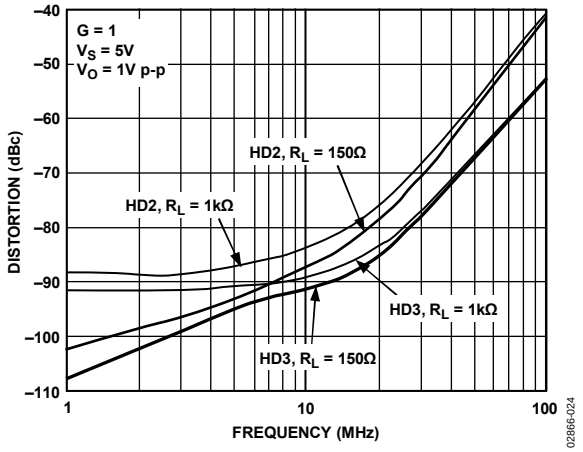


Figure 24. AD8008 Second and Third Harmonic Distortion vs. Frequency and R_L

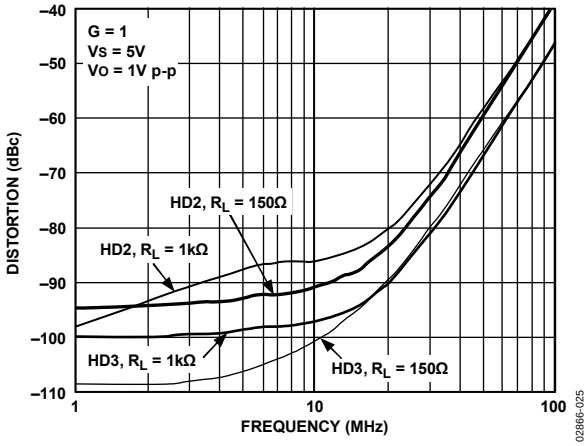


Figure 25. AD8008 Second and Third Harmonic Distortion vs. Frequency and R_L

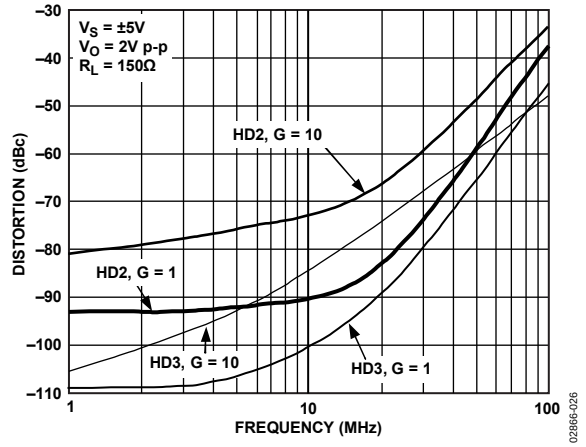


Figure 26. AD8008 Second and Third Harmonic Distortion vs. Frequency and Gain

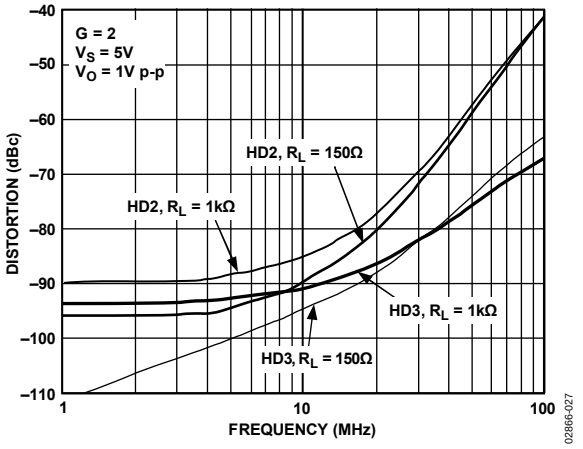


Figure 27. AD8008 Second and Third Harmonic Distortion vs. Frequency and R_L

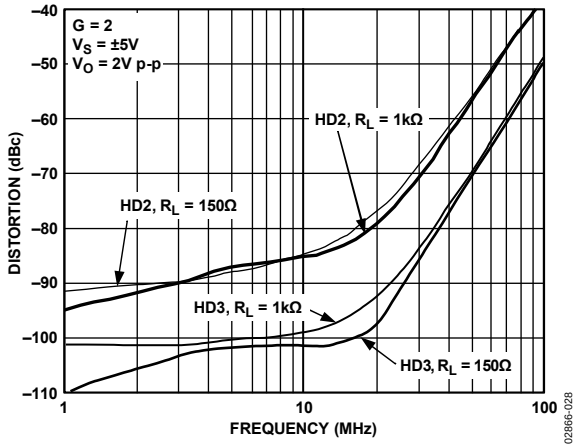


Figure 28. AD8008 Second and Third Harmonic Distortion vs. Frequency and R_L

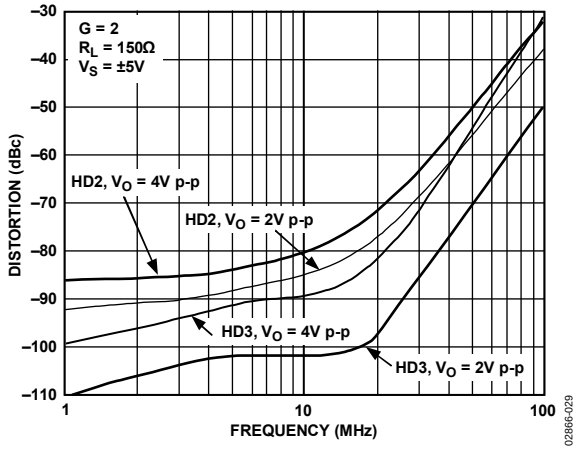


Figure 29. AD8008 Second and Third Harmonic Distortion vs. Frequency and V_O

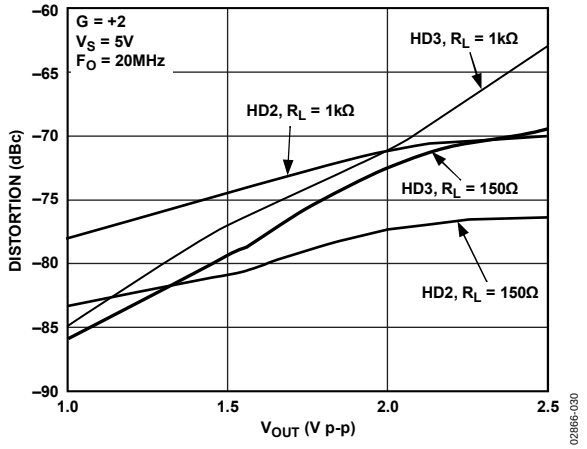


Figure 30. AD8007 Second and Third Harmonic Distortion vs. V_{OUT} and R_L

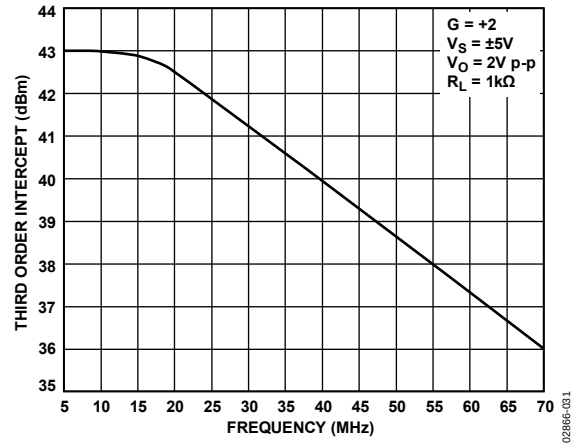


Figure 31. AD8007 Third-Order Intercept vs. Frequency

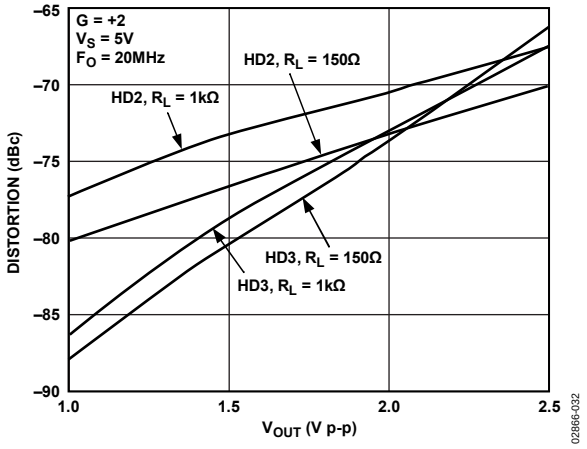


Figure 32. AD8008 Second and Third Harmonic Distortion vs. V_{OUT} and R_L

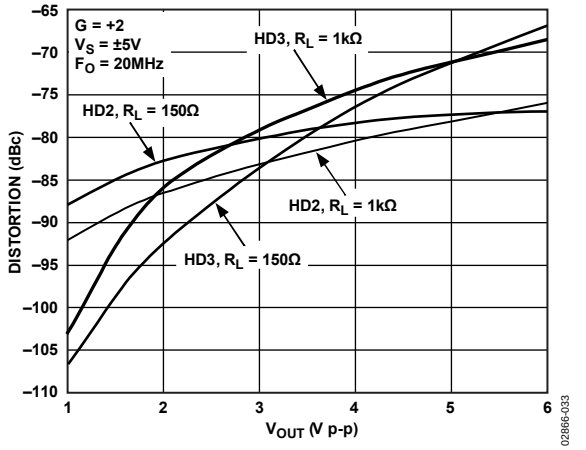


Figure 33. AD8007 Second and Third Harmonic Distortion vs. V_{OUT} and R_L

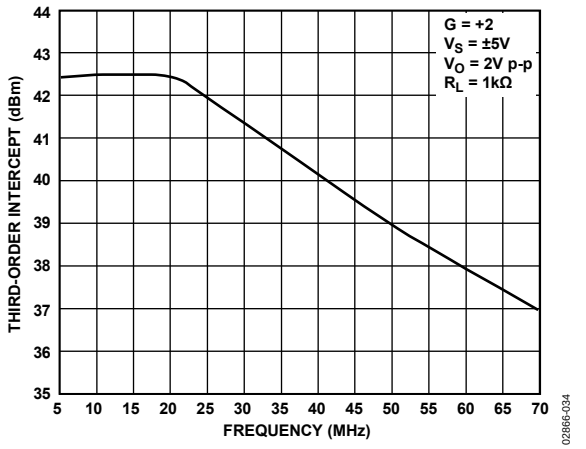


Figure 34. AD8008 Third-Order Intercept vs. Frequency

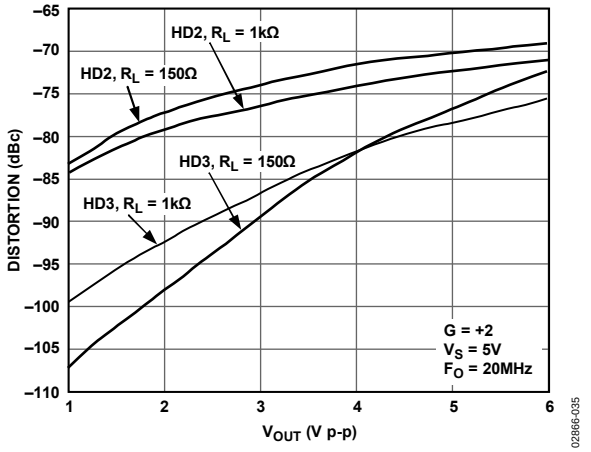


Figure 35. AD8008 Second and Third Harmonic Distortion vs. V_{OUT} and R_L

V_S = ±5 V, R_L = 150 Ω, R_S = 200 Ω, R_F = 499 Ω, unless otherwise noted.

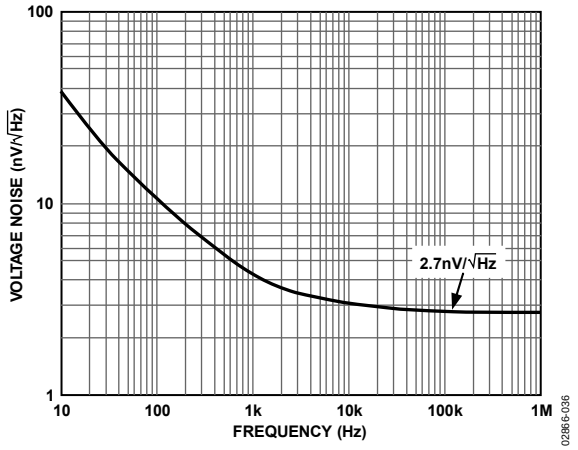


Figure 36. Input Voltage Noise vs. Frequency

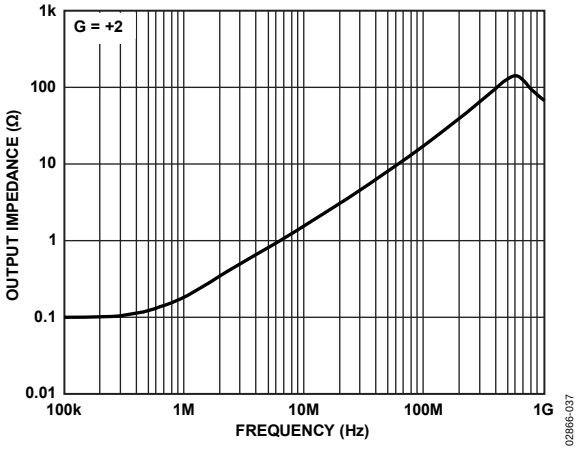


Figure 37. Output Impedance vs. Frequency

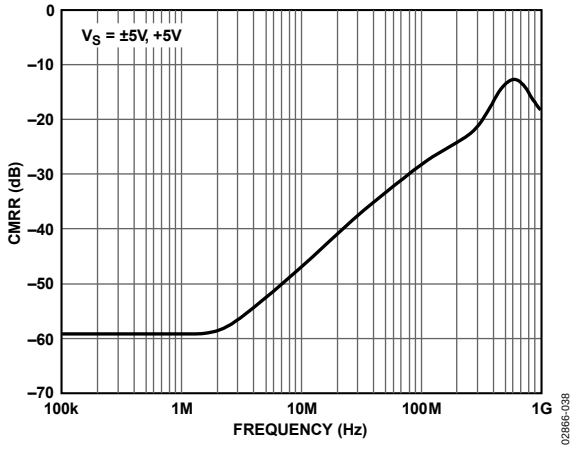


Figure 38. CMRR vs. Frequency

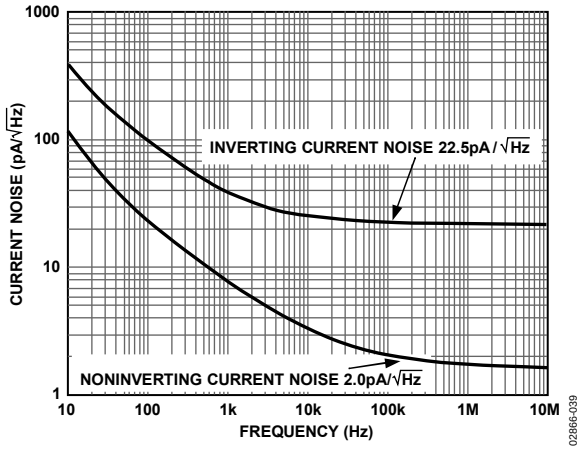


Figure 39. Input Current Noise vs. Frequency

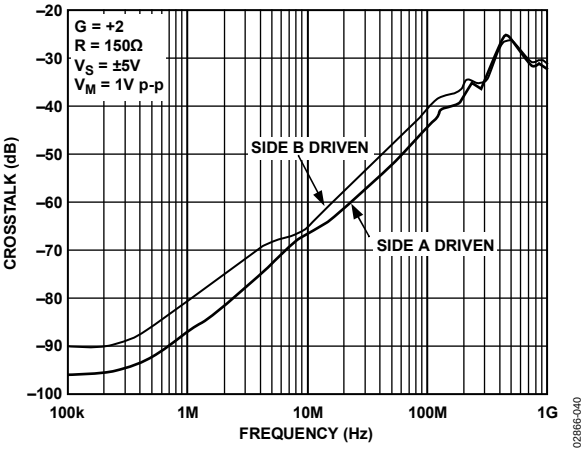


Figure 40. AD8008 Crosstalk vs. Frequency (Output to Output)

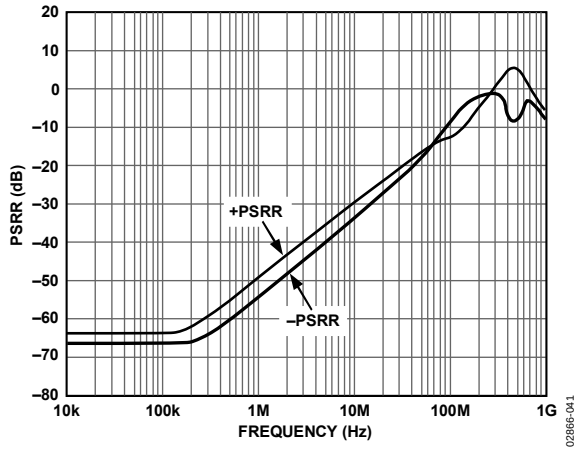


Figure 41. PSRR vs. Frequency

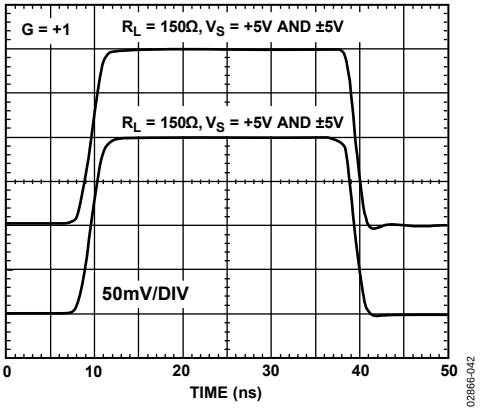


Figure 42. Small Signal Transient Response for R_L = 150 Ω, R_L = 1 kΩ and V_S = +5 V, V_S = ±5 V

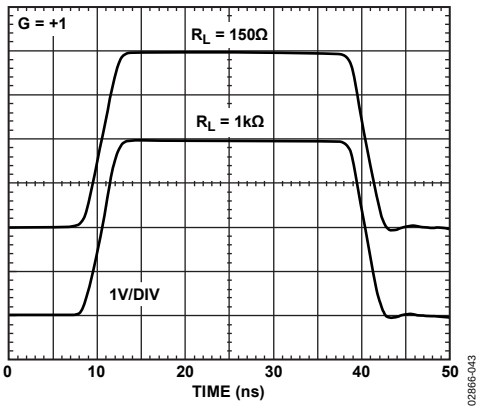


Figure 43. Large Signal Transient Response for R_L = 150 Ω, R_L = 1 kΩ

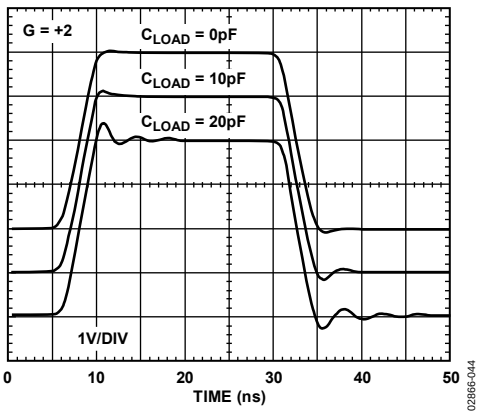


Figure 44. Large Signal Transient Response for C_{LOAD} = 0 pF, C_{LOAD} = 10 pF, and C_{LOAD} = 20 pF

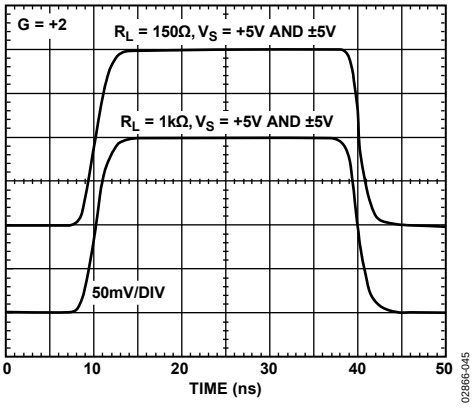


Figure 45. Small Signal Transient Response for R_L = 150 Ω, R_L = 1 kΩ and V_S = +5 V, V_S = ±5 V

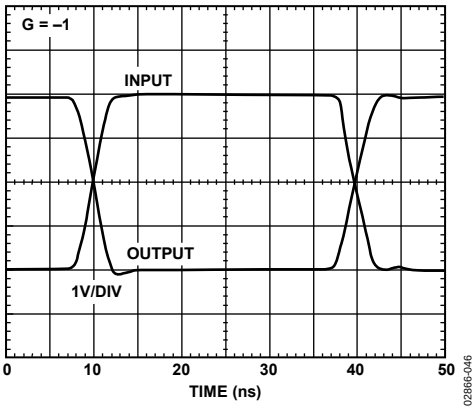


Figure 46. Large Signal Transient Response, G = −1, R_L = 150 Ω

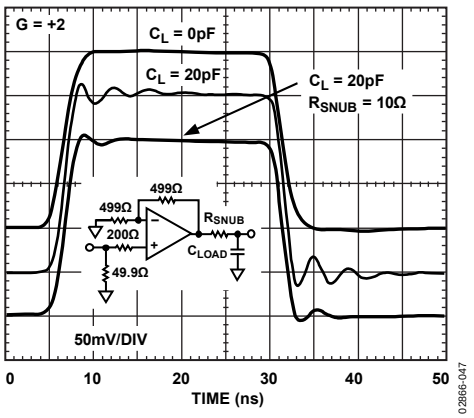


Figure 47. Small Signal Transient Response, Effect of Series Snub Resistor when Driving Capacitive Load

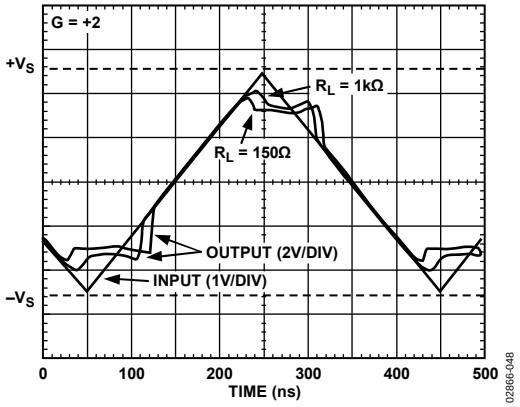


Figure 48. Output Overdrive Recovery, R_L = 1 kΩ, 150 Ω, V_{IN} = ±2.5 V

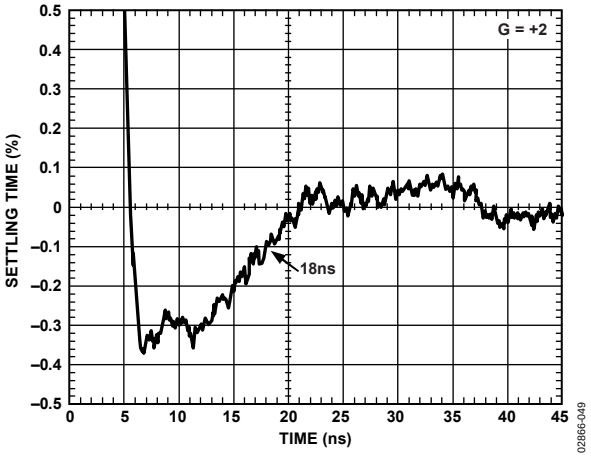


Figure 49. 0.1% Settling Time, 2 V Step

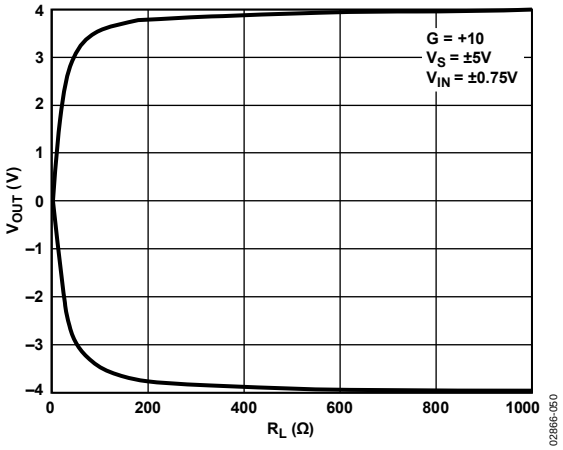


Figure 50. V_{OUT} Swing vs. R_L, V_S = ±5 V, G = +10, V_{IN} = ±0.75 V

THEORY OF OPERATION

The AD8007 (single) and AD8008 (dual) are current feedback amplifiers optimized for low distortion performance. A simplified conceptual diagram of the AD8007 is shown in Figure 51. It closely resembles a classic current feedback amplifier comprised of a complementary emitter-follower input stage, a pair of signal mirrors, and a diamond output stage. However, in the case of the AD8007/AD8008, several modifications were made to improve the distortion performance over that of a classic current feedback topology.

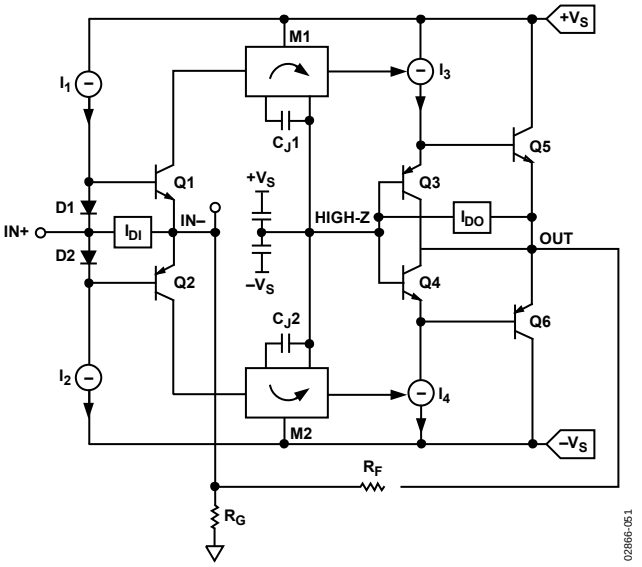


Figure 51. Simplified Schematic of AD8007

The signal mirrors were replaced with low distortion, high precision mirrors. In Figure 51, they are shown as M1 and M2. Their primary function from a distortion standpoint is to reduce the effect of highly nonlinear distortion caused by capacitances, CJ1 and CJ2. These capacitors represent the collector-to-base capacitances of the output devices of the mirrors.

A voltage imbalance arises across the output stage, as measured from the high impedance node, high-Z, to the output node, OUT. This imbalance is a result of delivering high output currents and is the primary cause of output distortion. Circuitry is included to sense this output voltage imbalance and generate a compensating current, I_{DO}. When injected into the circuit, I_{DO} reduces the distortion that could be generated at the output stage. Similarly, the nonlinear voltage imbalance across the input stage (measured from the noninverting to the inverting input) is sensed, and a current, I_{DI}, is injected to compensate for input-generated distortion.

The design and layout are strictly top-to-bottom symmetric to minimize the presence of even-order harmonics.

USING THE AD8007/AD8008

Supply Decoupling for Low Distortion

Decoupling for low distortion performance requires careful consideration. The commonly adopted practice of returning the high frequency supply decoupling capacitors to physically separate (and possibly distant) grounds can lead to degraded even-order harmonic performance. This situation is shown in Figure 52 using the AD8007 as an example; however, it is not recommended. For a sinusoidal input, each decoupling capacitor returns to its ground a quasi-rectified current carrying high even-order harmonics.

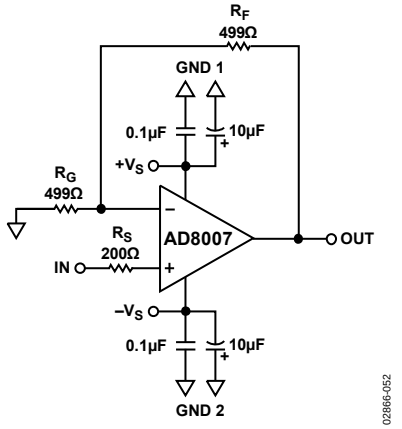


Figure 52. High Frequency Capacitors Returned to Physically Separate Grounds (Not Recommended)

The decoupling scheme shown in Figure 53 is recommended. In Figure 53, the two high frequency decoupling capacitors are first tied together at a common node and are then returned to the ground plane through a single connection. By first adding the two currents flowing through each high frequency decoupling capacitor, this ensures that the current returned into the ground plane is only at the fundamental frequency.

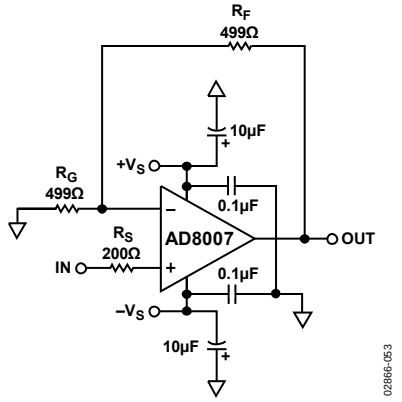


Figure 53. High Frequency Capacitors Returned to Ground at a Single Point (Recommended)

Whenever physical layout considerations prevent the decoupling scheme shown in Figure 53, the user can connect one of the high frequency decoupling capacitors directly across the supplies and connect the other high frequency decoupling capacitor to ground (see Figure 54).

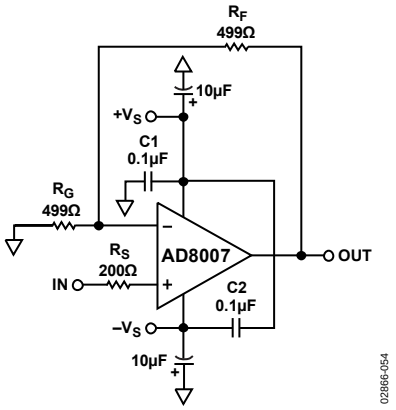


Figure 54. High Frequency Capacitors Connected Across the Supplies (Recommended)

LAYOUT CONSIDERATIONS

The standard noninverting configuration with recommended power supply bypassing is shown in Figure 54. The 0.1 µF high frequency decoupling capacitors should be X7R or NPO chip components. Connect C2 from the $+V_S$ pin to the $-V_S$ pin. Connect C1 from the $+V_S$ pin to signal ground.

The length of the high frequency bypass capacitor leads is critical. Parasitic inductance due to long leads works against the low impedance created by the bypass capacitor. The ground for the load impedance should be at the same physical location as the bypass capacitor grounds. For larger value capacitors, which are intended to be effective at lower frequencies, the current return path distance is less critical.

LAYOUT AND GROUNDING CONSIDERATIONS

GROUNDING

A ground plane layer is important in densely packed printed circuit boards (PCB) to minimize parasitic inductances. However, an understanding of where the current flows in a circuit is critical to implementing effective high speed circuit design. The length of the current path is directly proportional to the magnitude of parasitic inductances and thus the high frequency impedance of the path. High speed currents in an inductive ground return create unwanted voltage noise. Broad ground plane areas reduce parasitic inductance.

INPUT CAPACITANCE

Along with bypassing and ground, high speed amplifiers can be sensitive to parasitic capacitance between the inputs and ground. Even 1 pF or 2 pF of capacitance reduces the input impedance at high frequencies, in turn increasing the gain of the amplifier, which causes peaking of the frequency response or even oscillations if severe enough. Place the external passive components that are connected to the input pins as close as possible to the inputs to avoid parasitic capacitance. The ground and power planes must be kept at a distance of at least 0.05 mm from the input pins on all layers of the board.

OUTPUT CAPACITANCE

To a lesser extent, parasitic capacitances on the output can cause peaking of the frequency response. The following two methods minimize its effect:

- Put a small value resistor in series with the output to isolate the load capacitance from the output stage of the amplifier (see Figure 12).
- Increase the phase margin by increasing the gain of the amplifier or by increasing the value of the feedback resistor.

INPUT-TO-OUTPUT COUPLING

To minimize capacitive coupling, the input and output signal traces should not be parallel. When they are not parallel, they help reduce unwanted positive feedback.

EXTERNAL COMPONENTS AND STABILITY

The AD8007/AD8008 are current feedback amplifiers and, to a first order, the feedback resistor determines the bandwidth and stability. The gain, load impedance, supply voltage, and input impedances also have an effect.

Figure 11 shows the effect of changing R_F on the bandwidth and peaking for a gain of 2. Increasing R_F reduces peaking but also reduces bandwidth. Figure 6 shows that for a given R_F increasing the gain also reduces peaking and bandwidth. Table 4 shows the recommended R_F and R_G values that optimize bandwidth with minimal peaking.

Table 4. Recommended Component Values

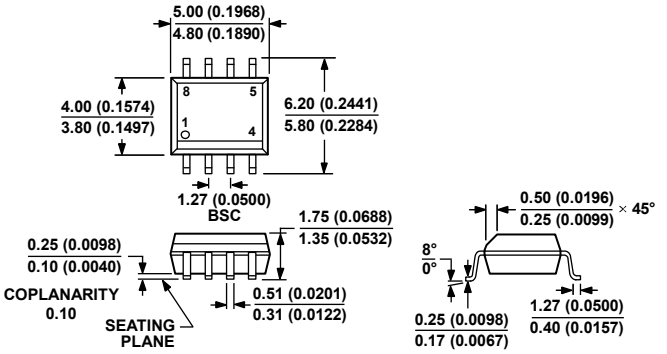
Gain	R_F (Ω)	R_G (Ω)	R_S (Ω)
−1	499	499	200
+1	499	Not applicable	200
+2	499	499	200
+5	499	124	200
+10	499	54.9	200

The load resistor also affects bandwidth, as shown in Figure 7 and Figure 10. A comparison between Figure 7 and Figure 10 also demonstrates the effect of gain and supply voltage.

When driving loads with a capacitive component, stability improves by using a series snub resistor, R_{SNUB}, at the output. The frequency and pulse responses for various capacitive loads are illustrated in Figure 12 and Figure 47, respectively.

For noninverting configurations, a resistor in series with the input, R_S, is needed to optimize stability for a gain of 1, as illustrated in Figure 8. For larger noninverting gains, the effect of a series resistor is reduced.

OUTLINE DIMENSIONS

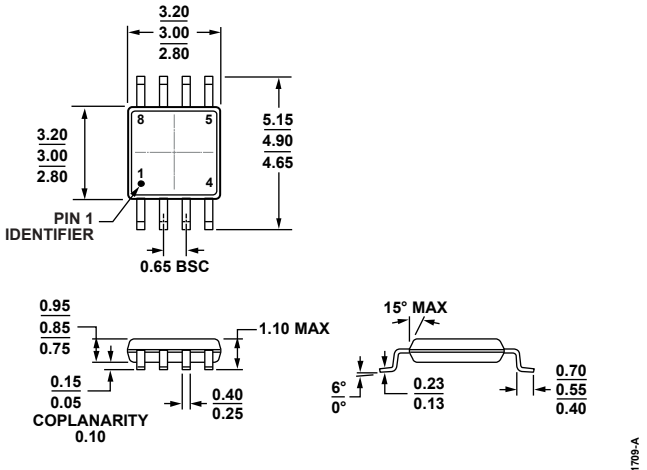


COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

012407-A

Figure 55. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)



COMPLIANT TO JEDEC STANDARDS MO-187-AA

091709-A

Figure 56. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

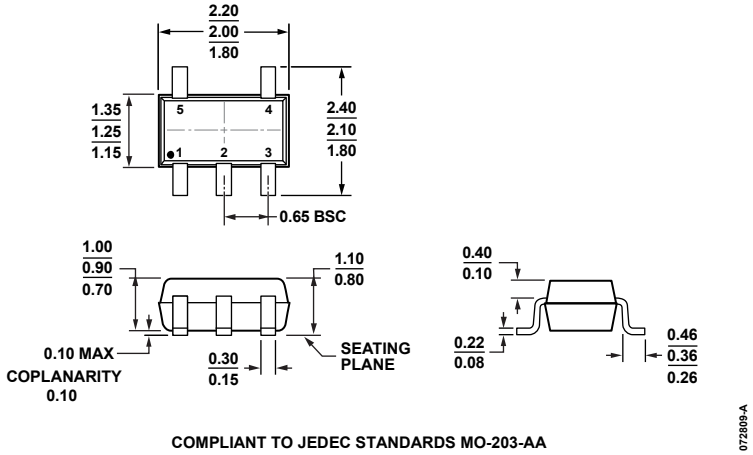


Figure 57. 5-Lead Thin Shrink Small Outline Transistor Package [SC70]
(KS-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Outline	Branding
AD8007AKS-R2	−40°C to +85°C	5-Lead SC70	KS-5	HTA
AD8007AKSZ-R2[1]	−40°C to +85°C	5-Lead SC70	KS-5	HTC
AD8007AKSZ-REEL[1]	−40°C to +85°C	5-Lead SC70	KS-5	HTC
AD8007AKSZ-REEL7[1]	−40°C to +85°C	5-Lead SC70	KS-5	HTC
AD8007AR	−40°C to +85°C	8-Lead SOIC	R-8	
AD8007AR-REEL	−40°C to +85°C	8-Lead SOIC	R-8	
AD8007AR-REEL7	−40°C to +85°C	8-Lead SOIC	R-8	
AD8007ARZ[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8007ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8007ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8008AR	−40°C to +85°C	8-Lead SOIC	R-8	
AD8008AR-REEL7	−40°C to +85°C	8-Lead SOIC	R-8	
AD8008AR-REEL	−40°C to +85°C	8-Lead SOIC	R-8	
AD8008ARZ[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8008ARZ-REEL7[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8008ARZ-REEL[1]	−40°C to +85°C	8-Lead SOIC	R-8	
AD8008ARM	−40°C to +85°C	8-Lead MSOP	RM-8	H2B
AD8008ARM-REEL	−40°C to +85°C	8-Lead MSOP	RM-8	H2B
AD8008ARM-REEL7	−40°C to +85°C	8-Lead MSOP	RM-8	H2B
AD8008ARMZ[1]	−40°C to +85°C	8-Lead MSOP	RM-8	H2B#
AD8008ARMZ-REEL[1]	−40°C to +85°C	8-Lead MSOP	RM-8	H2B#
AD8008ARMZ-REEL7[1]	−40°C to +85°C	8-Lead MSOP	RM-8	H2B#

[1] Z = RoHS Compliant Part, # denotes RoHS compliant part may be top or bottom marked.

NOTES

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