



**THE DATASHEET OF
AD7528JRZ-REEL7**



FEATURES

- On-Chip Latches for Both DACs
- +5 V to +15 V Operation
- DACs Matched to 1%
- Four Quadrant Multiplication
- TTL/CMOS Compatible
- Latch Free (Protection Schottkys not Required)

APPLICATIONS

- Digital Control of:
 - Gain/Attenuation
 - Filter Parameters
 - Stereo Audio Circuits
 - X-Y Graphics

GENERAL DESCRIPTION

The AD7528 is a monolithic dual 8-bit digital/analog converter featuring excellent DAC-to-DAC matching. It is available in skinny 0.3" wide 20-lead DIPs and in 20-lead surface mount packages.

Separate on-chip latches are provided for each DAC to allow easy microprocessor interface.

Data is transferred into either of the two DAC data latches via a common 8-bit TTL/CMOS compatible input port. Control input $\overline{\text{DAC A/DAC B}}$ determines which DAC is to be loaded. The AD7528's load cycle is similar to the write cycle of a random access memory and the device is bus compatible with most 8-bit microprocessors, including 6800, 8080, 8085, Z80.

The device operates from a +5 V to +15 V power supply, dissipating only 20 mW of power.

Both DACs offer excellent four quadrant multiplication characteristics with a separate reference input and feedback resistor for each DAC.

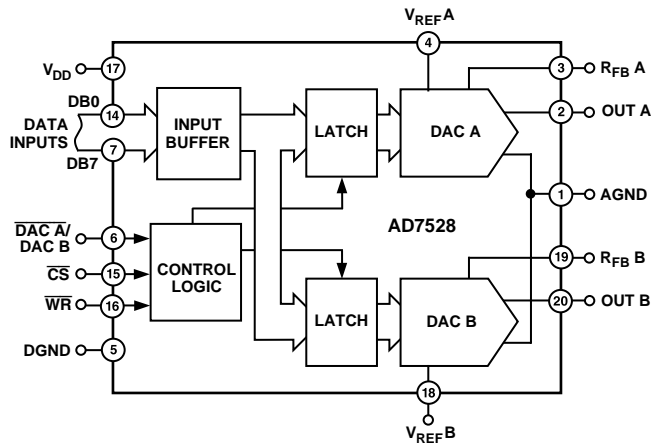
PRODUCT HIGHLIGHTS

1. DAC-to-DAC matching: since both of the AD7528 DACs are fabricated at the same time on the same chip, precise matching and tracking between DAC A and DAC B is inherent. The AD7528's matched CMOS DACs make a whole new range of applications circuits possible, particularly in the audio, graphics and process control areas.
2. Small package size: combining the inputs to the on-chip DAC latches into a common data bus and adding a $\overline{\text{DAC A/DAC B}}$ select line has allowed the AD7528 to be packaged in either a small 20-lead DIP, SOIC or PLCC.

REV. B

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FUNCTIONAL BLOCK DIAGRAM



ORDERING GUIDE¹

Model ²	Temperature Ranges	Relative Accuracy	Gain Error	Package Options ³
AD7528JN	-40°C to +85°C	±1 LSB	±4 LSB	N-20
AD7528KN	-40°C to +85°C	±1/2 LSB	±2 LSB	N-20
AD7528LN	-40°C to +85°C	±1/2 LSB	±1 LSB	N-20
AD7528JP	-40°C to +85°C	±1 LSB	±4 LSB	P-20A
AD7528KP	-40°C to +85°C	±1/2 LSB	±2 LSB	P-20A
AD7528LP	-40°C to +85°C	±1/2 LSB	±1 LSB	P-20A
AD7528JR	-40°C to +85°C	±1 LSB	±4 LSB	R-20
AD7528KR	-40°C to +85°C	±1/2 LSB	±2 LSB	R-20
AD7528LR	-40°C to +85°C	±1/2 LSB	±1 LSB	R-20
AD7528AQ	-40°C to +85°C	±1 LSB	±4 LSB	Q-20
AD7528BQ	-40°C to +85°C	±1/2 LSB	±2 LSB	Q-20
AD7528CQ	-40°C to +85°C	±1/2 LSB	±1 LSB	Q-20
AD7528SQ	-55°C to +125°C	±1 LSB	±4 LSB	Q-20
AD7528TQ	-55°C to +125°C	±1/2 LSB	±2 LSB	Q-20
AD7528UQ	-55°C to +125°C	±1/2 LSB	±1 LSB	Q-20

NOTES

¹Analog Devices reserves the right to ship side-brazed ceramic in lieu of cerdip. Parts will be marked with cerdip designator "Q."

²Processing to MIL-STD-883C, Class B is available. To order, add suffix "/883B" to part number. For further information, see Analog Devices' 1990 Military Products Databook.

³N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

AD7528—SPECIFICATIONS ($V_{REF A} = V_{REF B} = +10 V$; $OUT A = OUT B = 0 V$ unless otherwise noted)

Parameter	Version ¹	$V_{DD} = +5 V$		$V_{DD} = +15 V$		Units	Test Conditions/Comments	
		$T_A = +25^\circ C$	T_{MIN}, T_{MAX}	$T_A = +25^\circ C$	T_{MIN}, T_{MAX}			
STATIC PERFORMANCE²								
Resolution	All	8	8	8	8	Bits	This is an Endpoint Linearity Specification	
Relative Accuracy	J, A, S	± 1	± 1	± 1	± 1	LSB max		
	K, B, T	$\pm 1/2$	$\pm 1/2$	$\pm 1/2$	$\pm 1/2$	LSB max		
	L, C, U	$\pm 1/2$	$\pm 1/2$	$\pm 1/2$	$\pm 1/2$	LSB max		
Differential Nonlinearity	All	± 1	± 1	± 1	± 1	LSB max	All Grades Guaranteed Monotonic Over Full Operating Temperature Range Measured Using Internal $R_{FB A}$ and $R_{FB B}$ Both DAC Latches Loaded with 11111111 Gain Error is Adjustable Using Circuits of Figures 4 and 5	
Gain Error	J, A, S	± 4	± 6	± 4	± 5	LSB max		
	K, B, T	± 2	± 4	± 2	± 3	LSB max		
	L, C, U	± 1	± 3	± 1	± 1	LSB max		
Gain Temperature Coefficient ³ $\Delta\text{Gain}/\Delta\text{Temperature}$	All	± 0.007	± 0.007	± 0.0035	± 0.0035	%/°C max	DAC Latches Loaded with 00000000	
Output Leakage Current OUT A (Pin 2)	All	± 50	± 400	± 50	± 200	nA max		
OUT B (Pin 20)	All	± 50	± 400	± 50	± 200	nA max		
Input Resistance ($V_{REF A}, V_{REF B}$)	All	8	8	8	8	k Ω min		
$V_{REF A}/V_{REF B}$ Input Resistance Match	All	15	15	15	15	k Ω max	Input Resistance TC = -300 ppm/°C, Typical Input Resistance is 11 k Ω	
	All	± 1	± 1	± 1	± 1	% max		
DIGITAL INPUTS⁴								
Input High Voltage V_{IH}	All	2.4	2.4	13.5	13.5	V min	$V_{IN} = 0$ or V_{DD}	
Input Low Voltage V_{IL}	All	0.8	0.8	1.5	1.5	V max		
Input Current I_{IN}	All	± 1	± 10	± 1	± 10	μA max		
Input Capacitance DB0–DB7	All	10	10	10	10	pF max		
WR, CS, DAC A/DAC B	All	15	15	15	15	pF max		
SWITCHING CHARACTERISTICS⁵								
Chip Select to Write Set Up Time t_{CS}	All	90	100	60	80	ns min	See Timing Diagram	
Chip Select to Write Hold Time t_{CH}	All	0	0	10	15	ns min		
DAC Select to Write Set Up Time t_{AS}	All	90	100	60	80	ns min		
DAC Select to Write Hold Time t_{AH}	All	0	0	10	15	ns min		
Data Valid to Write Set Up Time t_{DS}	All	80	90	30	40	ns min		
Data Valid to Write Hold Time t_{DH}	All	0	0	0	0	ns min		
Write Pulsewidth t_{WR}	All	90	100	60	80	ns min		
POWER SUPPLY								
I_{DD}	All	2	2	2	2	mA max		See Figure 3 All Digital Inputs V_{IL} or V_{IH} All Digital Inputs 0 V or V_{DD}
	All	100	500	100	500	μA max		

AC PERFORMANCE CHARACTERISTICS⁵ (Measured Using Recommended P.C. Board Layout (Figure 7) and AD644 as Output Amplifiers)

Parameter	Version ¹	$V_{DD} = +5 V$		$V_{DD} = +15 V$		Units	Test Conditions/Comments
		$T_A = +25^\circ C$	T_{MIN}, T_{MAX}	$T_A = +25^\circ C$	T_{MIN}, T_{MAX}		
DC SUPPLY REJECTION ($\Delta\text{GAIN}/\Delta V_{DD}$)	All	0.02	0.04	0.01	0.02	% per % max	$\Delta V_{DD} = \pm 5\%$
CURRENT SETTLING TIME ²	All	350	400	180	200	ns max	To 1/2 LSB. OUT A/OUT B Load = 100 Ω . WR = CS = 0 V. DB0–DB7 = 0 V to V_{DD} or V_{DD} to 0 V
PROPAGATION DELAY (From Digital Input to 90% of Final Analog Output Current)	All	220	270	80	100	ns max	$V_{REF A} = V_{REF B} = +10 V$ OUT A, OUT B Load = 100 Ω $C_{EXT} = 13$ pF WR = CS = 0 V DB0–DB7 = 0 V to V_{DD} or V_{DD} to 0 V
DIGITAL-TO-ANALOG GLITCH IMPULSE	All	160		440		nV sec typ	For Code Transition 00000000 to 11111111
OUTPUT CAPACITANCE							
$C_{OUT A}$	All	50	50	50	50	pF max	DAC Latches Loaded with 00000000
$C_{OUT B}$		50	50	50	50	pF max	
$C_{OUT A}$		120	120	120	120	pF max	DAC Latches Loaded with 11111111
$C_{OUT B}$		120	120	120	120	pF max	
AC FEEDTHROUGH⁶							
$V_{REF A}$ to OUT A	All	-70	-65	-70	-65	dB max	$V_{REF A}, V_{REF B} = 20 V$ p-p Sine Wave @ 100 kHz
$V_{REF B}$ to OUT B		-70	-65	-70	-65	dB max	

Parameter	Version ¹	V _{DD} = +5 V		V _{DD} = +15 V		Units	Test Conditions/Comments
		T _A = +25°C	T _{MIN} , T _{MAX}	T _A = +25°C	T _{MIN} , T _{MAX}		
CHANNEL-TO-CHANNEL ISOLATION V _{REF} A to OUT B	All	-77		-77		dB typ	Both DAC Latches Loaded with 11111111. V _{REF} A = 20 V p-p Sine Wave @ 100 kHz V _{REF} B = 0 V see Figure 6.
		-77		-77		dB typ	
DIGITAL CROSSTALK	All	30		60		nV sec typ	Measured for Code Transition 00000000 to 11111111
HARMONIC DISTORTION	All	-85		-85		dB typ	V _{IN} = 6 V rms @ 1 kHz

NOTES

- ¹Temperature Ranges are J, K, L Versions: -40°C to +85°C
A, B, C Versions: -40°C to +85°C
S, T, U Versions: -55°C to +125°C
- ²Specifications applies to both DACs in AD7528.
- ³Guaranteed by design but not production tested.
- ⁴Logic inputs are MOS Gates. Typical input current (+25°C) is less than 1 nA.
- ⁵These characteristics are for design guidance only and are not subject to test.
- ⁶Feedthrough can be further reduced by connecting the metal lid on the ceramic package (suffix D) to DGND.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

- V_{DD} to AGND 0 V, +17 V
- V_{DD} to DGND 0 V, +17 V
- AGND to DGND V_{DD} + 0.3 V
- DGND to AGND V_{DD} + 0.3 V
- Digital Input Voltage to DGND -0.3 V, V_{DD} + 0.3 V
- V_{PIN2}, V_{PIN20} to AGND -0.3 V, V_{DD} + 0.3 V
- V_{REF} A, V_{REF} B to AGND ±25 V
- V_{RFB} A, V_{RFB} B to AGND ±25 V
- Power Dissipation (Any Package) to +75°C 450 mW
Derates above +75°C by 6 mW/°C
- Operating Temperature Range
 - Commercial (J, K, L) Grades -40°C to +85°C
 - Industrial (A, B, C) Grades -40°C to +85°C
 - Extended (S, T, U) Grades -55°C to +125°C
- Storage Temperature -65°C to +150°C
- Lead Temperature (Soldering, 10 secs) +300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not insert this device into powered sockets. Remove power before insertion or removal.

TERMINOLOGY

Relative Accuracy

Relative accuracy or endpoint nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero and full scale and is normally expressed in LSBs or as a percentage of full scale reading.

Differential Nonlinearity

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB max over the operating temperature range ensures monotonicity.

Gain Error

Gain error or full-scale error is a measure of the output error between an ideal DAC and the actual device output. For the

AD7528, ideal maximum output is V_{REF} - 1 LSB. Gain error of both DACs is adjustable to zero with external resistance.

Output Capacitance

Capacitance from OUT A or OUT B to AGND.

Digital to Analog Glitch Impulse

The amount of charge injected from the digital inputs to the analog output when the inputs change state. This is normally specified as the area of the glitch in either pA-secs or nV-secs depending upon whether the glitch is measured as a current or voltage signal. Glitch impulse is measured with V_{REF} A, V_{REF} B = AGND.

Propagation Delay

This is a measure of the internal delays of the circuit and is defined as the time from a digital input change to the analog output current reaching 90% of its final value.

Channel-to-Channel Isolation

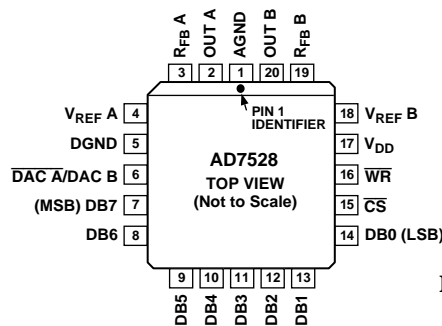
The proportion of input signal from one DAC's reference input which appears at the output of the other DAC, expressed as a ratio in dB.

Digital Crosstalk

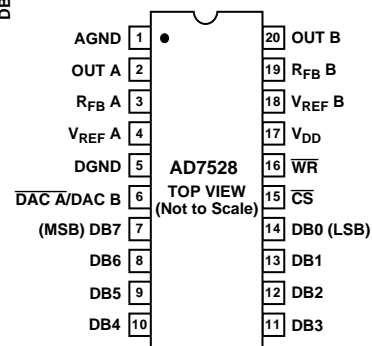
The glitch energy transferred to the output of one converter due to a change in digital input code to the other converter. Specified in nV secs.

PIN CONFIGURATIONS

PLCC



DIP, SOIC



AD7528

INTERFACE LOGIC INFORMATION

DAC Selection:

Both DAC latches share a common 8-bit input port. The control input $\overline{\text{DAC A/DAC B}}$ selects which DAC can accept data from the input port.

Mode Selection:

Inputs $\overline{\text{CS}}$ and $\overline{\text{WR}}$ control the operating mode of the selected DAC. See Mode Selection Table below.

Write Mode:

When $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are both low the selected DAC is in the write mode. The input data latches of the selected DAC are transparent and its analog output responds to activity on DB0–DB7.

Hold Mode:

The selected DAC latch retains the data which was present on DB0–DB7 just prior to $\overline{\text{CS}}$ or $\overline{\text{WR}}$ assuming a high state. Both analog outputs remain at the values corresponding to the data in their respective latches.

Mode Selection Table

DAC A/DAC B	$\overline{\text{CS}}$	$\overline{\text{WR}}$	DAC A	DAC B
L	L	L	WRITE	HOLD
H	L	L	HOLD	WRITE
X	H	X	HOLD	HOLD
X	X	H	HOLD	HOLD

L = Low State; H = High State; X = Don't Care.

WRITE CYCLE TIMING DIAGRAM



- NOTES:
- ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF V_{DD} .
 $V_{DD} = +5V$, $t_r = t_f = 20\text{ns}$;
 $V_{DD} = +15V$, $t_r = t_f = 40\text{ns}$;
 - TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_{IH} + V_{IL}}{2}$

CIRCUIT INFORMATION—D/A SECTION

The AD7528 contains two identical 8-bit multiplying D/A converters, DAC A and DAC B. Each DAC consists of a highly stable thin film R-2R ladder and eight N-channel current steering switches. A simplified D/A circuit for DAC A is shown in

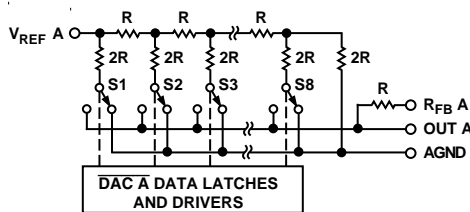


Figure 1. Simplified Functional Circuit for DAC A

Figure 1. An inverted R-2R ladder structure is used, that is, binary weighted currents are switched between the DAC output and AGND thus maintaining fixed currents in each ladder leg independent of switch state.

EQUIVALENT CIRCUIT ANALYSIS

Figure 2 shows an approximate equivalent circuit for one of the AD7528's D/A converters, in this case DAC A. A similar equivalent circuit can be drawn for DAC B. Note that AGND (Pin 1) is common for both DAC A and DAC B.

The current source I_{LEAKAGE} is composed of surface and junction leakages and, as with most semiconductor devices, approximately doubles every 10°C . The resistor R_O as shown in Figure 2 is the equivalent output resistance of the device which varies with input code (excluding all 0s code) from $0.8R$ to $2R$. R is typically $11\text{ k}\Omega$. C_{OUT} is the capacitance due to the N-channel switches and varies from about 50 pF to 120 pF depending upon the digital input. $g(V_{\text{REF A}}, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage $V_{\text{REF A}}$ and the transfer function of the R-2R ladder.

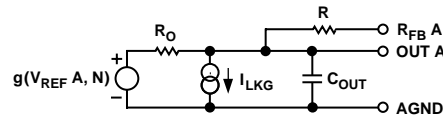


Figure 2. Equivalent Analog Output Circuit of DAC A

CIRCUIT INFORMATION—DIGITAL SECTION

The input buffers are simple CMOS inverters designed such that when the AD7528 is operated with $V_{DD} = 5\text{ V}$, the buffer converts TTL input levels (2.4 V and 0.8 V) into CMOS logic levels. When V_{IN} is in the region of 2.0 volts to 3.5 volts the input buffers operate in their linear region and pass a quiescent current, see Figure 3. To minimize power supply currents it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible.

The AD7528 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15\text{ volts}$. With $V_{DD} = +15\text{ V}$ the input logic levels are CMOS compatible only, i.e., 1.5 V and 13.5 V .

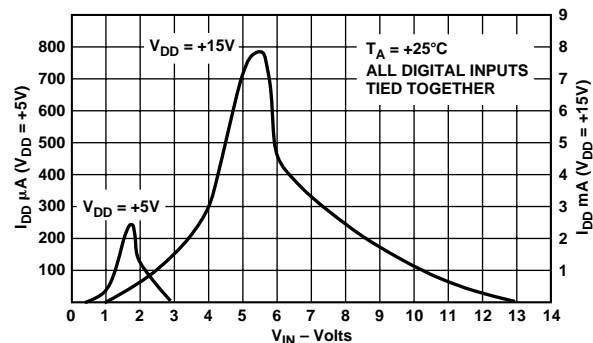


Figure 3. Typical Plots of Supply Current, I_{DD} vs. Logic Input Voltage V_{IN} , for $V_{DD} = +5\text{ V}$ and $+15\text{ V}$



NOTES:
¹R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE III FOR RECOMMENDED VALUES.
²C1, C2 PHASE COMPENSATION (10pF–15pF) IS REQUIRED WHEN USING HIGH SPEED AMPLIFIERS TO PREVENT RINGING OR OSCILLATION.

Figure 4. Dual DAC Unipolar Binary Operation (2 Quadrant Multiplication); See Table I

Table I. Unipolar Binary Code Table

DAC Latch Contents	Analog Output (DAC A or DAC B)
MSB LSB	
1 1 1 1 1 1 1 1	$-V_{IN} \left(\frac{255}{256} \right)$
1 0 0 0 0 0 0 1	$-V_{IN} \left(\frac{129}{256} \right)$
1 0 0 0 0 0 0 0	$-V_{IN} \left(\frac{128}{256} \right) = -\frac{V_{IN}}{2}$
0 1 1 1 1 1 1 1	$-V_{IN} \left(\frac{127}{256} \right)$
0 0 0 0 0 0 0 1	$-V_{IN} \left(\frac{1}{256} \right)$
0 0 0 0 0 0 0 0	$-V_{IN} \left(\frac{0}{256} \right) = 0$

Note: 1 LSB = $(2^{-8})(V_{IN}) = \frac{1}{256}(V_{IN})$



NOTES:
¹R1, R2 AND R3, R4 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED. SEE TABLE III FOR RECOMMENDED VALUES. ADJUST R1 FOR $V_{OUT A} = 0V$ WITH CODE 10000000 IN DAC A LATCH. ADJUST R3 FOR $V_{OUT B} = 0V$ WITH CODE 10000000 IN DAC B LATCH.
²MATCHING AND TRACKING IS ESSENTIAL FOR RESISTOR PAIRS R6, R7 AND R9, R10.
³C1, C2 PHASE COMPENSATION (10pF–15pF) MAY BE REQUIRED IF A1/A3 IS A HIGH SPEED AMPLIFIER.

Figure 5. Dual DAC Bipolar Operation (4 Quadrant Multiplication); See Table II

Table II. Bipolar (Offset Binary) Code Table

DAC Latch Contents	Analog Output (DAC A or DAC B)
MSB LSB	
1 1 1 1 1 1 1 1	$+V_{IN} \left(\frac{127}{128} \right)$
1 0 0 0 0 0 0 1	
1 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1	$-V_{IN} \left(\frac{1}{128} \right)$
0 0 0 0 0 0 0 1	$-V_{IN} \left(\frac{127}{128} \right)$
0 0 0 0 0 0 0 0	$-V_{IN} \left(\frac{128}{128} \right)$

Note: 1 LSB = $(2^{-7})(V_{IN}) = \frac{1}{128}(V_{IN})$

Table III. Recommended Trim Resistor Values vs. Grade

Trim Resistor	J/A/S	K/B/T	L/C/U
R1; R3	1 k	500	200
R2; R4	330	150	82

AD7528

APPLICATIONS INFORMATION

Application Hints

To ensure system performance consistent with AD7528 specifications, careful attention must be given to the following points:

- GENERAL GROUND MANAGEMENT:** AC or transient voltages between the AD7528 AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7528. In more complex systems where the AGND-DGND intertie is on the backplane, it is recommended that diodes be connected in inverse parallel between the AD7528 AGND and DGND pins (1N914 or equivalent).
- OUTPUT AMPLIFIER OFFSET:** CMOS DACs exhibit a code-dependent output resistance which in turn causes a code-dependent amplifier noise gain. The effect is a code-dependent differential nonlinearity term at the amplifier output which depends on V_{OS} (V_{OS} is amplifier input offset voltage). This differential nonlinearity term adds to the R/2R differential nonlinearity. To maintain monotonic operation, it is recommended that amplifier V_{OS} be no greater than 10% of 1 LSB over the temperature range of interest.
- HIGH FREQUENCY CONSIDERATIONS:** The output capacitance of a CMOS DAC works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

DYNAMIC PERFORMANCE

The dynamic performance of the two DACs in the AD7528 will depend upon the gain and phase characteristics of the output amplifiers together with the optimum choice of the PC board layout and decoupling components. Figure 6 shows the relation

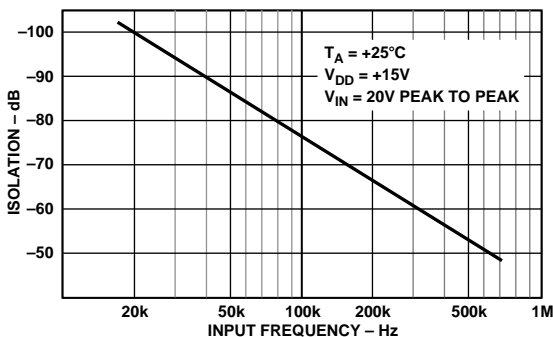


Figure 6. Channel-to-Channel Isolation

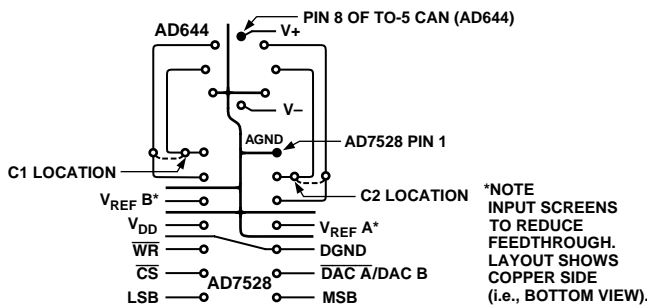


Figure 7. Suggested PC Board Layout for AD7528 with AD644 Dual Op Amp

ship between input frequency and channel to channel isolation. Figure 7 shows a printed circuit layout for the AD7528 and the AD644 dual op amp which minimizes feedthrough and crosstalk.

SINGLE SUPPLY APPLICATIONS

The AD7528 DAC R-2R ladder termination resistors are connected to AGND within the device. This arrangement is particularly convenient for single supply operation because AGND may be biased at any voltage between DGND and V_{DD} . Figure 8 shows a circuit which provides two +5 V to +8 V analog outputs by biasing AGND +5 V up from DGND. The two DAC reference inputs are tied together and a reference input voltage is obtained without a buffer amplifier by making use of the constant and matched impedances of the DAC A and DAC B reference inputs. Current flows through the two DAC R-2R ladders into R1 and R1 is adjusted until the $V_{REF A}$ and $V_{REF B}$ inputs are at +2 V. The two analog output voltages range from +5 V to +8 V for DAC codes 00000000 to 11111111.

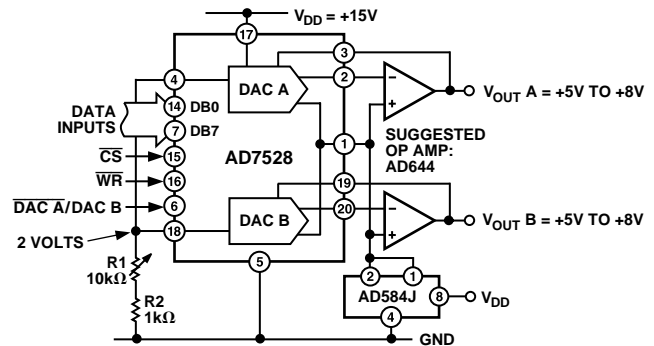


Figure 8. AD7528 Single Supply Operation

Figure 9 shows DAC A of the AD7528 connected in a positive reference, voltage switching mode. This configuration is useful in that V_{OUT} is the same polarity as V_{IN} allowing single supply operation. However, to retain specified linearity, V_{IN} must be in the range 0 V to +2.5 V and the output buffered or loaded with a high impedance, see Figure 10. Note that the input voltage is connected to the DAC OUT A and the output voltage is taken from the DAC $V_{REF A}$ pin.



Figure 9. AD7528 in Single Supply, Voltage Switching Mode

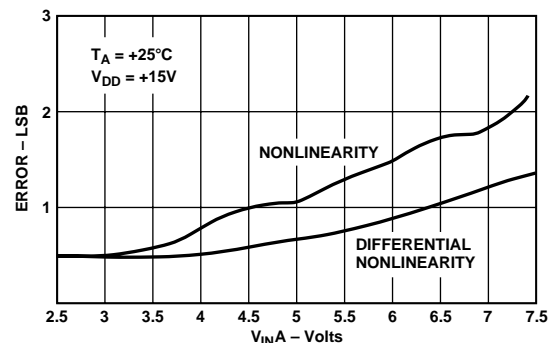


Figure 10. Typical AD7528 Performance in Single Supply Voltage Switching Mode (K/B/T, L/C/U Grades)

MICROPROCESSOR INTERFACE

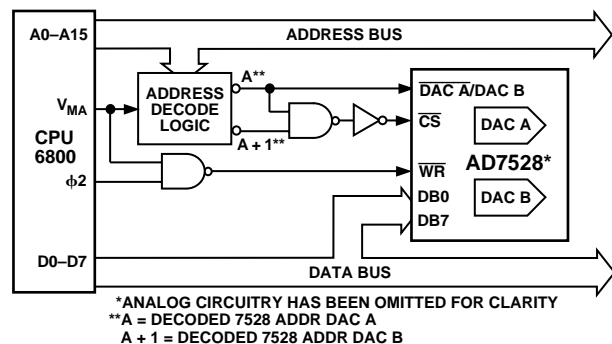


Figure 11. AD7528 Dual DAC to 6800 CPU Interface



Figure 12. AD7528 Dual DAC to 8085 CPU Interface

PROGRAMMABLE WINDOW COMPARATOR

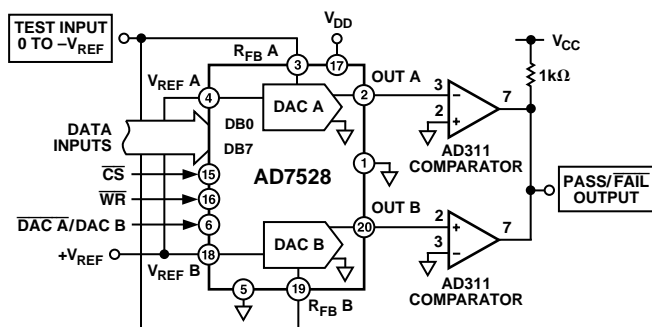


Figure 13. Digitally Programmable Window Comparator (Upper and Lower Limit Detector)

In the circuit of Figure 13 the AD7528 is used to implement a programmable window comparator. DACs A and B are loaded with the required upper and lower voltage limits for the test, respectively. If the test input is not within the programmed limits, the pass/fail output will indicate a fail (logic zero).

PROGRAMMABLE STATE VARIABLE FILTER

In this state variable or universal filter configuration (Figure 14) DACs A1 and B1 control the gain and Q of the filter characteristic while DACs A2 and B2 control the cutoff frequency, f_c . DACs A2 and B2 must track accurately for the simple expression for f_c to hold. This is readily accomplished by the AD7528. Op amps are $2 \times$ AD644. C3 compensates for the effects of op amp gain bandwidth limitations.

The filter provides low pass, high pass and band pass outputs and is ideally suited for applications where microprocessor control of filter parameters is required, e.g., equalizer, tone controls, etc.

Programmable range for component values shown is $f_c = 0$ kHz to 15 kHz and $Q = 0.3$ to 4.5.

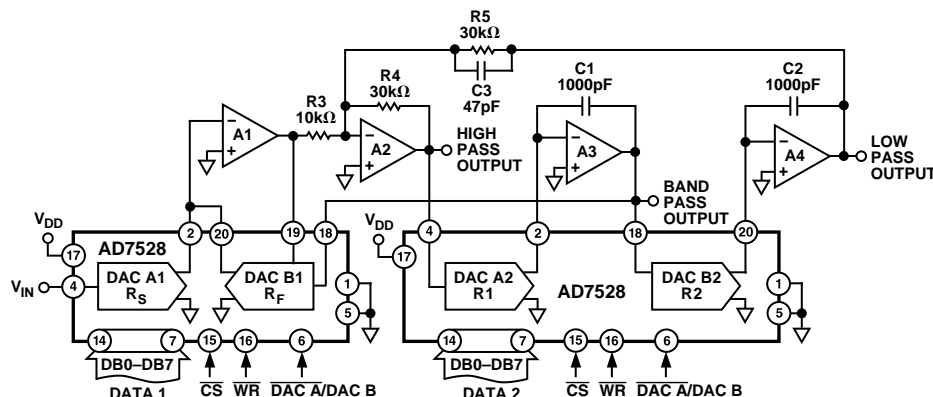


Figure 14. Digitally Controlled State Variable Filter

CIRCUIT EQUATIONS

$$C1 = C2, R1 = R2, R4 = R5$$

$$f_c = \frac{1}{2\pi R1 C1}$$

$$Q = \frac{R3}{R4} \times \frac{R_F}{R_{FBB1}}$$

$$A_o = \frac{R_F}{R_S}$$

NOTE
 DAC Equivalent Resistance
 Equals

$$\frac{256 \times (\text{DAC Ladder Resistance})}{\text{DAC Digital Code}}$$

AD7528

DIGITALLY CONTROLLED DUAL TELEPHONE ATTENUATOR

In this configuration the AD7528 functions as a 2-channel digitally controlled attenuator. Ideal for stereo audio and telephone signal level control applications. Table IV gives input codes vs. attenuation for a 0 dB to 15.5 dB range.

$$\text{Input Code} = 256 \times 10^{\exp\left(-\frac{\text{Attenuation, dB}}{20}\right)}$$

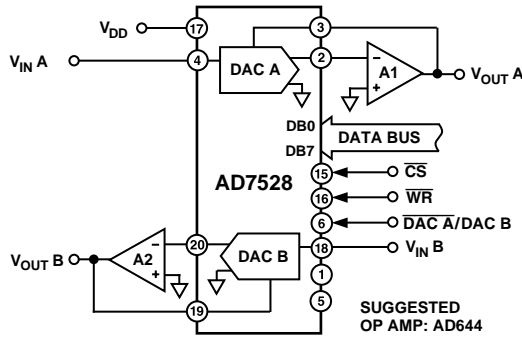


Figure 15. Digitally Controlled Dual Telephone Attenuator

Table IV. Attenuation vs. DAC A, DAC B Code for the Circuit of Figure 15

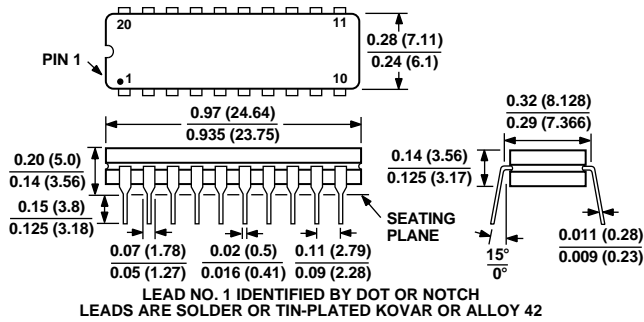
Attn. dB	DAC Input Code	Code In Decimal	Attn. dB	DAC Input Code	Code In Decimal
0.0	11111111	255	8.0	01100110	102
0.5	11110010	242	8.5	01100000	96
1.0	11100100	228	9.0	01011011	91
1.5	11010111	215	9.5	01010110	86
2.0	11001011	203	10.0	01010001	81
2.5	11000000	192	10.5	01001100	76
3.0	10110101	181	11.0	01001000	72
3.5	10101011	171	11.5	01000100	68
4.0	10100010	162	12.0	01000000	64
4.5	10011000	152	12.5	00111101	61
5.0	10010000	144	13.0	00111001	57
5.5	10001000	136	13.5	00110110	54
6.0	10000000	128	14.0	00110011	51
6.5	01111001	121	14.5	00110000	48
7.0	01110010	114	15.0	00101110	46
7.5	01101100	108	15.5	00101011	43

For further applications information the reader is referred to Analog Devices Application Note on the AD7528.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

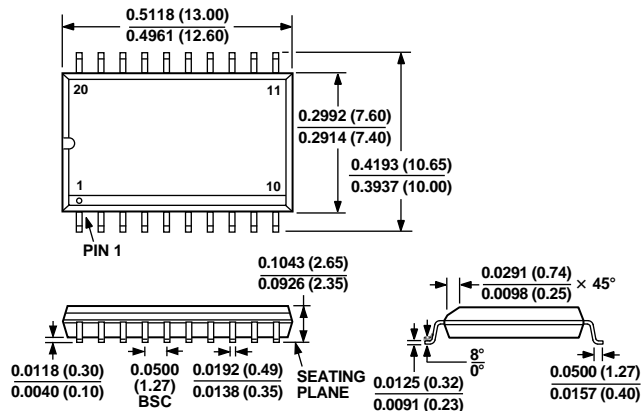
20-Lead Cerdip (Q-20)



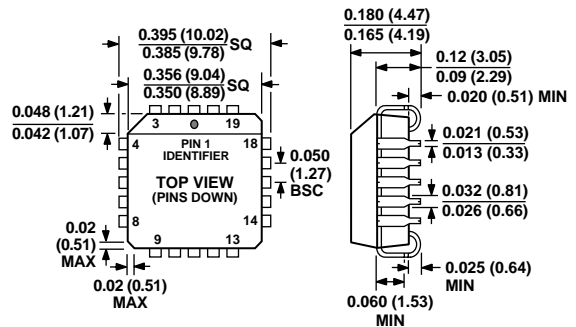
20-Lead Plastic DIP (N-20)



20-Lead SOIC (R-20)



20-Lead Plastic Leaded Chip Carrier (P-20A)



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