# THE DATASHEET OF

# AD7147AACBZ-RL

# CapTouch Programmable Controller for Single-Electrode Capacitance Sensors

# AD7147A

## FEATURES

- **Programmable capacitance-to-digital converter (CDC)**
  - **Femtofarad (fF) resolution**
  - **13 capacitance sensor inputs**
  - **9 ms update rate, all 13 sensor inputs**
  - **No external RC components required**
  - **Automatic conversion sequencer**
- **On-chip automatic calibration logic**
  - **Automatic compensation for environmental changes**
  - **Automatic adaptive threshold and sensitivity levels**
- **Register map is compatible with the AD714x**
- **On-chip RAM to store calibration data**
- **Serial peripheral interface (SPI) (AD7147A)**
- **I²C-compatible serial interface (AD7147A-1)**
- **Separate $V_{DRIVE}$ level for serial interface**
- **Interrupt output and general-purpose input/output (GPIO)**
- **25-ball, 2.3 mm × 2.1 mm WLCSP**
- **2.6 V to 3.6 V supply voltage**
- **Low operating current**
  - **Full power mode: 1 mA**
  - **Low power mode: 28.96 µA**

## APPLICATIONS

- **Cell phones**
- **Personal music and multimedia players**
- **Smart handheld devices**
- **Television, A/V, and remote controls**
- **Gaming consoles**
- **Digital still cameras**

## GENERAL DESCRIPTION

The AD7147A CapTouch™ controller is designed for use with capacitance sensors implementing functions such as buttons, scroll bars, and wheels. The sensors need only one PCB layer, enabling ultrathin applications.

The AD7147A is an integrated CDC with on-chip environmental calibration. The CDC has 13 inputs channeled through a switch matrix to a 16-bit, 250 kHz sigma-delta (Σ-Δ) converter. The CDC is capable of sensing changes in the capacitance of the external sensors and uses this information to register a sensor activation. By programming the registers, the user has full control over the CDC setup.

High resolution sensors require minor software to run on the host processor and may require two PCB layers.

## FUNCTIONAL BLOCK DIAGRAM

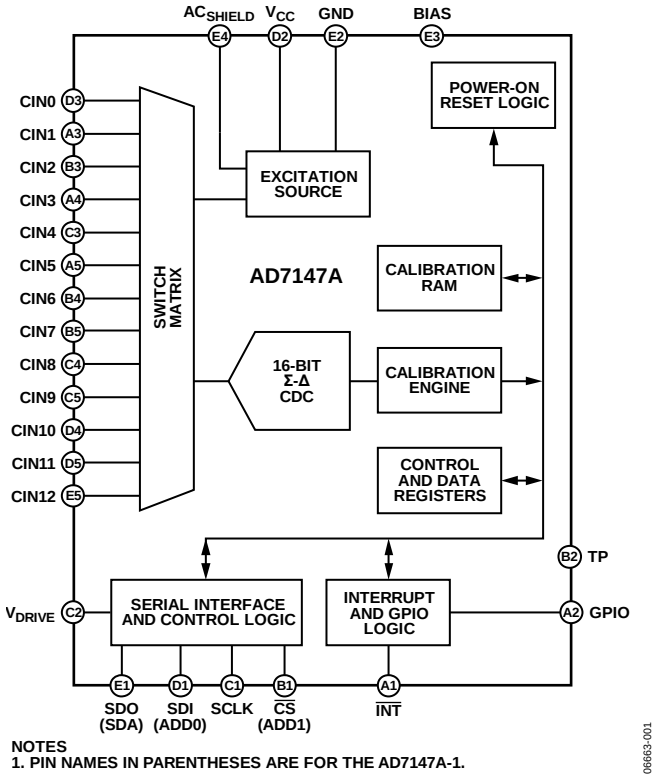


*Figure 1.*

The AD7147A is designed for single electrode capacitance sensors (grounded sensors). There is an active shield output to minimize noise pickup in the sensor.

The AD7147A has on-chip calibration logic to compensate for changes in the ambient environment. The calibration sequence is performed automatically and at continuous intervals as long as the sensors are not touched. This ensures that there are no false or nonregistering touches on the external sensors due to a changing environment.

The AD7147A has an SPI-compatible serial interface, and the AD7147A-1 has an I²C®-compatible serial interface. Both parts have an interrupt output, as well as a GPIO. There is a $V_{DRIVE}$ pin to set the voltage level for the serial interface independent of $V_{CC}$.

The AD7147A is available in a 25-ball, 2.3 mm × 2.1 mm WLCSP and operates from a 2.6 V to 3.6 V supply. The operating current consumption in low power mode is typically 28.96 µA for 13 sensors.

**Rev. B**



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# TABLE OF CONTENTS



## REVISION HISTORY

**12/09—Rev. A to Rev. B**

Changes to Figure 1 ... 1
Changes to Figure 5, Figure 6, and Pin Description for B2 ... 8
Changes to Figure 59 and Figure 60 ... 39
Changes to Ordering Guide ... 68

**3/09—Rev. 0 to Rev. A**

Changes to Ordering Guide ... 68

**1/09—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{CC}$ = 2.6 V to 3.6 V, $T_A$ = −40°C to +85°C, unless otherwise noted.

**Table 1.**

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|---|---|---|---|
| CAPACITANCE-TO-DIGITAL CONVERTER | | | | | |
| Update Rate | 8.73 | 9 | 9.27 | ms | 12 conversion stages, decimation = 64 |
| | 17.46 | 18 | 18.54 | ms | 12 conversion stages, decimation = 128 |
| | 34.9 | 36 | 37.1 | ms | 12 conversion stages, decimation = 256 |
| Resolution | | 16 | | Bits | |
| CINx Input Range | | ±8 | | pF | |
| No Missing Codes | 16 | | | Bits | Guaranteed by design, but not production tested |
| CINx Input Leakage | | 25 | | nA | |
| Maximum Output Load | | | 20 | pF | Capacitance load on CINx to ground |
| Total Unadjusted Error | | | ±20 | % | |
| Output Noise (Peak-to-Peak) | | 12 | | Codes | Decimation rate = 64 |
| | | 7 | | Codes | Decimation rate = 128 |
| | | 3 | | Codes | Decimation rate = 256 |
| Output Noise (RMS) | | 1.1 | | Codes | Decimation rate = 64 |
| | | 0.8 | | Codes | Decimation rate = 128 |
| | | 0.5 | | Codes | Decimation rate = 256 |
| $C_{STRAY}$ Offset Range | | 20 | | pF | |
| $C_{STRAY}$ Offset Resolution | | 0.32 | | pF | |
| Low Power Mode Delay Accuracy | | | 4 | % | Percentage of 200 ms, 400 ms, 600 ms, or 800 ms |
| $AC_{SHIELD}$ | | | | | |
| Frequency | | 250 | | kHz | |
| Output Voltage | 0 | | $V_{CC}$ | V | Oscillating |
| Short-Circuit Source Current | | 10 | | mA | |
| Short-Circuit Sink Current | | 10 | | mA | |
| Maximum Output Load | | | 150 | pF | Capacitance load on $AC_{SHIELD}$ to ground |
| LOGIC INPUTS (SDI, SCLK, $\overline{CS}$, SDA, GPIO) | | | | | |
| Input High Voltage, $V_{IH}$ | 0.7 × $V_{DRIVE}$ | | | V | |
| Input Low Voltage, $V_{IL}$ | | | 0.4 | V | |
| Input High Current, $I_{IH}$ | −1 | | | µA | $V_{IN}$ = $V_{DRIVE}$ |
| Input Low Current, $I_{IL}$ | | | 1 | µA | $V_{IN}$ = GND |
| Hysteresis | | 150 | | mV | |
| OPEN-DRAIN OUTPUTS (SCLK, SDA, $\overline{INT}$) | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = −1 mA |
| Output High Leakage Current, $I_{OH}$ | | ±0.1 | ±1 | µA | $V_{OUT}$ = $V_{DRIVE}$ |
| LOGIC OUTPUTS (SDO, GPIO) | | | | | |
| Output Low Voltage, $V_{OL}$ | | | 0.4 | V | $I_{SINK}$ = 1 mA, $V_{DRIVE}$ = 1.65 V to 3.6 V |
| Output High Voltage, $V_{OH}$ | $V_{DRIVE}$ − 0.6 | | | V | $I_{SOURCE}$ = 1 mA, $V_{DRIVE}$ = 1.65 V to 3.6 V |
| GPO, SDO Floating State Leakage Current | | | ±1 | µA | Pin three-state, leakage measured to GND and $V_{CC}$ |
| POWER | | | | | |
| $V_{CC}$ | 2.6 | 3.3 | 3.6 | V | |
| $V_{DRIVE}$ | 1.65 | | 3.6 | V | Serial interface operating voltage |
| $I_{CC}$ | | 0.8 | 1 | mA | In full power mode, $V_{CC}$ + $V_{DRIVE}$, Register 0x00, Bits[15:14] = 00 |
| | | 1.1 | 1.3 | mA | In full power mode, $V_{CC}$ + $V_{DRIVE}$, Register 0x00, Bits[15:14] = 01 |
| | | 1.2 | 1.5 | mA | In full power mode, $V_{CC}$ + $V_{DRIVE}$, Register 0x00, Bits[15:14] = 10 |
| | | 1.6 | 1.8 | mA | In full power mode, $V_{CC}$ + $V_{DRIVE}$, Register 0x00, Bits[15:14] = 11 |
| | | 15.5 | 24 | µA | Low power mode, converter idle, $V_{CC}$ + $V_{DRIVE}$, decimation = 256; Register 0x00, Bits[15:14] = 01 |
| | | 2.3 | 10 | µA | Full shutdown, $V_{CC}$ + $V_{DRIVE}$, Register 0x00, Bits[15:14] = 01 |

## AVERAGE CURRENT SPECIFICATIONS

**Table 2. Typical Average Current in Low Power Mode[1]**

| Low Power Mode Delay | Decimation Rate | Current Values of Conversion Stages (μA) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| 200 ms | 64 | 22.27 | 26.53 | 30.77 | 34.98 | 39.15 | 43.29 | 47.40 | 51.48 | 55.53 | 59.55 | 63.54 | 67.51 |
| | 128 | 27.95 | 36.37 | 44.66 | 52.84 | 60.89 | 68.82 | 76.64 | 84.34 | 91.94 | 99.42 | 106.80 | 114.08 |
| | 256 | 39.15 | 55.53 | 71.44 | 86.89 | 101.9 | 116.48 | 130.67 | 144.47 | 157.90 | 170.98 | 183.71 | 196.11 |
| 400 ms | 64 | 18.89 | 21.04 | 23.19 | 25.32 | 27.45 | 29.57 | 31.68 | 33.78. | 35.88 | 37.96 | 40.04 | 42.11 |
| | 128 | 21.76 | 26.03 | 30.27 | 34.48 | 38.66 | 42.80 | 46.92 | 51.00 | 55.05 | 59.08 | 63.07 | 67.04 |
| | 256 | 27.45 | 35.88 | 44.18 | 52.36 | 60.41 | 68.35 | 76.18 | 83.89 | 91.49 | 98.98 | 106.37 | 113.65 |
| 600 ms | 64 | 17.76 | 19.20 | 20.63 | 22.06 | 23.49 | 24.91 | 26.33 | 27.75 | 29.16 | 30.57 | 31.98 | 33.38 |
| | 128 | 19.68 | 22.54 | 25.39 | 28.22 | 31.04 | 33.85 | 36.64 | 39.42 | 42.18 | 44.93 | 47.67 | 50.39 |
| | 256 | 23.49 | 29.16 | 34.78 | 40.34 | 45.84 | 51.29 | 56.69 | 62.03 | 67.32 | 72.56 | 77.75 | 82.89 |
| 800 ms | 64 | 17.20 | 18.28 | 19.35 | 20.43 | 21.50 | 22.57 | 23.64 | 24.71 | 25.78 | 26.84 | 27.90 | 28.96 |
| | 128 | 18.63 | 20.79 | 22.93 | 25.07 | 27.20 | 29.32 | 31.43 | 33.53 | 35.63 | 37.72 | 39.80 | 41.87 |
| | 256 | 21.50 | 25.78 | 30.02 | 34.23 | 38.41 | 42.56 | 46.67 | 50.76 | 54.82 | 58.84 | 62.84 | 66.80 |

[1] $V_{CC}$ = 3.3 V, $T_A$ = 25°C, load = 50 pF.

**Table 3. Maximum Average Current in Low Power Mode[1]**

| Low Power Mode Delay | Decimation Rate | Current Values of Conversion Stages (μA) | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
| 200 ms | 64 | 32.62 | 38.12 | 43.58 | 48.99 | 54.35 | 59.67 | 64.95 | 70.18 | 75.37 | 80.52 | 85.63 | 90.69 |
| | 128 | 39.95 | 50.78 | 61.44 | 71.92 | 82.23 | 92.37 | 102.36 | 112.18 | 121.85 | 131.27 | 140.74 | 149.97 |
| | 256 | 54.35 | 75.37 | 95.72 | 115.42 | 134.51 | 153.02 | 170.96 | 188.38 | 205.28 | 221.70 | 237.65 | 253.15 |
| 400 ms | 64 | 28.32 | 31.10 | 33.86 | 36.61 | 39.35 | 42.08 | 44.80 | 47.50 | 50.19 | 52.88 | 55.55 | 58.21 |
| | 128 | 32.02 | 37.53 | 42.99 | 48.40 | 53.77 | 59.09 | 64.38 | 69.61 | 74.81 | 79.96 | 85.07 | 90.14 |
| | 256 | 39.35 | 50.19 | 60.86 | 71.35 | 81.67 | 91.82 | 101.82 | 111.65 | 121.33 | 130.86 | 140.24 | 149.47 |
| 600 ms | 64 | 26.88 | 28.74 | 30.59 | 32.43 | 34.27 | 36.11 | 37.94 | 39.76 | 41.58 | 43.39 | 45.20 | 47.00 |
| | 128 | 29.36 | 33.05 | 36.72 | 40.37 | 44.00 | 47.60 | 51.19 | 54.76 | 58.31 | 61.84 | 65.35 | 68.84 |
| | 256 | 34.27 | 41.58 | 48.80 | 55.95 | 63.01 | 70.00 | 76.92 | 83.76 | 90.52 | 97.21 | 103.83 | 110.39 |
| 800 ms | 64 | 26.16 | 27.56 | 28.95 | 30.33 | 31.72 | 33.10 | 34.48 | 35.85 | 37.23 | 38.60 | 39.96 | 41.33 |
| | 128 | 28.02 | 30.80 | 33.56 | 36.31 | 39.05 | 41.78 | 44.50 | 47.21 | 49.90 | 52.59 | 55.26 | 57.92 |
| | 256 | 31.72 | 37.23 | 42.69 | 48.11 | 53.48 | 58.80 | 64.09 | 69.33 | 74.53 | 79.68 | 84.80 | 89.87 |

[1] $V_{CC}$ = 3.6 V, $T_A$ = −40°C to +85°C, load = 50 pF.

## SPI TIMING SPECIFICATIONS (AD7147A)

$T_A$ = −40°C to +85°C, sample tested at 25°C to ensure compliance. $V_{DRIVE}$ = 1.65 V to 3.6 V, and $V_{CC}$ = 2.6 V to 3.6 V, unless otherwise noted. All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of $V_{CC}$) and timed from a voltage level of 1.6 V.

**Table 4. SPI Timing Specifications**

| Parameter | Limit | Unit | Description |
|---|---|---|---|
| $f_{SCLK}$ | 5 | MHz max | SCLK frequency |
| $t_1$ | 5 | ns min | $\overline{CS}$ falling edge to first SCLK falling edge |
| $t_2$ | 20 | ns min | SCLK high pulse width |
| $t_3$ | 20 | ns min | SCLK low pulse width |
| $t_4$ | 15 | ns min | SDI setup time |
| $t_5$ | 15 | ns min | SDI hold time |
| $t_6$ | 20 | ns max | SDO access time after SCLK falling edge |
| $t_7$ | 16 | ns max | $\overline{CS}$ rising edge to SDO high impedance |
| $t_8$ | 15 | ns min | SCLK rising edge to $\overline{CS}$ high |

### *SPI Timing Diagram*

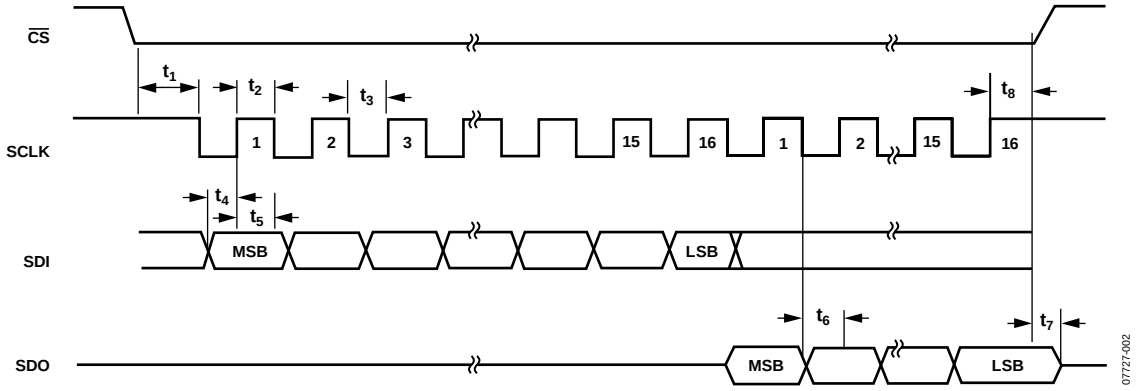



*Figure 2. SPI Detailed Timing Diagram*

## I²C TIMING SPECIFICATIONS (AD7147A-1)

$T_A$ = −40°C to +85°C, sample tested at 25°C to ensure compliance. $V_{DRIVE}$ = 1.65 V to 3.6 V, and $V_{CC}$ = 2.6 V to 3.6 V, unless otherwise noted. All input signals timed from a voltage level of 1.6 V.

**Table 5. I²C Timing Specifications**[1]

| Parameter | Limit | Unit | Description |
|---|---|---|---|
| $f_{SCLK}$ | 400 | kHz max | |
| $t_1$ | 0.6 | µs min | Start condition hold time, $t_{HD; STA}$ |
| $t_2$ | 1.3 | µs min | Clock low period, $t_{LOW}$ |
| $t_3$ | 0.6 | µs min | Clock high period, $t_{HIGH}$ |
| $t_4$ | 100 | ns min | Data setup time, $t_{SU; DAT}$ |
| $t_5$ | 300 | ns min | Data hold time, $t_{HD; DAT}$ |
| $t_6$ | 0.6 | µs min | Stop condition setup time, $t_{SU; STO}$ |
| $t_7$ | 0.6 | µs min | Start condition setup time, $t_{SU; STA}$ |
| $t_8$ | 1.3 | µs min | Bus-free time between stop and start conditions, $t_{BUF}$ |
| $t_R$ | 300 | ns max | Clock/data rise time |
| $t_F$ | 300 | ns max | Clock/data fall time |

[1] Guaranteed by design, not production tested.

### *I²C Timing Diagram*

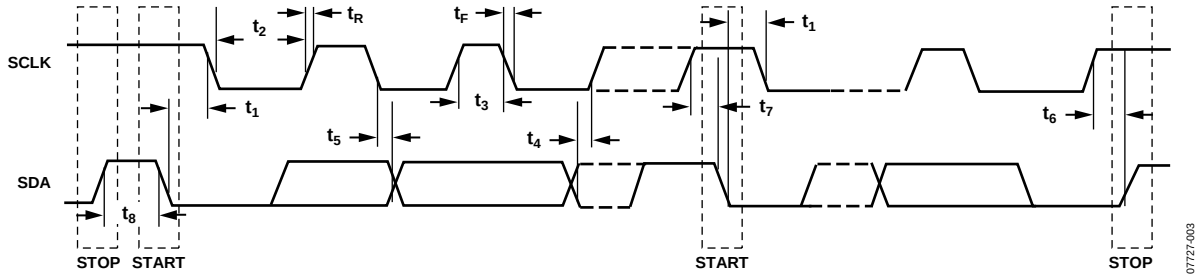



*Figure 3. I²C Detailed Timing Diagram*

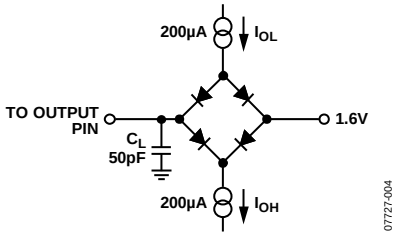



*Figure 4. Load Circuit for Digital Output Timing Specifications*

# ABSOLUTE MAXIMUM RATINGS

**Table 6.**

| Parameter | Rating |
|---|---|
| $V_{CC}$ to GND | −0.3 V to +3.6 V |
| Analog Input Voltage to GND | −0.3 V to $V_{CC}$ + 0.3 V |
| Digital Input Voltage to GND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| Digital Output Voltage to GND | −0.3 V to $V_{DRIVE}$ + 0.3 V |
| Input Current to Any Pin Except Supplies[1] | 10 mA |
| ESD Rating | |
| BIAS and $AC_{SHIELD}$ Pins (HBM Contact and Air Discharge) | 8 kV |
| All Other Pins (HBM Contact) | 2 kV |
| Operating Temperature Range | −40°C to +105°C |
| Storage Temperature Range | −65°C to +150°C |
| Junction Temperature | 150°C |
| WLCSP | |
| Power Dissipation | 1 W |
| $\theta_{JA}$ Thermal Impedance | 65°C/W |
| IR Reflow Peak Temperature | 260°C (± 0.5°C) |
| Lead Temperature (Soldering, 10 sec) | 300°C |

[1] Transient currents of up to 100 mA do not cause SCR latch-up.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

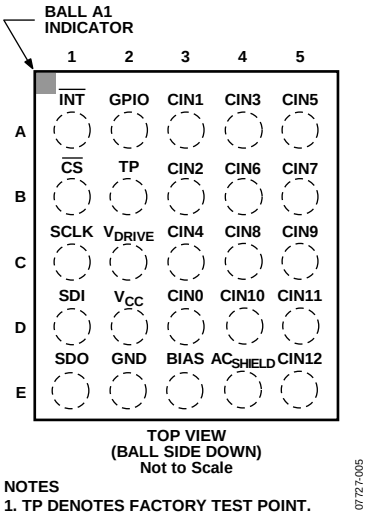



*Figure 5. AD7147A Pin Configuration*

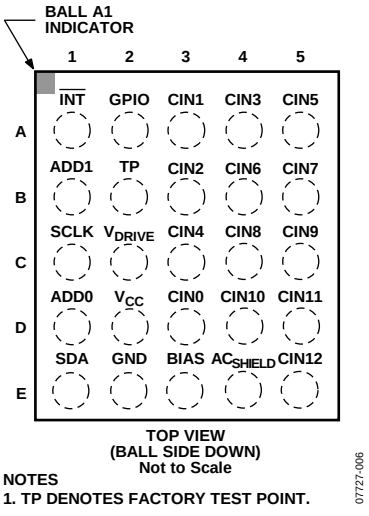



*Figure 6. AD7147A-1 Pin Configuration*

**Table 7. Pin Function Descriptions**

| Pin No. | | | |
|---|---|---|---|
| **AD7147A** | **AD7147A-1** | **Mnemonic** | **Description** |
| B4 | B4 | CIN6 | Capacitance Sensor Input. |
| B5 | B5 | CIN7 | Capacitance Sensor Input. |
| C4 | C4 | CIN8 | Capacitance Sensor Input. |
| C5 | C5 | CIN9 | Capacitance Sensor Input. |
| D4 | D4 | CIN10 | Capacitance Sensor Input. |
| D5 | D5 | CIN11 | Capacitance Sensor Input. |
| E5 | E5 | CIN12 | Capacitance Sensor Input. |
| E4 | E4 | $AC_{SHIELD}$ | CDC Active Shield Output. Connect to external shield or plane. |
| E3 | E3 | BIAS | Bias Node for Internal Circuitry. Requires 100 nF capacitor to ground. |
| E2 | E2 | GND | Ground Reference Point for All Circuitry. |
| D2 | D2 | $V_{CC}$ | Supply Voltage. |
| C2 | C2 | $V_{DRIVE}$ | Serial Interface Operating Voltage Supply. |
| E1 | N/A | SDO | SPI Serial Data Output. |
| N/A | E1 | SDA | $I^2C$ Serial Data Input/Output. SDA requires pull-up resistor. |
| D1 | N/A | SDI | SPI Serial Data Input. |
| N/A | D1 | ADD0 | $I^2C$ Address Bit 0. |
| C1 | C1 | SCLK | Clock Input for Serial Interface. |
| B1 | N/A | $\overline{CS}$ | SPI Chip Select Signal. |
| N/A | B1 | ADD1 | $I^2C$ Address Bit 1. |
| A1 | A1 | $\overline{INT}$ | General-Purpose Open-Drain Interrupt Output. Programmable polarity; requires pull-up resistor. |
| A2 | A2 | GPIO | Programmable General-Purpose Input/Output. |
| D3 | D3 | CIN0 | Capacitance Sensor Input. |
| A3 | A3 | CIN1 | Capacitance Sensor Input. |
| B3 | B3 | CIN2 | Capacitance Sensor Input. |
| A4 | A4 | CIN3 | Capacitance Sensor Input. |
| C3 | C3 | CIN4 | Capacitance Sensor Input. |
| A5 | A5 | CIN5 | Capacitance Sensor Input. |
| B2 | B2 | | Factory Test Point Only. Tie to ground. |

# TYPICAL PERFORMANCE CHARACTERISTICS

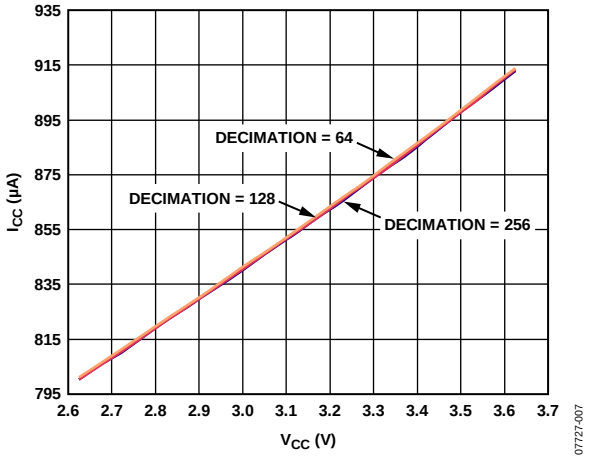



*Figure 7. Supply Current vs. Supply Voltage*

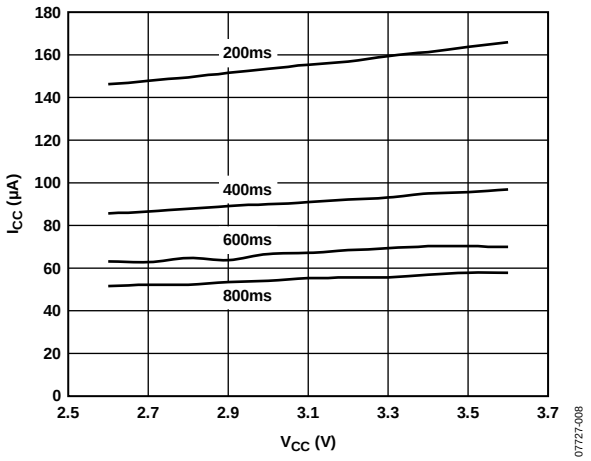



*Figure 8. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 256*

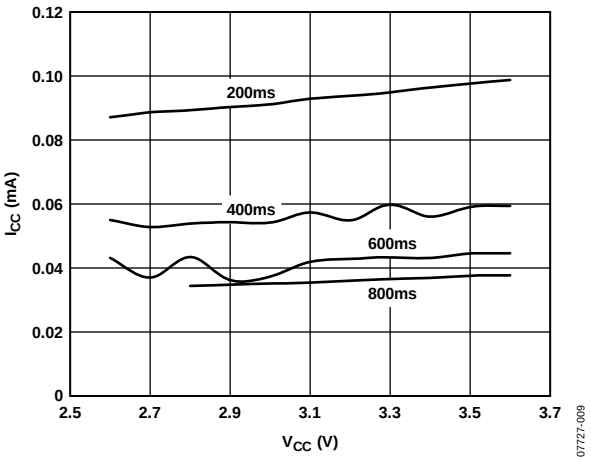



*Figure 9. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 128*

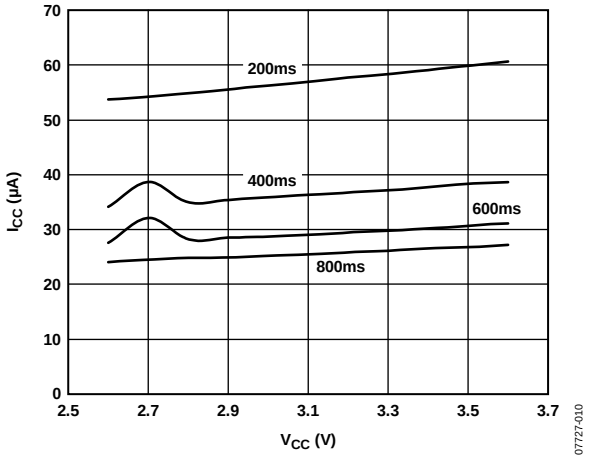



*Figure 10. Low Power Supply Current vs. Supply Voltage, Decimation Rate = 64*

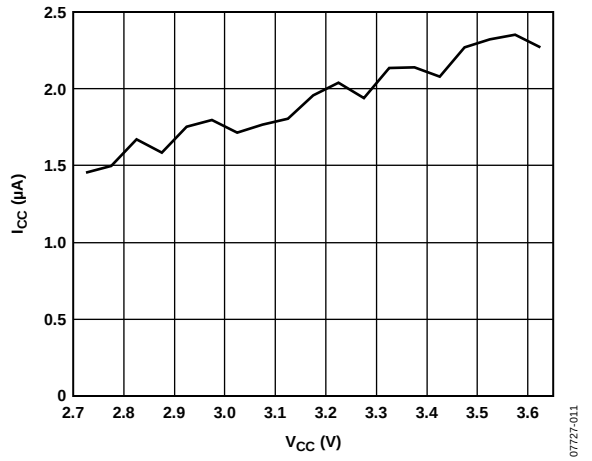



*Figure 11. Shutdown Supply Current vs. Supply Voltage*

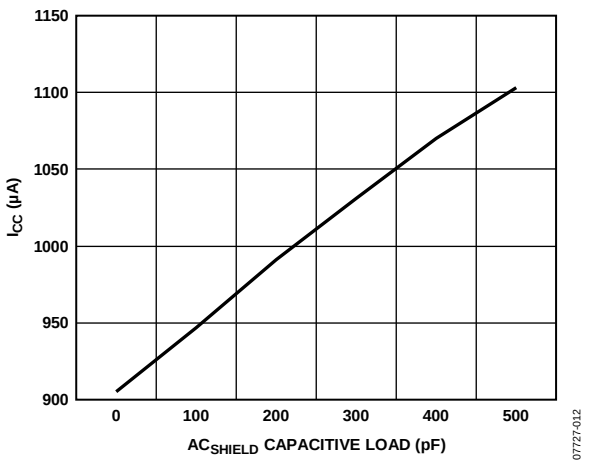



*Figure 12. Supply Current vs. Capacitive Load on $AC_{SHIELD}$*

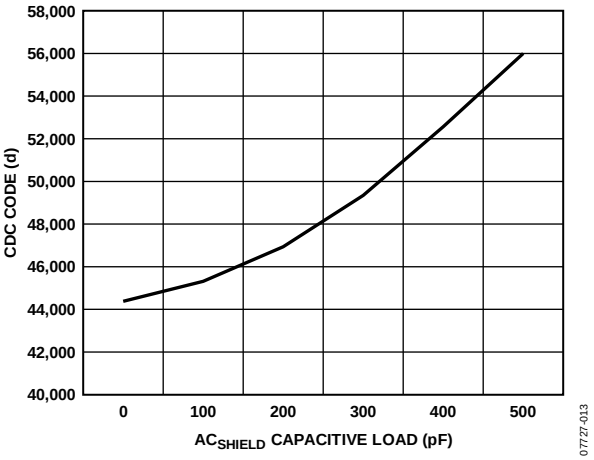



Figure 13. CDC Code vs. Capacitive Load on $AC_{SHIELD}$

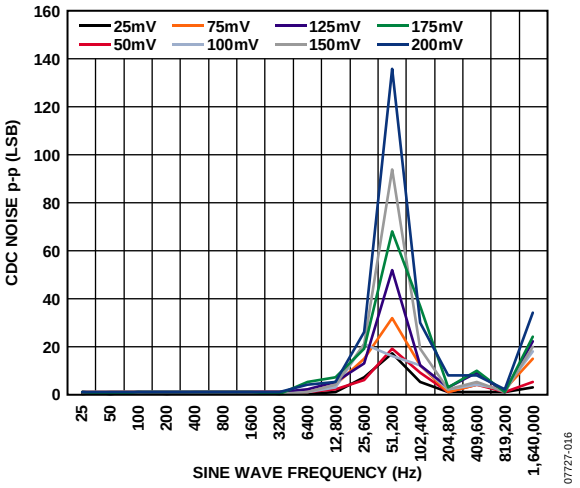



Figure 16. Power Supply Sine Wave Rejection, $V_{CC}$ = 3.6 V

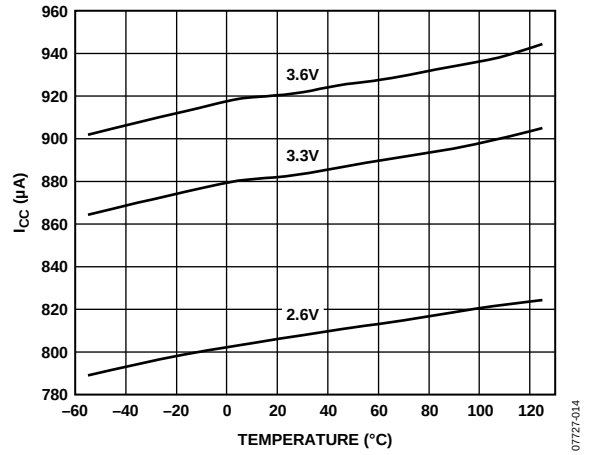



Figure 14. Supply Current vs. Temperature

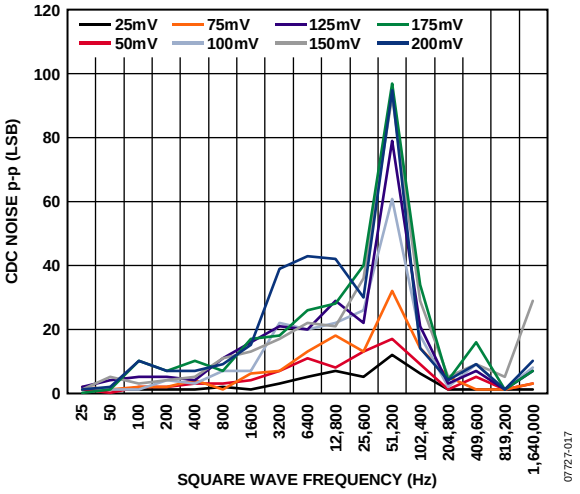



Figure 17. Power Supply Square Wave Rejection, $V_{CC}$ = 3.6 V

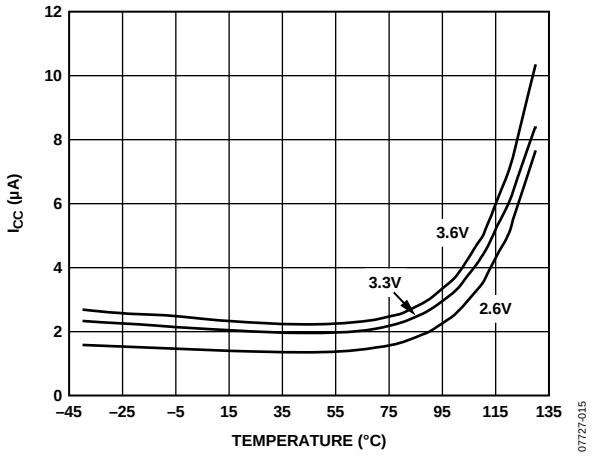



Figure 15. Shutdown Supply Current vs. Temperature

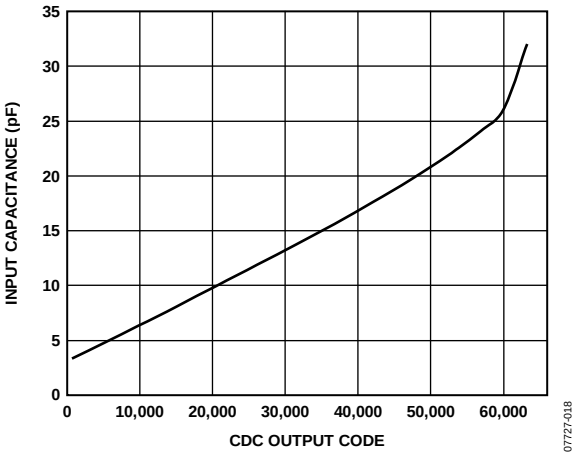



Figure 18. CDC Linearity, $V_{CC}$ = 3.3 V

# THEORY OF OPERATION

The AD7147A and AD7147A-1 are CDCs with on-chip environmental compensation. They are intended for use in portable systems requiring high resolution user input. The internal circuitry consists of a 16-bit, Σ-Δ converter that can change a capacitive input signal into a digital value. There are 13 input pins, CIN0 to CIN12. A switch matrix routes the input signals to the CDC. The result of each capacitance-to-digital conversion is stored in on-chip registers. The host subsequently reads the results over the serial interface. The AD7147A has an SPI interface, and the AD7147A-1 has an $I^2C$ interface, ensuring that the parts are compatible with a wide range of host processors. AD7147A refers to both the AD7147A and AD7147A-1, unless otherwise noted, from this point forward in this data sheet.

The AD7147A interfaces with up to 13 external capacitance sensors. These sensors can be arranged as buttons, scroll bars, or wheels, or as a combination of sensor types. The external sensors consist of an electrode on a single- or multiple-layer PCB that interfaces directly to the AD7147A.

The AD7147A can be set up to implement any set of input sensors by programming the on-chip registers. The registers can also be programmed to control features such as averaging, offsets, and gains for each of the external sensors. There is an on-chip sequencer that controls how each of the capacitance inputs is polled.

The AD7147A has on-chip digital logic and 528 words of RAM that are used for environmental compensation. The effects of humidity, temperature, and other environmental factors can affect the operation of capacitance sensors. Transparent to the user, the AD7147A performs continuous calibration to compensate for these effects, allowing the AD7147A to consistently provide error-free results.

The AD7147A requires a companion algorithm that runs on the host or another microcontroller to implement high resolution sensor functions, such as scroll bars or wheels. However, no companion algorithm is required to implement buttons. Button sensors are implemented on chip, entirely in digital logic.

The AD7147A can be programmed to operate in either full power mode or low power automatic wake-up mode. The automatic wake-up mode is particularly suited for portable devices that require low power operation to provide the user with significant power savings and full functionality.

The AD7147A has an interrupt output, $\overline{\text{INT}}$, to indicate when new data has been placed into the registers. $\overline{\text{INT}}$ is used to interrupt the host on sensor activation. The AD7147A operates from a 2.6 V to 3.6 V supply and is available in a 2.3 mm × 2.1 mm WLCSP.

## CAPACITANCE SENSING THEORY

The AD7147A measures capacitance changes from single electrode sensors. The sensor electrode on the PCB comprises one plate of a virtual capacitor. The other plate of the capacitor is the user's finger, which is grounded with respect to the sensor input.

The AD7147A first outputs an excitation signal to charge the plate of the capacitor. When the user comes close to the sensor, the virtual capacitor is formed, with the user acting as the second capacitor plate.

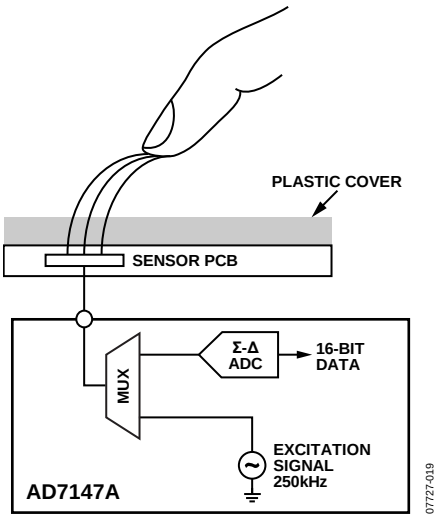



*Figure 19. Capacitance-Sensing Method*

A square wave excitation signal is applied to CINx during the conversion, and the modulator continuously samples the charge going through CINx. The output of the modulator is processed via a digital filter, and the resulting digital data is stored in the CDC_RESULT_Sx registers for each conversion stage, at Address 0x00B to Address 0x016.

### *Registering a Sensor Activation*

When a user approaches a sensor, the total capacitance associated with that sensor changes and is measured by the AD7147A. If the change causes a set threshold to be exceeded, the AD7147A interprets this as a sensor activation.

On-chip threshold limits are used to determine when a sensor activation occurs. Figure 20 shows the change in CDC_RESULT_Sx when a user activates a sensor. The sensor is deemed to be active only when the value of CDC_RESULT_Sx is either greater than the value of STAGEx_HIGH_THRESHOLD or less than the value of STAGEx_LOW_THRESHOLD.

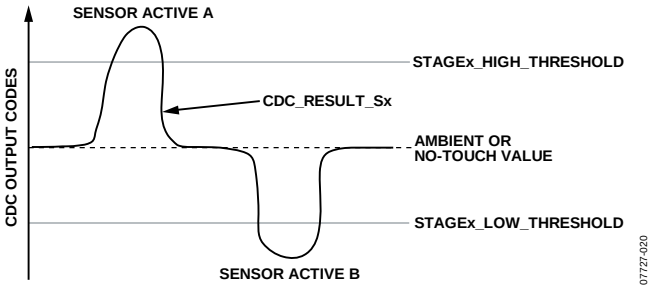



*Figure 20. Sensor Activation Thresholds*

In Figure 20, two sensor activations are shown. Sensor Active A occurs when a sensor is connected to the positive input of the converter. In this case, when a user activates the sensor, there is an increase in CDC code, and the value of CDC_RESULT_Sx exceeds that of STAGEx_HIGH_THRESHOLD. Sensor Active B occurs when the sensor is connected to the negative input of the converter. In this case, when a user activates the sensor, there is a decrease in CDC code, and the value of CDC_RESULT_Sx becomes less than the value of STAGEx_LOW_THRESHOLD.

For each conversion stage, the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD registers are in Bank 3. The values in these registers are updated automatically by the AD7147A due to its environmental calibration and adaptive threshold logic.

At power-up, the values in the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD registers are the same as those in the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW registers in Bank 2. The user must program the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW registers on device power-up. See the Environmental Calibration section of the data sheet for more information.

### *Complete Solution for Capacitance Sensing*

Analog Devices, Inc., provides a complete solution for capacitance sensing. The two main elements to the solution are the sensor PCB and the AD7147A.

If the application requires high resolution sensors such as scroll bars or wheels, software that runs on the host processor is required. The memory requirements for the host depend on the sensor and are typically 10 kB of code and 600 bytes of data memory, depending on the sensor type.

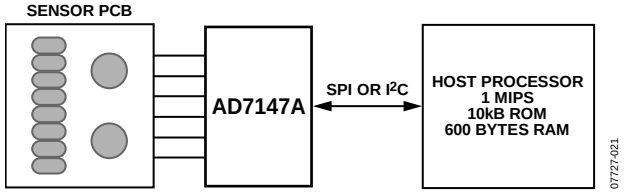



*Figure 21. Three-Part Capacitance Sensing Solution*

Analog Devices supplies the sensor PCB footprint design libraries to the customer and supplies any necessary software on an open-source basis.

## BIAS PIN

This pin is connected internally to a bias node of the AD7147A. To ensure correct operation of the AD7147A, connect a 100 nF capacitor between the BIAS pin and ground. The voltage seen at the BIAS pin is $V_{CC}/2$.

## OPERATING MODES

The AD7147A has three operating modes. Full power mode, where the device is always fully powered, is suited for applications where power is not a concern (for example, game consoles that have an ac power supply). Low power mode, where the part automatically powers down when no sensor is active, is tailored to provide significant power savings compared with full power mode and is suited for mobile applications, where power must be conserved. In shutdown mode, the part shuts down completely.

The POWER_MODE Bits[1:0] of the power control register (PWR_CONTROL, Address 0x000) set the operating mode on the AD7147A. Table 8 shows the POWER_MODE settings for each operating mode. To put the AD7147A into shutdown mode, set the POWER_MODE bits to either 01 or 11.

**Table 8. POWER_MODE Settings**

| POWER_MODE Bits | Operating Mode |
|---|---|
| 00 | Full power mode |
| 01 | Shutdown mode |
| 10 | Low power mode |
| 11 | Shutdown mode |

The power-on default setting of the POWER_MODE bits is 00, full power mode.

### Full Power Mode

In full power mode, all sections of the AD7147A remain fully powered and converting at all times. While a sensor is being touched, the AD7147A processes the sensor data. If no sensor is touched, the AD7147A measures the ambient capacitance level and uses this data for the on-chip compensation routines. In full power mode, the AD7147A converts at a constant rate. See the CDC Conversion Sequence Time section for more information.

### Low Power Mode

When AD7147A is in low power mode, the POWER_MODE bits are set to 10 upon device initialization. If the external sensors are not touched, the AD7147A reduces its conversion frequency, thereby greatly reducing its power consumption. The part remains in a reduced power state while the sensors are not touched. The AD7147A performs a conversion after a delay defined by the LP_CONV_DELAY bits, and it uses this data to update the compensation logic and check if the sensors are active. The LP_CONV_DELAY bits set the delay between conversions to 200 ms, 400 ms, 600 ms, or 800 ms.

In low power mode, the total current consumption of the AD7147A is an average of the current used during a conversion and the current used while the AD7147A is waiting for the next conversion to begin. For example, when LP_CONV_DELAY is 400 ms, the AD7147A typically uses 0.85 mA of current for 36 ms and 14 μA of current for 400 ms during the conversion interval. (Note that these conversion timings can be altered through the register settings. See the CDC Conversion Sequence Time section for more information.)

The time for the AD7147A to transition from a full power state to a reduced power state after the user stops touching the external sensors is configurable. The PWR_DOWN_TIMEOUT bits in the Ambient Compensation Control 0 register (AMB_COMP_CTRL0, Address 0x002) control the time delay before the AD7147A transitions to the reduced power state after the user stops touching the sensors.

### Low Latency from Touch to Response

In low power mode, the AD7147A remains in a low power state until proximity is detected on any one of the external sensors. When proximity is detected, the AD7147A begins a conversion sequence every 36 ms, or 18 ms, or 9 ms to read back data from the sensors. The latency between first touch and AD7147A response is greatly reduced compared to the AD7147 because the part is already in a full power state by the time the user touches the sensor.

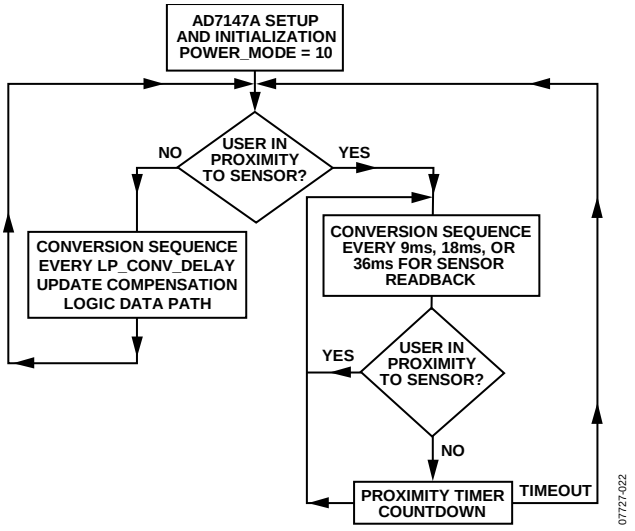



*Figure 22. Low Power Mode Operation, AD7147A*

# CAPACITANCE-TO-DIGITAL CONVERTER

The capacitance-to-digital converter on the AD7147A has a Σ-Δ architecture with 16-bit resolution. There are 13 possible inputs to the CDC that are connected to the input of the converter through a switch matrix. The sampling frequency of the CDC is 250 kHz.

## OVERSAMPLING THE CDC OUTPUT

The decimation rate, or oversampling ratio, is determined by Bits[9:8] of the power control register (PWR_CONTROL, Address 0x000), as listed in Table 9.

**Table 9. CDC Decimation Rate**

| Decimation Bits | Decimation Rate | CDC Output Rate Per Stage (ms) |
|---|---|---|
| 00 | 256 | 3.072 |
| 01 | 128 | 1.536 |
| 10 | 64 | 0.768 |
| 11 | 64 | 0.768 |

The decimation process on the AD7147A is an averaging process, where a number of samples are taken and the averaged result is output. Due to the architecture of the digital filter employed, the number of samples taken (per stage) is equal to 3× the decimation rate. So 3 × 256 or 3 × 128 samples are averaged to obtain each stage result.

The decimation process reduces the amount of noise present in the final CDC result. However, the higher the decimation rate, the lower the output rate per stage; therefore, there is a trade-off possible between the amount of noise in the signal and the speed of sampling.

## CAPACITANCE SENSOR OFFSET CONTROL

There are two programmable DACs on board the AD7147A to null the effect of any stray capacitances on the CDC measurement. These offsets are due to stray capacitance to ground.

A simplified block diagram in Figure 23 shows how to apply the STAGEx_AFE_OFFSET registers to null the offsets. The POS_AFE_OFFSET and NEG_AFE_OFFSET bits (Bits[13:8] and Bits[5:0], respectively) program the offset DACs to provide 0.32 pF resolution offset adjustment over a range of 20 pF.

The best practice is to ensure that the CDC output for any stage is approximately equal to midscale (~32,700) when all sensors are inactive. To correctly offset the stray capacitance to ground for each stage, use the following procedure:

1. Read back the CDC value from the CDC_RESULT_Sx register.
2. If this value is not close to midscale, increase the value of POS_AFE_OFFSET or NEG_AFE_OFFSET (depending on if the CINx input is connected to the positive or negative input of the converter) by 1. The CINx connections are determined by the STAGEx_CONNECTION registers.
3. If the CDC value in CDC_RESULT_Sx is now closer to midscale, repeat Step 2. If the CDC value is further from midscale, decrease the POS_AFE_OFFSET or NEG_AFE_OFFSET value by 1.

The goal is to ensure that the CDC_RESULT_Sx is as close to midscale as possible. This process is required only once during the initial capacitance sensor characterization.

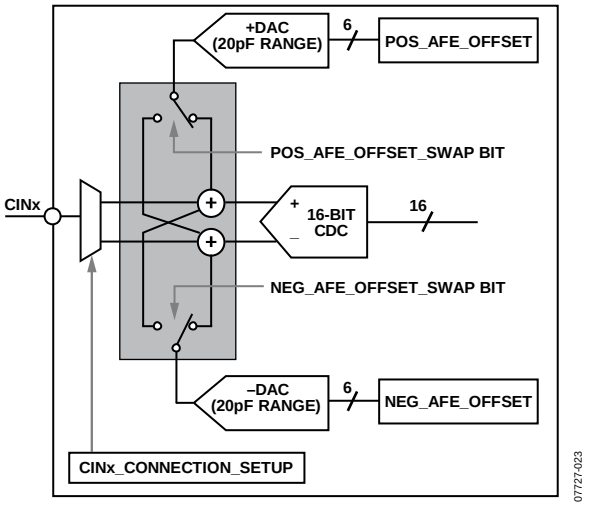



*Figure 23. Analog Front-End Offset Control*

## CONVERSION SEQUENCER

The AD7147A has an on-chip sequencer to implement conversion control for the input channels. Up to 12 conversion stages can be performed in one sequence. Each of the 12 conversions stages can measure the input from a different sensor. By using the Bank 2 registers, each stage can be uniquely configured to support multiple capacitance sensor interface requirements. For example, a slider sensor can be assigned to STAGE1 through STAGE8, with a button sensor assigned to STAGE0. For each conversion stage, the input mux that connects the CINx inputs to the converter can have a unique setting.

The AD7147A on-chip sequence controller provides conversion control, beginning with STAGE0. Figure 24 shows a block diagram of the CDC conversion stages and CINx inputs. A conversion sequence is defined as a sequence of CDC conversions starting at STAGE0 and ending at the stage determined by the value programmed in the SEQUENCE_STAGE_NUM bits (Bits[7:4], Address 0x00). Depending on the number and type of capacitance sensors that are used, not all conversion stages are required. Use the SEQUENCE_STAGE_NUM bits to set the number of conversions in one sequence. This number depends on the sensor interface requirements. For example, the register should be set to 5 if the CINx inputs are mapped to only six conversion stages. In addition, the STAGE_CAL_EN register (Address 0x001) should be set according to the number of stages that are used.

The number of required conversion stages depends solely on the number of sensors attached to the AD7147A. Figure 25 shows how many conversion stages are required for each sensor and how many inputs to the AD7147A each sensor requires.

A button sensor generally requires one sequencer stage; this is shown in Figure 25 as B1. However, it is possible to configure two button sensors to operate differentially for one conversion stage. Only one button can be activated at a time; pressing both buttons simultaneously results in neither button being activated. The configuration with two button sensors operating differentially requires one conversion stage and is shown in Figure 25, with B2 and B3 representing the differentially configured button sensors.

A wheel sensor requires eight stages, whereas a slider requires two stages. The result from each stage is used by the host software to determine the user's position on the slider or wheel. The algorithms that perform this process are available from Analog Devices and are free of charge but require signing a software license.

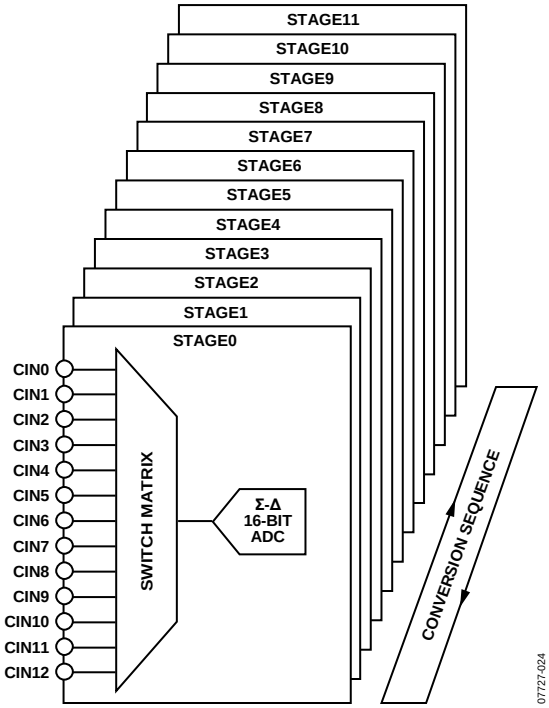



*Figure 24. CDC Conversion Stages*

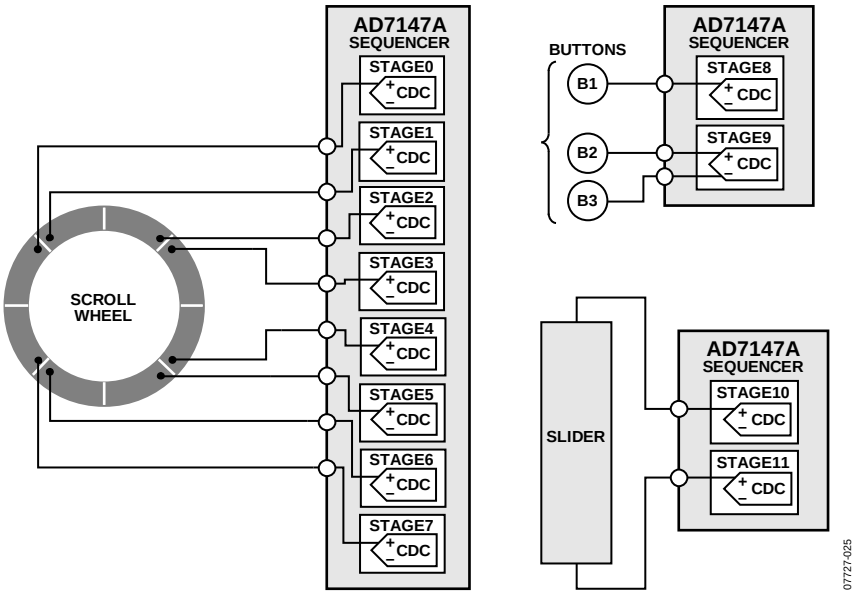



*Figure 25. Sequencer Setup for Sensors*

## CDC CONVERSION SEQUENCE TIME

**Table 10. CDC Conversion Times for Full Power Mode**

| | Conversion Time (ms) | | |
|---|---|---|---|
| **SEQUENCE_STAGE_NUM** | **Decimation = 64** | **Decimation = 128** | **Decimation = 256** |
| 0 | 0.768 | 1.536 | 3.072 |
| 1 | 1.536 | 3.072 | 6.144 |
| 2 | 2.304 | 4.608 | 9.216 |
| 3 | 3.072 | 6.144 | 12.288 |
| 4 | 3.84 | 7.68 | 15.36 |
| 5 | 4.608 | 9.216 | 18.432 |
| 6 | 5.376 | 10.752 | 21.504 |
| 7 | 6.144 | 12.288 | 24.576 |
| 8 | 6.912 | 13.824 | 27.648 |
| 9 | 7.68 | 15.36 | 30.72 |
| 10 | 8.448 | 16.896 | 33.792 |
| 11 | 9.216 | 18.432 | 36.864 |

The time required for the CDC to complete the measurement of all 12 stages is defined as the CDC conversion sequence time. The SEQUENCE_STAGE_NUM and DECIMATION bits determine the conversion time, as listed in Table 10.

For example, if the device is operated with a decimation rate of 128 and the SEQUENCE_STAGE_NUM bit is set to 5 for the conversion of six stages in a sequence, the conversion sequence time is 9.216 ms.

### *Full Power Mode CDC Conversion Sequence Time*

The full power mode CDC conversion sequence time for all 12 stages is set by configuring the SEQUENCE_STAGE_NUM and DECIMATION bits as outlined in Table 10.

Figure 26 shows a simplified timing diagram of the full power mode CDC conversion time. The full power mode CDC conversion time ($t_{CONV\_FP}$) is set using the values shown in Table 10.

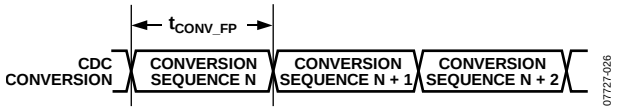



*Figure 26. Full Power Mode CDC Conversion Sequence Time*

### *Low Power Mode CDC Conversion Sequence Time with Delay*

The frequency of each CDC conversion while operating in the low power automatic wake-up mode is controlled by using the LP_CONV_DELAY Bits[3:2] located at Address 0x000 in addition to the registers listed in Table 10. This feature provides some flexibility for optimizing the trade-off between the conversion time needed to meet system requirements and the power consumption of the AD7147A.

For example, maximum power savings is achieved when the LP_CONV_DELAY bits are set to 11. With a setting of 11, the AD7147A automatically wakes up, performing a conversion every 800 ms.

**Table 11. LP_CONV_DELAY Settings**

| LP_CONV_DELAY Bits | Delay Between Conversions (ms) |
|---|---|
| 00 | 200 |
| 01 | 400 |
| 10 | 600 |
| 11 | 800 |

Figure 27 shows a simplified timing example of the low power mode CDC conversion time. As shown, the low power mode CDC conversion time is set by $t_{CONV\_FP}$ and the LP_CONV_DELAY bits.

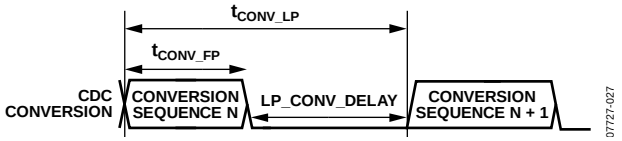



*Figure 27. Low Power Mode CDC Conversion Sequence Time*

## CDC CONVERSION RESULTS

Certain high resolution sensors require the host to read back the CDC conversion results for processing. The registers required for host processing are located in Bank 3. The host processes the data read back from these registers using a software algorithm to determine position information.

In addition to the results registers in Bank 3, the AD7147A provides the 16-bit CDC output data directly, starting at Address 0x00B of Bank 1. Reading back the CDC 16-bit conversion data register allows for customer-specific application data processing.

# CAPACITANCE SENSOR INPUT CONFIGURATION

Each input connection from the external capacitance sensors to the converter of the AD7147A can be uniquely configured by using the stage configuration registers in Bank 2 (see Table 39). These registers are used to configure the input pin connection setups, sensor offsets, sensor sensitivities, and sensor limits for each stage. Each sensor can be individually optimized. For example, a button sensor connected to STAGE0 can have different sensitivity and offset values than a button with another function that is connected to a different stage.

## CINx INPUT MULTIPLEXER SETUP

Table 35 and Table 36 list the available options for the CINx_CONNECTION_SETUP bits when the sensor input pins are connected to the CDC.

The AD7147A has an on-chip multiplexer that routes the input signals from each CINx pin to the input of the converter. Each input pin can be tied to either the negative or positive input of the CDC, or it can be left floating. Each input can also be internally connected to the BIAS signal to help prevent cross-coupling. If an input is not used, always connect it to BIAS.

Connecting a CINx input pin to the positive CDC input results in an increase in CDC output code when the corresponding sensor is activated. Connecting a CINx input pin to the negative CDC input results in a decrease in CDC output code when the corresponding sensor is activated.

The AD7147A performs a sequence of 12 conversions. The multiplexer can have different settings for each of the 12 conversions. For example, CIN0 is connected to the negative CDC input for conversion STAGE1, left floating for conversion STAGE1, and so on, for all 12 conversion stages.

For each CINx input for each conversion stage, two bits control how the input is connected to the converter, as shown in Figure 28.

### *Examples*

To connect CIN3 to the positive CDC input on Stage 0, use the following setting:

STAGE0_CONNECTION[6:0] = 0xFFBF
STAGE0_CONNECTION[12:7] = 0x2FFF

To connect CIN0 to the positive CDC input and CIN12 to the negative CIN input on STAGE5, use the following settings:

STAGE5_CONNECTION[6:0] = 0xFFFE
STAGE5_CONNECTION[12:7] = 0x37FF

## SINGLE-ENDED CONNECTIONS TO THE CDC

A single-ended connection to the CDC is defined as one CINx input connected to either the positive or negative CDC input for one conversion stage. A differential connection to the CDC is defined as one CINx input connected to the positive CDC input and a second CINx input connected to the negative input of the CDC for one conversion stage.

For any stage, if a single-ended connection to the CDC is made in that stage, the SE_CONNECTION_SETUP Bits[13:12] in the STAGEx_CONNECTION[12:7] register should be applied as described in Table 12.

**Table 12. SE_CONNECTION_SETUP Bits**

| SE_CONNECTION_SETUP | Description |
|---|---|
| 00 | Do not use. |
| 01 | Single-ended connection. For this stage, there is one CINx connected to the positive CDC input. |
| 10 | Single-ended connection. For this stage, there is one CINx connected to the negative CDC input. |
| 11 | Differential connection. For this stage, there is one CINx connected to the negative CDC input and one CINx connected to the positive CDC input. |

The SE_CONNECTION_SETUP Bits[13:12] ensure that during a single-ended connection to the CDC, the input paths to both CDC terminals are matched, which, in turn, improves the power-supply rejection of the converter measurement.

These bits should be applied in addition to setting the other bits in the STAGEx_CONNECTION registers, as outlined in the CINX Input Multiplexer Setup section.

If more than one CINx input is connected to either the positive or negative input of the converter for the same conversion, set SE_CONNECTION_SETUP to 11. For example, if CIN0 and CIN3 are connected to the positive input of the CDC, set SE_CONNECTION_SETUP to 11.

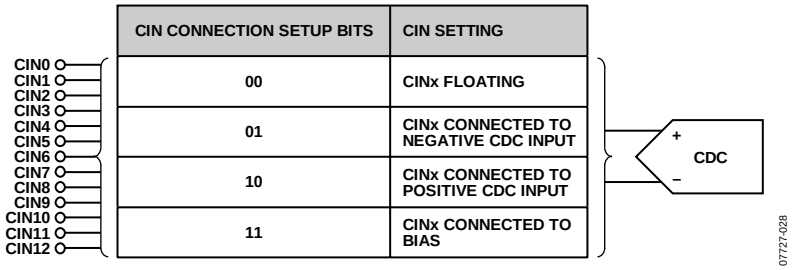



*Figure 28. Input Mux Configuration Options*

# NONCONTACT PROXIMITY DETECTION

The AD7147A internal signal processing continuously monitors all capacitance sensors for noncontact proximity detection. This feature provides the ability to detect when a user is approaching a sensor, at which time all internal calibration is immediately disabled while the AD7147 is automatically configured to detect a valid contact.

The proximity control register bits are described in Table 13. The FP_PROXIMITY_CNT and LP_PROXIMITY_CNT register bits control the length of the calibration disable period after the user stops touching the sensor and is not in close proximity to the sensor during full or low power mode. The calibration is disabled during this period and then enabled again. Figure 29 and Figure 30 show examples of how these register bits are used to set the calibration disable periods for the full and low power modes.

The calibration disable period in full power mode is the value of the FP_PROXIMITY_CNT multiplied by 16 multiplied by the time for one conversion sequence in full power mode. The calibration disable period in low power mode is the value of the LP_PROXIMITY_CNT multiplied by 4 multiplied by the time for one conversion sequence in low power mode.

## RECALIBRATION

In certain situations, for example, when a user hovers over a sensor for a long time, the proximity flag can be set for a long period. The environmental calibration on the AD7147A is suspended while proximity is detected, but changes may occur to the ambient capacitance level during the proximity event. This means that the ambient value stored on the AD7147A no longer represents the actual ambient value. In this case, even when the user is not in close proximity to the sensor, the proximity flag may still be set. This situation can occur if the user interaction creates some moisture on the sensor, causing the new sensor ambient value to be different from the expected value. In this situation, the AD7147A automatically forces a recalibration internally. This ensures that the ambient values are recalibrated, regardless of how long the user hovers over the sensor. A recalibration ensures maximum AD7147A sensor performance.

The AD7147A recalibrates automatically when the measured CDC value exceeds the stored ambient value by an amount determined by the PROXIMITY_RECAL_LVL bits for a set period of time known as the recalibration timeout. In full power mode, the recalibration timeout is controlled by FP_PROXIMITY_RECAL; in low power mode, by LP_PROXMTY_RECAL.

The recalibration timeout in full power mode is the value of FP_PROXIMITY_RECAL multiplied by the time for one conversion sequence in full power mode. The recalibration timeout in low power mode is the value of LP_PROXIMITY_RECAL multiplied by the time for one conversion sequence in low power mode.

Figure 31 and Figure 32 show examples of how the FP_PROXIMITY_RECAL and LP_PROXIMITY_RECAL register bits control the timeout period before a recalibration while operating in the full and low power modes. In these examples, a user approaches a sensor and then leaves, but the proximity detection remains active. The measured CDC value exceeds the stored ambient value by the amount set in the PROXIMITY_RECAL_LVL bits for the entire timeout period. The sensor is automatically recalibrated at the end of the timeout period.

## PROXIMITY SENSITIVITY

The fast filter in Figure 33 is used to detect when someone is close to the sensor (proximity). Two conditions, detected by Comparator 1 and Comparator 2, set the internal proximity detection signal: Comparator 1 detects when a user is approaching or leaving a sensor, and Comparator 2 detects when a user hovers over a sensor or approaches a sensor very slowly.

The sensitivity of Comparator 1 is controlled by the PROXIMITY_DETECTION_RATE bits (Address 0x003). For example, if PROXIMITY_DETECTION_RATE is set to 4, the Proximity 1 signal is set when the absolute difference between WORD1 and WORD3 exceeds (4 × 16) LSB codes.

The PROXIMITY_RECAL_LVL bits (Address 0x003) control the sensitivity of Comparator 2. For example, if PROXIMITY_RECAL_LVL is set to 75, the Proximity 2 signal is set when the absolute difference between the fast filter average value and the ambient value exceeds (75 × 16) LSB codes.

**Table 13. Proximity Control Registers (See Figure 33)**

| Bit Name | Length (Bits) | Register Address | Description |
|---|---|---|---|
| FP_PROXIMITY_CNT | 4 | 0x002[7:4] | Calibration disable time in full power mode. |
| LP_PROXIMITY_CNT | 4 | 0x002[11:8] | Calibration disable time in low power mode. |
| FP_PROXIMITY_RECAL | 10 | 0x004[9:0] | Full power mode proximity recalibration time control. |
| LP_PROXIMITY_RECAL | 6 | 0x004[15:10] | Low power mode proximity recalibration time control. |
| PROXIMITY_RECAL_LVL | 8 | 0x003[7:0] | Proximity recalibration level. This value, multiplied by 16, controls the sensitivity of Comparator 2 (see Figure 33). |
| PROXIMITY_DETECTION_RATE | 6 | 0x003[13:8] | Proximity detection rate. This value, multiplied by 16, controls the sensitivity of Comparator 1 (see Figure 33). |

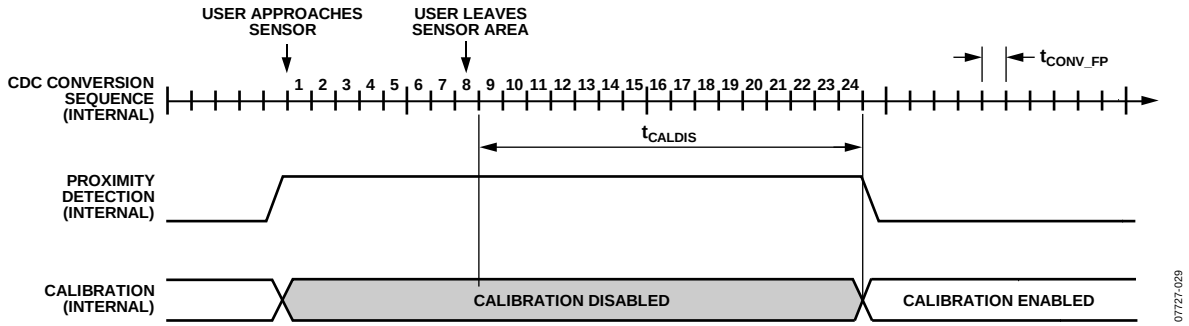



*Figure 29. Example of Full Power Mode Proximity Detection (FP_PROXIMITY_CNT = 1)*

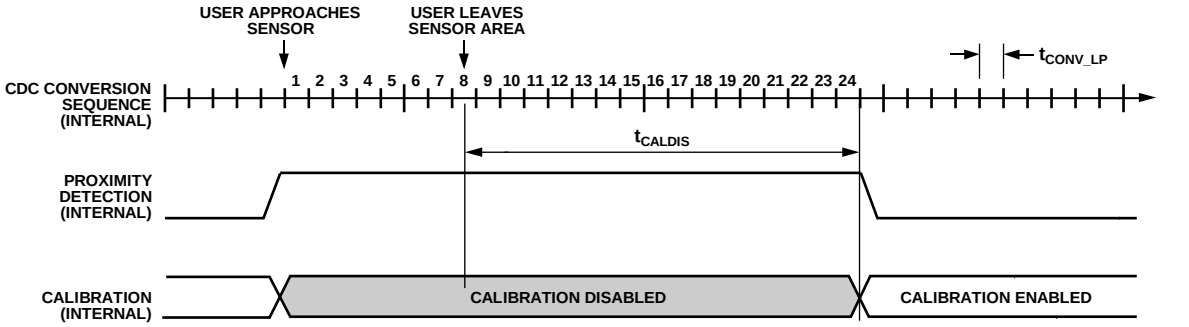



*Figure 30. Example of Low Power Mode Proximity Detection (LP_PROXIMITY_CNT = 4)*

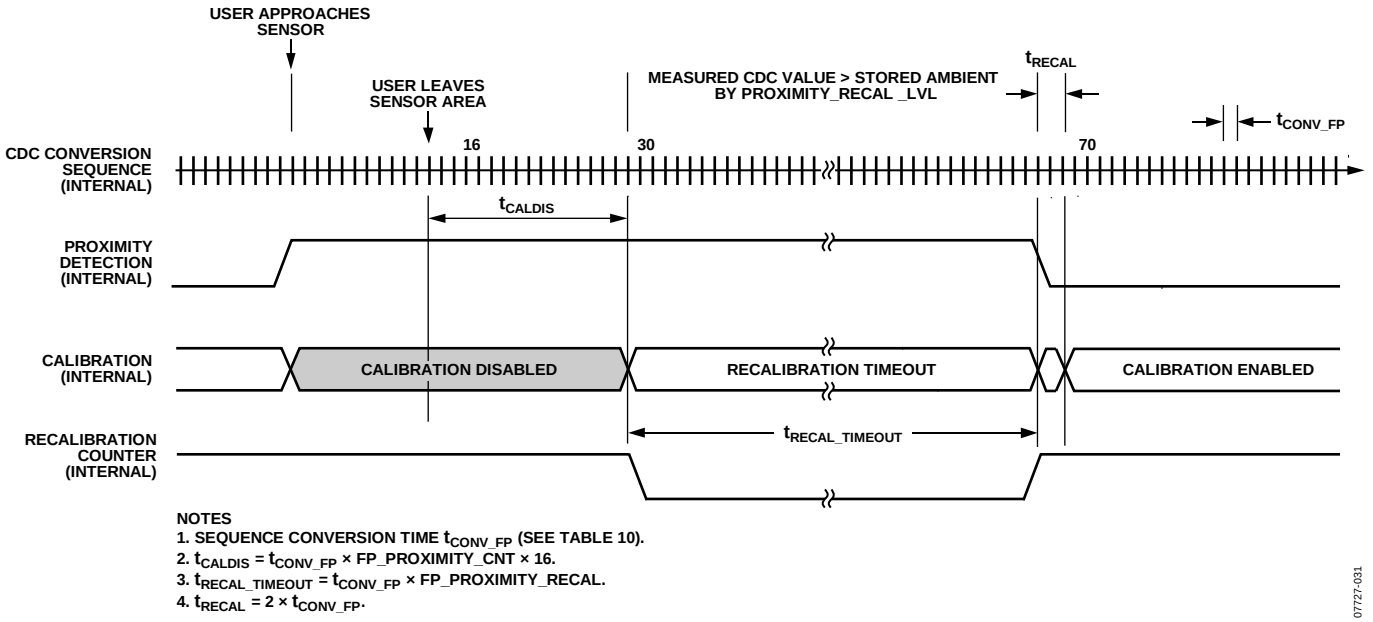



*Figure 31. Example of Full Power Mode Proximity Detection with Forced Recalibration (FP_PROXIMITY_CNT = 1 and FP_PROXIMITY_RECAL = 40)*

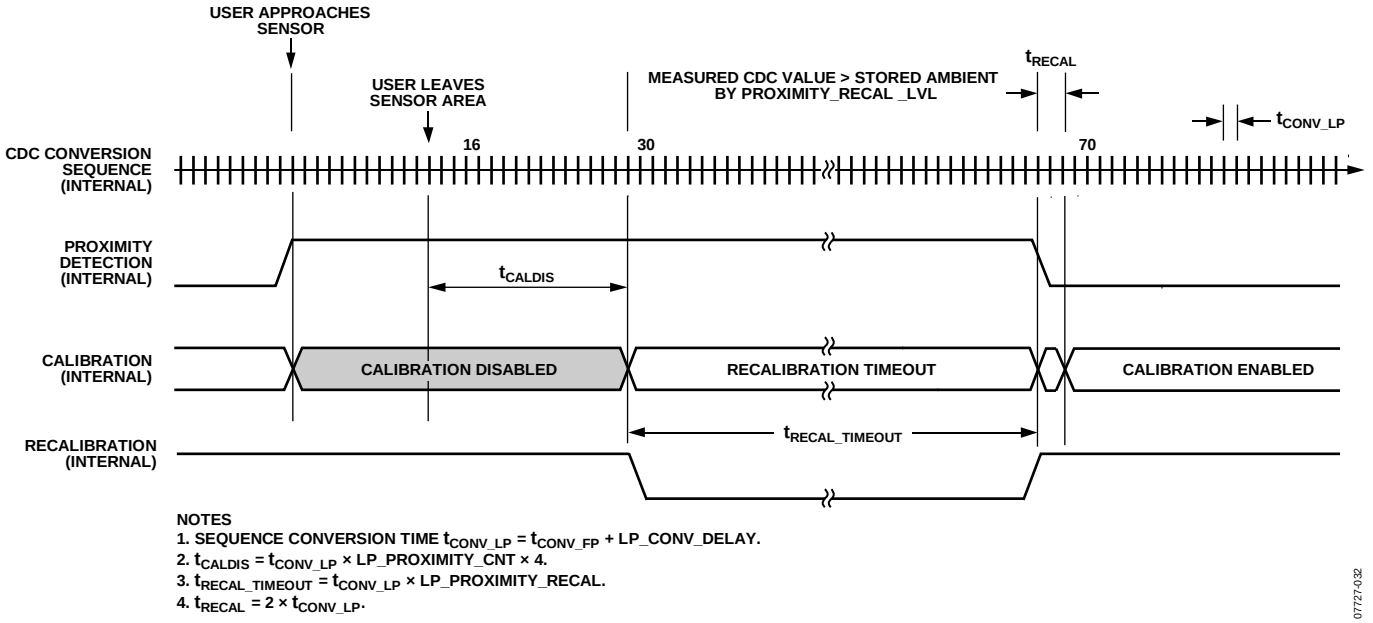



*Figure 32. Example of Low Power Mode Proximity Detection with Forced Recalibration (LP_PROXIMITY_CNT = 4 and LP_PROXIMITY_RECAL = 40)*

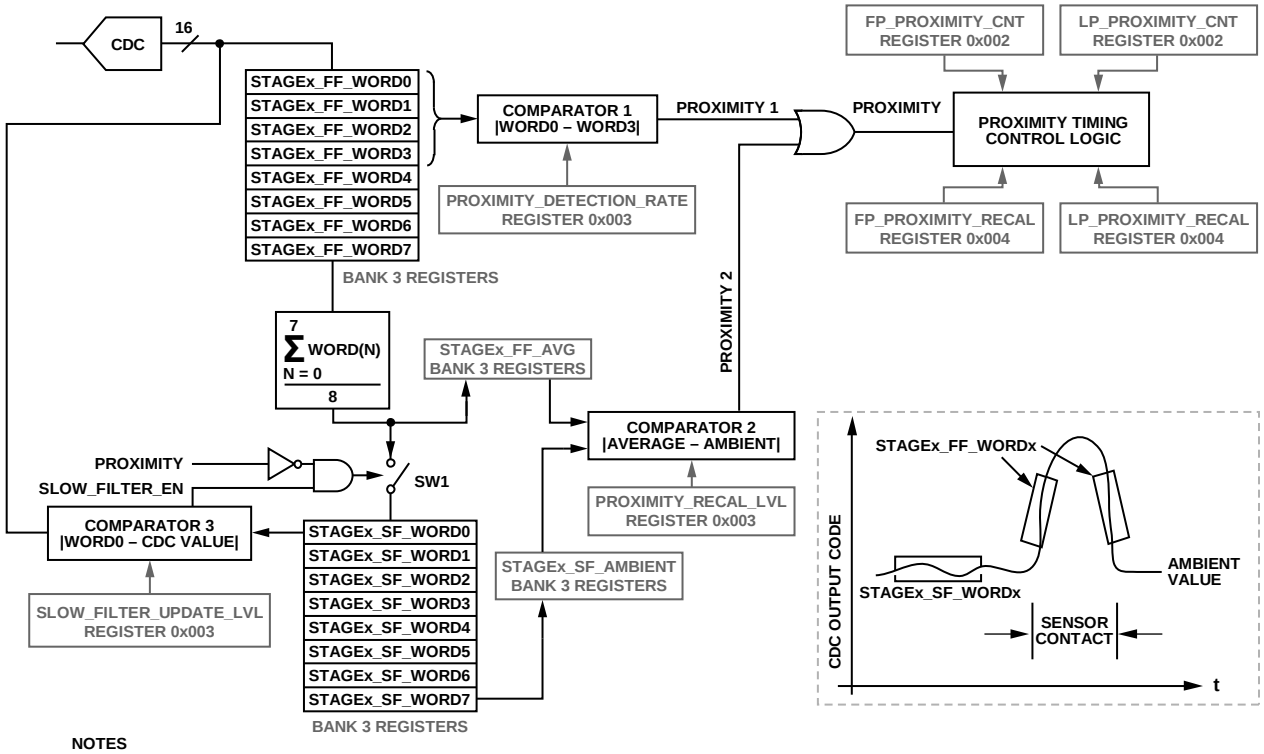
## FF_SKIP_CNT

The proximity detection fast FIFO is used by the on-chip logic to determine if proximity is detected. The fast FIFO expects to receive samples from the converter at a set rate. The fast filter skip control, FF_SKIP_CNT (Bits[3:0], Address 0x002), is used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence. This value determines which CDC samples are not used (skipped) by the proximity detection fast FIFO.

Determining the FF_SKIP_CNT value is required only once during the initial setup of the capacitance sensor interface. Table 13 shows how FF_SKIP_CNT controls the update rate of the fast FIFO. The recommended value for the setting when using all 12 conversion stages on the AD7147A is 0000, or no samples skipped.

**Table 14. FF_SKIP_CNT Settings**

| FF_SKIP_CNT | FAST FIFO Update Rate | | |
|---|---|---|---|
| | **Decimation = 64** | **Decimation = 128** | **Decimation = 256** |
| 0 | 0.768 × (SEQUENCE_STAGE_NUM + 1) ms | 1.536 × (SEQUENCE_STAGE_NUM + 1) ms | 3.072 × (SEQUENCE_STAGE_NUM + 1) ms |
| 1 | 1.536 × (SEQUENCE_STAGE_NUM + 1) ms | 3.072 × (SEQUENCE_STAGE_NUM + 1) ms | 6.144 × (SEQUENCE_STAGE_NUM + 1) ms |
| 2 | 2.304 × (SEQUENCE_STAGE_NUM + 1) ms | 4.608 × (SEQUENCE_STAGE_NUM + 1) ms | 9.216 × (SEQUENCE_STAGE_NUM + 1) ms |
| 3 | 3.072 × (SEQUENCE_STAGE_NUM + 1) ms | 6.144 × (SEQUENCE_STAGE_NUM + 1) ms | 12.288 × (SEQUENCE_STAGE_NUM + 1) ms |
| 4 | 3.84 × (SEQUENCE_STAGE_NUM + 1) ms | 7.68 × (SEQUENCE_STAGE_NUM + 1) ms | 15.36 × (SEQUENCE_STAGE_NUM + 1) ms |
| 5 | 4.608 × (SEQUENCE_STAGE_NUM + 1) ms | 9.216 × (SEQUENCE_STAGE_NUM + 1) ms | 18.432 × (SEQUENCE_STAGE_NUM + 1) ms |
| 6 | 5.376 × (SEQUENCE_STAGE_NUM + 1) ms | 10.752 × (SEQUENCE_STAGE_NUM + 1) ms | 21.504 × (SEQUENCE_STAGE_NUM + 1) ms |
| 7 | 6.144 × (SEQUENCE_STAGE_NUM + 1) ms | 12.288 × (SEQUENCE_STAGE_NUM + 1) ms | 24.576 × (SEQUENCE_STAGE_NUM + 1) ms |
| 8 | 6.912 × (SEQUENCE_STAGE_NUM + 1) ms | 13.824 × (SEQUENCE_STAGE_NUM + 1) ms | 27.648 × (SEQUENCE_STAGE_NUM + 1) ms |
| 9 | 7.68 × (SEQUENCE_STAGE_NUM + 1) ms | 15.36 × (SEQUENCE_STAGE_NUM + 1) ms | 30.72 × (SEQUENCE_STAGE_NUM + 1) ms |
| 10 | 8.448 × (SEQUENCE_STAGE_NUM + 1) ms | 16.896 × (SEQUENCE_STAGE_NUM + 1) ms | 33.792 × (SEQUENCE_STAGE_NUM + 1) ms |
| 11 | 9.216 × (SEQUENCE_STAGE_NUM + 1) ms | 18.432 × (SEQUENCE_STAGE_NUM + 1) ms | 36.864 × (SEQUENCE_STAGE_NUM + 1) ms |
| 12 | 9.984 × (SEQUENCE_STAGE_NUM + 1) ms | 19.968 × (SEQUENCE_STAGE_NUM + 1) ms | 39.936 × (SEQUENCE_STAGE_NUM + 1) ms |
| 13 | 10.752 × (SEQUENCE_STAGE_NUM + 1) ms | 21.504 × (SEQUENCE_STAGE_NUM + 1) ms | 43.008 × (SEQUENCE_STAGE_NUM + 1) ms |
| 14 | 11.52 × (SEQUENCE_STAGE_NUM + 1) ms | 23.04 × (SEQUENCE_STAGE_NUM + 1) ms | 46.08 × (SEQUENCE_STAGE_NUM + 1) ms |
| 15 | 12.288 × (SEQUENCE_STAGE_NUM + 1) ms | 24.576 × (SEQUENCE_STAGE_NUM + 1) ms | 49.152 × (SEQUENCE_STAGE_NUM + 1) ms |




**NOTES**

1. SLOW_FILTER_EN, WHICH IS THE NAME OF THE OUTPUT OF COMPARATOR 3, IS SET AND SW1 IS CLOSED WHEN |STAGEx_SF_WORD0 – CDC VALUE| EXCEEDS THE VALUE PROGRAMMED IN THE SLOW_FILTER_UPDATE_LVL REGISTER PROVIDING PROXIMITY IS NOT SET.
2. PROXIMITY 1 IS SET WHEN |STAGEx_FF_WORD0 – STAGEx_FF_WORD3| EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_DETECTION_RATE REGISTER.
3. PROXIMITY 2 IS SET WHEN |AVERAGE – AMBIENT| EXCEEDS THE VALUE PROGRAMMED IN THE PROXIMITY_RECAL_LVL REGISTER.
4. DESCRIPTION OF COMPARATOR FUNCTIONS:
   COMPARATOR 1: USED TO DETECT WHEN A USER IS APPROACHING OR LEAVING A SENSOR.
   COMPARATOR 2: USED TO DETECT WHEN A USER IS HOVERING OVER A SENSOR OR APPROACHING A SENSOR VERY SLOWLY. ALSO USED TO DETECT IF THE SENSOR AMBIENT LEVEL HAS CHANGED AS A RESULT OF THE USER INTERACTION. FOR EXAMPLE, HUMIDITY OR DIRT LEFT BEHIND ON SENSOR.
   COMPARATOR 3: USED TO ENABLE THE SLOW FILTER UPDATE RATE. THE SLOW FILTER IS UPDATED WHEN SLOW_FILTER_EN IS SET AND PROXIMITY IS NOT SET.

*Figure 33. Proximity-Detection Logic*

# ENVIRONMENTAL CALIBRATION

The AD7147A provides on-chip capacitance sensor calibration to automatically adjust for environmental conditions that have an effect on the ambient levels of the capacitance sensor. The output levels of the capacitance sensor are sensitive to temperature, humidity, and, in some cases, dirt.

The AD7147A achieves optimal and reliable sensor performance by continuously monitoring the CDC ambient levels and compensating for any environmental changes by adjusting the values of the STAGEx_HIGH_THRESHOLD registers and the STAGEx_LOW_THRESHOLD registers as described in the Threshold Equations section. The CDC ambient level is defined as the output level of the capacitance sensor during periods when the user is not approaching or in contact with the sensor.

After the AD7147A is configured, the compensation logic runs automatically with each conversion when the AD7147A is not being touched. This allows the AD7147A to compensate for rapidly changing environmental conditions.

The ambient compensation control registers provide the host with access to general setup and controls for the compensation algorithm. On-chip RAM stores the compensation data for each conversion stage, as well as setup information specific for each stage.

Figure 34 shows an example of the ideal behavior of a capacitance sensor, where the CDC ambient level remains constant regardless of the environmental conditions. The CDC output shown is for a pair of differential button sensors, where one sensor caused an increase and the other caused a decrease in measured capacitance when activated. The positive and negative sensor threshold levels are calculated as a percentage of the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values, and are based on the threshold sensitivity settings and the ambient value. These values are sufficient to detect a sensor contact and result in the AD7147A asserting the $\overline{\text{INT}}$ output when the threshold levels are exceeded.

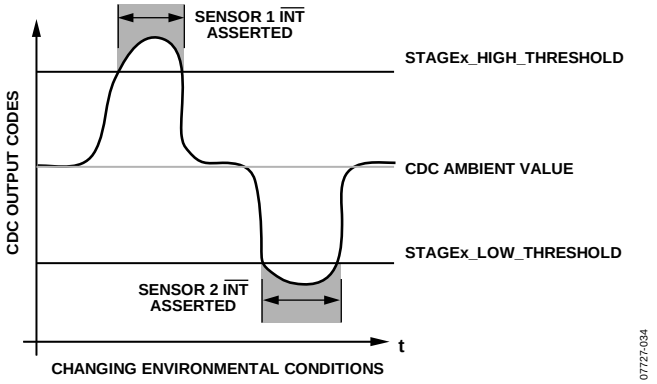



*Figure 34. Ideal Sensor Behavior with a Constant Ambient Level*

## CAPACITANCE SENSOR BEHAVIOR WITHOUT CALIBRATION

Figure 35 shows the typical behavior of a capacitance sensor when calibration is not applied and the ambient levels drifting over time as environmental conditions change. As a result of the initial threshold levels remaining constant while the ambient levels drift upward, Sensor 2 fails to detect a user contact in this example.

The Capacitance Sensor Behavior with Calibration section describes how the AD7147A adaptive calibration algorithm prevents such errors from occurring.

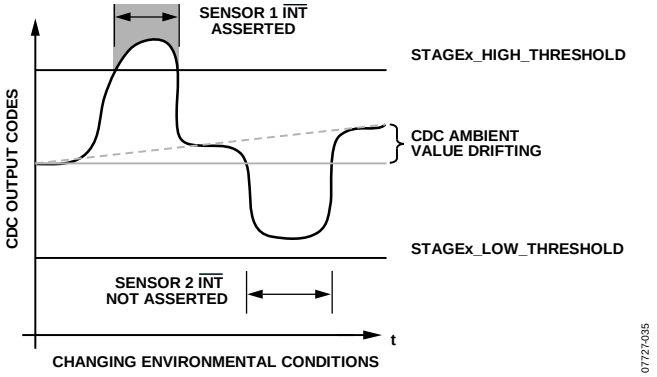



*Figure 35. Typical Sensor Behavior Without Calibration*

## THRESHOLD EQUATIONS

### *On-Chip Logic Stage High Threshold*

$$STAGEx\_HIGH\_THRESHOLD = STAGEx\_SF\_AMBIENT + \left(\frac{STAGEx\_OFFSET\_HIGH}{4}\right) + \left(\frac{\left(STAGEx\_OFFSET\_HIGH - \frac{STAGEx\_OFFSET\_HIGH}{4}\right)}{16}\right) \times POS\_THRESHOLD\_SENSITIVITY \quad (1)$$

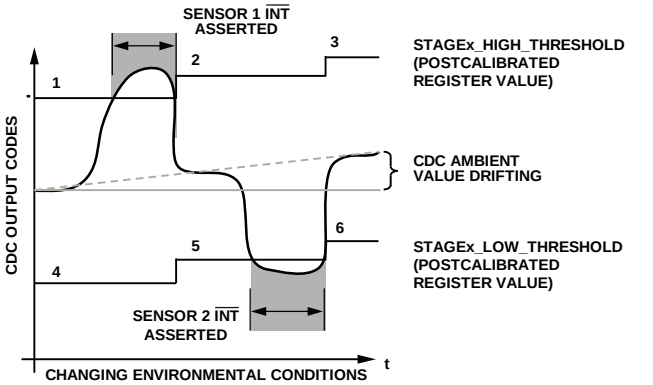
### *On-Chip Logic Stage Low Threshold*

$$STAGEx\_LOW\_THRESHOLD = STAGEx\_SF\_AMBIENT + \left(\frac{STAGEx\_OFFSET\_LOW}{4}\right) + \left(\frac{\left(STAGEx\_OFFSET\_LOW - \frac{STAGEx\_OFFSET\_LOW}{4}\right)}{16}\right) \times NEG\_THRESHOLD\_SENSITIVITY \quad (2)$$

## CAPACITANCE SENSOR BEHAVIOR WITH CALIBRATION

The AD7147A on-chip adaptive calibration algorithm prevents sensor detection errors such as the one shown in Figure 35. This is achieved by monitoring the CDC ambient levels and readjusting the initial STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values according to the amount of ambient drift measured on each sensor. Based on the new stage offset values, the internal STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD values described in Equation 1 and Equation 2 are automatically updated.

This closed-loop routine ensures the reliability and repeatable operation of every sensor connected to the AD7147A when they are subjected to dynamic environmental conditions. Figure 36 shows a simplified example of how the AD7147A applies the adaptive calibration process, resulting in no interrupt errors even with changing CDC ambient levels due to dynamic environmental conditions.




[1]INITIAL STAGEx_OFFSET_HIGH REGISTER VALUE.
[2]POSTCALIBRATED REGISTER STAGEx_HIGH_THRESHOLD.
[3]POSTCALIBRATED REGISTER STAGEx_HIGH_THRESHOLD.
[4]INITIAL STAGEx_LOW_THRESHOLD.
[5]POSTCALIBRATED REGISTER STAGEx_LOW_THRESHOLD.
[6]POSTCALIBRATED REGISTER STAGEx_LOW_THRESHOLD.

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*Figure 36. Typical Sensor Behavior with Calibration Applied on the Data Path*

## SLOW FIFO

As shown in Figure 33, there are a number of FIFOs implemented on the AD7147A. These FIFOs are located in Bank 3 of the on-chip memory. The slow FIFOs are used by the on-chip logic to monitor the ambient capacitance level from each sensor.

### *AVG_FP_SKIP and AVG_LP_SKIP*

In Register 0x001, Bits[13:12] are the slow FIFO skip control for full power mode, AVG_FP_SKIP. Bits[15:14] in the same register are the slow FIFO skip control for low power mode, AVG_LP_SKIP, and determine which CDC samples are not used (skipped) in the slow FIFO. Changing the values of the AVG_FP_SKIP and AVG_LP_SKIP bits slows down or speeds up the rate at which the ambient capacitance value tracks the measured capacitance value read by the converter.

- Slow FIFO update rate in full power mode = AVG_FP_SKIP × [(3 × Decimation Rate) × (SEQUENCE_STAGE_NUM + 1) × (FF_SKIP_CNT + 1) × 4 × $10^{-6}$].
- Slow FIFO update rate in low power mode = ((AVG_LP_SKIP + 1) × (3 × Decimation Rate) × (SEQUENCE_STAGE_NUM + 1) × (4 × $10^{-6}$))+ LP_CONV_DELAY.

The slow FIFO is used by the on-chip logic to track the ambient capacitance value. The slow FIFO expects to receive samples from the converter at a rate between 33 ms and 40 ms. AVG_FP_SKIP and AVG_LP_SKIP are used to normalize the frequency of the samples going into the FIFO, regardless of how many conversion stages are in a sequence.

Determining the AVG_FP_SKIP and AVG_LP_SKIP values is required only once during the initial setup of the capacitance sensor interface. The recommended values for these settings when using all 12 conversion stages on the AD7147A are as follows:

- AVG_FP_SKIP = 00 = skip three samples
- AVG_LP_SKIP = 00 = skip zero samples

## SLOW_FILTER_UPDATE_LVL

SLOW_FILTER_UPDATE_LVL controls whether the most recent CDC measurement goes into the slow FIFO (slow filter). The slow filter is updated when the difference between the current CDC value and the last value of the slow FIFO is greater than the value of SLOW_FILTER_UPDATE_LVL, which is in the Ambient Control 1 register (AMB_COMP_CTRL1), Address 0x003.

# ADAPTIVE THRESHOLD AND SENSITIVITY

The AD7147A provides an on-chip, self-adjusting adaptive threshold and sensitivity algorithm. This algorithm continuously monitors the output levels of each sensor and automatically rescales the threshold levels in proportion to the sensor area covered by the user. As a result, the AD7147A maintains optimal threshold and sensitivity levels for all users regardless of their finger sizes.

The threshold level is always referenced from the ambient level and is defined as the CDC converter output level that must be exceeded before a valid sensor contact can occur. The sensitivity level is defined as how sensitive the sensor must be before a valid contact can be registered.

Figure 37 provides an example of how the adaptive threshold and sensitivity algorithm works. The positive and negative sensor threshold levels are calculated as a percentage of the STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW values and are based on the threshold sensitivity settings and the ambient value. After the AD7147A is configured, initial estimates are supplied for both STAGEx_OFFSET_HIGH and STAGEx_OFFSET_LOW, and then the calibration engine automatically adjusts the STAGEx_HIGH_THRESHOLD and STAGEx_LOW_THRESHOLD values for sensor response.

The AD7147A tracks the average maximum and minimum values measured from each sensor. These values provide an indication of how the user is interacting with the sensor. A large finger results in a large average maximum or minimum value, whereas a small finger results in smaller values. When the average maximum or minimum value changes, the threshold levels are rescaled to ensure that the threshold levels are appropriate for the current user. Figure 38 shows how the minimum and maximum sensor responses are tracked by the on-chip logic.

Reference A in Figure 37 shows a less sensitive threshold level for a user with small fingers and demonstrates the disadvantages of a fixed threshold level.

By enabling the adaptive threshold and sensitivity algorithm, the positive and negative threshold levels are determined by the POS_THRESHOLD_SENSITIVITY and NEG_THRESHOLD_ SENSITIVITY bit values and by the most recent average maximum sensor output value. These bits can be used to select 16 different positive and negative sensitivity levels ranging between 25% and 95.32% of the most recent average maximum output level referenced from the ambient value. The smaller the sensitivity percentage setting, the easier it is to trigger a sensor activation. Reference B shows that the positive adaptive threshold level is set at almost midsensitivity with a 62.51% threshold level by setting POS_THRESHOLD_ SENSITIVITY = 1000. Figure 37 also provides a similar example for the negative threshold level, with NEG_THRESHOLD_SENSITIVITY = 0011.

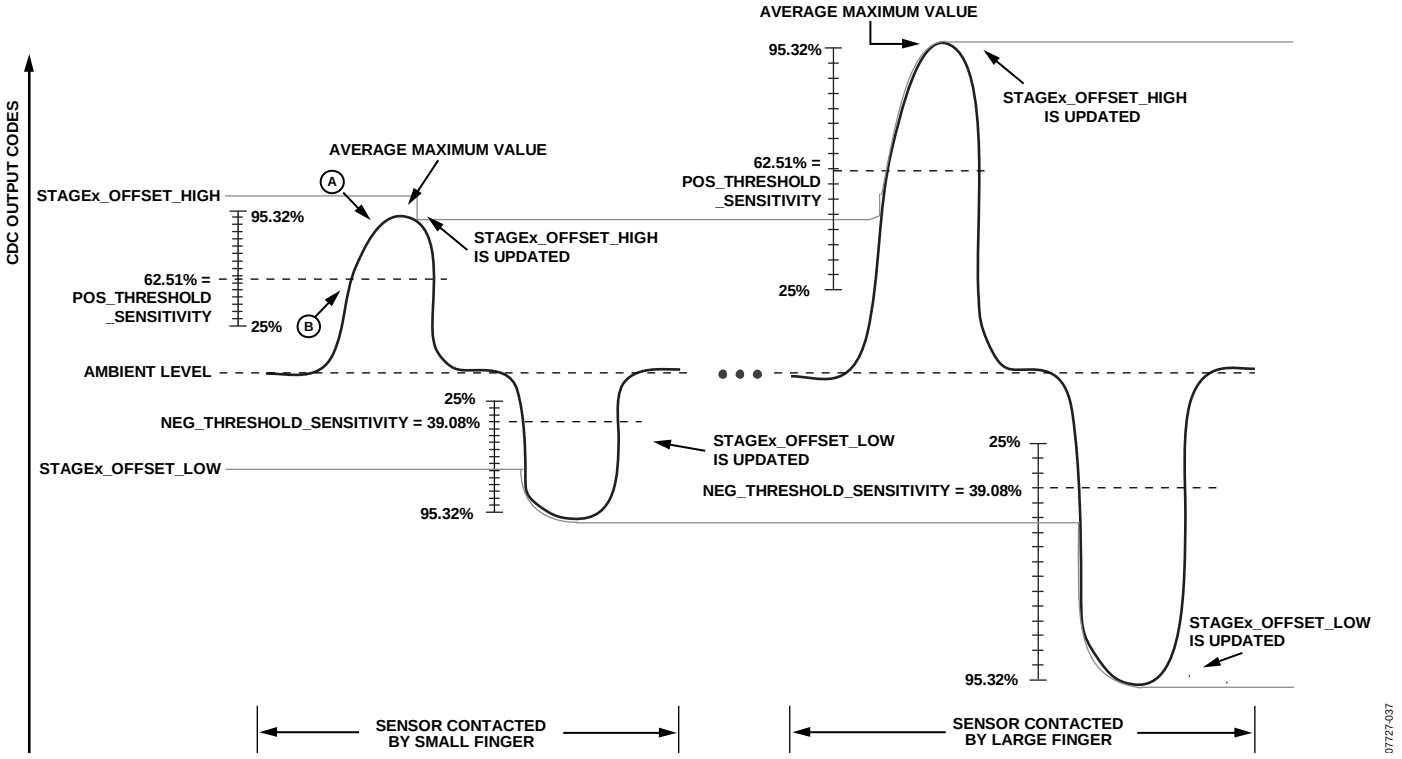



*Figure 37. Example of Threshold Sensitivity (POS_THRESHOLD_SENSITIVITY = 1000, NEG_THRESHOLD_SENSITIVITY = 0011)*

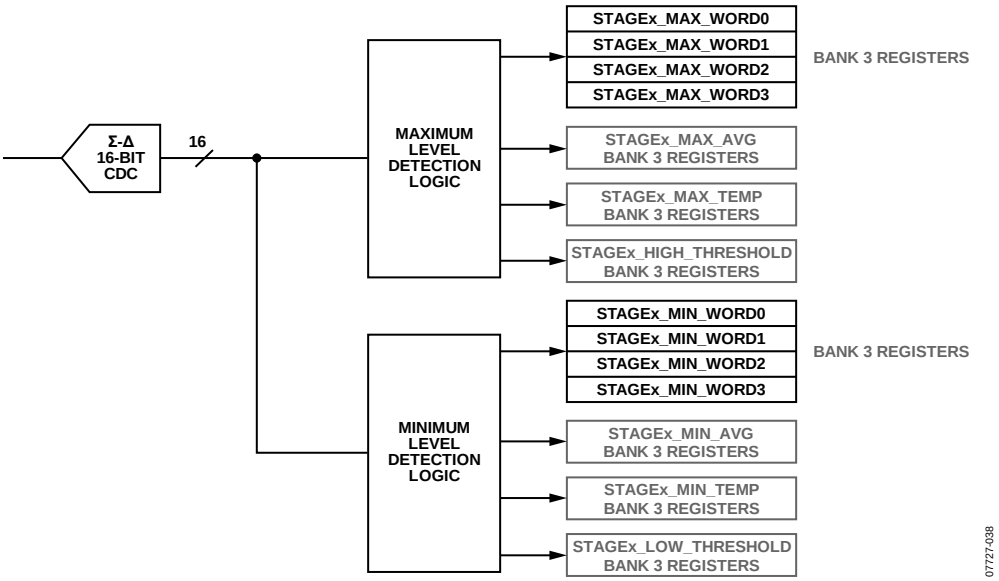



*Figure 38. Tracking the Minimum and Maximum Average Sensor Values*

**Table 15. Additional Information About Environmental Calibration and Adaptive Threshold Registers**

| Register/Bit | Register Location | Description |
|---|---|---|
| NEG_THRESHOLD_SENSITIVITY | Bank 2 | Used in Equation 2. This value is programmed once at startup. |
| NEG_PEAK_DETECT | Bank 2 | Used by internal adaptive threshold logic only.<br>The NEG_PEAK_DETECT is set to a percentage of the difference between the ambient CDC value and the minimum average CDC value. If the output of the CDC approaches the NEG_PEAK_DETECT percentage of the minimum average, the minimum average value is updated. |
| POS_THRESHOLD_SENSITIVITY | Bank 2 | Used in Equation 1. This value is programmed once at startup. |
| POS_PEAK_DETECT | Bank 2 | Used by internal adaptive threshold logic only.<br>The POS_PEAK_DETECT is set to a percentage of the difference between the ambient CDC value and the maximum average CDC value. If the output of the CDC approaches the POS_PEAK_DETECT percentage of the maximum average, the maximum average value is updated. |
| STAGEx_OFFSET_LOW | Bank 2 | Used in Equation 2. An initial value (based on sensor characterization) is programmed into this register at startup. The AD7147A on-chip calibration algorithm automatically updates this register based on the amount of sensor drift due to changing ambient conditions. Set this register to 80% of the STAGEx_OFFSET_LOW_CLAMP value. |
| STAGEx_OFFSET_HIGH | Bank 2 | Used in Equation 1. An initial value (based on sensor characterization) is programmed into this register at startup. The AD7147A on-chip calibration algorithm automatically updates this register based on the amount of sensor drift due to changing ambient conditions. Set this register to 80% of the STAGEx_OFFSET_HIGH_CLAMP value. |
| STAGEx_OFFSET_HIGH_CLAMP | Bank 2 | Used by internal environmental calibration and adaptive threshold algorithms only.<br>An initial value (based on sensor characterization) is programmed into this register at startup. The value in this register prevents a user from causing the output value of a sensor to exceed the expected nominal value.<br>Set this register to the maximum expected sensor response or the maximum change in CDC output code. |
| STAGEx_OFFSET_LOW_CLAMP | Bank 2 | Used by internal environmental calibration and adaptive threshold algorithms only.<br>An initial value (based on sensor characterization) is programmed into this register at startup. The value in this register prevents a user from causing the output value of a sensor to exceed the expected nominal value.<br>Set this register to the minimum expected sensor response or the minimum change in CDC output code. |
| STAGEx_SF_AMBIENT | Bank 3 | Used in Equation 1 and Equation 2. This is the ambient sensor output when the sensor is not touched, as calculated using the slow FIFO. |
| STAGEx_HIGH_THRESHOLD | Bank 3 | Equation 1 value. |
| STAGEx_LOW_THRESHOLD | Bank 3 | Equation 2 value. |

# INTERRUPT OUTPUT

The AD7147A has an interrupt output that triggers an interrupt service routine on the host processor. The $\overline{\text{INT}}$ signal is on Pin A1 and is an open-drain output. There are three types of interrupt events on the AD7147A: a CDC conversion-complete interrupt, a sensor-touch interrupt, and a GPIO interrupt. Each interrupt has enable and status registers. The conversion-complete and sensor-touch (sensor-activation) interrupts can be enabled on a per-conversion-stage basis. The status registers indicate what type of interrupt triggered the $\overline{\text{INT}}$ pin. Status registers are cleared, and the $\overline{\text{INT}}$ signal is reset high during a read operation. The signal returns high as soon as the read address has been set up.

## CDC CONVERSION-COMPLETE INTERRUPT

The AD7147A interrupt signal asserts low to indicate the completion of a conversion stage and that new conversion result data is available in the registers.

The interrupt can be independently enabled for each conversion stage. Each conversion-stage-complete interrupt can be enabled via the STAGE_COMPLETE_INT_ENABLE register (Address 0x007). This register has a bit that corresponds to each conversion stage. Setting this bit to 1 enables the interrupt for that stage. Clearing this bit to 0 disables the conversion-complete interrupt for that stage.

The AD7147A interrupt should be enabled only for the last stage in a conversion sequence. For example, if there are five conversion stages, only the conversion-complete interrupt for STAGE4 is enabled. Therefore, $\overline{\text{INT}}$ asserts only when all five conversion stages are complete and the host can read new data from all five result registers. The interrupt is cleared by reading the STAGE_COMPLETE_INT_STATUS register located at Address 0x00A.

Register 0x00A is the conversion-complete interrupt status register. Each bit in this register corresponds to a conversion stage. If a bit is set, it means that the conversion-complete interrupt for the corresponding stage was triggered. This register is cleared upon a read if the underlying condition that triggered the interrupt is not present.

## SENSOR-TOUCH INTERRUPT

The sensor-touch interrupt mode is implemented when the host processor requires an interrupt only when a sensor is contacted.

Configuring the AD7147A into this mode results in the interrupt being asserted when the user makes contact with the sensor and again when the user stops touching the sensor. The second interrupt is required to alert the host processor that the user is no longer contacting the sensor.

The registers located at Address 0x005 and Address 0x006 are used to enable the interrupt output for each stage. The registers located at Address 0x008 and Address 0x009 are used to read back the interrupt status for each stage.

Figure 39 shows the interrupt output timing during contact with one of the sensors connected to STAGE0 while operating in the sensor-touch interrupt mode. For a low limit configuration, the interrupt output is asserted as soon as the sensor is contacted and again after the user has stopped touching the sensor. (Note that the interrupt output remains low until the host processor reads back the interrupt status registers located at Address 0x008 and Address 0x009.)

The interrupt output is asserted when there is a change in the interrupt status bits. This can indicate that a user is touching the sensor(s) for the first time, the number of sensors being touched has changed, or the user is no longer touching the sensor(s). Reading the status bits in the interrupt status register shows the current sensor activations.

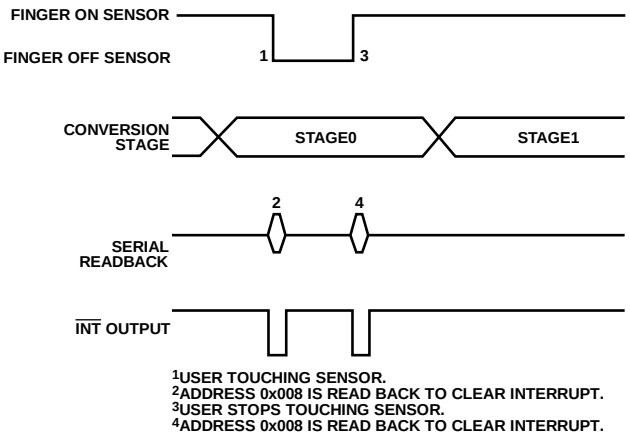
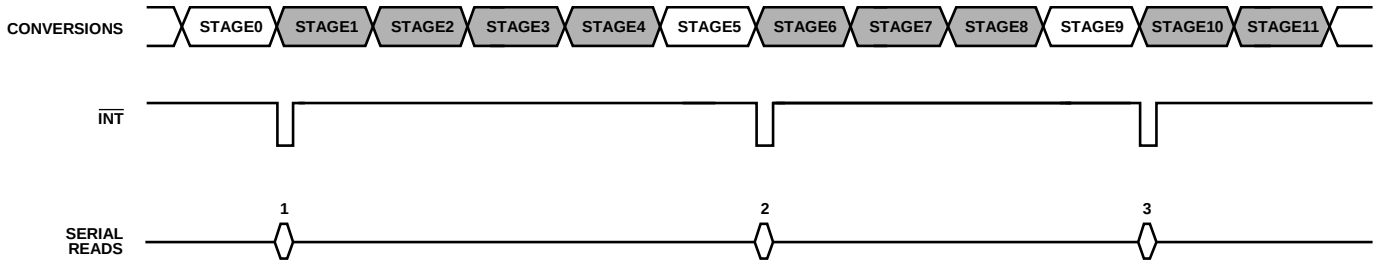



*Figure 39. Example of Sensor-Touch Interrupt*




**NOTES**
**THIS IS AN EXAMPLE OF A CDC CONVERSION-COMPLETE INTERRUPT.**

**THIS TIMING EXAMPLE SHOWS THAT THE INTERRUPT OUTPUT HAS BEEN ENABLED TO BE ASSERTED AT THE END OF A CONVERSION CYCLE FOR STAGE0, STAGE5, AND STAGE9. THE INTERRUPTS FOR ALL OTHER STAGES HAVE BEEN DISABLED.**

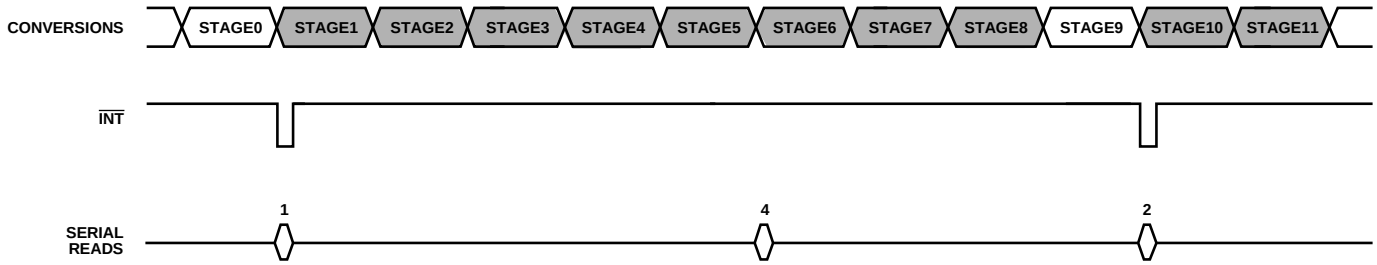
**STAGEx CONFIGURATION PROGRAMMING NOTES FOR STAGE0, STAGE5, AND STAGE9 (x = 0, 5, 9):**
**STAGEx_LOW_INT_ENABLE (ADDRESS 0x005) = 0**
**STAGEx_HIGH_INT_ENABLE (ADDRESS 0x006) = 0**
**STAGEx_COMPLETE_INT_ENABLE (ADDRESS 0x007) = 1**

**STAGEx CONFIGURATION PROGRAMMING NOTES FOR STAGE1 THROUGH STAGE8, STAGE10, AND STAGE11 (x = 1, 2, 3, 4, 6, 7, 8, 10, 11):**
**STAGEx_LOW_INT_ENABLE (ADDRESS 0x005) = 0**
**STAGEx_HIGH_INT_ENABLE (ADDRESS 0x006) = 0**
**STAGEx_COMPLETE_INT_ENABLE (ADDRESS 0x007) = 0**

**SERIAL READBACK REQUIREMENTS FOR STAGE0, STAGE5, AND STAGE9 (THIS READBACK OPERATION IS REQUIRED TO CLEAR THE INTERRUPT OUTPUT.):**
**[1]READ THE STAGE0_COMPLETE_INT_STATUS (ADDRESS 0x00A) BIT**
**[2]READ THE STAGE5_COMPLETE_INT_STATUS (ADDRESS 0x00A) BIT**
**[3]READ THE STAGE9_COMPLETE_INT_STATUS (ADDRESS 0x00A) BIT**

07727-040

*Figure 40. Example of Configuring the Registers for Conversion-Complete Interrupt Setup*




**NOTES**
**THIS IS AN EXAMPLE OF A SENSOR-TOUCH INTERRUPT FOR A CASE WHERE THE LOW THRESHOLD LEVELS WERE EXCEEDED.**

**FOR EXAMPLE, THE SENSOR CONNECTED TO STAGE0 AND STAGE9 WERE CONTACTED, AND THE LOW THRESHOLD LEVELS WERE EXCEEDED, RESULTING IN THE INTERRUPT BEING ASSERTED. THE STAGE6 INTERRUPT WAS NOT ASSERTED BECAUSE THE USER DID NOT CONTACT THE SENSOR CONNECTED TO STAGE6.**

**STAGEx CONFIGURATION PROGRAMMING NOTES FOR STAGE0, STAGE6, AND STAGE9 (x = 0, 6, 9):**
**STAGEx_LOW_INT_ENABLE (ADDRESS 0x005) = 1**
**STAGEx_HIGH_INT_ENABLE (ADDRESS 0x006) = 0**
**STAGEx_COMPLETE_INT_ENABLE (ADDRESS 0x007) = 0**

**STAGEx CONFIGURATION PROGRAMMING NOTES FOR STAGE1 THROUGH STAGE7, STAGE8, STAGE10, AND STAGE11 (x = 1, 2, 3, 4, 5, 7, 8, 10, 11):**
**STAGEx_LOW_INT_ENABLE (ADDRESS 0x005) = 0**
**STAGEx_HIGH_INT_ENABLE (ADDRESS 0x006) = 0**
**STAGEx_COMPLETE_INT_ENABLE (ADDRESS 0x007) = 0**

**SERIAL READBACK REQUIREMENTS FOR STAGE0 AND STAGE9 (THIS READBACK OPERATION IS REQUIRED TO CLEAR THE INTERRUPT OUTPUT.):**
**[1]READ THE STAGE0_LOW_INT_STATUS (ADDRESS 0x008) BIT**
**[2]READ THE STAGE5_LOW_INT_STATUS (ADDRESS 0x008) BIT**

07727-041

*Figure 41. Example of Configuring the Registers for Sensor-Touch Interrupt Setup*

## GPIO $\overline{\text{INT}}$ OUTPUT CONTROL

The $\overline{\text{INT}}$ output signal can be controlled by the GPIO pin when the GPIO is configured as an input. The GPIO is configured as an input by setting the GPIO_SETUP bits in the interrupt enable register to 01. See the General-Purpose Input/Output (GPIO) section for more information on how to configure the GPIO.

Enable the GPIO interrupt by setting the GPIO_INT_ENABLE bit in Register 0x007 to 1, or disable the GPIO interrupt by clearing this bit to 0. The GPIO status bit in the conversion-complete interrupt status register reflects the status of the GPIO interrupt. This bit is set to 1 when the GPIO has triggered $\overline{\text{INT}}$. The bit is cleared upon reading the GPIO_INT_STATUS bit if the condition that caused the interrupt is no longer present.

The GPIO interrupt can be set to trigger on a rising edge, falling edge, high level, or low level at the GPIO input pin. Table 16 shows how the settings of the GPIO_INPUT_CONFIG bits in the interrupt enable (STAGE_LOW_INT_ENABLE) register affect the behavior of $\overline{\text{INT}}$.

Figure 42 to Figure 45 show how the interrupt output is cleared upon a read from the GPIO_INT_STATUS bit.

**Table 16. GPIO Interrupt Behavior**

| GPIO_INPUT_CONFIG | GPIO Pin | GPIO_INT_STATUS | $\overline{\text{INT}}$ | $\overline{\text{INT}}$ Behavior |
|---|---|---|---|---|
| 00 = Negative Level Triggered | 1 | 0 | 1 | Not triggered |
| 00 = Negative Level Triggered | 0 | 1 | 0 | Asserted while signal on GPIO pin is low |
| 01 = Positive Edge Triggered | 1 | 1 | 0 | Pulses low at low-to-high GPIO transition |
| 01 = Positive Edge Triggered | 0 | 0 | 1 | Not triggered |
| 10 = Negative Edge Triggered | 1 | 0 | 1 | Pulses low at high-to-low GPIO transition |
| 10 = Negative Edge Triggered | 0 | 1 | 0 | Not triggered |
| 11 = Positive Level Triggered | 1 | 1 | 0 | Asserted while signal on GPIO pin is high |
| 11 = Positive Level Triggered | 0 | 0 | 1 | Not triggered |

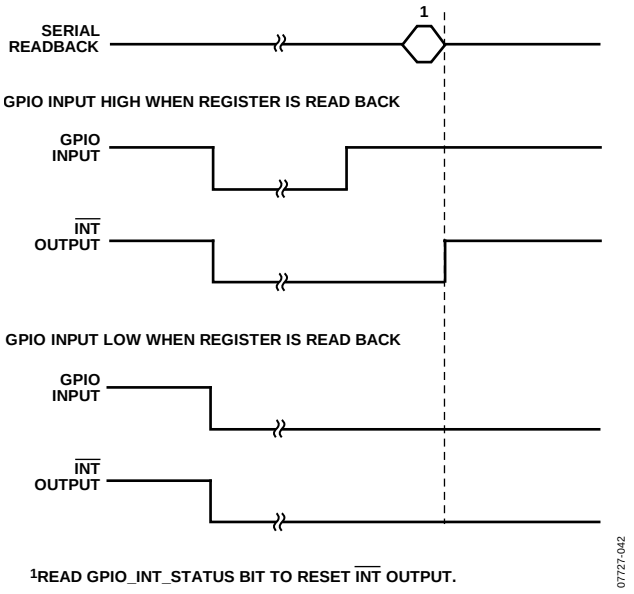



*Figure 42. Example of $\overline{INT}$ Output Controlled by the GPIO Input (GPIO_SETUP = 01, GPIO_INPUT_CONFIG = 00)*

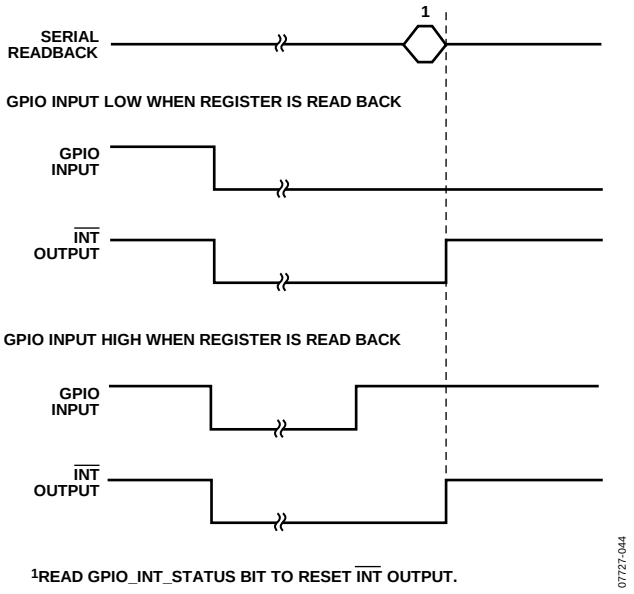



*Figure 44. Example of $\overline{INT}$ Output Controlled by the GPIO Input (GPIO_SETUP = 01, GPIO_INPUT_CONFIG = 10)*

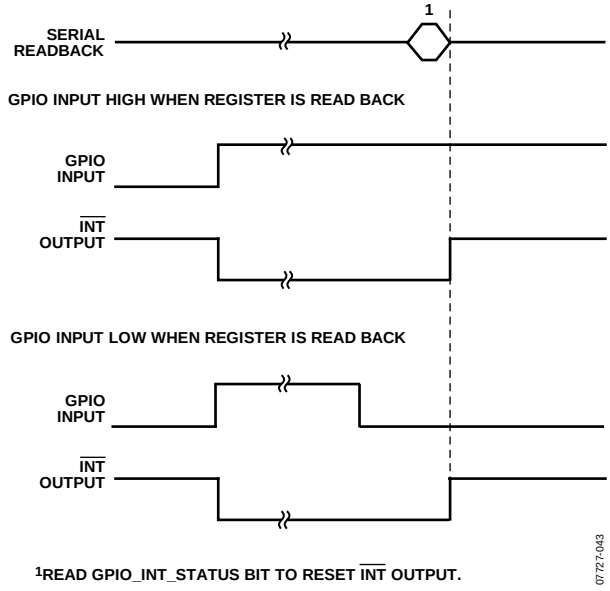



*Figure 43. Example of $\overline{INT}$ Output Controlled by the GPIO Input (GPIO_SETUP = 01, GPIO_INPUT_CONFIG = 01)*

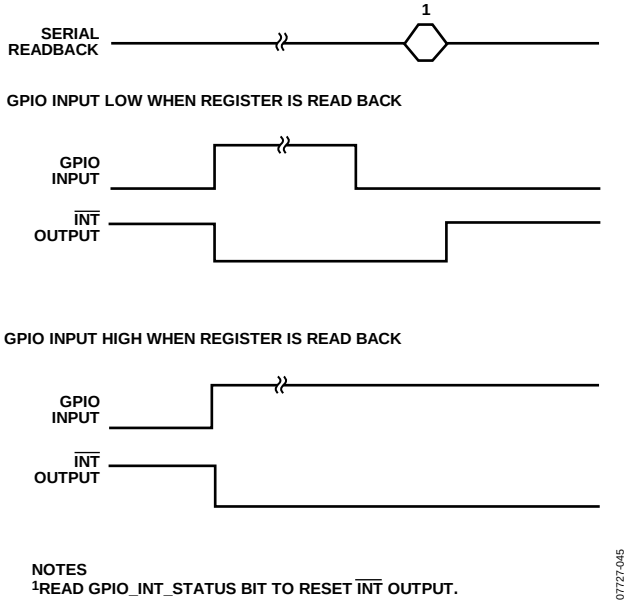



*Figure 45. Example of $\overline{INT}$ Output Controlled by the GPIO Input (GPIO_SETUP = 01, GPIO_INPUT_CONFIG = 11)*

# OUTPUTS

## $AC_{SHIELD}$ OUTPUT

The AD7147A measures the capacitance between CINx and ground. Any capacitance to ground on the signal path between the CINx pins and the sensor is included in the AD7147A conversion result.

To eliminate stray capacitance to ground, the $AC_{SHIELD}$ signal should be used to shield the connection between the sensor and CINx, as shown in Figure 46. The plane around the sensors should also be connected to $AC_{SHIELD}$.

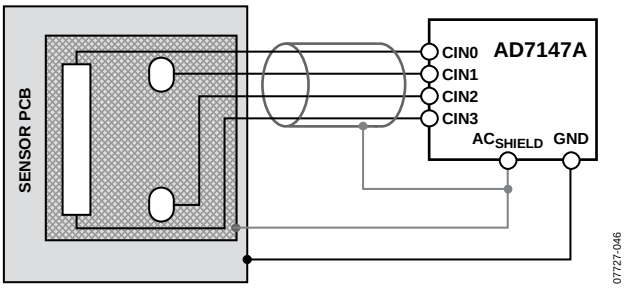



*Figure 46. $AC_{SHIELD}$*

The $AC_{SHIELD}$ output is the same signal waveform as the excitation signal on CINx. Therefore, there is no ac current between CINx and $AC_{SHIELD}$, and any capacitance between these pins does not affect the CINx charge transfer.

Using $AC_{SHIELD}$ eliminates capacitance-to-ground pickup, which means that the AD7147A can be placed up to 10 cm away from the sensors. This allows the AD7147A to be placed on a separate PCB from that of the sensors if the connections between the sensors and the CINx inputs are correctly shielded using $AC_{SHIELD}$.

## GENERAL-PURPOSE INPUT/OUTPUT (GPIO)

The AD7147A has one GPIO pin. It can be configured as an input or an output. The GPIO_SETUP Bits[13:12] in the STAGE_LOW_INT_ENABLE register determine how the GPIO pin is configured.

**Table 17. GPIO_SETUP Bits**

| GPIO_SETUP | GPIO Configuration |
|---|---|
| 00 | GPIO disabled |
| 01 | Input |
| 10 | Output low |
| 11 | Output high |

When the GPIO is configured as an output, the voltage level on the pin is set to either a low level or a high level, as defined by the GPIO_SETUP bits (see Table 17).

The GPIO_INPUT_CONFIG bits in the STAGE_LOW_INT_ENABLE register determine the response of the AD7147A to a signal on the GPIO pin when the GPIO is configured as an input. The GPIO can be configured as either active high or active low, as well as either edge triggered or level triggered (see Table 18).

**Table 18. GPIO_INPUT_CONFIG Bits**

| GPIO_INPUT_CONFIG | GPIO Configuration |
|---|---|
| 00 | Triggered on negative level (active low) |
| 01 | Triggered on positive edge (active high) |
| 10 | Triggered on negative edge (active low) |
| 11 | Triggered on positive level (active high) |

When GPIO is configured as an input, it triggers the interrupt output on the AD7147A.

Table 16 lists the interrupt output behavior for each of the GPIO configuration setups.

## USING THE GPIO TO TURN ON/OFF AN LED

The GPIO on the AD7147A can be used to turn an LED on and off by setting the GPIO as either output high or low. Setting the GPIO output high turns on the LED; setting the GPIO output low turns off the LED. The GPIO pin connects to a transistor that provides the drive current for the LED. Suitable transistors include the KTC3875 from Korea Electronics Co., Ltd. (KEC).

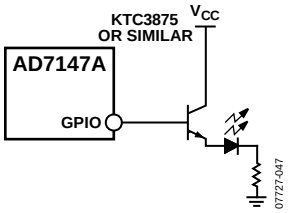



*Figure 47. Controlling an LED Using the GPIO*

# SERIAL INTERFACES

The AD7147A is available with an SPI interface. The AD7147A-1 is available with an I²C-compatible interface. Both parts are the same, with the exception of the serial interface.

## SPI INTERFACE

The AD7147A has a 4-wire serial peripheral interface (SPI). The SPI has a data input pin (SDI) for inputting data to the device, a data output pin (SDO) for reading data back from the device, and a data clock pin (SCLK) for clocking data into and out of the device. A chip select pin ($\overline{CS}$) enables or disables the serial interface. $\overline{CS}$ is required for correct operation of the SPI. Data is clocked out of the AD7147A on the negative edge of SCLK and data is clocked into the device on the positive edge of SCLK.

### *SPI Command Word*

All data transactions on the SPI bus begin with the master taking $\overline{CS}$ from high to low and sending out the command word. This indicates to the AD7147A whether the transaction is a read or a write and provides the address of the register from which to begin the data transfer. The following bit map shows the SPI command word.

**MSB** **LSB**

| 15 | 14 | 13 | 12 | 11 | 10 | 9:0 |
|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 0 | 0 | R/$\overline{W}$ | Register address |

Bits[15:11] of the command word must be set to 11100 to successfully begin a bus transaction.

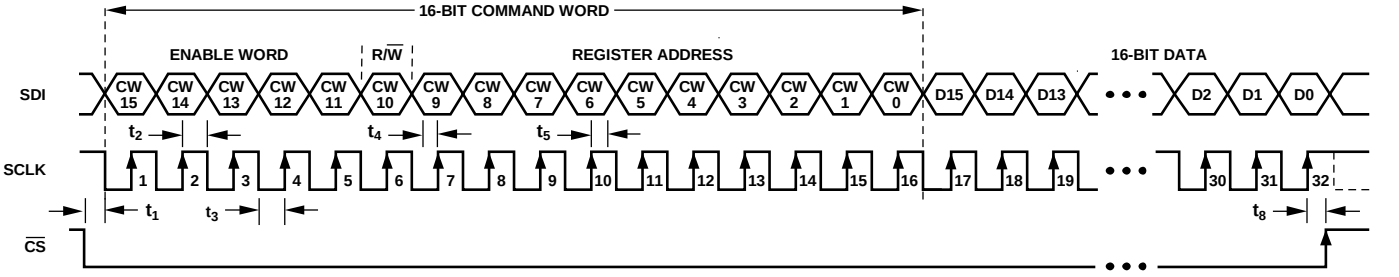
Bit 10 is the read/write bit; 1 indicates a read, and 0 indicates a write.

Bits[9:0] contain the target register address. When reading or writing to more than one register, this address indicates the address of the first register to be written to or read from.

### *Writing Data*

Data is written to the AD7147A in 16-bit words. The first word written to the device is the command word, with the read/write bit set to 0. The master then supplies the 16-bit input data-word on the SDI line. The AD7147A clocks the data into the register addressed in the command word. If there is more than one word of data to be clocked in, the AD7147A automatically increments the address pointer and clocks the subsequent data-word into the next register.

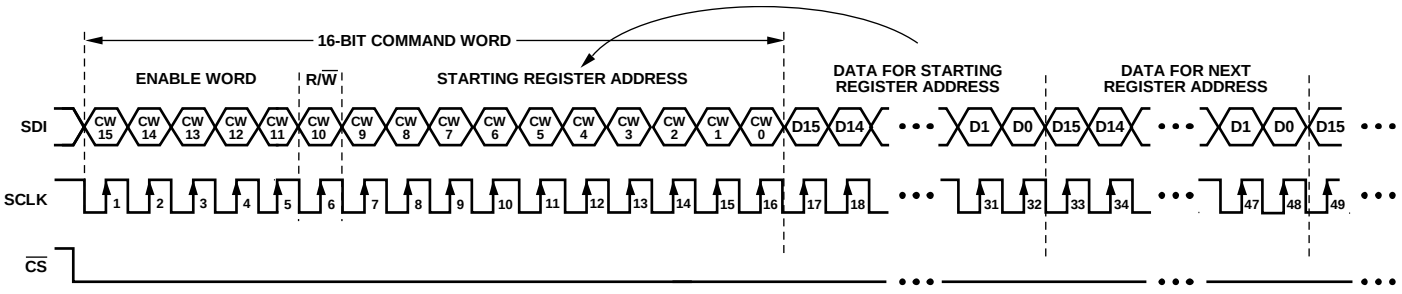
The AD7147A continues to clock in data on the SDI line until either the master finishes the write transition by pulling $\overline{CS}$ high or the address pointer reaches its maximum value. The AD7147A address pointer does not wrap around. When it reaches its maximum value, any data provided by the master on the SDI line is ignored by the AD7147A.




NOTES
1. SDI BITS ARE LATCHED ON SCLK RISING EDGES. SCLK CAN IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
2. ALL 32 BITS MUST BE WRITTEN: 16 BITS FOR THE CONTROL WORD AND 16 BITS FOR THE DATA.
3. 16-BIT COMMAND WORD SETTINGS FOR SERIAL WRITE OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 0 (R/$\overline{W}$)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (10-BIT MSB-JUSTIFIED REGISTER ADDRESS)

07727-048

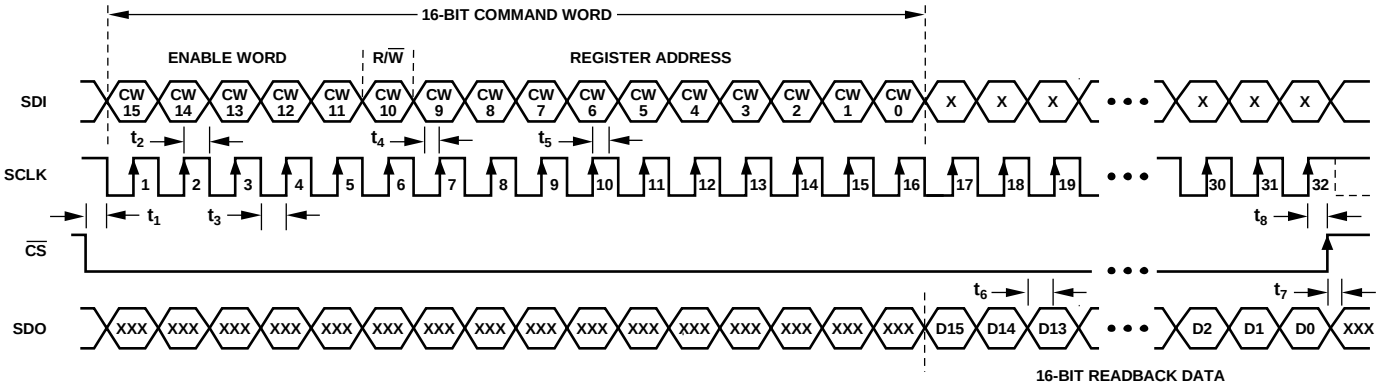
*Figure 48. Single Register Write SPI Timing*




NOTES
1. MULTIPLE SEQUENTIAL REGISTERS CAN BE LOADED CONTINUOUSLY.
2. THE FIRST (LOWEST ADDRESS) REGISTER ADDRESS IS WRITTEN, FOLLOWED BY MULTIPLE 16-BIT DATA-WORDS.
3. THE ADDRESS AUTOMATICALLY INCREMENTS WITH EACH 16-BIT DATA-WORD (ALL 16 BITS MUST BE WRITTEN).
4. CS IS HELD LOW UNTIL THE LAST DESIRED REGISTER HAS BEEN LOADED.
5. 16-BIT COMMAND WORD SETTINGS FOR SEQUENTIAL WRITE OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 0 (R/W)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (STARTING MSB-JUSTIFIED REGISTER ADDRESS)

07727-049

*Figure 49. Sequential Register Write SPI Timing*




NOTES
1. SDI BITS ARE LATCHED ON SCLK RISING EDGES. SCLK CAN IDLE HIGH OR LOW BETWEEN WRITE OPERATIONS.
2. THE 16-BIT CONTROL WORD MUST BE WRITTEN ON SDI: 5 BITS FOR ENABLE WORD, 1 BIT FOR R/W, AND 10 BITS FOR REGISTER ADDRESS.
3. THE REGISTER DATA IS READ BACK ON THE SDO PIN.
4. X DENOTES DON'T CARE.
5. XXX DENOTES HIGH IMPEDANCE THREE-STATE OUTPUT.
6. CS IS HELD LOW UNTIL ALL REGISTER BITS HAVE BEEN READ BACK.
7. 16-BIT COMMAND WORD SETTINGS FOR SINGLE READBACK OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 1 (R/W)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (10-BIT MSB-JUSTIFIED REGISTER ADDRESS)

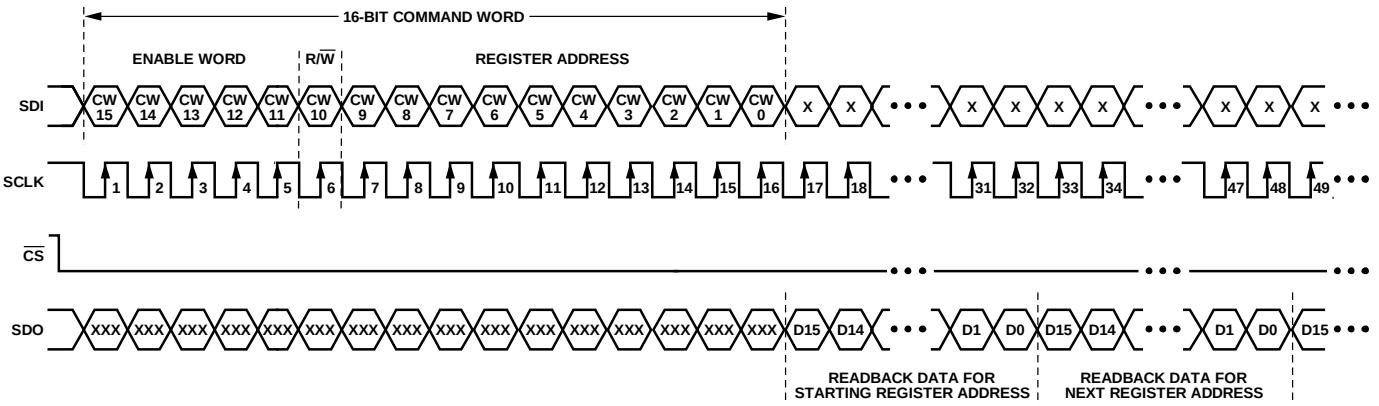
07727-050

*Figure 50. Single Register Readback SPI Timing*

### *Reading Data*

A read transaction begins when the master writes the command word to the AD7147A with the read/write bit set to 1. The master then supplies 16 clock pulses per data-word to be read, and the AD7147A clocks out data from the addressed register on the SDO line. The first data-word is clocked out on the first falling edge of SCLK following the command word, as shown in Figure 50.

The AD7147A continues to clock out data on the SDO line if the master continues to supply the clock signal on SCLK. The read transaction finishes when the master takes CS high. If the AD7147A address pointer reaches its maximum value, the AD7147A repeatedly clocks out data from the addressed register. The address pointer does not wrap around.




NOTES
1. MULTIPLE REGISTERS CAN BE READ BACK CONTINUOUSLY.
2. THE 16-BIT CONTROL WORD MUST BE WRITTEN ON SDI: 5 BITS FOR ENABLE WORD, 1 BIT FOR R/$\overline{W}$, AND 10 BITS FOR REGISTER ADDRESS.
3. THE ADDRESS AUTOMATICALLY INCREMENTS WITH EACH 16-BIT DATA-WORD BEING READ BACK ON THE SDO PIN.
4. $\overline{CS}$ IS HELD LOW UNTIL ALL REGISTER BITS HAVE BEEN READ BACK.
5. X DENOTES DON'T CARE.
6. XXX DENOTES HIGH IMPEDANCE THREE-STATE OUTPUT.
7. 16-BIT COMMAND WORD SETTINGS FOR SEQUENTIAL READBACK OPERATION:
   CW[15:11] = 11100 (ENABLE WORD)
   CW[10] = 1 (R/$\overline{W}$)
   CW[9:0] = [AD9, AD8, AD7, AD6, AD5, AD4, AD3, AD2, AD1, AD0] (STARTING MSB-JUSTIFIED REGISTER ADDRESS)

07727-051

*Figure 51. Sequential Register Readback SPI Timing*

## I²C-COMPATIBLE INTERFACE

The AD7147A-1 supports the industry standard, 2-wire I²C serial interface protocol. The two wires associated with the I²C timing are the SCLK and SDA inputs. The SDA is an I/O pin that allows both register write and register readback operations. The AD7147A-1 is always a slave device on the I²C serial interface bus.

The AD7147A-1 has a 7-bit device address, Address 0101 1XX. The lower two bits are set by tying the ADD0 and ADD1 pins high or low. The AD7147A-1 responds when the master device sends its device address over the bus. The AD7147A-1 cannot initiate data transfers on the bus.

**Table 19. AD7147A-1 I²C Device Address**

| ADD1 | ADD0 | I²C Address |
|---|---|---|
| 0 | 0 | 0101 100 |
| 0 | 1 | 0101 101 |
| 1 | 0 | 0101 110 |
| 1 | 1 | 0101 111 |

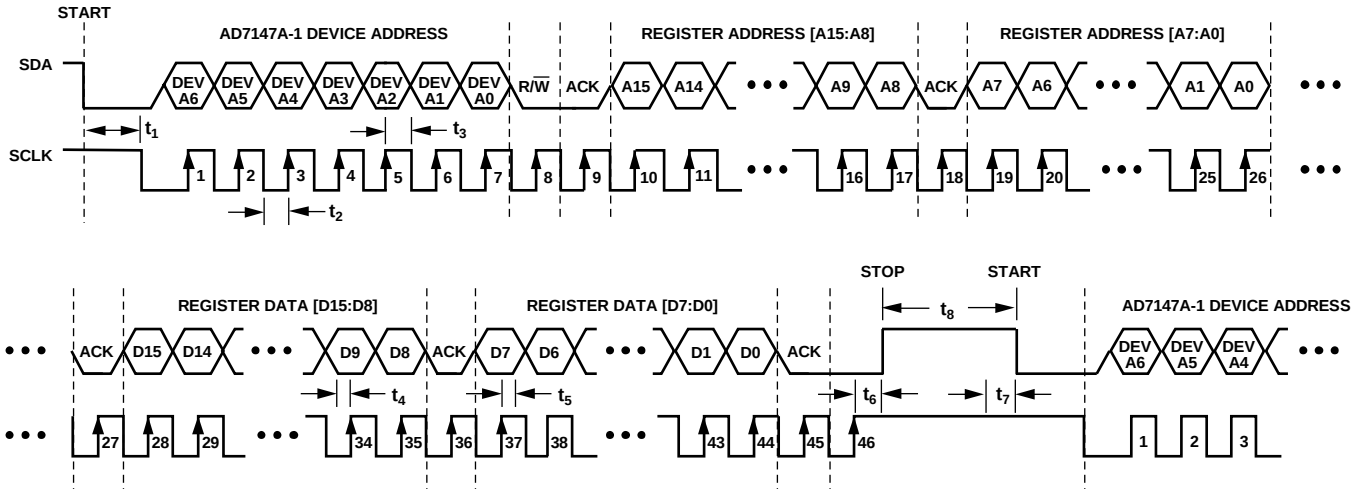
### *Data Transfer*

Data is transferred over the I²C serial interface in 8-bit bytes. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCLK, remains high. This indicates that an address/data stream follows.

All slave peripherals connected to the serial bus respond to the start condition and shift in the next eight bits, consisting of a 7-bit address (MSB first) plus an R/$\overline{W}$ bit that determines the direction of the data transfer. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the ninth clock pulse. This is known as the acknowledge bit. All other devices on the bus then remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is 0, the master writes to the slave device. If the R/$\overline{W}$ bit is 1, the master reads from the slave device.

Data is sent over the serial bus in a sequence of nine clock pulses—eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high can be interpreted as a stop signal. The number of data bytes transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes are read or written, a stop condition is established. A stop condition is defined by a low-to-high transition on SDA while SCLK remains high. If the AD7147A encounters a stop condition, it returns to its idle condition, and the address pointer register resets to Address 0x00.




**NOTES**
1. A START CONDITION AT THE BEGINNING IS DEFINED AS A HIGH-TO-LOW TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
2. A STOP CONDITION AT THE END IS DEFINED AS A LOW-TO-HIGH TRANSITION ON SDA WHILE SCLK REMAINS HIGH.
3. 7-BIT DEVICE ADDRESS [DEV A6:DEV A0] = [0 1 0 1 1 X X], WHERE X IS A DON'T CARE BIT.
4. 16-BIT REGISTER ADDRESS [A15:A0] = [X, X, X, X, X, A9, A8, A7, A6, A5, A4, A3, A2, A1, A0], WHERE X IS A DON'T CARE BIT.
5. REGISTER ADDRESS [A15:A8] AND REGISTER ADDRESS [A7:A0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.
6. REGISTER DATA [D15:D8] AND REGISTER DATA [D7:D0] ARE ALWAYS SEPARATED BY A LOW ACK BIT.

07727-052

*Figure 52. Example of I²C Timing for Single Register Write Operation*

### *Writing Data over the I²C Bus*

The process for writing to the AD7147A-1 over the I²C bus is shown in Figure 52 and Figure 54. The device address is sent over the bus, followed by the R/$\overline{W}$ bit being set to 0 and then two bytes of data that contain the 10-bit address of the internal data register to be written. The following bit map shows the upper register address bytes. Note that Bit 7 to Bit 2 in the upper address byte are don't care bits. The address is contained in the 10 LSBs of the register address bytes.

**MSB** **LSB**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| X | X | X | X | X | X | Register Address Bit 9 | Register Address Bit 8 |

The following bit map shows the lower register address bytes:

**MSB** **LSB**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| Reg Add Bit 7 | Reg Add Bit 6 | Reg Add Bit 5 | Reg Add Bit 4 | Reg Add Bit 3 | Reg Add Bit 2 | Reg Add Bit 1 | Reg Add Bit 0 |

The third data byte contains the eight MSBs of the data to be written to the internal register. The fourth data byte contains the eight LSBs of data to be written to the internal register.

The AD7147A-1 address pointer register automatically increments after each write. This allows the master to sequentially write to all registers on the AD7147A-1 in the same write transaction. However, the address pointer register does not wrap around after the last address. Therefore, any data written to the AD7147A-1 after the address pointer has reached its maximum value is discarded.

All registers on the AD7147A-1 are 16 bits. Two consecutive 8-bit data bytes are combined and written to the 16-bit registers. To avoid errors, all writes to the device must contain an even number of data bytes.

To finish the transaction, the master generates a stop condition on SDO, or generates a repeat start condition if the master is to maintain control of the bus.

### *Reading Data over the I²C Bus*

To read from the AD7147A-1, the address pointer register must first be set to the address of the required internal register. The master performs a write transaction and then writes to the AD7147A-1 to set the address pointer. Next, the master outputs a repeat start condition to keep control of the bus, or if this is not possible, ends the write transaction with a stop condition. A read transaction is initiated, with the R/$\overline{W}$ bit set to 1.

The AD7147A-1 supplies the upper eight bits of data from the addressed register in the first readback byte, followed by the lower eight bits in the next byte. This is shown in Figure 53 and Figure 54.

Because the address pointer automatically increments after each read, the AD7147A-1 continues to output readback data until the master sends a no acknowledge and stop condition to the bus. If the address pointer reaches its maximum value and the master continues to read from the part, the AD7147A-1 repeatedly sends data from the last register that was addressed.

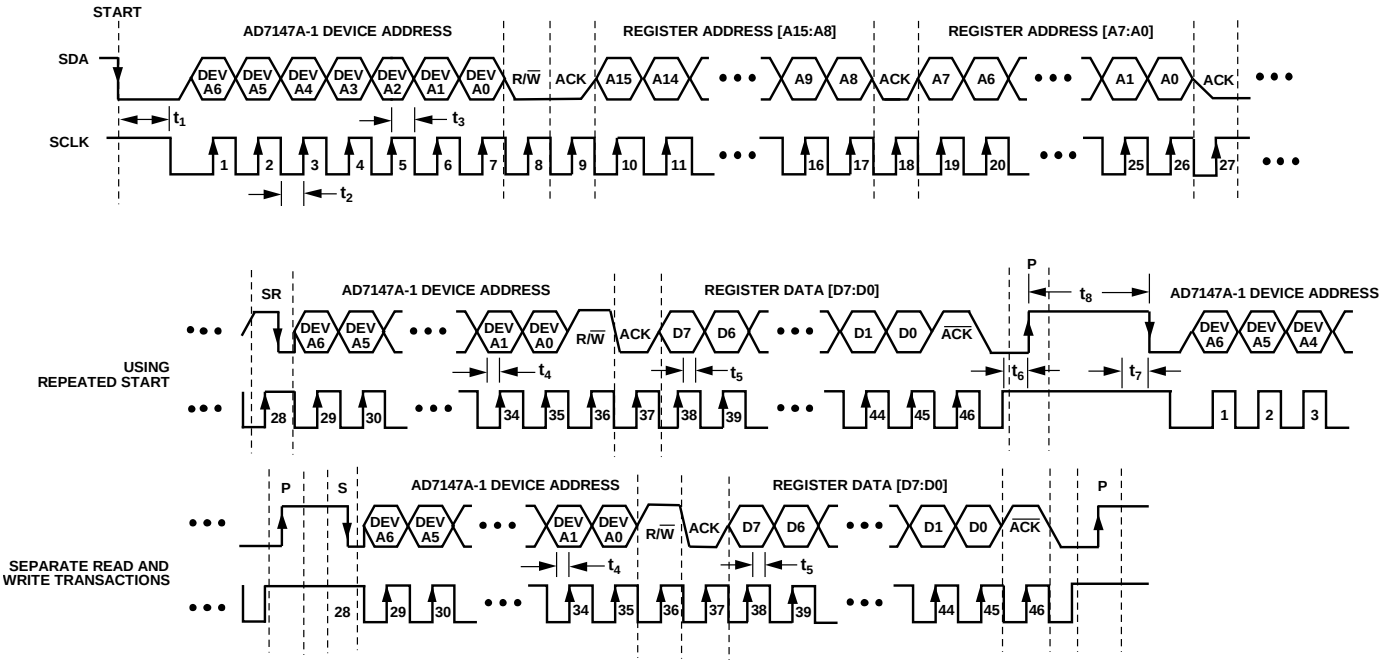



*Figure 53. Example of I²C Timing for Single Register Readback Operation*

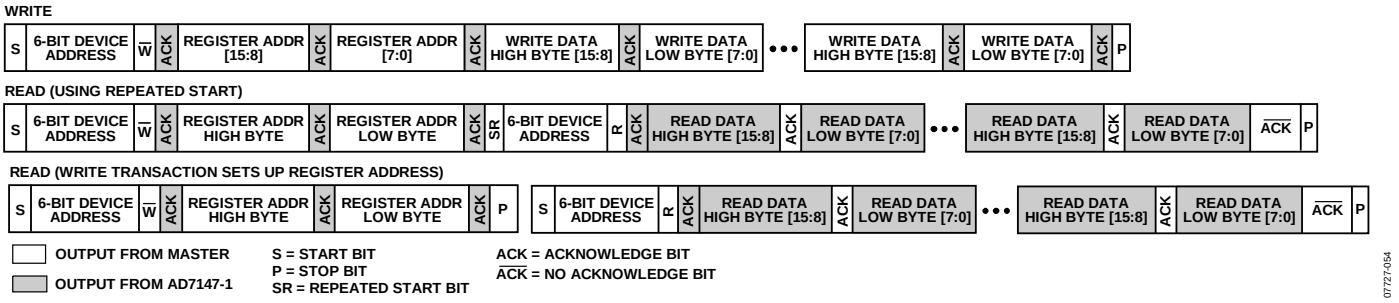



*Figure 54. Example of Sequential I²C Write and Readback Operations*

## $V_{DRIVE}$ INPUT

The supply voltage for the pins (SDO, SDI, SCLK, SDA, $\overline{CS}$, $\overline{INT}$, and GPIO) associated with both the I²C and SPI serial interfaces is supplied from the $V_{DRIVE}$ pin and is separate from the main $V_{CC}$ supply.

This allows the AD7147A to be connected directly to processors whose supply voltage is less than the minimum operating voltage of the AD7147A without the need for external level-shifters. The $V_{DRIVE}$ pin can be connected to voltage supplies as low as 1.65 V and as high as $V_{CC}$.

# PCB DESIGN GUIDELINES

## CAPACITIVE SENSOR BOARD MECHANICAL SPECIFICATIONS

**Table 20.**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Distance from Edge of Any Sensor to Edge of Grounded Metal Object | $D_1$ | 0.1 | | | mm |
| Distance Between Sensor Edges[1] | $D_2 = D_3 = D_4$ | 0 | | | mm |
| Distance Between Bottom of Sensor Board and Controller Board or Grounded Metal Casing[2] | $D_5$ | | 1.0 | | mm |

[1] The distance is dependent on the application and the position of the switches relative to each other and with respect to the user's finger position and handling. Adjacent sensors with no space between them are implemented differentially.

[2] The 1.0 mm specification is intended to prevent direct sensor board contact with any conductive material. This specification, however, does not guarantee an absence of EMI coupling from the controller board to the sensors. To avoid potential EMI-coupling issues, place a grounded metal shield between the capacitive sensor board and the main controller board, as shown in Figure 57.

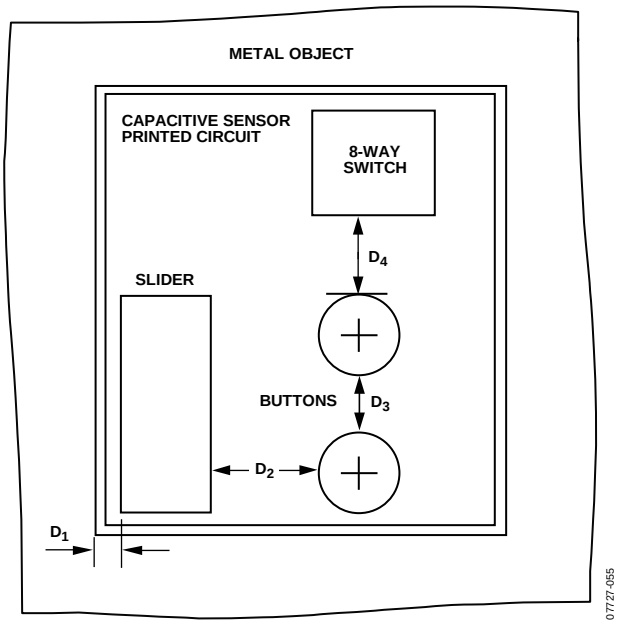



*Figure 55. Capacitive Sensor Board, Top View*

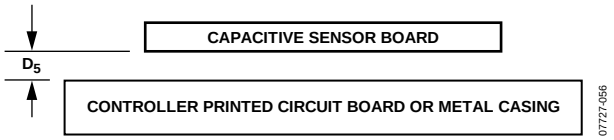



*Figure 56. Capacitive Sensor Board, Side View*

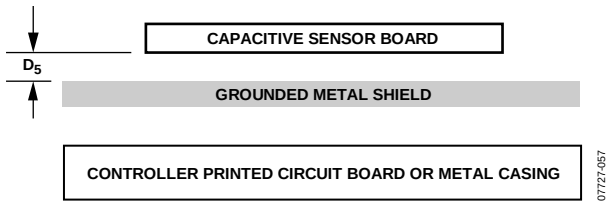



*Figure 57. Capacitive Sensor Board with Grounded Shield*

## WLCSP PACKAGE

Nonsolder mask definer PCB fabrication is recommended to increase the reliability of the solder joint.

The copper pad on the user's PCB should be 80% of the diameter of the WLCSP ball. The solder mask opening should be 50 µm on either side of the copper pad.

See the AN-617 Application Note, *MicroCSP™ Wafer Level Chip Scale Package*, for more information and layout guidelines for the WLCSP package.

# POWER-UP SEQUENCE

To power up the AD7147A, use the following sequence when initially developing the AD7147A and microprocessor serial interface:

1. Turn on the power supplies to the AD7147A.
2. Write to the Bank 2 registers at Address 0x080 through Address 0x0DF. These registers are contiguous; therefore, a sequential register write sequence can be applied.
   Note that the Bank 2 register values are unique for each application. Register values come from characterization of the sensor in the application. The characterization process is outlined in the AN-929 Application Note, available from Analog Devices.
3. Write to the Bank 1 registers at Address 0x000 through Address 0x007, outlined as follows. These registers are contiguous; therefore, a sequential register write sequence can be applied (see Figure 49 and Figure 54).
   Caution: At this time, Address 0x001 must remain set to a default value of 0x0000 during this contiguous write operation.
   Register values:
   Address 0x000 = 0x82B2
   Address 0x001 = 0x000
   Address 0x002 = 0x3230 (depends on number of conversion stages used)
   Address 0x003 = 0x419
   Address 0x004 = 832
   Address 0x005 = interrupt enable register (depends on required interrupt behavior)
   Address 0x006 = interrupt enable register (depends on required interrupt behavior)
   Address 0x007 = interrupt enable register (depends on required interrupt behavior)
4. Write to the Bank 1 register, Address 0x001 = 0x0FFF (depends on number of conversion stages used).
5. Read back the corresponding interrupt status register at Address 0x008, Address 0x009, or Address 0x00A. This is determined by the interrupt output configuration, as explained in the Interrupt Output section.
   Note that the specific registers required to be read back depend on each application. For buttons, the interrupt status registers are read back while other sensors read data back from the AD7147A according to the slider or wheel algorithm requirements. Analog Devices can provide this information after the user develops the sensor board.
6. Repeat Step 5 every time $\overline{\text{INT}}$ is asserted.

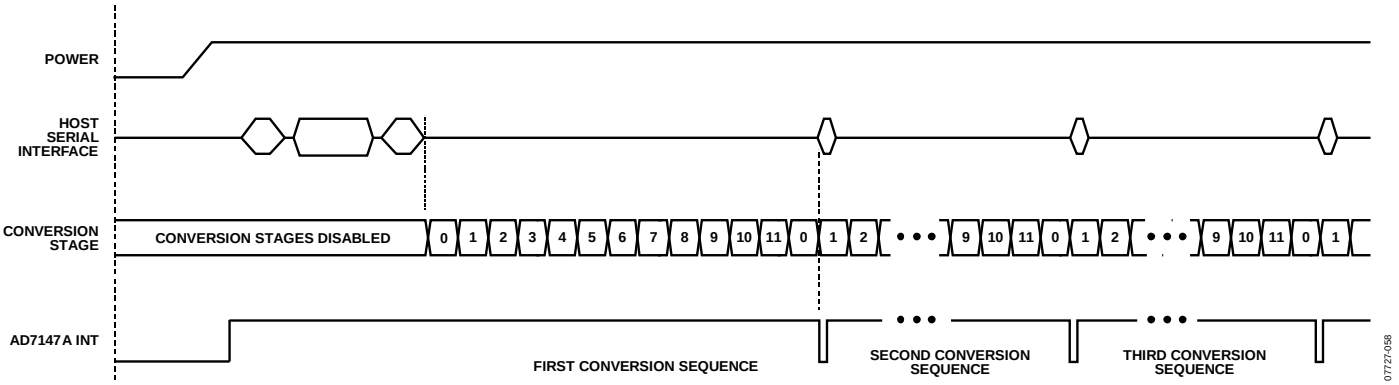



*Figure 58. Recommended Start-Up Sequence*

# TYPICAL APPLICATION CIRCUITS

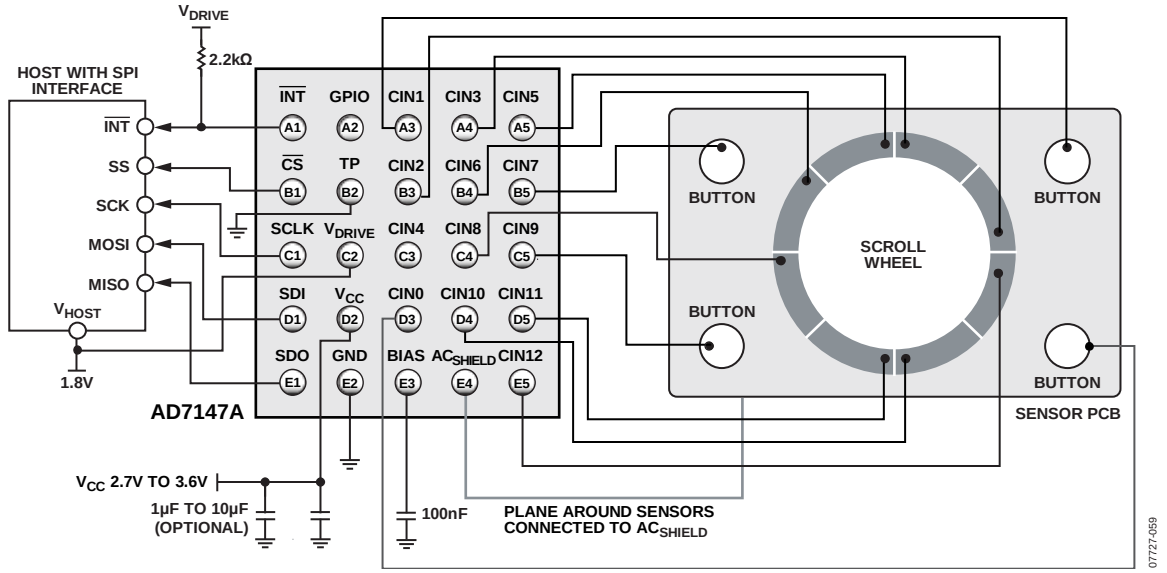



*Figure 59. Typical Application Circuit with SPI Interface*

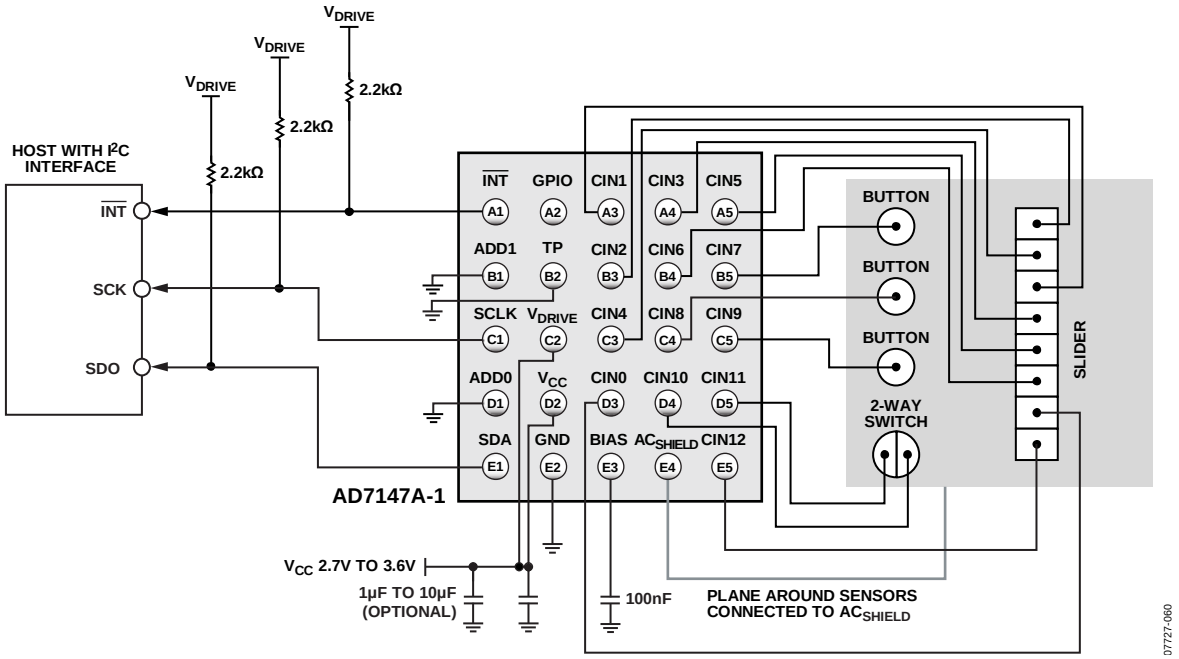



*Figure 60. Typical Application Circuit with I²C Interface*

# REGISTER MAP

The AD7147A address space is divided into three register banks, referred to as Bank 1, Bank 2, and Bank 3. Figure 61 illustrates the division of these banks.

Bank 1 registers contain control registers, CDC conversion control registers, interrupt enable registers, interrupt status registers, CDC 16-bit conversion data registers, device ID registers, and proximity status registers.

Bank 2 registers contain the configuration registers used to configure the individual CINx inputs for each conversion stage. Initialize the Bank 2 configuration registers immediately after power-up to obtain valid CDC conversion result data.

Bank 3 registers contain the results of each conversion stage. These registers automatically update at the end of each conversion sequence. Although these registers are primarily used by the AD7147A internal data processing, they are accessible by the host processor for additional external data processing, if desired.

Default values are undefined for Bank 2 registers and Bank 3 registers until after power-up and configuration of the Bank 2 registers.

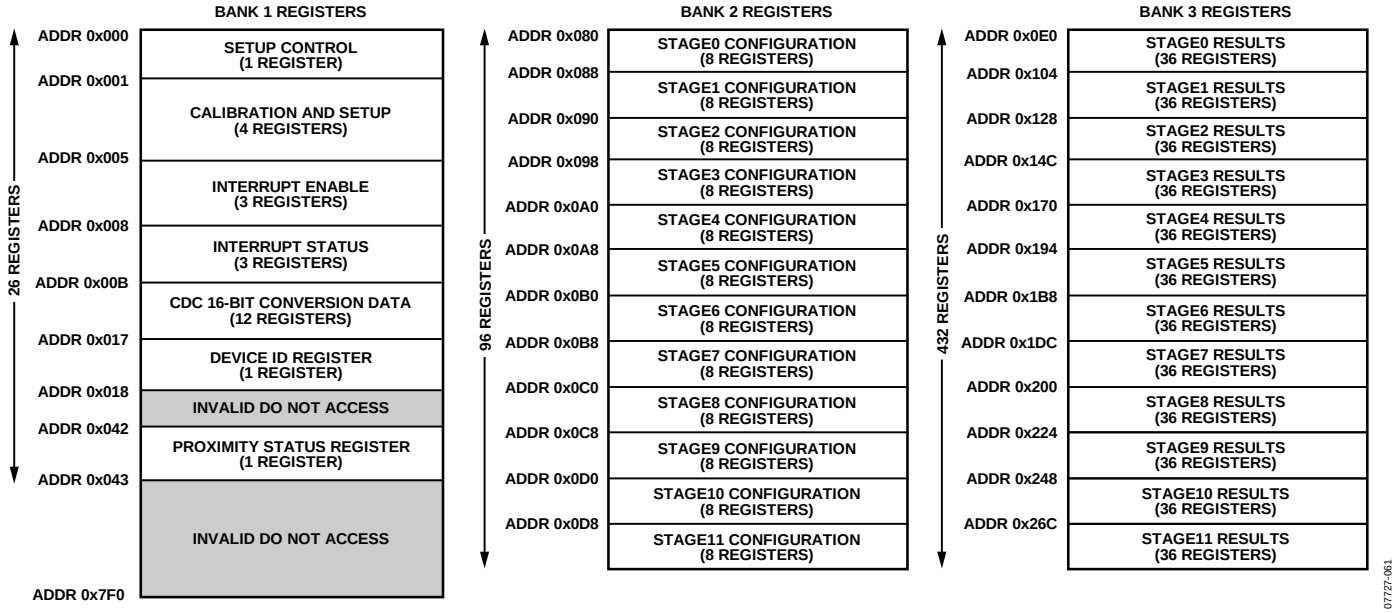



*Figure 61. Layout of Bank 1, Bank 2, and Bank 3 Registers*

# DETAILED REGISTER DESCRIPTIONS

## BANK 1 REGISTERS

All addresses and default values are expressed in hexadecimal.

**Table 21. PWR_CONTROL Register**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x000 | [1:0] | 0 | R/W | POWER_MODE | Operating modes<br>00 = full power mode (normal operation, CDC conversions approximately every 36 ms)<br>01 = full shutdown mode (no CDC conversions)<br>10 = low power mode (automatic wake-up operation)<br>11 = full shutdown mode (no CDC conversions) |
| | [3:2] | 0 | R/W | LP_CONV_DELAY | Low power mode conversion delay<br>00 = 200 ms<br>01 = 400 ms<br>10 = 600 ms<br>11 = 800 ms |
| | [7:4] | 0 | R/W | SEQUENCE_STAGE_NUM | Number of stages in sequence (N + 1)<br>0000 = 1 conversion stage in sequence<br>0001 = 2 conversion stages in sequence<br>…<br>Maximum value = 1011 = 12 conversion stages per sequence |
| | [9:8] | 0 | R/W | DECIMATION | ADC decimation factor<br>00 = decimate by 256<br>01 = decimate by 128<br>10 = decimate by 64<br>11 = decimate by 64 |
| | [10] | 0 | R/W | SW_RESET | Software reset control (self-clearing)<br>1 = resets all registers to default values |
| | [11] | 0 | R/W | INT_POL | Interrupt polarity control<br>0 = active low<br>1 = active high |
| | [12] | 0 | R/W | EXT_SOURCE | Excitation source control<br>0 = enable excitation source to CINx pins<br>1 = disable excitation source to CINx pins |
| | [13] | 0 | | Unused | Set to 0 |
| | [15:14] | 0 | R/W | CDC_BIAS | CDC bias current control<br>00 = normal operation<br>01 = normal operation + 20%<br>10 = normal operation + 35%<br>11 = normal operation + 50% |

**Table 22. STAGE_CAL_EN Register**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x001 | [0] | 0 | R/W | STAGE0_CAL_EN | STAGE0 calibration enable<br>0 = disable<br>1 = enable |
| | [1] | 0 | R/W | STAGE1_CAL_EN | STAGE1 calibration enable<br>0 = disable<br>1 = enable |
| | [2] | 0 | R/W | STAGE2_CAL_EN | STAGE2 calibration enable<br>0 = disable<br>1 = enable |
| | [3] | 0 | R/W | STAGE3_CAL_EN | STAGE3 calibration enable<br>0 = disable<br>1 = enable |
| | [4] | 0 | R/W | STAGE4_CAL_EN | STAGE4 calibration enable<br>0 = disable<br>1 = enable |
| | [5] | 0 | R/W | STAGE5_CAL_EN | STAGE5 calibration enable<br>0 = disable<br>1 = enable |
| | [6] | 0 | R/W | STAGE6_CAL_EN | STAGE6 calibration enable<br>0 = disable<br>1 = enable |
| | [7] | 0 | R/W | STAGE7_CAL_EN | STAGE7 calibration enable<br>0 = disable<br>1 = enable |
| | [8] | 0 | R/W | STAGE8_CAL_EN | STAGE8 calibration enable<br>0 = disable<br>1 = enable |
| | [9] | 0 | R/W | STAGE9_CAL_EN | STAGE9 calibration enable<br>0 = disable<br>1 = enable |
| | [10] | 0 | R/W | STAGE10_CAL_EN | STAGE10 calibration enable<br>0 = disable<br>1 = enable |
| | [11] | 0 | R/W | STAGE11_CAL_EN | STAGE11 calibration enable<br>0 = disable<br>1 = enable |
| | [13:12] | 0 | R/W | AVG_FP_SKIP | Full power mode skip control<br>00 = skip three samples<br>01 = skip seven samples<br>10 = skip 15 samples<br>11 = skip 31 samples |
| | [15:14] | 0 | R/W | AVG_LP_SKIP | Low power mode skip control<br>00 = use all samples<br>01 = skip one sample<br>10 = skip two samples<br>11 = skip three samples |

**Table 23. AMB_COMP_CTRL0 Register**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x002 | [3:0] | 0 | R/W | FF_SKIP_CNT | Fast filter skip control (N + 1)<br>0000 = no sequence of results is skipped<br>0001 = one sequence of results is skipped for every one allowed into fast FIFO<br>0010 = two sequences of results are skipped for every one allowed into fast FIFO<br>1011 = maximum value = 12 sequences of results are skipped for every one allowed into fast FIFO |
| | [7:4] | F | R/W | FP_PROXIMITY_CNT | Calibration disable period in full power mode = FP_PROXIMITY_CNT × 16 × time for one conversion sequence in full power mode |
| | [11:8] | F | R/W | LP_PROXIMITY_CNT | Calibration disable period in low power mode = LP_PROXIMITY_CNT × 4 × time for one conversion sequence in low power mode |
| | [13:12] | 0 | R/W | PWR_DOWN_TIMEOUT | Full power to low power mode timeout control<br>00 = 1.25 × (FP_PROXIMITY_CNT)<br>01 = 1.50 × (FP_PROXIMITY_CNT)<br>10 = 1.75 × (FP_PROXIMITY_CNT)<br>11 = 2.00 × (FP_PROXIMITY_CNT) |
| | [14] | 0 | R/W | FORCED_CAL | Forced calibration control<br>0 = normal operation<br>1 = forces all conversion stages to recalibrate |
| | [15] | 0 | R/W | CONV_RESET | Conversion reset control (self-clearing)<br>0 = normal operation<br>1 = resets the conversion sequence to STAGE0 |

**Table 24. AMB_COMP_CTRL1 Register**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x003 | [7:0] | 64 | R/W | PROXIMITY_RECAL_LVL | Proximity recalibration level. Value is multiplied by 16 to determine actual recalibration level. |
| | [13:8] | 1 | R/W | PROXIMITY_DETECTION_RATE | Proximity detection rate. Value is multiplied by 16 to determine actual detection rate. |
| | [15:14] | 0 | R/W | SLOW_FILTER_UPDATE_LVL | Slow filter update level. |

**Table 25. AMB_COMP_CTRL2 Register**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x004 | [9:0] | 3FF | R/W | FP_PROXIMITY_RECAL | Full power mode proximity recalibration time control |
| | [15:10] | 3F | R/W | LP_PROXIMITY_RECAL | Low power mode proximity recalibration time control |

**Table 26. STAGE_LOW_INT_ENABLE Register**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x005 | [0] | 0 | R/W | STAGE0_LOW_INT_ENABLE | STAGE0 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE0 low threshold is exceeded |
| | [1] | 0 | R/W | STAGE1_LOW_INT_ENABLE | STAGE1 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE1 low threshold is exceeded |
| | [2] | 0 | R/W | STAGE2_LOW_INT_ENABLE | STAGE2 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE2 low threshold is exceeded |
| | [3] | 0 | R/W | STAGE3_LOW_INT_ENABLE | STAGE3 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE3 low threshold is exceeded |
| | [4] | 0 | R/W | STAGE4_LOW_INT_ENABLE | STAGE4 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE4 low threshold is exceeded |
| | [5] | 0 | R/W | STAGE5_LOW_INT_ENABLE | STAGE5 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE5 low threshold is exceeded |
| | [6] | 0 | R/W | STAGE6_LOW_INT_ENABLE | STAGE6 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE6 low threshold is exceeded |
| | [7] | 0 | R/W | STAGE7_LOW_INT_ENABLE | STAGE7 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE7 low threshold is exceeded |
| | [8] | 0 | R/W | STAGE8_LOW_INT_ENABLE | STAGE8 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE8 low threshold is exceeded |
| | [9] | 0 | R/W | STAGE9_LOW_INT_ENABLE | STAGE9 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE9 low threshold is exceeded |
| | [10] | 0 | R/W | STAGE10_LOW_INT_ENABLE | STAGE10 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE10 low threshold is exceeded |
| | [11] | 0 | R/W | STAGE11_LOW_INT_ENABLE | STAGE11 low interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted if STAGE11 low threshold is exceeded |
| | [13:12] | 0 | R/W | GPIO_SETUP | GPIO setup<br>00 = disable GPIO pin<br>01 = configure GPIO as an input<br>10 = configure GPIO as an active low output<br>11 = configure GPIO as an active high output |
| | [15:14] | 0 | R/W | GPIO_INPUT_CONFIG | GPIO input configuration<br>00 = triggered on negative level<br>01 = triggered on positive edge<br>10 = triggered on negative edge<br>11 = triggered on positive level |

**Table 27. STAGE_HIGH_INT_ENABLE Register**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x006 | [0] | 0 | R/W | STAGE0_HIGH_INT_ENABLE | STAGE0 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE0 high threshold is exceeded |
| | [1] | 0 | R/W | STAGE1_HIGH_INT_ENABLE | STAGE1 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE1 high threshold is exceeded |
| | [2] | 0 | R/W | STAGE2_HIGH_INT_ENABLE | STAGE2 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE2 high threshold is exceeded |
| | [3] | 0 | R/W | STAGE3_HIGH_INT_ENABLE | STAGE3 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE3 high threshold is exceeded |
| | [4] | 0 | R/W | STAGE4_HIGH_INT_ENABLE | STAGE4 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE4 high threshold is exceeded |
| | [5] | 0 | R/W | STAGE5_HIGH_INT_ENABLE | STAGE5 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE5 high threshold is exceeded |
| | [6] | 0 | R/W | STAGE6_HIGH_INT_ENABLE | STAGE6 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE6 high threshold is exceeded |
| | [7] | 0 | R/W | STAGE7_HIGH_INT_ENABLE | STAGE7 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE7 high threshold is exceeded |
| | [8] | 0 | R/W | STAGE8_HIGH_INT_ENABLE | STAGE8 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE8 high threshold is exceeded |
| | [9] | 0 | R/W | STAGE9_HIGH_INT_ENABLE | STAGE9 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE9 high threshold is exceeded |
| | [10] | 0 | R/W | STAGE10_HIGH_INT_ENABLE | STAGE10 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE10 high threshold is exceeded |
| | [11] | 0 | R/W | STAGE11_HIGH_INT_ENABLE | STAGE11 high interrupt enable<br>0 = interrupt source disabled<br>1 = $\overline{\text{INT}}$ asserted if STAGE11 high threshold is exceeded |
| | [15:12] | | | Unused | Set to 0 |

**Table 28. STAGE_COMPLETE_INT_ENABLE Register**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x007 | [0] | 0 | R/W | STAGE0_COMPLETE_INT_ENABLE | STAGE0 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE0 conversion |
| | [1] | 0 | R/W | STAGE1_COMPLETE_INT_ENABLE | STAGE1 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE1 conversion |
| | [2] | 0 | R/W | STAGE2_COMPLETE_INT_ENABLE | STAGE2 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE2 conversion |
| | [3] | 0 | R/W | STAGE3_COMPLETE_INT_ENABLE | STAGE3 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE3 conversion |
| | [4] | 0 | R/W | STAGE4_COMPLETE_INT_ENABLE | STAGE4 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE4 conversion |
| | [5] | 0 | R/W | STAGE5_COMPLETE_INT_ENABLE | STAGE5 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE5 conversion |
| | [6] | 0 | R/W | STAGE6_COMPLETE_INT_ENABLE | STAGE6 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE6 conversion |
| | [7] | 0 | R/W | STAGE7_COMPLETE_INT_ENABLE | STAGE7 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE7 conversion |
| | [8] | 0 | R/W | STAGE8_COMPLETE_INT_ENABLE | STAGE8 conversion complete interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE8 conversion |
| | [9] | 0 | R/W | STAGE9_COMPLETE_INT_ENABLE | STAGE9 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE9 conversion |
| | [10] | 0 | R/W | STAGE10_COMPLETE_INT_ENABLE | STAGE10 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE10 conversion |
| | [11] | 0 | R/W | STAGE11_COMPLETE_INT_ENABLE | STAGE11 conversion interrupt control<br>0 = interrupt source disabled<br>1 = $\overline{INT}$ asserted at completion of STAGE11 conversion |
| | [12] | 0 | R/W | GPIO_INT_ENABLE | Interrupt control when GPIO input pin changes level<br>0 = disabled<br>1 = enabled |
| | [15:13] | | | Unused | Set to 0 |

**Table 29. STAGE_LOW_INT_STATUS Register[1]**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x008 | [0] | 0 | R | STAGE0_LOW_INT_STATUS | STAGE0 CDC conversion low limit interrupt result<br>1 = indicates STAGE0_LOW_THRESHOLD value was exceeded |
| | [1] | 0 | R | STAGE1_LOW_INT_STATUS | STAGE1 CDC conversion low limit interrupt result<br>1 = indicates STAGE1_LOW_THRESHOLD value was exceeded |
| | [2] | 0 | R | STAGE2_LOW_INT_STATUS | STAGE2 CDC conversion low limit interrupt result<br>1 = indicates STAGE2_LOW_THRESHOLD value was exceeded |
| | [3] | 0 | R | STAGE3_LOW_INT_STATUS | STAGE3 CDC conversion low limit interrupt result<br>1 = indicates STAGE3_LOW_THRESHOLD value was exceeded |
| | [4] | 0 | R | STAGE4_LOW_INT_STATUS | STAGE4 CDC conversion low limit interrupt result<br>1 = indicates STAGE4_LOW_THRESHOLD value was exceeded |
| | [5] | 0 | R | STAGE5_LOW_INT_STATUS | STAGE5 CDC conversion low limit interrupt result<br>1 = indicates STAGE5_LOW_THRESHOLD value was exceeded |
| | [6] | 0 | R | STAGE6_LOW_INT_STATUS | STAGE6 CDC conversion low limit interrupt result<br>1 = indicates STAGE6_LOW_THRESHOLD value was exceeded |
| | [7] | 0 | R | STAGE7_LOW_INT_STATUS | STAGE7 CDC conversion low limit interrupt result<br>1 = indicates STAGE7_LOW_THRESHOLD value was exceeded |
| | [8] | 0 | R | STAGE8_LOW_INT_STATUS | STAGE8 CDC conversion low limit interrupt result<br>1 = indicates STAGE8_LOW_THRESHOLD value was exceeded |
| | [9] | 0 | R | STAGE9_LOW_INT_STATUS | STAGE9 CDC conversion low limit interrupt result<br>1 = indicates STAGE9_LOW_THRESHOLD value was exceeded |
| | [10] | 0 | R | STAGE10_LOW_INT_STATUS | STAGE10 CDC conversion low limit interrupt result<br>1 = indicates STAGE10_LOW_THRESHOLD value was exceeded |
| | [11] | 0 | R | STAGE11_LOW_INT_STATUS | STAGE11 CDC conversion low limit interrupt result<br>1 = indicates STAGE11_LOW_THRESHOLD value was exceeded |
| | [15:12] | | | Unused | Set to 0 |

[1] Registers self-clear to 0 after readback if the limits are not exceeded.

**Table 30. STAGE_HIGH_INT_STATUS Register[1]**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x009 | [0] | 0 | R | STAGE0_HIGH_INT_STATUS | STAGE0 CDC conversion high limit interrupt result<br>1 = indicates STAGE0_HIGH_THRESHOLD value was exceeded |
| | [1] | 0 | R | STAGE1_HIGH_INT_STATUS | STAGE1 CDC conversion high limit interrupt result<br>1 = indicates STAGE1_HIGH_THRESHOLD value was exceeded |
| | [2] | 0 | R | STAGE2_HIGH_INT_STATUS | STAGE2 CDC conversion high limit interrupt result<br>1 = indicates STAGE2_HIGH_THRESHOLD value was exceeded |
| | [3] | 0 | R | STAGE3_HIGH_INT_STATUS | STAGE3 CDC conversion high limit interrupt result<br>1 = indicates STAGE3_HIGH_THRESHOLD value was exceeded |
| | [4] | 0 | R | STAGE4_HIGH_INT_STATUS | STAGE4 CDC conversion high limit interrupt result<br>1 = indicates STAGE4_HIGH_THRESHOLD value was exceeded |
| | [5] | 0 | R | STAGE5_HIGH_INT_STATUS | STAGE5 CDC conversion high limit interrupt result<br>1 = indicates STAGE5_HIGH_THRESHOLD value was exceeded |
| | [6] | 0 | R | STAGE6_HIGH_INT_STATUS | STAGE6 CDC conversion high limit interrupt result<br>1 = indicates STAGE6_HIGH_THRESHOLD value was exceeded |
| | [7] | 0 | R | STAGE7_HIGH_INT_STATUS | STAGE7 CDC conversion high limit interrupt result<br>1 = indicates STAGE7_HIGH_THRESHOLD value was exceeded |
| | [8] | 0 | R | STAGE8_HIGH_INT_STATUS | STAGE8 CDC conversion high limit interrupt result<br>1 = indicates STAGE8_HIGH_THRESHOLD value was exceeded |
| | [9] | 0 | R | STAGE9_HIGH_INT_STATUS | STAGE9 CDC conversion high limit interrupt result<br>1 = indicates STAGE9_HIGH_THRESHOLD value was exceeded |
| | [10] | 0 | R | STAGE10_HIGH_INT_STATUS | STAGE10 CDC conversion high limit interrupt result<br>1 = indicates STAGE10_HIGH_THRESHOLD value was exceeded |
| | [11] | 0 | R | STAGE11_HIGH_INT_STATUS | STAGE11 CDC conversion high limit interrupt result<br>1 = indicates STAGE11_HIGH_THRESHOLD value was exceeded |
| | [15:12] | | | Unused | Set to 0 |

[1] Registers self-clear to 0 after readback if the limits are not exceeded.

**Table 31. STAGE_COMPLETE_INT_STATUS Register[1]**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x00A | [0] | 0 | R | STAGE0_COMPLETE_INT_STATUS | STAGE0 conversion-complete register interrupt status<br>1 = indicates STAGE0 conversion completed |
| | [1] | 0 | R | STAGE1_COMPLETE_INT_STATUS | STAGE1 conversion-complete register interrupt status<br>1 = indicates STAGE1 conversion completed |
| | [2] | 0 | R | STAGE2_COMPLETE_INT_STATUS | STAGE2 conversion-complete register interrupt status<br>1 = indicates STAGE2 conversion completed |
| | [3] | 0 | R | STAGE3_COMPLETE_INT_STATUS | STAGE3 conversion-complete register interrupt status<br>1 = indicates STAGE3 conversion completed |
| | [4] | 0 | R | STAGE4_COMPLETE_INT_STATUS | STAGE4 conversion-complete register interrupt status<br>1 = indicates STAGE4 conversion completed |
| | [5] | 0 | R | STAGE5_COMPLETE_INT_STATUS | STAGE5 conversion-complete register interrupt status<br>1 = indicates STAGE5 conversion completed |
| | [6] | 0 | R | STAGE6_COMPLETE_INT_STATUS | STAGE6 conversion-complete register interrupt status<br>1 = indicates STAGE6 conversion completed |
| | [7] | 0 | R | STAGE7_COMPLETE_INT_STATUS | STAGE7 conversion-complete register interrupt status<br>1 = indicates STAGE7 conversion completed |
| | [8] | 0 | R | STAGE8_COMPLETE_INT_STATUS | STAGE8 conversion-complete register interrupt status<br>1 = indicates STAGE8 conversion completed |
| | [9] | 0 | R | STAGE9_COMPLETE_INT_STATUS | STAGE9 conversion-complete register interrupt status<br>1 = indicates STAGE9 conversion completed |
| | [10] | 0 | R | STAGE10_COMPLETE_INT_STATUS | STAGE10 conversion-complete register interrupt status<br>1 = indicates STAGE10 conversion completed |
| | [11] | 0 | R | STAGE11_COMPLETE_INT_STATUS | STAGE11 conversion-complete register interrupt status<br>1 = indicates STAGE11 conversion completed |
| | [12] | 0 | R | GPIO_INT_STATUS | GPIO input pin status<br>1 = indicates level on GPIO pin has changed |
| | [15:13] | | | Unused | Set to 0 |

[1] Registers self-clear to 0 after readback if the limits are not exceeded.

**Table 32. CDC 16-Bit Conversion Data Registers**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x00B | [15:0] | 0 | R | CDC_RESULT_S0 | STAGE0 CDC 16-bit conversion data |
| 0x00C | [15:0] | 0 | R | CDC_RESULT_S1 | STAGE1 CDC 16-bit conversion data |
| 0x00D | [15:0] | 0 | R | CDC_RESULT_S2 | STAGE2 CDC 16-bit conversion data |
| 0x00E | [15:0] | 0 | R | CDC_RESULT_S3 | STAGE3 CDC 16-bit conversion data |
| 0x00F | [15:0] | 0 | R | CDC_RESULT_S4 | STAGE4 CDC 16-bit conversion data |
| 0x010 | [15:0] | 0 | R | CDC_RESULT_S5 | STAGE5 CDC 16-bit conversion data |
| 0x011 | [15:0] | 0 | R | CDC_RESULT_S6 | STAGE6 CDC 16-bit conversion data |
| 0x012 | [15:0] | 0 | R | CDC_RESULT_S7 | STAGE7 CDC 16-bit conversion data |
| 0x013 | [15:0] | 0 | R | CDC_RESULT_S8 | STAGE8 CDC 16-bit conversion data |
| 0x014 | [15:0] | 0 | R | CDC_RESULT_S9 | STAGE9 CDC 16-bit conversion data |
| 0x015 | [15:0] | 0 | R | CDC_RESULT_S10 | STAGE10 CDC 16-bit conversion data |
| 0x016 | [15:0] | 0 | R | CDC_RESULT_S11 | STAGE11 CDC 16-bit conversion data |

**Table 33. Device ID Register**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x017 | [3:0] | 0 | R | REVISION_CODE | Revision code |
| | [15:4] | 147 | R | DEVID | Device ID = 0001 0100 0111 |

**Table 34. Proximity Status Register**

| Address | Data Bit | Default Value | Type | Name | Description |
|---|---|---|---|---|---|
| 0x042 | [0] | 0 | R | STAGE0_PROXIMITY_STATUS | STAGE0 proximity status register<br>1 = indicates proximity has been detected on STAGE0 |
| | [1] | 0 | R | STAGE1_PROXIMITY_STATUS | STAGE1 proximity status register<br>1 = indicates proximity has been detected on STAGE1 |
| | [2] | 0 | R | STAGE2_PROXIMITY_STATUS | STAGE2 proximity status register<br>1 = indicates proximity has been detected on STAGE2 |
| | [3] | 0 | R | STAGE3_PROXIMITY_STATUS | STAGE3 proximity status register<br>1 = indicates proximity has been detected on STAGE3 |
| | [4] | 0 | R | STAGE4_PROXIMITY_STATUS | STAGE4 proximity status register<br>1 = indicates proximity has been detected on STAGE4 |
| | [5] | 0 | R | STAGE5_PROXIMITY_STATUS | STAGE5 proximity status register<br>1 = indicates proximity has been detected on STAGE5 |
| | [6] | 0 | R | STAGE6_PROXIMITY_STATUS | STAGE6 proximity status register<br>1 = indicates proximity has been detected on STAGE6 |
| | [7] | 0 | R | STAGE7_PROXIMITY_STATUS | STAGE7 proximity status register<br>1 = indicates proximity has been detected on STAGE7 |
| | [8] | 0 | R | STAGE8_PROXIMITY_STATUS | STAGE8 proximity status register<br>1 = indicates proximity has been detected on STAGE8 |
| | [9] | 0 | R | STAGE9_PROXIMITY_STATUS | STAGE9 proximity status register<br>1 = indicates proximity has been detected on STAGE9 |
| | [10] | 0 | R | STAGE10_PROXIMITY_STATUS | STAGE10 proximity status register<br>1 = indicates proximity has been detected on STAGE10 |
| | [11] | 0 | R | STAGE11_PROXIMITY_STATUS | STAGE11 proximity status register<br>1 = indicates proximity has been detected on STAGE11 |
| | [15:12] | | | Unused | Set to 0 |

## BANK 2 REGISTERS

All address values are expressed in hexadecimal.

**Table 35. STAGEx_CONNECTION[6:0] Register Description (x = 0 to 11)**

| Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|
| [1:0] | X | R/W | CIN0_CONNECTION_SETUP | CIN0 connection setup<br>00 = CIN0 not connected to CDC inputs<br>01 = CIN0 connected to CDC negative input<br>10 = CIN0 connected to CDC positive input<br>11 = CIN0 connected to BIAS (connect unused CINx inputs) |
| [3:2] | X | R/W | CIN1_CONNECTION_SETUP | CIN1 connection setup<br>00 = CIN1 not connected to CDC inputs<br>01 = CIN1 connected to CDC negative input<br>10 = CIN1 connected to CDC positive input<br>11 = CIN1 connected to BIAS (connect unused CINx inputs) |
| [5:4] | X | R/W | CIN2_CONNECTION_SETUP | CIN2 connection setup<br>00 = CIN2 not connected to CDC inputs<br>01 = CIN2 connected to CDC negative input<br>10 = CIN2 connected to CDC positive input<br>11 = CIN2 connected to BIAS (connect unused CINx inputs) |
| [7:6] | X | R/W | CIN3_CONNECTION_SETUP | CIN3 connection setup<br>00 = CIN3 not connected to CDC inputs<br>01 = CIN3 connected to CDC negative input<br>10 = CIN3 connected to CDC positive input<br>11 = CIN3 connected to BIAS (connect unused CINx inputs) |
| [9:8] | X | R/W | CIN4_CONNECTION_SETUP | CIN4 connection setup<br>00 = CIN4 not connected to CDC inputs<br>01 = CIN4 connected to CDC negative input<br>10 = CIN4 connected to CDC positive input<br>11 = CIN4 connected to BIAS (connect unused CINx inputs) |
| [11:10] | X | R/W | CIN5_CONNECTION_SETUP | CIN5 connection setup<br>00 = CIN5 not connected to CDC inputs<br>01 = CIN5 connected to CDC negative input<br>10 = CIN5 connected to CDC positive input<br>11 = CIN5 connected to BIAS (connect unused CINx inputs) |
| [13:12] | X | R/W | CIN6_CONNECTION_SETUP | CIN6 connection setup<br>00 = CIN6 not connected to CDC inputs<br>01 = CIN6 connected to CDC negative input<br>10 = CIN6 connected to CDC positive input<br>11 = CIN6 connected to BIAS (connect unused CINx inputs) |
| [15:14] | X | | Unused | Set to 0 |

[1] X = don't care.

**Table 36. STAGEx_CONNECTION[12:7] Register Description (x = 0 to 11)**

| Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|
| [1:0] | X | R/W | CIN7_CONNECTION_SETUP | CIN7 connection setup<br>00 = CIN7 not connected to CDC inputs<br>01 = CIN7 connected to CDC negative input<br>10 = CIN7 connected to CDC positive input<br>11 = CIN7 connected to BIAS (connect unused CINx inputs) |
| [3:2] | X | R/W | CIN8_CONNECTION_SETUP | CIN8 connection setup<br>00 = CIN8 not connected to CDC inputs<br>01 = CIN8 connected to CDC negative input<br>10 = CIN8 connected to CDC positive input<br>11 = CIN8 connected to BIAS (connect unused CINx inputs) |
| [5:4] | X | R/W | CIN9_CONNECTION_SETUP | CIN9 connection setup<br>00 = CIN9 not connected to CDC inputs<br>01 = CIN9 connected to CDC negative input<br>10 = CIN9 connected to CDC positive input<br>11 = CIN9 connected to BIAS (connect unused CINx inputs) |
| [7:6] | X | R/W | CIN10_CONNECTION_SETUP | CIN10 connection setup<br>00 = CIN10 not connected to CDC inputs<br>01 = CIN10 connected to CDC negative input<br>10 = CIN10 connected to CDC positive input<br>11 = CIN10 connected to BIAS (connect unused CINx inputs) |
| [9:8] | X | R/W | CIN11_CONNECTION_SETUP | CIN11 connection setup<br>00 = CIN11 not connected to CDC inputs<br>01 = CIN11 connected to CDC negative input<br>10 = CIN11 connected to CDC positive input<br>11 = CIN11 connected to BIAS (connect unused CINx inputs) |
| [11:10] | X | R/W | CIN12_CONNECTION_SETUP | CIN12 connection setup<br>00 = CIN12 not connected to CDC inputs<br>01 = CIN12 connected to CDC negative input<br>10 = CIN12 connected to CDC positive input<br>11 = CIN12 connected to BIAS (connect unused CINx inputs) |
| [13:12] | X | R/W | SE_CONNECTION_SETUP | Single-ended measurement connection setup<br>00 = Do not use<br>01 = Use when one CINx is connected to CDC positive input, single-ended measurements only<br>10 = Use when one CINx is connected to CDC negative input, single-ended measurements only<br>11 = Differential connection to CDC |
| [14] | X | R/W | NEG_AFE_OFFSET_DISABLE | Negative AFE offset enable control<br>0 = enable<br>1 = disable |
| [15] | X | R/W | POS_AFE_OFFSET_DISABLE | Positive AFE offset enable control<br>0 = enable<br>1 = disable |

[1] X = don't care.

**Table 37. STAGEx_AFE_OFFSET Register Description (x = 0 to 11)**

| Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|
| [5:0] | X | R/W | NEG_AFE_OFFSET | Negative AFE offset setting (20 pF range)<br>1 LSB value = 0.32 pF of offset |
| [6] | X | | Unused | Set to 0 |
| [7] | X | R/W | NEG_AFE_OFFSET_SWAP | Negative AFE offset swap control<br>0 = NEG_AFE_OFFSET applied to CDC negative input<br>1 = NEG_AFE_OFFSET applied to CDC positive input |
| [13:8] | X | R/W | POS_AFE_OFFSET | Positive AFE offset setting (20 pF range)<br>1 LSB value = 0.32 pF of offset |
| [14] | X | | Unused | Set to 0 |
| [15] | X | R/W | POS_AFE_OFFSET_SWAP | Positive AFE offset swap control<br>0 = POS_AFE_OFFSET applied to CDC positive input<br>1 = POS_AFE_OFFSET applied to CDC negative input |

[1] X = don't care.

**Table 38. STAGEx_SENSITIVITY Register Description (x = 0 to 11)**

| Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|
| [3:0] | X | R/W | NEG_THRESHOLD_SENSITIVITY | Negative threshold sensitivity control<br>0000 = 25%, 0001 = 29.73%, 0010 = 34.40%, 0011 = 39.08%<br>0100 = 43.79%, 0101 = 48.47%, 0110 = 53.15%<br>0111 = 57.83%, 1000 = 62.51%, 1001 = 67.22%<br>1010 = 71.90%, 1011 = 76.58%, 1100 = 81.28%<br>1101 = 85.96%, 1110 = 90.64%, 1111 = 95.32% |
| [6:4] | X | R/W | NEG_PEAK_DETECT | Negative peak detect setting<br>000 = 40% level, 001 = 50% level, 010 = 60% level<br>011 = 70% level, 100 = 80% level, 101 = 90% level |
| [7] | X | R/W | Unused | Set to 0 |
| [11:8] | X | R/W | POS_THRESHOLD_SENSITIVITY | Positive threshold sensitivity control<br>0000 = 25%, 0001 = 29.73%, 0010 = 34.40%, 0011 = 39.08%<br>0100 = 43.79%, 0101 = 48.47%, 0110 = 53.15%<br>0111 = 57.83%, 1000 = 62.51%, 1001 = 67.22%<br>1010 = 71.90%, 1011 = 76.58%, 1100 = 81.28%<br>1101 = 85.96%, 1110 = 90.64%, 1111 = 95.32% |
| [14:12] | X | R/W | POS_PEAK_DETECT | Positive peak detect setting<br>000 = 40% level, 001 = 50% level, 010 = 60% level<br>011 = 70% level, 100 = 80% level, 101 = 90% level |
| [15] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 39. STAGE0 to STAGE12 Configuration Registers**

| Address | Data Bit | Default[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x080 | [15:0] | X | R/W | STAGE0_CONNECTION[6:0] | STAGE0 CIN[6:0] connection setup (see Table 35) |
| 0x081 | [15:0] | X | R/W | STAGE0_CONNECTION[12:7] | STAGE0 CIN[12:7] connection setup (see Table 36) |
| 0x082 | [15:0] | X | R/W | STAGE0_AFE_OFFSET | STAGE0 AFE offset control (see Table 37) |
| 0x083 | [15:0] | X | R/W | STAGE0_SENSITIVITY | STAGE0 sensitivity control (see Table 38) |
| 0x084 | [15:0] | X | R/W | STAGE0_OFFSET_LOW | STAGE0 initial offset low value |
| 0x085 | [15:0] | X | R/W | STAGE0_OFFSET_HIGH | STAGE0 initial offset high value |
| 0x086 | [15:0] | X | R/W | STAGE0_OFFSET_HIGH_CLAMP | STAGE0 offset high clamp value |
| 0x087 | [15:0] | X | R/W | STAGE0_ OFFSET_LOW_CLAMP | STAGE0 offset low clamp value |
| 0x088 | [15:0] | X | R/W | STAGE1_CONNECTION[6:0] | STAGE1 CIN[6:0] connection setup (see Table 35) |
| 0x089 | [15:0] | X | R/W | STAGE1_CONNECTION[12:7] | STAGE1 CIN[12:7] connection setup (see Table 36) |
| 0x08A | [15:0] | X | R/W | STAGE1_AFE_OFFSET | STAGE1 AFE offset control (see Table 37) |
| 0x08B | [15:0] | X | R/W | STAGE1_SENSITIVITY | STAGE1 sensitivity control (see Table 38) |
| 0x08C | [15:0] | X | R/W | STAGE1_OFFSET_LOW | STAGE1 initial offset low value |
| 0x08D | [15:0] | X | R/W | STAGE1_OFFSET_HIGH | STAGE1 initial offset high value |
| 0x08E | [15:0] | X | R/W | STAGE1_OFFSET_HIGH_CLAMP | STAGE1 offset high clamp value |
| 0x08F | [15:0] | X | R/W | STAGE1_OFFSET_LOW_CLAMP | STAGE1 offset low clamp value |
| 0x090 | [15:0] | X | R/W | STAGE2_CONNECTION[6:0] | STAGE2 CIN[6:0] connection setup (see Table 35) |
| 0x091 | [15:0] | X | R/W | STAGE2_CONNECTION[12:7] | STAGE2 CIN[12:7] connection setup (see Table 36) |
| 0x092 | [15:0] | X | R/W | STAGE2_AFE_OFFSET | STAGE2 AFE offset control (see Table 37) |
| 0x093 | [15:0] | X | R/W | STAGE2_SENSITIVITY | STAGE2 sensitivity control (see Table 38) |
| 0x094 | [15:0] | X | R/W | STAGE2_OFFSET_LOW | STAGE2 initial offset low value |
| 0x095 | [15:0] | X | R/W | STAGE2_OFFSET_HIGH | STAGE2 initial offset high value |
| 0x096 | [15:0] | X | R/W | STAGE2_OFFSET_HIGH_CLAMP | STAGE2 offset high clamp value |
| 0x097 | [15:0] | X | R/W | STAGE2_OFFSET_LOW_CLAMP | STAGE2 offset low clamp value |
| 0x098 | [15:0] | X | R/W | STAGE3_CONNECTION[6:0] | STAGE3 CIN[6:0] connection setup (see Table 35) |
| 0x099 | [15:0] | X | R/W | STAGE3_CONNECTION[12:7] | STAGE3 CIN[12:7] connection setup (see Table 36) |
| 0x09A | [15:0] | X | R/W | STAGE3_AFE_OFFSET | STAGE3 AFE offset control (see Table 37) |
| 0x09B | [15:0] | X | R/W | STAGE3_SENSITIVITY | STAGE3 sensitivity control (see Table 38) |
| 0x09C | [15:0] | X | R/W | STAGE3_OFFSET_LOW | STAGE3 initial offset low value |
| 0x09D | [15:0] | X | R/W | STAGE3_OFFSET_HIGH | STAGE3 initial offset high value |
| 0x09E | [15:0] | X | R/W | STAGE3_OFFSET_HIGH_CLAMP | STAGE3 offset high clamp value |
| 0x09F | [15:0] | X | R/W | STAGE3_OFFSET_LOW_CLAMP | STAGE3 offset low clamp value |
| 0x0A0 | [15:0] | X | R/W | STAGE4_CONNECTION[6:0] | STAGE4 CIN[6:0] connection setup (see Table 35) |
| 0x0A1 | [15:0] | X | R/W | STAGE4_CONNECTION[12:7] | STAGE4 CIN[12:7] connection setup (see Table 36) |
| 0x0A2 | [15:0] | X | R/W | STAGE4_AFE_OFFSET | STAGE4 AFE offset control (see Table 37) |
| 0x0A3 | [15:0] | X | R/W | STAGE4_SENSITIVITY | STAGE4 sensitivity control (see Table 38) |
| 0x0A4 | [15:0] | X | R/W | STAGE4_OFFSET_LOW | STAGE4 initial offset low value |
| 0x0A5 | [15:0] | X | R/W | STAGE4_OFFSET_HIGH | STAGE4 initial offset high value |
| 0x0A6 | [15:0] | X | R/W | STAGE4_OFFSET_HIGH_CLAMP | STAGE4 offset high clamp value |
| 0x0A7 | [15:0] | X | R/W | STAGE4_OFFSET_LOW_CLAMP | STAGE4 offset low clamp value |
| 0x0A8 | [15:0] | X | R/W | STAGE5_CONNECTION[6:0] | STAGE5 CIN[6:0] connection setup (see Table 35) |
| 0x0A9 | [15:0] | X | R/W | STAGE5_CONNECTION[12:7] | STAGE5 CIN[12:7] connection setup (see Table 36) |
| 0x0AA | [15:0] | X | R/W | STAGE5_AFE_OFFSET | STAGE5 AFE offset control (see Table 37) |
| 0x0AB | [15:0] | X | R/W | STAGE5_SENSITIVITY | STAGE5 sensitivity control (see Table 38) |
| 0x0AC | [15:0] | X | R/W | STAGE5_OFFSET_LOW | STAGE5 initial offset low value |
| 0x0AD | [15:0] | X | R/W | STAGE5_OFFSET_HIGH | STAGE5 initial offset high value |
| 0x0AE | [15:0] | X | R/W | STAGE5_OFFSET_HIGH_CLAMP | STAGE5 offset high clamp value |
| 0x0AF | [15:0] | X | R/W | STAGE5_OFFSET_LOW_CLAMP | STAGE5 offset low clamp value |

| Address | Data Bit | Default[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x0B0 | [15:0] | X | R/W | STAGE6_CONNECTION[6:0] | STAGE6 CIN[6:0] connection setup (see Table 35) |
| 0x0B1 | [15:0] | X | R/W | STAGE6_CONNECTION[12:7] | STAGE6 CIN[12:7] connection setup (see Table 36) |
| 0x0B2 | [15:0] | X | R/W | STAGE6_AFE_OFFSET | STAGE6 AFE offset control (see Table 37) |
| 0x0B3 | [15:0] | X | R/W | STAGE6_SENSITIVITY | STAGE6 sensitivity control (see Table 38) |
| 0x0B4 | [15:0] | X | R/W | STAGE6_OFFSET_LOW | STAGE6 initial offset low value |
| 0x0B5 | [15:0] | X | R/W | STAGE6_OFFSET_HIGH | STAGE6 initial offset high value |
| 0x0B6 | [15:0] | X | R/W | STAGE6_OFFSET_HIGH_CLAMP | STAGE6 offset high clamp value |
| 0x0B7 | [15:0] | X | R/W | STAGE6_OFFSET_LOW_CLAMP | STAGE6 offset low clamp value |
| 0x0B8 | [15:0] | X | R/W | STAGE7_CONNECTION[6:0] | STAGE7 CIN[6:0] connection setup (see Table 35) |
| 0x0B9 | [15:0] | X | R/W | STAGE7_CONNECTION[12:7] | STAGE7 CIN[12:7] connection setup (see Table 36) |
| 0x0BA | [15:0] | X | R/W | STAGE7_AFE_OFFSET | STAGE7 AFE offset control (see Table 37) |
| 0x0BB | [15:0] | X | R/W | STAGE7_SENSITIVITY | STAGE7 sensitivity control (see Table 38) |
| 0x0BC | [15:0] | X | R/W | STAGE7_OFFSET_LOW | STAGE7 initial offset low value |
| 0x0BD | [15:0] | X | R/W | STAGE7_OFFSET_HIGH | STAGE7 initial offset high value |
| 0x0BE | [15:0] | X | R/W | STAGE7_OFFSET_HIGH_CLAMP | STAGE7 offset high clamp value |
| 0x0BF | [15:0] | X | R/W | STAGE7_OFFSET_LOW_CLAMP | STAGE7 offset low clamp value |
| 0x0C0 | [15:0] | X | R/W | STAGE8_CONNECTION[6:0] | STAGE8 CIN[6:0] connection setup (see Table 35) |
| 0x0C1 | [15:0] | X | R/W | STAGE8_CONNECTION[12:7] | STAGE8 CIN[12:7] connection setup (see Table 36) |
| 0x0C2 | [15:0] | X | R/W | STAGE8_AFE_OFFSET | STAGE8 AFE offset control (see Table 37) |
| 0x0C3 | [15:0] | X | R/W | STAGE8_SENSITIVITY | STAGE8 sensitivity control (see Table 38) |
| 0x0C4 | [15:0] | X | R/W | STAGE8_OFFSET_LOW | STAGE8 initial offset low value |
| 0x0C5 | [15:0] | X | R/W | STAGE8_OFFSET_HIGH | STAGE8 initial offset high value |
| 0x0C6 | [15:0] | X | R/W | STAGE8_OFFSET_HIGH_CLAMP | STAGE8 offset high clamp value |
| 0x0C7 | [15:0] | X | R/W | STAGE8_OFFSET_LOW_CLAMP | STAGE8 offset low clamp value |
| 0x0C8 | [15:0] | X | R/W | STAGE9_CONNECTION[6:0] | STAGE9 CIN[6:0] connection setup (see Table 35) |
| 0x0C9 | [15:0] | X | R/W | STAGE9_CONNECTION[12:7] | STAGE9 CIN[12:7] connection setup (see Table 36) |
| 0x0CA | [15:0] | X | R/W | STAGE9_AFE_OFFSET | STAGE9 AFE offset control (see Table 37) |
| 0x0CB | [15:0] | X | R/W | STAGE9_SENSITIVITY | STAGE9 sensitivity control (see Table 38) |
| 0x0CC | [15:0] | X | R/W | STAGE9_OFFSET_LOW | STAGE9 initial offset low value |
| 0x0CD | [15:0] | X | R/W | STAGE9_OFFSET_HIGH | STAGE9 initial offset high value |
| 0x0CE | [15:0] | X | R/W | STAGE9_OFFSET_HIGH_CLAMP | STAGE9 offset high clamp value |
| 0x0CF | [15:0] | X | R/W | STAGE9_OFFSET_LOW_CLAMP | STAGE9 offset low clamp value |
| 0x0D0 | [15:0] | X | R/W | STAGE10_CONNECTION[6:0] | STAGE10 CIN[6:0] connection setup (see Table 35) |
| 0x0D1 | [15:0] | X | R/W | STAGE10_CONNECTION[12:7] | STAGE10 CIN[12:7] connection setup (see Table 36) |
| 0x0D2 | [15:0] | X | R/W | STAGE10_AFE_OFFSET | STAGE10 AFE offset control (see Table 37) |
| 0x0D3 | [15:0] | X | R/W | STAGE10_SENSITIVITY | STAGE10 sensitivity control (see Table 38) |
| 0x0D4 | [15:0] | X | R/W | STAGE10_OFFSET_LOW | STAGE10 initial offset low value |
| 0x0D5 | [15:0] | X | R/W | STAGE10_OFFSET_HIGH | STAGE10 initial offset high value |
| 0x0D6 | [15:0] | X | R/W | STAGE10_OFFSET_HIGH_CLAMP | STAGE10 offset high clamp value |
| 0x0D7 | [15:0] | X | R/W | STAGE10_OFFSET_LOW_CLAMP | STAGE10 offset low clamp value |
| 0x0D8 | [15:0] | X | R/W | STAGE11_CONNECTION[6:0] | STAGE11 CIN[6:0] connection setup (see Table 35) |
| 0x0D9 | [15:0] | X | R/W | STAGE11_CONNECTION[12:7] | STAGE11 CIN[12:7] connection setup (see Table 36) |
| 0x0DA | [15:0] | X | R/W | STAGE11_AFE_OFFSET | STAGE11 AFE offset control (see Table 37) |
| 0x0DB | [15:0] | X | R/W | STAGE11_SENSITIVITY | STAGE11 sensitivity control (see Table 38) |
| 0x0DC | [15:0] | X | R/W | STAGE11_OFFSET_LOW | STAGE11 initial offset low value |
| 0x0DD | [15:0] | X | R/W | STAGE11_OFFSET_HIGH | STAGE11 initial offset high value |
| 0x0DE | [15:0] | X | R/W | STAGE11_OFFSET_HIGH_CLAMP | STAGE11 offset high clamp value |
| 0x0DF | [15:0] | X | R/W | STAGE11_OFFSET_LOW_CLAMP | STAGE11 offset low clamp value |

[1] X = don't care.

## BANK 3 REGISTERS

All address values are expressed in hexadecimal.

**Table 40. STAGE0 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x0E0 | [15:0] | X | R/W | STAGE0_CONV_DATA | STAGE0 CDC 16-bit conversion data (copy of CDC_RESULT_S0 register) |
| 0x0E1 | [15:0] | X | R/W | STAGE0_FF_WORD0 | STAGE0 fast FIFO WORD0 |
| 0x0E2 | [15:0] | X | R/W | STAGE0_FF_WORD1 | STAGE0 fast FIFO WORD1 |
| 0x0E3 | [15:0] | X | R/W | STAGE0_FF_WORD2 | STAGE0 fast FIFO WORD2 |
| 0x0E4 | [15:0] | X | R/W | STAGE0_FF_WORD3 | STAGE0 fast FIFO WORD3 |
| 0x0E5 | [15:0] | X | R/W | STAGE0_FF_WORD4 | STAGE0 fast FIFO WORD4 |
| 0x0E6 | [15:0] | X | R/W | STAGE0_FF_WORD5 | STAGE0 fast FIFO WORD5 |
| 0x0E7 | [15:0] | X | R/W | STAGE0_FF_WORD6 | STAGE0 fast FIFO WORD6 |
| 0x0E8 | [15:0] | X | R/W | STAGE0_FF_WORD7 | STAGE0 fast FIFO WORD7 |
| 0x0E9 | [15:0] | X | R/W | STAGE0_SF_WORD0 | STAGE0 slow FIFO WORD0 |
| 0x0EA | [15:0] | X | R/W | STAGE0_SF_WORD1 | STAGE0 slow FIFO WORD1 |
| 0x0EB | [15:0] | X | R/W | STAGE0_SF_WORD2 | STAGE0 slow FIFO WORD2 |
| 0x0EC | [15:0] | X | R/W | STAGE0_SF_WORD3 | STAGE0 slow FIFO WORD3 |
| 0x0ED | [15:0] | X | R/W | STAGE0_SF_WORD4 | STAGE0 slow FIFO WORD4 |
| 0x0EE | [15:0] | X | R/W | STAGE0_SF_WORD5 | STAGE0 slow FIFO WORD5 |
| 0x0EF | [15:0] | X | R/W | STAGE0_SF_WORD6 | STAGE0 slow FIFO WORD6 |
| 0x0F0 | [15:0] | X | R/W | STAGE0_SF_WORD7 | STAGE0 slow FIFO WORD7 |
| 0x0F1 | [15:0] | X | R/W | STAGE0_SF_AMBIENT | STAGE0 slow FIFO ambient value |
| 0x0F2 | [15:0] | X | R/W | STAGE0_FF_AVG | STAGE0 fast FIFO average value |
| 0x0F3 | [15:0] | X | R/W | STAGE0_PEAK_DETECT_WORD0 | STAGE0 peak FIFO WORD0 value |
| 0x0F4 | [15:0] | X | R/W | STAGE0_PEAK_DETECT_WORD1 | STAGE0 peak FIFO WORD1 value |
| 0x0F5 | [15:0] | X | R/W | STAGE0_MAX_WORD0 | STAGE0 maximum value FIFO WORD0 |
| 0x0F6 | [15:0] | X | R/W | STAGE0_MAX_WORD1 | STAGE0 maximum value FIFO WORD1 |
| 0x0F7 | [15:0] | X | R/W | STAGE0_MAX_WORD2 | STAGE0 maximum value FIFO WORD2 |
| 0x0F8 | [15:0] | X | R/W | STAGE0_MAX_WORD3 | STAGE0 maximum value FIFO WORD3 |
| 0x0F9 | [15:0] | X | R/W | STAGE0_MAX_AVG | STAGE0 average maximum FIFO value |
| 0x0FA | [15:0] | X | R/W | STAGE0_HIGH_THRESHOLD | STAGE0 high threshold value |
| 0x0FB | [15:0] | X | R/W | STAGE0_MAX_TEMP | STAGE0 temporary maximum value |
| 0x0FC | [15:0] | X | R/W | STAGE0_MIN_WORD0 | STAGE0 minimum value FIFO WORD0 |
| 0x0FD | [15:0] | X | R/W | STAGE0_MIN_WORD1 | STAGE0 minimum value FIFO WORD1 |
| 0x0FE | [15:0] | X | R/W | STAGE0_MIN_WORD2 | STAGE0 minimum value FIFO WORD2 |
| 0x0FF | [15:0] | X | R/W | STAGE0_MIN_WORD3 | STAGE0 minimum value FIFO WORD3 |
| 0x100 | [15:0] | X | R/W | STAGE0_MIN_AVG | STAGE0 average minimum FIFO value |
| 0x101 | [15:0] | X | R/W | STAGE0_LOW_THRESHOLD | STAGE0 low threshold value |
| 0x102 | [15:0] | X | R/W | STAGE0_MIN_TEMP | STAGE0 temporary minimum value |
| 0x103 | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 41. STAGE1 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x104 | [15:0] | X | R/W | STAGE1_CONV_DATA | STAGE1 CDC 16-bit conversion data (copy of CDC_RESULT_S1 register |
| 0x105 | [15:0] | X | R/W | STAGE1_FF_WORD0 | STAGE1 fast FIFO WORD0 |
| 0x106 | [15:0] | X | R/W | STAGE1_FF_WORD1 | STAGE1 fast FIFO WORD1 |
| 0x107 | [15:0] | X | R/W | STAGE1_FF_WORD2 | STAGE1 fast FIFO WORD2 |
| 0x108 | [15:0] | X | R/W | STAGE1_FF_WORD3 | STAGE1 fast FIFO WORD3 |
| 0x109 | [15:0] | X | R/W | STAGE1_FF_WORD4 | STAGE1 fast FIFO WORD4 |
| 0x10A | [15:0] | X | R/W | STAGE1_FF_WORD5 | STAGE1 fast FIFO WORD5 |
| 0x10B | [15:0] | X | R/W | STAGE1_FF_WORD6 | STAGE1 fast FIFO WORD6 |
| 0x10C | [15:0] | X | R/W | STAGE1_FF_WORD7 | STAGE1 fast FIFO WORD7 |
| 0x10D | [15:0] | X | R/W | STAGE1_SF_WORD0 | STAGE1 slow FIFO WORD0 |
| 0x10E | [15:0] | X | R/W | STAGE1_SF_WORD1 | STAGE1 slow FIFO WORD1 |
| 0x10F | [15:0] | X | R/W | STAGE1_SF_WORD2 | STAGE1 slow FIFO WORD2 |
| 0x110 | [15:0] | X | R/W | STAGE1_SF_WORD3 | STAGE1 slow FIFO WORD3 |
| 0x111 | [15:0] | X | R/W | STAGE1_SF_WORD4 | STAGE1 slow FIFO WORD4 |
| 0x112 | [15:0] | X | R/W | STAGE1_SF_WORD5 | STAGE1 slow FIFO WORD5 |
| 0x113 | [15:0] | X | R/W | STAGE1_SF_WORD6 | STAGE1 slow FIFO WORD6 |
| 0x114 | [15:0] | X | R/W | STAGE1_SF_WORD7 | STAGE1 slow FIFO WORD7 |
| 0x115 | [15:0] | X | R/W | STAGE1_SF_AMBIENT | STAGE1 slow FIFO ambient value |
| 0x116 | [15:0] | X | R/W | STAGE1_FF_AVG | STAGE1 fast FIFO average value |
| 0x117 | [15:0] | X | R/W | STAGE1_PEAK_DETECT_WORD0 | STAGE1 peak FIFO WORD0 value |
| 0x118 | [15:0] | X | R/W | STAGE1_PEAK_DETECT_WORD1 | STAGE1 peak FIFO WORD1 value |
| 0x119 | [15:0] | X | R/W | STAGE1_MAX_WORD0 | STAGE1 maximum value FIFO WORD0 |
| 0x11A | [15:0] | X | R/W | STAGE1_MAX_WORD1 | STAGE1 maximum value FIFO WORD1 |
| 0x11B | [15:0] | X | R/W | STAGE1_MAX_WORD2 | STAGE1 maximum value FIFO WORD2 |
| 0x11C | [15:0] | X | R/W | STAGE1_MAX_WORD3 | STAGE1 maximum value FIFO WORD3 |
| 0x11D | [15:0] | X | R/W | STAGE1_MAX_AVG | STAGE1 average maximum FIFO value |
| 0x11E | [15:0] | X | R/W | STAGE1_HIGH_THRESHOLD | STAGE1 high threshold value |
| 0x11F | [15:0] | X | R/W | STAGE1_MAX_TEMP | STAGE1 temporary maximum value |
| 0x120 | [15:0] | X | R/W | STAGE1_MIN_WORD0 | STAGE1 minimum value FIFO WORD0 |
| 0x121 | [15:0] | X | R/W | STAGE1_MIN_WORD1 | STAGE1 minimum value FIFO WORD1 |
| 0x122 | [15:0] | X | R/W | STAGE1_MIN_WORD2 | STAGE1 minimum value FIFO WORD2 |
| 0x123 | [15:0] | X | R/W | STAGE1_MIN_WORD3 | STAGE1 minimum value FIFO WORD3 |
| 0x124 | [15:0] | X | R/W | STAGE1_MIN_AVG | STAGE1 average minimum FIFO value |
| 0x125 | [15:0] | X | R/W | STAGE1_LOW_THRESHOLD | STAGE1 low threshold value |
| 0x126 | [15:0] | X | R/W | STAGE1_MIN_TEMP | STAGE1 temporary minimum value |
| 0x127 | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 42. STAGE2 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x128 | [15:0] | X | R/W | STAGE2_CONV_DATA | STAGE2 CDC 16-bit conversion data (copy of CDC_RESULT_S2 register) |
| 0x129 | [15:0] | X | R/W | STAGE2_FF_WORD0 | STAGE2 fast FIFO WORD0 |
| 0x12A | [15:0] | X | R/W | STAGE2_FF_WORD1 | STAGE2 fast FIFO WORD1 |
| 0x12B | [15:0] | X | R/W | STAGE2_FF_WORD2 | STAGE2 fast FIFO WORD2 |
| 0x12C | [15:0] | X | R/W | STAGE2_FF_WORD3 | STAGE2 fast FIFO WORD3 |
| 0x12D | [15:0] | X | R/W | STAGE2_FF_WORD4 | STAGE2 fast FIFO WORD4 |
| 0x12E | [15:0] | X | R/W | STAGE2_FF_WORD5 | STAGE2 fast FIFO WORD5 |
| 0x12F | [15:0] | X | R/W | STAGE2_FF_WORD6 | STAGE2 fast FIFO WORD6 |
| 0x130 | [15:0] | X | R/W | STAGE2_FF_WORD7 | STAGE2 fast FIFO WORD7 |
| 0x131 | [15:0] | X | R/W | STAGE2_SF_WORD0 | STAGE2 slow FIFO WORD0 |
| 0x132 | [15:0] | X | R/W | STAGE2_SF_WORD1 | STAGE2 slow FIFO WORD1 |
| 0x133 | [15:0] | X | R/W | STAGE2_SF_WORD2 | STAGE2 slow FIFO WORD2 |
| 0x134 | [15:0] | X | R/W | STAGE2_SF_WORD3 | STAGE2 slow FIFO WORD3 |
| 0x135 | [15:0] | X | R/W | STAGE2_SF_WORD4 | STAGE2 slow FIFO WORD4 |
| 0x136 | [15:0] | X | R/W | STAGE2_SF_WORD5 | STAGE2 slow FIFO WORD5 |
| 0x137 | [15:0] | X | R/W | STAGE2_SF_WORD6 | STAGE2 slow FIFO WORD6 |
| 0x138 | [15:0] | X | R/W | STAGE2_SF_WORD7 | STAGE2 slow FIFO WORD7 |
| 0x139 | [15:0] | X | R/W | STAGE2_SF_AMBIENT | STAGE2 slow FIFO ambient value |
| 0x13A | [15:0] | X | R/W | STAGE2_FF_AVG | STAGE2 fast FIFO average value |
| 0x13B | [15:0] | X | R/W | STAGE2_PEAK_DETECT_WORD0 | STAGE2 peak FIFO WORD0 value |
| 0x13C | [15:0] | X | R/W | STAGE2_PEAK_DETECT_WORD1 | STAGE2 peak FIFO WORD1 value |
| 0x13D | [15:0] | X | R/W | STAGE2_MAX_WORD0 | STAGE2 maximum value FIFO WORD0 |
| 0x13E | [15:0] | X | R/W | STAGE2_MAX_WORD1 | STAGE2 maximum value FIFO WORD1 |
| 0x13F | [15:0] | X | R/W | STAGE2_MAX_WORD2 | STAGE2 maximum value FIFO WORD2 |
| 0x140 | [15:0] | X | R/W | STAGE2_MAX_WORD3 | STAGE2 maximum value FIFO WORD3 |
| 0x141 | [15:0] | X | R/W | STAGE2_MAX_AVG | STAGE2 average maximum FIFO value |
| 0x142 | [15:0] | X | R/W | STAGE2_HIGH_THRESHOLD | STAGE2 high threshold value |
| 0x143 | [15:0] | X | R/W | STAGE2_MAX_TEMP | STAGE2 temporary maximum value |
| 0x144 | [15:0] | X | R/W | STAGE2_MIN_WORD0 | STAGE2 minimum value FIFO WORD0 |
| 0x145 | [15:0] | X | R/W | STAGE2_MIN_WORD1 | STAGE2 minimum value FIFO WORD1 |
| 0x146 | [15:0] | X | R/W | STAGE2_MIN_WORD2 | STAGE2 minimum value FIFO WORD2 |
| 0x147 | [15:0] | X | R/W | STAGE2_MIN_WORD3 | STAGE2 minimum value FIFO WORD3 |
| 0x148 | [15:0] | X | R/W | STAGE2_MIN_AVG | STAGE2 average minimum FIFO value |
| 0x149 | [15:0] | X | R/W | STAGE2_LOW_THRESHOLD | STAGE2 low threshold value |
| 0x14A | [15:0] | X | R/W | STAGE2_MIN_TEMP | STAGE2 temporary minimum value |
| 0x14B | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 43. STAGE3 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x14C | [15:0] | X | R/W | STAGE3_CONV_DATA | STAGE3 CDC 16-bit conversion data (copy of CDC_RESULT_S3 register) |
| 0x14D | [15:0] | X | R/W | STAGE3_FF_WORD0 | STAGE3 fast FIFO WORD0 |
| 0x14E | [15:0] | X | R/W | STAGE3_FF_WORD1 | STAGE3 fast FIFO WORD1 |
| 0x14F | [15:0] | X | R/W | STAGE3_FF_WORD2 | STAGE3 fast FIFO WORD2 |
| 0x150 | [15:0] | X | R/W | STAGE3_FF_WORD3 | STAGE3 fast FIFO WORD3 |
| 0x151 | [15:0] | X | R/W | STAGE3_FF_WORD4 | STAGE3 fast FIFO WORD4 |
| 0x152 | [15:0] | X | R/W | STAGE3_FF_WORD5 | STAGE3 fast FIFO WORD5 |
| 0x153 | [15:0] | X | R/W | STAGE3_FF_WORD6 | STAGE3 fast FIFO WORD6 |
| 0x154 | [15:0] | X | R/W | STAGE3_FF_WORD7 | STAGE3 fast FIFO WORD7 |
| 0x155 | [15:0] | X | R/W | STAGE3_SF_WORD0 | STAGE3 slow FIFO WORD0 |
| 0x156 | [15:0] | X | R/W | STAGE3_SF_WORD1 | STAGE3 slow FIFO WORD1 |
| 0x157 | [15:0] | X | R/W | STAGE3_SF_WORD2 | STAGE3 slow FIFO WORD2 |
| 0x158 | [15:0] | X | R/W | STAGE3_SF_WORD3 | STAGE3 slow FIFO WORD3 |
| 0x159 | [15:0] | X | R/W | STAGE3_SF_WORD4 | STAGE3 slow FIFO WORD4 |
| 0x15A | [15:0] | X | R/W | STAGE3_SF_WORD5 | STAGE3 slow FIFO WORD5 |
| 0x15B | [15:0] | X | R/W | STAGE3_SF_WORD6 | STAGE3 slow FIFO WORD6 |
| 0x15C | [15:0] | X | R/W | STAGE3_SF_WORD7 | STAGE3 slow FIFO WORD7 |
| 0x15D | [15:0] | X | R/W | STAGE3_SF_AMBIENT | STAGE3 slow FIFO ambient value |
| 0x15E | [15:0] | X | R/W | STAGE3_FF_AVG | STAGE3 fast FIFO average value |
| 0x15F | [15:0] | X | R/W | STAGE3_PEAK_DETECT_WORD0 | STAGE3 peak FIFO WORD0 value |
| 0x160 | [15:0] | X | R/W | STAGE3_PEAK_DETECT_WORD1 | STAGE3 peak FIFO WORD1 value |
| 0x161 | [15:0] | X | R/W | STAGE3_MAX_WORD0 | STAGE3 maximum value FIFO WORD0 |
| 0x162 | [15:0] | X | R/W | STAGE3_MAX_WORD1 | STAGE3 maximum value FIFO WORD1 |
| 0x163 | [15:0] | X | R/W | STAGE3_MAX_WORD2 | STAGE3 maximum value FIFO WORD2 |
| 0x164 | [15:0] | X | R/W | STAGE3_MAX_WORD3 | STAGE3 maximum value FIFO WORD3 |
| 0x165 | [15:0] | X | R/W | STAGE3_MAX_AVG | STAGE3 average maximum FIFO value |
| 0x166 | [15:0] | X | R/W | STAGE3_HIGH_THRESHOLD | STAGE3 high threshold value |
| 0x167 | [15:0] | X | R/W | STAGE3_MAX_TEMP | STAGE3 temporary maximum value |
| 0x168 | [15:0] | X | R/W | STAGE3_MIN_WORD0 | STAGE3 minimum value FIFO WORD0 |
| 0x169 | [15:0] | X | R/W | STAGE3_MIN_WORD1 | STAGE3 minimum value FIFO WORD1 |
| 0x16A | [15:0] | X | R/W | STAGE3_MIN_WORD2 | STAGE3 minimum value FIFO WORD2 |
| 0x16B | [15:0] | X | R/W | STAGE3_MIN_WORD3 | STAGE3 minimum value FIFO WORD3 |
| 0x16C | [15:0] | X | R/W | STAGE3_MIN_AVG | STAGE3 average minimum FIFO value |
| 0x16D | [15:0] | X | R/W | STAGE3_LOW_THRESHOLD | STAGE3 low threshold value |
| 0x16E | [15:0] | X | R/W | STAGE3_MIN_TEMP | STAGE3 temporary minimum value |
| 0x16F | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 44. STAGE4 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x170 | [15:0] | X | R/W | STAGE4_CONV_DATA | STAGE4 CDC 16-bit conversion data (copy of CDC_RESULT_S4 register) |
| 0x171 | [15:0] | X | R/W | STAGE4_FF_WORD0 | STAGE4 fast FIFO WORD0 |
| 0x172 | [15:0] | X | R/W | STAGE4_FF_WORD1 | STAGE4 fast FIFO WORD1 |
| 0x173 | [15:0] | X | R/W | STAGE4_FF_WORD2 | STAGE4 fast FIFO WORD2 |
| 0x174 | [15:0] | X | R/W | STAGE4_FF_WORD3 | STAGE4 fast FIFO WORD3 |
| 0x175 | [15:0] | X | R/W | STAGE4_FF_WORD4 | STAGE4 fast FIFO WORD4 |
| 0x176 | [15:0] | X | R/W | STAGE4_FF_WORD5 | STAGE4 fast FIFO WORD5 |
| 0x177 | [15:0] | X | R/W | STAGE4_FF_WORD6 | STAGE4 fast FIFO WORD6 |
| 0x178 | [15:0] | X | R/W | STAGE4_FF_WORD7 | STAGE4 fast FIFO WORD7 |
| 0x179 | [15:0] | X | R/W | STAGE4_SF_WORD0 | STAGE4 slow FIFO WORD0 |
| 0x17A | [15:0] | X | R/W | STAGE4_SF_WORD1 | STAGE4 slow FIFO WORD1 |
| 0x17B | [15:0] | X | R/W | STAGE4_SF_WORD2 | STAGE4 slow FIFO WORD2 |
| 0x17C | [15:0] | X | R/W | STAGE4_SF_WORD3 | STAGE4 slow FIFO WORD3 |
| 0x17D | [15:0] | X | R/W | STAGE4_SF_WORD4 | STAGE4 slow FIFO WORD4 |
| 0x17E | [15:0] | X | R/W | STAGE4_SF_WORD5 | STAGE4 slow FIFO WORD5 |
| 0x17F | [15:0] | X | R/W | STAGE4_SF_WORD6 | STAGE4 slow FIFO WORD6 |
| 0x180 | [15:0] | X | R/W | STAGE4_SF_WORD7 | STAGE4 slow FIFO WORD7 |
| 0x181 | [15:0] | X | R/W | STAGE4_SF_AMBIENT | STAGE4 slow FIFO ambient value |
| 0x182 | [15:0] | X | R/W | STAGE4_FF_AVG | STAGE4 fast FIFO average value |
| 0x183 | [15:0] | X | R/W | STAGE4_PEAK_DETECT_WORD0 | STAGE4 peak FIFO WORD0 value |
| 0x184 | [15:0] | X | R/W | STAGE4_PEAK_DETECT_WORD1 | STAGE4 peak FIFO WORD1 value |
| 0x185 | [15:0] | X | R/W | STAGE4_MAX_WORD0 | STAGE4 maximum value FIFO WORD0 |
| 0x186 | [15:0] | X | R/W | STAGE4_MAX_WORD1 | STAGE4 maximum value FIFO WORD1 |
| 0x187 | [15:0] | X | R/W | STAGE4_MAX_WORD2 | STAGE4 maximum value FIFO WORD2 |
| 0x188 | [15:0] | X | R/W | STAGE4_MAX_WORD3 | STAGE4 maximum value FIFO WORD3 |
| 0x189 | [15:0] | X | R/W | STAGE4_MAX_AVG | STAGE4 average maximum FIFO value |
| 0x18A | [15:0] | X | R/W | STAGE4_HIGH_THRESHOLD | STAGE4 high threshold value |
| 0x18B | [15:0] | X | R/W | STAGE4_MAX_TEMP | STAGE4 temporary maximum value |
| 0x18C | [15:0] | X | R/W | STAGE4_MIN_WORD0 | STAGE4 minimum value FIFO WORD0 |
| 0x18D | [15:0] | X | R/W | STAGE4_MIN_WORD1 | STAGE4 minimum value FIFO WORD1 |
| 0x18E | [15:0] | X | R/W | STAGE4_MIN_WORD2 | STAGE4 minimum value FIFO WORD2 |
| 0x18F | [15:0] | X | R/W | STAGE4_MIN_WORD3 | STAGE4 minimum value FIFO WORD3 |
| 0x190 | [15:0] | X | R/W | STAGE4_MIN_AVG | STAGE4 average minimum FIFO value |
| 0x191 | [15:0] | X | R/W | STAGE4_LOW_THRESHOLD | STAGE4 low threshold value |
| 0x192 | [15:0] | X | R/W | STAGE4_MIN_TEMP | STAGE4 temporary minimum value |
| 0x193 | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 45. STAGE5 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x194 | [15:0] | X | R/W | STAGE5_CONV_DATA | STAGE5 CDC 16-bit conversion data (copy of CDC_RESULT_S5 register) |
| 0x195 | [15:0] | X | R/W | STAGE5_FF_WORD0 | STAGE5 fast FIFO WORD0 |
| 0x196 | [15:0] | X | R/W | STAGE5_FF_WORD1 | STAGE5 fast FIFO WORD1 |
| 0x197 | [15:0] | X | R/W | STAGE5_FF_WORD2 | STAGE5 fast FIFO WORD2 |
| 0x198 | [15:0] | X | R/W | STAGE5_FF_WORD3 | STAGE5 fast FIFO WORD3 |
| 0x199 | [15:0] | X | R/W | STAGE5_FF_WORD4 | STAGE5 fast FIFO WORD4 |
| 0x19A | [15:0] | X | R/W | STAGE5_FF_WORD5 | STAGE5 fast FIFO WORD5 |
| 0x19B | [15:0] | X | R/W | STAGE5_FF_WORD6 | STAGE5 fast FIFO WORD6 |
| 0x19C | [15:0] | X | R/W | STAGE5_FF_WORD7 | STAGE5 fast FIFO WORD7 |
| 0x19D | [15:0] | X | R/W | STAGE5_SF_WORD0 | STAGE5 slow FIFO WORD0 |
| 0x19E | [15:0] | X | R/W | STAGE5_SF_WORD1 | STAGE5 slow FIFO WORD1 |
| 0x19F | [15:0] | X | R/W | STAGE5_SF_WORD2 | STAGE5 slow FIFO WORD2 |
| 0x1A0 | [15:0] | X | R/W | STAGE5_SF_WORD3 | STAGE5 slow FIFO WORD3 |
| 0x1A1 | [15:0] | X | R/W | STAGE5_SF_WORD4 | STAGE5 slow FIFO WORD4 |
| 0x1A2 | [15:0] | X | R/W | STAGE5_SF_WORD5 | STAGE5 slow FIFO WORD5 |
| 0x1A3 | [15:0] | X | R/W | STAGE5_SF_WORD6 | STAGE5 slow FIFO WORD6 |
| 0x1A4 | [15:0] | X | R/W | STAGE5_SF_WORD7 | STAGE5 slow FIFO WORD7 |
| 0x1A5 | [15:0] | X | R/W | STAGE5_SF_AMBIENT | STAGE5 slow FIFO ambient value |
| 0x1A6 | [15:0] | X | R/W | STAGE5_FF_AVG | STAGE5 fast FIFO average value |
| 0x1A7 | [15:0] | X | R/W | STAGE5_PEAK_DETECT_WORD0 | STAGE5 peak FIFO WORD0 value |
| 0x1A8 | [15:0] | X | R/W | STAGE5_PEAK_DETECT_WORD1 | STAGE5 peak FIFO WORD1 value |
| 0x1A9 | [15:0] | X | R/W | STAGE5_MAX_WORD0 | STAGE5 maximum value FIFO WORD0 |
| 0x1AA | [15:0] | X | R/W | STAGE5_MAX_WORD1 | STAGE5 maximum value FIFO WORD1 |
| 0x1AB | [15:0] | X | R/W | STAGE5_MAX_WORD2 | STAGE5 maximum value FIFO WORD2 |
| 0x1AC | [15:0] | X | R/W | STAGE5_MAX_WORD3 | STAGE5 maximum value FIFO WORD3 |
| 0x1AD | [15:0] | X | R/W | STAGE5_MAX_AVG | STAGE5 average maximum FIFO value |
| 0x1AE | [15:0] | X | R/W | STAGE5_HIGH_THRESHOLD | STAGE5 high threshold value |
| 0x1AF | [15:0] | X | R/W | STAGE5_MAX_TEMP | STAGE5 temporary maximum value |
| 0x1B0 | [15:0] | X | R/W | STAGE5_MIN_WORD0 | STAGE5 minimum value FIFO WORD0 |
| 0x1B1 | [15:0] | X | R/W | STAGE5_MIN_WORD1 | STAGE5 minimum value FIFO WORD1 |
| 0x1B2 | [15:0] | X | R/W | STAGE5_MIN_WORD2 | STAGE5 minimum value FIFO WORD2 |
| 0x1B3 | [15:0] | X | R/W | STAGE5_MIN_WORD3 | STAGE5 minimum value FIFO WORD3 |
| 0x1B4 | [15:0] | X | R/W | STAGE5_MIN_AVG | STAGE5 average minimum FIFO value |
| 0x1B5 | [15:0] | X | R/W | STAGE5_LOW_THRESHOLD | STAGE5 low threshold value |
| 0x1B6 | [15:0] | X | R/W | STAGE5_MIN_TEMP | STAGE5 temporary minimum value |
| 0x1B7 | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 46. STAGE6 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x1B8 | [15:0] | X | R/W | STAGE6_CONV_DATA | STAGE6 CDC 16-bit conversion data (copy of CDC_RESULT_S6 register) |
| 0x1B9 | [15:0] | X | R/W | STAGE6_FF_WORD0 | STAGE6 fast FIFO WORD0 |
| 0x1BA | [15:0] | X | R/W | STAGE6_FF_WORD1 | STAGE6 fast FIFO WORD1 |
| 0x1BB | [15:0] | X | R/W | STAGE6_FF_WORD2 | STAGE6 fast FIFO WORD2 |
| 0x1BC | [15:0] | X | R/W | STAGE6_FF_WORD3 | STAGE6 fast FIFO WORD3 |
| 0x1BD | [15:0] | X | R/W | STAGE6_FF_WORD4 | STAGE6 fast FIFO WORD4 |
| 0x1BE | [15:0] | X | R/W | STAGE6_FF_WORD5 | STAGE6 fast FIFO WORD5 |
| 0x1BF | [15:0] | X | R/W | STAGE6_FF_WORD6 | STAGE6 fast FIFO WORD6 |
| 0x1C0 | [15:0] | X | R/W | STAGE6_FF_WORD7 | STAGE6 fast FIFO WORD7 |
| 0x1C1 | [15:0] | X | R/W | STAGE6_SF_WORD0 | STAGE6 slow FIFO WORD0 |
| 0x1C2 | [15:0] | X | R/W | STAGE6_SF_WORD1 | STAGE6 slow FIFO WORD1 |
| 0x1C3 | [15:0] | X | R/W | STAGE6_SF_WORD2 | STAGE6 slow FIFO WORD2 |
| 0x1C4 | [15:0] | X | R/W | STAGE6_SF_WORD3 | STAGE6 slow FIFO WORD3 |
| 0x1C5 | [15:0] | X | R/W | STAGE6_SF_WORD4 | STAGE6 slow FIFO WORD4 |
| 0x1C6 | [15:0] | X | R/W | STAGE6_SF_WORD5 | STAGE6 slow FIFO WORD5 |
| 0x1C7 | [15:0] | X | R/W | STAGE6_SF_WORD6 | STAGE6 slow FIFO WORD6 |
| 0x1C8 | [15:0] | X | R/W | STAGE6_SF_WORD7 | STAGE6 slow FIFO WORD7 |
| 0x1C9 | [15:0] | X | R/W | STAGE6_SF_AMBIENT | STAGE6 slow FIFO ambient value |
| 0x1CA | [15:0] | X | R/W | STAGE6_FF_AVG | STAGE6 fast FIFO average value |
| 0x1CB | [15:0] | X | R/W | STAGE6_PEAK_DETECT_WORD0 | STAGE6 peak FIFO WORD0 value |
| 0x1CC | [15:0] | X | R/W | STAGE6_PEAK_DETECT_WORD1 | STAGE6 peak FIFO WORD1 value |
| 0x1CD | [15:0] | X | R/W | STAGE6_MAX_WORD0 | STAGE6 maximum value FIFO WORD0 |
| 0x1CE | [15:0] | X | R/W | STAGE6_MAX_WORD1 | STAGE6 maximum value FIFO WORD1 |
| 0x1CF | [15:0] | X | R/W | STAGE6_MAX_WORD2 | STAGE6 maximum value FIFO WORD2 |
| 0x1D0 | [15:0] | X | R/W | STAGE6_MAX_WORD3 | STAGE6 maximum value FIFO WORD3 |
| 0x1D1 | [15:0] | X | R/W | STAGE6_MAX_AVG | STAGE6 average maximum FIFO value |
| 0x1D2 | [15:0] | X | R/W | STAGE6_HIGH_THRESHOLD | STAGE6 high threshold value |
| 0x1D3 | [15:0] | X | R/W | STAGE6_MAX_TEMP | STAGE6 temporary maximum value |
| 0x1D4 | [15:0] | X | R/W | STAGE6_MIN_WORD0 | STAGE6 minimum value FIFO WORD0 |
| 0x1D5 | [15:0] | X | R/W | STAGE6_MIN_WORD1 | STAGE6 minimum value FIFO WORD1 |
| 0x1D6 | [15:0] | X | R/W | STAGE6_MIN_WORD2 | STAGE6 minimum value FIFO WORD2 |
| 0x1D7 | [15:0] | X | R/W | STAGE6_MIN_WORD3 | STAGE6 minimum value FIFO WORD3 |
| 0x1D8 | [15:0] | X | R/W | STAGE6_MIN_AVG | STAGE6 average minimum FIFO value |
| 0x1D9 | [15:0] | X | R/W | STAGE6_LOW_THRESHOLD | STAGE6 low threshold value |
| 0x1DA | [15:0] | X | R/W | STAGE6_MIN_TEMP | STAGE6 temporary minimum value |
| 0x1DB | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 47. STAGE7 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x1DC | [15:0] | X | R/W | STAGE7_CONV_DATA | STAGE7 CDC 16-bit conversion data (copy of CDC_RESULT_S7 register) |
| 0x1DD | [15:0] | X | R/W | STAGE7_FF_WORD0 | STAGE7 fast FIFO WORD0 |
| 0x1DE | [15:0] | X | R/W | STAGE7_FF_WORD1 | STAGE7 fast FIFO WORD1 |
| 0x1DF | [15:0] | X | R/W | STAGE7_FF_WORD2 | STAGE7 fast FIFO WORD2 |
| 0x1E0 | [15:0] | X | R/W | STAGE7_FF_WORD3 | STAGE7 fast FIFO WORD3 |
| 0x1E1 | [15:0] | X | R/W | STAGE7_FF_WORD4 | STAGE7 fast FIFO WORD4 |
| 0x1E2 | [15:0] | X | R/W | STAGE7_FF_WORD5 | STAGE7 fast FIFO WORD5 |
| 0x1E3 | [15:0] | X | R/W | STAGE7_FF_WORD6 | STAGE7 fast FIFO WORD6 |
| 0x1E4 | [15:0] | X | R/W | STAGE7_FF_WORD7 | STAGE7 fast FIFO WORD7 |
| 0x1E5 | [15:0] | X | R/W | STAGE7_SF_WORD0 | STAGE7 slow FIFO WORD0 |
| 0x1E6 | [15:0] | X | R/W | STAGE7_SF_WORD1 | STAGE7 slow FIFO WORD1 |
| 0x1E7 | [15:0] | X | R/W | STAGE7_SF_WORD2 | STAGE7 slow FIFO WORD2 |
| 0x1E8 | [15:0] | X | R/W | STAGE7_SF_WORD3 | STAGE7 slow FIFO WORD3 |
| 0x1E9 | [15:0] | X | R/W | STAGE7_SF_WORD4 | STAGE7 slow FIFO WORD4 |
| 0x1EA | [15:0] | X | R/W | STAGE7_SF_WORD5 | STAGE7 slow FIFO WORD5 |
| 0x1EB | [15:0] | X | R/W | STAGE7_SF_WORD6 | STAGE7 slow FIFO WORD6 |
| 0x1EC | [15:0] | X | R/W | STAGE7_SF_WORD7 | STAGE7 slow FIFO WORD7 |
| 0x1ED | [15:0] | X | R/W | STAGE7_SF_AMBIENT | STAGE7 slow FIFO ambient value |
| 0x1EE | [15:0] | X | R/W | STAGE7_FF_AVG | STAGE7 fast FIFO average value |
| 0x1EF | [15:0] | X | R/W | STAGE7_PEAK_DETECT_WORD0 | STAGE7 peak FIFO WORD0 value |
| 0x1F0 | [15:0] | X | R/W | STAGE7_PEAK_DETECT_WORD1 | STAGE7 peak FIFO WORD1 value |
| 0x1F1 | [15:0] | X | R/W | STAGE7_MAX_WORD0 | STAGE7 maximum value FIFO WORD0 |
| 0x1F2 | [15:0] | X | R/W | STAGE7_MAX_WORD1 | STAGE7 maximum value FIFO WORD1 |
| 0x1F3 | [15:0] | X | R/W | STAGE7_MAX_WORD2 | STAGE7 maximum value FIFO WORD2 |
| 0x1F4 | [15:0] | X | R/W | STAGE7_MAX_WORD3 | STAGE7 maximum value FIFO WORD3 |
| 0x1F5 | [15:0] | X | R/W | STAGE7_MAX_AVG | STAGE7 average maximum FIFO value |
| 0x1F6 | [15:0] | X | R/W | STAGE7_HIGH_THRESHOLD | STAGE7 high threshold value |
| 0x1F7 | [15:0] | X | R/W | STAGE7_MAX_TEMP | STAGE7 temporary maximum value |
| 0x1F8 | [15:0] | X | R/W | STAGE7_MIN_WORD0 | STAGE7 minimum value FIFO WORD0 |
| 0x1F9 | [15:0] | X | R/W | STAGE7_MIN_WORD1 | STAGE7 minimum value FIFO WORD1 |
| 0x1FA | [15:0] | X | R/W | STAGE7_MIN_WORD2 | STAGE7 minimum value FIFO WORD2 |
| 0x1FB | [15:0] | X | R/W | STAGE7_MIN_WORD3 | STAGE7 minimum value FIFO WORD3 |
| 0x1FC | [15:0] | X | R/W | STAGE7_MIN_AVG | STAGE7 average minimum FIFO value |
| 0x1FD | [15:0] | X | R/W | STAGE7_LOW_THRESHOLD | STAGE7 low threshold value |
| 0x1FE | [15:0] | X | R/W | STAGE7_MIN_TEMP | STAGE7 temporary minimum value |
| 0x1FF | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 48. STAGE8 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x200 | [15:0] | X | R/W | STAGE8_CONV_DATA | STAGE8 CDC 16-bit conversion data (copy of CDC_RESULT_S8 register) |
| 0x201 | [15:0] | X | R/W | STAGE8_FF_WORD0 | STAGE8 fast FIFO WORD0 |
| 0x202 | [15:0] | X | R/W | STAGE8_FF_WORD1 | STAGE8 fast FIFO WORD1 |
| 0x203 | [15:0] | X | R/W | STAGE8_FF_WORD2 | STAGE8 fast FIFO WORD2 |
| 0x204 | [15:0] | X | R/W | STAGE8_FF_WORD3 | STAGE8 fast FIFO WORD3 |
| 0x205 | [15:0] | X | R/W | STAGE8_FF_WORD4 | STAGE8 fast FIFO WORD4 |
| 0x206 | [15:0] | X | R/W | STAGE8_FF_WORD5 | STAGE8 fast FIFO WORD5 |
| 0x207 | [15:0] | X | R/W | STAGE8_FF_WORD6 | STAGE8 fast FIFO WORD6 |
| 0x208 | [15:0] | X | R/W | STAGE8_FF_WORD7 | STAGE8 fast FIFO WORD7 |
| 0x209 | [15:0] | X | R/W | STAGE8_SF_WORD0 | STAGE8 slow FIFO WORD0 |
| 0x20A | [15:0] | X | R/W | STAGE8_SF_WORD1 | STAGE8 slow FIFO WORD1 |
| 0x20B | [15:0] | X | R/W | STAGE8_SF_WORD2 | STAGE8 slow FIFO WORD2 |
| 0x20C | [15:0] | X | R/W | STAGE8_SF_WORD3 | STAGE8 slow FIFO WORD3 |
| 0x20D | [15:0] | X | R/W | STAGE8_SF_WORD4 | STAGE8 slow FIFO WORD4 |
| 0x20E | [15:0] | X | R/W | STAGE8_SF_WORD5 | STAGE8 slow FIFO WORD5 |
| 0x20F | [15:0] | X | R/W | STAGE8_SF_WORD6 | STAGE8 slow FIFO WORD6 |
| 0x210 | [15:0] | X | R/W | STAGE8_SF_WORD7 | STAGE8 slow FIFO WORD7 |
| 0x211 | [15:0] | X | R/W | STAGE8_SF_AMBIENT | STAGE8 slow FIFO ambient value |
| 0x212 | [15:0] | X | R/W | STAGE8_FF_AVG | STAGE8 fast FIFO average value |
| 0x213 | [15:0] | X | R/W | STAGE8_PEAK_DETECT_WORD0 | STAGE8 peak FIFO WORD0 value |
| 0x214 | [15:0] | X | R/W | STAGE8_PEAK_DETECT_WORD1 | STAGE8 peak FIFO WORD1 value |
| 0x215 | [15:0] | X | R/W | STAGE8_MAX_WORD0 | STAGE8 maximum value FIFO WORD0 |
| 0x216 | [15:0] | X | R/W | STAGE8_MAX_WORD1 | STAGE8 maximum value FIFO WORD1 |
| 0x217 | [15:0] | X | R/W | STAGE8_MAX_WORD2 | STAGE8 maximum value FIFO WORD2 |
| 0x218 | [15:0] | X | R/W | STAGE8_MAX_WORD3 | STAGE8 maximum value FIFO WORD3 |
| 0x219 | [15:0] | X | R/W | STAGE8_MAX_AVG | STAGE8 average maximum FIFO value |
| 0x21A | [15:0] | X | R/W | STAGE8_HIGH_THRESHOLD | STAGE8 high threshold value |
| 0x21B | [15:0] | X | R/W | STAGE8_MAX_TEMP | STAGE8 temporary maximum value |
| 0x21C | [15:0] | X | R/W | STAGE8_MIN_WORD0 | STAGE8 minimum value FIFO WORD0 |
| 0x21D | [15:0] | X | R/W | STAGE8_MIN_WORD1 | STAGE8 minimum value FIFO WORD1 |
| 0x21E | [15:0] | X | R/W | STAGE8_MIN_WORD2 | STAGE8 minimum value FIFO WORD2 |
| 0x21F | [15:0] | X | R/W | STAGE8_MIN_WORD3 | STAGE8 minimum value FIFO WORD3 |
| 0x220 | [15:0] | X | R/W | STAGE8_MIN_AVG | STAGE8 average minimum FIFO value |
| 0x221 | [15:0] | X | R/W | STAGE8_LOW_THRESHOLD | STAGE8 low threshold value |
| 0x222 | [15:0] | X | R/W | STAGE8_MIN_TEMP | STAGE7 temporary minimum value |
| 0x223 | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 49. STAGE9 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x224 | [15:0] | X | R/W | STAGE9_CONV_DATA | STAGE9 CDC 16-bit conversion data (copy of CDC_RESULT_S9 register) |
| 0x225 | [15:0] | X | R/W | STAGE9_FF_WORD0 | STAGE9 fast FIFO WORD0 |
| 0x226 | [15:0] | X | R/W | STAGE9_FF_WORD1 | STAGE9 fast FIFO WORD1 |
| 0x227 | [15:0] | X | R/W | STAGE9_FF_WORD2 | STAGE9 fast FIFO WORD2 |
| 0x228 | [15:0] | X | R/W | STAGE9_FF_WORD3 | STAGE9 fast FIFO WORD3 |
| 0x229 | [15:0] | X | R/W | STAGE9_FF_WORD4 | STAGE9 fast FIFO WORD4 |
| 0x22A | [15:0] | X | R/W | STAGE9_FF_WORD5 | STAGE9 fast FIFO WORD5 |
| 0x22B | [15:0] | X | R/W | STAGE9_FF_WORD6 | STAGE9 fast FIFO WORD6 |
| 0x22C | [15:0] | X | R/W | STAGE9_FF_WORD7 | STAGE9 fast FIFO WORD7 |
| 0x22D | [15:0] | X | R/W | STAGE9_SF_WORD0 | STAGE9 slow FIFO WORD0 |
| 0x22E | [15:0] | X | R/W | STAGE9_SF_WORD1 | STAGE9 slow FIFO WORD1 |
| 0x22F | [15:0] | X | R/W | STAGE9_SF_WORD2 | STAGE9 slow FIFO WORD2 |
| 0x230 | [15:0] | X | R/W | STAGE9_SF_WORD3 | STAGE9 slow FIFO WORD3 |
| 0x231 | [15:0] | X | R/W | STAGE9_SF_WORD4 | STAGE9 slow FIFO WORD4 |
| 0x232 | [15:0] | X | R/W | STAGE9_SF_WORD5 | STAGE9 slow FIFO WORD5 |
| 0x233 | [15:0] | X | R/W | STAGE9_SF_WORD6 | STAGE9 slow FIFO WORD6 |
| 0x234 | [15:0] | X | R/W | STAGE9_SF_WORD7 | STAGE9 slow FIFO WORD7 |
| 0x235 | [15:0] | X | R/W | STAGE9_SF_AMBIENT | STAGE9 slow FIFO ambient value |
| 0x236 | [15:0] | X | R/W | STAGE9_FF_AVG | STAGE9 fast FIFO average value |
| 0x237 | [15:0] | X | R/W | STAGE9_PEAK_DETECT_WORD0 | STAGE9 peak FIFO WORD0 value |
| 0x238 | [15:0] | X | R/W | STAGE9_PEAK_DETECT_WORD1 | STAGE9 peak FIFO WORD1 value |
| 0x239 | [15:0] | X | R/W | STAGE9_MAX_WORD0 | STAGE9 maximum value FIFO WORD0 |
| 0x23A | [15:0] | X | R/W | STAGE9_MAX_WORD1 | STAGE9 maximum value FIFO WORD1 |
| 0x23B | [15:0] | X | R/W | STAGE9_MAX_WORD2 | STAGE9 maximum value FIFO WORD2 |
| 0x23C | [15:0] | X | R/W | STAGE9_MAX_WORD3 | STAGE9 maximum value FIFO WORD3 |
| 0x23D | [15:0] | X | R/W | STAGE9_MAX_AVG | STAGE9 average maximum FIFO value |
| 0x23E | [15:0] | X | R/W | STAGE9_HIGH_THRESHOLD | STAGE9 high threshold value |
| 0x23F | [15:0] | X | R/W | STAGE9_MAX_TEMP | STAGE9 temporary maximum value |
| 0x240 | [15:0] | X | R/W | STAGE9_MIN_WORD0 | STAGE9 minimum value FIFO WORD0 |
| 0x241 | [15:0] | X | R/W | STAGE9_MIN_WORD1 | STAGE9 minimum value FIFO WORD1 |
| 0x242 | [15:0] | X | R/W | STAGE9_MIN_WORD2 | STAGE9 minimum value FIFO WORD2 |
| 0x243 | [15:0] | X | R/W | STAGE9_MIN_WORD3 | STAGE9 minimum value FIFO WORD3 |
| 0x244 | [15:0] | X | R/W | STAGE9_MIN_AVG | STAGE9 average minimum FIFO value |
| 0x245 | [15:0] | X | R/W | STAGE9_LOW_THRESHOLD | STAGE9 low threshold value |
| 0x246 | [15:0] | X | R/W | STAGE9_MIN_TEMP | STAGE9 temporary minimum value |
| 0x247 | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 50. STAGE10 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x248 | [15:0] | X | R/W | STAGE10_CONV_DATA | STAGE10 CDC 16-bit conversion data (copy of CDC_RESULT_S10 register) |
| 0x249 | [15:0] | X | R/W | STAGE10_FF_WORD0 | STAGE10 fast FIFO WORD0 |
| 0x24A | [15:0] | X | R/W | STAGE10_FF_WORD1 | STAGE10 fast FIFO WORD1 |
| 0x24B | [15:0] | X | R/W | STAGE10_FF_WORD2 | STAGE10 fast FIFO WORD2 |
| 0x24C | [15:0] | X | R/W | STAGE10_FF_WORD3 | STAGE10 fast FIFO WORD3 |
| 0x24D | [15:0] | X | R/W | STAGE10_FF_WORD4 | STAGE10 fast FIFO WORD4 |
| 0x24E | [15:0] | X | R/W | STAGE10_FF_WORD5 | STAGE10 fast FIFO WORD5 |
| 0x24F | [15:0] | X | R/W | STAGE10_FF_WORD6 | STAGE10 fast FIFO WORD6 |
| 0x250 | [15:0] | X | R/W | STAGE10_FF_WORD7 | STAGE10 fast FIFO WORD7 |
| 0x251 | [15:0] | X | R/W | STAGE10_SF_WORD0 | STAGE10 slow FIFO WORD0 |
| 0x252 | [15:0] | X | R/W | STAGE10_SF_WORD1 | STAGE10 slow FIFO WORD1 |
| 0x253 | [15:0] | X | R/W | STAGE10_SF_WORD2 | STAGE10 slow FIFO WORD2 |
| 0x254 | [15:0] | X | R/W | STAGE10_SF_WORD3 | STAGE10 slow FIFO WORD3 |
| 0x255 | [15:0] | X | R/W | STAGE10_SF_WORD4 | STAGE10 slow FIFO WORD4 |
| 0x256 | [15:0] | X | R/W | STAGE10_SF_WORD5 | STAGE10 slow FIFO WORD5 |
| 0x257 | [15:0] | X | R/W | STAGE10_SF_WORD6 | STAGE10 slow FIFO WORD6 |
| 0x258 | [15:0] | X | R/W | STAGE10_SF_WORD7 | STAGE10 slow FIFO WORD7 |
| 0x259 | [15:0] | X | R/W | STAGE10_SF_AMBIENT | STAGE10 slow FIFO ambient value |
| 0x25A | [15:0] | X | R/W | STAGE10_FF_AVG | STAGE10 fast FIFO average value |
| 0x25B | [15:0] | X | R/W | STAGE10_PEAK_DETECT_WORD0 | STAGE10 peak FIFO WORD0 value |
| 0x25C | [15:0] | X | R/W | STAGE10_PEAK_DETECT_WORD1 | STAGE10 peak FIFO WORD1 value |
| 0x25D | [15:0] | X | R/W | STAGE10_MAX_WORD0 | STAGE10 maximum value FIFO WORD0 |
| 0x25E | [15:0] | X | R/W | STAGE10_MAX_WORD1 | STAGE10 maximum value FIFO WORD1 |
| 0x25F | [15:0] | X | R/W | STAGE10_MAX_WORD2 | STAGE10 maximum value FIFO WORD2 |
| 0x260 | [15:0] | X | R/W | STAGE10_MAX_WORD3 | STAGE10 maximum value FIFO WORD3 |
| 0x261 | [15:0] | X | R/W | STAGE10_MAX_AVG | STAGE10 average maximum FIFO value |
| 0x262 | [15:0] | X | R/W | STAGE10_HIGH_THRESHOLD | STAGE10 high threshold value |
| 0x263 | [15:0] | X | R/W | STAGE10_MAX_TEMP | STAGE10 temporary maximum value |
| 0x264 | [15:0] | X | R/W | STAGE10_MIN_WORD0 | STAGE10 minimum value FIFO WORD0 |
| 0x265 | [15:0] | X | R/W | STAGE10_MIN_WORD1 | STAGE10 minimum value FIFO WORD1 |
| 0x266 | [15:0] | X | R/W | STAGE10_MIN_WORD2 | STAGE10 minimum value FIFO WORD2 |
| 0x267 | [15:0] | X | R/W | STAGE10_MIN_WORD3 | STAGE10 minimum value FIFO WORD3 |
| 0x268 | [15:0] | X | R/W | STAGE10_MIN_AVG | STAGE10 average minimum FIFO value |
| 0x269 | [15:0] | X | R/W | STAGE10_LOW_THRESHOLD | STAGE10 low threshold value |
| 0x26A | [15:0] | X | R/W | STAGE10_MIN_TEMP | STAGE10 temporary minimum value |
| 0x26B | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

**Table 51. STAGE11 Results Registers**

| Address | Data Bit | Default Value[1] | Type | Name | Description |
|---|---|---|---|---|---|
| 0x26C | [15:0] | X | R/W | STAGE11_CONV_DATA | STAGE11 CDC 16-bit conversion data (copy of CDC_RESULT_S11 register) |
| 0x26D | [15:0] | X | R/W | STAGE11_FF_WORD0 | STAGE11 fast FIFO WORD0 |
| 0x26E | [15:0] | X | R/W | STAGE11_FF_WORD1 | STAGE11 fast FIFO WORD1 |
| 0x26F | [15:0] | X | R/W | STAGE11_FF_WORD2 | STAGE11 fast FIFO WORD2 |
| 0x270 | [15:0] | X | R/W | STAGE11_FF_WORD3 | STAGE11 fast FIFO WORD3 |
| 0x271 | [15:0] | X | R/W | STAGE11_FF_WORD4 | STAGE11 fast FIFO WORD4 |
| 0x272 | [15:0] | X | R/W | STAGE11_FF_WORD5 | STAGE11 fast FIFO WORD5 |
| 0x273 | [15:0] | X | R/W | STAGE11_FF_WORD6 | STAGE11 fast FIFO WORD6 |
| 0x274 | [15:0] | X | R/W | STAGE11_FF_WORD7 | STAGE11 fast FIFO WORD7 |
| 0x275 | [15:0] | X | R/W | STAGE11_SF_WORD0 | STAGE11 slow FIFO WORD0 |
| 0x276 | [15:0] | X | R/W | STAGE11_SF_WORD1 | STAGE11 slow FIFO WORD1 |
| 0x277 | [15:0] | X | R/W | STAGE11_SF_WORD2 | STAGE11 slow FIFO WORD2 |
| 0x278 | [15:0] | X | R/W | STAGE11_SF_WORD3 | STAGE11 slow FIFO WORD3 |
| 0x279 | [15:0] | X | R/W | STAGE11_SF_WORD4 | STAGE11 slow FIFO WORD4 |
| 0x27A | [15:0] | X | R/W | STAGE11_SF_WORD5 | STAGE11 slow FIFO WORD5 |
| 0x27B | [15:0] | X | R/W | STAGE11_SF_WORD6 | STAGE11 slow FIFO WORD6 |
| 0x27C | [15:0] | X | R/W | STAGE11_SF_WORD7 | STAGE11 slow FIFO WORD7 |
| 0x27D | [15:0] | X | R/W | STAGE11_SF_AMBIENT | STAGE11 slow FIFO ambient value |
| 0x27E | [15:0] | X | R/W | STAGE11_FF_AVG | STAGE11 fast FIFO average value |
| 0x27F | [15:0] | X | R/W | STAGE11_PEAK_DETECT_WORD0 | STAGE11 peak FIFO WORD0 value |
| 0x280 | [15:0] | X | R/W | STAGE11_PEAK_DETECT_WORD1 | STAGE11 peak FIFO WORD1 value |
| 0x281 | [15:0] | X | R/W | STAGE11_MAX_WORD0 | STAGE11 maximum value FIFO WORD0 |
| 0x282 | [15:0] | X | R/W | STAGE11_MAX_WORD1 | STAGE11 maximum value FIFO WORD1 |
| 0x283 | [15:0] | X | R/W | STAGE11_MAX_WORD2 | STAGE11 maximum value FIFO WORD2 |
| 0x284 | [15:0] | X | R/W | STAGE11_MAX_WORD3 | STAGE11 maximum value FIFO WORD3 |
| 0x285 | [15:0] | X | R/W | STAGE11_MAX_AVG | STAGE11 average maximum FIFO value |
| 0x286 | [15:0] | X | R/W | STAGE11_HIGH_THRESHOLD | STAGE11 high threshold value |
| 0x287 | [15:0] | X | R/W | STAGE11_MAX_TEMP | STAGE11 temporary maximum value |
| 0x288 | [15:0] | X | R/W | STAGE11_MIN_WORD0 | STAGE11 minimum value FIFO WORD0 |
| 0x289 | [15:0] | X | R/W | STAGE11_MIN_WORD1 | STAGE11 minimum value FIFO WORD1 |
| 0x28A | [15:0] | X | R/W | STAGE11_MIN_WORD2 | STAGE11 minimum value FIFO WORD2 |
| 0x28B | [15:0] | X | R/W | STAGE11_MIN_WORD3 | STAGE11 minimum value FIFO WORD3 |
| 0x28C | [15:0] | X | R/W | STAGE11_MIN_AVG | STAGE11 average minimum FIFO value |
| 0x28D | [15:0] | X | R/W | STAGE11_LOW_THRESHOLD | STAGE11 low threshold value |
| 0x28E | [15:0] | X | R/W | STAGE11_MIN_TEMP | STAGE11 temporary minimum value |
| 0x28F | [15:0] | X | R/W | Unused | Set to 0 |

[1] X = don't care.

# OUTLINE DIMENSIONS

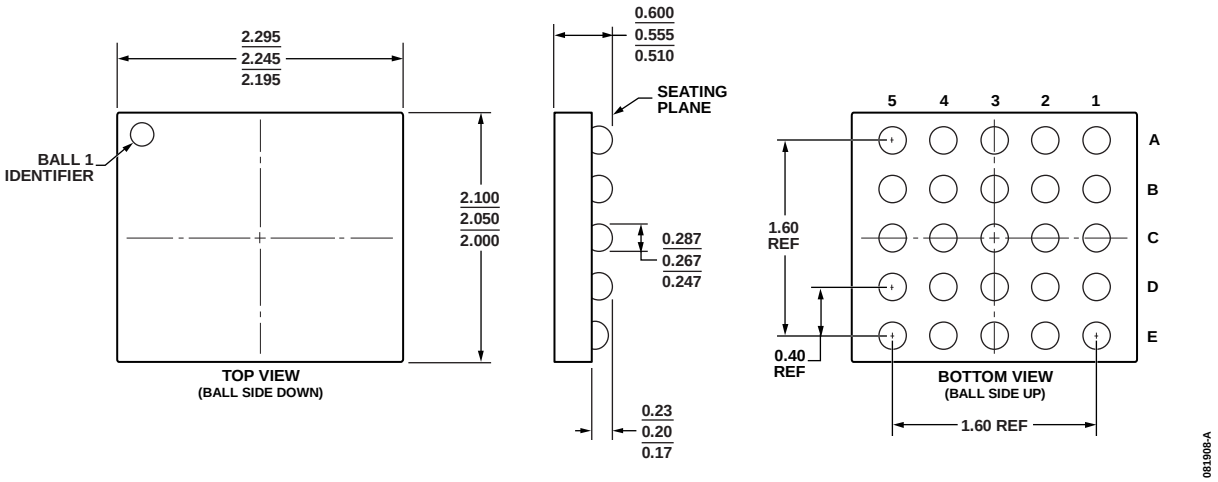



*Figure 62. 25-Ball Wafer Level Chip Scale Package [WLCSP]*
*(CB-25-3)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model | Temperature Range | Description | Serial Interface Description | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|
| AD7147AACBZ-RL[1, 2] | −40°C to +85°C | Wake-up on proximity | SPI Interface | 25-Ball WLCSP | CB-25-3 | T3K |
| AD7147AACBZ500RL7[1, 2] | −40°C to +85°C | Wake-up on proximity | SPI Interface | 25-Ball WLCSP | CB-25-3 | T3K |
| AD7147A-1ACBZ-RL[1, 2] | −40°C to +85°C | Wake-up on proximity | I²C Interface | 25-Ball WLCSP | CB-25-3 | T3J |
| AD7147A-1ACBZ500RL7[1, 2] | −40°C to +85°C | Wake-up on proximity | I²C Interface | 25-Ball WLCSP | CB-25-3 | T3J |
| EVAL-AD7147EBZ[1] | | | SPI Interface | Evaluation Board | | |
| EVAL-AD7147-1EBZ[1] | | | I²C Interface | Evaluation Board | | |

[1] Z = RoHS Compliant Part.
[2] This package is halide free.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View AD7147AACBZ-RL on WIN SOURCE
- Analog Devices Inc. Information

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