THE DATASHEET OF

AD5061YRJZ-1500RL7

16-Bit V_{OUT}, *nano*DAC, SPI Interface, 2.7 V to 5.5 V in an SOT-23

Data Sheet **AD5061**

FEATURES

- Single 16-bit digital-to-analog converter (DAC), 4 LSB INL
- Power-on reset to midscale or zero-scale
- Guaranteed monotonic by design
- 3 power-down functions
- Low power serial interface with Schmitt triggered inputs
- Small 8-lead SOT-23 package, low power
- Fast settling time of 4 µs typically
- 2.7 V to 5.5 V power supply
- Low glitch on power-up
- $\overline{\text{SYNC}}$ interrupt facility

APPLICATIONS

- Process control
- Data acquisition systems
- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources
- Programmable attenuators

GENERAL DESCRIPTION

The AD5061, a member of the Analog Devices, Inc., *nano*DAC™ family, is a low power, single 16-bit buffered voltage-out DAC that operates from a single 2.7 V to 5.5 V supply. The device offers a relative accuracy specification of ±4 LSB and operation is guaranteed monotonic with a ±1 LSB DNL specification. The device uses a versatile 3-wire serial interface that operates at clock rates up to 30 MHz, and is compatible with standard SPI, QSPI™, MICROWIRE, and DSP interface standards. The reference for the AD5061 is supplied from an external V_{REF} pin. A reference buffer is also provided on-chip. The device incorporates a power-on reset circuit that ensures the DAC output powers up to mid-scale or zero scale and remains there until a valid write takes place to the device. The device contains a power-down feature that reduces the current consumption of the device to typically 330 nA at 5 V and provides software-selectable output loads while in power-down mode. The device is put into power-down mode over the serial interface. Total unadjusted error for the device is <3 mV. This device exhibits very low glitch on power-up.

FUNCTIONAL BLOCK DIAGRAM

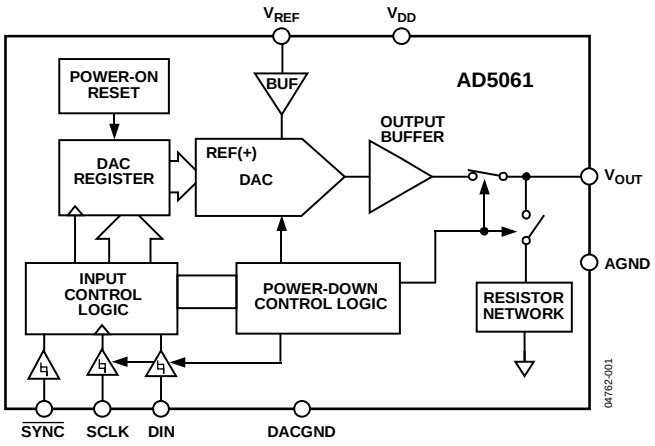

Figure 1.

Table 1. Related Devices

Part No.	Description
AD5062	2.7 V to 5.5 V, 16-bit *nano*DAC converter, 1 LSB INL, SOT-23
AD5063	2.7 V to 5.5 V, 16-bit *nano*DAC converter, 1 LSB INL, MSOP
AD5040/AD5060	2.7 V to 5.5 V, 14-bit/16-bit *nano*DAC converter, 1 LSB INL, SOT-23

PRODUCT HIGHLIGHTS

1. Available in a small 8-lead SOT-23 package.
2. 16-bit resolution, 4 LSB INL.
3. Low glitch on power-up.
4. High speed serial interface with clock speeds up to 30 MHz.
5. Three power-down modes available to the user.
6. Reset to known output voltage (midscale or zero scale).

Rev. E
Document Feedback

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7/2005—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 5.5 V, V_{REF} = 4.096 V, R_L = unloaded, C_L = unloaded, and T_{MIN} to T_{MAX}, unless otherwise specified.

Table 2.

Parameter	B Grade[1] Min	Typ	Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution	16			Bits	
Relative Accuracy (INL)[2]		±0.5	±4	LSB	−40°C to +85°C, B grade
		±0.5	±4	LSB	−40°C to +125°C, Y grade
Total Unadjusted Error (TUE)		±0.5	±3.0	mV	−40°C to +85°C, B grade
		±0.5	±3.0	mV	−40°C to +125°C, Y grade
Differential Nonlinearity (DNL)		±0.5	±1	LSB	Guaranteed monotonic, −40°C to +85°C, B grade
		±0.5	±1	LSB	Guaranteed monotonic, −40°C to +125°C, Y grade
Gain Error		±0.01	±0.05	% of FSR	T_A = −40°C to +85°C, B grade
		±0.01	±0.05	% of FSR	T_A = −40°C to +125°C , Y grade
Gain Error Temperature Coefficient		1		ppm of FSR/°C	
Offset Error		±0.02	±3.0	mV	T_A = −40°C to + 85°C, B grade
		±0.02	±3.0	mV	T_A = −40°C to + 125°C, Y grade
Offset Error Temperature Coefficient		0.5		µV/°C	
Full-Scale Error		±0.05	±3.0	mV	All 1s loaded to DAC register, T_A = −40°C to +85°C, B grade
		±0.05	±3.0	mV	All 1s loaded to DAC register, T_A = −40°C to +125°C , Y grade
OUTPUT CHARACTERISTICS[3]					
Output Voltage Range	0		V_{REF}	V	
Output Voltage Settling Time		4		µs	¼ scale to ¾ scale code transition to ±1 LSB, R_L = 5 kΩ
Output Noise Spectral Density		64		nV/√Hz	DAC code = midscale, 1 kHz
Output Voltage Noise		6		µV p-p	DAC code = midscale , 0.1 Hz to 10 Hz bandwidth
Digital to Analog Glitch Impulse		2		nV-s	1 LSB change around major carry, R_L = 5 KΩ
Digital Feedthrough		0.003		nV-s	DAC code = full-scale
DC Output Impedance (Normal)		0.015		Ω	Output impedance tolerance ±10%
DC Output Impedance (Power-Down)					
(Output Connected to 1 kΩ Network)		1		kΩ	Output impedance tolerance ±400 Ω
(Output Connected to 100 kΩ Network)		100		kΩ	Output impedance tolerance ±20 kΩ
Capacitive Load Stability			1	nF	Loads used: R_L = 5 kΩ, R_L = 100 kΩ, R_L = ∞
Output Slew Rate		1.2		V/µs	¼ scale to ¾ scale code transition to ±1 LSB, R_L = 5 kΩ, C_L = 200 pF
Short-Circuit Current		60		mA	DAC code = full-scale, output shorted to GND, T_A = 25°C
		45		mA	DAC code = zero-scale, output shorted to V_{DD}, T_A = 25°C
DAC Power-Up Time		4.5		µs	Time to exit power-down mode to normal mode of AD5061, 24th clock edge to 90% of DAC final value, output unloaded
DC Power Supply Rejection Ratio		−92		dB	V_{DD} ± 10%, DAC code = full-scale
Wideband Spurious-Free Dynamic Range		−67		dB	Output frequency = 10 kHz
REFERENCE INPUT/OUTPUT					
V_{REF} Input Range[4]	2		V_{DD} − 50	mV	
Input Current (Power-Down)		±0.1		µA	Zero-scale loaded
Input Current (Normal)			±0.5	µA	
DC Input Impedance		1		MΩ	

Parameter	B Grade[1] Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS					
Input Current[5]		±1	±5	μA	
Input Low Voltage (V_{IL})			0.8	V	V_{DD} = 4.5 V to 5.5 V
			0.8	V	V_{DD} = 2.7 V to 3.6 V
Input High Voltage (V_{IH})	2.0			V	V_{DD} = 2.7 V to 5.5 V
	1.8			V	V_{DD} = 2.7 V to 3.6 V
Pin Capacitance		4		pF	
POWER REQUIREMENTS					
V_{DD}	2.7		5.5	V	All digital inputs at 0 V or V_{DD}
I_{DD} (Normal Mode)					DAC active and excluding load current
V_{DD} = 2.7 V to 5.5 V		1.0	1.2	mA	$V_{IN} = V_{DD}$ and V_{IL} = GND, V_{DD} = 5.5 V, V_{REF} = 4.096 V, code = midscale
		0.89		mA	$V_{IN} = V_{DD}$ and V_{IL} = GND, V_{DD} = 3.0 V, V_{REF} = 4.096 V, code = midscale
I_{DD} (All Power-Down Modes)					
V_{DD} = 2.5 V to 5.5 V			1	μA	$V_{IH} = V_{DD}$ and V_{IL} = GND, V_{DD} = 5.5 V, V_{REF} = 4.096 V, code = midscale
		0.265		μA	$V_{IH} = V_{DD}$ and V_{IL} = GND, V_{DD} = 3.0 V, V_{REF} = 4.096 V, code = midscale

[1] Temperature range for B grade: −40°C to +85°C, typical at 25°C; temperature range for Y grade: −40°C to +125°C.
[2] Linearity calculated using a reduced code range (160 to 65535).
[3] Guaranteed by design and characterization, not production tested.
[4] The typical output supply headroom performance for various reference voltages at −40°C can be seen in Figure 27.
[5] Total current flowing into all pins.

TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, all specifications T_{MIN} to T_{MAX}, unless otherwise specified. All input signals are specified with $t_R = t_F$ = 1 ns/V (10% to 90% of V_{DD}) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.

Table 3.

Parameter	Limit	Unit	Test Conditions/Comments
t_1[1]	33	ns min	SCLK cycle time
t_2	5	ns min	SCLK high time
t_3	3	ns min	SCLK low time
t_4	10	ns min	$\overline{\text{SYNC}}$ to SCLK falling edge set-up time
t_5	3	ns min	Data set-up time
t_6	2	ns min	Data hold time
t_7	0	ns min	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge
t_8	12	ns min	Minimum $\overline{\text{SYNC}}$ high time
t_9	9	ns min	$\overline{\text{SYNC}}$ rising edge to next SCLK fall ignore

[1] Maximum SCLK frequency is 30 MHz.

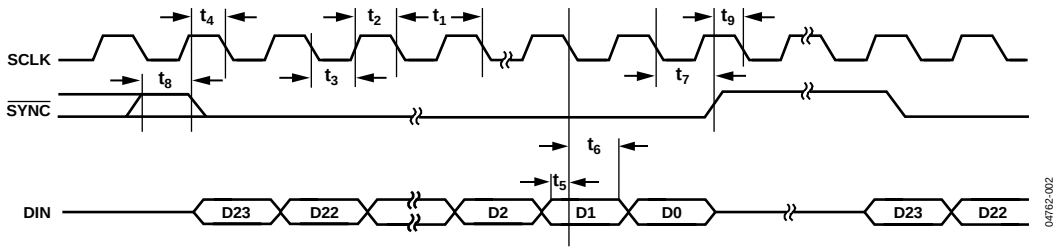


Figure 2. Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7.0 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REF} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Grade)	−40°C to + 85°C
Extended Automotive Temperature Range (Y Grade)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Junction Temperature	150°C
Power Dissipation	$(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Impedance	
θ_{JA}	206°C/W
θ_{JC}	44°C/W
Reflow Soldering (Pb-Free)	
Peak Temperature	260°C
Time at Peak Temperature	10 sec to 40 sec
Electrostatic Discharge (ESD)	1.5 kV

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

This device is a high performance integrated circuit with an ESD rating of <2 kV, and is ESD sensitive. Take proper precautions for handling and assembly.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

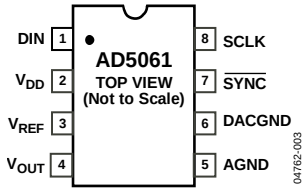


Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	DIN	Serial Data Input. This device has a 24-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.
2	V_{DD}	Power Supply Input. These devices can operate from 2.7 V to 5.5 V and V_{DD} must be decoupled to GND.
3	V_{REF}	Reference Voltage Input.
4	V_{OUT}	Analog Output Voltage from DAC.
5	AGND	Ground Reference Point for Analog Circuitry.
6	DACGND	Ground Input to the DAC.
7	$\overline{SYNC}$	Level Triggered Control Input (Active Low). This is the frame synchronization signal for the input data. When $\overline{SYNC}$ goes low, it enables the input shift register and data is transferred in on the falling edges of the following clocks. The DAC is updated following the 24th clock cycle unless $\overline{SYNC}$ is taken high before this edge, in which case the rising edge of $\overline{SYNC}$ acts as an interrupt and the write sequence is ignored by the DAC.
8	SCLK	Serial Clock Input. Data is clocked into the input shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 30 MHz.

TYPICAL PERFORMANCE CHARACTERISTICS

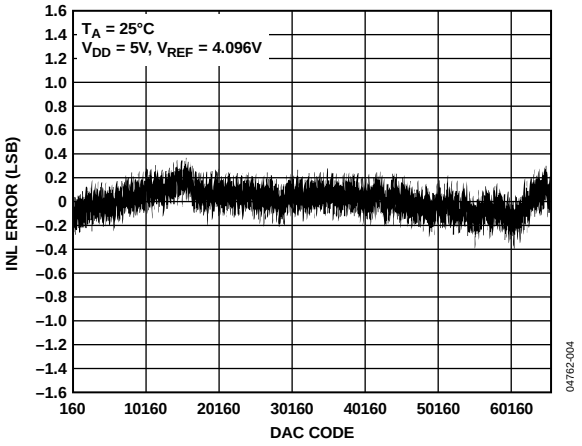


Figure 4. Typical INL Plot

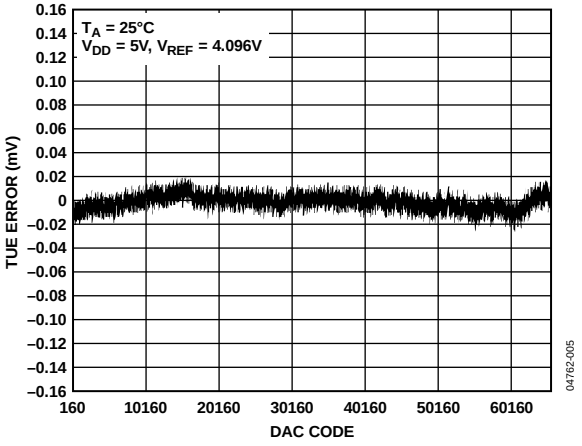


Figure 5. Typical TUE Plot

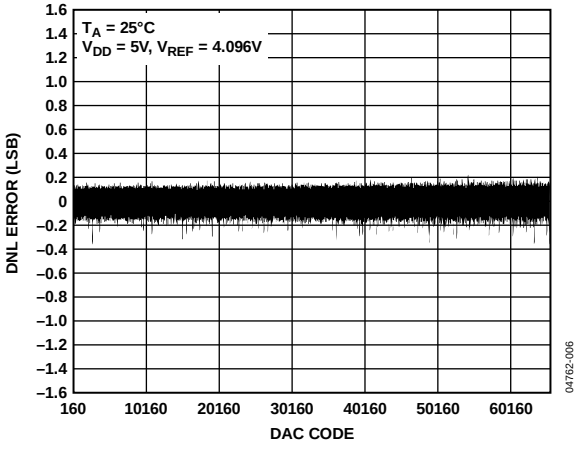


Figure 6. Typical DNL Plot

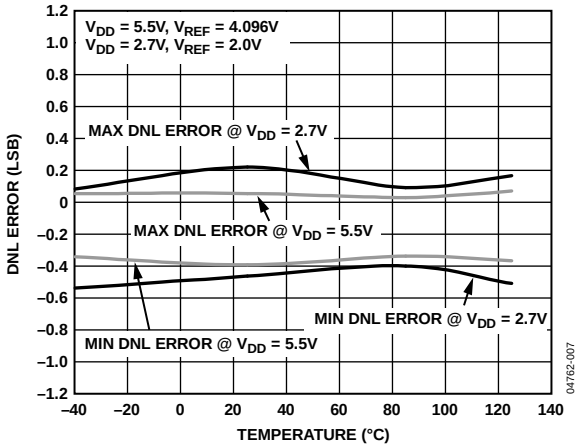


Figure 7. DNL vs. Temperature

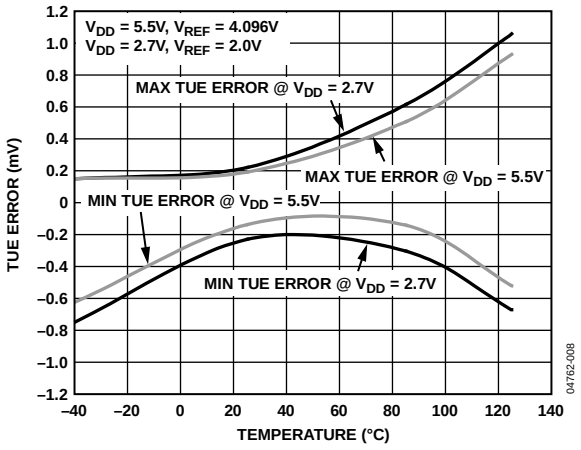


Figure 8. TUE vs. Temperature

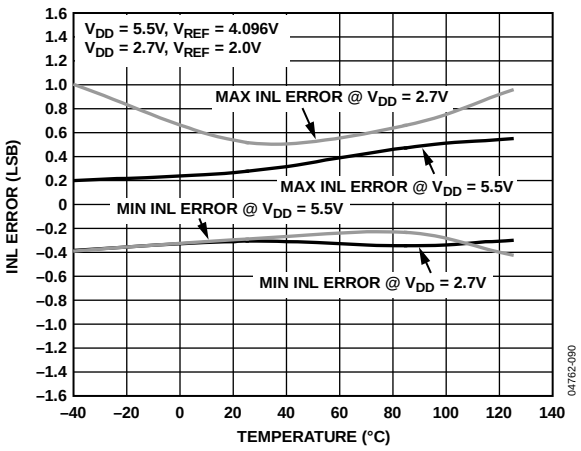


Figure 9. INL vs. Temperature

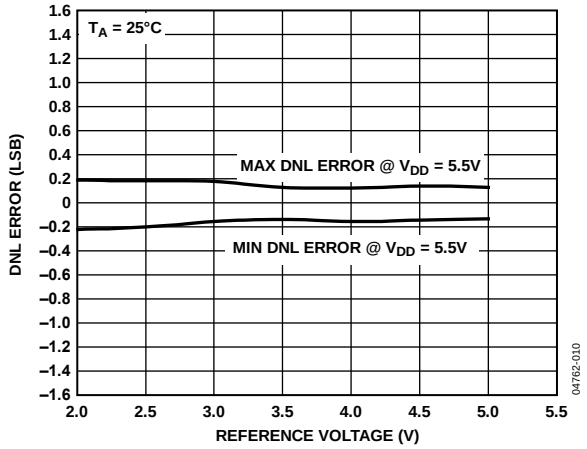


Figure 10. DNL vs. Reference Input Voltage

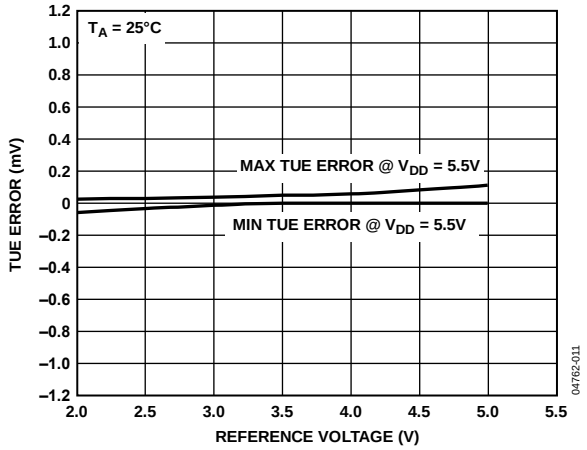


Figure 11. TUE vs. Reference Input Voltage

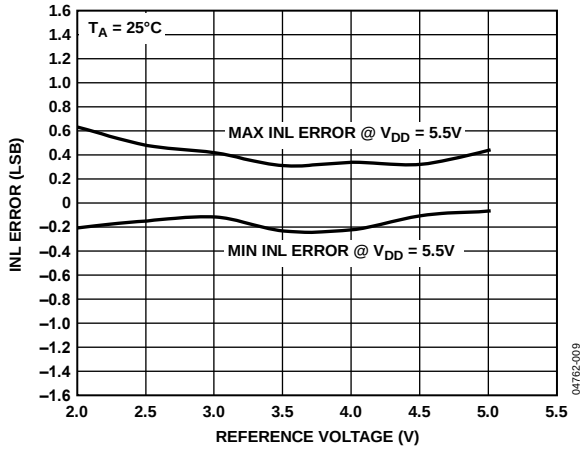


Figure 12. INL vs. Reference Input Voltage

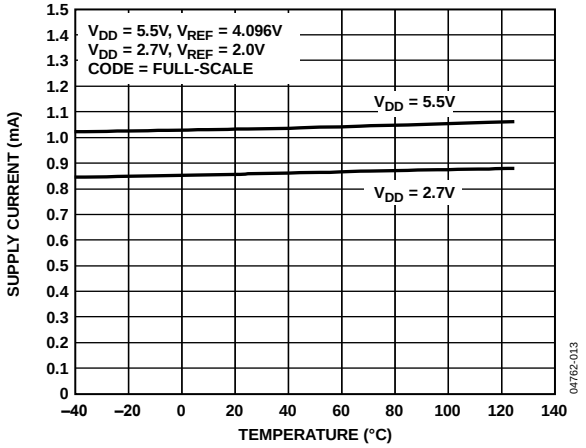


Figure 13. Supply Current vs. Temperature

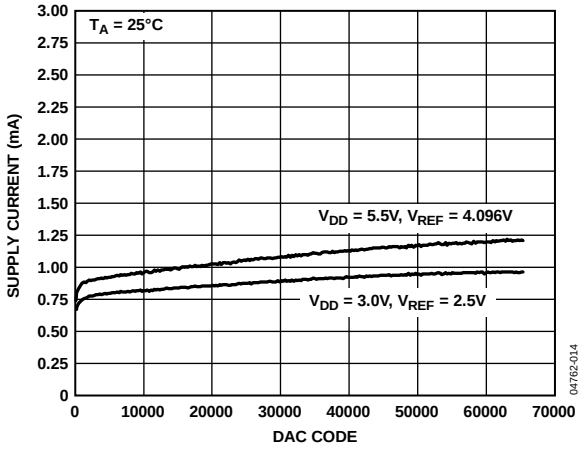


Figure 14. Supply Current vs. Digital Input Code

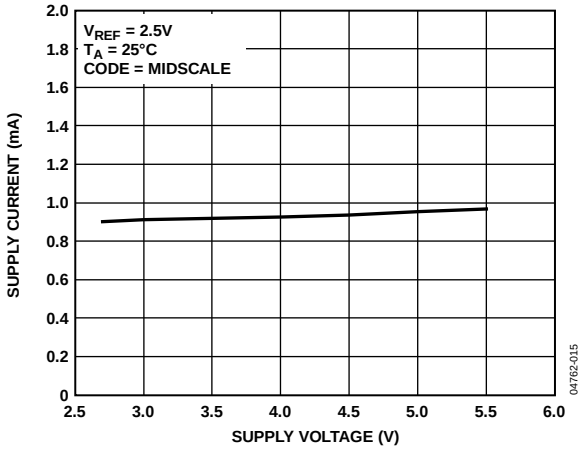


Figure 15. Supply Current vs. Supply Voltage

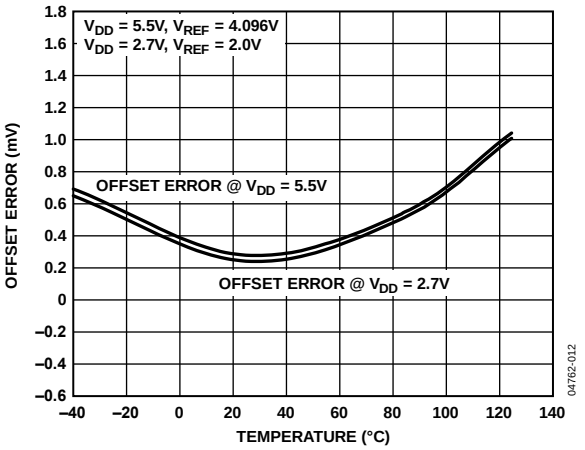


Figure 16. Offset vs. Temperature

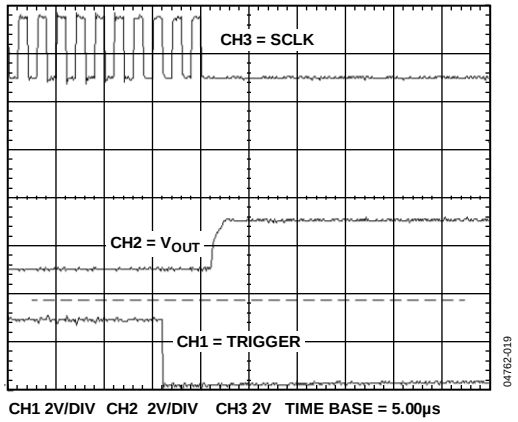


Figure 19. Exiting Power-Down Time to Midscale

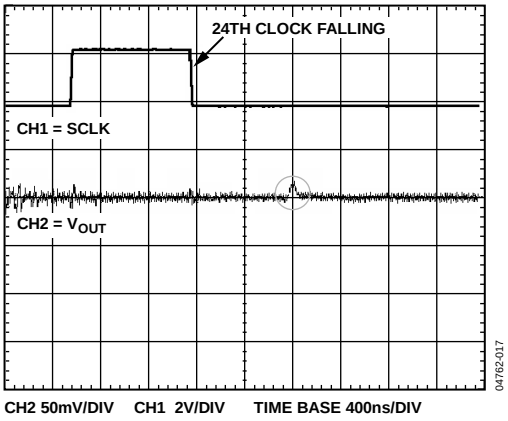


Figure 17. Digital to Analog Glitch Impulse, See Figure 21

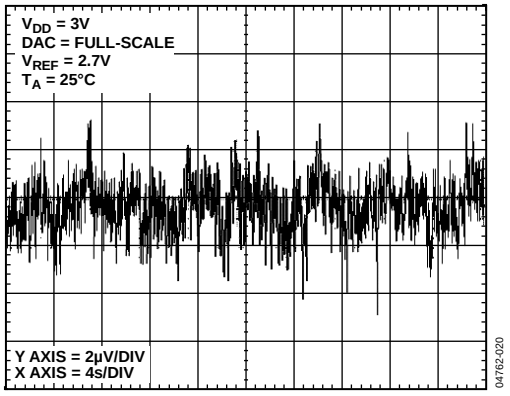


Figure 20. 0.1 Hz to 10 Hz Noise Plot

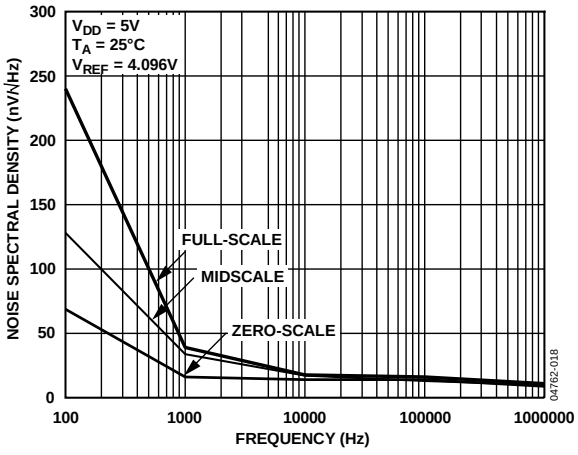


Figure 18. Output Noise Spectral Density

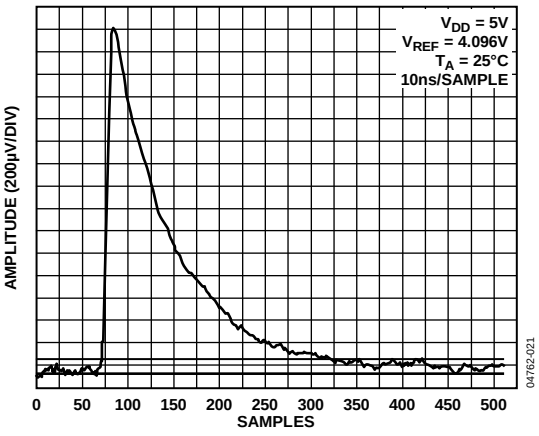


Figure 21. Glitch Energy

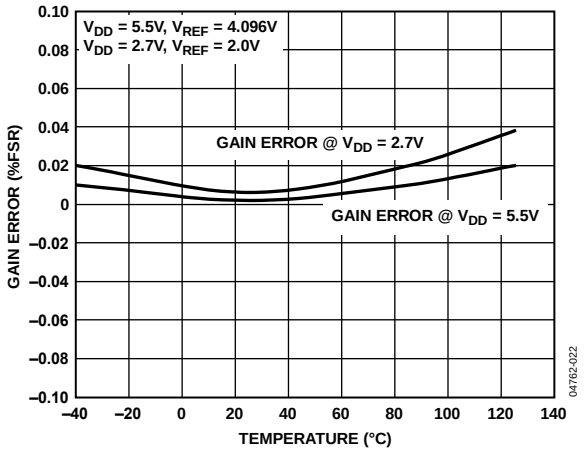


Figure 22. *Gain Error vs. Temperature*

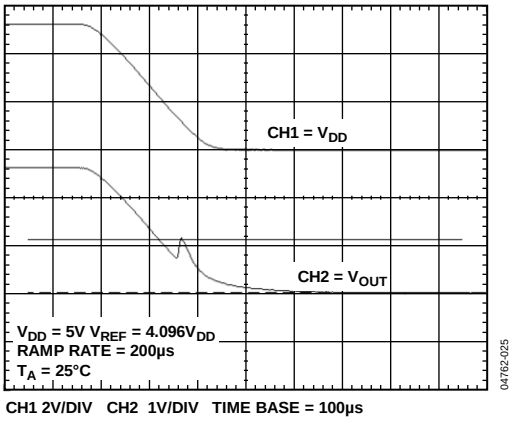


Figure 25. Hardware Power-Down Glitch

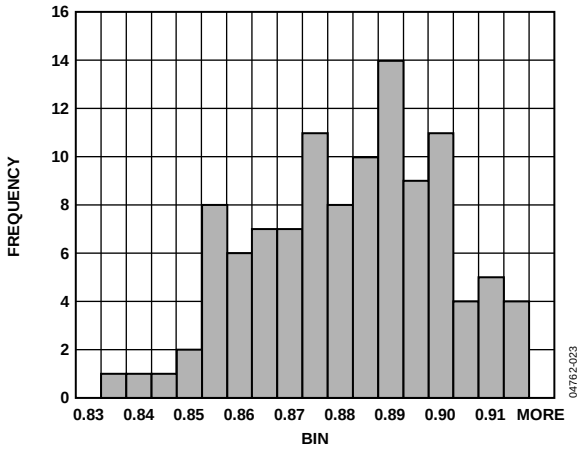


Figure 23. I_{DD} Histogram at V_{DD} = 3 V

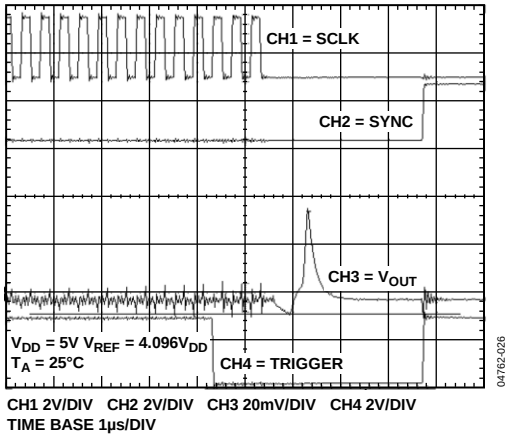


Figure 26. Exiting Software Power-Down Glitch

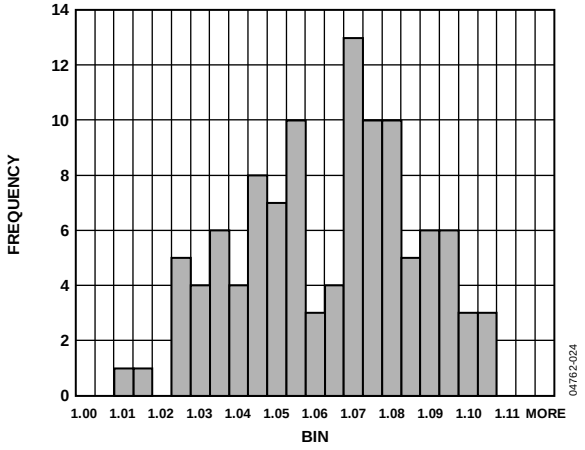


Figure 24. I_{DD} Histogram at V_{DD} = 5 V

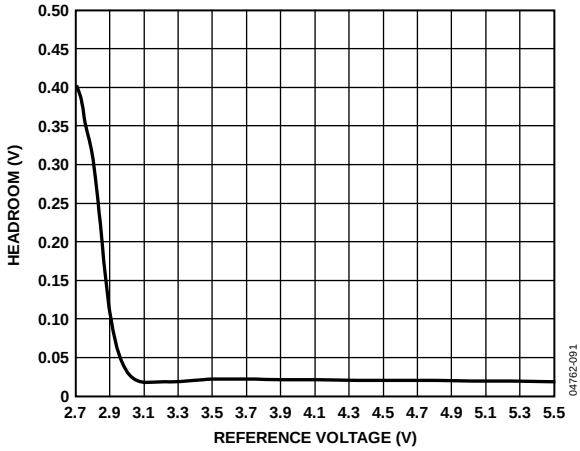


Figure 27. V_{DD} Headroom vs. Reference Voltage

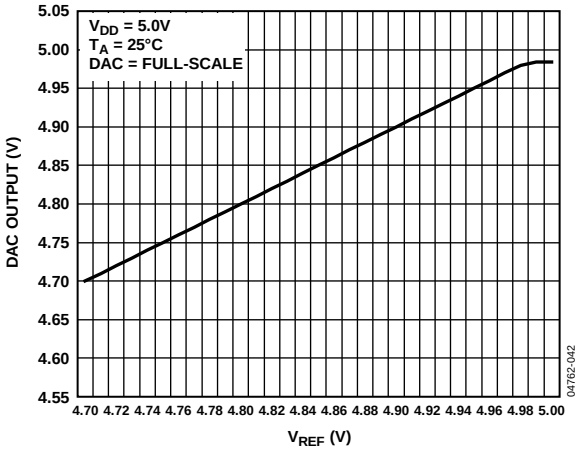


Figure 28. Typical Output Voltage vs. Reference Voltage

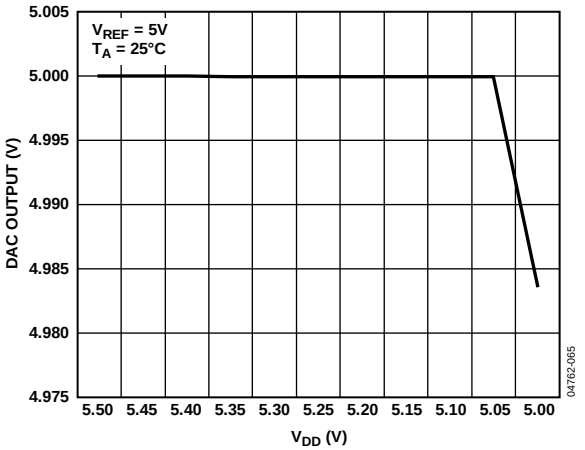


Figure 29. Typical Output Voltage vs. Supply Voltage

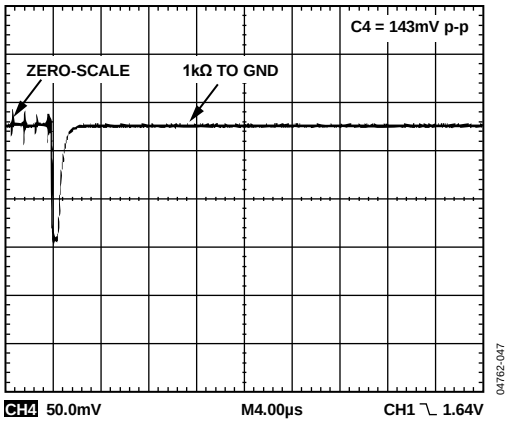


Figure 30. Typical Glitch upon Entering Software Power-Down to Zero-Scale

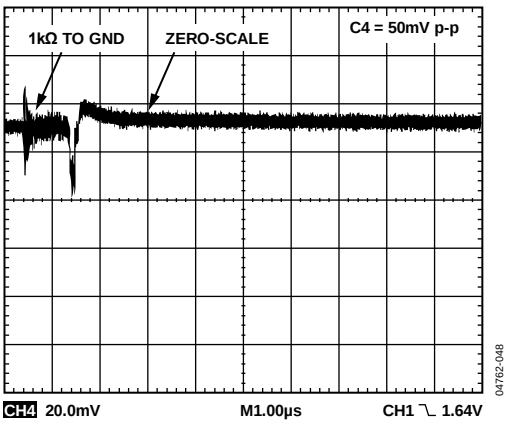


Figure 31. Typical Glitch upon Exiting Software Power-Down to Zero-Scale

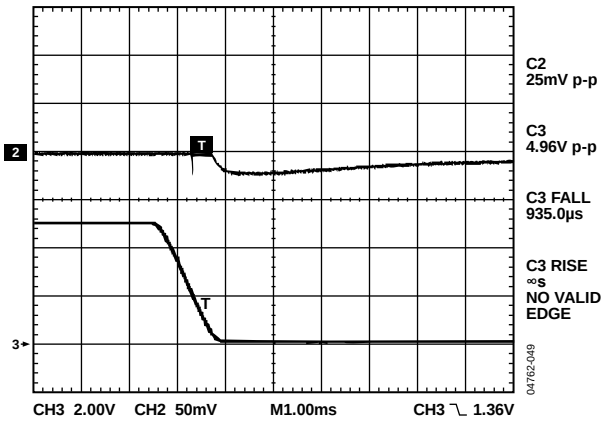


Figure 32. Typical Glitch upon Exiting Hardware Power-Down to Three State

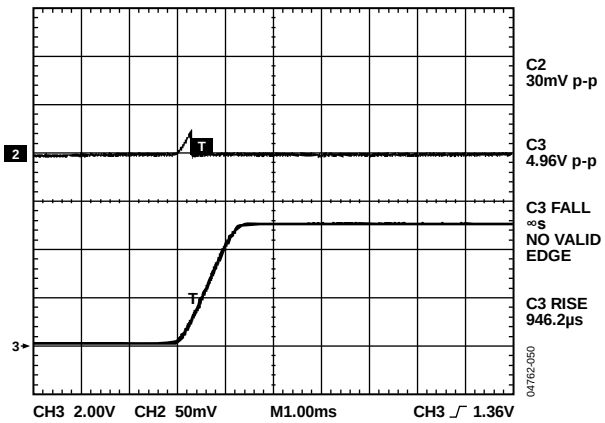


Figure 33. Typical Glitch upon Entering Hardware Power-Down to Zero-Scale

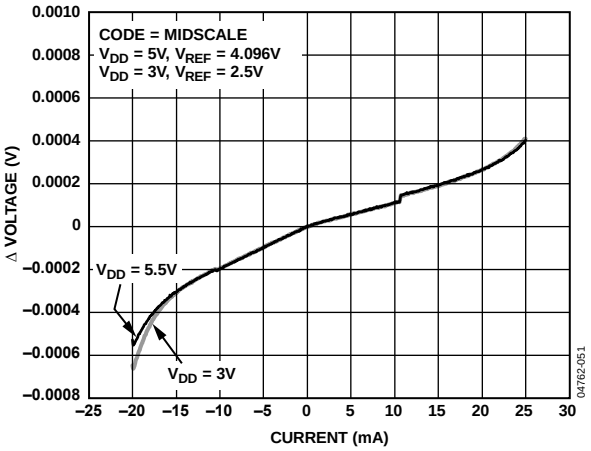


Figure 34. Typical Output Load Regulation

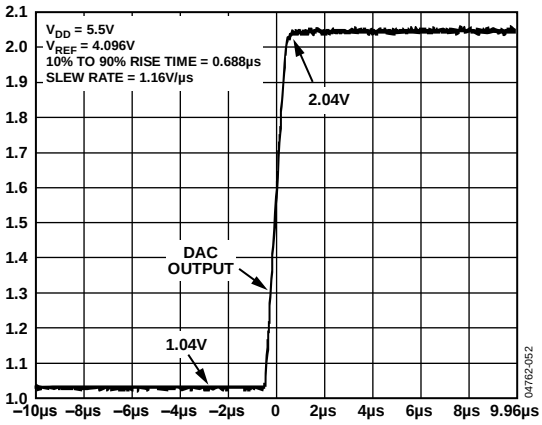


Figure 36. Typical Output Slew Rate

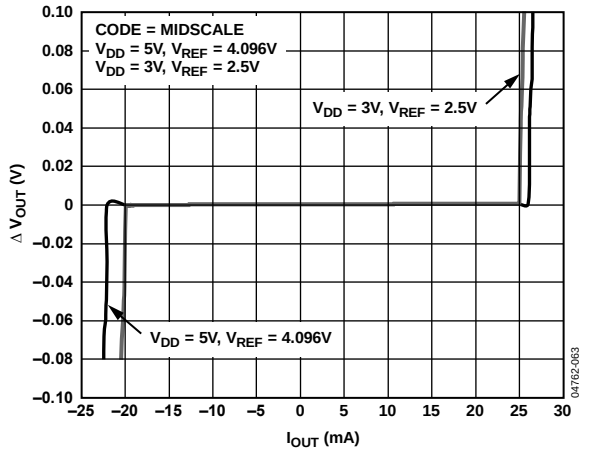


Figure 35. Typical Current Limiting Plot

TERMINOLOGY

Relative Accuracy (INL)
For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot is shown in Figure 4.

Differential Nonlinearity (DNL)
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical AD5061 DNL vs. code plot is shown in Figure 6.

Offset Error
Offset error is a measure of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output is 0 V. Offset error is expressed in mV.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded to the DAC register. Ideally, the output is V_{DD} − 1 LSB. Full-scale error is expressed in percent of full-scale range.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed as a percent of the full-scale range.

Total Unadjusted Error (TUE)
Total unadjusted error is a measure of the output error taking all the various errors into account. A typical TUE vs. code plot is shown in Figure 5.

Offset Error Temperature Coefficient
This is a measure of the change in offset error with a change in temperature. It is expressed in μV/°C.

Gain Error Temperature Coefficient
This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Digital to Analog Glitch Impulse
Digital to analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition; see Figure 17 and Figure 21. The expanded view in Figure 17 shows the glitch generated following completion of the calibration routine; Figure 21 zooms in on this glitch.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but is measured when the DAC output is not updated. It is specified in nV-s and measured with a full-scale code change on the data bus; that is, from all 0s to all 1s, and vice versa.

THEORY OF OPERATION

The AD5061 is a single 16-bit, serial input, voltage output DAC. It operates from supply voltages of 2.7 V to 5.5 V. Data is written to the AD5061 in a 24-bit word format, via a 3-wire serial interface.

The AD5061 incorporates a power-on reset circuit that ensures the DAC output powers up to zero-scale or midscale. The device also has a software power-down mode pin that reduces the typical current consumption to less than 1 µA.

DAC ARCHITECTURE

The DAC architecture of the AD5061 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 37. The four MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects one of 15 matched resistors to either DACGND or V_{REF} buffer output. The remaining 12 bits of the data word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

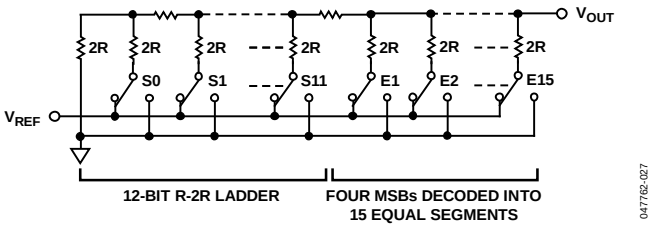


Figure 37. DAC Ladder Structure

REFERENCE BUFFER

The AD5061 operates with an external reference. The reference input (V_{REF}) has an input range of 2 V to V_{DD} − 50 mV. This input voltage is then used to provide a buffered reference for the DAC core.

SERIAL INTERFACE

The AD5061 has a 3-wire serial interface ($\overline{SYNC}$, SCLK, and DIN), which is compatible with SPI, QSPI, and MICROWIRE interface standards, as well as most DSPs. See Figure 2 for a timing diagram of a typical write sequence.

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line is clocked into the 24-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 30 MHz, making this device compatible with high speed DSPs. On the 24th falling clock edge, the last data bit is clocked in and the programmed function is executed (that is, a change in the DAC register contents and/or a change in the mode of operation).

At this stage, the $\overline{SYNC}$ line may be kept low or be brought high. In either case, it must be brought high for a minimum of 12 ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Because the $\overline{SYNC}$ buffer draws more current when V_{IH} = 1.8 V than it does when V_{IH} = 0.8 V, idle $\overline{SYNC}$ low between write sequences for an even lower power operation of the device. As previously indicated, however, it must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 24 bits wide; see Figure 38. PD1 and PD0 are control bits that control which mode of operation the device is in (normal mode or any one of three power-down modes). There is a more complete description of the various modes in the Power-Down Modes section. The next 16 bits are the data bits. These are transferred to the DAC register on the 24th falling edge of SCLK.

$\overline{SYNC}$ INTERRUPT

In a normal write sequence, the $\overline{SYNC}$ line is kept low for at least 24 falling edges of SCLK and the DAC is updated on the 24th falling edge. However, if $\overline{SYNC}$ is brought high before the 24th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs; see Figure 40.

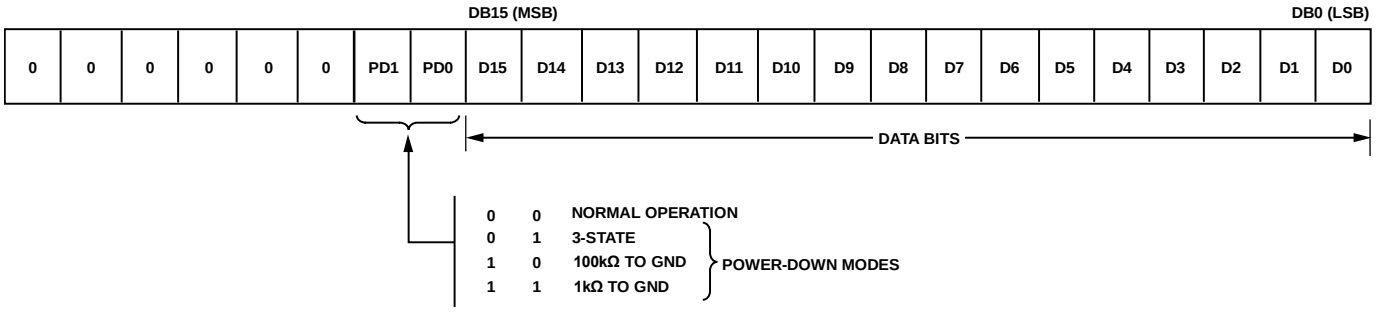


Figure 38. Input Register Contents

POWER-ON TO ZERO-SCALE OR MIDSCALE

The AD5061 contains a power-on reset circuit that controls the output voltage during power-up. The DAC register is filled with the zero-scale or midscale code and the output voltage is zero-scale or midscale. It remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

SOFTWARE RESET

The device can be put into software reset by setting all bits in the DAC register to 1; this includes writing 1s to Bit D23 to Bit D16, which is not the normal mode of operation. Note that the $\overline{\text{SYNC}}$ interrupt command cannot be performed if a software reset command is started.

POWER-DOWN MODES

The AD5061 contains four separate modes of operation. These modes are software-programmable by setting two bits (DB17 and DB16) in the control register. Table 6 shows how the state of the bits corresponds to the mode of operation of the device.

Table 6. Modes of Operation

DB17	DB16	Operating Mode
0	0	Normal operation
		Power-down mode:
0	1	3-state
1	0	100 kΩ to GND
1	1	1 kΩ to GND

When both bits are set to 0, the device works normally with its normal power consumption. However, for the three power-down modes, the supply current falls to less than 1 µA at 5 V (265 nA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the device is known while the device is in power-down mode. There are three different options. The output is connected internally to GND through a 1 kΩ resistor or a 100 kΩ resistor, or it is left open-circuited (3-state). The output stage is illustrated in Figure 39.

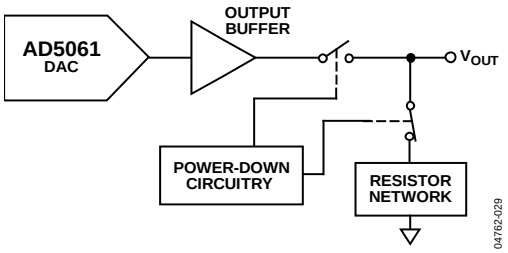


Figure 39. Output Stage During Power-Down

The bias generator, the DAC core and other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 2.5 µs for V_{DD} = 5 V, and 5 µs for V_{DD} = 3 V, see Figure 19.

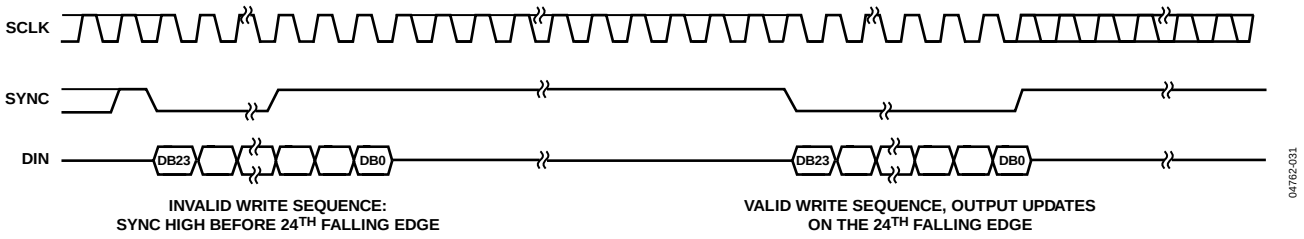
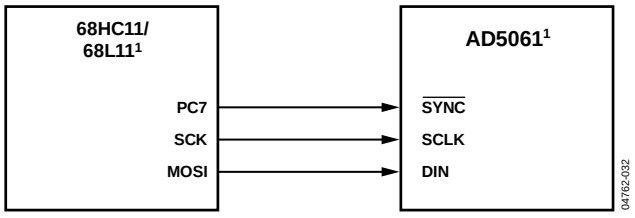


Figure 40. $\overline{\text{SYNC}}$ Interrupt Facility

MICROPROCESSOR INTERFACING

AD5061 to 68HC11/68L11 Interface

Figure 41 shows a serial interface between the AD5061 and the 68HC11/68L11 microcontroller. SCK of the 68HC11/68L11 drives the SCLK pin of the AD5061, while the MOSI output drives the serial data line of the DAC. The $\overline{\text{SYNC}}$ signal is derived from a port line (PC7). The set-up conditions for correct operation of this interface require that the 68HC11/68L11 be configured so that its CPOL bit is 0 and its CPHA bit is 1. When data is being transmitted to the DAC, the $\overline{\text{SYNC}}$ line is taken low (PC7). When the 68HC11/68L11 is configured where its CPOL bit is 0 and its CPHA bit is 1, data appearing on the MOSI output is valid on the falling edge of SCK. Serial data from the 68HC11/68L11 is transmitted in 8-bit bytes with only eight falling clock edges occurring in the transmit cycle. Data is transmitted MSB first. To load data to the AD5061, PC7 is left low after the first eight bits are transferred, a second serial write operation is performed to the DAC, and PC7 is taken high at the end of this procedure.

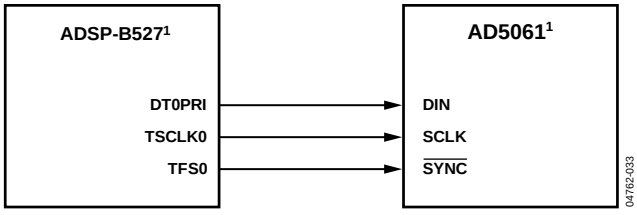


[1]ADDITIONAL PINS OMITTED FOR CLARITY

Figure 41. AD5061 to 68HC11/68L11 Interface

AD5061 to Blackfin® ADSP-BF527 Interface

Figure 42 shows a serial interface between the AD5061 and the Blackfin ADSP-BF527 microprocessor. The ADSP-BF527 processor incorporates two dual-channel synchronous serial ports, SPORT1 and SPORT0, for serial and multiprocessor communications. Using SPORT0 to connect to the AD5061, the setup for the interface is the following: DT0PRI drives the DIN pin of the AD5061, while TSCLK0 drives the SCLK of the device; the $\overline{\text{SYNC}}$ is driven from TFS0.

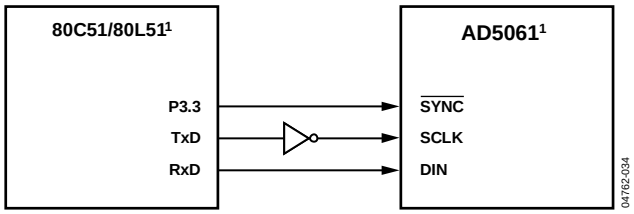


[1]ADDITIONAL PINS OMITTED FOR CLARITY

Figure 42. AD5061 to Blackfin ADSP-BF527 Interface

AD5061 to 80C51/80L51 Interface

Figure 43 shows a serial interface between the AD5061 and the 80C51/80L51 microcontroller. The setup for the interface is the following: TxD of the 80C51/80L51 drives SCLK of the AD5061 while RxD drives the serial data line of the device. The $\overline{\text{SYNC}}$ signal is again derived from a bit-programmable pin on the port. In this case, Port Line P3.3 is used. When data is transmitted to the AD5061, P3.3 is taken low. The 80C51/80L51 transmits data only in 8-bit bytes; thus only eight falling clock edges occur in the transmit cycle. To load data to the DAC, P3.3 is left low after the first eight bits are transmitted, and a second write cycle is initiated to transmit the second byte of data. P3.3 is taken high following the completion of this cycle. The 80C51/80L51 outputs the serial data in a format that has the LSB first. The AD5061 requires its data with the MSB as the first bit received. The 80C51/80L51 transmit routine must take this into account.

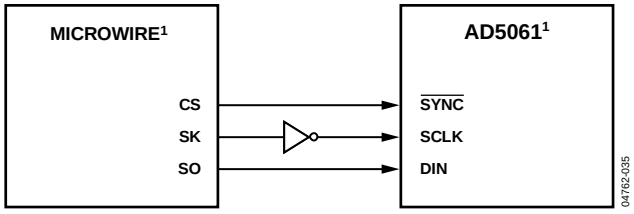


[1]ADDITIONAL PINS OMITTED FOR CLARITY

Figure 43. AD5061 to 80C51/80L51 Interface

AD5061 to MICROWIRE Interface

Figure 44 shows an interface between the AD5061 and any MICROWIRE-compatible device. Serial data is shifted out on the falling edge of the serial clock and is clocked into the AD5061 on the rising edge of the SK.



[1]ADDITIONAL PINS OMITTED FOR CLARITY

Figure 44. AD5061 to MICROWIRE Interface

APPLICATIONS INFORMATION

CHOOSING A REFERENCE

To achieve the optimum performance from the AD5061, give thought to the choice of a precision voltage reference. The AD5061 has just one reference input, V_{REF}. The voltage on the reference input is used to supply the positive input to the DAC. Therefore, any error in the reference is reflected in the DAC.

There are four possible sources of error when choosing a voltage reference for high accuracy applications: initial accuracy, ppm drift, long-term drift, and output voltage noise. Initial accuracy on the output voltage of the DAC results in a full-scale error in the DAC. To minimize these errors, a reference with high initial accuracy is preferred. In addition, choosing a reference with an output trim adjustment, such as the ADR435, allows a system designer to trim out system errors by setting a reference voltage to a voltage other than the nominal voltage. The trim adjustment can also be used at the operating temperature to trim out any errors.

Because the supply current required by the AD5061 is extremely low, the device is ideal for low supply applications. The ADR395 voltage reference is recommended. This voltage reference requires less than 100 µA of quiescent current and can, therefore, drive multiple DACs in one system, if required. This voltage reference also provides very good noise performance at 8 µV p-p in the 0.1 Hz to 10 Hz range.

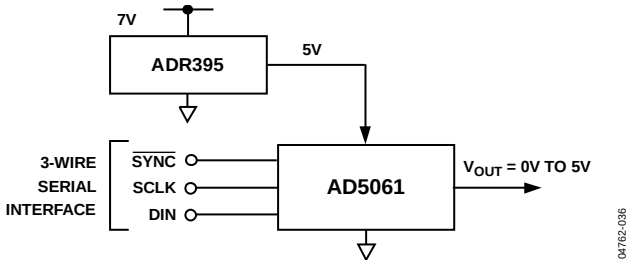


Figure 45. ADR395 as Reference to the AD5061

Long-term drift is a measure of how much the reference drifts over time. A reference with a tight long-term drift specification ensures that the overall solution remains relatively stable during its entire lifetime. The temperature coefficient of a reference output voltage affects INL, DNL, and TUE. Chose a reference with a tight temperature coefficient specification to reduce temperature dependence of the DAC output voltage on ambient conditions.

In high accuracy applications, which have a relatively low noise budget, reference output voltage noise must be considered. It is important to choose a reference with as low an output noise voltage as is practical for the system noise resolution required. Precision voltage references, such as the ADR435, produce low output noise in the 0.1 Hz to 10 Hz region.

Table 7. Precision References Device List for the AD5061

Part No.	Initial Accuracy (mV Maximum)	Temperature Drift (ppm/°C Maximum)	0.1 Hz to 10 Hz Noise (µV p-p Typical)
ADR435	±2	3 (8-lead SOIC_N)	8
ADR425	±2	3 (8-lead SOIC_N)	3.4
ADR02	±3	3 (8-lead SOIC_N)	10
ADR02	±3	3 (5-lead SC70)	10
ADR395	±5	9 (5-lead TSOT)	8

Table 7 shows examples of recommended precision references for use as a supply to the AD5061.

BIPOLAR OPERATION

The AD5061 is designed for single-supply operation, but a bipolar output range is also possible using the circuit shown in Figure 46. The circuit shown yields an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD8675/AD820/AD8032 or an OP196/OP295.

Calculate the output voltage for any input code as follows:

$$V_O = \left[V_{DD} \times \left(\frac{D}{65536} \right) \times \left(\frac{R1+R2}{R1} \right) - V_{DD} \times \left(\frac{R2}{R1} \right) \right]$$

where D represents the input code in decimal (0 to 65536).

With V_{REF} = 5 V, R1 = R2 = 10 kΩ,

$$V_O = \left(\frac{10 \times D}{65536} \right) - 5\,\text{V}$$

This equation results in an output voltage range of ±5 V with 0x0000 corresponding to a −5 V output and 0xFFFF corresponding to a +5 V output.

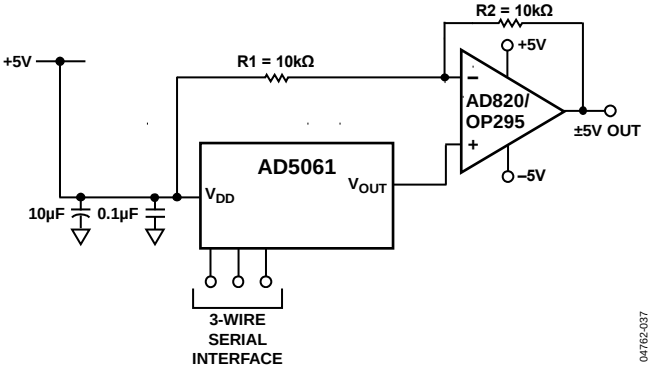


Figure 46. Bipolar Operation with the AD5061

USING A GALVANICALLY ISOLATED INTERFACE CHIP

In process control applications in industrial environments, it is often necessary to use a galvanically isolated interface to protect and isolate the controlling circuitry from any hazardous common-mode voltages that may occur in the area where the DAC is functioning. *i*Coupler® provides isolation in excess of 2.5 kV. Because the AD5061 uses a 3-wire serial logic interface, the ADuM1300 provides an ideal digital solution for the DAC interface.

The ADuM1300 isolator provides three independent isolation channels in a variety of channel configurations and data rates. It operates across the full range from 2.7 V to 5.5 V, providing compatibility with lower voltage systems and enabling a voltage translation functionality across the isolation barrier.

Figure 47 shows a typical galvanically isolated configuration using the AD5061. The power supply to the device also needs to be isolated; this is accomplished by using a transformer. On the DAC side of the transformer, a 5 V regulator provides the 5 V supply required for the AD5061.

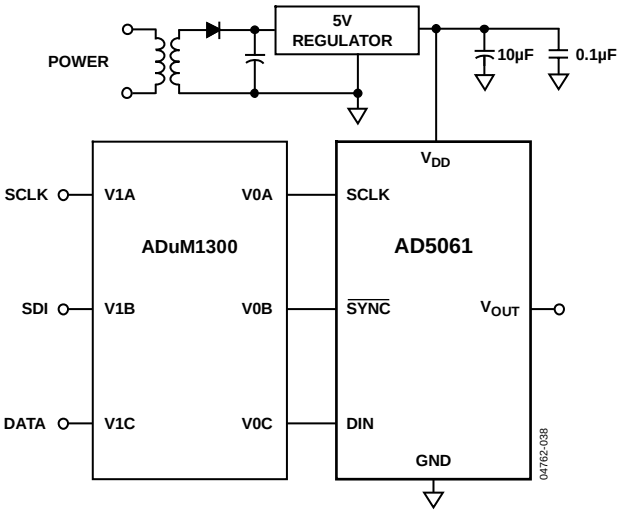


Figure 47. AD5061 with a Galvanically Isolated Interface

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5061 must have separate analog and digital sections, each having its own area of the board. If the AD5061 is in a system where other devices require an AGND to DGND connection, then the connection must be made at one point only. This ground point must be as close as possible to the AD5061.

The power supply to the AD5061 must be bypassed with 10 µF and 0.1 µF capacitors. The capacitors must be physically as close as possible to the device with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor has low effective series resistance (ESR) and effective series inductance (ESI), as do common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line itself must have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals must be shielded from other devices of the board by digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique where the component side of the board is dedicated to the ground plane only, and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

OUTLINE DIMENSIONS

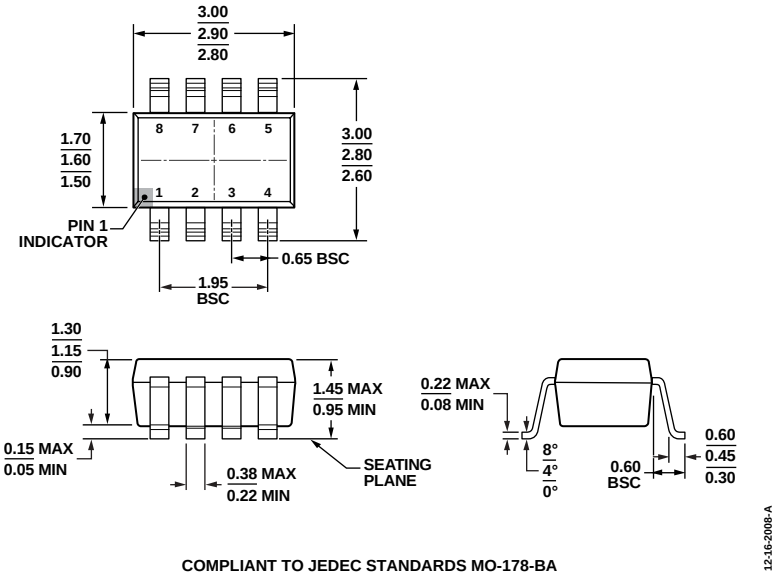


Figure 48. 8-Lead Small Outline Transistor Package [SOT-23]
(RJ-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1, 2]	Temperature Range	INL	Description	Package Description	Package Option	Marking Code
AD5061BRJZ-1500RL7	−40°C to +85°C	4 LSB	2.7 V to 5.5 V, Reset to 0 V	8-Lead SOT-23	RJ-8	D43
AD5061BRJZ-2REEL7	−40°C to +85°C	4 LSB	2.7 V to 5.5 V, Reset to Midscale	8-Lead SOT-23	RJ-8	D44
AD5061BRJZ-2500RL7	−40°C to +85°C	4 LSB	2.7 V to 5.5 V, Reset to Midscale	8-Lead SOT-23	RJ-8	D44
AD5061YRJZ-1500RL7	−40°C to +125°C	4 LSB	2.7 V to 5.5 V, Reset to 0 V	8-Lead SOT-23	RJ-8	D6G
AD5061YRJZ-1REEL7	−40°C to +125°C	4 LSB	2.7 V to 5.5 V, Reset to 0 V	8-Lead SOT-23	RJ-8	D6G
EVAL-AD5061SDZ				Evaluation Board		
EVAL-SDP-CB1Z				Evaluation Controller Board		

[1] Z = RoHS Compliant Part.
[2] The EVAL-AD5061SDZ and the EVAL-SDP-CB1Z must be used and ordered together.

Looking for pricing, stock, or lifecycle information?

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- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management