THE DATASHEET OF

EA512US

ACT512

Rev 4, 13-Feb-14

ActiveQR™ Quasi-Resonant PWM Controller

FEATURES

- **CCM and Quasi-Resonant Operation**
- **Adjustable up to 75kHz Switching Frequency**
- **OCP/OLP Protection**
- **Integrated Patented Frequency Foldback Technique**
- **Integrated Patented Line Compensation**
- **Built-in Soft-Start Circuit**
- **Line Under-Voltage, Thermal, Output Over-voltage, Output Short Protections**
- **Current Sense Resistor Short Protection**
- **Transformer Winding Short Protection**
- **100mW Standby Power**
- **Complies with Global Energy Efficiency and CEC Average Efficiency Standards**
- **Tiny SOT23-6 Packages**

APPLICATIONS

- **AC/DC Adaptors/Chargers for Cell Phones, Cordless Phone, PDAs, E-books**
- **Adaptors for Portable Media Player, DSCs, Set-top boxes, DVD players, records**
- **Linear Adapter Replacements**

GENERAL DESCRIPTION

The ACT512 is a high performance peak current mode PWM controller. ACT512 applies *ActiveQR*™ and frequency foldback technique to reduce EMI and improve efficiency. ACT512's maximum design switching frequency is set at 75kHz. Very low standby power, good dynamic response and accurate voltage regulation is achieved with an opto-coupler and the secondary side control circuit.

The idle mode operation enables low standby power of 100mW with small output voltage ripple. By applying frequency foldback and *ActiveQR*™ technology, ACT512 increases the average system efficiency compared to conventional solutions and exceeds the latest ES2.0 efficiency standard with good margin.

ACT512 integrates comprehensive protection. In case of over temperature, over voltage, winding short, current sense resistor short, open loop and overload conditions, it would enter into auto restart mode including Cycle-by-Cycle current limiting.

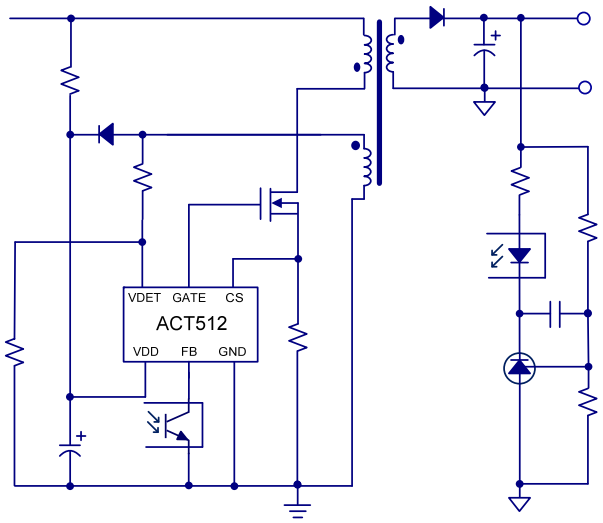
ACT512 is to achieve no overshoot and very short rise time even with a big capacitive load with the built-in fast and soft start process.

In full load condition, ACT512 is able to be designed to work in both CCM mode and DCM mode to meet different types of applications. Quasi-Resonant (QR) operation mode can improve efficiency during DCM operation, and reduce EMI and further reduce the components in input filter.

ACT512 is ideal for applications up to 60 Watts.

Figure 1:

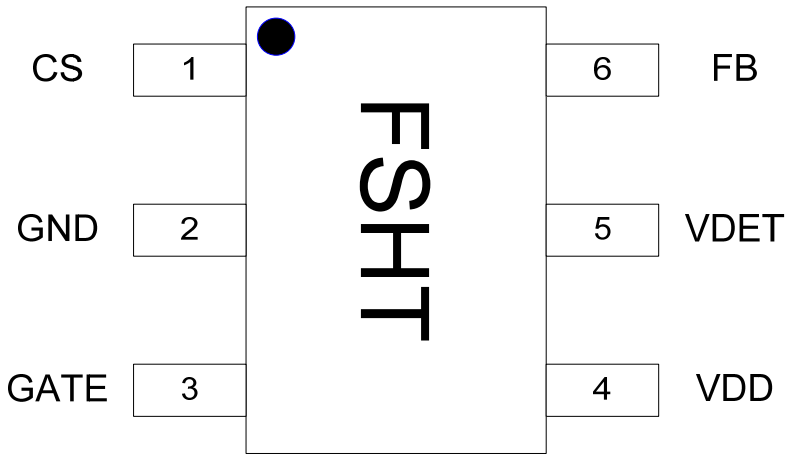
Simplified Application Circuit



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE	PINS	PACKING METHOD	TOP MARK
ACT512US-T	-40°C to 85°C	SOT23-6	6	TUBE & REEL	FSHT

PIN CONFIGURATION



SOT23-6
ACT512US

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CS	Current Sense Pin. Connect an external resistor (R_{CS}) between this pin and ground to set peak current limit for the primary switch.
2	GND	Ground.
3	GATE	Gate Drive. Gate driver for the external MOSFET transistor.
4	VDD	Power Supply. This pin provides bias power for the IC during startup and steady state operation.
5	VDET	Valley Detector Pin. Connect this pin to a resistor divider network from the auxiliary winding to detect zero-crossing points for valley turn on operation.
6	FB	Feedback Pin. Connect this pin to optocouplers's collector for output regulation.

ABSOLUTE MAXIMUM RATINGS①

PARAMETER	VALUE	UNIT
FB, CS, VDET to GND	-0.3 to + 6	V
VDD, GATE to GND	-0.3 to + 28	V
Maximum Power Dissipation (SOT23-6)	0.45	W
Operating Junction Temperature	-40 to 150	˚C
Junction to Ambient Thermal Resistance (θ_{JA})	220	˚C/W
Storage Temperature	-55 to 150	˚C
Lead Temperature (Soldering, 10 sec)	300	˚C

①: Do not exceed these limits to prevent damage to the device. Exposure to absolute maximum rating conditions for long periods.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 14V, L_M = 0.8mH, R_{CS} = 0.87Ω, V_{OUT} = 12V, N_P = 56, N_S =9, N_A =10, T_A = 25°C, unless otherwise specified.)

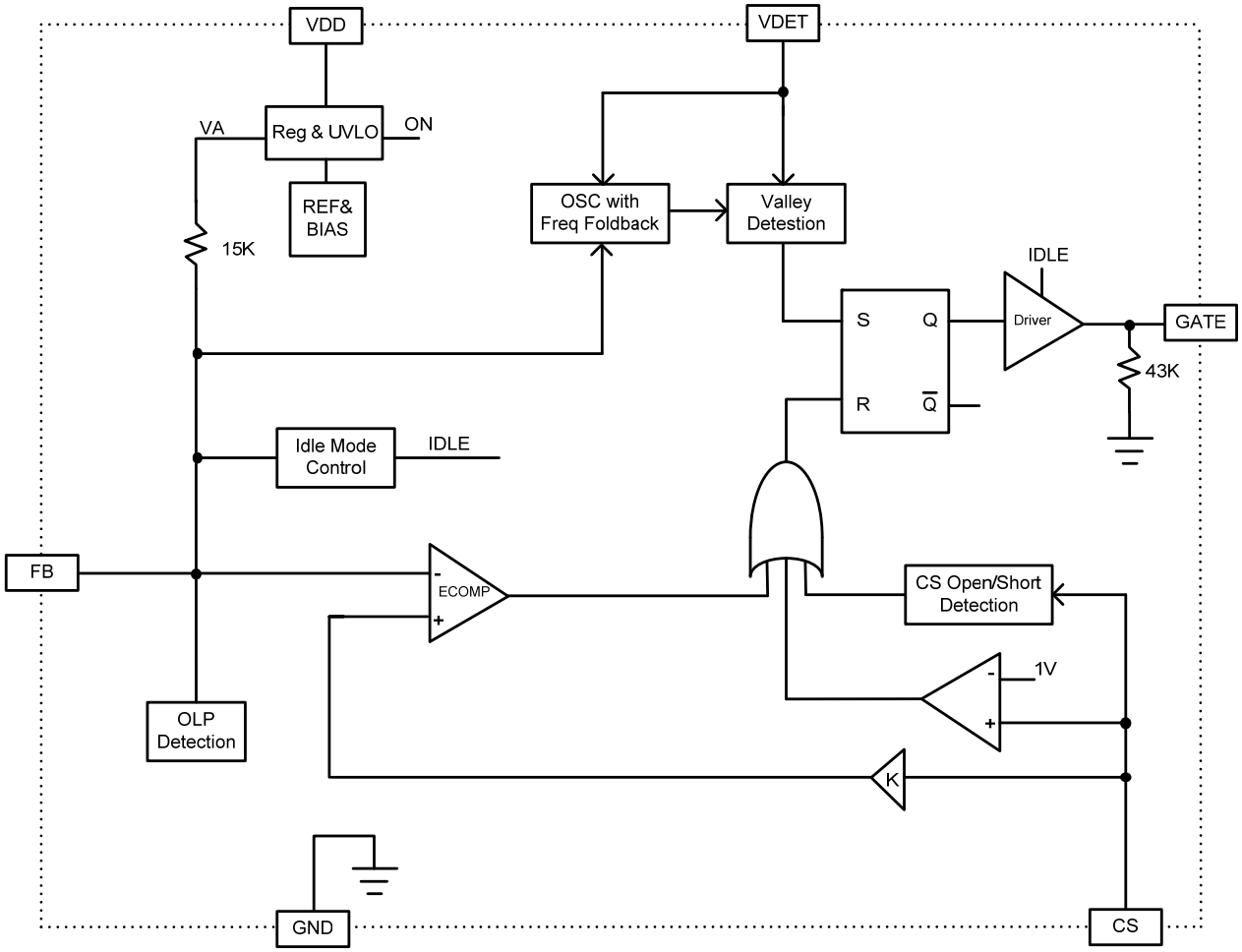
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply						
VDD Turn-On Voltage	V_{DDON}	V_{DD} Rising from 0V	11.3	12.3	13.3	V
VDD Turn-Off Voltage	V_{DDOFF}	V_{DD} Falling after Turn-on	6.7	7.4	8.1	V
VDD Over Voltage Protection	V_{DDOVP}	V_{DD} Rising from 0V		25		V
Start Up Supply Current	I_{DDST}	V_{DD} = 10V, before VDD Turn-on		8	15	μA
IDD Supply Current	I_{DD}	V_{DD} = 15V, after VDD Turn-on ,FB floating		0.6		mA
IDD Supply Current at Standby	I_{DDSTBY}	FB = 1.3V		0.4		mA
IDD Supply Current at Fault	$I_{DDFAULT}$	Fault mode, FB Floating		250		μA
Feedback						
FB Pull up Resistor	R_{FB}			15		kΩ
CS to FB Gain	A_{CS}			3		V/V
VFB at Max Peak Current				3 + V_{BE}		V
FB Threshold to Stop Switching	V_{FBBM1}			1.32		V
FB Threshold to Start Switching	V_{FBBM2}			1.41		V
Output Overload Threshold				4.2		V
OverLoad/Over Voltage Blanking Time	$T_{OVBLANK}$			320		ms

ELECTRICAL CHARACTERISTICS CONT'D

(V_{DD} = 14V, L_M = 0.8mH, R_{CS} = 0.87Ω, V_{OUT} = 12V, N_P = 54, N_S = 9, N_A = 10, T_A = 25°C, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Current Limit						
CS Current Limit Threshold	V_{CSLIM}		0.91	0.96	1.01	V
Leading Edge Blanking Time	$T_{CSBLANK}$		240	300	360	ns
GATE DRIVE						
Gate Rise Time	T_{RISE}	VDD = 10V, CL = 1nF		150	250	ns
Gate Falling Time	T_{FALL}	VDD = 10V, CL = 1nF		115	200	ns
Gate Low Level ON-Resistance	R_{ONLO}	I_{SINK} = 30mA		7		Ω
Gate High Level ON-Resistance	R_{ONHI}	I_{SOURCE} = 30mA		40		Ω
Gate Leakage Current		GATE = 25V, before VDD turn-on			1	μA
Oscillator						
Maximum Switching Frequency	f_{MAX}			75		kHz
Switching Frequency Foldback	f_{MIN}	FB = 2.3V+V_{BE}		f_{MAX}/3		kHz
Maximum Duty Cycle	D_{MAX}		65	75		%
Valley Detection						
ZCD Threshold Voltage	$VDET_{TH}$			100		mV
Valley Detection Time Window		After valley detection time window, if no valley detected, forcedly turn-on main switch		3.5		μs
VDET Leakage Current				1		μA
Protection						
CS Short Waiting Time				2		μs
CS Short Detection Threshold				0.115		V
CS Open Threshold Voltage				1.73		V
Abnormal OCP Blanking Time				150		ns
Thermal Shutdown Temperature				135		˚C
Line UVLO	$I_{VDETUVLO}$			0.1		mA
Line OVP	$I_{VDETOVP}$			2		mA
VDET Over Voltage Protection	$V_{DETVOOVP}$		2.448	2.72	2.992	V
VDET Vo Short Threshold	$V_{DETVOshort}$		0.406	0.58	0.754	V

FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ACT512 is a high performance peak current mode low-voltage PWM controller IC. The controller includes the most advance features that are required in the adaptor applications up to 60 Watt. Unique fast startup, frequency foldback, QR switching technique, accurate peak current line compensation, idle mode, short winding protection, OCP, OTP, OVP and UVLO are included in the controller.

Startup

Startup current of ACT512 is designed to be very low so that VDD could be charged to V_{DDON} threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, two 1MΩ, 1/8 W startup resistors could be used together with a VDD capacitor(4.7uF) to provide a fast startup and yet low power dissipation design solution.
During startup period, the IC begins to operate with minimum Ippk to minimize the switching stresses for the main switch, output diode and transformers. And then, the IC operates at maximum power output to achieve fast rise time. After this, V_{OUT} reaches about 90% V_{OUT}, the IC operates with a 'soft-landing' mode(decrease Ippk) to avoid output overshoot.

Constant Voltage (CV) Mode Operation

In constant voltage operation, the ACT512 regulates its output voltage through secondary side control circuit . The output voltage information is sensed at FB pin through OPTO coupling. The error signal at FB pin is amplified through TL431 and OPTO circuit. When the secondary output voltage is above regulation, the error amplifier output voltage decreases to reduce the switch current. When the secondary output voltage is below regulation, the error amplifier output voltage increases to ramp up the switch current to bring the secondary output back to regulation. The output regulation voltage is determined by the following relationship:

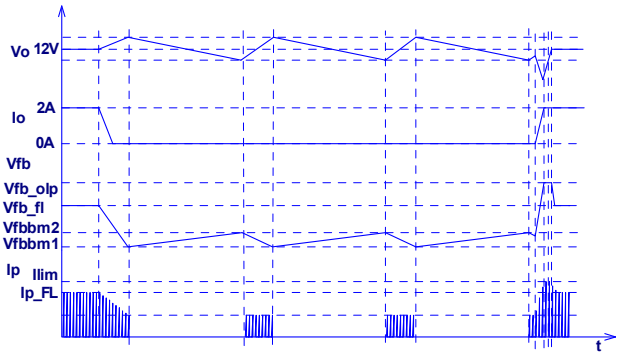
$$V_{OUTCV} = V_{REF\_TL431} \times (1 + \frac{R_{F1}}{R_{F2}}) \quad (1)$$

where R_{F1} (R15) and R_{F2} (R16) are top and bottom feedback resistor of the TL431.

No Load Idle Mode

In no load standby mode, the feedback voltage falls below V_{FBBM2} and reaches V_{FBBM1}, ACT512 stop switching. After it stops, as a result of a feedback reaction, the feedback voltage increases. When the feedback voltage reaches V_{FBBM2}, ACT512 start switching again. Feedback voltage drops again and output voltage starts to bounds back and forward with very small output ripple. ACT512 leaves idle mode when load is added strong enough to pull feedback voltage exceed V_{FBBM2}.

Figure 2:
Idle Mode



Primary Inductor Current Limit Compensation

The ACT512 integrates a primary inductor peak current limit compensation circuit to achieve constant OLP over wide line and wide inductance.

Frequency Foldback

When the load drops to 75% of full load level, ACT512 starts to reduce the switching frequency, which is proportional to the load current ,to improve the efficiency of the converter.

ACT512's load adaptive switching frequency enables applications to meet all latest green energy standards. The actual minimum average switching frequency is programmable with output capacitance, feedback circuit and dummy load (while still meeting standby power).

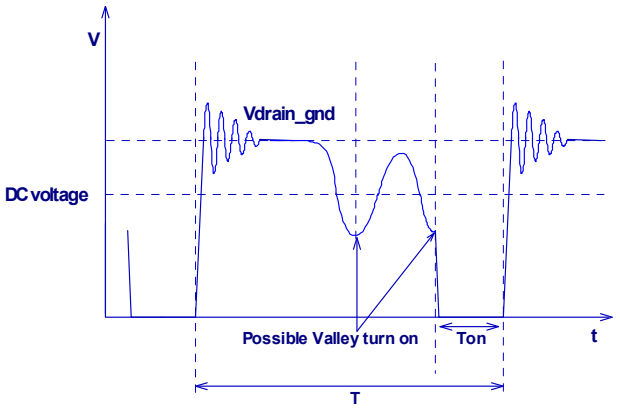
Valley Switching

ACT512 employed valley switching from no load to heavy load to reduce switching loss and EMI. In discontinuous mode operation, the resonant voltage between inductance and parasitic capacitance on MOSFET source pin is coupled by auxiliary winding and reflected on VDET pin through feedback network R5, R6. Internally, the VDET pin is connected to an zero-crossing detector to generate the switch turn on signal when the conditions are met.

FUNCTIONAL DESCRIPTION CONT'D

Figure 3:

Valley Switching



Protection Features

The ACT512 provides full protection functions. The following table summarizes all protection functions.

Auto-Restart Operation

ACT512 will enter into auto-restart mode when a fault is identified. There is a startup phase in the auto-restart mode. After this startup phase the conditions are checked whether the failure is still present. Normal operation proceeds once the failure mode is removed. Otherwise, new startup phase will be initiated again.

To reduce the power loss during fault mode, the startup delay control is implemented. The startup delay time increases over lines.

PROTECTION FUNCTIONS	FAILURE CONDITION	PROTECTION MODE
V_{DD} Over Voltage	V_{DD} > 25V (4 duty cycle)	Auto Restart
V_{VDET} Over Voltage/No Voltage	V_{VD} > 2.72V or No switching for 4 cycles	Auto Restart
Over Temperature	T > 135˚C	Auto Restart
Short Winding/ Short Diode	V_{CS} > 1.72V	Auto Restart
Over Load/Open Loop	IPK = I_{LIMIT} or V_{FB} = 3.5V + V_{BE} for 320ms	Auto Restart
Output Short Circuit	V_{DET} < 0.58V	Auto Restart
V_{DD} Under Voltage	V_{DD} < 7.4V	Auto Restart

TYPICAL APPLICATION

Design Example

The design example below gives the procedure for 12V/2A flyback converter using ACT512. Refer to application circuit Figure 4, the design for an adapter application starts with the following specification:

Input Voltage Range	90VAC - 265VAC, 50/60Hz
Output Power, P_O	24W
Output Voltage, V_{OUTCV}	12V
Full Load Current, I_{OUTFL}	2A
OCP Current, I_{OUTMAX}	2.3-2.6A
System Efficiency CV, η	0.86

The operation for the circuit shown in Figure 4 is as follows: the rectifier bridge D1−D4 and the capacitor C1/C2 convert the AC line voltage to DC bus voltage. This voltage supplies the primary winding of the transformer T1 and the startup circuit of R7/R8 and C4 to VDD pin of ACT512. The primary power current path is formed by the transformer's primary winding, Q1, and the current sense resistor R9. The resistors R3, R2, diode D5 and capacitor C3 create a snubber clamping network that protects Q1 from damage due to high voltage spike during Q1's turn off. The network consisting of capacitor C4, diode D6 and resistor R4 provides a VDD supply voltage for ACT512 from the auxiliary winding of the transformer. The resistor R4 is optional, which filters out spikes and noise to makes VDD more stable. C4 is the decoupling capacitor of the supply voltage and energy storage component for startup. During power startup, the current charges C4 through startup resistor R7/R8 from the rectified bus voltage. The diode D8 and the capacitor C5/L2/C6 rectify filter the output voltage. The resistor divider consists of R15 and R16 programs the output voltage. Since a bridge rectifier and bulk input capacitors are used, the resulting minimum and maximum DC input voltages can be calculated:

$$V_{INDC\_MIN} = \sqrt{2V_{INAC\_MIN}^2 - \frac{2P_{OUT}\left(\frac{1}{2f_L} - t_C\right)}{\eta \times C_{IN}}} \quad (2)$$

$$= \sqrt{2 \times 90^2 - \frac{2 \times 24 \times \left(\frac{1}{2 \times 47} - 3.5\,ms\right)}{0.86 \times 47\,\mu F}} \approx 90\,V$$

$$V_{IN(MAX)DC} = \sqrt{2} \times V_{IN(MAX)AC} \quad (3)$$

$$= \sqrt{2} \times (265\,V_{AC}) = 375\,V$$

Where η is the estimated circuit efficiency, f_L is the line frequency, t_C is the estimated rectifier conduction time, C_{IN} is empirically selected to be 47μF electrolytic capacitors.

The maximum duty cycle is set to be 45% at low line voltage 90VAC and the circuit efficiency is estimated to be 86%. Then in CCM the primary to secondary turn ratio N_P/N_S:

$$\frac{N_p}{N_s} = \frac{D_{CCM\_max} \times V_{IN\_min}}{(1 - D_{CCM\_max}) \times V_o} \quad (4)$$

$$= \frac{0.45 \times 90}{(1 - 0.45) \times 12} = 6.136$$

EF25 core is selected for the transformer. The core minimum Ae is 0.51cm^2. The minimum turn of the primary winding is:

$$N_p \geq \frac{V_{in\_min} \times D_{CCM\_max} \times 10^8}{f_{max} \times \Delta B_{max} \times Ae_{min}(gaus \times cm^2)} \quad (5)$$

$$= \frac{90 \times 0.45 \times 10^8}{75000 \times 2500 \times 0.51} = 42\,T$$

VDD voltage is set to 13V, base on the data we can get primary, secondly and auxiliary turns:

$$\frac{N_A}{N_s} = \frac{V_{dd} + V_{d\_aux}}{V_o + V_{d\_sec}} = \frac{13 + 0.7}{12 + 0.45} = 1.1 \quad (6)$$

$$N_p = 56T, N_s = 9T, N_a = 10T \quad (7)$$

We set DCM/CCM boundary is 185Vac,then the duty at full load is:

$$D_{CCM} = \frac{V_o \times N_p}{V_{INDC} \times N_s + V_o \times N_p} \quad (8)$$

$$= \frac{12 \times 56}{185 \times 1.414 \times 9 + 12 \times 56} = 0.22$$

The peak current of primary is:

$$I_{ppk} = \frac{2 \times V_o \times I_o}{V_{in} \times D_{DCM} \times \eta} \quad (9)$$

$$= \frac{2 \times 12 \times 2}{185 \times 1.414 \times 0.22 \times 0.86} = 0.97\,A$$

The primary inductance is:

$$L_m = \frac{V_{indc} \times D_{uty}}{I_{ppk} \times f_{sw}} = \frac{185 \times 1.414 \times 0.22}{0.97 \times 75000} = 0.8mH \quad (10)$$

TYPICAL APPLICATION CONT'D

Determining the value of the current sense resistor (R7) uses the maximum current in the design. So the input primary maximum current at maximum load:

$$I_{p\_OCP} = \sqrt{\frac{2 \times I_{OUT\_OCP} \times V_{OUT}}{L_P \times f_{sw} \times \eta}} = \sqrt{\frac{2 \times 2.6 \times 12}{0.8 \times 75 \times 0.86}} = 1.1A \quad (11)$$

Since the ACT512 internal current limit is set to 0.96V, the design of the current sense resistor is given by:

$$R_{CS} = \frac{V_{CS}}{I_{p\_OCP}} = \frac{0.96}{1.1} \approx 0.87\,\Omega \quad (12)$$

The voltage feedback resistors are selected according to the design. Because the line UVLO is 75VDC, the upper feedback resistor is given by:

$$R_{FB\_UP} = V_{INDC\_UVLO} \times \frac{N_A}{N_p \times I_{FB\_UVLO}} = \frac{60 \times 10}{56 \times 0.2\,mA} \approx 54.9k\Omega \quad (13)$$

The lower feedback resistor is selected as:

$$R_{FB\_LOW} = \frac{V_{FB}}{(V_{OUT} + V_D)\frac{N_A}{N_S} - V_{FB}} R_{FB\_UP} = \frac{2.2}{(12 + 0.45) \times 1.1 - 2.2} \times 54.9k\Omega \approx 11.7k\Omega \quad (14)$$

When selecting the output capacitor, a low ESR electrolytic capacitor is recommended to minimize ripple from the current ripple. The approximate equation for the output capacitance value is given by:

$$C_{OUT} = \frac{I_{OUT}}{f_{sw} \times V_{RIPPLE}} = \frac{2}{75k \times 50mV} = 533\mu F \quad (15)$$

Two 680µF electrolytic capacitors are used to further reduce the output ripple.

PCB Layout Guideline

Good PCB layout is critical to have optimal performance. Decoupling capacitor (C4) and feedback resistor (R5/R6) should be placed close to VDD and FB pin respectively. There are two main power path loops. One is formed by C1/C2, primary winding, mosfet transistor and current sense resistor (R9). The other is secondary winding, rectifier D8 and output capacitors (C5/C6). Keep these loop areas as small as possible. Connecting high current ground returns, the input capacitor ground lead, and the ACT512 GND pin to a single point (star ground configuration).

Figure 4:
Universal VAC Input, 12V/2A Output Adaptor

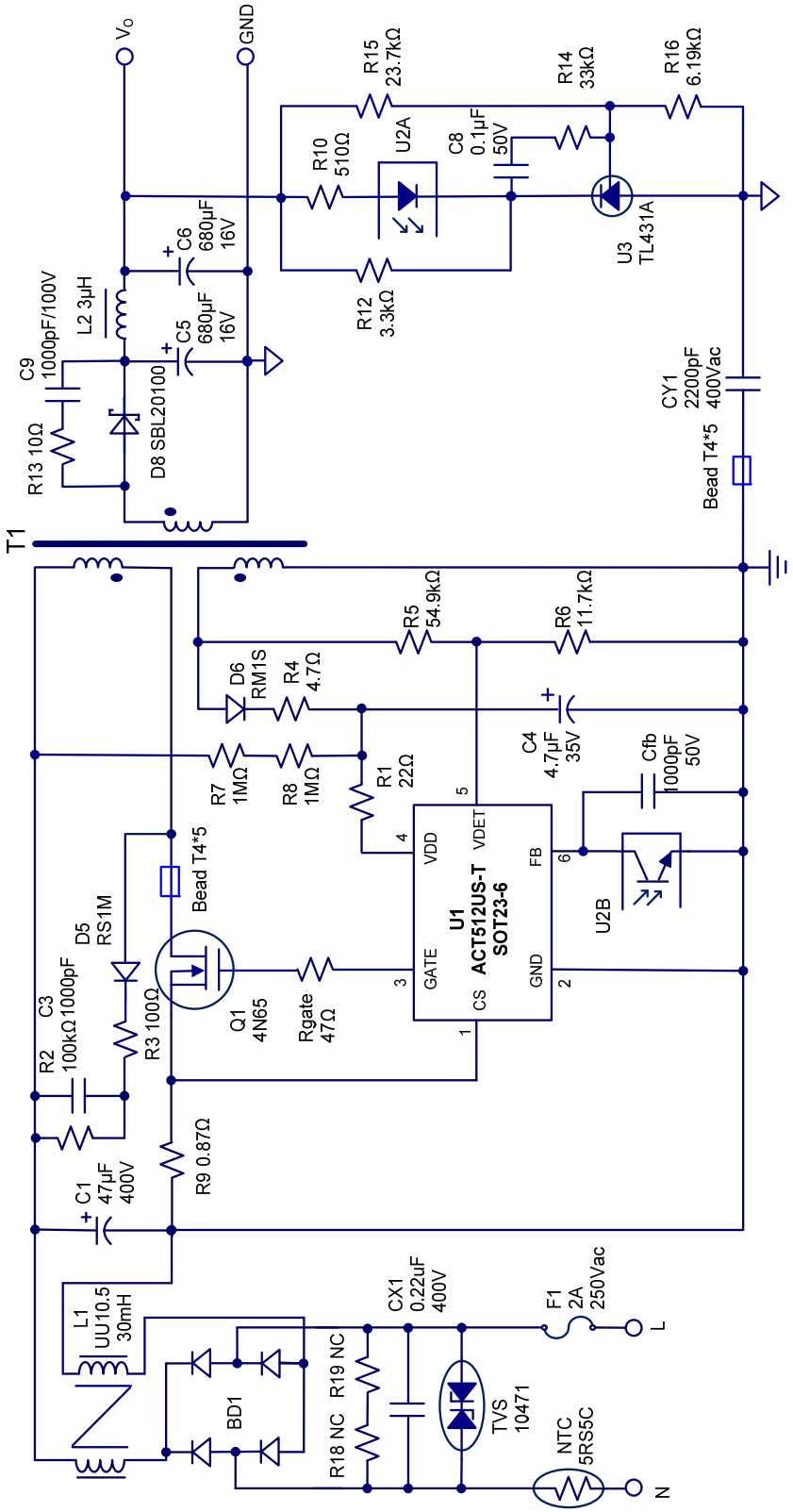


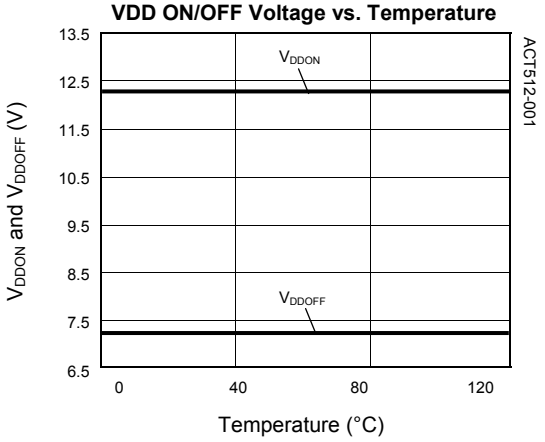
Table 1:

ACT512 12V24W Bill of Materials

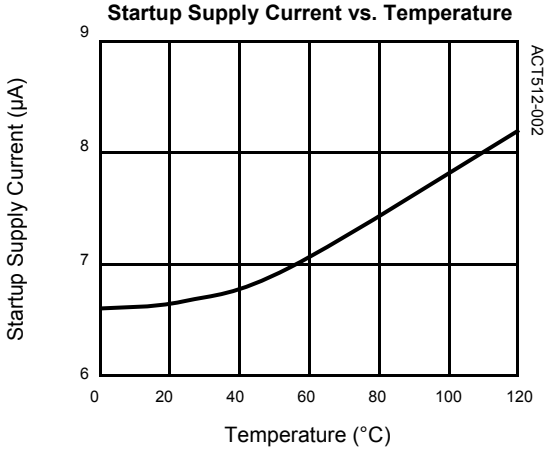
ITEM	REFERENCE	DESCRIPTION	QTY	MANUFACTURER
1	U1	IC, ACT512, SOT23-6	1	Active-Semi
2	C1	Capacitor, Electrolytic, 47μF/400V, 16 × 14mm	1	KSC
3	C3	Capacitor, Ceramic,1000pF/500V,0805,SMD	1	POE
4	C4	Capacitor, Electrolytic, 4.7μF/35V, 5 × 11mm	1	KSC
5	C5,C6	Capacitor, Electrolytic, 680μF/25V, 10 × 11.5mm	2	KSC
6	C8	Capacitor, Ceramic, 0.1μF/50V,0805,SMD	1	POE
7	C9	Capacitor, Ceramic,1000pF/100V,0805,SMD	1	POE
8	Cfb	Capacitor, Ceramic,1000pF/50V,0805,SMD	1	POE
9	D1-D4	Diode, Rectifier ,1000V2A, RL207, DO-41	4	Good-Ark
10	D5,D6	Diode, Ultra Fast, FR107,1000V/1.0A, DO-41	2	Good-Ark
11	D8	Diode, Schottky, 100V/20A, SBL20100, DO-220	1	Good-Ark
12	L1	CM Inductor, 30mH, UU10.5	1	SoKa
13	Bead1,2	T6*2*3, R5	2	SoKa
14	L3	DM Inductor, 3μH, R5	1	SoKa
15	Q1	Mosfet Transisor, 4N65, TO-220F	1	ST
16	PCB1	PCB, L*W*T = 48.5x29x1.6mm, Cem-1, Rev:A	1	Jintong
17	F1	Fusible, 2A/250V	1	TY-OHM
18	R12	Chip Resistor, 3.3kΩ, 0805, 5%	1	TY-OHM
19	R2	Carbon Resistor, 100kΩ, 2W, 5%	1	TY-OHM
20	R3	Chip Resistor, 100Ω, 0805, 5%	1	TY-OHM
21	R4	Chip Resistor, 4.7Ω, 0805, 5%	1	TY-OHM
22	R5	Chip Resistor, 54.9kΩ, 0805, 1%	1	TY-OHM
23	R6	Chip Resistor, 11.7kΩ, 0805, 1%	1	TY-OHM
24	R7,R8	Chip Resistor, 1MΩ, 0805, 5%	2	TY-OHM
25	R9	Chip Resistor, 0.87Ω,1W, 1%	1	TY-OHM
26	R10	Chip Resistor, 510Ω, 0805, 5%	1	TY-OHM
27	R14	Chip Resistor, 300kΩ, 0805, 5%	1	TY-OHM
28	R15	Chip Resistor, 23.7kΩ, 0805, 1%	1	TY-OHM
29	R16	Chip Resistor, 6.19kΩ, 0805, 1%	1	TY-OHM
30	Rgate	Chip Resistor, 47Ω, 0805, 5%	1	TY-OHM
31	T1	Transformer, L_P = 0.8mH, RM8	1	
32	NTC	Thermistor, SC053	1	TY-OHM
33	TVS	Varistor, 10471	1	TY-OHM
34	CX1	X capacitance, 0.22μF/400V,X1	2	
35	CY1	Y capacitance, 2200pF/400V,Y1	1	SEC
36	U2	Opto-coupler, PC817C CTR = 200%	1	Sharp
37	U3	Voltage Regulator, TL431A, V_{REF} = 2.5V	1	ST

TYPICAL PERFORMANCE CHARACTERISTICS

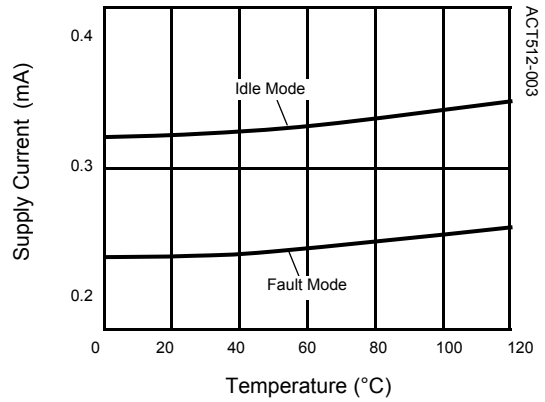
VDD ON/OFF Voltage vs. Temperature



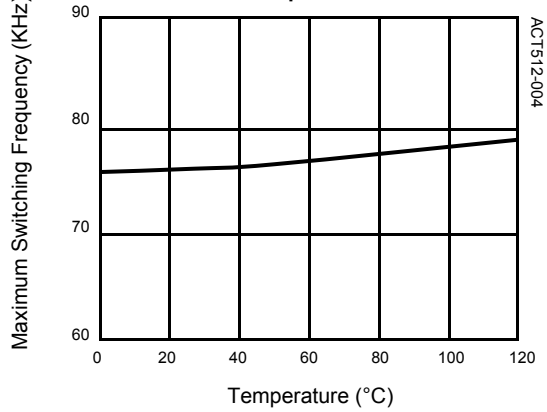
Startup Supply Current vs. Temperature



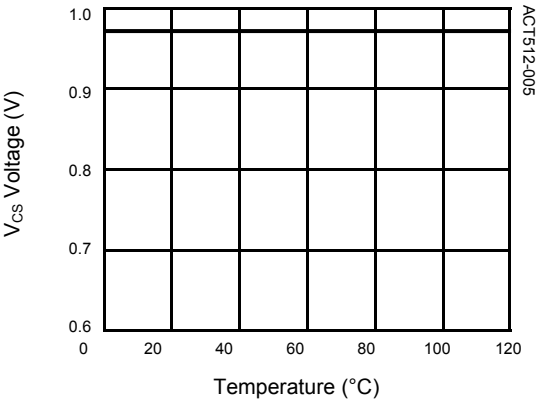
Supply Current at Idle/Fault Mode vs. Temperature



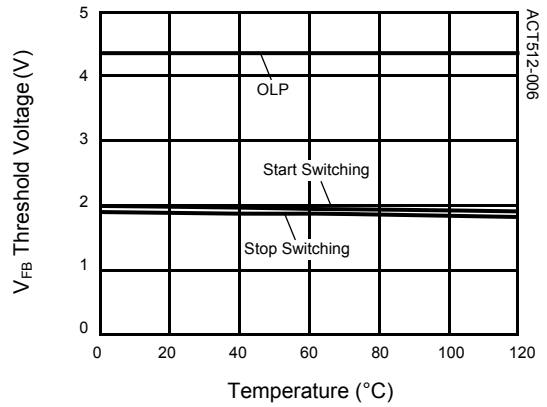
Maximum Switching Frequency vs. Temperature



V_{CS} Voltage vs. Temperature

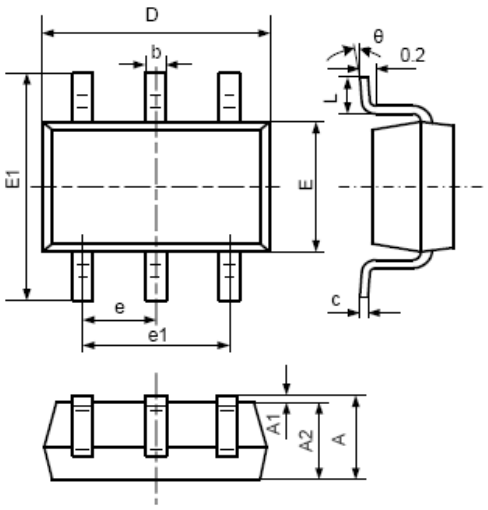


V_{FB} Threshold Voltage vs. Temperature



PACKAGE OUTLINE

SOT23-6 PACKAGE OUTLINE AND DIMENSIONS



SYMBOL	DIMENSION IN MILLIMETERS		DIMENSION IN INCHES	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.700 REF		0.028 REF	
L1	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View EA512US on WIN SOURCE
- Active-Semi International Inc. Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management