THE DATASHEET OF

9FGP204BKLF

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Frequency Timing Generator for Peripherals 9FGP204

Recommended Application:

Peripheral Clock for Intel Server

Output Features:

- 1 - 0.7V current-mode differential CPU pair
- 6 - 50MHz RMII outputs
- 2 - 125MHz RGMII outputs
- 1 - DOT 96MHz output
- 1 - 33.33MHz output
- 1 - 32.768KHz output
- 2 - 25MHz REF outputs

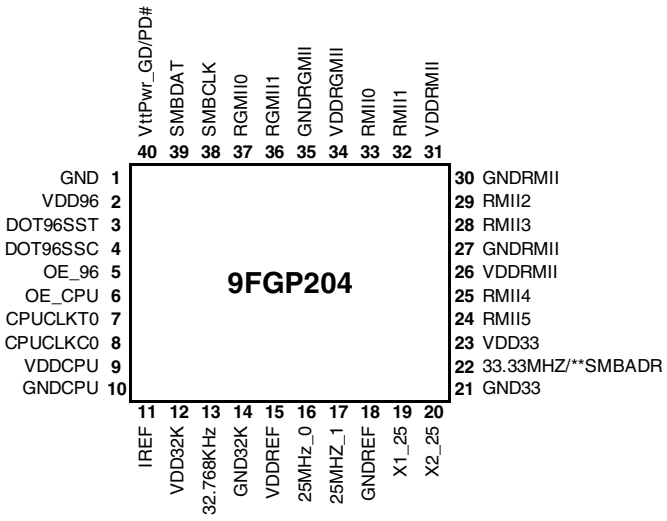
Key Specifications:

- Exact synthesis on CPU, RGMII, RMII & 33.33MHz clocks
- +/- 100ppm frequency accuracy on other clocks

Features/Benefits:

- Selectable SMBus Address - D0/D1 or C0/C1
- Spread Spectrum capability on CPU and DOT 96MHz clocks
- SMBus Control:
  - M/N and spread programming on CPU and DOT 96MHz clocks via SMBus
  - Differential outputs can be disabled via pins or SMBus

Pin Configuration



40-VFQFPN

* Internal Pull-Up Resistor

** Internal Pull-Dow n Resistor

Functionality

CPU FS2 Byte0 Bit2	CPU FS1 Byte0 Bit1	CPU FS0 Byte0 Bit0	CPUCLK MHz	DOT96SS MHz	33.33 MHz	RMII MHz	RGMII MHz	25 MHz	32.768 KHz
0	0	0	266.67	96.00	33.33	50.00	125.00	25.00	32.768
0	0	1	133.33	96.00	33.33	50.00	125.00	25.00	32.768
0	1	0	200.00	96.00	33.33	50.00	125.00	25.00	32.768
0	1	1	166.67	96.00	33.33	50.00	125.00	25.00	32.768
1	0	0	333.33	96.00	33.33	50.00	125.00	25.00	32.768
1	0	1	100.00	96.00	33.33	50.00	125.00	25.00	32.768
1	1	0	400.00	96.00	33.33	50.00	125.00	25.00	32.768
1	1	1	Reserved	96.00	33.33	50.00	125.00	25.00	32.768

Power up default is highlighted.

SMBus Address Selection

SMBADR	
*SMBADR = 0	SMBADR = 1
D0/D1	C0/C1

* Default value

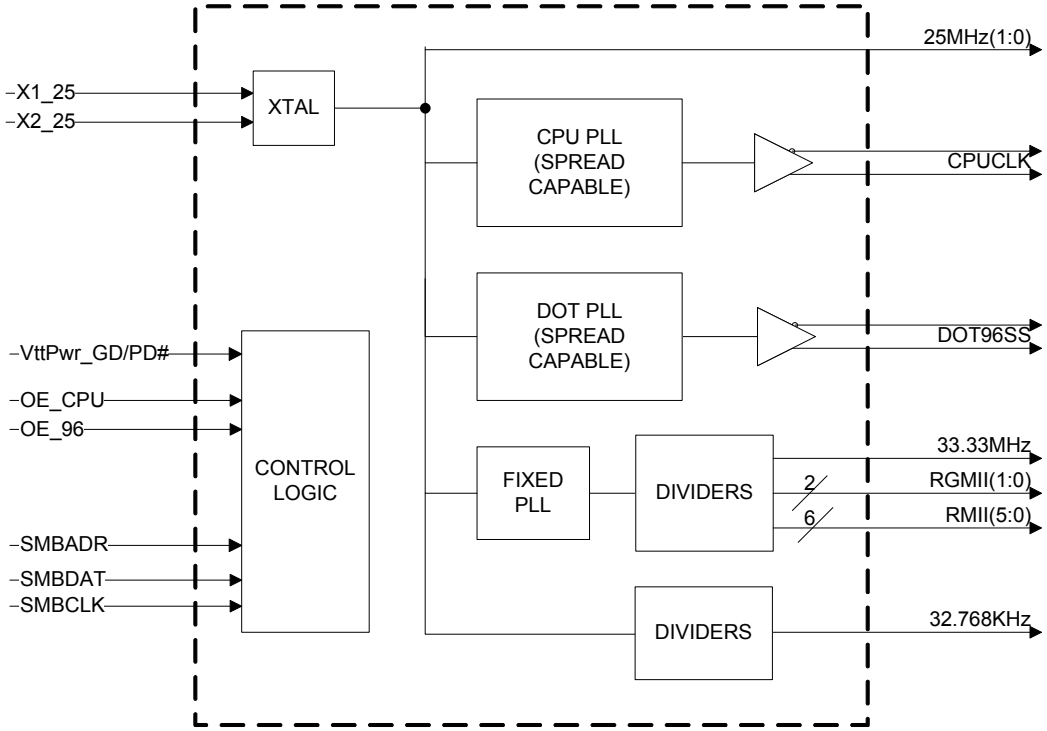
Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	GND	PWR	Ground pin.
2	VDD96	PWR	Power pin for the DOT96 clocks, nominal 3.3V
3	DOT96SST	OUT	True clock of differential pair for 96.00MHz spread spectrum capable DOT clock. These are current mode outputs. External resistors are required for voltage bias.
4	DOT96SSC	OUT	Complementary clock of differential pair for 96.00MHz spread spectrum capable DOT clock. These are current mode outputs. External resistors are required for voltage bias.
5	OE_96	IN	Active high input for enabling 96Hz outputs. 1 = enable output(s), 0 =disable output(s)
6	OE_CPU	IN	Active high input for enabling CPU DIFF pairs. 1 = enable output(s), 0 =disable output(s)
7	CPUCLKT0	OUT	True clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
8	CPUCLKC0	OUT	Complementary clock of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
9	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
10	GNDCPU	PWR	Ground pin for the CPU outputs
11	IREF	OUT	This pin establishes the reference for the differential current-mode output pairs. It requires a fixed precision resistor to ground. 475ohm is the standard value for 100ohm differential impedance. Other impedances require different values. See data sheet.
12	VDD32K	PWR	Power pin for the 32.768KHz outputs, nominal 3.3V
13	32.768KHz	OUT	32.768KHz clock output
14	GND32K	PWR	Ground pin for the 32.768KHz outputs
15	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
16	25MHz_0	OUT	25MHz clock output, 3.3V
17	25MHZ_1	OUT	25MHz clock output, 3.3V
18	GNDREF	PWR	Ground pin for the REF outputs.
19	X1_25	IN	Crystal input, Nominally 25.00MHz.
20	X2_25	OUT	Crystal output.
21	GND33	PWR	Ground pin for the 33.33MHz outputs
22	33.33MHZ/**SMBADR	I/O	33.33MHz clock output / SMBus address select bit.
23	VDD33	PWR	Power pin for the 33.33MHz outputs, nominal 3.3V
24	RMII5	OUT	3.3V 50MHz RMII clock output
25	RMII4	OUT	3.3V 50MHz RMII clock output
26	VDDRMII	PWR	3.3V power pin for the RMII clocks.
27	GNDRMII	PWR	Ground pin for the RMII outputs
28	RMII3	OUT	3.3V 50MHz RMII clock output
29	RMII2	OUT	3.3V 50MHz RMII clock output
30	GNDRMII	PWR	Ground pin for the RMII outputs
31	VDDRMII	PWR	3.3V power pin for the RMII clocks.
32	RMII1	OUT	3.3V 50MHz RMII clock output
33	RMII0	OUT	3.3V 50MHz RMII clock output
34	VDDRGMII	PWR	3.3V power pin for the RGMII clocks and PLL
35	GNDRGMII	PWR	Ground pin for the RGMII outputs
36	RGMII1	OUT	3.3V 125MHz RGMII clock output
37	RGMII0	OUT	3.3V 125MHz RGMII clock output
38	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
39	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
40	VttPwr_GD/PD#	IN	This 3.3V LVTTL input is a level sensitive strobe used to determine when latch inputs are valid and are ready to be sampled. This is an active high input. / Asynchronous active low input pin used to power down the device into a low power state.

General Description

The **9FGP204** is a peripheral clock for Intel Servers. It is driven with a 25MHz crystal and generates a variety of clocks, including 125MHz RGMII. An SMBus interface allows full control of the device.

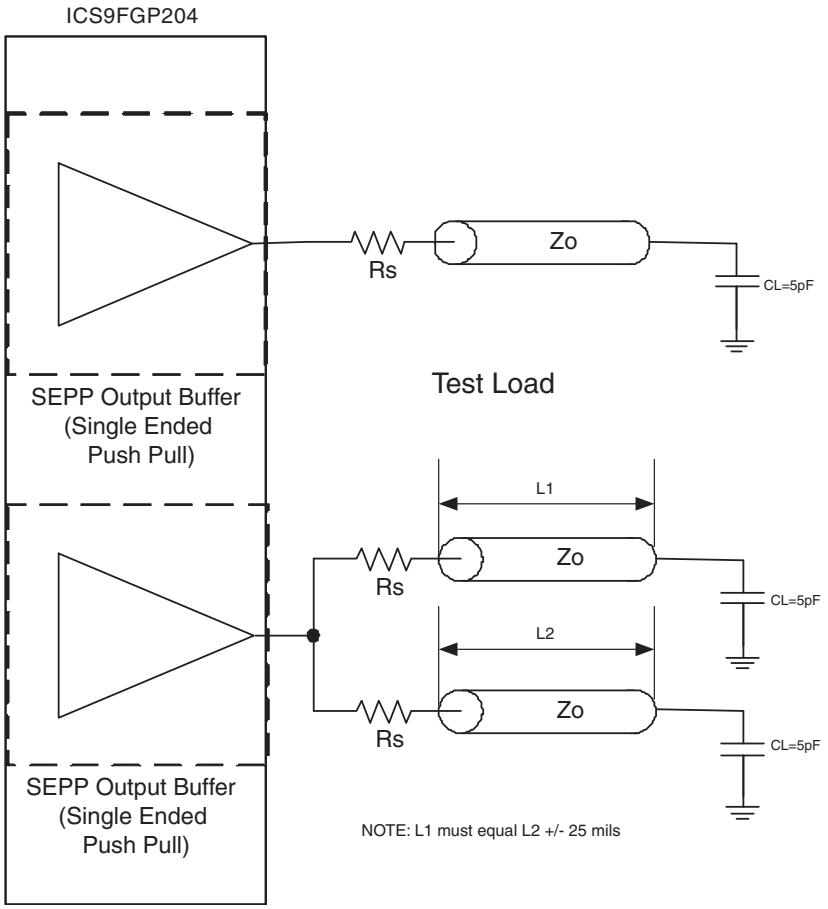
Block Diagram



Power Supply Pins

Pin Number		Description
VDD	GND	
9	10	CPUCLK output and PLL
2	1	DOT96SS output and PLL
34	35	125 MHz RGMII outputs and PLL
26,31	27,30	50 MHz RMII outputs
23	21	33.33MHz output
12	14	32.768KHz output
15	18	XTAL, REF outputs

Note: All VDD should be connected to a common power rail with proper filtering and decoupling. Pins 2, 9 and 34 should be treated as analog pins for decoupling purposes.



Drive Strength for all the single-ended outputs can be controlled by the SMBus Bytes 4 and 5 as shown in the Default Drive Strength Table.

Default Drive Strength Table

	Default Drive	Optional Drive
RGMII	1 Load	NA
RMII	1 Load	2 Loads
33.33MHz	2 Loads	1 Load
25Mhz	2 Loads	1 Load
32.768KHz	2 Loads	1 Load

Series Termination Resistor Values EXCEPT RGMII

Output Drive Strength	Series Resistor (Rs) for driving 1 Load	Series Resistor (Rs) for driving 2 Loads
1 Load	22 ohms	N/A
2 Loads	33 ohms	8.2 ohms

Note: All values are for Zo = 50Ω

Series Termination Resistor Values - RGMII

Output Drive Strength	Series Resistor (Rs) for driving 1 Load	Series Resistor (Rs) for driving 2 Loads
1 Load	27 ohms	N/A

Note: All values are for Zo = 50Ω

Truth Table 1: VttPwr_GD/PD# and OE_96

VttPwr_GD/PD# Pin 40	OE_96 Pin 5	Clocks
0	0	All clocks are powered down
0	1	All clocks are powered down
1	0	All clocks are enabled except DOT96SS
1	1	*All clocks are enabled including DOT96SS

*Assuming DOT96 Output Enable from SMBus Byte2 Bit0 sets to enable (default)

Truth Table 2: VttPwr_GD/PD# and OE_CPU

VttPwr_GD/PD# Pin 40	OE_CPU Pin 6	Clocks
0	0	All clocks are powered down
0	1	All clocks are powered down
1	0	All clocks are enabled except CPUCLK
1	1	*All clocks are enabled including CPUCLK

*Assuming CPUCLK Output Enable from SMBus Byte2 Bit1 sets to enable (default)

Table 1: CPU Spread and Frequency Selection

CPU SS_EN Byte 0 Bit 3	CPU FS2 Byte 0 Bit 2	CPU FS1 Byte 0 Bit 1	CPU FS0 Byte 0 Bit 0	CPU MHz	Down Spread %
0	0	0	0	266.67	0%
0	0	0	1	133.33	0%
0	0	1	0	200.00	0%
0	0	1	1	166.67	0%
0	1	0	0	333.33	0%
0	1	0	1	100.00	0%
0	1	1	0	400.00	0%
0	1	1	1	200.00	0%
1	0	0	0	266.67	0.5%
1	0	0	1	133.33	0.5%
1	0	1	0	200.00	0.5%
1	0	1	1	166.67	0.5%
1	1	0	0	333.33	0.5%
1	1	0	1	100.00	0.5%
1	1	1	0	400.00	0.5%
1	1	1	1	200.00	0.5%

Table2: DOT96 Spread and Frequency Selection Table

DOT96 SS_EN	FS3	FS2	FS1	FS0	DOT96SS MHz	Spread %	
Byte 0 bit 4	Byte 3 bit 3	Byte 3 bit 2	Byte 3 bit 1	Byte 3 bit 0			
0	0	0	0	0	96.00	0	
0	0	0	0	1	96.00	0	
0	0	0	1	0	96.00	0	
0	0	0	1	1	96.00	0	
0	0	1	0	0	96.00	0	
0	0	1	0	1	96.00	0	
0	0	1	1	0	96.00	0	
0	0	1	1	1	96.00	0	
0	1	0	0	0	96.00	0	
0	1	0	0	1	96.00	0	
0	1	0	1	0	96.00	0	
0	1	0	1	1	96.00	0	
0	1	1	0	0	96.00	0	
0	1	1	0	1	96.00	0	
0	1	1	1	0	96.00	0	
0	1	1	1	1	96.00	0	
1	0	0	0	0	96.00	+/-0.25	Center
1	0	0	0	1	96.00	+/-0.5	Center
1	0	0	1	0	96.00	+/-0.75	Center
1	0	0	1	1	96.00	+/-1.0	Center
1	0	1	0	0	96.00	-0.25	Down
1	0	1	0	1	96.00	-0.50	Down
1	0	1	1	0	96.00	-0.75	Down
1	0	1	1	1	96.00	-1.0	Down
1	1	0	0	0	96.00	-1.25	Down
1	1	0	0	1	96.00	-1.50	Down
1	1	0	1	0	96.00	-1.75	Down
1	1	0	1	1	96.00	-2.0	Down
1	1	1	0	0	96.00	-2.25	Down
1	1	1	0	1	96.00	-2.5	Down
1	1	1	1	0	96.00	-2.75	Down
1	1	1	1	1	96.00	-3.00	Down

Absolute Maximum Ratings

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
3.3V Supply Voltage	VDDxxx	-	GND - 0.5	3.3V	GND + 4.5	V	1
Maximum difference across all VDD pins	VDDdelta	-			0.5	V	1
Storage Temperature	Ts	-	-65		150	˚C	1
Ambient Operating Temp	Tambient	-	0		70	°C	1
Junction Temperature	Tj	-			125	°C	1
Input ESD protection HBM	ESD prot	-	2000			V	1

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - Input/Supply/Common Output Parameters

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V_{IH}	3.3 V +/-5%	2		V_{DD} + 0.3	V	1
Input Low Voltage	V_{IL}	3.3 V +/-5%	V_{SS} - 0.3		0.8	V	1
Input High Current	I_{IH}	$V_{IN} = V_{DD}$	-5		5	uA	1
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			uA	1
Low Threshold Input-High Voltage	V_{IH_FS}	3.3 V +/-5%	0.7		V_{DD} + 0.3	V	1
Low Threshold Input-Low Voltage	V_{IL_FS}	3.3 V +/-5%	V_{SS} - 0.3		0.35	V	1
Operating Current	$I_{DD3.3OP}$	all outputs driven, CPU@100M		204	225	mA	1
Powerdown Current	$I_{DD3.3PD}$	all diff pairs driven		20	30	mA	1
		all differential pairs tri-stated		5	8	mA	1
Input Frequency	F_i	V_{DD} = 3.3 V		25.00000		MHz	2
Pin Inductance	L_{pin}				7	nH	1
Input Capacitance	C_{IN}	Logic Inputs			4	pF	1
	C_{OUT}	Output pin capacitance			5	pF	1
	C_{INX}	X1 & X2 pins			5	pF	1
Clk Stabilization	T_{STAB}	From VDD Power-Up or de-assertion of PD to 1st clock		0.5	2.5	ms	1
Modulation Frequency		Triangular Modulation	30		33	kHz	1
Tdrive_PD		CPU output enable after PD de-assertion		260	300	us	1
Tfall_PD		PD fall time of			5	ns	1
Trise_PD		PD rise time of			5	ns	1
SMBus Voltage	V_{DD}		2.7		5.5	V	1
Low-level Output Voltage	V_{OL}	@ I_{PULLUP}			0.4	V	1
Current sinking at V_{OL} = 0.4 V	I_{PULLUP}		4	5		mA	1
SCLK/SDATA Clock/Data Rise Time	T_{RI2C}	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T_{FI2C}	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] Input frequency should be measured at the REF pin and tuned to ideal 25.00MHz to meet ppm frequency accuracy on PLL outputs.

Electrical Characteristics - CPU 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660	731	850	mV	1,3
Voltage Low	VLow		-150	70	150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		800	1150	mV	1
Min Voltage	Vuds		-300	8		mV	1
Crossing Voltage (abs)	Vx(abs)		250	366	550	mV	1
Crossing Voltage (var)	d-Vx	Variation of crossing over all edges		16	140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1,2
Average period	T_{period}	100.00MHz nominal	9.9990	10.0000	10.0001	ns	2
		100.00MHz spread	10.0240	10.0250	10.0251	ns	2
Absolute min/max period	$T_{absmin/max}$	100.00MHz nominal/spread	9.9490		10.1011	ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	376	700	ps	1,4
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	335	700	ps	1,4
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V		104	125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V		92	125	ps	1
Rise/Fall Matching	t_{RFM}	Single-ended measurement, averaging on		12.7	20	%	1
Slew Rate	t_{SLEW}	Differential Measurment	1	2	4	V/ns	1,5
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	49.8	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom, CPUCLK		45	50	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz_x is tuned to exactly 25.000MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

[4] Rise/fall time measured on single-ended waveform per CK410 specification.

[5] Slew rate measured on differential waveform per CK505 specification.

Electrical Characteristics - DOT96SS 0.7V Current Mode Differential Pair

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	Notes
Current Source Output Impedance	Zo	$V_O = V_x$	3000			Ω	1
Voltage High	VHigh	Statistical measurement on single ended signal	660	725	850	mV	1,3
Voltage Low	VLow		-150	51	150	mV	1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		764	1150	mV	1
Min Voltage	Vuds		-300	5		mV	1
Crossing Voltage (abs)	Vx(abs)		250	372	550	mV	1
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1
Long Accuracy	ppm	see Tperiod min-max values	-100	-41	100	ppm	1,2
Average period	Tperiod	96.00MHz nominal	10.4156	10.4166	10.4176	ns	2
		96.00MHz -0.5% spread	10.4417	10.4427	10.4437	ns	2
Absolute min period	Tabsmin	96.00MHz nominal/-0.5% spread	10.1917		10.6937	ns	1,2
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	361	700	ps	1,4
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	375	700	ps	1,4
Rise Time Variation	d-t_r	V_{OL} = 0.175V, V_{OH} = 0.525V		107	125	ps	1
Fall Time Variation	d-t_f	V_{OH} = 0.525V V_{OL} = 0.175V		107	125	ps	1
Rise/Fall Matching	t_{RFM}	Single-ended measurement, averaging on		15	20	%	1
Slew Rate	t_{SLEW}	Differential Measurment	1	2	4	V/ns	1,5
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	51.3	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	Measurement from differential wavefrom		54	250	ps	1

*T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%; C_L =2pF, R_S=33.2Ω, R_P=49.9Ω, I_{REF} = 475Ω

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz_x is tuned to exactly 25.000MHz

[3]$I_{REF} = V_{DD}/(3xR_R)$. For R_R = 475Ω (1%), I_{REF} = 2.32mA. I_{OH} = 6 x I_{REF} and V_{OH} = 0.7V @ Z_O=50Ω.

[4] Rise/fall time measured on single-ended waveform per CK410 specification.

[5] Slew rate measured on differential waveform per CK505 specification.

Electrical Characteristics - REF - 25MHz

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Long Accuracy	ppm	see Tperiod min-max values	-50	0	50	ppm	1,2
Clock period	T_{period}	25.00MHz output nominal	39.998	40.000	40.002	ns	2
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-29			mA	1
		V_{OH}@MAX = 3.135 V			-23	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	29			mA	1
		V_{OL} @ MAX = 0.4 V			27	mA	1
Rise Time	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.14	2	ns	1
Fall Time	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.32	2	ns	1
Skew	t_{sk1}	V_T = 1.5 V		16	500	ps	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	53.2	55	%	1
Jitter, Cycle-cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		75	200	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz_x is tuned to exactly 25.000MHz

Electrical Characteristics - RGMII - 125MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-50	0	50	ppm	1,2
Clock period	Tperiod	125.00MHz output nominal	7.9996	8.000	8.0004	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_r	V_{OL}=20%xVdd, V_{OH}=80%xVdd		0.66	0.75	ns	1
Fall Time	t_f	V_{OL}=20%xVdd, V_{OH}=80%xVdd		0.70	0.75	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	52.9	55	%	1
Group Skew	t_{skew_RGMII}	V_T = 1.5 V,		15	100	ps	1
Jitter, Long Term	t_{jabs}	V_T = 1.5 V, 10 : sec interval		141	500	ps	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		75	250	ps	1
Jitter, Peak	t_{jpeak}	V_T = 1.5 V		68	100	ps	1,3

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz_x is tuned to exactly 25.000MHz

[3]1/2 of the peak-to-peak jitter. (Lg+ + lLg-l)/2

Electrical Characteristics - RMII - 50MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-50	0	50	ppm	1,2
Clock period	Tperiod	50.00MHz output nominal	19.9990	20.0000	20.001	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.1	3	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.1	3	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	35	51.5	65	%	1
Group Skew	$t_{skew_RMII(5:0)}$	V_T = 1.5 V, across all 6 outputs		60	200	ps	1
Jitter, Long Term	t_{jabs}	V_T = 1.5 V, 10 8sec interval		127	500	ps	1
Jitter, Peak	t_{jpeak}	V_T = 1.5 V		88	100	ps	1,3

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

[2] All Long Term Accuracy and Clock Period specifications are guaranteed assuming that 25MHz_x is tuned to exactly 25.000MHz

[3]1/2 of the peak-to-peak jitter. (Lg+ + lLg-l)/2

Electrical Characteristics - 33.33MHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	0	100	ppm	1
Clock period	Tperiod	33.33MHz output non-spread	29.9970	30.0000	30.0030	ns	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	0.87	2	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.35	2	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	50.7	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		104	350	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

Electrical Characteristics - 32.768KHz

PARAMETER	SYMBOL	CONDITIONS*	MIN	TYP	MAX	UNITS	NOTES
Long Accuracy	ppm	see Tperiod min-max values	-100	-79	100	ppm	1
Clock period	Tperiod	32.768KHz output nominal	30.5149	30.5180	30.5211	us	1
Output High Voltage	V_{OH}	I_{OH} = -1 mA	2.4			V	1
Output Low Voltage	V_{OL}	I_{OL} = 1 mA			0.4	V	1
Output High Current	I_{OH}	V_{OH} @MIN = 1.0 V	-33			mA	1
		V_{OH}@MAX = 3.135 V			-33	mA	1
Output Low Current	I_{OL}	V_{OL} @ MIN = 1.95 V	30			mA	1
		V_{OL} @ MAX = 0.4 V			38	mA	1
Rise Time	t_r	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.39	4	ns	1
Fall Time	t_f	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.6	4	ns	1
Duty Cycle	d_{t1}	V_T = 1.5 V	45	49.5	55	%	1
Jitter, Cycle to cycle	$t_{jcyc-cyc}$	V_T = 1.5 V		220	500	ps	1

*TA = 0 - 70°C; Supply Voltage VDD = 3.3 V +/-5%, CL = 5 pF with Rs as shown in the termination table (unless otherwise specified)

[1]Guaranteed by design and characterization, not 100% tested in production.

General SMBus serial interface information for the 9FGP204

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D0 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the beginning byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address D0 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address D1 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if X(H) was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address *D0(H)			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
○			
○			○
○			○
			○
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address *D0(H)			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address *D1(H)			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			○
○			○
○			○
○			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

* The SMBus address depends on the latched value of pin 22. Please see SMBus Address Selection table on page 1.

SMBus Table: CPU Frequency Select and Spread Spectrum Control Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		0
Bit 6	-	Reserved	Reserved	Rev 0.20	Reserved		0
Bit 5	-	Reserved	Reserved	RW	Reserved		0
Bit 4	-	DOT96 SS_EN	DOT96 Spread Spectrum Enable	RW	Disable	Enable	0
Bit 3	-	CPU SS_EN	CPU Spread Spectrum Enable	RW	See Table 1: CPU Frequency Selection Table		0
Bit 2	-	CPU FS2	CPU Freq Select Bit 2	RW			1
Bit 1	-	CPU FS1	CPU Freq Select Bit 1	RW			0
Bit 0	-	CPU FS0	CPU Freq Select Bit 0	RW			1

SMBus Table: RMII Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	24	RMII_5 Enable	RMII_7 Output Control	RW	Disable	Enable	1
Bit 6	25	RMII_4 Enable	RMII_6 Output Control	RW	Disable	Enable	1
Bit 5	28	RMII_3 Enable	RMII_5 Output Control	RW	Disable	Enable	1
Bit 4	29	RMII_2 Enable	RMII_4 Output Control	RW	Disable	Enable	1
Bit 3	32	RMII_1 Enable	RMII_3 Output Control	RW	Disable	Enable	1
Bit 2	33	RMII_0 Enable	RMII_2 Output Control	RW	Disable	Enable	1
Bit 1	36	RGMII_1 Enable	RGMII_1 Output Control	RW	Disable	Enable	1
Bit 0	37	RGMII_0 Enable	RGMII_0 Output Control	RW	Disable	Enable	1

SMBus Table: DOT, CPU, 32.768KHz, 25MHz and 33.33MHz Outputs Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	7,8	CPUCLK PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 6	3,4	DOT96SS PD Drive Mode	Driven in PD	RW	Driven	Hi-Z	0
Bit 5	22	33.33MHz Enable	33.33MHz Output Control	RW	Disable	Enable	1
Bit 4	17	25MHz_1 Enable	25MHz_1 Output Control	RW	Disable	Enable	1
Bit 3	16	25MHz_0 Enable	25MHz_0 Output Control	RW	Disable	Enable	1
Bit 2	13	32.768kHz Enable	32.768KHz Output Control	RW	Disable	Enable	1
Bit 1	6	CPUCLK Enable	CPUCLK Output Control	RW	Disable	Enable	1
Bit 0	5	DOT96SS Enable	DOT96SS Output Control	RW	Disable	Enable	1

SMBus Table: DOT96 Frequency Select and Spread Spectrum Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		0
Bit 6	-	Reserved	Reserved	RW	Reserved		0
Bit 5	-	Reserved	Reserved	RW	Reserved		0
Bit 4	-	Reserved	Reserved	RW	Reserved		0
Bit 3	-	DOT96SS FS3	DOT96 Freq Select Bit 3	RW	See Table 2: DOT Frequency Selection Table		0
Bit 2	-	DOT96SS FS2	DOT96 Freq Select Bit 2	RW			0
Bit 1	-	DOT96SS FS1	DOT96 Freq Select Bit 1	RW			0
Bit 0	-	DOT96SS FS0	DOT96 Freq Select Bit 0	RW			0

SMBus Table: RMII Strength Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	24	RMII_5 Str	RMII_7 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 6	25	RMII_4 Str	RMII_6 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 5	28	RMII_3 Str	RMII_5 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 4	29	RMII_2 Str	RMII_4 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 3	32	RMII_1 Str	RMII_3 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 2	33	RMII_0 Str	RMII_2 Strength Control	RW	1-Load (1X)	2-Loads (2X)	0
Bit 1	-	Reserved	Reserved	RW	Reserved		0
Bit 0	-	Reserved	Reserved	RW	Reserved		0

SMBus Table: 32.768KHz, 25Mhz and 33.33MHz Strength Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	Reserved		0
Bit 6	-	Reserved	Reserved	RW	Reserved		0
Bit 5	22	33.33MHz Str	33.33MHz Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 4	17	25MHz_1 Str	25MHz_1 Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 3	16	25MHz_0 Str	25MHz_1 Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 2	13	32.768kHz Str	32.768kHz Strength Control	RW	1-Load (1X)	2-Loads (2X)	1
Bit 1	-	Reserved	Reserved	RW	Reserved		0
Bit 0	-	Reserved	Reserved	RW	Reserved		0

SMBus Table: Vendor & Revision ID Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	A rev = 0000 B rev = 0001		X
Bit 6	-	RID2		R			X
Bit 5	-	RID1		R			X
Bit 4	-	RID0		R			X
Bit 3	-	VID3	VENDOR ID	R	ICS/IDT = 0001		0
Bit 2	-	VID2		R			0
Bit 1	-	VID1		R			0
Bit 0	-	VID0		R			1

SMBus Table: Device ID

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID 7 (MSB)	Device ID	RW	Reserved		0
Bit 6	-	Device ID 6		RW	Reserved		0
Bit 5	-	Device ID 5		RW	Reserved		1
Bit 4	-	Device ID 4		RW	Reserved		0
Bit 3	-	Device ID 3		RW	Reserved		0
Bit 2	-	Device ID 2		RW	Reserved		1
Bit 1	-	Device ID 1		RW	Reserved		0
Bit 0	-	Device ID 0 (LSB)		RW	Reserved		0

SMBus Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register configures how many bytes will be read back.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	0
Bit 1	-	BC1		RW	-	-	0
Bit 0	-	BC0		RW	-	-	1

SMBus Table: Reserved

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	Reserved						0
Bit 1	Reserved						0
Bit 0	Reserved						0

SMBus Table: PLLs M/N Programming Enable Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/N_EN	PLLs M/N Programming Enable	RW	Disable	Enable	0
Bit 6	Reserved						0
Bit 5	Reserved						0
Bit 4	Reserved						0
Bit 3	Reserved						0
Bit 2	Reserved						0
Bit 1	Reserved						0
Bit 0	Reserved						0

SMBus Table: CPU PLL VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 25 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div 9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: CPU PLL VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 11 and 12 will configure the VCO frequency. Default at power up = latch-in or Byte 0 Rom table. VCO Frequency = 25 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: CPU PLL Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 13 and 14 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

SMBus Table: DOT PLL VCO Frequency Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div8	N Divider Prog bit 8	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 25 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div9	N Divider Prog bit 9	RW			X
Bit 5	-	M Div5	M Divider Programming bits	RW			X
Bit 4	-	M Div4		RW			X
Bit 3	-	M Div3		RW			X
Bit 2	-	M Div2		RW			X
Bit 1	-	M Div1		RW			X
Bit 0	-	M Div0		RW			X

SMBus Table: DOT PLL VCO Frequency Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	N Div7	N Divider Programming b(7:0)	RW	The decimal representation of M and N Divier in Byte 17 and 18 will configure the VCO frequency. Default at power up = Byte 0 Rom table. VCO Frequency = 25 x [NDiv(9:0)+8] / [MDiv(5:0)+2]		X
Bit 6	-	N Div6		RW			X
Bit 5	-	N Div5		RW			X
Bit 4	-	N Div4		RW			X
Bit 3	-	N Div3		RW			X
Bit 2	-	N Div2		RW			X
Bit 1	-	N Div1		RW			X
Bit 0	-	N Div0		RW			X

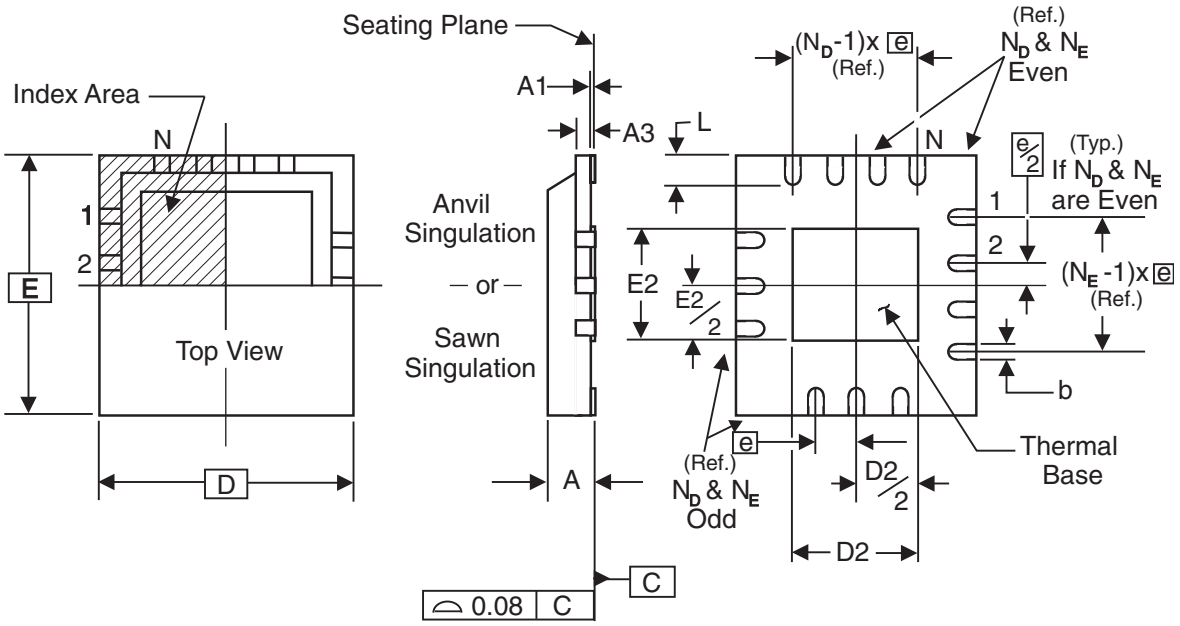
SMBus Table: DOT PLL Spread Spectrum Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	Spread Spectrum Programming b(7:0)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 6	-	SSP6		RW			X
Bit 5	-	SSP5		RW			X
Bit 4	-	SSP4		RW			X
Bit 3	-	SSP3		RW			X
Bit 2	-	SSP2		RW			X
Bit 1	-	SSP1		RW			X
Bit 0	-	SSP0		RW			X

SMBus Table: DOT PLL Spread Spectrum Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	Reserved						0
Bit 6	-	SSP14	Spread Spectrum Programming b(14:8)	RW	These Spread Spectrum bits in Byte 19 and 20 will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.		X
Bit 5	-	SSP13		RW			X
Bit 4	-	SSP12		RW			X
Bit 3	-	SSP11		RW			X
Bit 2	-	SSP10		RW			X
Bit 1	-	SSP9		RW			X
Bit 0	-	SSP8		RW			X

Bytes 19:21 are reserved.



THERMALLY ENHANCED, VERY THIN, FINE PITCH

QUAD FLAT / NO LEAD PLASTIC PACKAGE

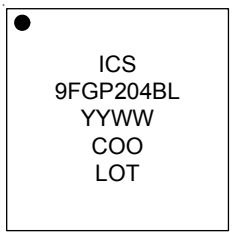
DIMENSIONS

SYMBOL	MIN.	MAX.
A	0.8	1.0
A1	0	0.05
A3	0.25 Reference	
b	0.1 8	0.3
e	0.50 BASIC	

DIMENSIONS

SYMBOL	(JEDEC reference only) VJJD-2 / -5	(IDT package) 40L TOLERANCE
N	40	40
N_D	1 0	1 0
N_E	1 0	1 0
D x E BASIC	6.00 x 6.00	6.00 x 6.00
D2 MIN. / MAX.	1.75 / 4.80	2.75 / 3.0
E2 MIN. / MAX.	1.75 / 4.80	2.75 / 3.0
L MIN. / MAX.	0.30 / 0.50	0.3 / 0.5

Marking Diagram



Notes:
1. “LOT” is the lot sequence number.
2. “COO” denotes country of origin.
3. “YYWW” is the last two digits of the year and week that the part was assembled.
4. “L” denotes RoHS compliant package.

Ordering Information

Part / Order Number	Shipping Packaging	Package	Temperature
9FGP204BKLF	Trays	40-pin MLF	0 to +70° C
9FGP204BKLFT	Tape and Reel	40-pin MLF	0 to +70° C

Parts that are ordered with an “LF” to the suffix are the Pb-Free configuration and are RoHS compliant.

Revision History

Rev.	Issue Date	Who	Description	Page #
A	4/7/2010	RDW	1. Updated Series Termination values and highlighted values are for Zo = 50 ohms. 2. Raised Idd MAX to 225mA from 200 mA 3. Adding Rise/Fall Matching spec to CPU and DOT96SS Electrical Tables. 4. Removed All CPU frequencies except 100 from CPU Electrical Table. 5. Updated Min/Max clock periods to reflect new 50 ps cycle to cycle jitter limit on CPU output. 4. Updated electrical tables with typical values from char report.	4, 7, 8, 9, 10, 11
B	8/29/2011	RDW	1. Removed OE pins for RMII from the block diagram.	3
C	4/23/2015	RDW	Added marking diagram and associated notes	

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