THE DATASHEET OF

89HT0832PZCHLG

89HT0832P Signal Retimer

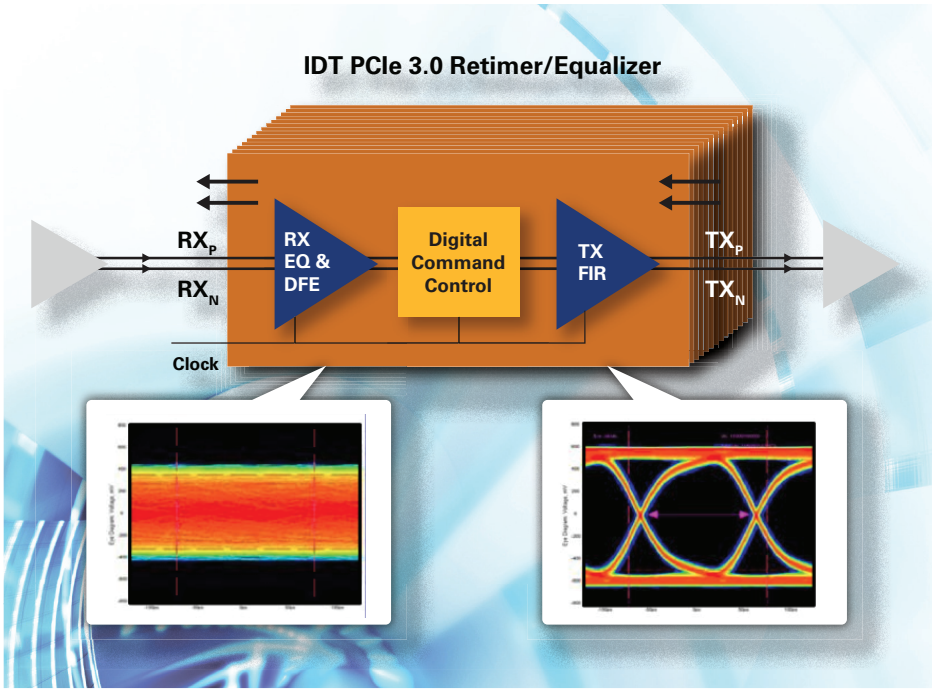
32 Channel PCIe® Signal Retimers for 8.0Gbps, 5.0Gbps and 2.5Gbps

Integrated Device Technology

ANALOG AND RF | **INTERFACE AND CONNECTIVITY** | MEMORY AND LOGIC | POWER MANAGEMENT | TIMING AND SYNCHRONIZATION

FEATURES

- **High Performance Retimer**
  - Fullly complies with new PCIe 3.0 link equalization procedure
  - Eliminates random input jitter (R_j)
  - Eliminates deterministic ISI jitter (D_j)
  - Compensates for PCB trace and cable attenuations
  - Performance and power tunable for each data rate
  - Multi-stage RX equalizer: CTLE and 5 tap DFE
  - 4-tap TX FIR filter implement boost, preshoot and deemphasis fully compliant with PCIe 3:0 standard
  - Wide swing, transmit driver offers up to 8dB of transmi deemphasis to meet the needs of the most challenging of backplanes
- **PCIe Standards and Compatibility**
  - PCI Express Base Specification 3.0 compliant
  - PCI Express Base Specification 2.1 compliant
- **Power Management**
  - Low power
  - Supports the following optional PCI Express features
    - L0s ASPM
    - L1 ASPM
- **Hot Plug Support**
- **SerDes Power Savings**
  - Supports low swing (half-swing) SerDes operation
  - SerDes associated with unused lanes are placed in a low power state automatically
- **Link Configurability**
  - Links can be configured as 1x16, 2x8, 4x4, 1x8 & 2x4
  - Automatic per port link width negotiation (e.g., a x16 port can link train to x16, x8, x4, or x1)
  - Per-lane SerDes configuration
- **Clocking**
  - Uses standard 100 MHz PCIe reference clock
  - SSCLK (Spread Spectrum Clocking) supported with common clock configuration
  - Non-SSCLK supported with common and non-common clock configuration
- **I²C Interface**
  - Dedicated master interface
    - External EEPROM configuration loading
  - Dedicated slave interface
    - Configuration loading
    - Writing new or initial image into external EEPROM
    - Expose internal global CSR space to system controller
- **Reliability, Availability and Serviceability (RAS)**
  - Physical layer error checking and accounting
  - End-to-end data path parity protection
  - Checksum Serial EEPROM content protected
- **Test and Debug**
  - All registers accessible from I²C, or JTAG port
  - Supports IEEE 1149.6 AC JTAG and IEEE 1149.1 JTAG
  - SERDES Rx eye generation (on-chip)
  - Several loopback modes
  - Pattern generator/checker
- Packaged in a 20x13mm, 345-pin CABGA, 0.8mm ball spacing



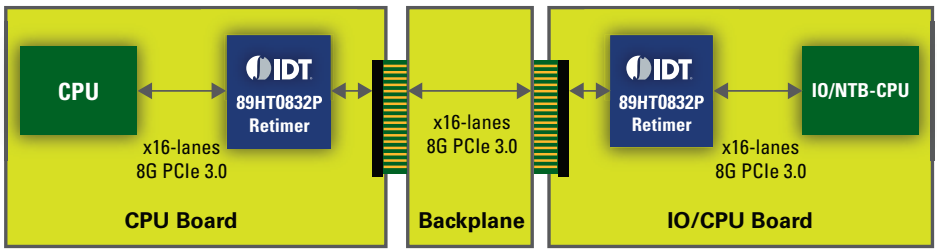
General Description

The 89HT0832P (T0832P) is a Signal Retimer/Conditioner used to improve signal integrity for enhancing system performance and reliability across long PCB traces or cables. It removes both random and deterministic jitter from the input signal eliminating inter-symbol interference, and resets the output jitter budget. The new PCIe 3.0 equalization procedure is fully supported, including phase 2 and 3, on both channel segments. The T0832P provides 32 differential, 8Gbps PCIe Express® 3.0 channels, supporting up to 16 full lanes. The Retimer also fully supports PCIe Express 5Gbps and 2.5Gbps features. The T0832P is targeted to meet the high-performance needs of PCIe® Gen 3/2/1 applications.

Applications

IDT's Retimer products fit into server, storage, blade and communication products.

T0832P System Diagram



Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View 89HT0832PZCHLG on WIN SOURCE
- IDT, Integrated Device Technology Inc Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management