WINSOURCE ELECTRONICS

# THE DATASHEET OF

# 8535AGI-31LF

# Low Skew, 1-To-4, Crystal Oscillator/LVCMOS-To-3.3V LVPECL Fanout Buffer

# ICS8535I-31

## General Description

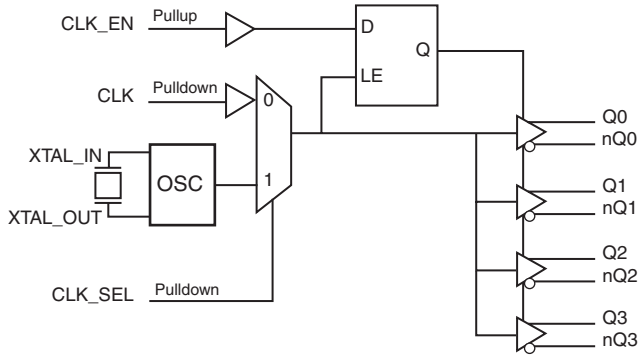
The ICS8535I-31 is a low skew, high performance 1-to-4 3.3V Crystal Oscillator/LVCMOS-to-3.3V LVPECL fanout buffer. The ICS8535I-31 has selectable single ended clock or crystal inputs. The single ended clock input accepts LVCMOS or LVTTL input levels and translate them to 3.3V LVPECL levels. The output enable is internally synchronized to eliminate runt pulses on the outputs during asynchronous assertion/deassertion of the clock enable pin.

Guaranteed output and part-to-part skew characteristics make the ICS8535I-31 ideal for those applications demanding well defined performance and repeatability.

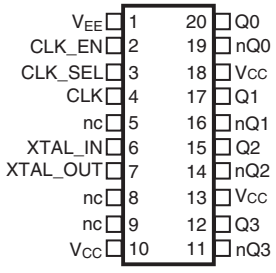
## Features

- Four differential 3.3V LVPECL outputs
- Selectable LVCMOS/LVTTL CLK or crystal inputs
- CLK can accept the following input levels: LVCMOS, LVTTL
- Maximum output frequency: 266MHz
- Output skew: 30ps (typical)
- Part-to-part skew: 200ps (maximum)
- Propagation delay: 1.75ns (maximum)
- Additive phase jitter, RMS: 0.057ps (typical)
- Full 3.3V supply mode
- -40°C to 85°C ambient operating temperature
- Replaces the ICS8535I-11
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

## Block Diagram




## Pin Assignment




**ICS8535I-31**

**20-Lead TSSOP**
**6.5mm x 4.4mm x 0.92mm package body**
**G Package**
**Top View**

## Table 1. Pin Descriptions

| Number | Name | Type | | Description |
|---|---|---|---|---|
| 1 | $V_{EE}$ | Power | | Negative supply pin. |
| 2 | CLK_EN | Input | Pullup | Synchronizing clock enable. When HIGH, clock outputs follows clock input. When LOW, Q outputs are forced low, nQ outputs are forced high. LVCMOS / LVTTL interface levels. |
| 3 | CLK_SEL | Input | Pulldown | Clock select input. When HIGH, selects XTAL inputs When LOW, selects CLK input. LVCMOS / LVTTL interface levels. |
| 4 | CLK | Input | Pulldown | Single-ended clock input. LVCMOS/LVTTL interface levels. |
| 5, 8, 9 | nc | Unused | | No connect. |
| 6, 7 | XTAL_IN, XTAL_OUT | Input | | Crystal oscillator interface. XTAL_IN is the input. XTAL_OUT is the output. |
| 10, 13, 18 | $V_{CC}$ | Power | | Positive supply pins. |
| 11, 12 | nQ3, Q3 | Output | | Differential output pair. LVPECL interface levels. |
| 14, 15 | nQ2, Q2 | Output | | Differential output pair. LVPECL interface levels. |
| 16, 17 | nQ1, Q1 | Output | | Differential output pair. LVPECL interface levels. |
| 19, 20 | nQ0, Q0 | Output | | Differential output pair. LVPECL interface levels. |

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

## Table 2. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | | | 4 | | pF |
| $R_{PULLUP}$ | Input Pullup Resistor | | | 51 | | kΩ |
| $R_{PULLDOWN}$ | Input Pulldown Resistor | | | 51 | | kΩ |

# Function Tables

**Table 3A. Control Input Function Table**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| **CLK_EN** | **CLK_SEL** | **Selected Source** | **Q0:Q3** | **nQ0:nQ3** |
| 0 | 0 | CLK0 | Disabled; Low | Disabled; High |
| 0 | 1 | CLK1 | Disabled; Low | Disabled; High |
| 1 | 0 | CLK0 | Enabled | Enabled |
| 1 | 1 | CLK1 | Enabled | Enabled |

After CLK_EN switches, the clock outputs are disabled or enabled following a rising and falling input clock or crystal oscillator edge as shown in *Figure 1.* In the active mode, the state of the outputs are a function of the CLK input as described in *Table 3B.*

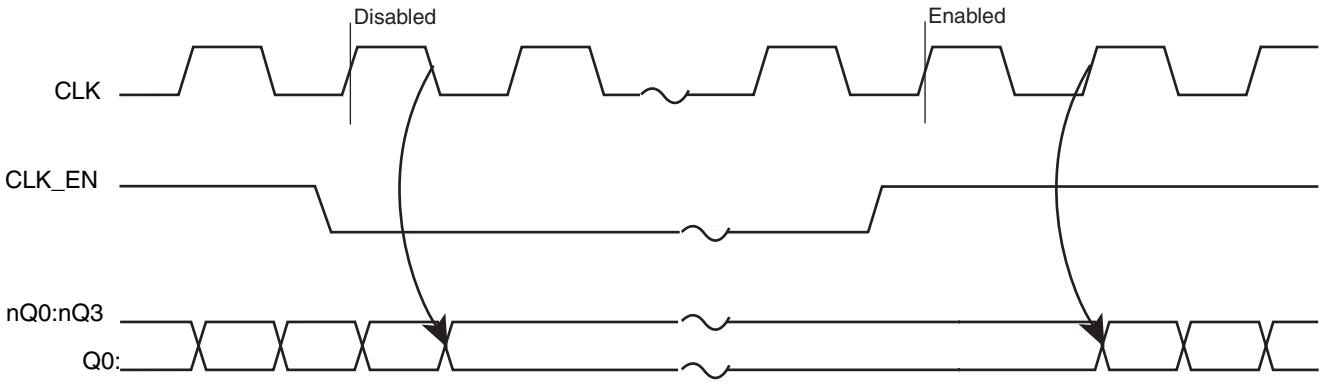



**Figure 1. CLK_EN Timing Diagram**

**Table 3B. Clock Input Function Table**

| Inputs | Outputs | |
|---|---|---|
| **CLK** | **Q0:Q3** | **nQ0:nQ3** |
| 0 | LOW | HIGH |
| 1 | HIGH | LOW |

## Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

| Item | Rating |
|---|---|
| Supply Voltage, $V_{CC}$ | 4.6V |
| Inputs, $V_I$ | -0.5V to $V_{CC}$ + 0.5V |
| Outputs, $I_O$<br>Continuos Current<br>Surge Current | <br>50mA<br>100mA |
| Package Thermal Impedance, $\theta_{JA}$ | 73.2°C/W (0 lfpm) |
| Storage Temperature, $T_{STG}$ | -65°C to 150°C |

## DC Electrical Characteristics

**Table 4A. Power Supply DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Core Supply Voltage | | 3.135 | 3.3 | 3.465 | V |
| $I_{EE}$ | Power Supply Current | | | | 65 | mA |

**Table 4B. LVCMOS/LVTTL DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | | 2 | | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | | -0.3 | | 0.8 | V |
| $I_{IH}$ | Input High Current | CLK, CLK_SEL | $V_{CC}$ = $V_{IN}$ = 3.465V | | | 150 | µA |
| | | CLK_EN | $V_{CC}$ = $V_{IN}$ = 3.465V | | | 5 | µA |
| $I_{IL}$ | Input Low Current | CLK, CLK_SEL | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -5 | | | µA |
| | | CLK_EN | $V_{CC}$ = 3.465V, $V_{IN}$ = 0V | -150 | | | µA |

**Table 4C. LVPECL DC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage; NOTE 1 | | $V_{CC}$ – 1.4 | | $V_{CC}$ – 0.9 | V |
| $V_{OL}$ | Output Low Voltage; NOTE 1 | | $V_{CC}$ – 2.0 | | $V_{CC}$ – 1.7 | V |
| $V_{SWING}$ | Peak-to-Peak Output Voltage Swing | | 0.6 | | 1.0 | V |

NOTE 1: Outputs terminated with 50Ω to $V_{CC}$ – 2V

**Table 5. Crystal Characteristics**

| Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|
| Mode of Oscillation | | Fundamental | | | |
| Frequency | | 12 | | 40 | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitance | | | | 7 | pF |
| Drive Level | | | | 1 | mW |

# AC Electrical Characteristics

**Table 6. AC Characteristics,** $V_{CC}$ = 3.3V ± 5%, $T_A$ = -40°C to 85°C

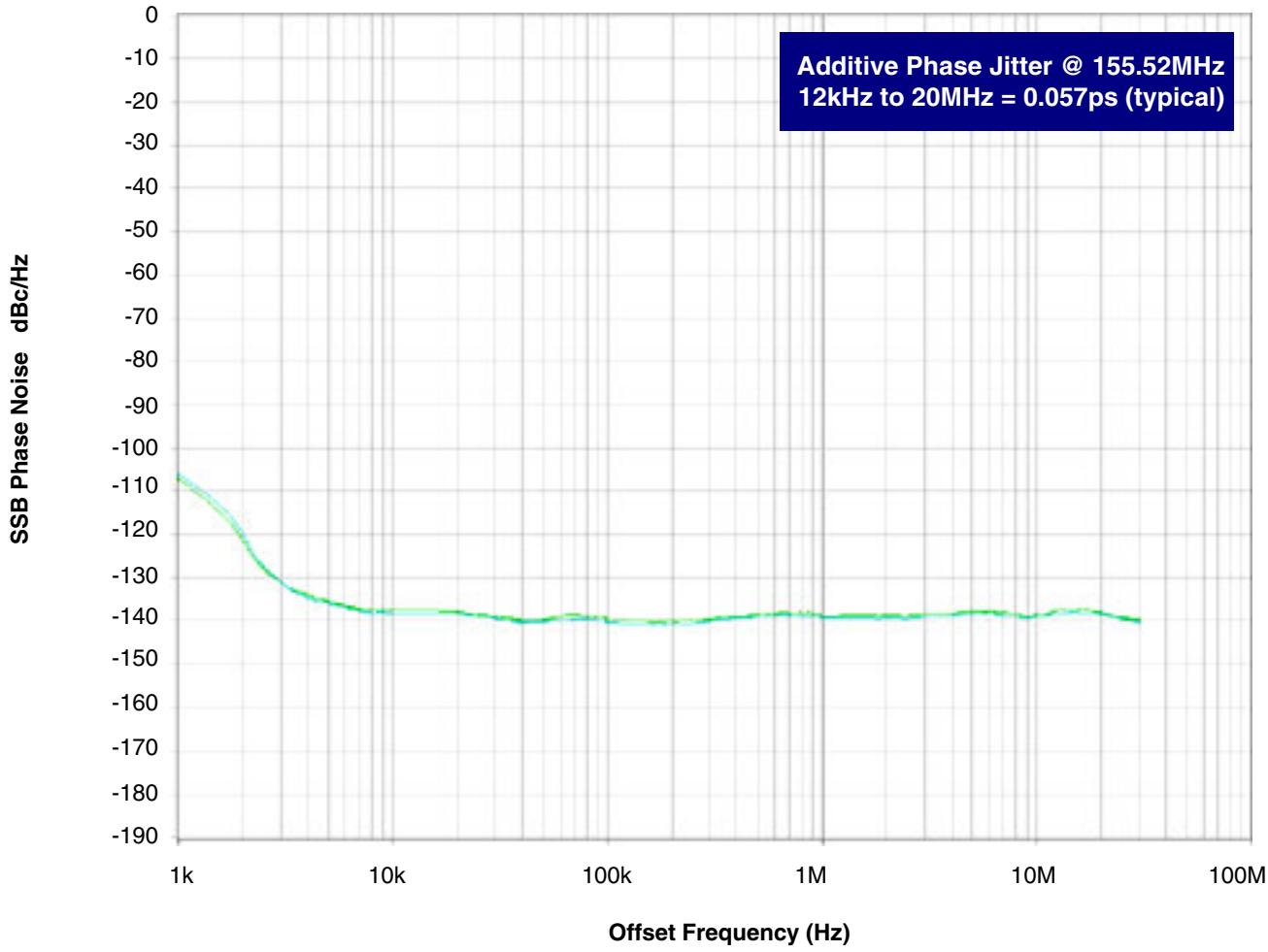
| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Units |
|---|---|---|---|---|---|---|
| $f_{MAX}$ | Output Frequency | | | | 266 | MHz |
| $t_{PD}$ | Propagation Delay; NOTE 1 | | 1.4 | | 1.75 | ns |
| *t*jit | Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section | 155.52MHz, Integration Range: 12kHz – 20MHz | | 0.057 | | ps |
| *t*sk(o) | Output Skew; NOTE 2, 3 | | | 30 | | ps |
| *t*sk(pp) | Part-to-Part Skew; NOTE 3, 4 | | | | 200 | ps |
| $t_R$ / $t_F$ | Output Rise/Fall Time | 20% to 80% | 300 | | 600 | ps |
| odc | Output Duty Cycle | | 46 | | 54 | % |

All parameters measured at $f \leq$ 266MHz unless noted otherwise.
NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE 1: Measured from $V_{CC}$/2 of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at the differential output crossing point.
NOTE 3: This parameter is defined in accordance with JEDEC Standard 65.
NOTE 4: Defined as skew between outputs on different devices operating at the same supply voltage and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

## Additive Phase Jitter

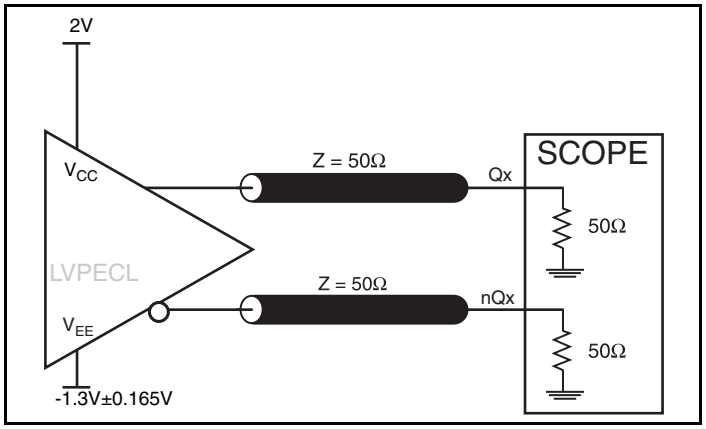
The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.



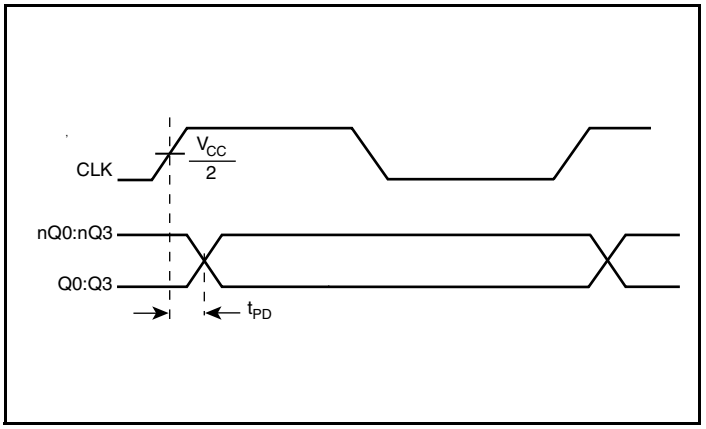

As with most timing specifications, phase noise measurements has issues relating to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependent on the input source and measurement equipment.

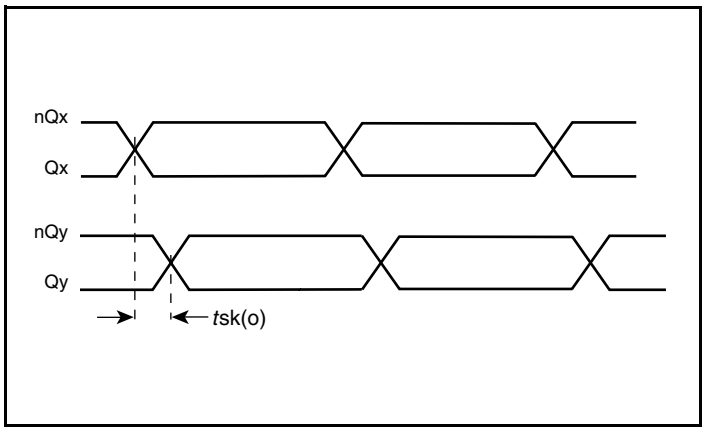
# Parameter Measurement Information



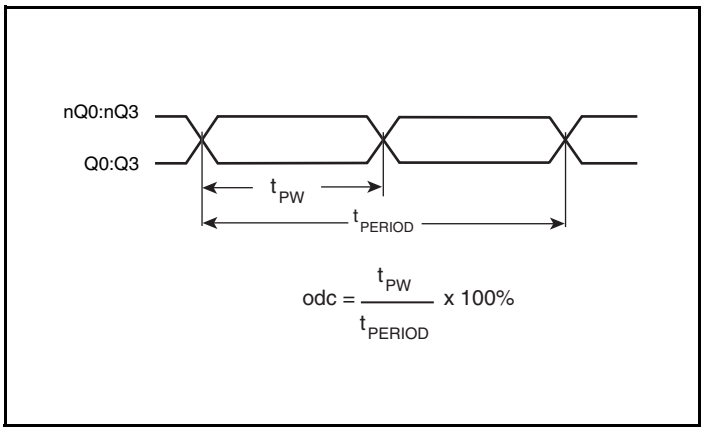

**3.3V Core/3.3V Output Load AC Test Circuit**



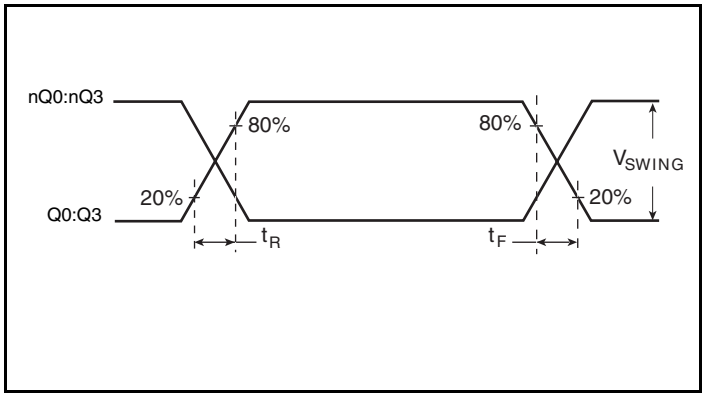

**Propagation Delay**




**Output Skew**




**Output Duty Cycle/Pulse Width/Period**




**Output Rise/Fall Time**

# Application Information

## Recommendations for Unused Input and Output Pins

### Inputs:

#### Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

#### CLK Input

For applications not requiring the use of a clock input, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the CLK to ground.

#### LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

### Outputs:

#### LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

## Crystal Input Interface

The ICS8535I-31 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using an 18pF parallel resonant crystal and were chosen to minimize the ppm error.

These same capacitor values will tune any 18pF parallel resonant crystal over the frequency range and other parameters specified in this data sheet. The optimum C1 and C2 values can be slightly adjusted for different board layouts

.

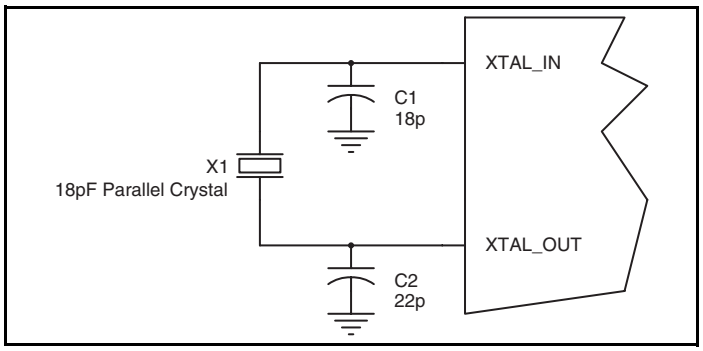



**Figure 2. Crystal Input Interface**

## LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is guaranteed by using a quartz crystal.

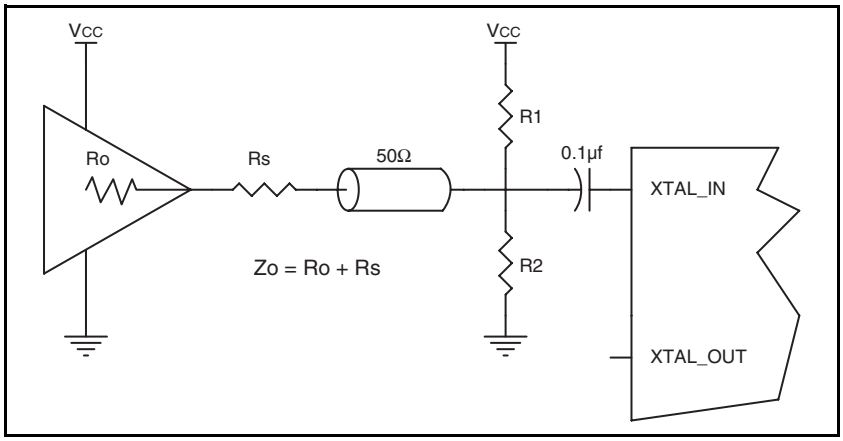



**Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface**

## Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

The differential outputs are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

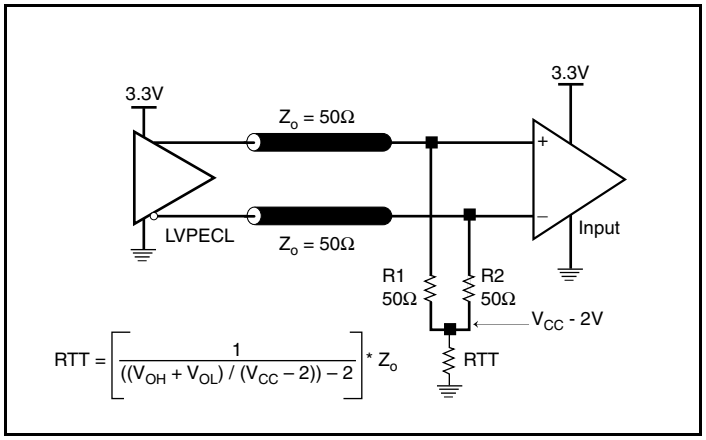



**Figure 4A. 3.3V LVPECL Output Termination**

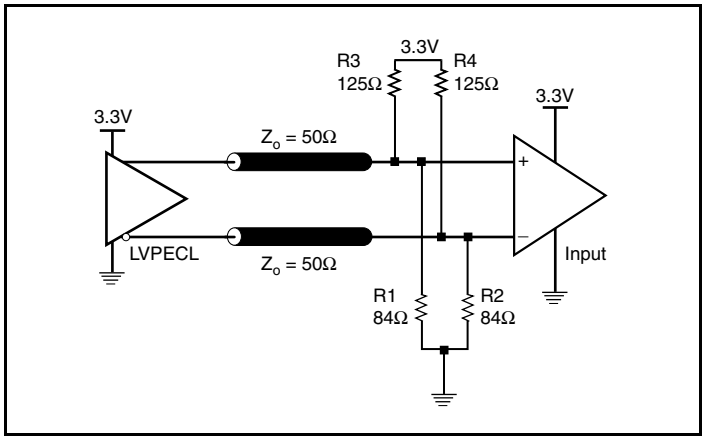



**Figure 4B. 3.3V LVPECL Output Termination**

# Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8535I-31.
Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8535I-31 is the sum of the core power plus the power plus the power dissipated in the load(s).
The following is the power dissipation for $V_{CC}$ = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = $V_{CC\_MAX}$ * $I_{EE\_MAX}$ = 3.465V * 65mA = **225.2mW**
- Power (outputs)$_{MAX}$ = **30mW/Loaded Output Pair**

  If all outputs are loaded, the total power is 4 * 30mW = 120mW

**Total Power**$_{\_MAX}$ (3.465V, with all outputs switching) = 225.2mW + 120mW = **345.2mW**

### 2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = $\theta_{JA}$ * Pd_total + $T_A$

Tj = Junction Temperature

$\theta_{JA}$ = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

$T_A$ = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance $\theta_{JA}$ must be used. Assuming a moderate air flow of 200 linear feet per meter and a multi-layer board, the appropriate value is 66.6°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.345W * 66.6°C/W = 108°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

**Table 7. Thermal Resistance $\theta_{JA}$ for 20 Lead TSSOP, Forced Convection**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per minute | **0** | **200** | **500** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

**3. Calculations and Equations.**

The purpose of this section is to calculate the power dissipation for the LVPECL output pairs.

LVPECL output driver circuit and termination are shown in *Figure 5.*

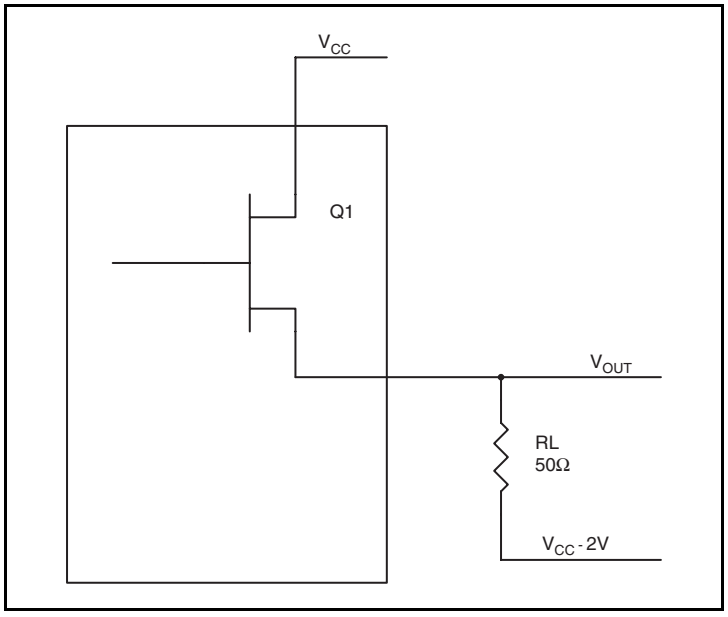



**Figure 5. LVPECL Driver Circuit and Termination**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of $V_{CC}$ – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} =$ **$V_{CC\_MAX}$ – 0.9V**
  ($V_{CC\_MAX} – V_{OH\_MAX}$) = **0.9V**
- For logic low, $V_{OUT} = V_{OL\_MAX} =$ **$V_{CC\_MAX}$ – 1.7V**
  ($V_{CC\_MAX} – V_{OL\_MAX}$) = **1.7V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V - (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
[(2V - 0.9V)/50Ω] * 0.9V = **19.8mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
[(2V – 1.7V)/50Ω] * 1.7V = **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

## Reliability Information

**Table 8. $\theta_{JA}$ vs. Air Flow Table for a 20 Lead TSSOP**

| $\theta_{JA}$ by Velocity | | | |
|---|---|---|---|
| Linear Feet per minute | **0** | **200** | **500** |
| Multi-Layer PCB, JEDEC Standard Test Boards | 73.2°C/W | 66.6°C/W | 63.5°C/W |

## Transistor Count

The transistor count for ICS8535I-31 is: 428

# Package Outline and Package Dimensions

### Package Outline - G Suffix for 20 Lead TSSOP

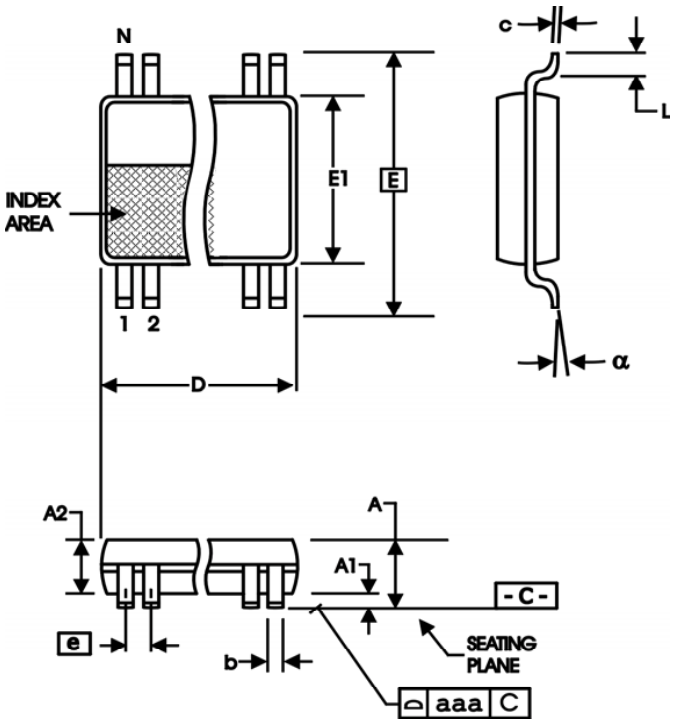



**Table 9. Package Dimensions 20 Lead TSSOP**

| All Dimensions in Millimeters | | |
|---|---|---|
| **Symbol** | **Minimum** | **Maximum** |
| **N** | 20 | |
| **A** | | 1.20 |
| **A1** | 0.05 | 0.15 |
| **A2** | 0.80 | 1.05 |
| **b** | 0.19 | 0.30 |
| **c** | 0.09 | 0.20 |
| **D** | 6.40 | 6.60 |
| **E** | 6.40 Basic | |
| **E1** | 4.30 | 4.50 |
| **e** | 0.65 Basic | |
| **L** | 0.45 | 0.75 |
| $\alpha$ | 0° | 8° |
| **aaa** | | 0.10 |

Reference Document: JEDEC Publication 95, MO-153

## Ordering Information

### Table 10. Ordering Information

| Part/Order Number | Marking | Package | Shipping Packaging | Temperature |
|---|---|---|---|---|
| 8535AGI-31 | ICS8535AGI31 | 20 Lead TSSOP | Tube | -40°C to 85°C |
| 8535AGI-31T | ICS8535AGI31 | 20 Lead TSSOP | 2500 Tape & Reel | -40°C to 85°C |
| 8535AGI-31LF | ICS8535AI31L | “Lead-Free” 20 Lead TSSOP | Tube | -40°C to 85°C |
| 8535AGI-31LFT | ICS8535AI31L | “Lead-Free” 20 Lead TSSOP | 2500 Tape & Reel | -40°C to 85°C |

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

# Revision History Sheet

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| A | <br><br>T10 | 8<br>9<br>13 | Added *Recommendations for Unused Input and Output Pins.*<br>Added *LVCMOS-to-Crystal Interface* section.<br>Ordering Information Table - added lead-free marking. | 8/16/07 |
| A | | 8 | Crystal Input Interface - Updated Drawing | 7/29/09 |
| A | T6 | 5<br>8<br>9 | AC Characteristics Table - added Thermal note.<br>Figure 2, Crystal Input Interface - added C1/C2 values.<br>LVCMOS to XTAL Interface - added new sentence to end of paragraph.<br>Updated Header/Footer throughout the datasheet. | 7/30/09 |
| A | T6 | 5 | AC Characteristics Table heading - corrected temperature from “0 to 70°C” to “-40 to 85°C” | 1/27/10 |

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

**Sales**
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
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