WINSOURCE ELECTRONICS

THE DATASHEET OF

78M6612-IMR/F

19-5348; Rev 2; 1/12

Teridian Smart Grid Solutions

78M6612
Single-Phase, Dual-Outlet Power and Energy Measurement IC

DATA SHEET

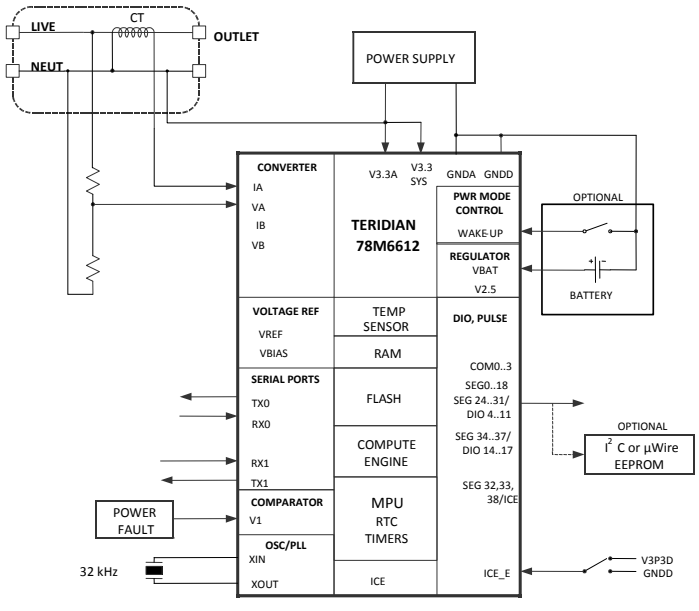
DS_6612_001

DESCRIPTION

The Teridian™ 78M6612 is a highly integrated, single-phase, power and energy measurement and monitoring system-on-chip (SoC) that includes a 32-bit compute engine (CE), an MPU core, RTC, and flash. Our Single Converter Technology® with a 22-bit delta-sigma ADC, four analog inputs, digital temperature compensation, and precision voltage reference supports a wide range of single-phase, dual-outlet power measurement applications with very few external components.

With measurement technology leveraged from Maxim's flagship utility metering ICs, the device offers features including 32 KB of flash program memory, 2 KB shared RAM, three low-power modes with internal timer or external event wake-up, two UARTs, I²C/MICROWIRE® EEPROM I/F, and an in-system programmable flash. Complete outlet measurement unit (OMU) and AC power monitor (AC-PMON) firmware is available or can be preloaded into the IC.

A complete array of ICE and development tools, programming libraries and reference designs enable rapid development and certification of power and energy measurement solutions that meet the most demanding worldwide electricity metering standards.



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MICROWIRE is a registered trademark of National Semiconductor Corp.

FEATURES

- Measures Each Outlet of a Duplex Receptacle with a Single IC
- Provides Complete Energy Measurement and Communication Protocol Capability in a Single IC
- Intelligent Switch Control Capability
- < 0.5% Wh Accuracy Over 2000:1 Current Range and Over Temperature
- Exceeds IEC 62053/ANSIC12.20 Standards
- Voltage Reference < 40 ppm/°C
- Four Sensor Inputs – VDD Referenced
- Low Jitter Wh and VARh Pulse Test Outputs (10 kHz max)
- Pulse Count for Pulse Outputs
- Line Frequency Count for RTC
- Digital Temperature Compensation
- Sag Detection for Phase A and B
- Independent 32-Bit Compute Engine
- 46-64 Hz Line Frequency Range with Same Calibration
- Phase Compensation (±7°)
- Battery Backup for RTC and Battery Monitor
- Three Battery Modes with Wake-Up Timer:
  - Brownout Mode (48 µA)
  - LCD Mode (5.7 µA)
  - Sleep Mode (2.9 µA)
- Energy Display on Main Power Failure
- Wake-Up Timer
- 22-Bit Delta-Sigma ADC
- 8-Bit MPU (80515), 1 Clock Cycle per Instruction with Integrated ICE for MPU Debug
- RTC with Temperature Compensation
- Auto-Calibration
- Hardware watchdog Timer, Power-Fail Monitor
- LCD Driver (Up to 152 Pixels)
- Up to 18 General-Purpose I/O Pins
- 32 kHz Time Base
- 32 KB Flash with Security
- 2 KB MPU XRAM
- Two UARTs
- Digital I/O Pins Compatible with 5 V Inputs
- 64-Pin LQFP or 68-Pin QFN Package
- RoHS-Compliant (6/6) Lead(Pb)-Free Packages
- Complete Application Firmware Available

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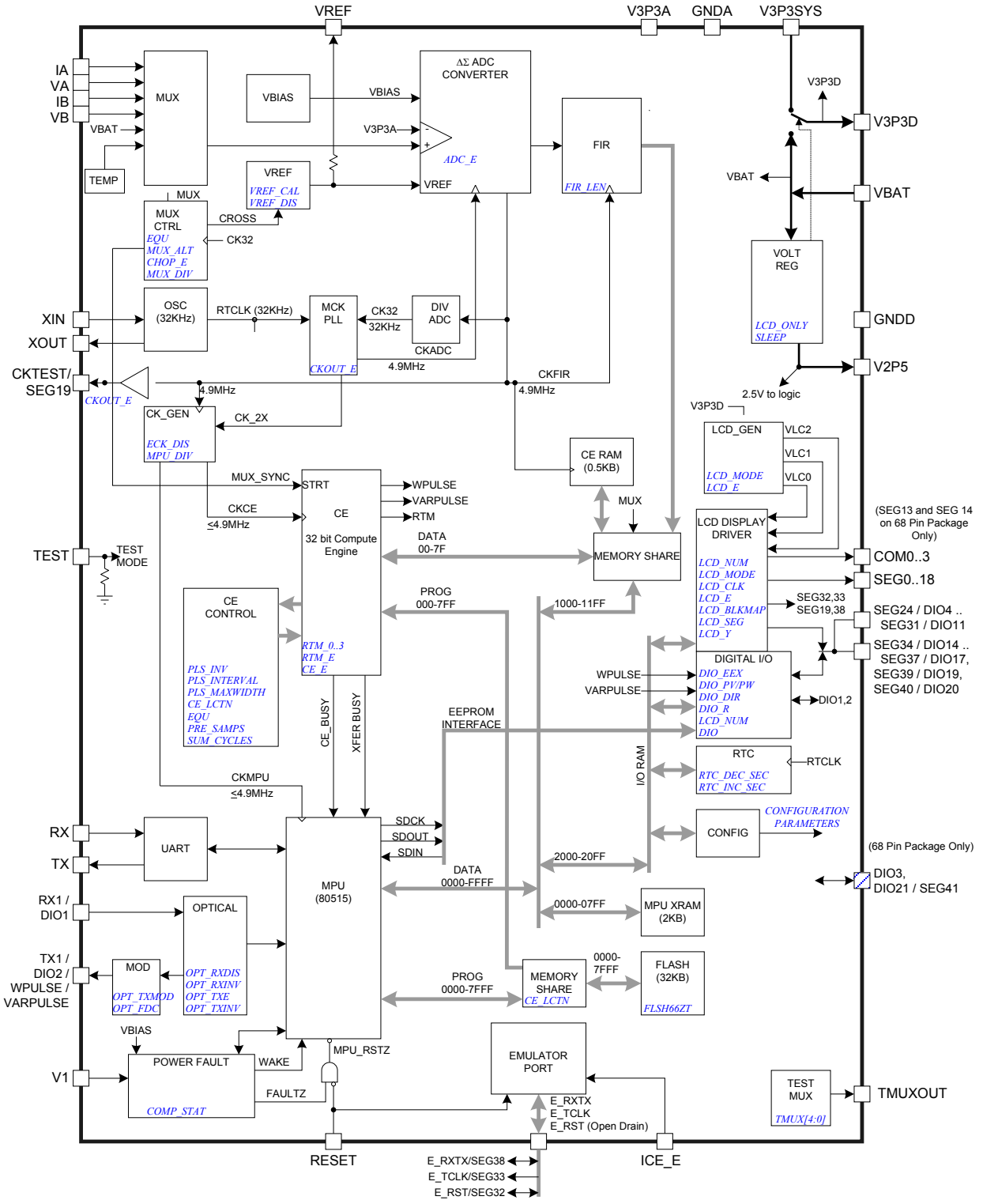


Figure 1: IC Functional Block Diagram

1 Hardware Description

1.1 Hardware Overview

The Teridian 78M6612 single-chip measurement and monitoring IC integrates all the primary AC measurement and control blocks required to implement a solid-state electricity Power and Energy Measurement function. The 78M6618 includes:

- A four-input analog front end (AFE)
- An independent digital computation engine (CE)
- An 8051-compatible microprocessor (MPU) which executes one instruction per clock cycle (80515)
- A precision voltage reference
- A temperature sensor
- LCD drivers
- RAM and Flash memory
- A real time clock (RTC)
- A variety of I/O pins

Various current sensor technologies are supported including Current Transformers (CT), and Resistive Shunts.

In a typical application, the 32-bit compute engine (CE) of the 78M6612 sequentially processes the samples from the analog inputs on pins IA, VA, IB, VB and performs calculations to measure active energy (Wh), reactive energy (VARh), A^2h, and V^2h for four-quadrant measurement. These measurements are then accessed by the MPU, processed further, and output using the peripheral devices available to the MPU.

In addition to advanced measurement functions, the real time clock function allows the 78M6612 to record time of use (TOU) measurement information for multi-rate applications and to time-stamp events. Measurements can be displayed on 3.3 V LCDs if desired. Flexible mapping of LCD display segments will facilitate utilization of existing custom LCDs. Design trade-off between number of LCD segments vs. DIO pins can be implemented in software to accommodate various requirements.

In addition to the temperature-trimmed ultra-precision voltage reference, the on-chip digital temperature compensation mechanism includes a temperature sensor and associated controls for correction of unwanted temperature effects on measurement and RTC accuracy, e.g. to meet the requirements of ANSI and IEC standards. Temperature-dependent external components such as crystal oscillator, current transformers (CTs), and their corresponding signal conditioning circuits can be characterized and their correction factors can be programmed to produce measurements with exceptional accuracy over the industrial temperature range.

A block diagram of the IC is shown in Figure 1. A detailed description of various functional blocks follows.

1.2 Analog Front End (AFE)

The AFE functions as a data acquisition system, controlled by the MPU. It consists of an input multiplexer, a delta-sigma A/D converter, and a voltage reference. The main signals (IA, VA, IB, VB) are sampled and the ADC counts obtained are stored in CE DRAM where they can be accessed by the CE and, if necessary, by the MPU.

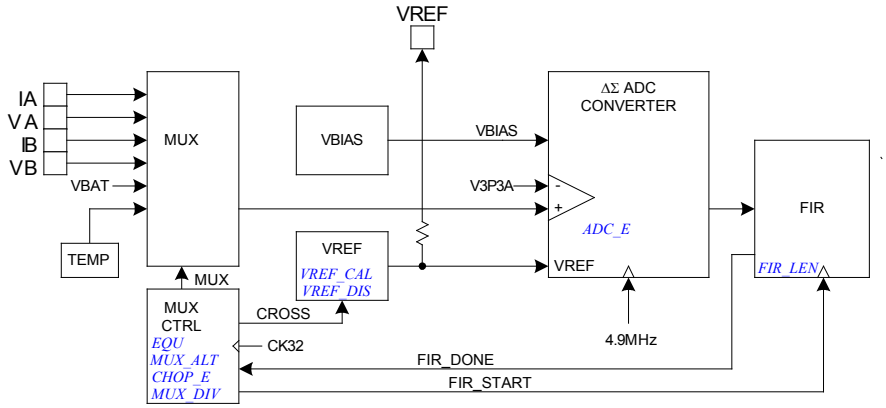


Figure 2: AFE Block Diagram

1.2.1 Input Multiplexer

The input multiplexer supports up to four input signals that are applied to pins IA, VA, IB, and VB of the device. Additionally, using the alternate multiplexer selection, it has the ability to select temperature and the battery voltage. The multiplexer can be operated in two modes:

- During a normal multiplexer cycle, the signals from the IA, IB, VA, and VB pins are selected.
- During the alternate multiplexer cycle, the temperature signal (TEMP) and the battery monitor are selected, along with the signal sources shown in Table 1. To prevent unnecessary drainage on the battery, the battery monitor is enabled only with the *BME* bit (0x2020[6]) in the I/O RAM.

The alternate multiplexer cycles are usually performed infrequently (e.g. every second or so) by the MPU. In order to prevent disruption of the voltage tracking PLL and voltage allpass networks, VA is not replaced in the ALT mux selections. Table 1 details the regular and alternative multiplexer sequences. Missing samples due to an ALT multiplexer sequence are filled in by the CE.

Table 1: Inputs Selected in Regular and Alternate Multiplexer Cycles

	Regular MUX Sequence				ALT MUX Sequence			
	Mux State				Mux State			
EQU	**0**	**1**	**2**	**3**	**0**	**1**	**2**	**3**
2	IA	VA	IB	VB	TEMP	VA	VBAT	VB

In a typical application, IA and IB are connected to current sensors that sense the current on each branch of the line voltage. VA and VB are typically connected to voltage sensors through resistor dividers. The multiplexer control circuit is clocked by CK32, the 32.768 kHz clock from the PLL block, and launches with each new pass of the CE program. The duration of each multiplexer state depends on the number of ADC samples processed by the FIR.

1.2.2 A/D Converter (ADC)

A single delta-sigma A/D converter digitizes the voltage and current inputs to the 78M6612. The resolution of the ADC is configurable to either 21 or 22 bit. At the end of each ADC conversion, the FIR filter output data is stored into the CE RAM location.

1.2.3 FIR Filter

The finite impulse response filter is an integral part of the ADC and it is optimized for use with the multiplexer. The purpose of the FIR filter is to decimate the ADC output to the desired resolution. At the end of each ADC conversion, the output data is stored into the CE RAM location determined by the multiplexer selection. FIR data is stored LSB justified, but shifted left by nine bits.

1.2.4 Voltage References

The device includes an on-chip precision bandgap voltage reference that incorporates auto-zero techniques. The reference is trimmed to minimize errors caused by component mismatch and drift. The result is a voltage output with a predictable temperature coefficient.

1.2.5 Temperature Sensor

The 78M6612 includes an on-chip temperature sensor implemented as a bandgap reference. It is used to determine the die temperature The MPU reads the temperature sensor output during alternate multiplexer cycles. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see Section 3.4 Temperature Compensation).

1.2.6 Battery Monitor

The 78M6618 also has the ability to measure battery voltage by the ADC during alternative multiplexer frames. When set, an on-chip 45 kΩ load resistor is applied to the battery and a scaled fraction of the battery voltage is applied to the ADC input. Battery operating modes are not supported in all firmware libraries. Contact Maxim support for more information.

1.3 Digital Computation Engine (CE)

The CE, a dedicated 32-bit signal processor, performs the precision computations necessary to accurately measure energy. The CE calculations and processes include:

- Multiplication of each current sample with its associated voltage sample to obtain the energy per sample (when multiplied with the constant sample time).
- Frequency-insensitive delay cancellation on all four channels (to compensate for the delay between samples caused by the multiplexing scheme).
- 90° phase shifter (for narrowband VAR calculations).
- Pulse generation.
- Monitoring of the input signal frequency (for frequency and phase information).
- Monitoring of the input signal amplitude (for sag detection).
- Scaling of the processed samples based on calibration coefficients.

CE code is provided by Maxim as a part of the application firmware available. The CE is not programmable by the user. Measurement algorithms in the CE code can be customized by Maxim upon request.

The CE program resides in Flash memory. Allocated Flash space for the CE program cannot exceed 1024 words (2 KB). The CE can access up to 2 KB of data RAM (XRAM), or 512 32-bit data words. The CE is also aided by support hardware to facilitate implementation of equations, pulse counters and accumulators. Usage of this hardware is firmware specific.

1.3.1 Real-Time Monitor

The CE contains a Real-Time Monitor (RTM), which can be programmed to monitor four selectable CE DRAM locations at full sample rate for system debug purposes. The four monitored locations can be serially output to the TMUXOUT pin via the digital output multiplexer at the beginning of each CE code pass. The RTM output is clocked by CKTEST.

1.3.2 Pulse Generator

The CE provides four pulse generators used to output CE status indicators (e.g. SAG) directly to designated DIO pins.

1.3.3 Data RAM (XRAM)

The CE and MPU use a single general-purpose Data RAM (also referred to as XRAM). When the MPU and CE are clocking at maximum frequency (10 MHz), the RAM may be accessed up to four times during each 100 ns interval. These consist of two MPU accesses, one CE access and one SPI access.

1.4 80515 MPU Core

The 78M6612 includes an 80515 MPU (8-bit, 8051-compatible) that processes most instructions in one clock cycle. Using a 5 MHz (4.9152 MHz) clock results in a processing throughput of 5 MIPS. The 80515 architecture eliminates redundant bus states and implements parallel execution of fetch and execution phases. Normally a machine cycle is aligned with a memory fetch, therefore, most of the 1-byte instructions are performed in a single machine cycle (MPU clock cycle). This leads to an 8x average performance improvement (in terms of MIPS) over the Intel® 8051 device running at the same clock frequency. Actual processor clocking speed can be adjusted to the total processing demand of the application (measurement calculations, memory management and I/O management).

Typical power and energy measurement functions based on the results provided by the internal 32-bit compute engine (CE) are available for the MPU as part of Maxim's standard library. A standard ANSI "C" 80515 application program library is available to help reduce design cycle.

1.4.1 UARTs

The 78M6612 includes two UARTs (UART0 and UART1) that can be programmed to communicate with a variety of external devices. The UARTs are dedicated 2-wire serial interfaces, which can communicate at rates up to 38,400 bits/s. All UART transfers are programmable for parity enable, parity, 2 stop bits/1 stop bit and XON/XOFF option for variable communication baud rates from 300 to 38,400 bps.

1.5 On-Chip Resources

1.5.1 Oscillator

The 78M6612 oscillator drives a standard 32.768 kHz watch crystal. These crystals are accurate and do not require a high-current oscillator circuit. The 78M6612 oscillator has been designed specifically to handle these crystals and is compatible with their high impedance and limited power handling capability.

1.5.2 PLL and Internal Clocks

Timing for the device is derived from the 32.768 kHz oscillator output. On-chip timing functions include:

- The MPU master clock
- A real time clock (RTC)
- The delta-sigma sample clock.

The two general-purpose counter/timers are contained in the MPU.

The ADC master clock, CKADC, is generated by an on-chip PLL. It multiplies the oscillator output frequency (CK32) by 150.

The CE clock frequency is always CK32 * 150, or 4.9152 MHz, where CK32 is the 32 kHz clock. The MPU clock frequency is determined by MPU_DIV and can be 4.9152 MHz *2^{-MPU_DIV} Hz where MPU_DIV varies from 0 to 7 (MPU_DIV is 0 on power-up). This makes the MPU clock scalable from 4.9152 MHz down to 38.4 kHz. The circuit also generates a 2x MPU clock for use by the emulator. This 2x MPU clock is not generated when ECK_DIS is asserted by the MPU.

The setting of MPU_DIV is maintained when the device transitions to BROWNOUT mode, but the time base in BROWNOUT mode is 28,672 Hz.

1.5.3 Real-Time Clock (RTC)

The RTC is driven directly by the crystal oscillator. The RTC consists of a counter chain and output registers. The counter chain consists of seconds, minutes, hours, day of week, day of month, month, and year. The RTC is not supported in all firmware libraries. Contact Maxim support for more information.

1.5.4 Temperature Sensor

The device includes an on-chip temperature sensor for determining the temperature of the bandgap reference. The MPU may request an alternate multiplexer frame containing the temperature sensor output by asserting *MUX_ALT*. The primary use of the temperature data is to determine the magnitude of compensation required to offset the thermal drift in the system (see Section 3.4 Temperature Compensation).

1.5.5 Flash Memory

The 78M6612 includes 32 KB of on-chip Flash memory. The Flash memory primarily contains MPU and CE program code. It also contains images of the CE DRAM, MPU RAM, and I/O RAM. On power-up, before enabling the CE, the MPU copies these images to their respective locations.

The Flash memory is segmented into individually erasable 1024-byte pages. Flash space allocated for the CE program is limited to 1024 words (2 KB). The CE program must begin on a 1-KB boundary of the Flash address space.

Flash Write Procedures

The MPU has the ability to write to the Flash memory when the CE is disabled. As an alternative to using Flash, a small EEPROM can store data without compromises. EEPROM interfaces are included in the device.

Updating Individual Bytes in Flash Memory

The original state of a Flash byte is 0xFF (all ones). Once a value other than 0xFF is written to a Flash memory cell, overwriting with a different value usually requires that the cell be erased first. Since cells cannot be erased individually, the page has to be copied to RAM, followed by a page erase. After this, the page can be updated in RAM and then written back to the Flash memory.

Flash Erase Procedures

Flash erasure is initiated by writing a specific data pattern to specific SFR registers in the proper sequence. These special pattern/sequence requirements prevent inadvertent erasure of the Flash memory.

The mass erase sequence is:

1. Write 1 to the *FLSH_MEEN* bit (SFR address 0xB2[1].
2. Write pattern 0xAA to *FLSH_ERASE* (SFR address 0x94).

The mass erase cycle can only be initiated when the ICE port is enabled.

The page erase sequence is:

1. Write the page address to *FLSH_PGADR* (SFR address 0xB7[7:1].
2. Write pattern 0x55 to *FLSH_ERASE* (SFR address 0x94).

1.5.6 Optical Interface

The device includes an interface to implement an IR/optical port on UART1. The pin TX1 is designed to directly drive an external LED for transmitting data on an optical link. The pin RX1 is designed to sense the input from an external photo detector used as the receiver for the optical link. The IR/optical interface is not supported in all firmware libraries. Contact Maxim support for more information.

1.5.7 Digital I/O

The device includes up to 18 pins (QFN 68 package) or 16 pins (LQFP 64 package) of general purpose digital I/O. These pins are compatible with 5V inputs (no current-limiting resistors are needed). Some of them are dedicated DIO (DIO3), some are dual-function that can alternatively be used as LCD drivers (DIO4-11, 14-17, 19-21) and some share functions with the optical port (DIO1, DIO2). On reset or power-up, all DIO pins are inputs until they are configured for the desired direction under MPU control. The pins are configured by the DIO registers and by the five bits of the *LCD_NUM* register (located in I/O RAM). Once declared as DIO, each pin can be configured independently as an input or output with the *DIO_DIRn* bits. A 3-bit configuration word, *DIO_Rx*, can be used for certain pins, when configured as DIO, to individually assign an internal resource such as an interrupt or a timer control. Table 2 lists the direction registers and configurability associated with each group of DIO pins. Table 3 shows the configuration for a DIO pin through its associated bit in its *DIO_DIR* register.

Tables showing the relationship between *LCD_NUM* and the available segment/DIO pins can be found in Section 3.5 Connecting LCDs and in Section 4.3 I/O Description under *LCD_NUM[4:0]*.

Table 2: Data/Direction Registers and Internal Resources for DIO Pin Groups

DIO	**x**	**1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**
Pin no. (64 LQFP)	–	57	3	–	36	37	38	39	40	41	42	43	–	–	20	21
Pin no. (68 QFN)	–	60	3	5	39	40	41	42	43	44	45	46	–	–	21	22
Data Register	–	1	2	3	4	5	6	7	0	1	2	3	–	–	6	7
	–								*DIO1=P1* (SFR 0x90)							
Direction Register	–	1	2	3	4	5	6	7	0	1	2	3	–	–	6	7
	–								*DIO_DIR1* (SFR 0x91)							
Internal Resources Configurable	–	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	Y	–	–	–	–

DIO	**16**	**17**	**18**	**19**	**20**	**21**	**22**	**23**
Pin no. (64 LQFP)	22	12	–	23	44	–	–	–
Pin no. (68 QFN)	23	13	–	24	47	68		
Data Register	0	1	–	3	4	5	–	–
	DIO2=P2 (SFR 0xA0)							
Direction Register	0	1	–	3	4	5	–	–
	DIO_DIR2 (SFR 0xA1)							
Internal Resources Configurable	N	N	–	N	N	N	–	–

Table 3: *DIO_DIR* Control Bit

	DIO_DIR [n]	
	0	**1**
DIO Pin n Function	Input	Output

Additionally, if DIO6 and DIO7 are declared outputs, they can be configured as dedicated pulse outputs (WPULSE = DIO6, VARPULSE = DIO7) using *DIO_PW* and *DIO_PV* registers. In this case, DIO6 and DIO7 are under CE control. DIO4 and DIO5 can be configured to implement the EEPROM Interface.

If the optical UART is not used, TX1 and RX1 can be configured as dedicated DIO pins (DIO1, DIO2, see Section 1.5.6 Optical Interface).

A 3-bit configuration word, I/O RAM register, *DIO_Rx* (0x2009[2:0] through 0x200E[6:4]) can be used for certain pins, when configured as DIO, to individually assign an internal resource such as an interrupt or a timer control (see Table 2 for DIO pins available for this option). This way, DIO pins can be tracked even if they are configured as outputs.

Tracking DIO pins configured as outputs is useful for pulse counting without external hardware.

When driving LEDs, relay coils etc., the DIO pins should sink the current into ground (as shown in Figure 3, right), not source it from V3P3D (as shown in Figure 3, left). This is due to the resistance of the internal switch that connects V3P3D to either V3P3SYS or VBAT.

When configured as inputs, the dual-function (DIO/SEG) pins should not be pulled above V3P3SYS in MISSION and above VBAT in LCD and BROWNOUT modes. Doing so will distort the LCD waveforms of the other pins. This limitation applies to any pin that can be configured as a LCD driver.

The control resources selectable for the DIO pins are listed in Table 4. If more than one input is connected to the same resource, the resources are combined using a logical OR.

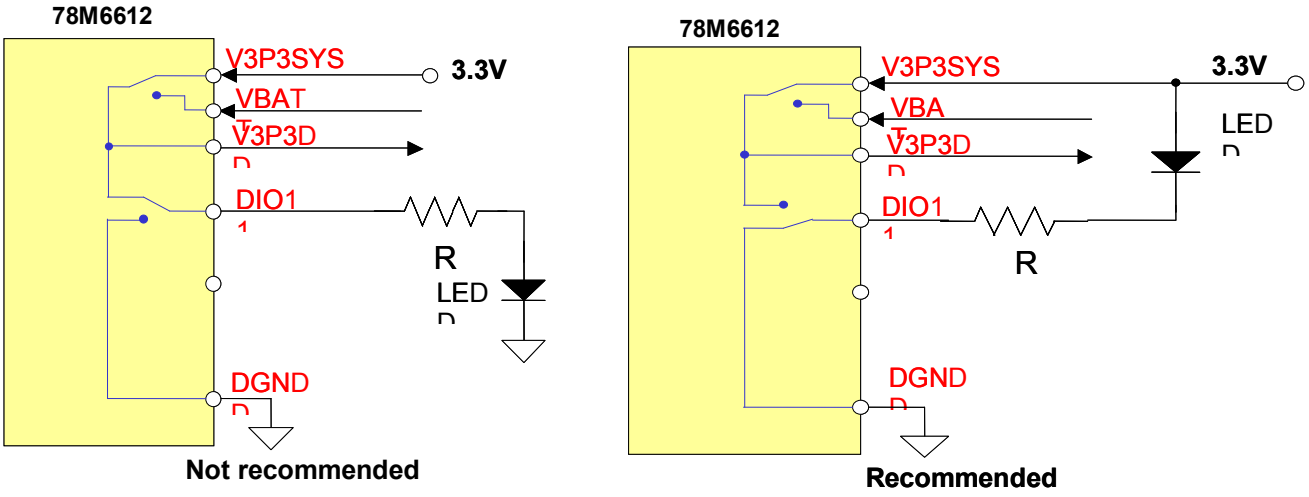


Figure 3: Connecting an External Load to DIO Pins

Table 4: Selectable Controls using the *DIO_DIR* Bits

DIO_R Value	Resource Selected for DIO Pin
0	NONE
1	Reserved
2	T0 (counter0 clock)
3	T1 (counter1 clock)
4	High priority I/O interrupt (INT0 rising)
5	Low priority I/O interrupt (INT1 rising)
6	High priority I/O interrupt (INT0 falling)
7	Low priority I/O interrupt (INT1 falling)

1.5.8 LCD Drivers

The device in the 68-pin QFN package contains 20 dedicated LCD segment drivers in addition to the 18 multi-use pins described above. Thus, the device is capable of driving between 80 to 152 pixels of LCD display with 25% duty cycle (or 60 to 114 pixels with 33% duty cycle). At eight pixels per digit, this corresponds to 10 to 19 digits.

The device in the 64-pin LQFP package contains 18 dedicated LCD segment drivers in addition to the 17 multi-use pins described above. Thus, the device is capable of driving between 72 to 140 pixels of LCD display with 25% duty cycle (or 60 to 105 pixels with 33% duty cycle). At eight pixels per digit, this corresponds to 9 to 17 digits.

The LCD drivers are grouped into four commons and up to 38 segment drivers (68-pin package), or 4 commons and 35 segment drivers (64-pin package). The LCD interface is flexible and can drive either digit segments or enunciator symbols.

Segment drivers SEG18 and SEG19 can be configured to blink at either 0.5 Hz or 1 Hz. The blink rate is controlled by *LCD_Y*. There can be up to four pixels/segments connected to each of these drivers. *LCD_BLKMAP18[3:0]* and *LCD_BLKMAP19[3:0]* identify which pixels, if any, are to blink.

LCD interface memory is powered by the non-volatile supply. The bits of the LCD memory are preserved in LCD and SLEEP modes, even if their pin is not configured as SEG. In this case, they can be useful as general- purpose non-volatile storage.

1.5.9 EEPROM Interface

The 78M6612 provides hardware support for an optional two-pin or a three-wire (µ-wire) EEPROM interface.

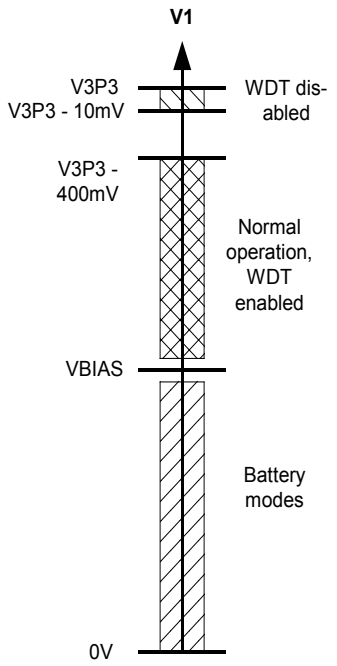
Two-Pin EEPROM Interface

The dedicated 2-pin serial interface communicates with external EEPROM devices. The interface is multiplexed onto the DIO4 (SCK) and DIO5 (SDA) pins.

Three-Wire (µ-Wire) EEPROM Interface

A 500 kHz 3-wire interface, using SDATA, SCK, and a DIO pin for CS is also available.

1.5.10 Hardware Watchdog Timer



In addition to the basic watchdog timer included in the 80515 MPU, an independent, robust, fixed-duration, watchdog timer (WDT) is included in the device. It uses the crystal oscillator as its time base and must be refreshed by the MPU firmware at least every 1.5 seconds. When not refreshed on time the WDT overflows, and the part is reset as if the RESET pin were pulled high, except that the I/O RAM bits will be maintained. 4096 oscillator cycles (or 125 ms) after the WDT overflow, the MPU will be launched from program address 0x0000. Asserting ICR_E will deactivate the WDT.

The WDT can also be disabled by tying the V1 pin to V3P3. Of course, this also deactivates V1 power fault detection. Since there is no method in firmware to disable the crystal oscillator or the WDT, it is guaranteed that whatever state the part might find itself in, upon WDT overflow, the part will be reset to a known state.

Figure 4: Functions Defined by V1

1.5.11 Test Ports (TXUXOUT pin)

One out of 16 digital or 8 analog signals can be selected to be output on the TMUXOUT pin. The function of the multiplexer is described in the applicable firmware documentation.

2 Functional Description

2.1 Theory of Operation

The energy delivered by a power source into a load can be expressed as:

$$E = \int_0^t V(t)I(t)dt$$

The following formulas apply for wide band mode (true RMS):

- P = ∑ (*i*(t) * *v*(t))
- Q = √(S^2 – P^2)
- S = V * I
- V = √∑*v*(t)^2
- I = √∑*i*(t)^2

For actual measurement equations, refer to the applicable *78M6612 Firmware Description Document*.

For some applications, not only voltage and current amplitudes, but also phase angles and harmonic content may change constantly. Thus, simple RMS measurements are inherently inaccurate. A modern solid-state electricity measurement IC such as the 78M6612 functions by emulating the integral operation above, i.e. it processes current and voltage samples through an ADC at a constant frequency. As long as the ADC resolution is high enough and the sample frequency is beyond the harmonic range of interest, the current and voltage samples, multiplied with the time period of sampling will yield an accurate quantity for the momentary energy. Summing up the momentary energy quantities over time will result in accumulated energy.

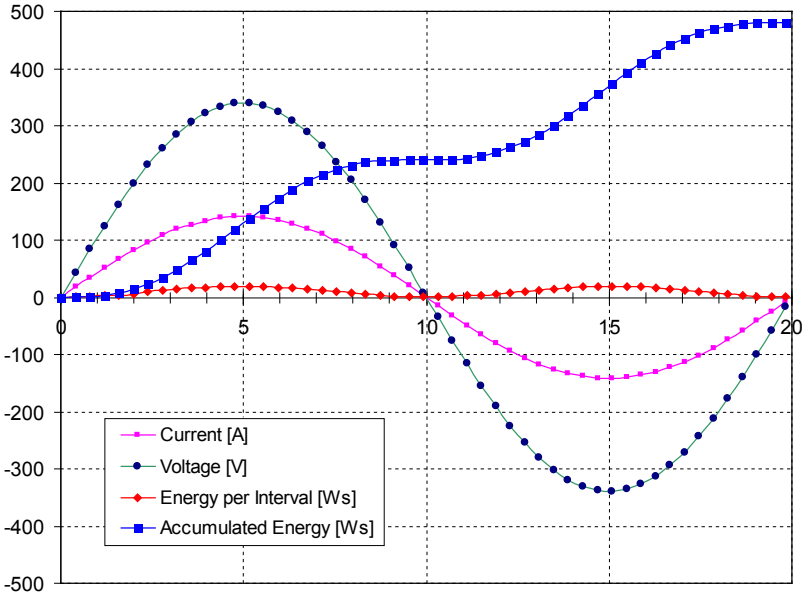


Figure 5: Voltage, Current, Momentary and Accumulated Energy

Figure 5 shows the shapes of V(t), I(t), the momentary power and the accumulated power, resulting from 50 samples of the voltage and current signals over a period of 20 ms. The application of 240 VAC and 100 A results in an accumulation of 480 Ws (= 0.133 Wh) over the 20 ms period, as indicated by the Accumulated Power curve. The described sampling method works reliably, even in the presence of dynamic phase shift and harmonic distortion.

2.2 Fault and Reset Behavior

2.2.1 Reset Mode

When the RESET pin is pulled high, all digital activity stops. The oscillator and RTC module continue to run. Additionally, all I/O RAM bits are set to their default states. As long as V1, the input voltage at the power fault block, is greater than VBIAS, the internal 2.5 V regulator continues to provide power to the digital section.

Once initiated, the reset mode persists until the reset timer times out. This occurs in 4096 cycles of the real time clock after RESET goes low, at which time the MPU begins executing its preboot and boot sequences from address 00.

2.2.2 Power Fault Circuit

The 78M6612 includes a comparator to monitor system power fault conditions. When the output of the comparator falls (V1<VBIAS), the PLL status bits in the I/O RAM are zeroed and the IC power downs. Once system power returns, the MPU remains in reset and does not start until 2048 to 4096 CK32 clock cycles later. Program execution starts at address 0x00. MPU RAM will be re-initialized.

2.3 Data Flow

The data flow between the Compute Engine (CE) and the MPU is shown in Figure 6. In a typical application, the 32-bit CE sequentially processes the samples from the current and voltage inputs on pins IA, VA, IB, and VB, performing calculations to measure active power (Wh), reactive power (VARh), A^2h, and V^2h for four-quadrant measurement. These measurements are then accessed by the MPU, processed further and output using the peripheral devices available to the MPU.

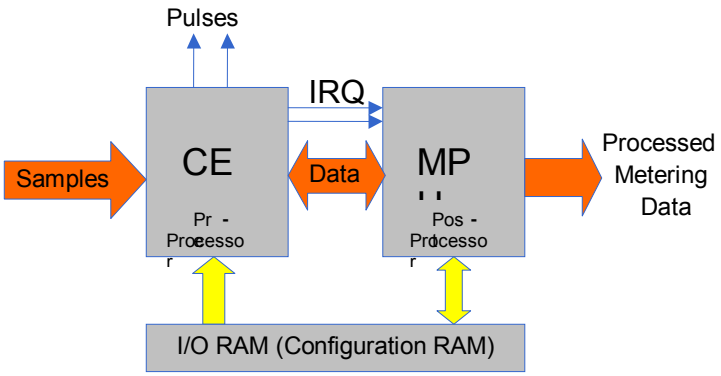


Figure 6: MPU/CE Data Flow

2.4 CE/MPU Communication

Figure 7 shows the functional relationship between the CE and the MPU. The CE is controlled by the MPU via shared registers in the I/O RAM and RAM. The CE outputs two interrupt signals to the MPU to indicate the CE is actively processing data and the CE is updating data to the output region of the RAM.

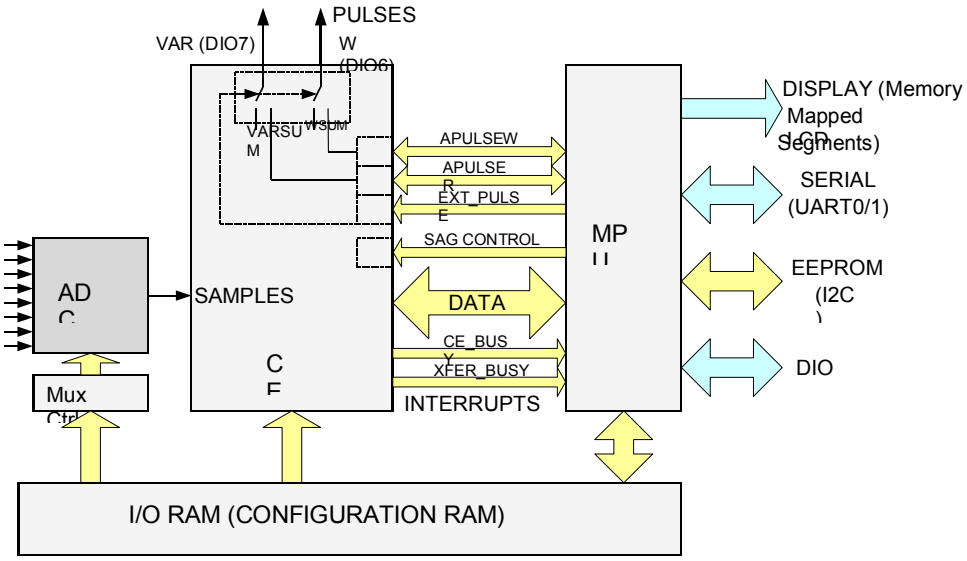


Figure 7: MPU/CE Communication

3 Application Information

3.1 Connection of Sensors (CT, Resistive Shunt)

Figure 8, Figure 9, and Figure 10 show how resistive voltage dividers, resistive current shunts, and current transformers are connected to the voltage and current inputs of the 78M6612.

$$V_{out} = V_{in} * R_{out}/(R_{out} + R_{in})$$

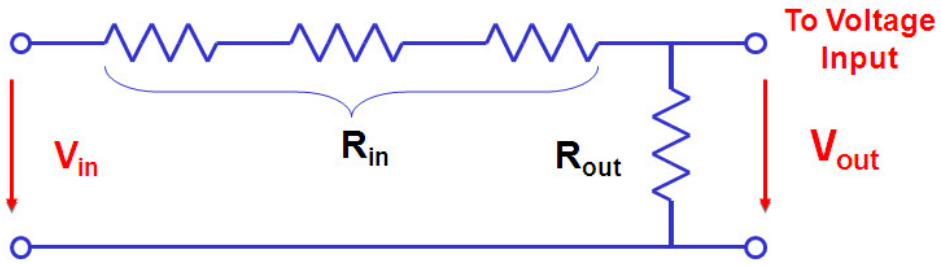


Figure 8: Resistive Voltage Divider

$$V_{out} = R * I_{in}$$

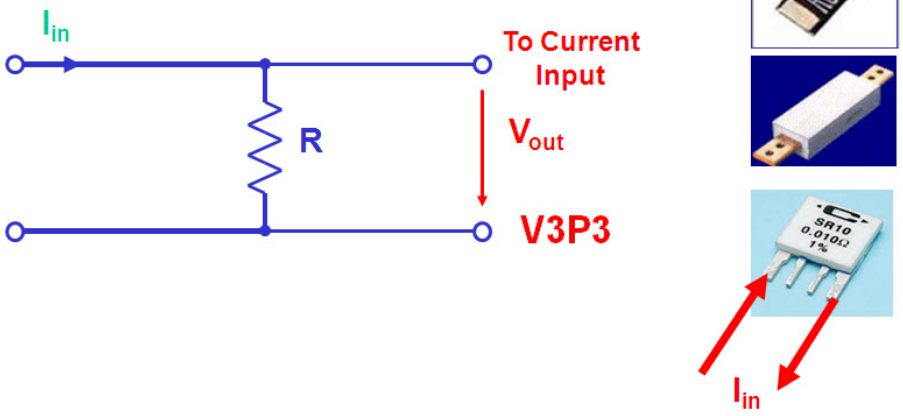


Figure 9: Resistive Current Shunt

$$V_{out} = R * I_{out} = R * I_{in}/N$$

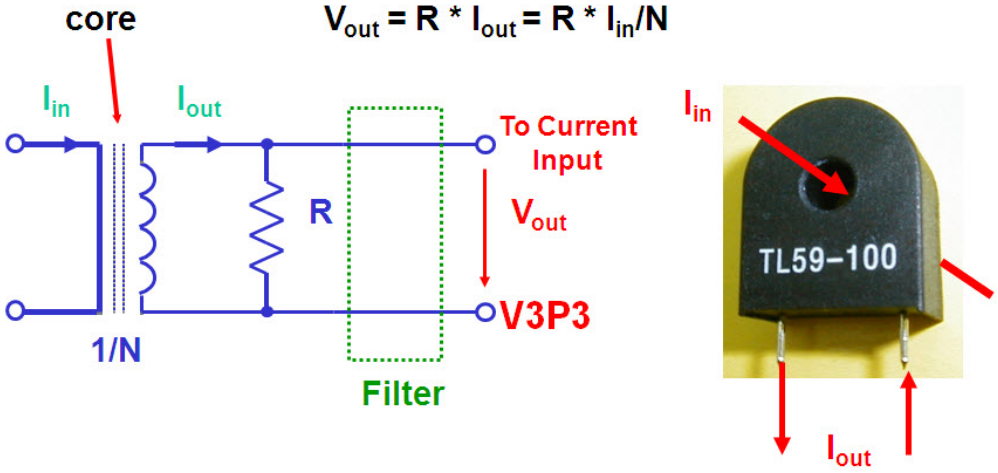


Figure 10: Current Transformer

3.2 Connecting 5 V Devices

All digital input pins of the 78M6612 are compatible with external 5 V devices. I/O pins configured as inputs do not require current-limiting resistors when they are connected to external 5 V devices.

3.3 Temperature Measurement

Measurement of absolute temperature uses the on-chip temperature sensor and applying the following formula:

$$T = \frac{(N(T) - N_n)}{S_n} + T_n$$

In the above formula, T is the temperature in °C, *N(T)* is the ADC count at temperature T, N_n is the ADC count at 25°C, S_n is the sensitivity in LSB/°C and T_n is +25 °C.

3.4 Temperature Compensation

Temperature Coefficients: The internal voltage reference is calibrated during device manufacture.

The temperature coefficients TC1 and TC2 are given as constants that represent typical component behavior (in μV/°C and μV/°C^2, respectively).

Since TC1 and TC2 are given in μV/°C and μV/°C^2, respectively, the value of the VREF voltage (1.195V) has to be taken into account when transitioning to PPM/°C and PPM/°C^2. This means that PPMC = 26.84*TC1/1.195, and PPMC2 = 1374*TC2/1.195).

Temperature Compensation: The CE provides the bandgap temperature to the MPU, which then may digitally compensate the power outputs for the temperature dependence of VREF.

The MPU, not the CE, is entirely in charge of providing temperature compensation. The MPU applies the following formula to determine *GAIN_ADJ* (address 0x12). In this formula *TEMP_X* is the deviation from nominal or calibration temperature expressed in multiples of 0.1°C:

$$GAIN\_ADJ = 16385 + \frac{TEMP\_X \cdot PPMC}{2^{14}} + \frac{TEMP\_X^2 \cdot PPMC2}{2^{23}}$$

In a power and energy measurement unit, the 78M6612 is not the only component contributing to temperature dependency. A whole range of components (e.g. current transformers, resistor dividers, power sources, filter capacitors) will contribute temperature effects. Since the output of the on-chip temperature sensor is accessible to the MPU, temperature-compensation mechanisms with great flexibility are possible (e.g. system-wide temperature correction over the entire unit rather than local to the chip).

3.5 Connecting LCDs

The 78M6612 has an on-chip LCD controller capable of controlling static or multiplexed LCDs. Figure 11 shows the basic connection for an LCD.

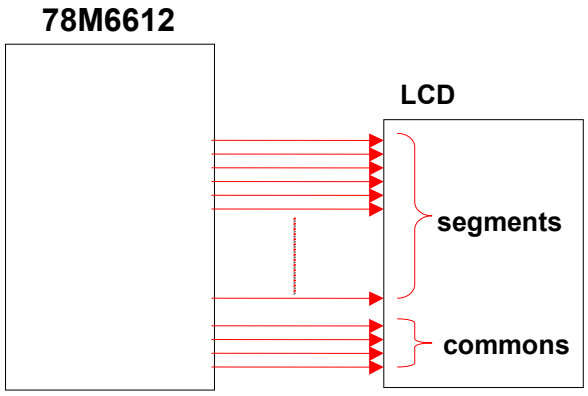


Figure 11: Connecting LCDs

The LCD segment pins can be organized in the following groups:

- Seventeen pins are dedicated LCD segment pins (SEG0 to SEG13, SEG16 to SEG18).
- Four pins are dual-function pins CKTEST/SEG19, E_RXTX/SEG38, E_TCLK/SEG33, and E_RST/SEG32.
- Fourteen pins are available as combined DIO and segment pins SEG24/DIO4 to SEG31/DIO11, SEG34/DIO14 to SEG37/DIO17, SEG39/DIO19, and SEG40/DIO20.
- The QFN-68 package adds an additional combination pin, SEG41/DIO21. Also adds two additional LCD segment pins, SEG13 and SEG14.

3.6 Connecting I²C EEPROMs

I²C EEPROMs or other I²C compatible devices should be connected to the DIO pins DIO4 and DIO5, as shown in Figure 12.

Pull-up resistors of roughly 10 kΩ to V3P3D should be used for both SCL and SDA signals. The *DIO_EEX* register in I/O RAM must be set to 01 in order to convert the DIO pins DIO4 and DIO5 to I²C pins SCL and SDA.

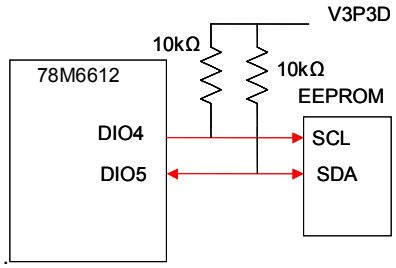


Figure 12: I²C EEPROM Connection

3.7 Connecting Three-Wire EEPROMs

µWire EEPROMs and other compatible devices should be connected to the DIO pins DIO4 and DIO5, as shown in Figure 13 and described below:

- DIO5 connects to both the DI and DO pins of the three-wire device.
- The CS pin must be connected to a vacant DIO pin of the 78M6618.
- In order to prevent bus contention, a 10 kΩ to resistor is used to separate the DI and DO signals.
- The CS and CLK pins should be pulled down with resistors to prevent operation of the three-wire device on power-up, before the 78M6618 can establish a stable signal for CS and CLK.
- The *DIO_EEX* register in I/O RAM must be set to 2 (b10) in order to convert the DIO pins DIO4 and DIO5 to µWire pins.

CAUTION The µ-Wire EEPROM interface is only functional when *MPU_DIV[2:0]* = 000.

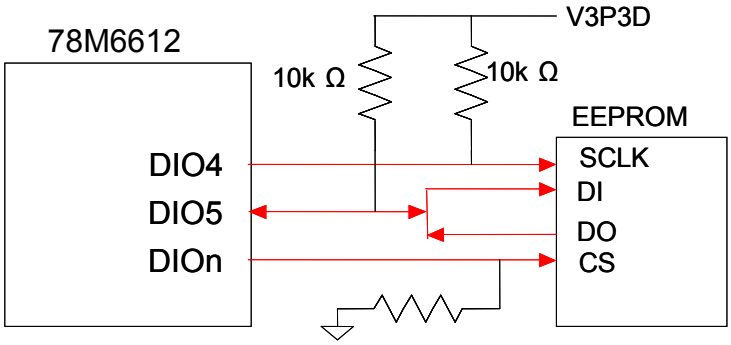


Figure 13: Three-Wire EEPROM Connection

3.8 UART0 (TX0/RX0)

The UART0 RX0 pin should be pulled down by a 10 kΩ resistor and additionally protected by a 100 pF ceramic capacitor, as shown in Figure 14.

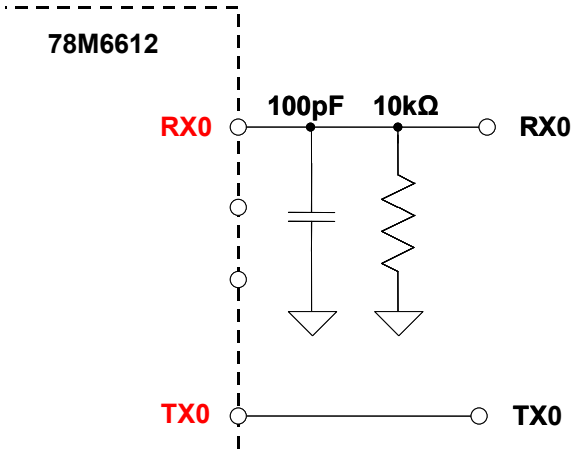


Figure 14: Connections for the RX0 Pin

3.9 UART1 (TX1/RX1)

The TX1 and RX1 pins can be used for a regular serial interface (by connecting a RS-232 transceiver for example), or they can be used to directly operate optical components (for example, an infrared diode and phototransistor implementing a FLAG interface).

3.10 Connecting V1 and Reset Pins

A voltage divider should be used to establish that V1 is in a safe range (see Figure 15). V1 must be lower than 2.9 V in all cases in order to keep the hardware watchdog timer enabled. A series 5 kΩ resistor (R3) and a capacitor to ground (C1) are added for enhanced EMC immunity. The parallel impedance of R1 and R2 should be approximately 8 kΩ to 10 kΩ in order to provide hysteresis for the power fault monitor.

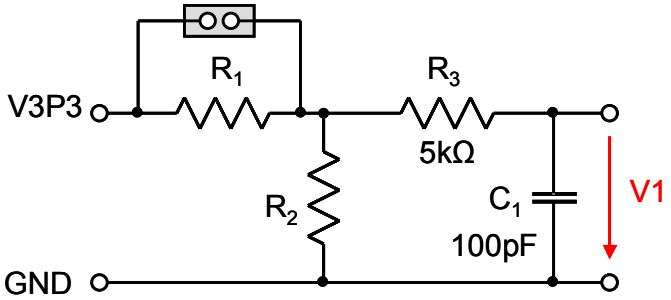


Figure 15: Voltage Divider for V1

Even though a functional power and measurement unit will not necessarily need a reset switch, it is useful to have a reset pushbutton switch for prototyping, as shown in Figure 16, left side. The RESET signal may be sourced from V3P3SYS, or VBAT (if a battery is present), or from a combination of these sources, depending on the application.

For production, the RESET pin should be protected by the external components shown in Figure 16, right side. R_1 should be in the range of 100 Ω and mounted as closely as possible to the IC. The RESET pin can also be directly connected to ground.

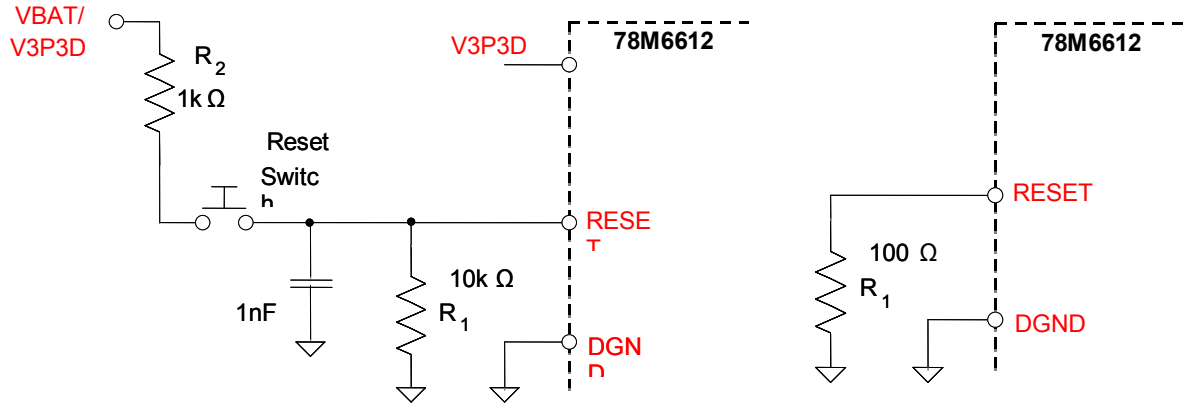


Figure 16: External Components for RESET: Development Circuit (Left), Production Circuit (Right)

3.11 Connecting the Emulator Port Pins

Even when the emulator is not used, small shunt capacitors to ground (22 pF) should be used for protection from EMI as illustrated in Figure 17. Production boards should have the ICE_E pin connected to ground.

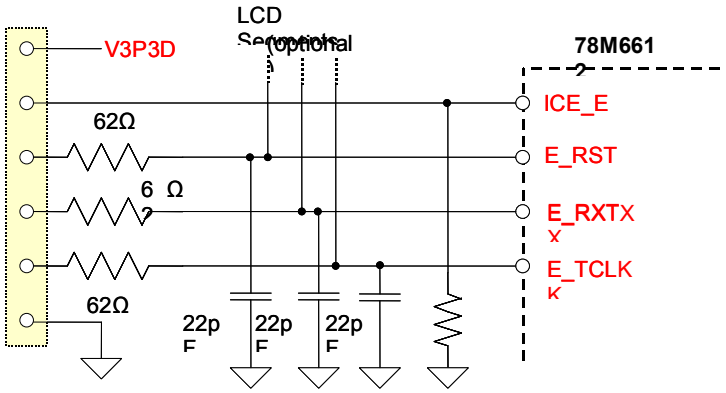


Figure 17: External Components for the Emulator Interface

3.12 Flash Programming

Operational or test code can be programmed into the Flash memory using either an in-circuit emulator or the Flash Programmer Module (TFP2) available from Maxim. The Flash programming procedure uses the E_RST, E_RXTX, and E_TCLK pins.

3.13 MPU Firmware Library

Any applications-specific MPU functions mentioned above are available from Maxim as a standard ANSI C library and as ANSI "C" source code. Sample application code using the measurement library is pre-programmed in Evaluation Kits for the 78M6618 IC and can be pre-programmed into engineering IC samples for system evaluation. Application code allows for quick and efficient evaluation of the IC without having to write firmware or having to purchase an in-circuit emulator (ICE). A Software Licensing Agreement (SLA) can be signed to receive either the source Flash HEX file for use in a production environment or source code and SDK documentation for modification.

3.14 Crystal Oscillator

The oscillator drives a standard 32.768 kHz watch crystal. The oscillator has been designed specifically to handle these crystals and is compatible with their high impedance and limited power handling capability. Good layouts will have XIN and XOUT shielded from each other.

Since the oscillator is self-biasing, an external resistor must not be connected across the crystal.

3.15 Measurement Calibration

Once the 78M6612 energy measurement device has been installed in a measurement system, it is typically calibrated. A complete calibration includes the following:

- Calibration of the metrology section, i.e. calibration for tolerances of the current sensors, voltage dividers and signal conditioning components as well as of the internal reference voltage (VREF).
- Establishment of the reference temperature (Section 3.3) for temperature measurement and temperature compensation (Section 3.4).

The metrology section can be calibrated using the gain and phase adjustment factors accessible to the CE. The gain adjustment is used to compensate for tolerances of components used for signal conditioning, especially the resistive components. Phase adjustment is provided to compensate for phase shifts introduced by certain types of current sensors or by the effects of reactive power supplies.

Due to the flexibility of the MPU firmware, any calibration method, such as calibration based on energy, or current and voltage can be implemented. It is also possible to implement segment-wise calibration (depending on current range).

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Table 5 shows the absolute maximum ranges for the device. Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under recommended operating conditions (Section 4.3) is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

Table 5: Absolute Maximum Ratings

Supplies and Ground Pins	
V3P3SYS, V3P3A	-0.5 V to 4.6 V
VBAT	-0.5 V to 4.6 V
GNDD	-0.5 V to +0.5 V
Analog Output Pins	
V3P3D	-10 mA to 10 mA, -0.5 V to 4.6 V
VREF	-10 mA to +10 mA, -0.5 V to V3P3A+0.5 V
V2P5	-10 mA to +10 mA, -0.5 V to 3.0 V
Analog Input Pins	
IA, VA, IB, VB, V1	-10 mA to +10 mA -0.5 V to V3P3A+0.5 V
XIN, XOUT	-10 mA to +10 mA -0.5 V to 3.0 V
All Other Pins	
Configured as SEG or COM drivers	-1 mA to +1 mA, -0.5 to V3P3D+0.5
Configured as Digital Inputs	-10 mA to +10 mA, -0.5 to 6 V
Configured as Digital Outputs	-15 mA to +15 mA, -0.5 V to V3P3D+0.5 V
All other pins	-0.5 V to V3P3D+0.5 V
Temperature and ESD Stress	
Operating junction temperature (peak, 100 ms)	140 °C
Operating junction temperature (continuous)	125 °C
Storage temperature	-45 °C to +165 °C
Solder temperature – 10 second duration	250 °C
ESD stress on all pins	4 kV

Stresses beyond Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltages are with respect to GNDA.

4.2 Recommended External Components

Table 6: Recommended External Components

Name	From	To	Function	Value	Unit
C1	V3P3A	AGND	Bypass capacitor for 3.3V supply.	≥0.1±20%	µF
C2	V3P3D	DGND	Bypass capacitor for 3.3V output.	0.1±20%	µF
CSYS	V3P3SYS	DGND	Bypass capacitor for V3P3SYS.	≥1.0±30%	µF
C2P5	V2P5	DGND	Bypass capacitor for V2P5.	0.1±20%	µF
XTAL	XIN	XOUT	32.768 kHz crystal – electrically similar to ECS .327-12.5-17X or Vishay XT26T, load capacitance 12.5 pF.	32.768	kHz
CXS †	XIN	AGND	Load capacitor for crystal (exact value depends on crystal specifications and parasitic capacitance of board).	27±10%	pF
CXL †	XOUT	AGND		27±10%	pF

† Depending on trace capacitance, higher or lower values for CXS and CXL must be used. Capacitance from XIN to GNDD and XOUT to GNDD (combining pin, trace and crystal capacitance) should be 35 pF to 37 pF.

4.3 Recommended Operating Conditions

Table 7: Recommended Operation Conditions

Parameter	Condition	Min	Typ	Max	Unit
V3P3SYS, V3P3A: 3.3V Supply Voltage V3P3A and V3P3SYS must be at the same voltage	Normal Operation	3.0	3.3	3.6	V
	Battery Backup	0		3.6	V
VBAT	No Battery	Externally Connect to V3P3SYS			
	Battery Backup BRN and LCD modes SLEEP mode	 3.0 2.0		 3.8 3.8	 V V
Operating Temperature		-40		+85	ºC

4.4 Performance Specifications

4.4.1 Input Logic Levels

Table 8: Input Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level input voltage†, V_{IH}		2			V
Digital low-level input voltage†, V_{IL}				0.8	V
Input pull-up current, I_{IL} E_RXTX, E_RST, CKTEST Other digital inputs	VIN=0V, ICE_E=1	 10 10 -1	 0	 100 100 1	 µA µA µA
Input pull down current, I_{IH} ICE_E Other digital inputs	VIN=V3P3D	 10 -1	 0	 100 1	 µA µA

†In battery powered modes, digital inputs should be below 0.3 V or above 2.5 V to minimize battery current.

4.4.2 Output Logic Levels

Table 9: Output Logic Levels

Parameter	Condition	Min	Typ	Max	Unit
Digital high-level output voltage V_{OH}	I_{LOAD} = 1 mA	V3P3D-0.4			V
	I_{LOAD} = 15 mA	V3P3D-0.6			V
Digital low-level output voltage V_{OL}	I_{LOAD} = 1 mA	0		0.4	V
	I_{LOAD} = 15 mA			0.8	V
TX1 V_{OH} (V3P3D-TX1)	I_{SOURCE}=1 mA			0.4	V
TX1 V_{OL}	I_{SINK}=20 mA			0.7	V

4.4.3 Power-Fault Comparator

Table 10: Power-Fault Comparator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Offset Voltage: V1-VBIAS		-20		+15	mV
Hysteresis Current: V1	Vin = VBIAS – 100 mV	0.8		1.2	µA
Response Time: V1	±100 mV overdrive	2	5	10	µs
WDT Disable Threshold (V1-V3P3A)		-400		-10	mV

4.4.4 Battery Monitor

Table 11: Power-Fault Comparator Performance Specifications (*BME=1)*

Parameter	Condition	Min	Typ	Max	Unit
Load Resistor		27	45	63	kΩ
LSB Value - does not include the 9-bit left shift at CE input.	*FIR_LEN*=0 *FIR_LEN*=1	-6.0 -2.6	-5.4 -2.3	-4.9 -2.0	µV µV
Offset Error		-200	-72	+100	mV

4.4.5 Supply Current

Table 12: Supply Current Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
V3P3A + V3P3SYS current	Normal Operation, V3P3A=V3P3SYS=3.3V *MPU_DIV[1:0]*=3 (614 kHz) *CKOUT_E[1:0]*=00, *CE_EN*=1, *RTM_E*=0, *ECK_DIS*=1, *ADC_E*=1, ICE_E=0		6.1	7.7	mA
VBAT current		-300		+300	nA
V3P3A + V3P3SYS current vs. MPU clock frequency	Same conditions as above		0.5		mA/ MHz
V3P3A + V3P3SYS current, Write Flash	Normal Operation as above, except write Flash at maximum rate, *CE_E*=0, *ADC_E*=0		9.1	10	mA
VBAT current †	VBAT=3.6V BROWNOUT mode, <25°C BROWNOUT mode, <>5°C LCD Mode, 25 °C LCD mode, over temperature SLEEP Mode, 25 °C Sleep mode, over temperature		 48 65 5.7 2.9 	 120 150 8.5 15 5.0 10	 µA µA µA µA µA µA

†Current into V3P3A and V3P3SYS pins is not zero if voltage is applied at these pins in brownout, LCD or sleep modes.

4.4.6 V3P3D Switch

Table 13: V3P3D Switch Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
On resistance – V3P3SYS to V3P3D	$\lvert I_{V3P3D} \rvert \le 1$ mA			10	Ω
On resistance – VBAT to V3P3D	$\lvert I_{V3P3D} \rvert \le 1$ mA			40	Ω

4.4.7 2.5V Voltage Regulator

Unless otherwise specified, load = 5 mA.

Table 14: 2.5 V Voltage Regulator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Voltage overhead V3P3-V2P5	Reduce V3P3 until V2P5 drops 200 mV			440	mV
PSSR ΔV2P5/ΔV3P3	RESET=0, iload=0	-3		+3	mV/V

4.4.8 Low Power Voltage Regulator

Unless otherwise specified, V3P3SYS=V3P3A=0.

Table 15: Low-Power Voltage Regulator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
V2P5	I_{LOAD}=0	2.0	2.5	2.7	V
V2P5 load regulation	I_{LOAD}=0 mA to 1 mA			30	mV
VBAT voltage requirement	I_{LOAD}=1 mA, Reduce VBAT until REG_LP_OK=0			3.0	V
PSRR ΔV2P5/ΔVBAT	I_{LOAD}=0	-50		50	mV/V

4.4.9 Crystal Oscillator

Table 16: Crystal Oscillator Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Maximum Output Power to Crystal	Crystal connected			1	μW
XIN to XOUT Capacitance				3	pF
Capacitance to DGND XIN XOUT				 5 5	 pF pF

4.4.10 VREF, VBIAS

Unless otherwise specified, $VREF\_DIS$=0.

Table 17: VREF, VBIAS Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
VREF output voltage, VNOM(25)	Ta = 22ºC	1.193	1.195	1.197	V
VREF chop step				50	mV
VREF output impedance	$VREF\_CAL$ =1, I_{LOAD} = 10 µA, -10 µA			2.5	kΩ
VNOM definition[1]	$VNOM(T) = VREF(22) + (T-22)TC1 + (T-22)^2 TC2$				V
VREF temperature coefficients TC1 TC2			+7.0 -0.341		 µV/ºC µV/°C^2
VREF aging			±25		ppm/ year
VREF(T) deviation from VNOM(T) $\frac{VREF(T)-VNOM(T)}{VNOM}\frac{10^6}{62}$	Ta = -40ºC to +85ºC	-40		+40	ppm/º C
VBIAS voltage	Ta = 25 ºC Ta = -40 ºC to 85 ºC	(-1%) (-4%)	1.6 1.6	(+1%) (+4%)	V V

[1] This relationship describes the nominal behavior of VREF at different temperatures.

4.4.11 LCD Drivers

The information in Table 18 applies to all COM and SEG pins.

Table 18: LCD Drivers Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
VLC2 Max Voltage	With respect to VLCD	-0.1		0+.1	V
VLC1 Voltage, ⅓ bias ½ bias	 With respect to 2*VLC2/3 With respect to VLC2/2	 -4 -3		 0 +2	 % %
VLC0 Voltage, ⅓ bias ½ bias	 With respect to VLC2/3 With respect to VLC2/2	 -3 -3		 +2 +2	 % %

VLCD is V3P3SYS in MISSION mode and VBAT in BROWNOUT and LCD modes.

4.4.12 ADC Converter, V3P3A Referenced

FIR_LEN=0, *VREF_DIS*=0, LSB values do not include the 9-bit left shift at CE input.

Table 19: ADC Converter Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Recommended Input Range (Vin-**V3P3A**)		-250		250	mV peak
Voltage to Current Crosstalk: $\frac{10^6 * Vcrosstalk}{Vin}\cos(\angle Vin - \angle Vcrosstalk)$	*Vin* = 200 mV peak, 65 Hz, on VA *Vcrosstalk* = largest measurement on IA or IB	-10		10	µV/V
THD (First 10 harmonics) 250 mV-pk 20 mV-pk	Vin=65 Hz, 64 kpts FFT, Blackman-Harris window			 -75 -90	 dB dB
Input Impedance	Vin=65 Hz	40		90	kΩ
Temperature coefficient of Input Impedance	Vin=65 Hz		1.7		Ω/°C
LSB size	*FIR_LEN*=0 *FIR_LEN*=1		357 151		nV/LSB
Digital Full Scale	*FIR_LEN*=0 *FIR_LEN*=1		±884736 ±2097152		LSB
ADC Gain Error vs %Power Supply Variation $\frac{10^6 \Delta Nout_{PK}\, 357nV/V_{IN}}{100 \Delta V3P3A/3.3}$	Vin=200 mV pk, 65 Hz V3P3A=3.0V, 3.6V			50	ppm/%
Input Offset (Vin-V3P3A)		-10		10	mV

4.4.13 UART1 Interface

Table 20: UART1 Interface Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
TX1 V_{OH} (V3P3D-TX1)	I_{SOURCE}=1 mA			0.4	V
TX1 V_{OL}	I_{SINK}=20 mA			0.7	V

4.4.14 Temperature Sensor

Table 21: Temperature Sensor Performance Specifications

Parameter	Condition	Min	Typ	Max	Unit
Nominal Sensitivity (S_n) †	T_A=25ºC, T_A=75ºC, *FIR_LEN* = 1 Nominal relationship: $N(T)= S_n*(T-T_n)+N_n$		-2180		LSB/ºC
Nominal (N_n) ††			1.0		10^6 LSB
Temperature Error† $ERR = T - \left(\frac{(N(T) - N_n)}{S_n} + T_n\right)$	T_A = -40ºC to +85ºC Tn = 25°C	-10		+10	ºC

† LSB values do not include the 9-bit left shift at CE input.
†† N_n is measured at T_n during calibration and is stored in MPU or CE for use in temperature calculations.

4.5 Timing Specifications

4.5.1 RAM and Flash Memory

Table 22: RAM and Flash Memory Specifications

Parameter	Condition	Min	Typ	Max	Unit
CE DRAM wait states	CKMPU = 4.9152 MHz	5			Cycles
	CKMPU = 1.25 MHz	2			Cycles
	CKMPU = 614 kHz	1			Cycles
Flash Read Pulse Width	V3P3A=V3P3SYS=0 BROWNOUT MODE	30		100	ns
Flash write cycles	-40 °C to +85 °C	20,000			Cycles
Flash data retention	25 °C	100			Years
Flash data retention	85 °C	10			Years
Flash byte writes between page or mass erase operations				2	Cycles

4.5.2 Flash Memory Timing

Table 23: Flash Memory Timing Specifications

Parameter	Condition	Min	Typ	Max	Unit
Write Time per Byte				42	µs
Page Erase (512 bytes)				20	ms
Mass Erase				200	ms

4.5.3 EEPROM Interface

Table 24: EEPROM Interface Timing

Parameter	Condition	Min	Typ	Max	Unit
Write Clock frequency (I^2C)	CKMPU=4.9152 MHz, Using interrupts		78		kHz
	CKMPU=4.9152 MHz, “bit-banging” DIO4/5		150		kHz
Write Clock frequency (3-wire)	CKMPU=4.9152 MHz		500		kHz

4.5.4 RESET and V1

Table 25: RESET and V1 Timing

Parameter	Condition	Min	Typ	Max	Unit
Reset pulse fall time				1	µs
Reset pulse width		5			µs
V1 Response Time	±100 mv overdrive	10	37	100	µs

4.5.5 RTC

Table 26: RTC Range

Parameter	Condition	Min	Typ	Max	Unit
Range for date		2000		2255	year

5 Packaging

5.1 64-Pin LQFP Package

5.1.1 Pinout

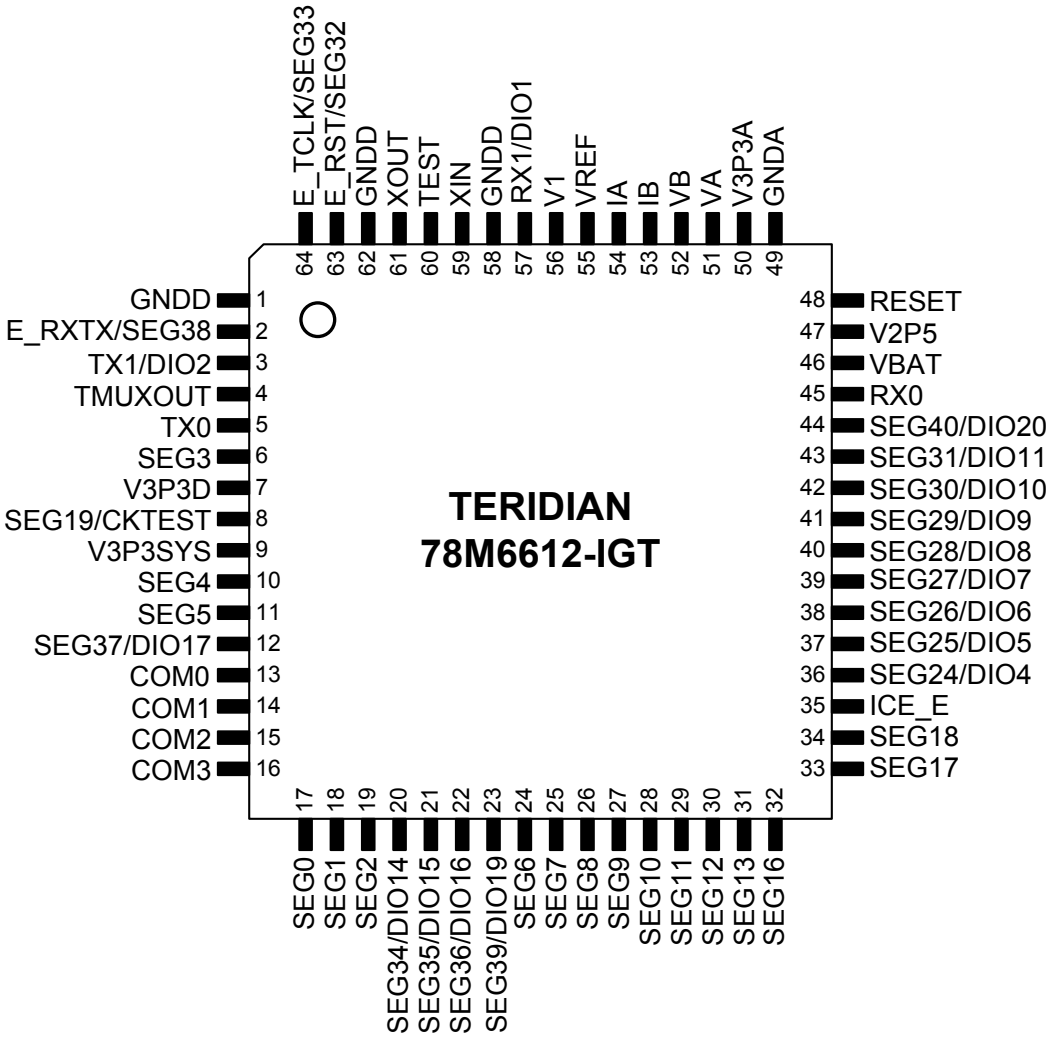
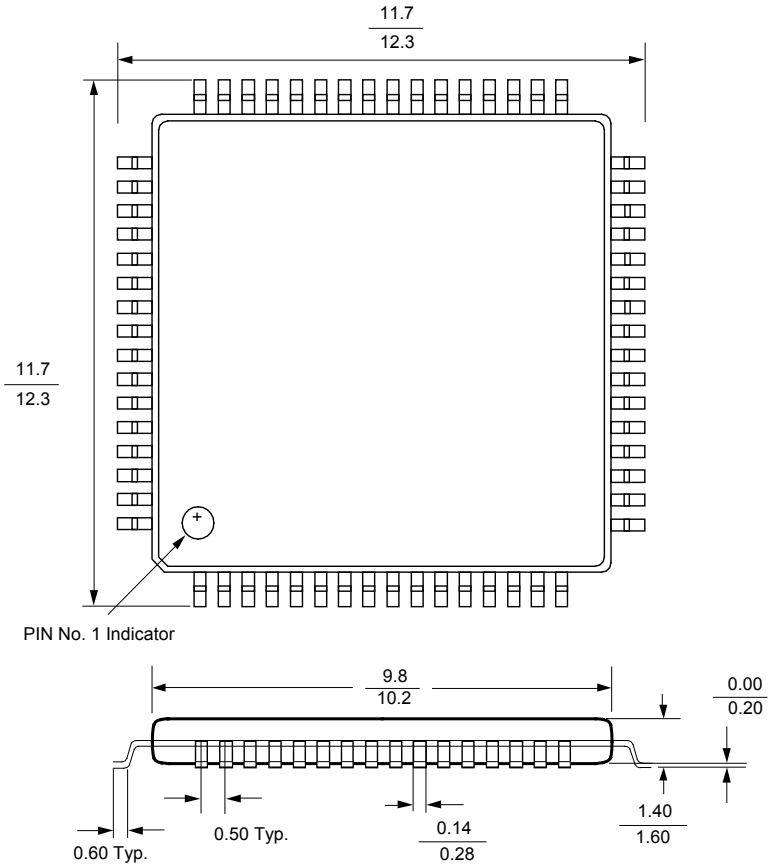


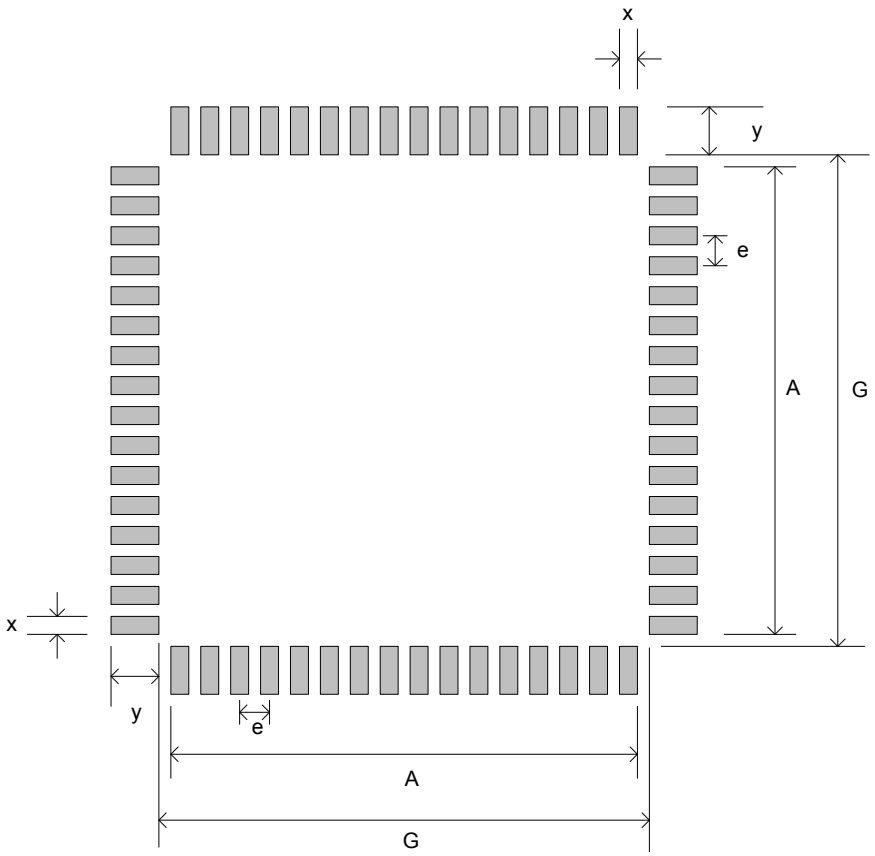
Figure 18: 64-Pin LQFP Pinout

5.1.2 Package Outline (LQFP 64)



NOTE: Controlling dimensions are in mm.

5.1.3 Recommended PCB Land Pattern for the LQFP-64 Package



Recommended PCB Land Pattern Dimensions

Symbol	Description	Typical Dimension
e	Lead pitch	0.5 mm
x	Pad width	0.25 mm
y	Pad length. See Note.	2.0 mm
A		7.75 mm
G		9.0 mm

Note: The y dimension has been elongated to allow for hand soldering and reworking. Production assembly may allow this dimension to be reduced as long as the G dimension is maintained.

5.2 68-Pin QFN Package

5.2.1 Pinout

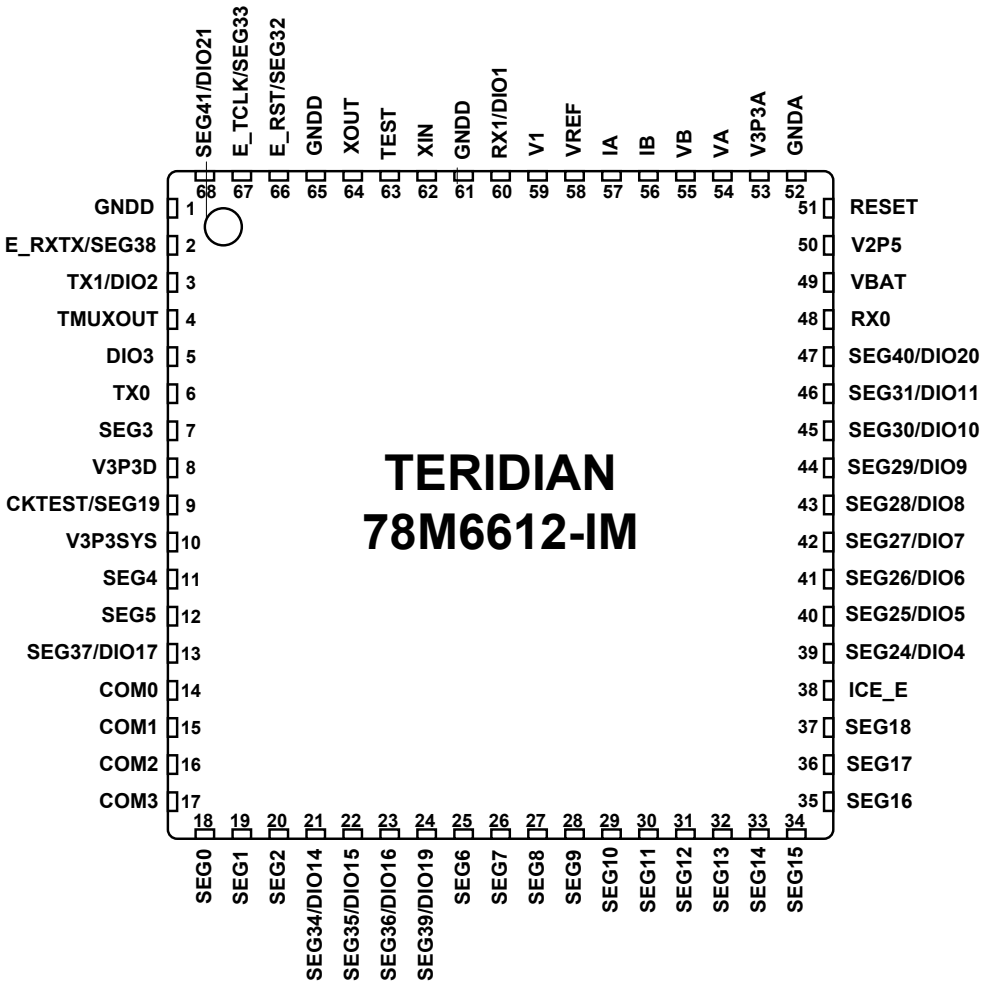
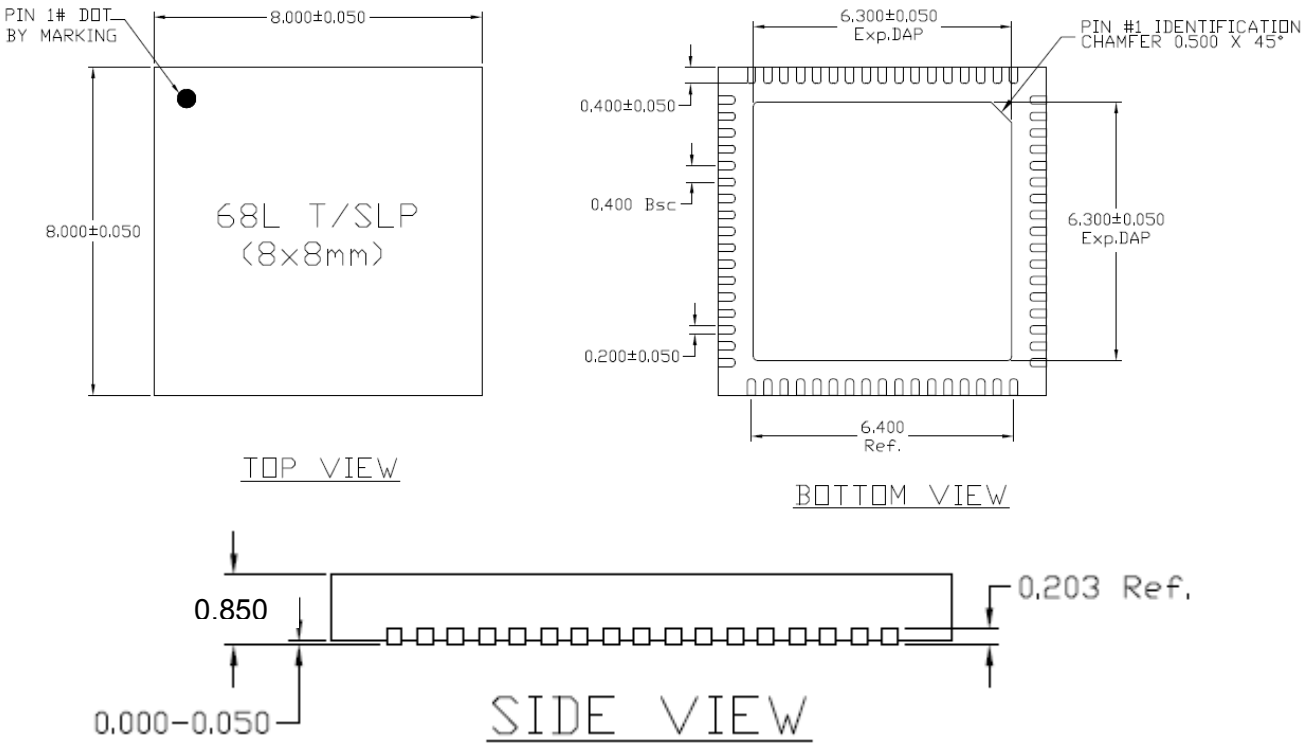


Figure 19: 68-Pin QFN Pinout

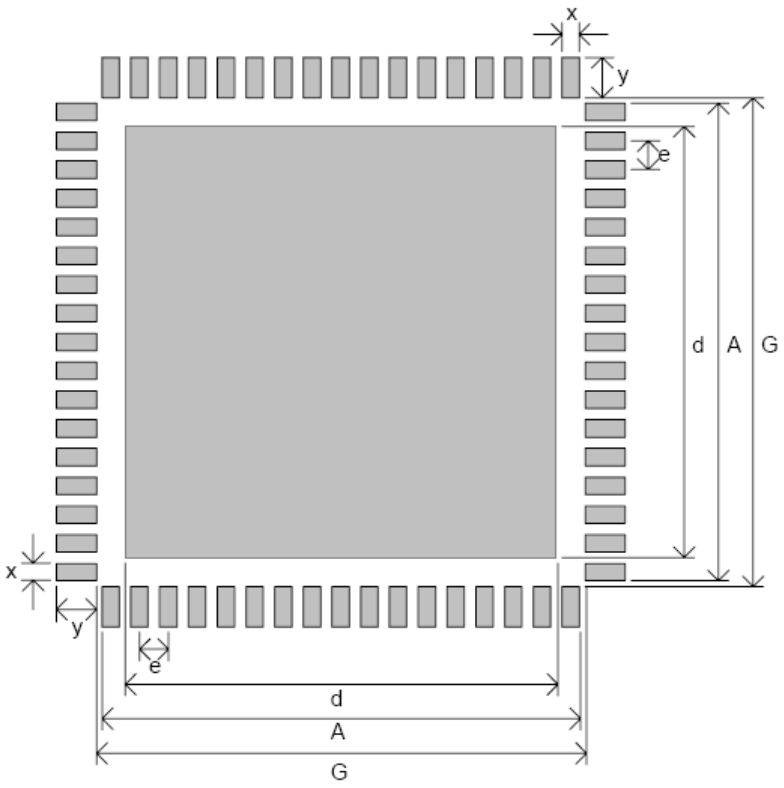
5.2.2 Package Outline



Dimensions (in mm):

*) Pin length is nominally 0.4 mm (min. 0.3 mm, max 0.4 mm).
**) Exposed pad is internally connected to GNDD.

5.2.3 Recommended PCB Land Pattern for the QFN-68 Package



Recommended PCB Land Pattern Dimensions

Symbol	Description	Typical Dimension
e	Lead pitch	0.4 mm
x	Pad width	0.23 mm
y	Pad length. See Note 3.	0.8 mm
d	See Note 1.	6.3 mm
A		6.63 mm
G		7.2 mm

Note 1: Do not place unmasked vias in region denoted by dimension d.

Note 2: Soldering of bottom internal pad is not required for proper operation.

Note 3: The y dimension has been elongated to allow for hand soldering and reworking. Production assembly may allow this dimension to be reduced as long as the G dimension is maintained.

6 Pin Descriptions

6.1 Power/Ground Pins

Table 27: Power/Ground Pins

Name	Type	Circuit	Description
GNDA	P	–	Analog ground: This pin should be connected directly to the ground plane.
GNDD	P	–	Digital ground: This pin should be connected directly to the ground plane.
V3P3A	P	–	Analog power supply: A 3.3V power supply should be connected to this pin, must be the same voltage as V3P3SYS.
V3P3SYS	P	–	System 3.3 V supply. This pin should be connected to a 3.3 V power supply.
V3P3D	O	13	Auxiliary voltage output of the chip, controlled by the internal 3.3 V selection switch. In mission mode, this pin is internally connected to V3P3SYS. In BROWNOUT mode, it is internally connected to VBAT. This pin is floating in LCD and sleep mode.
VBAT	P	12	Battery backup power supply. A battery or super-capacitor is to be connected between VBAT and GNDD. If no battery is used, connect VBAT to V3P3SYS.
V2P5	O	10	Output of the internal 2.5 V regulator. A 0.1 μF capacitor to GNDA should be connected to this pin.

6.2 Analog Pins

Table 28: Analog Pins

Name	Type	Circuit	Description
IA, IB	I	6	Line Current Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of current sensors. **Unused pins must be connected to V3P3A.**
VA, VB	I	6	Line Voltage Sense Inputs: These pins are voltage inputs to the internal A/D converter. Typically, they are connected to the outputs of resistor dividers. **Unused pins must be connected to V3P3A or tied to the voltage sense input that is in use.**
V1	I	7	Comparator Input: This pin is a voltage input to the internal power-fail comparator. The input voltage is compared to the internal BIAS voltage (1.6 V). If the input voltage is above VBIAS, the comparator output will be high (1). If the comparator output is lower, a voltage fault will occur and the chip will be forced to battery mode.
VREF	O	9	Voltage Reference for the ADC. This pin is normally disabled by setting the *VREF_CAL* bit in the I/O RAM and can then be left unconnected. If enabled, a 0.1 μF capacitor to GNDA should be connected.
XIN XOUT	I	8	Crystal Inputs: A 32 kHz crystal should be connected across these pins. Typically, a 27 pF capacitor is also connected from each pin to GNDA. It is important to minimize the capacitance between these pins. See the crystal manufacturer datasheet for details.

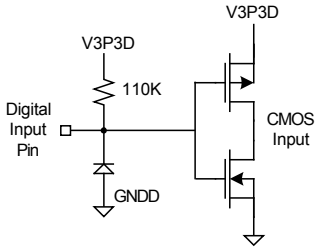
Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified in Section 7 I/O Equivalent Circuits.

6.3 Digital Pins

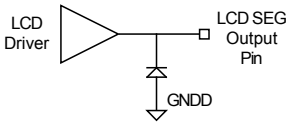
Name	Type	Circuit	Description
COM3, COM2, COM1, COM0	O	5	LCD common outputs: These four pins provide the select signals for the LCD display.
SEG0…SEG18	O	5	Dedicated LCD segment output pins. **SEG 14 and SEG15 are only available on the 68-pin package.**
SEG24/DIO4… SEG31/DIO11	I/O	3, 4, 5	Multi-use pins, configurable as either LCD SEG driver or DIO. (DIO4 = SCK, DIO5 = SDA when configured as EEPROM interface, WPULSE = DIO6, VARPULSE = DIO7 when configured as pulse outputs). **If unused, these pins must be configured as DIOs and set to outputs by the firmware.**
SEG34/DIO14 … SEG37/DIO17, SEG39/DIO19, SEG40/DIO20	I/O	3, 4, 5	Multi-use pins, configurable as either LCD SEG driver or DIO. **If unused, these pins must be configured as DIOs and set to outputs by the firmware.**
SEG41/DIO21	I/O	3, 4, 5	Multi-use pins, configurable as LCD driver or DIO (QFN 68 package only). **If unused, this pin must be configured as a DIO and set to an output by the firmware.**
E_RXTX/SEG38 E_RST/SEG32	I/O	1, 4, 5	Multi-use pins, configurable as either emulator port pins (when ICE_E pulled high) or LCD SEG drivers (when ICE_E tied to GND).
E_TCLK/SEG33	O	4, 5	
ICE_E	I	2	ICE enable. When zero, E_RST, E_TCLK, and E_RXTX become SEG32, SEG33, and SEG38 respectively. For production units, this pin should be pulled to GND to disable the emulator port. This pin should be brought out to the programming interface in order to create a way for reprogramming parts that have the *SECURE* bit set.
CKTEST/SEG19	O	4, 5	Multi-use pin, configurable as either Clock PLL output or LCD segment driver. Can be enabled and disabled by *CKOUT_E[1:0]*.
TMUXOUT	O	4	Digital output test multiplexer. Controlled by *TMUX[4:0]*.
RX1/DIO1	I/O	3, 4, 7	Multi-use pin, configurable as UART1 Input or general DIO. When configured as RX1, this pin can optionally receive a signal from an external photo-detector used in an IR serial interface. **If unused, this pin must be terminated to V3P3D or GNDD, or configured as a DIO and set to an output by the firmware.**
TX1/DIO2	I/O	3, 4	Multi-use pin, configurable as a transmit output from UART1 (or optionally an Optical LED Transmit Output), WPULSE, RPULSE, or general DIO. When configured as TX1, this pin is capable of directly driving an LED for transmitting data in an IR serial interface. **If unused, this pin must be left open, or configured as a DIO and set to an output by the firmware.**
DIO3	I/O	3, 4	DIO pin **(QFN 68 package only)**
RESET	I	3	This input pin resets the chip into a known state. For normal operation, this pin is connected to GNDD. To reset the chip, this pin should be pulled high. No external reset circuitry is necessary. Direct connect to ground in normal operation.
RX0	I	3	UART input. **If unused, this pin must be terminated to V3P3D or GNDD.**
TX0	O	4	UART output.
TEST	I	7	Enables Production Test. **Must be grounded in normal operation.**

Pin types: P = Power, O = Output, I = Input, I/O = Input/Output
The circuit number denotes the equivalent circuit, as specified on the following page.

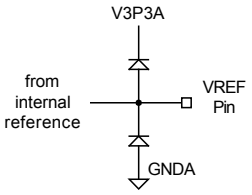
7 I/O Equivalent Circuits



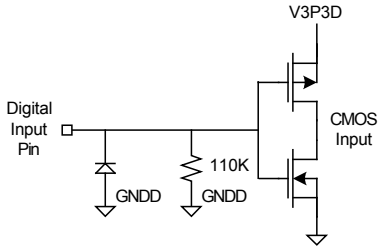
Digital Input Equivalent Circuit
Type 1:
Standard Digital Input or
pin configured as DIO Input
with Internal Pull-Up



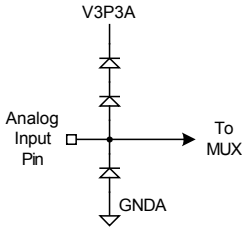
LCD Output Equivalent Circuit
Type 5:
LCD SEG or
pin configured as LCD SEG



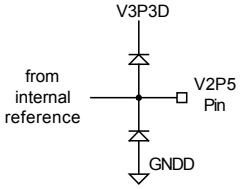
VREF Equivalent Circuit
Type 9:
VREF



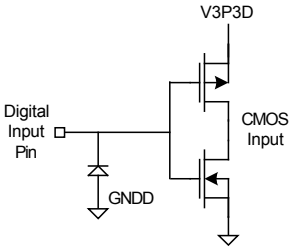
Digital Input
Type 2:
Pin configured as DIO Input
with Internal Pull-Down



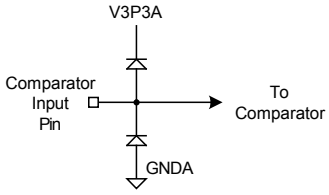
Analog Input Equivalent Circuit
Type 6:
ADC Input



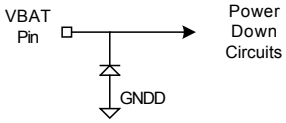
V2P5 Equivalent Circuit
Type 10:
V2P5



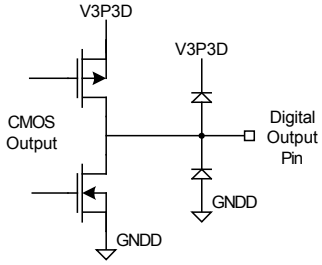
Digital Input Type 3:
Standard Digital Input or
pin configured as DIO Input



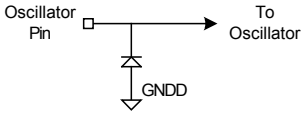
Comparator Input Equivalent
Circuit Type 7:
Comparator Input



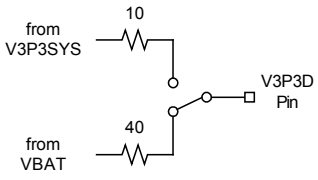
VBAT Equivalent Circuit
Type 12:
VBAT Power



Digital Output Equivalent Circuit
Type 4:
Standard Digital Output or
pin configured as DIO Output



Oscillator Equivalent Circuit
Type 8:
Oscillator I/O



V3P3D Equivalent Circuit
Type 13:
V3P3D

8 Ordering Information

Part	Part Description (Package, accuracy)	Flash Memory Size	Packaging	Ordering Number	Package Marking
78M6612	64-pin LQFP, 0.5% (Lead(Pb)-free)	32KB	Bulk	78M6612-IGT/F	78M6612-IGT
78M6612	64-pin LQFP, 0.5% (Lead(Pb)-free)	32KB	Tape & Reel	78M6612-IGTR/F	78M6612-IGT
78M6612	64-pin LQFP, 0.5% (Lead(Pb)-free)	32KB	*Programmed, Bulk	78M6612-IGT/F/P	78M6612-IGT
78M6612	64-pin LQFP, 0.5% (Lead(Pb)-free)	32KB	*Programmed, Tape & Reel	78M6612-IGTR/F/P	78M6612-IGT
78M6612	68-pin QFN, 0.5% (Lead(Pb)-free)	32KB	Bulk	78M6612-IM/F	78M6612-IM
78M6612	68-pin QFN, 0.5% (Lead(Pb)-free)	32KB	Tape & Reel	78M6612-IMR/F	78M6612-IM
78M6612	68-pin QFN, 0.5% (Lead(Pb)-free)	32KB	*Programmed, Bulk	78M6612-IM/F/P	78M6612-IM
78M6612	68-pin QFN, 0.5% (Lead(Pb)-free)	32KB	*Programmed, Tape & Reel	78M6612-IMR/F/P	78M6612-IM

*Contact the factory for more information on programmed part options.

9 Contact Information

For more information about Maxim products or to check the availability of the 78M6613, contact technical support at **www.maxim-ic.com/support**.

Revision History

REVISION	DATE	DESCRIPTION
1.0	4/1/2009	First publication.
1.3	5/7/2010	Moved firmware specific information to respective developers manuals. Added Caution to Section 1.4.6: "Caution. If UART1 is being used for full duplex operation, TX interrupts may be inadvertently cleared and thus a TX safety timer is recommended." Added Caution to Section 1.4.6 about UART0 interrupts. In Section 3.10, changed "I/O RAM register *TX1DIS*" to "I/O RAM register *TX1E*". In Figure 18, corrected the name of pin 45 from "RX" to "RX0".
2	1/12	Added Maxim logo.

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