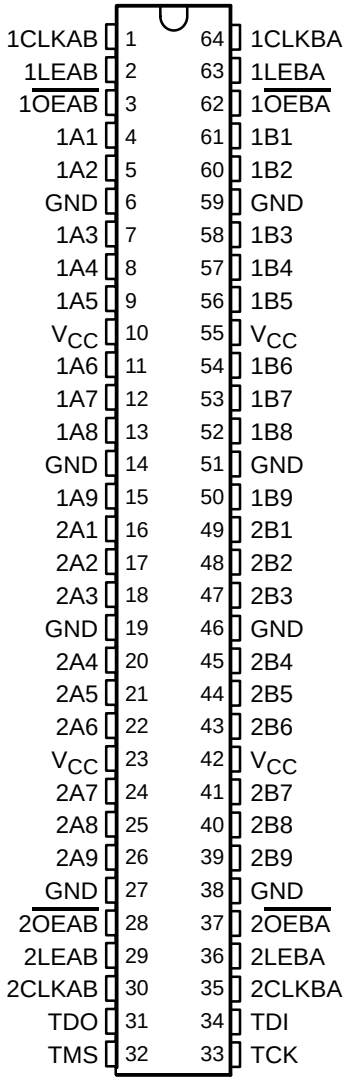
# THE DATASHEET OF

# 74LVTH18511DGGRG4

- **Member of the Texas Instruments Widebus™ Family**
- **UBT™ Transceiver Combines D-Type Latches and D-Type Flip-Flops for Operation in Transparent, Latched, or Clocked Mode**
- **State-of-the-Art 3.3-V ABT Design Supports Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V $V_{CC}$)**
- **Supports Unregulated Battery Operation Down to 2.7 V**
- **Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors**
- **Compatible With the IEEE Std 1149.1-1990 (JTAG) Test Access Port and Boundary Scan Architecture**
- **IEEE Std 1149.1-1990 Required Instructions and Optional CLAMP, HIGHZ, IDCODE**

**DGG PACKAGE**
**(TOP VIEW)**




## description/ordering information

The SN74LVTH18511 is an 18-bit universal bus transceiver with boundary scan. This device supports IEEE Std 1149.1-1990 boundary scan to facilitate testing of complex circuit-board assemblies. Scan access to the test circuitry is accomplished via the 4-wire test access port (TAP) interface.

Additionally, this device is designed specifically for low-voltage (3.3-V) $V_{CC}$ operation, but with the capability to provide a TTL interface to a 5-V system environment.

In the normal mode, this device is an 18-bit UBT that combines D-type latches and D-type flip-flops to allow data flow in transparent, latched, or clocked modes. It can be used either as two 9-bit transceivers or one 18-bit transceiver. Activating the TAP in the normal mode does not affect the functional operation of the UBT.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | TSSOP – DGG | Tape and reel | SN74LVTH18511DGGR | LVTH18511 |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## description /ordering information(continued)

Data flow in each direction is controlled by output-enable ($\overline{OEAB}$ and $\overline{OEBA}$), latch-enable (LEAB and LEBA), and clock (CLKAB and CLKBA) inputs. For A-to-B data flow, the devices operate in the transparent mode when LEAB is high. When LEAB is low, the A data is latched while CLKAB is held at a static low or high logic level. Otherwise, if LEAB is low, A data is stored on a low-to-high transition of CLKAB. When $\overline{OEAB}$ is low, the B outputs are active. When $\overline{OEAB}$ is high, the B outputs are in the high-impedance state. B-to-A data flow is similar to A-to-B data flow, but uses the $\overline{OEBA}$, LEBA, and CLKBA inputs.

In the test mode, the normal operation of the UBT is inhibited, and the test circuitry is enabled to observe and control the I/O boundary of the device. When enabled, the test circuitry performs boundary scan test operations according to the protocol described in IEEE Std 1149.1-1990.

Four dedicated test pins are used to observe and control the operation of the test circuitry: test data input (TDI), test data output (TDO), test mode select (TMS), and test clock (TCK). All testing and scan operations are synchronized to the TAP interface.

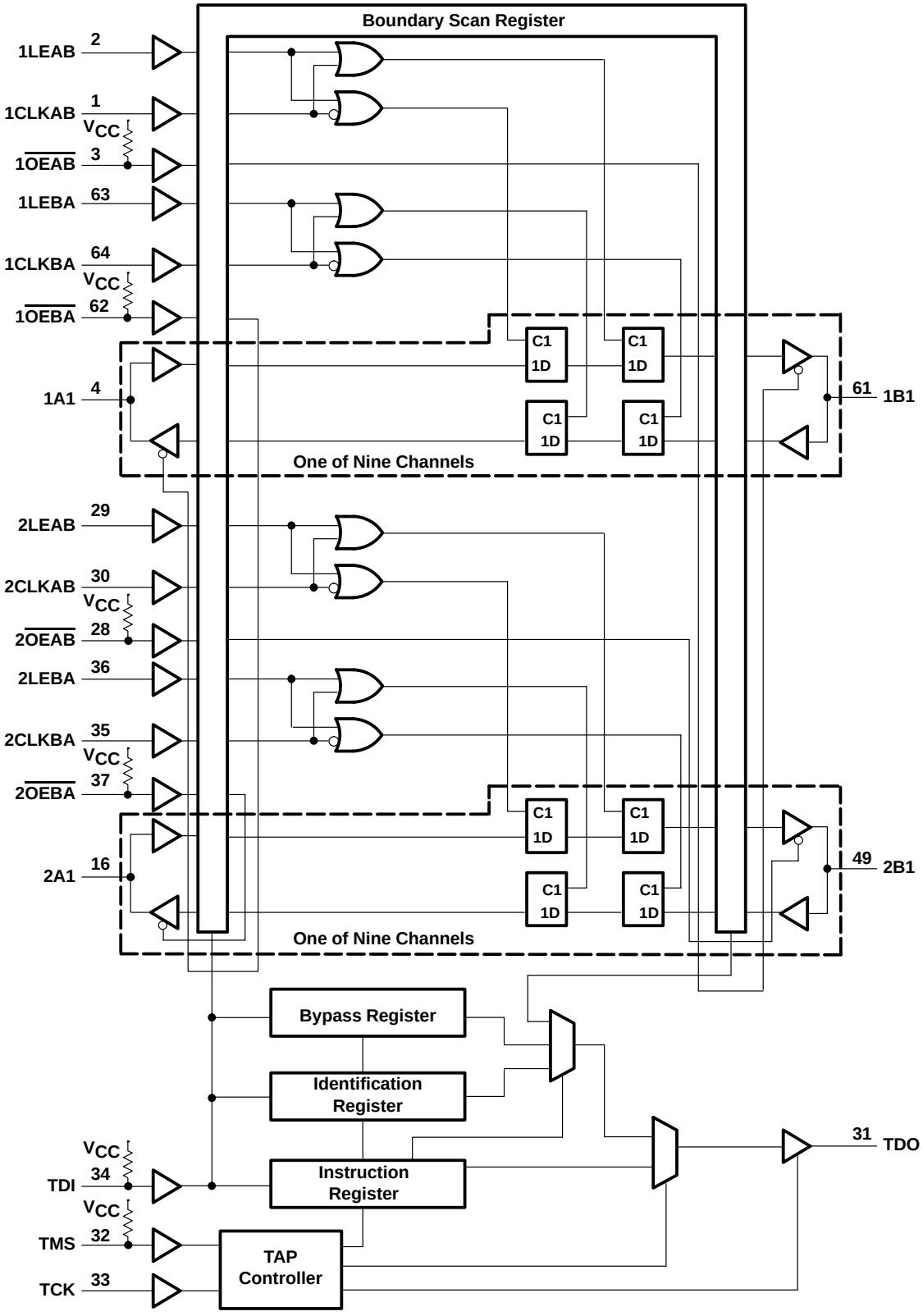
Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**FUNCTION TABLE†**
**(normal mode, each register)**

| INPUTS | | | | OUTPUT |
|---|---|---|---|---|
| $\overline{OEAB}$ | LEAB | CLKAB | A | B |
| L | L | L | X | $B_0$‡ |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | H | X | L | L |
| L | H | X | H | H |
| H | X | X | X | Z |

† A-to-B data flow is shown. B-to-A data flow is similar, but uses $\overline{OEBA}$, LEBA, and CLKBA.
‡ Output level before the indicated steady-state input conditions were established

## functional block diagram



## Terminal Functions

| TERMINAL NAME | DESCRIPTION |
|---|---|
| 1A1–1A9, 2A1–2A9 | Normal-function A-bus I/O ports. See function table for normal-mode logic. |
| 1B1–1B9, 2B1–2B9 | Normal-function B-bus I/O ports. See function table for normal-mode logic. |
| 1CLKAB, 1CLKBA, 2CLKAB, 2CLKBA | Normal-function clock inputs. See function table for normal-mode logic. |
| GND | Ground |
| 1LEAB, 1LEBA, 2LEAB, 2LEBA | Normal-function latch enables. See function table for normal-mode logic. |
| $1\overline{OEAB}$, $1\overline{OEBA}$, $2\overline{OEAB}$, $2\overline{OEBA}$ | Normal-function output enables. See function table for normal-mode logic. An internal pullup at each terminal forces the terminal to a high level if left unconnected. |
| TCK | Test clock. One of four terminals required by IEEE Std 1149.1-1990. Test operations of the device are synchronous to TCK. Data is captured on the rising edge of TCK, and outputs change on the falling edge of TCK. |
| TDI | Test data input. One of four terminals required by IEEE Std 1149.1-1990. TDI is the serial input for shifting data through the instruction register or selected data register. An internal pullup forces TDI to a high level if left unconnected. |
| TDO | Test data output. One of four terminals required by IEEE Std 1149.1-1990. TDO is the serial output for shifting data through the instruction register or selected data register. |
| TMS | Test mode select. One of four terminals required by IEEE Std 1149.1-1990. TMS directs the device through its TAP controller states. An internal pullup forces TMS to a high level if left unconnected. |
| $V_{CC}$ | Supply voltage |

## test architecture

Serial-test information is conveyed by means of a 4-wire test bus or TAP, that conforms to IEEE Std 1149.1-1990. Test instructions, test data, and test control signals all are passed along this serial-test bus. The TAP controller monitors two signals from the test bus, TCK and TMS. The TAP controller extracts the synchronization (TCK) and state control (TMS) signals from the test bus and generates the appropriate on-chip control signals for the test structures in the device. Figure 1 shows the TAP-controller state diagram.

The TAP controller is fully synchronous to the TCK signal. Input data is captured on the rising edge of TCK and output data changes on the falling edge of TCK. This scheme ensures that data to be captured is valid for fully one-half of the TCK cycle.

The functional block diagram shows the IEEE Std 1149.1-1990 4-wire test bus and boundary scan architecture and the relationship among the test bus, the TAP controller, and the test registers. As shown, the device contains an 8-bit instruction register and three test-data registers: a 48-bit boundary scan register, a 1-bit bypass register, and a 32-bit device identification register.

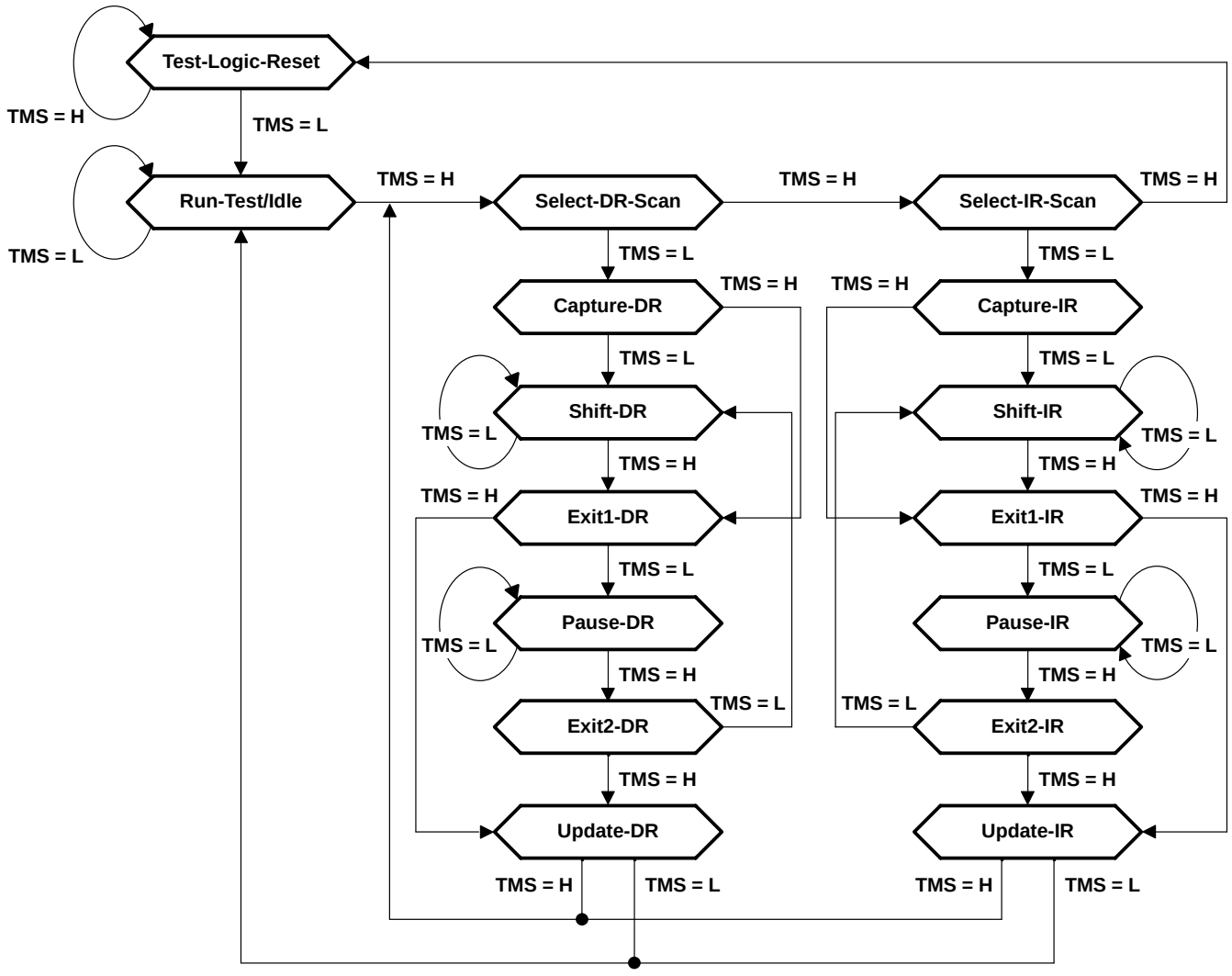



**Figure 1. TAP-Controller State Diagram**

## state diagram description

The TAP controller is a synchronous finite-state machine that provides test control signals throughout the device. The state diagram shown in Figure 1 is in accordance with IEEE Std 1149.1-1990. The TAP controller proceeds through its states, based on the level of TMS at the rising edge of TCK.

As shown, the TAP controller consists of 16 states. There are six stable states (indicated by a looping arrow in the state diagram) and ten unstable states. A stable state is a state the TAP controller can retain for consecutive TCK cycles. Any state that does not meet this criterion is an unstable state.

There are two main paths through the state diagram: one to access and control the selected data register and one to access and control the instruction register. Only one register can be accessed at a time.

### Test-Logic-Reset

The device powers up in the Test-Logic-Reset state. In the stable Test-Logic-Reset state, the test logic is reset and is disabled so that the normal logic function of the device is performed. The instruction register is reset to an opcode that selects the optional IDCODE instruction, if supported, or the BYPASS instruction. Certain data registers also can be reset to their power-up values.

The state machine is constructed such that the TAP controller returns to the Test-Logic-Reset state in no more than five TCK cycles if TMS is left high. The TMS pin has an internal pullup resistor that forces it high if left unconnected or if a board defect causes it to be open circuited.

For the SN74LVTH18511, the instruction register is reset to the binary value 10000001, which selects the IDCODE instruction. Bits 47–44 in the boundary scan register are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked the outputs would be at the high-impedance state). Reset value of other bits in the boundary scan register should be considered indeterminate.

### Run-Test/Idle

The TAP controller must pass through the Run-Test/Idle state (from Test-Logic-Reset) before executing any test operations. The Run-Test/Idle state also can be entered following data-register or instruction-register scans. Run-Test/Idle is a stable state in which the test logic actively can be running a test or can be idle. The test operations selected by the boundary-control register are performed while the TAP controller is in the Run-Test/Idle state.

### Select-DR-Scan, Select-IR-Scan

No specific function is performed in the Select-DR-Scan and Select-IR-Scan states, and the TAP controller exits either of these states on the next TCK cycle. These states allow the selection of either data-register scan or instruction-register scan.

### Capture-DR

When a data-register scan is selected, the TAP controller must pass through the Capture-DR state. In the Capture-DR state, the selected data register captures a data value as specified by the current instruction. Such capture operations occur on the rising edge of TCK, upon which the TAP controller exits the Capture-DR state.

### Shift-DR

Upon entry to the Shift-DR state, the data register is placed in the scan path between TDI and TDO, and on the first falling edge of TCK, TDO goes from the high-impedance state to an active state. TDO enables to the logic level present in the least-significant bit of the selected data register.

While in the stable Shift-DR state, data is shifted serially through the selected data register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-DR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-DR to Shift-DR or from Exit2-DR to Shift-DR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-DR state.

**Exit1-DR, Exit2-DR**

The Exit1-DR and Exit2-DR states are temporary states that end a data-register scan. It is possible to return to the Shift-DR state from either Exit1-DR or Exit2-DR without recapturing the data register. On the first falling edge of TCK after entry to Exit1-DR, TDO goes from the active state to the high-impedance state.

**Pause-DR**

No specific function is performed in the stable Pause-DR state, in which the TAP controller can remain indefinitely. The Pause-DR state suspends and resumes data-register scan operations without loss of data.

**Update-DR**

If the current instruction calls for the selected data register to be updated with current data, such update occurs on the falling edge of TCK, following entry to the Update-DR state.

**Capture-IR**

When an instruction-register scan is selected, the TAP controller must pass through the Capture-IR state. In the Capture-IR state, the instruction register captures its current status value. This capture operation occurs on the rising edge of TCK, upon which the TAP controller exits the Capture-IR state. For the SN74LVTH18511, the status value loaded in the Capture-IR state is the fixed binary value 10000001.

**Shift-IR**

Upon entry to the Shift-IR state, the instruction register is placed in the scan path between TDI and TDO. On the first falling edge of TCK, TDO goes from the high-impedance state to the active state. TDO enables to the logic level present in the least-significant bit of the instruction register.

While in the stable Shift-IR state, instruction data is shifted serially through the instruction register on each TCK cycle. The first shift occurs on the first rising edge of TCK after entry to the Shift-IR state (i.e., no shifting occurs during the TCK cycle in which the TAP controller changes from Capture-IR to Shift-IR or from Exit2-IR to Shift-IR). The last shift occurs on the rising edge of TCK, upon which the TAP controller exits the Shift-IR state.

**Exit1-IR, Exit2-IR**

The Exit1-IR and Exit2-IR states are temporary states that end an instruction-register scan. It is possible to return to the Shift-IR state from either Exit1-IR or Exit2-IR without recapturing the instruction register. On the first falling edge of TCK after entry to Exit1-IR, TDO goes from the active state to the high-impedance state.

**Pause-IR**

No specific function is performed in the stable Pause-IR state, in which the TAP controller can remain indefinitely. The Pause-IR state suspends and resumes instruction-register scan operations without loss of data.

**Update-IR**

The current instruction is updated and takes effect on the falling edge of TCK, following entry to the Update-IR state.

## register overview

With the exception of the bypass and device-identification registers, any test register can be thought of as a serial shift register with a shadow latch on each bit. The bypass and device-identification registers differ in that they contain only a shift register. During the appropriate capture state (Capture-IR for instruction register, Capture-DR for data registers), the shift register can be parallel loaded from a source specified by the current instruction. During the appropriate shift state (Shift-IR or Shift-DR), the contents of the shift register are shifted out from TDO while new contents are shifted in at TDI. During the appropriate update state (Update-IR or Update-DR), the shadow latches are updated from the shift register.

### instruction register description

The instruction register (IR) is eight bits long and tells the device what instruction is to be executed. Information contained in the instruction includes the mode of operation (either normal mode, in which the device performs its normal logic function, or test mode, in which the normal logic function is inhibited or altered), the test operation to be performed, which of the three data registers is to be selected for inclusion in the scan path during data-register scans, and the source of data to be captured into the selected data register during Capture-DR.

Table 3 lists the instructions supported by the SN74LVTH18511.

During Capture-IR, the IR captures the binary value 10000001. As an instruction is shifted in, this value is shifted out via TDO and can be inspected as verification that the IR is in the scan path. During Update-IR, the value that has been shifted into the IR is loaded into shadow latches. At this time, the current instruction is updated and any specified mode change takes effect. At power up or in the Test-Logic-Reset state, the IR is reset to the binary value 10000001, which selects the IDCODE instruction. The IR order of scan is shown in Figure 2.

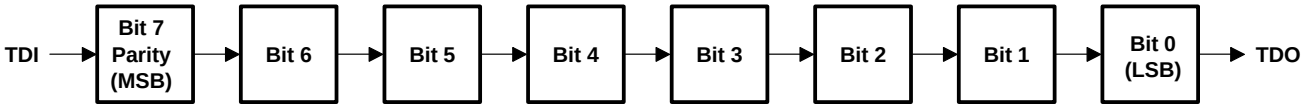



**Figure 2. Instruction Register Order of Scan**

## data register description

### boundary scan register

The boundary scan register (BSR) is 48 bits long. It contains one boundary scan cell (BSC) for each normal-function input pin and one BSC for each normal-function I/O pin (one single cell for both input data and output data). The BSR is used to store test data that is to be applied externally to the device output pins, and/or to capture data that appears internally at the outputs of the normal on-chip logic and/or externally at the device input pins.

The source of data to be captured into the BSR during Capture-DR is determined by the current instruction. The contents of the BSR can change during Run-Test/Idle, as determined by the current instruction. At power up or in Test-Logic-Reset, BSCs 47–44 are reset to logic 1, ensuring that these cells, which control A-port and B-port outputs, are set to benign values (i.e., if test mode were invoked, the outputs would be at the high-impedance state). Reset values of other BSCs should be considered indeterminate.

The BSR order of scan is from TDI through bits 47–0 to TDO. Table 1 shows the BSR bits and their associated device pin signals.

**Table 1. Boundary Scan Register Configuration**

| BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL | BSR BIT NUMBER | DEVICE SIGNAL |
|---|---|---|---|---|---|
| 47 | 2$\overline{\text{OEAB}}$ | 35 | 2A9-I/O | 17 | 2B9-I/O |
| 46 | 1$\overline{\text{OEAB}}$ | 34 | 2A8-I/O | 16 | 2B8-I/O |
| 45 | 2$\overline{\text{OEBA}}$ | 33 | 2A7-I/O | 15 | 2B7-I/O |
| 44 | 1$\overline{\text{OEBA}}$ | 32 | 2A6-I/O | 14 | 2B6-I/O |
| 43 | 2CLKAB | 31 | 2A5-I/O | 13 | 2B5-I/O |
| 42 | 1CLKAB | 30 | 2A4-I/O | 12 | 2B4-I/O |
| 41 | 2CLKBA | 29 | 2A3-I/O | 11 | 2B3-I/O |
| 40 | 1CLKBA | 28 | 2A2-I/O | 10 | 2B2-I/O |
| 39 | 2LEAB | 27 | 2A1-I/O | 9 | 2B1-I/O |
| 38 | 1LEAB | 26 | 1A9-I/O | 8 | 1B9-I/O |
| 37 | 2LEBA | 25 | 1A8-I/O | 7 | 1B8-I/O |
| 36 | 1LEBA | 24 | 1A7-I/O | 6 | 1B7-I/O |
| — | — | 23 | 1A6-I/O | 5 | 1B6-I/O |
| — | — | 22 | 1A5-I/O | 4 | 1B5-I/O |
| — | — | 21 | 1A4-I/O | 3 | 1B4-I/O |
| — | — | 20 | 1A3-I/O | 2 | 1B3-I/O |
| — | — | 19 | 1A2-I/O | 1 | 1B2-I/O |
| — | — | 18 | 1A1-I/O | 0 | 1B1-I/O |

### bypass register

The bypass register is a 1-bit scan path that can be selected to shorten the length of the system scan path, reducing the number of bits per test pattern that must be applied to complete a test operation. During Capture-DR, the bypass register captures a logic 0. The bypass register order of scan is shown in Figure 3.

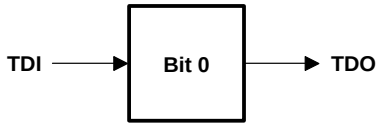



**Figure 3. Bypass Register Order of Scan**

### device-identification register

The device-identification register (IDR) is 32 bits long. It can be selected and read to identify the manufacturer, part number, and version of this device.

For the SN74LVTH18511, the binary value 00000000000010000010000000101111 (0008202F, hex) is captured (during Capture-DR state) in the IDR to identify this device as Texas Instruments SN74LVTH18511.

The IDR order of scan is from TDI through bits 31–0 to TDO. Table 2 shows the IDR bits and their significance.

**Table 2. Device-Identification Register Configuration**

| IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE | IDR BIT NUMBER | IDENTIFICATION SIGNIFICANCE |
|---|---|---|---|---|---|
| 31 | VERSION3 | 27 | PARTNUMBER15 | 11 | MANUFACTURER10† |
| 30 | VERSION2 | 26 | PARTNUMBER14 | 10 | MANUFACTURER09† |
| 29 | VERSION1 | 25 | PARTNUMBER13 | 9 | MANUFACTURER08† |
| 28 | VERSION0 | 24 | PARTNUMBER12 | 8 | MANUFACTURER07† |
| — | — | 23 | PARTNUMBER11 | 7 | MANUFACTURER06† |
| — | — | 22 | PARTNUMBER10 | 6 | MANUFACTURER05† |
| — | — | 21 | PARTNUMBER09 | 5 | MANUFACTURER04† |
| — | — | 20 | PARTNUMBER08 | 4 | MANUFACTURER03† |
| — | — | 19 | PARTNUMBER07 | 3 | MANUFACTURER02† |
| — | — | 18 | PARTNUMBER06 | 2 | MANUFACTURER01† |
| — | — | 17 | PARTNUMBER05 | 1 | MANUFACTURER00† |
| — | — | 16 | PARTNUMBER04 | 0 | LOGIC1† |
| — | — | 15 | PARTNUMBER03 | — | — |
| — | — | 14 | PARTNUMBER02 | — | — |
| — | — | 13 | PARTNUMBER01 | — | — |
| — | — | 12 | PARTNUMBER00 | — | — |

† Note that, for TI products, bits 11–0 of the device-identification register always contain the binary value 000000101111 (02F, hex).

## instruction-register opcode description

The instruction-register opcodes are shown in Table 3. The following descriptions detail the operation of each instruction.

**Table 3. Instruction-Register Opcodes**

| BINARY CODE† BIT 7 → BIT 0 MSB → LSB | BOUNDARY SCAN INSTRUCTION | DESCRIPTION | SELECTED DATA REGISTER | MODE |
|---|---|---|---|---|
| 00000000 | EXTEST | Boundary scan | Boundary scan | Test |
| 10000001 | IDCODE | Identification read | Device identification | Normal |
| 10000010 | SAMPLE/PRELOAD | Sample boundary | Boundary scan | Normal |
| 00000110 | HIGHZ | Control boundary to high impedance | Bypass | Modified test |
| 10000111 | CLAMP | Control boundary to 1/0 | Bypass | Test |
| 00001001 | PRIVATE | Internal TI use only | | |
| 00001010 | PRIVATE | Internal TI use only | | |
| 10001011 | PRIVATE | Internal TI use only | | |
| 00001100 | PRIVATE | Internal TI use only | | |
| 10001101 | PRIVATE | Internal TI use only | | |
| 10001110 | PRIVATE | Internal TI use only | | |
| 00001111 | PRIVATE | Internal TI use only | | |
| All others | BYPASS | Bypass scan | Bypass | Normal |

† Bit 7 is used to maintain even parity in the 8-bit instruction.

### boundary scan

This instruction conforms to the IEEE Std 1149.1-1990 EXTEST instruction. The BSR is selected in the scan path. Data appearing at the device input and I/O pins is captured in the associated BSCs. Data that has been scanned into the I/O BSCs for pins in the output mode is applied to the device I/O pins. Data present at the device pins, except for output enables, is passed through the BSCs to the normal on-chip logic. For I/O pins, the operation of a pin as input or output is determined by the contents of the output-enable BSCs (bits 47–44 of the BSR). When a given output enable is active (logic 0), the associated I/O pins operate in the output mode. Otherwise, the I/O pins operate in the input mode. The device operates in the test mode.

### identification read

This instruction conforms to the IEEE Std 1149.1-1990 IDCODE instruction. The IDR is selected in the scan path. The device operates in the normal mode.

### sample boundary

This instruction conforms to the IEEE Std 1149.1-1990 SAMPLE/PRELOAD instruction. The BSR is selected in the scan path. Data appearing at the device input pins and I/O pins in the input mode is captured in the associated BSCs, while data appearing at the outputs of the normal on-chip logic is captured in the BSCs associated with I/O pins in the output mode. The device operates in the normal mode.

### bypass scan

This instruction conforms to the IEEE Std 1149.1-1990 BYPASS instruction. The bypass register is selected in the scan path. A logic 0 value is captured in the bypass register during Capture-DR. The device operates in the normal mode.

**control boundary to high impedance**

This instruction conforms to the IEEE Std 1149.1a-1993 HIGHZ instruction. The bypass register is selected in the scan path. A logic-0 value is captured in the bypass register during Capture-DR. The device operates in a modified test mode in which all device I/O pins are placed in the high-impedance state, the device input pins remain operational, and the normal on-chip logic function is performed.

**control boundary to 1/0**

This instruction conforms to the IEEE Std 1149.1a-1993 CLAMP instruction. The bypass register is selected in the scan path. A logic-0 value is captured in the bypass register during Capture-DR. Data in the I/O BSCs for pins in the output mode is applied to the device I/O pins. The device operates in the test mode.

## timing description

All test operations of the SN74LVTH18511 are synchronous to the TCK signal. Data on the TDI, TMS, and normal-function inputs is captured on the rising edge of TCK. Data appears on the TDO and normal-function output pins on the falling edge of TCK. The TAP controller is advanced through its states (as shown in Figure 1) by changing the value of TMS on the falling edge of TCK and then applying a rising edge to TCK.

A simple timing example is shown in Figure 4. In this example, the TAP controller begins in the Test-Logic-Reset state and is advanced through its states, as necessary, to perform one instruction-register scan and one data-register scan. While in the Shift-IR and Shift-DR states, TDI is used to input serial data, and TDO is used to output serial data. The TAP controller then is returned to the Test-Logic-Reset state. Table 4 details the operation of the test circuitry during each TCK cycle.

**Table 4. Explanation of Timing Example**

| TCK CYCLE(S) | TAP STATE AFTER TCK | DESCRIPTION |
|---|---|---|
| 1 | Test-Logic-Reset | TMS is changed to a logic-0 value on the falling edge of TCK to begin advancing the TAP controller toward the desired state. |
| 2 | Run-Test/Idle | |
| 3 | Select-DR-Scan | |
| 4 | Select-IR-Scan | |
| 5 | Capture-IR | The IR captures the 8-bit binary value 10000001 on the rising edge of TCK as the TAP controller exits the Capture-IR state. |
| 6 | Shift-IR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 7–13 | Shift-IR | One bit is shifted into the IR on each TCK rising edge. With TDI held at a logic 1 value, the 8-bit binary value 11111111 is scanned serially into the IR. At the same time, the 8-bit binary value 10000001 is scanned serially out of the IR via TDO. In TCK cycle 13, TMS is changed to a logic 1 value to end the IR scan on the next TCK cycle. The last bit of the instruction is shifted as the TAP controller advances from Shift-IR to Exit1-IR. |
| 14 | Exit1-IR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 15 | Update-IR | The IR is updated with the new instruction (BYPASS) on the falling edge of TCK. |
| 16 | Select-DR-Scan | |
| 17 | Capture-DR | The bypass register captures a logic-0 value on the rising edge of TCK as the TAP controller exits the Capture-DR state. |
| 18 | Shift-DR | TDO becomes active and TDI is made valid on the falling edge of TCK. The first bit is shifted into the TAP on the rising edge of TCK as the TAP controller advances to the next state. |
| 19–20 | Shift-DR | The binary value 101 is shifted in via TDI, while the binary value 010 is shifted out via TDO. |
| 21 | Exit1-DR | TDO becomes inactive (goes to the high-impedance state) on the falling edge of TCK. |
| 22 | Update-DR | The selected data register is updated with the new data on the falling edge of TCK. |
| 23 | Select-DR-Scan | |
| 24 | Select-IR-Scan | |
| 25 | Test-Logic-Reset | Test operation completed |

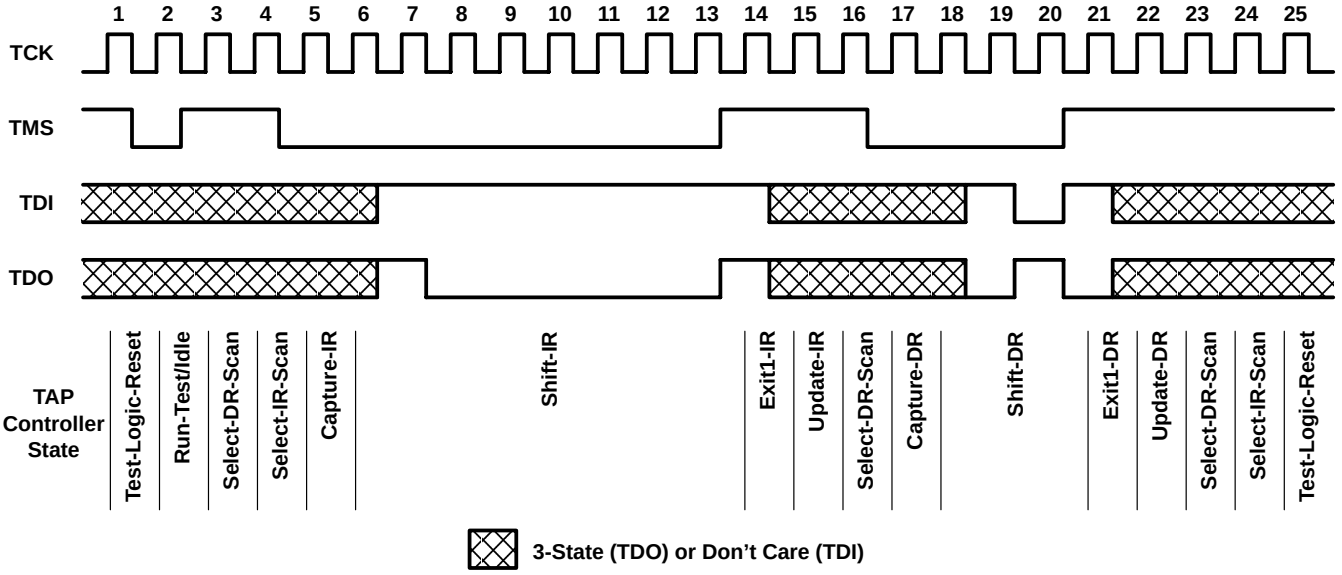



**Figure 4. Timing Example**

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Voltage range applied to any output in the high or power-off state, $V_O$ (see Note 1) . . . . . –0.5 V to 7 V
Current into any output in the low state, $I_O$ . . . . . 128 mA
Current into any output in the high state, $I_O$ (see Note 2) . . . . . 64 mA
Input clamp current, $I_{IK}$ ($V_I < 0$) . . . . . –50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$) . . . . . –50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3) . . . . . 55°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings can be exceeded if the input and output clamp-current ratings are observed.
2. This current flows only when the output is in the high state and $V_O > V_{CC}$.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 4)

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | 2.7 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_I$ | Input voltage | | | 5.5 | V |
| $I_{OH}$ | High-level output current | | | –32 | mA |
| $I_{OL}$ | Low-level output current | | | 32 | mA |
| $I_{OL}$‡ | Low-level output current | | | 64 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | Outputs enabled | | 10 | ns/V |
| $T_A$ | Operating free-air temperature | | –40 | 85 | °C |

‡ Current duty cycle ≤ 50%, f ≥ 1 kHz

NOTE 4: All unused control inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER | | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | | $V_{CC}$ = 2.7 V, | $I_I$ = –18 mA | | | –1.2 | V |
| $V_{OH}$ | | $V_{CC}$ = 2.7 V to 3.6 V, | $I_{OH}$ = –100 μA | $V_{CC}$–0.2 | | | V |
| | | $V_{CC}$ = 2.7 V, | $I_{OH}$ = –3 mA | 2.4 | | | |
| | | $V_{CC}$ = 3 V | $I_{OH}$ = –8 mA | 2.4 | | | |
| | | | $I_{OH}$ = –32 mA | 2 | | | |
| $V_{OL}$ | | $V_{CC}$ = 2.7 V | $I_{OL}$ = 100 μA | | | 0.2 | V |
| | | | $I_{OL}$ = 24 mA | | | 0.5 | |
| | | $V_{CC}$ = 3 V | $I_{OL}$ = 16 mA | | | 0.4 | |
| | | | $I_{OL}$ = 32 mA | | | 0.5 | |
| | | | $I_{OL}$ = 64 mA | | | 0.55 | |
| $I_I$ | CLK, LE, TCK | $V_{CC}$ = 3.6 V, | $V_I$ = $V_{CC}$ or GND | | | ±1 | μA |
| | | $V_{CC}$ = 0 or 3.6 V, | $V_I$ = 5.5 V | | | 10 | |
| | $\overline{OE}$, TDI, TMS | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 5 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | |
| | | | $V_I$ = 0 | –25 | | –100 | |
| | A or B ports‡ | $V_{CC}$ = 3.6 V | $V_I$ = 5.5 V | | | 20 | |
| | | | $V_I$ = $V_{CC}$ | | | 1 | |
| | | | $V_I$ = 0 | | | –5 | |
| $I_{off}$ | | $V_{CC}$ = 0, | $V_I$ or $V_O$ = 0 to 4.5 V | | | ±100 | μA |
| $I_{I(hold)}$§ | A or B ports | $V_{CC}$ = 3 V | $V_I$ = 0.8 V | 75 | 150 | 500 | μA |
| | | | $V_I$ = 2 V | –75 | –150 | –500 | |
| $I_{OZH}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 3 V | | | 1 | μA |
| $I_{OZL}$ | TDO | $V_{CC}$ = 3.6 V, | $V_O$ = 0.5 V | | | –1 | μA |
| $I_{OZPU}$ | TDO | $V_{CC}$ = 0 to 1.5 V, | $V_O$ = 0.5 V or 3 V | | | ±50 | μA |
| $I_{OZPD}$ | TDO | $V_{CC}$ = 1.5 V to 0, | $V_O$ = 0.5 V or 3 V | | | ±50 | μA |
| $I_{CC}$ | | $V_{CC}$ = 3.6 V, $I_O$ = 0, $V_I$ = $V_{CC}$ or GND | Outputs high | | 0.6 | 2 | mA |
| | | | Outputs low | | 18 | 24 | |
| | | | Outputs disabled | | 0.6 | 2 | |
| $\Delta I_{CC}$¶ | | $V_{CC}$ = 3 V to 3.6 V, One input at $V_{CC}$ – 0.6 V, Other inputs at $V_{CC}$ or GND | | | | 0.5 | mA |
| $C_i$ | | $V_I$ = 3 V or 0 | | | 4 | | pF |
| $C_{io}$ | | $V_O$ = 3 V or 0 | | | 10 | | pF |
| $C_o$ | | $V_O$ = 3 V or 0 | | | 8 | | pF |

† All typical values are at $V_{CC}$ = 3.3 V, $T_A$ = 25°C.
‡ Unused pins at $V_{CC}$ or GND
§ The parameter $I_{I(hold)}$ includes the off-state output leakage current.
¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than $V_{CC}$ or GND.

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 5)**

| | | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | CLKAB or CLKBA | | | 100 | | 80 | MHz |
| $t_w$ | Pulse duration | CLKAB or CLKBA high or low | | 4.4 | | 5.6 | | ns |
| | | LEAB or LEBA high | | 3 | | 3 | | |
| $t_{su}$ | Setup time | A before CLKAB↑ or B before CLKBA↑ | | 2.8 | | 3 | | ns |
| | | A before LEAB↓ or B before LEBA↓ | CLK high | 1.5 | | 0.7 | | |
| | | | CLK low | 1.6 | | 1.6 | | |
| $t_h$ | Hold time | A after CLKAB↑ or B after CLKBA↑ | | 1.4 | | 1.1 | | ns |
| | | A after LEAB↓ or B after LEBA↓ | | 3.1 | | 3.5 | | |

**timing requirements over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 5)**

| | | | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{clock}$ | Clock frequency | TCK | | 50 | | 40 | MHz |
| $t_w$ | Pulse duration | TCK high or low | 9.5 | | 10.5 | | ns |
| $t_{su}$ | Setup time | A, B, CLK, LE, or $\overline{OE}$ before TCK↑ | 6.5 | | 7 | | ns |
| | | TDI before TCK↑ | 2.5 | | 3.5 | | |
| | | TMS before TCK↑ | 2.5 | | 3.5 | | |
| $t_h$ | Hold time | A, B, CLK, LE, or $\overline{OE}$ after TCK↑ | 1.7 | | 1 | | ns |
| | | TDI after TCK↑ | 1.5 | | 1 | | |
| | | TMS after TCK↑ | 1.5 | | 1 | | |
| $t_d$ | Delay time | Power up to TCK↑ | 50 | | 50 | | ns |
| $t_r$ | Rise time | $V_{CC}$ power up | 1 | | 1 | | µs |

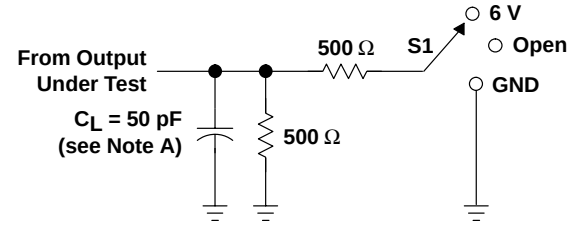
**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (normal mode) (see Figure 5)**

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | CLKAB or CLKBA | | 100 | | 80 | | MHz |
| $t_{PLH}$ | A or B | B or A | 1.5 | 4.9 | | 5.6 | ns |
| $t_{PHL}$ | | | 1.5 | 4.9 | | 5.6 | |
| $t_{PLH}$ | CLKAB or CLKBA | B or A | 1.5 | 5.8 | | 6.8 | ns |
| $t_{PHL}$ | | | 1.5 | 5.8 | | 6.8 | |
| $t_{PLH}$ | LEAB or LEBA | B or A | 1.5 | 7.4 | | 8.4 | ns |
| $t_{PHL}$ | | | 1.5 | 5.7 | | 6.4 | |
| $t_{PZH}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 1.5 | 7.1 | | 8.3 | ns |
| $t_{PZL}$ | | | 1.5 | 7.1 | | 8.3 | |
| $t_{PHZ}$ | $\overline{OEAB}$ or $\overline{OEBA}$ | B or A | 2.5 | 7.8 | | 8.4 | ns |
| $t_{PLZ}$ | | | 2.5 | 7.8 | | 8.4 | |

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (test mode) (see Figure 5)**

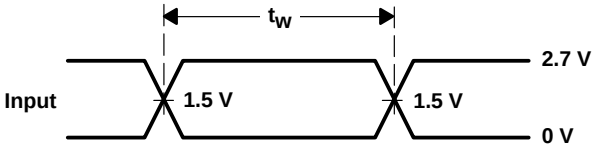
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | $V_{CC}$ = 3.3 V ± 0.3 V | | $V_{CC}$ = 2.7 V | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $f_{max}$ | TCK | | 50 | | 40 | | MHz |
| $t_{PLH}$ | TCK↓ | A or B | 2.5 | 14 | | 17 | ns |
| $t_{PHL}$ | | | 2.5 | 14 | | 17 | |
| $t_{PLH}$ | TCK↓ | TDO | 1 | 5.5 | | 6.5 | ns |
| $t_{PHL}$ | | | 1.5 | 6.5 | | 7.5 | |
| $t_{PZH}$ | TCK↓ | A or B | 4 | 17 | | 20 | ns |
| $t_{PZL}$ | | | 4 | 17 | | 20 | |
| $t_{PZH}$ | TCK↓ | TDO | 1 | 5.5 | | 6.5 | ns |
| $t_{PZL}$ | | | 1.5 | 5.5 | | 6.5 | |
| $t_{PHZ}$ | TCK↓ | A or B | 4 | 18 | | 20 | ns |
| $t_{PLZ}$ | | | 4 | 17 | | 18.5 | |
| $t_{PHZ}$ | TCK↓ | TDO | 1.5 | 7 | | 8.5 | ns |
| $t_{PLZ}$ | | | 1.5 | 7 | | 8 | |

## PARAMETER MEASUREMENT INFORMATION

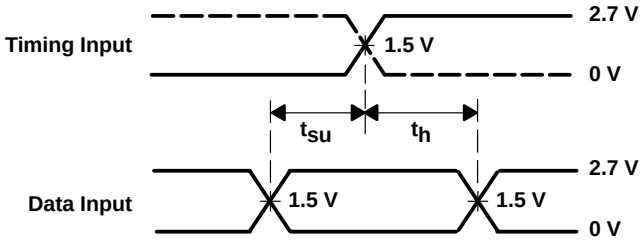



LOAD CIRCUIT

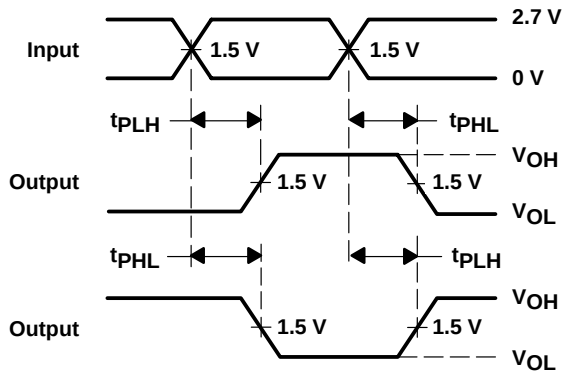
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 6 V |
| $t_{PHZ}/t_{PZH}$ | GND |



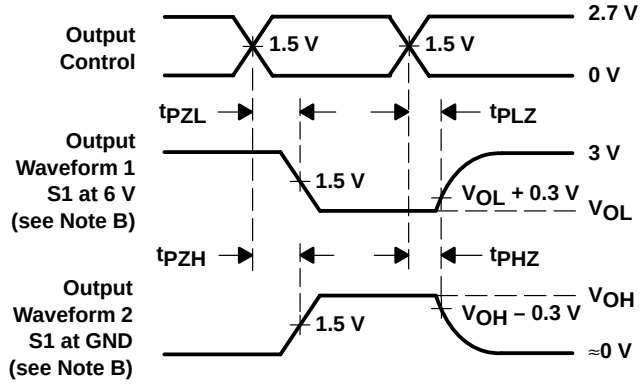

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



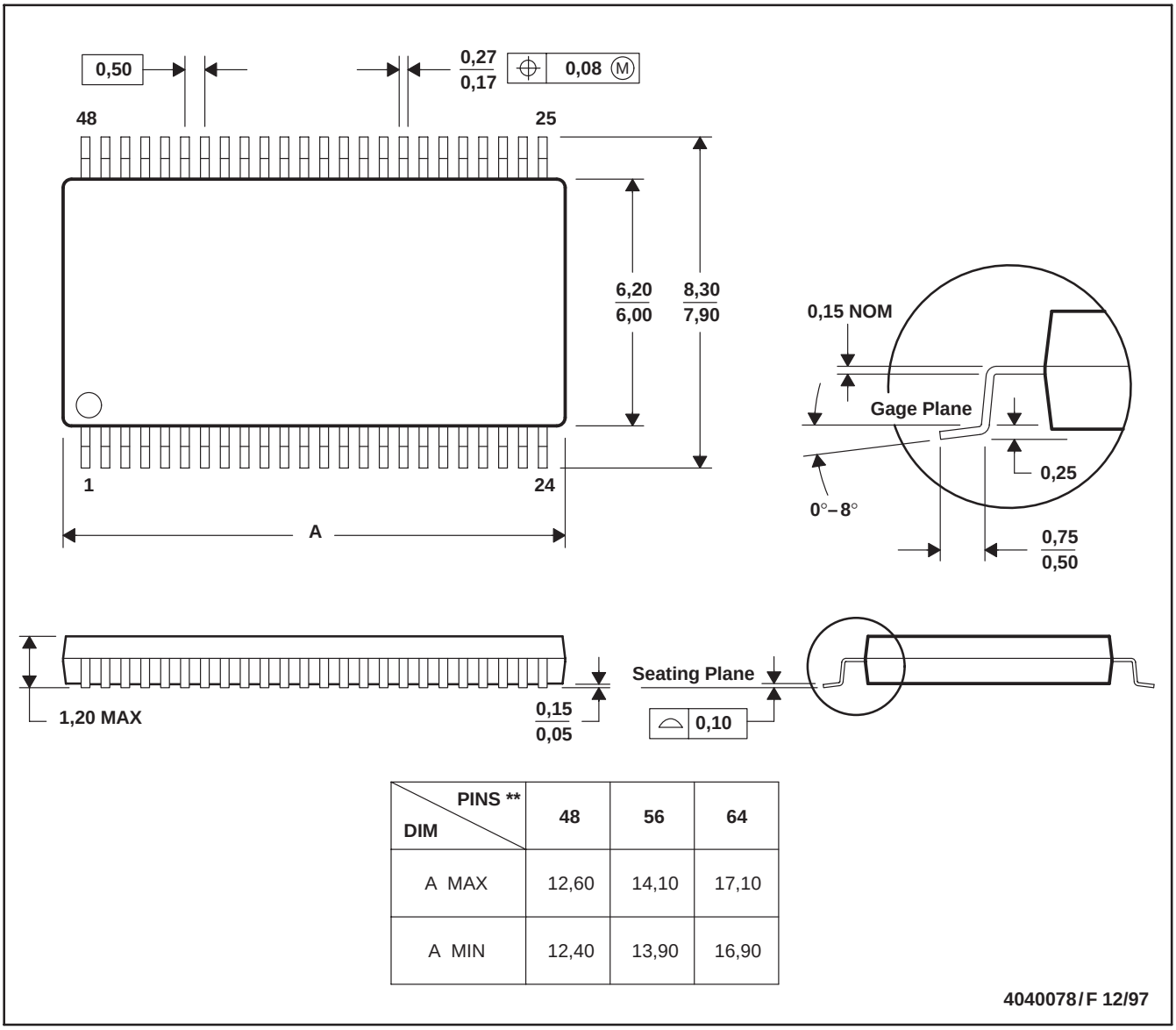

VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 2.5 ns, $t_f$ ≤ 2.5 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 5. Load Circuit and Voltage Waveforms**

**DGG (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**48 PINS SHOWN**




| DIM \ PINS ** | 48 | 56 | 64 |
|---|---|---|---|
| A MAX | 12,60 | 14,10 | 17,10 |
| A MIN | 12,40 | 13,90 | 16,90 |

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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