

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT194

4-bit bidirectional universal shift register

Product specification
File under Integrated Circuits, IC06

December 1990

4-bit bidirectional universal shift register

74HC/HCT194

FEATURES

- Shift-left and shift-right capability
- Synchronous parallel and serial data transfer
- Easily expanded for both serial and parallel operation
- Asynchronous master reset
- Hold (“do nothing”) mode
- Output capability: standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT194 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The functional characteristics of the 74HC/HCT194 4-bit bidirectional universal shift registers are indicated in the logic diagram and function table. The registers are fully synchronous.

The “194” design has special features which increase the range of application. The synchronous operation of the device is determined by the mode select inputs (S₀, S₁). As shown in the mode select table, data can be entered

and shifted from left to right (Q₀ → Q₁ → Q₂, etc.) or, right to left (Q₃ → Q₂ → Q₁, etc.) or parallel data can be entered, loading all 4 bits of the register simultaneously. When both S₀ and S₁ are LOW, existing data is retained in a hold (“do nothing”) mode. The first and last stages provide D-type serial data inputs (D_{SR}, D_{SL}) to allow multistage shift right or shift left data transfers without interfering with parallel load operation.

Mode select and data inputs are edge-triggered, responding only to the LOW-to-HIGH transition of the clock (CP). Therefore, the only timing restriction is that the mode control and selected data inputs must be stable one set-up time prior to the positive transition of the clock pulse.

The four parallel data inputs (D₀ to D₃) are D-type inputs. Data appearing on the D₀ to D₃ inputs, when S₀ and S₁ are HIGH, is transferred to the Q₀ to Q₃ outputs respectively, following the next LOW-to-HIGH transition of the clock. When LOW, the asynchronous master reset (\overline{MR}) overrides all other input conditions and forces the Q outputs LOW.

The “194” is similar in operation to the “195” universal shift register, with added features of shift-left without external connections and hold (“do nothing”) modes of operation.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay CP to Q _n	C _L = 15 pF; V _{CC} = 5 V	14	15	ns
t _{PHL}	\overline{MR} to Q _n		11	15	ns
f _{max}	maximum clock frequency		102	77	MHz
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	40	40	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

Σ = (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}; for HCT the condition is V_I = GND to V_{CC} – 1.5 V

4-bit bidirectional universal shift register

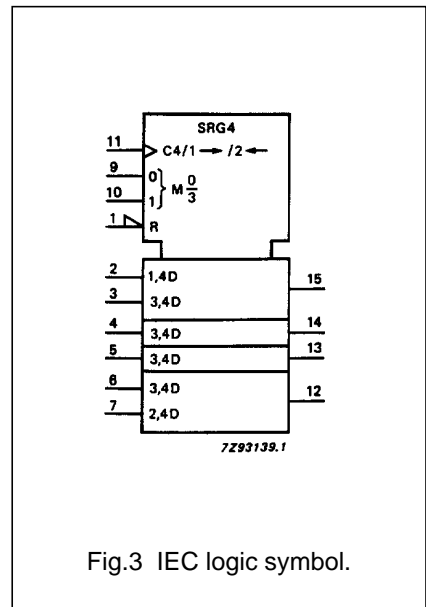
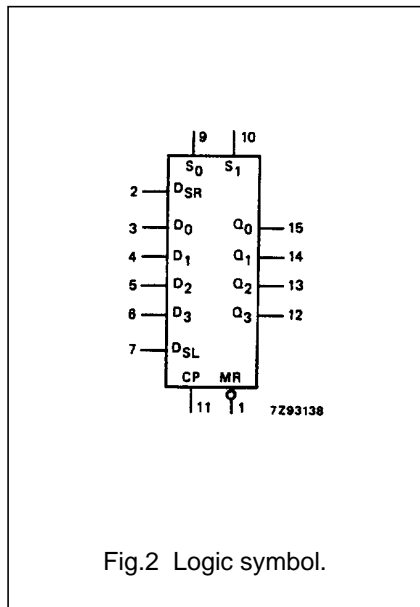
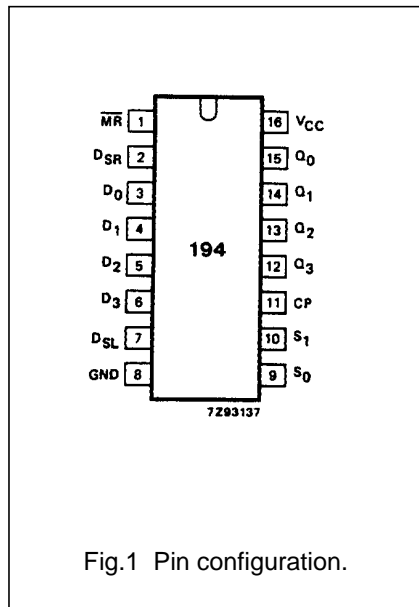
74HC/HCT194

ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	\overline{MR}	asynchronous master reset input (active LOW)
2	D _{SR}	serial data input (shift right)
3, 4, 5, 6	D ₀ to D ₃	parallel data inputs
7	D _{SL}	serial data input (shift left)
8	GND	ground (0 V)
9, 10	S ₀ , S ₁	mode control inputs
11	CP	clock input (LOW-to-HIGH edge-triggered)
15, 14, 13, 12	Q ₀ to Q ₃	parallel outputs
16	V _{CC}	positive supply voltage



4-bit bidirectional universal shift register

74HC/HCT194

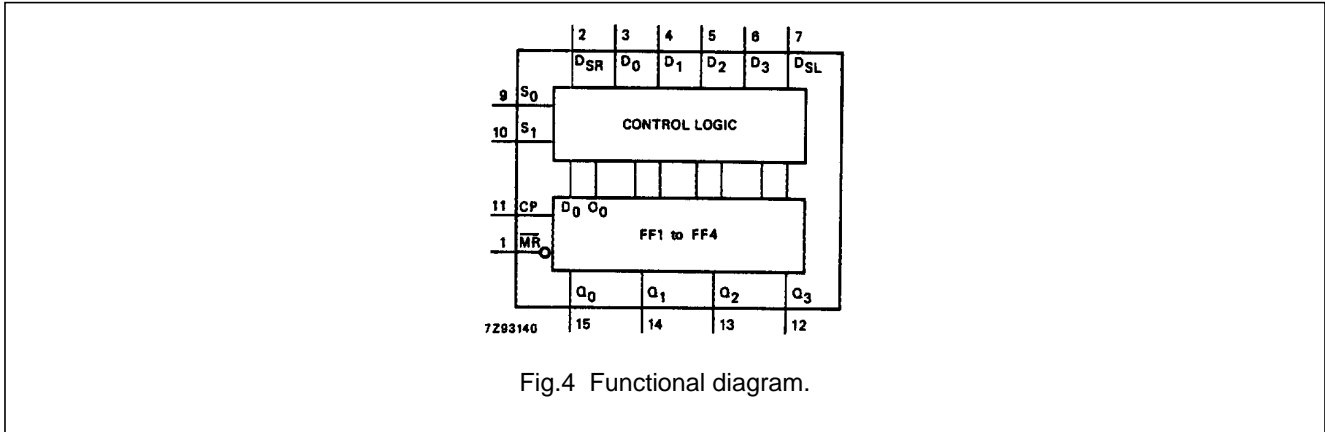


Fig.4 Functional diagram.

FUNCTION TABLE

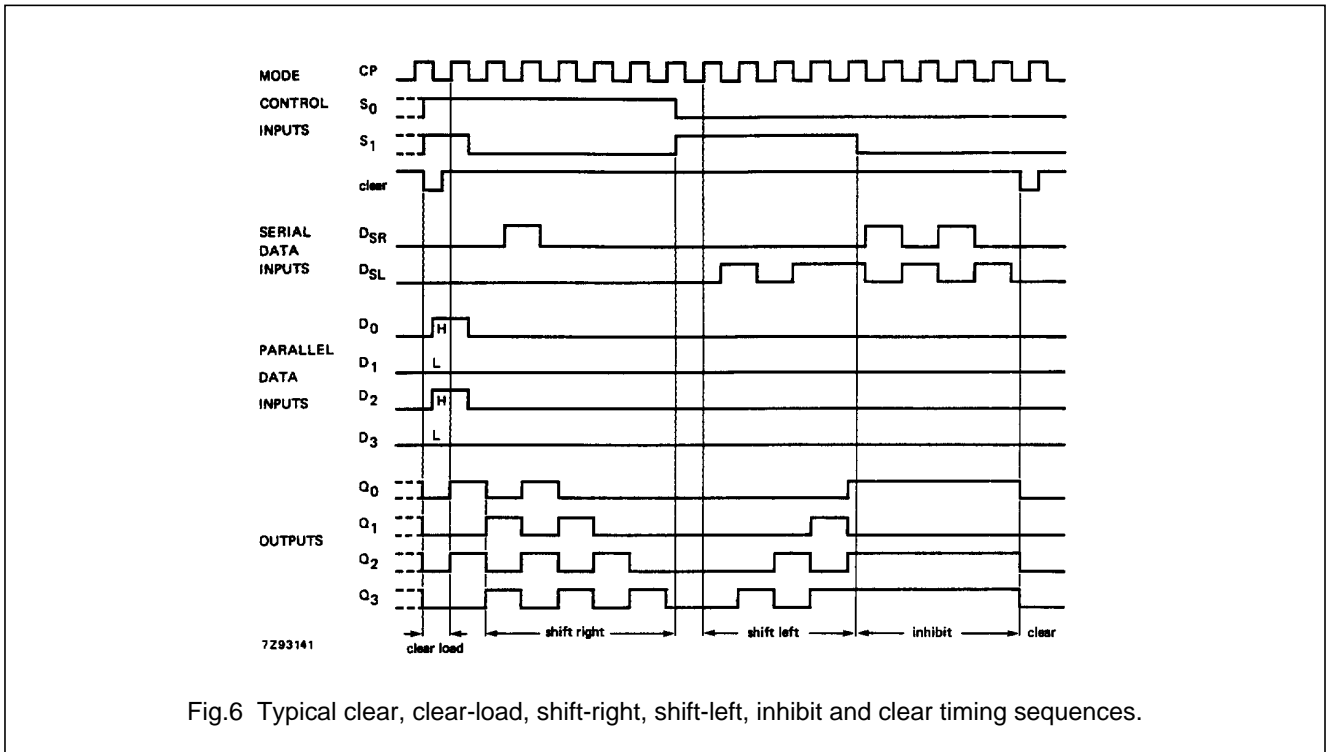
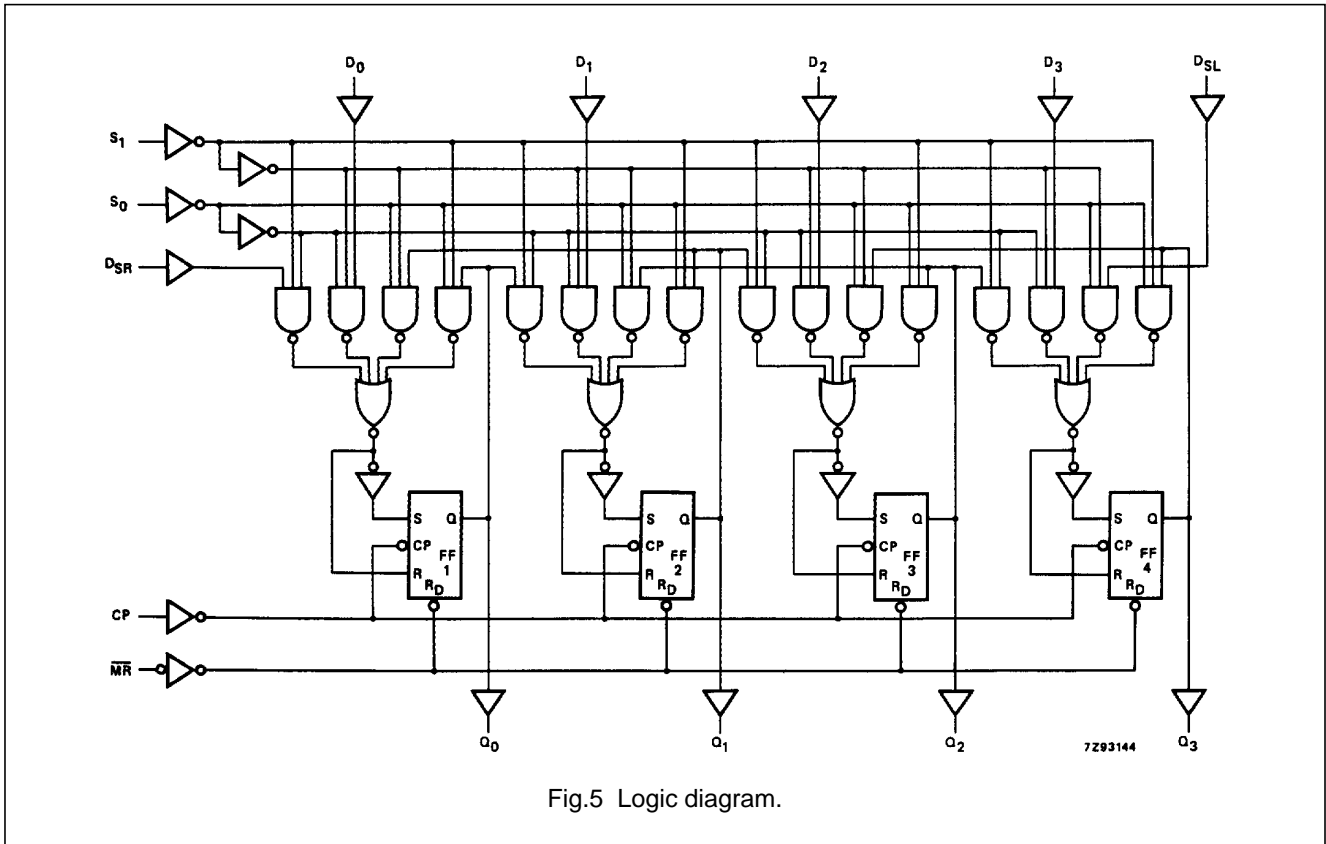
OPERATING MODES	INPUTS							OUTPUTS			
	CP	\overline{MR}	S ₁	S ₀	D _{SR}	D _{SL}	D _n	Q ₀	Q ₁	Q ₂	Q ₃
reset (clear)	X	L	X	X	X	X	X	L	L	L	L
hold ("do nothing")	X	H	l	l	X	X	X	q ₀	q ₁	q ₂	q ₃
shift left	↑	H	h	l	X	l	X	q ₁	q ₂	q ₃	L
	↑	H	h	l	X	h	X	q ₁	q ₂	q ₃	H
shift right	↑	H	l	h	l	X	X	L	q ₀	q ₁	q ₂
	↑	H	l	h	h	X	X	H	q ₀	q ₁	q ₂
parallel load	↑	H	h	h	X	X	d _n	d ₀	d ₁	d ₂	d ₃

Notes

- H = HIGH voltage level
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
 L = LOW voltage level
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
 q,d = lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW-to-HIGH CP transition
 X = don't care
 ↑ = LOW-to-HIGH CP transition

4-bit bidirectional universal shift register

74HC/HCT194



4-bit bidirectional universal shift register

74HC/HCT194

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

4-bit bidirectional universal shift register

74HC/HCT194

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V_{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t_{PHL}/t_{PLH}	propagation delay CP to Q_n		47 17 14	145 29 25		180 36 31		220 44 38	ns	2.0 4.5 6.0	Fig.7
t_{PHL}	propagation delay MR to Q_n		39 14 11	140 28 24		175 35 30		210 42 36	ns	2.0 4.5 6.0	Fig.8
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.7
t_W	clock pulse width HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.7
t_W	master reset pulse width; LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.8
t_{rem}	removal time \overline{MR} to CP	60 12 10	17 6 5		75 15 13		90 18 15		ns	2.0 4.5 6.0	Fig.8
t_{su}	set-up time D_n to CP	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig.9
t_{su}	set-up time S_0, S_1 to CP	80 16 12	22 8 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.10
t_{su}	set-up time D_{SR}, D_{SL} to CP	70 14 12	19 7 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	
t_h	hold time D_n to CP	0 0 0	-14 -5 -4		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.9
t_h	hold time S_0, S_1 to CP	0 0 0	-11 -4 -3		0 0 0		0 0 0		ns	2.0 4.5 6.0	Fig.10
t_h	hold time D_{SR}, D_{SL} to CP	0 0 0	-17 -6 -5		0 0 0		0 0 0		ns	2.0 4.5 6.0	
f_{max}	maximum clock pulse frequency	6.0 30 35	31 93 111		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.7

4-bit bidirectional universal shift register

74HC/HCT194

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
D _n	0.15
D _{SR} , D _{SL}	0.15
CP	0.50
\overline{MR}	0.45
S _n	0.90

4-bit bidirectional universal shift register

74HC/HCT194

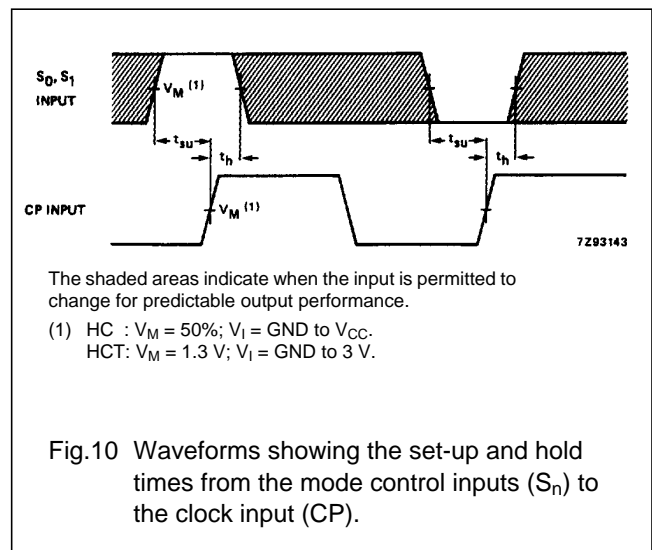
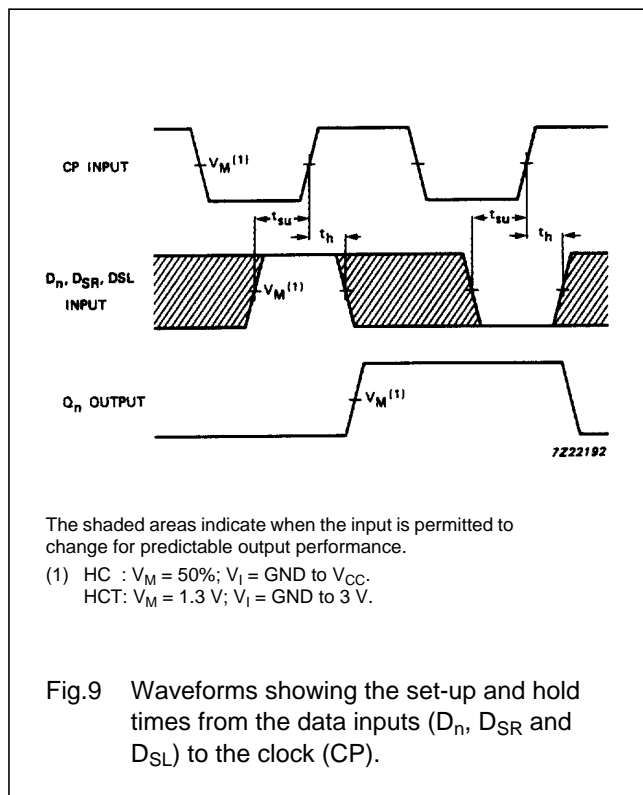
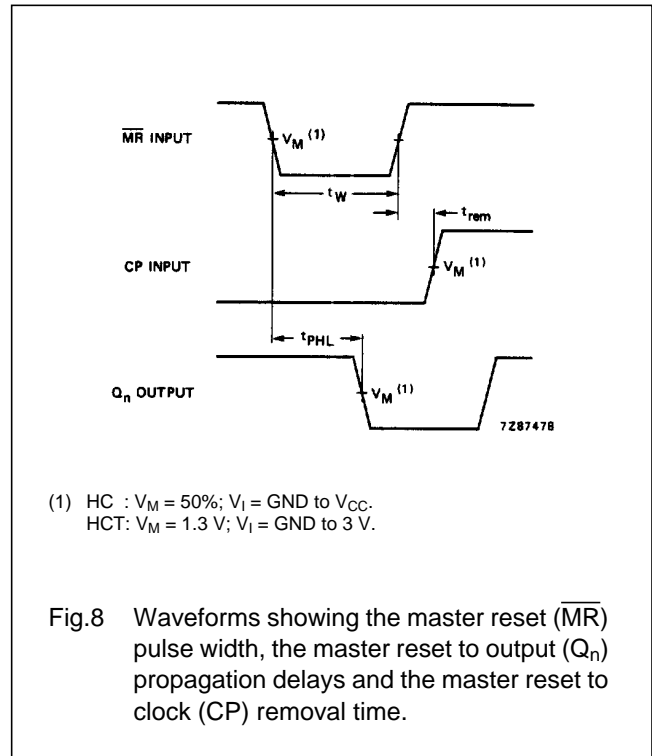
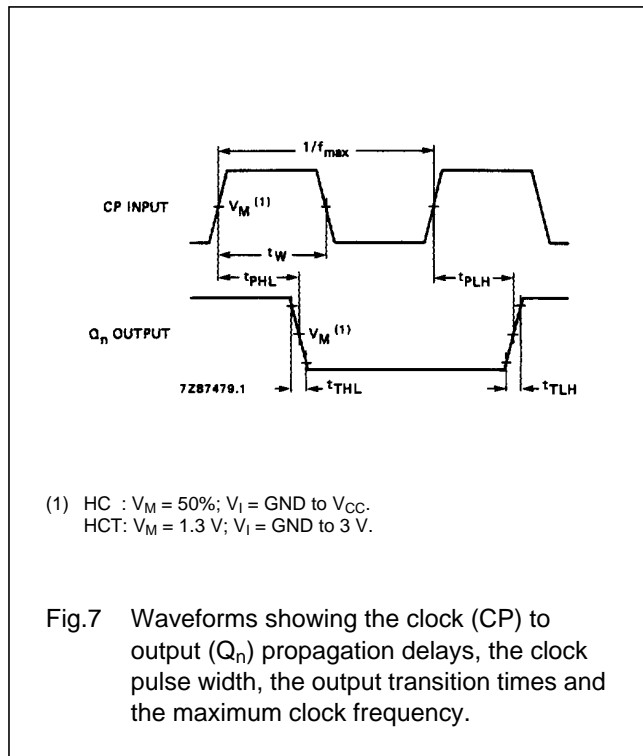
AC CHARACTERISTICS FOR 74HCTGND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		18	32		40		48	ns	4.5	Fig.7
t _{PHL}	propagation delay MR to Q _n		18	32		40		48	ns	4.5	Fig.8
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.7
t _W	clock pulse width HIGH or LOW	16	7		20		24		ns	4.5	Fig.7
t _W	master reset pulse width; LOW	16	7		20		24		ns	4.5	Fig.8
t _{rem}	removal time MR to CP	12	6		15		18		ns	4.5	Fig.8
t _{su}	set-up time D _n to CP	14	7		18		21		ns	4.5	Fig.9
t _{su}	set-up time S ₀ , S ₁ to CP	20	10		25		30		ns	4.5	Fig.10
t _{su}	set-up time D _{SR} , D _{SL} to CP	14			18		21		ns	4.5	Fig.9
t _h	hold time D _n to CP	0	-7		0		0		ns	4.5	Fig.9
t _h	hold time S ₀ , S ₁ to CP	0	-5		0		0		ns	4.5	Fig.10
t _h	hold time D _{SR} , D _{SL} to CP	0	-7		0		0		ns	4.5	Fig.9
f _{max}	maximum clock pulse frequency	30	70		24		20		MHz	4.5	Fig.7

4-bit bidirectional universal shift register

74HC/HCT194

AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".

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