



**THE DATASHEET OF  
CD74HC4351M96**



## High-Speed CMOS Logic Analog Multiplexers/Demultiplexers with Latch

### Features

- Wide Analog Input Voltage Range . . . . .  $\pm 5V$  (Max)
- Low "On" Resistance
  - $V_{CC} - V_{EE} = 4.5V$  . . . . .  $70\Omega$  (Typ)
  - $V_{CC} - V_{EE} = 9V$  . . . . .  $40\Omega$  (Typ)
- Low Crosstalk Between Switches
- Fast Switching and Propagation Speeds
- "Break-Before-Make" Switching
- Wide Operating Temperature Range . . .  $-55^{\circ}C$  to  $125^{\circ}C$
- HC Types
  - 2V to 6V Operation, Control; 0V to 10V Switch
  - High Noise Immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- HCT Types
  - 4.5V to 5.5V Operation, Control; 0V to 10V Switch
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)
  - CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$

### Description

The 'HC4351, CD74HCT4351, and CD74HC4352 are digitally controlled analog switches which utilize silicon-gate

CMOS technology to achieve operating speeds similar to LSTTL with the low power consumption of standard CMOS integrated circuits.

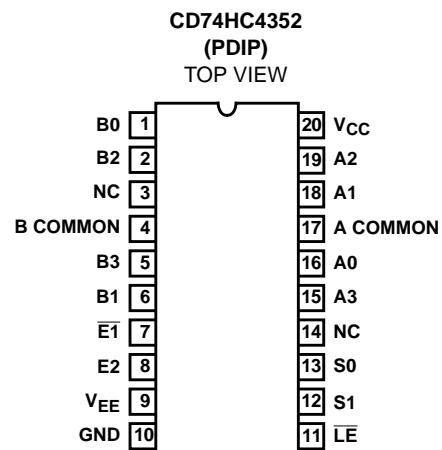
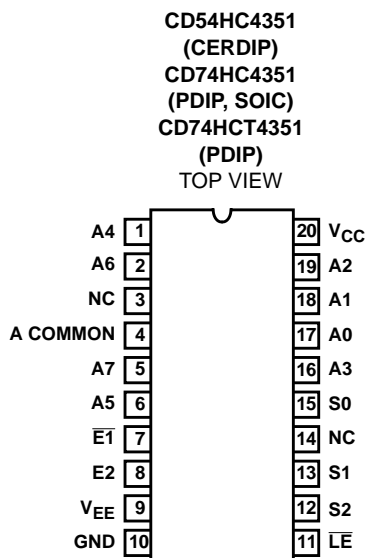
These analog multiplexers/demultiplexers are, in essence, the HC/HCT4015 and HC4052 preceded by address latches that are controlled by an active low Latch Enable input ( $\overline{LE}$ ). Two Enable inputs, one active low ( $\overline{E1}$ ), and the other active high (E2) are provided allowing enabling with either input voltage level.

### Ordering Information

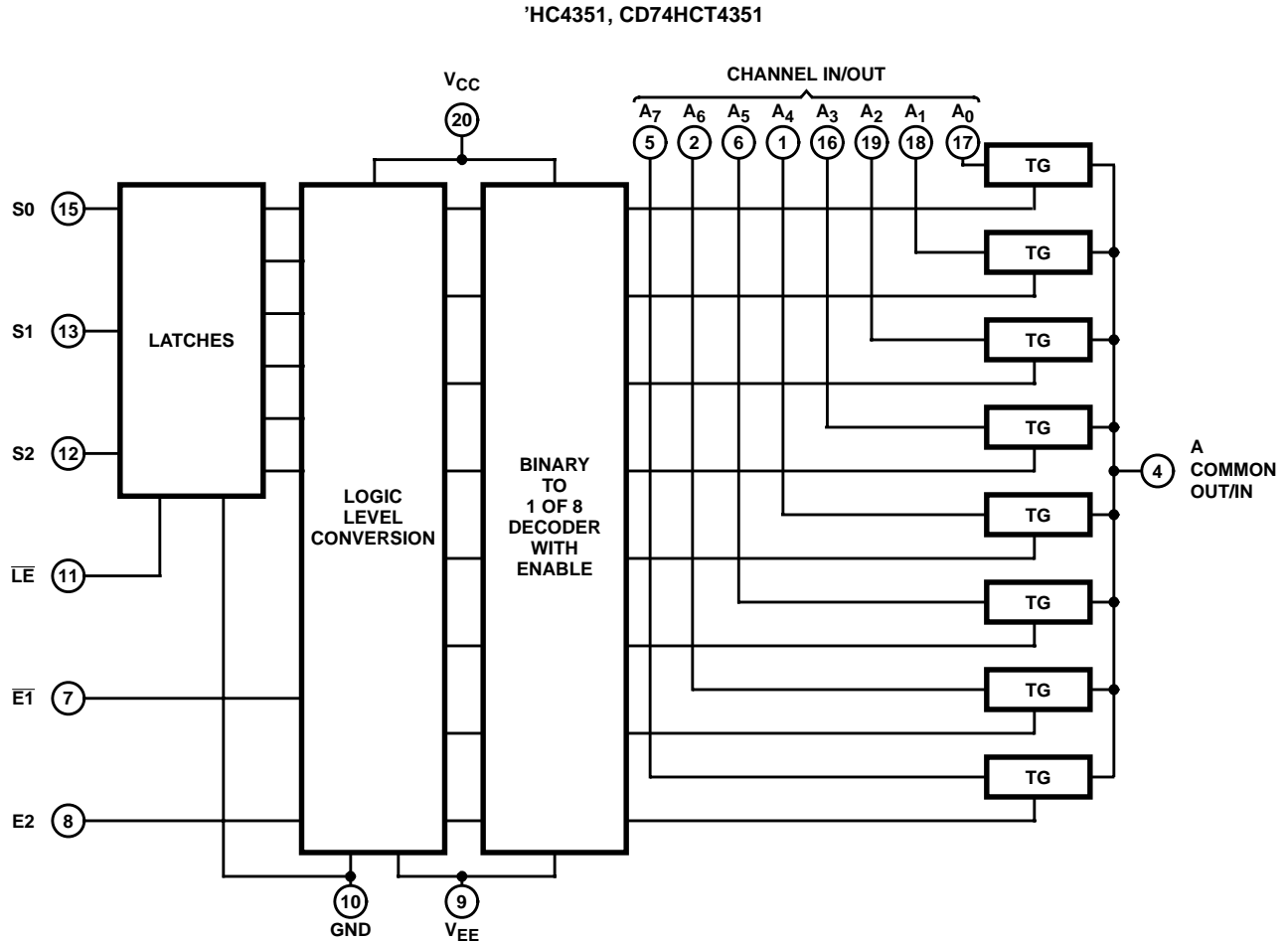
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC4351F3A	-55 to 125	20 Ld CERDIP
CD74HC4351E	-55 to 125	20 Ld PDIP
CD74HC4351M	-55 to 125	20 Ld SOIC
CD74HC4351M96	-55 to 125	20 Ld SOIC
CD74HCT4351E	-55 to 125	20 Ld PDIP
CD74HC4352E	-55 to 125	20 Ld PDIP

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

### Pinouts



Functional Diagram



TRUTH TABLE  
'HC4351, CD74HCT4351

INPUT STATES					(NOTE 1) "ON" SWITCHES $\overline{LE} = H$
$\overline{E1}$	E2	S2	S1	S0	
L	H	L	L	L	A <sub>0</sub>
L	H	L	L	H	A <sub>1</sub>
L	H	L	H	L	A <sub>2</sub>
L	H	L	H	H	A <sub>3</sub>
L	H	H	L	L	A <sub>4</sub>
L	H	H	L	H	A <sub>5</sub>
L	H	H	H	L	A <sub>6</sub>
L	H	H	H	H	A <sub>7</sub>
H	L	X	X	X	None

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

NOTE:

1. When  $\overline{LE}$  is low S0-S2 data are latched and switches cannot change state.

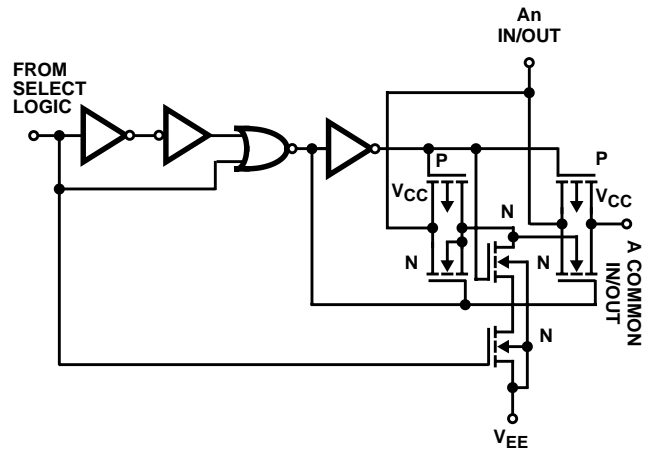


FIGURE 1. DETAIL OF ONE HC/HCT4351 SWITCH



# CD54HC4351, CD74HC4351, CD74HCT4351, CD74HC4352

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ .....	-0.5V to 7V
DC Supply Voltage, $V_{CC} - V_{EE}$ .....	-0.5V to 10.5V
DC Supply Voltage, $V_{EE}$ .....	0.5V to -7V
DC Input Diode Current, $I_{IK}$ For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Switch Diode Current, $I_{OK}$ For $V_I < V_{EE} - 0.5V$ or $V_I < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Switch Current, $I_{OK}$ (Note 3) For $V_I > V_{EE} - 0.5V$ or $V_I < V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Diode Current, $I_{OK}$ For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$ For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Operating Conditions

Temperature Range, $T_A$ .....	-55°C to 125°C
Supply Voltage Range, $V_{CC}$ HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
Supply Voltage Range, $V_{CC} - V_{EE}$ HC, HCT Types (Figure 3) .....	.2V to 10V
Supply Voltage Range, $V_{EE}$ HC, HCT Types (Figure 4) .....	0V to -6V
DC Input or Output Voltage, $V_I$ .....	GND to $V_{CC}$
Analog Switch I/O Voltage, $V_{IS}$ .....	$V_{EE}$ (Min) ..... $V_{CC}$ (Max)
Input Rise and Fall Time, $t_r, t_f$ 2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTES:

- In certain applications, the external load-resistor current may include both  $V_{CC}$  and signal-line components. To avoid drawing  $V_{CC}$  current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6V (calculated from  $R_{ON}$  values shown in the DC Electrical Specifications table). No  $V_{CC}$  current will flow through  $R_L$  if the switch current flows into terminal 3 on the 'HC4351 and CD74HCT4351; terminals 3 and 13 on the CD74HC4352.
- The package thermal impedance is calculated in accordance with JESD 51-7.

## Thermal Information

Thermal Resistance (Typical, Note 4)	$\theta_{JA}$ (°C/W)
E (PDIP) Package .....	69
M (SOIC) Package .....	58
Maximum Junction Temperature .....	150°C
Maximum Storage Temperature Range .....	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s) .....	300°C (SOIC - Lead Tips Only)

## Recommended Operating Area as a Function of Supply Voltage

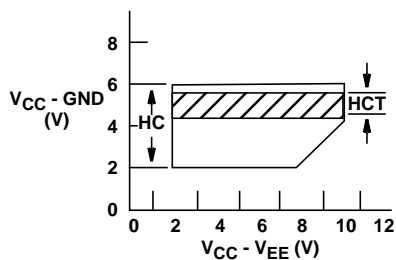


FIGURE 3.

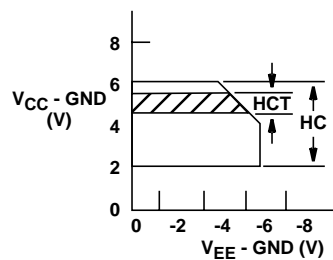


FIGURE 4.

**CD54HC4351, CD74HC4351, CD74HCT4351, CD74HC4352**

**DC Electrical Specifications**

PARAMETER	SYMBOL	TEST CONDITIONS				25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS	
		V <sub>I</sub> (V)	V <sub>IS</sub> (V)	V <sub>EE</sub> (V)	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX		
<b>HC TYPES</b>														
High Level Input Voltage	V <sub>IH</sub>	-	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
					4.5	3.15	-	-	3.15	-	3.15	-	V	
					6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	V <sub>IL</sub>	-	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
					4.5	-	-	1.35	-	1.35	-	1.35	V	
					6	-	-	1.8	-	1.8	-	1.8	V	
“ON” Resistance I <sub>O</sub> = 1mA Figure 9	R <sub>ON</sub>	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>CC</sub> or V <sub>EE</sub>	0	4.5	-	70	160	-	200	-	240	Ω	
				0	6	-	60	140	-	175	-	210	Ω	
				-4.5	4.5	-	40	120	-	150	-	180	Ω	
			V <sub>CC</sub> to V <sub>EE</sub>	0	4.5	-	90	180	-	225	-	270	Ω	
				0	6	-	80	160	-	200	-	240	Ω	
				-4.5	4.5	-	45	130	-	162	-	195	Ω	
Maximum “ON” Resistance Between Any Two Channels	ΔR <sub>ON</sub>	-	-	0	4.5	-	10	-	-	-	-	Ω		
				0	6	-	8.5	-	-	-	-	Ω		
				-4.5	4.5	-	5	-	-	-	-	Ω		
Switch On/Off Leakage Current 4 Channels (4352)	I <sub>IZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>	For Switch OFF: When V <sub>IS</sub> = V <sub>CC</sub> V <sub>OS</sub> = V <sub>EE</sub> ; When V <sub>IS</sub> = V <sub>EE</sub> ; V <sub>OS</sub> = V <sub>CC</sub> For Switch ON: All Applicable Combinations of V <sub>IS</sub> and V <sub>OS</sub> Voltage Levels	0	6	-	-	±0.1	-	±1	-	±1	μA	
				-5	5	-	-	±0.2	-	±2	-	±2	μA	
Switch On/Off Leakage Current 8 Channels (4351)	I <sub>IZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>		0	6	-	-	±0.2	-	±2	-	±2	μA	
				-5	5	-	-	±0.4	-	±4	-	±4	μA	
Control Input Leakage Current	I <sub>IL</sub>	V <sub>CC</sub> or GND		-	0	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current I <sub>O</sub> = 0	I <sub>CC</sub>	V <sub>CC</sub> or GND		When V <sub>IS</sub> = V <sub>EE</sub> ; V <sub>OS</sub> = V <sub>CC</sub> ; When V <sub>IS</sub> = V <sub>CC</sub> ; V <sub>OS</sub> = V <sub>EE</sub>	0	6	-	-	8	-	80	-	160	μA
			-5		5	-	-	16	-	160	-	320	μA	

**CD54HC4351, CD74HC4351, CD74HCT4351, CD74HC4352**

**DC Electrical Specifications (Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS				25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	V <sub>IS</sub> (V)	V <sub>EE</sub> (V)	V <sub>CC</sub> (V)	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HCT TYPES</b>													
High Level Input Voltage	V <sub>IH</sub>	-	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
“ON” Resistance I <sub>O</sub> = 1mA Figure 9	R <sub>ON</sub>	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>CC</sub> or V <sub>EE</sub>	0	4.5	-	70	160	-	200	-	240	Ω
				-4.5	4.5	-	40	120	-	150	-	180	Ω
		V <sub>CC</sub> to V <sub>EE</sub>	0	4.5	-	90	180	-	225	-	270	Ω	
			-4.5	4.5	-	45	130	-	162	-	195	Ω	
Maximum “ON” Resistance Between Any Two Channels	ΔR <sub>ON</sub>	-	-	0	4.5	-	10	-	-	-	-	-	Ω
				-4.5	4.5	-	5	-	-	-	-	-	-
Switch On/Off Leakage Current 4 Channels (4352)	I <sub>IZ</sub>	V <sub>IH</sub> or V <sub>IL</sub>	For Switch OFF: When V <sub>IS</sub> = V <sub>CC</sub> V <sub>OS</sub> = V <sub>EE</sub> ; When V <sub>IS</sub> = V <sub>EE</sub> , V <sub>OS</sub> = V <sub>CC</sub> For Switch ON: All Applicable Combinations of V <sub>IS</sub> and V <sub>OS</sub> Voltage Levels	0	6	-	-	±0.1	-	±1	-	±1	μA
-5				5	-	-	±0.2	-	±2	-	±2	μA	
0				6	-	-	±0.2	-	±2	-	±2	μA	
-5				5	-	-	±0.4	-	±4	-	±4	μA	
Switch On/Off Leakage Current 8 Channels (4351)													
Control Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND	-	0	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current I <sub>O</sub> = 0	I <sub>CC</sub>	Any Voltage Between V <sub>CC</sub> and GND	When V <sub>IS</sub> = V <sub>EE</sub> , V <sub>OS</sub> = V <sub>CC</sub> ; When V <sub>IS</sub> = V <sub>CC</sub> , V <sub>OS</sub> = V <sub>EE</sub>	0	5.5	-	-	8	-	80	-	160	μA
				-4.5	5.5	-	-	16	-	160	-	320	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 5)	V <sub>CC</sub> -2.1	-	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

5. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

**HCT Input Loading Table**

TYPE	INPUT	UNIT LOADS
All	$\overline{E1}$ , E2, Sn	0.5
(4351, 4352)	$\overline{LE}$	1.5

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Table, e.g., 360μA max at 25°C.

**CD54HC4351, CD74HC4351, CD74HCT4351, CD74HC4352**

**Switching Specifications** Input  $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{EE}$ (V)	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
Propagation Delay, Switch In to Switch Out	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	0	2	-	-	35	-	45	-	55	ns
			0	4.5	-	-	7	-	9	-	11	ns
			0	6	-	-	6	-	8	-	9	ns
			-4.5	4.5	-	-	5	-	7	-	8	ns
Maximum Switch Turn "ON" Delay 4351 $\bar{E}1, E2, \bar{L}E$ to $V_{OS}$	$t_{PZH}, t_{PZL}$	$C_L = 50\text{pF}$	0	2	-	-	300	-	375	-	450	ns
			0	4.5	-	-	60	-	75	-	90	ns
			0	6	-	-	51	-	64	-	77	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	-	5	-	27	-	-	-	-	-	ns
Maximum Switch Turn "ON" Delay 4352 $\bar{E}1, E2, \bar{L}E$ to $V_{OS}$	$t_{PZH}, t_{PZL}$	$C_L = 50\text{pF}$	0	2	-	-	350	-	440	-	525	ns
			0	4.5	-	-	70	-	88	-	105	ns
			0	6	-	-	60	-	75	-	90	ns
			-4.5	4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn "ON" Delay 4351 $S_n$ to $V_{OS}$	$t_{PZH}, t_{PZL}$	$C_L = 50\text{pF}$	0	2	-	-	300	-	375	-	450	ns
			0	4.5	-	-	60	-	75	-	90	ns
			0	6	-	-	51	-	64	-	77	ns
			-4.5	4.5	-	-	50	-	63	-	75	ns
		$C_L = 15\text{pF}$	-	5	-	27	-	-	-	-	-	ns
Maximum Switch Turn "ON" Delay 4352 $S_n$ to $V_{OS}$	$t_{PZH}, t_{PZL}$	$C_L = 50\text{pF}$	0	2	-	-	375	-	470	-	565	ns
			0	4.5	-	-	75	-	94	-	113	ns
			0	6	-	-	64	-	80	-	96	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 $\bar{E}1$ to $V_{OS}$	$t_{PHZ}, t_{PLZ}$	$C_L = 50\text{pF}$	0	2	-	-	250	-	315	-	375	ns
			0	4.5	-	-	50	-	63	-	75	ns
			0	6	-	-	43	-	54	-	64	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
		$C_L = 15\text{pF}$	-	5	-	21	-	-	-	-	-	ns

**CD54HC4351, CD74HC4351, CD74HCT4351, CD74HC4352**

**Switching Specifications** Input  $t_r$ ,  $t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>EE</sub> (V)	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Maximum Switch Turn "OFF" Delay 4351 E2 to V <sub>OS</sub>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	0	2	-	-	250	-	315	-	375	ns
			0	4.5	-	-	50	-	63	-	75	ns
			0	6	-	-	43	-	54	-	64	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
		C <sub>L</sub> = 15pF	-	5	-	21	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 LE to V <sub>OS</sub>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	0	2	-	-	275	-	345	-	415	ns
			0	4.5	-	-	55	-	69	-	83	ns
			0	6	-	-	47	-	59	-	71	ns
			-4.5	4.5	-	-	45	-	56	-	68	ns
		C <sub>L</sub> = 15pF	-	5	-	21	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 Sn to V <sub>OS</sub>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	0	2	-	-	275	-	345	-	415	ns
			0	4.5	-	-	55	-	69	-	83	ns
			0	6	-	-	47	-	59	-	71	ns
			-4.5	4.5	-	-	48	-	60	-	71	ns
		C <sub>L</sub> = 15pF	-	5	-	21	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4352 E1, E2, LE to V <sub>OS</sub>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	0	2	-	-	275	-	345	-	415	ns
			0	4.5	-	-	55	-	69	-	83	ns
			0	6	-	-	47	-	59	-	71	ns
			-4.5	4.5	-	-	50	-	63	-	75	ns
		C <sub>L</sub> = 15pF	-	5	-	21	-	-	-	-	-	ns
Setup Time 4351 Sn to LE	t <sub>SU</sub>	C <sub>L</sub> = 50pF	0	2	-	-	60	-	75	-	90	ns
			0	4.5	-	-	12	-	15	-	18	ns
			0	6	-	-	10	-	13	-	15	ns
			-4.5	4.5	-	-	18	-	23	-	27	ns
			C <sub>L</sub> = 15pF	-	5	-	21	-	-	-	-	-
Hold Time 4351 and 4352 Sn to LE	t <sub>H</sub>	C <sub>L</sub> = 50pF	0	2	5	-	-	5	-	5	-	ns
			0	4.5	5	-	-	5	-	5	-	ns
			0	6	5	-	-	5	-	5	-	ns
			-4.5	4.5	5	-	-	5	-	5	-	ns
			C <sub>L</sub> = 15pF	-	5	-	21	-	-	-	-	-
Pulse Width 4351 and 4352 LE	t <sub>W</sub>	C <sub>L</sub> = 50pF	0	2	100	-	-	125	-	150	-	ns
			0	4.5	20	-	-	25	-	30	-	ns
			0	6	17	-	-	21	-	26	-	ns
			-4.5	4.5	25	-	-	31	-	38	-	ns
			C <sub>L</sub> = 15pF	-	5	-	21	-	-	-	-	-
Input (Control) Capacitance	C <sub>I</sub>	-	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 6, 7) 4351	C <sub>PD</sub>	-	-	5	-	50	-	-	-	-	pF	

**CD54HC4351, CD74HC4351, CD74HCT4351, CD74HC4352**

**Switching Specifications** Input  $t_r$ ,  $t_f = 6\text{ns}$  (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>EE</sub> (V)	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Power Dissipation Capacitance (Notes 6, 7) 4352	C <sub>PD</sub>	-	-	5	-	74	-	-	-	-	-	pF
<b>HCT TYPES</b>												
Propagation Delay, Switch In to Switch Out	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	7	-	9	-	11	ns
			-4.5	4.5	-	-	5	-	7	-	8	ns
Maximum Switch Turn "ON" Delay 4351 E <sub>1</sub> , E <sub>2</sub> , LE to V <sub>OS</sub>	t <sub>PZH</sub> , t <sub>PZL</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	75	-	94	-	113	ns
			-4.5	4.5	-	-	60	-	75	-	90	ns
		C <sub>L</sub> = 15pF	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn "ON" Delay 4351 Sn to V <sub>OS</sub>	t <sub>PZH</sub> , t <sub>PZL</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	75	-	94	-	113	ns
			-4.5	4.5	-	-	60	-	75	-	90	ns
		C <sub>L</sub> = 15pF	-	5	-	35	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 E <sub>1</sub> to V <sub>OS</sub>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	55	-	69	-	83	ns
			-4.5	4.5	-	-	40	-	50	-	60	ns
		C <sub>L</sub> = 15pF	-	5	-	23	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 E <sub>2</sub> to V <sub>OS</sub>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	60	-	75	-	90	ns
			-4.5	4.5	-	-	50	-	63	-	75	ns
		C <sub>L</sub> = 15pF	-	5	-	23	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 LE to V <sub>OS</sub>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	60	-	75	-	90	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
		C <sub>L</sub> = 15pF	-	5	-	23	-	-	-	-	-	ns
Maximum Switch Turn "OFF" Delay 4351 Sn to V <sub>OS</sub>	t <sub>PHZ</sub> , t <sub>PLZ</sub>	C <sub>L</sub> = 50pF	0	4.5	-	-	65	-	81	-	98	ns
			-4.5	4.5	-	-	55	-	69	-	83	ns
		C <sub>L</sub> = 15pF	-	5	-	23	-	-	-	-	-	ns
Setup Time 4351 Sn to LE		C <sub>L</sub> = 50pF	0	4.5	-	-	12	-	15	-	18	ns
			-4.5	4.5	-	-	14	-	18	-	21	ns
Hold Time 4351 and 4352 Sn to LE		C <sub>L</sub> = 50pF	0	4.5	5	-	-	5	-	5	-	ns
			-4.5	4.5	5	-	-	5	-	5	-	ns
Pulse Width 4351 LE	t <sub>W</sub>	C <sub>L</sub> = 50pF	0	4.5	25	-	-	31	-	28	-	ns
			-4.5	4.5	25	-	-	31	-	38	-	ns
Input (Control) Capacitance	C <sub>I</sub>	-	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 6, 7) 4351	C <sub>PD</sub>	-	-	5	-	52	-	-	-	-	-	pF

**NOTES:**

6. C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

7.  $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L + C_S) V_{CC}^2 f_o$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $C_S$  = switch capacitance,  $V_{CC}$  = supply voltage.

**CD54HC4351, CD74HC4351, CD74HCT4351, CD74HC4352**

**Analog Channel Specifications**  $T_A = 25^\circ\text{C}$

PARAMETER	SYMBOL	TEST CONDITIONS	TYPE	$V_{EE}$ (V)	$V_{CC}$ (V)	HC/HCT	UNITS
Switch Input Capacitance	$C_I$		All	-	-	5	pF
Common Capacitance	$C_{COM}$		4351	-	-	25	pF
			4352	-	-	12	pF
Minimum Switch Frequency Response at -3dB (Figure 6, 8)	$f_{MAX}$	See Figure 11 (Notes 8, 9)	4351	-	-	145	MHz
			4352	-2.25	2.25	165	MHz
			4351	-	-	180	MHz
			4352	-4.5	4.5	185	MHz
Crosstalk Between Any Two Switches (Note 11)		See Figure 10 (Notes 9, 10)	4351	-	-	N/A	dB
			4352	-2.25	2.25	(TBE)	dB
			4351	-	-	N/A	dB
			4352	-4.5	4.5	(TBE)	dB
Sine-Wave Distortion		See Figure 12	All	-2.25	2.25	0.035	%
			All	-4.5	4.5	0.018	%
$\bar{E}$ or S to Switch Feedthrough Noise		See Figure 13 (Notes 9, 10)	4351	-	-	-	mV
			4352	-2.25	2.25	(TBE)	mV
			4351	-	-	-	mV
			4352	-4.5	4.5	(TBE)	mV
Switch "OFF" Signal Feedthrough (Figure 6, 8)		See Figure 14 (Notes 9, 10)	4351	-	-	-73	dB
			4352	-2.25	2.25	-65	dB
			4351	-	-	-75	dB
			4352	-4.5	4.5	-67	dB

**NOTES:**

8. Adjust input voltage to obtain 0dBm at  $V_{OS}$  for,  $f_{in} = 1\text{MHz}$ .
9.  $V_{IS}$  is centered at  $(V_{CC} - V_{EE})/2$ .
10. Adjust input for 0dBm.
11. Not applicable for 'HC4351 and CD74HCT4351.

Typical Performance Curves

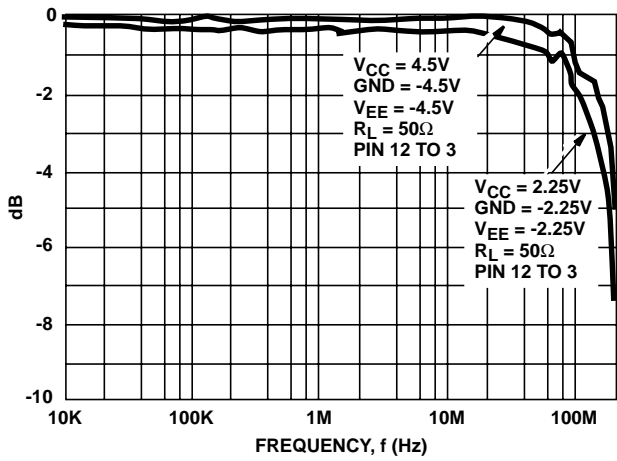


FIGURE 5. CHANNEL ON BANDWIDTH ('HC4351, CD74HCT4351)

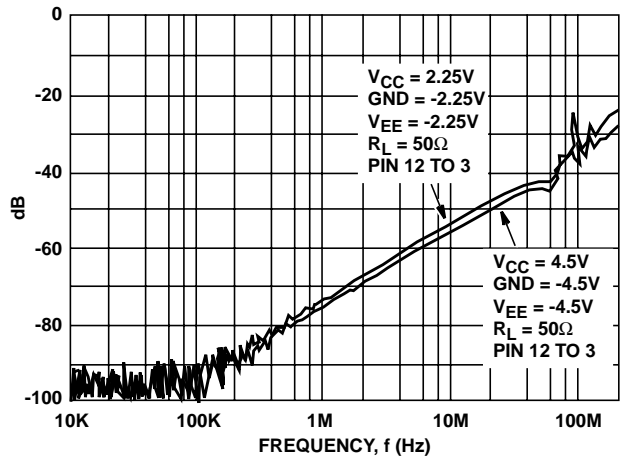


FIGURE 6. CHANNEL OFF FEEDTHROUGH ('HC4351, CD74HCT4351)

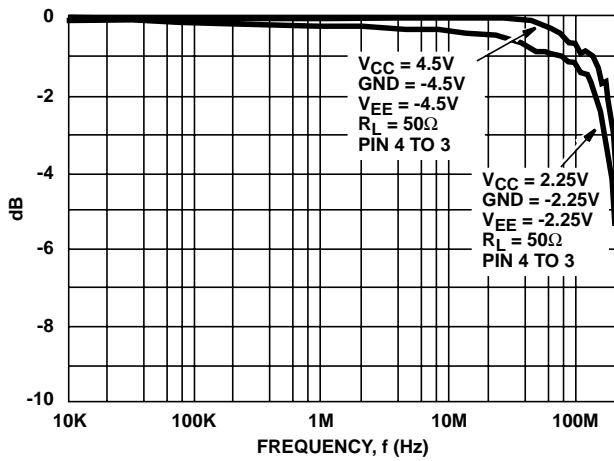


FIGURE 7. CHANNEL ON BANDWIDTH (CD74HC4352)

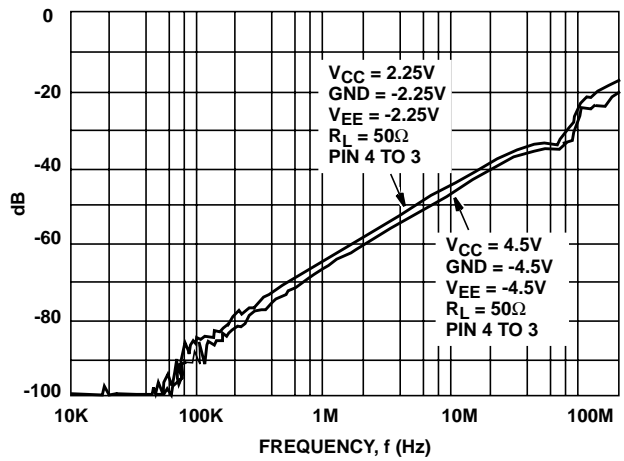


FIGURE 8. CHANNEL OFF FEEDTHROUGH (CD74HC4352)

Typical Performance Curves (Continued)

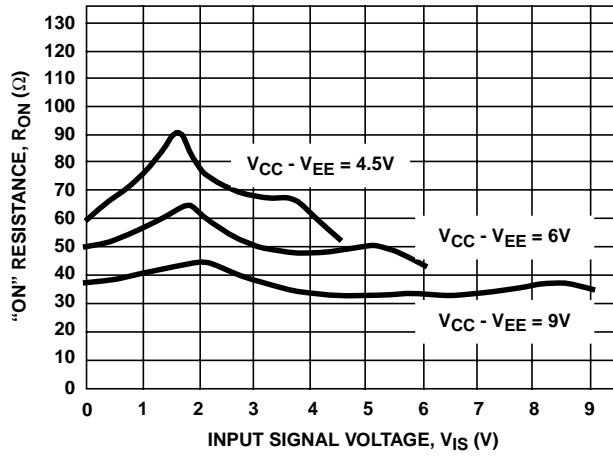


FIGURE 9. TYPICAL ON RESISTANCE vs INPUT SIGNAL VOLTAGE

Analog Test Circuits

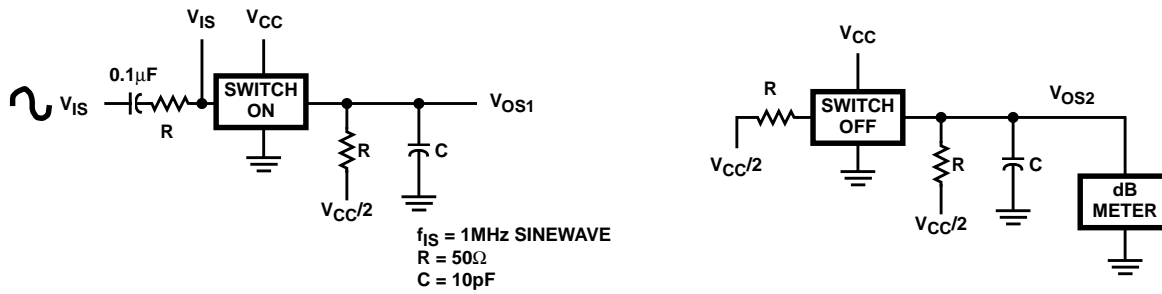


FIGURE 10. CROSTALK BETWEEN TWO SWITCHES TEST CIRCUIT

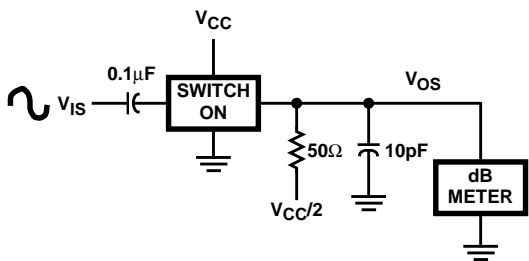


FIGURE 11. FREQUENCY RESPONSE TEST CIRCUIT

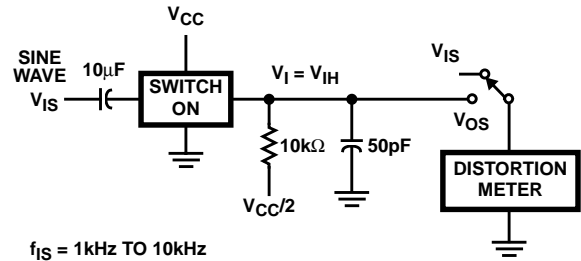


FIGURE 12. TOTAL HARMONIC DISTORTION TEST CIRCUIT

Analog Test Circuits (Continued)

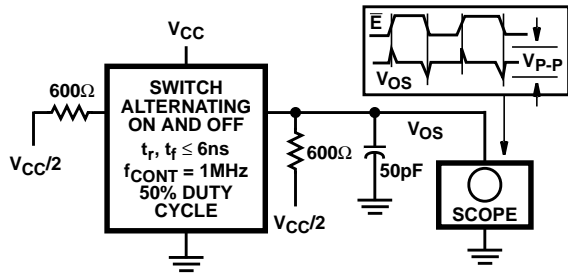


FIGURE 13. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

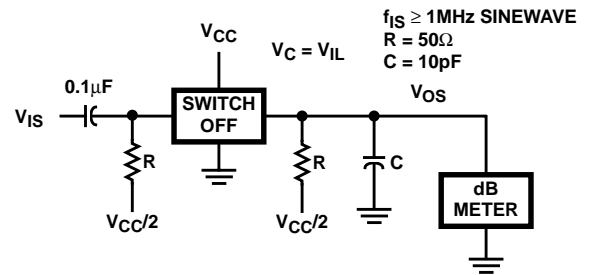
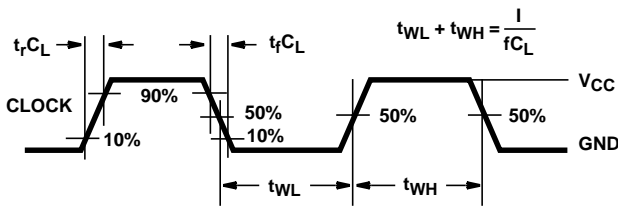


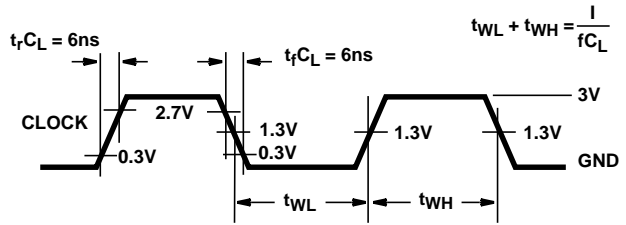
FIGURE 14. SWITCH OFF SIGNAL FEEDTHROUGH

Test Circuits and Waveforms



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 15. HC CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH



NOTE: Outputs should be switching from 10%  $V_{CC}$  to 90%  $V_{CC}$  in accordance with device truth table. For  $f_{MAX}$ , input duty cycle = 50%.

FIGURE 16. HCT CLOCK PULSE RISE AND FALL TIMES AND PULSE WIDTH

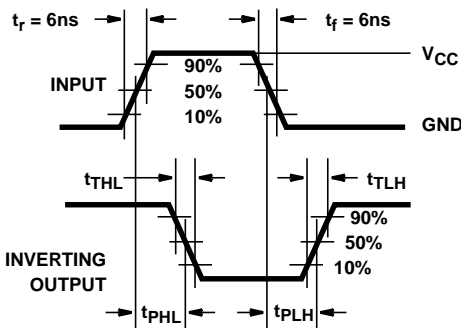


FIGURE 17. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

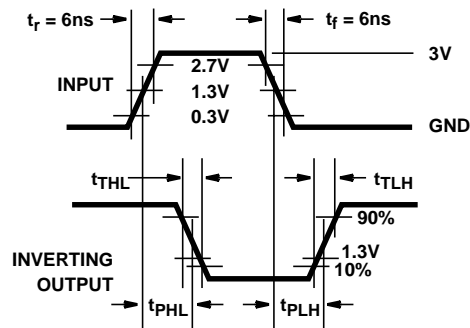


FIGURE 18. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

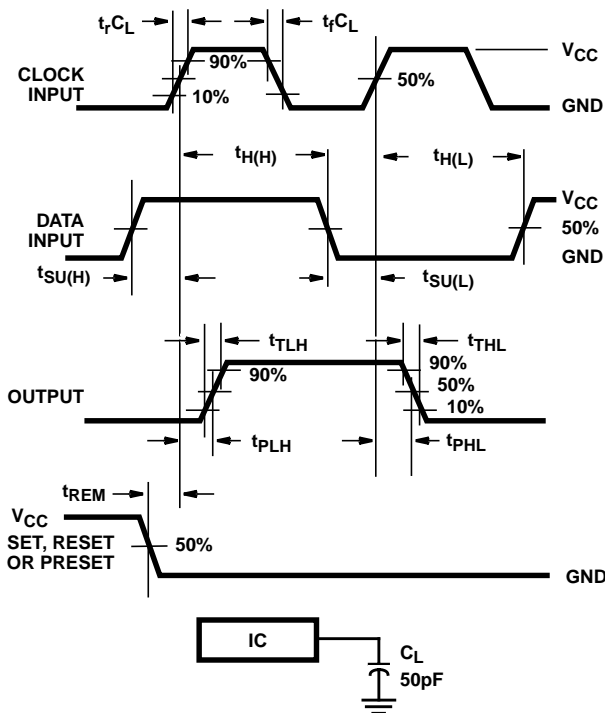


FIGURE 19. HC SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

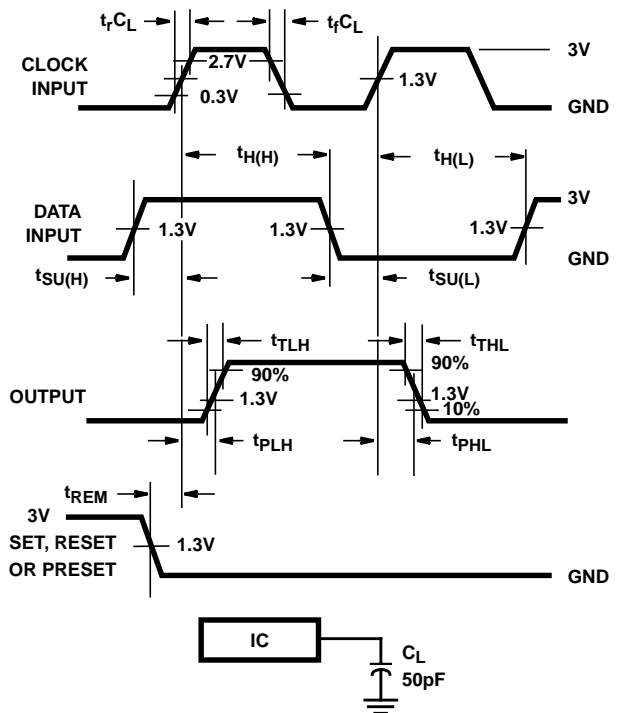


FIGURE 20. HCT SETUP TIMES, HOLD TIMES, REMOVAL TIME, AND PROPAGATION DELAY TIMES FOR EDGE TRIGGERED SEQUENTIAL LOGIC CIRCUITS

**Test Circuits and Waveforms** (Continued)

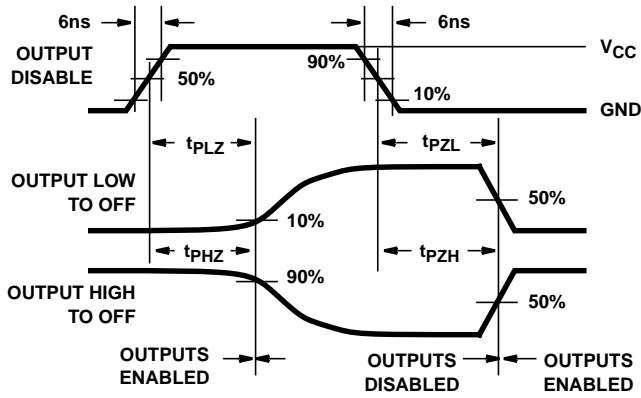


FIGURE 21. HC THREE-STATE PROPAGATION DELAY WAVEFORM

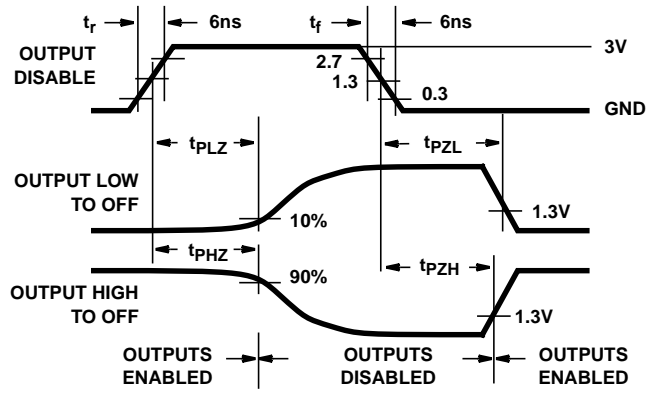
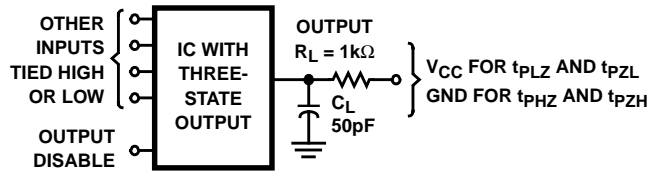


FIGURE 22. HCT THREE-STATE PROPAGATION DELAY WAVEFORM



NOTE: Open drain waveforms  $t_{PLZ}$  and  $t_{PZL}$  are the same as those for three-state shown on the left. The test circuit is Output  $R_L = 1k\Omega$  to  $V_{CC}$ ,  $C_L = 50pF$ .

FIGURE 23. HC AND HCT THREE-STATE PROPAGATION DELAY TEST CIRCUIT

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD54HC4351F3A	ACTIVE	CDIP	J	20	1	TBD	A42	N / A for Pkg Type	-55 to 125	CD54HC4351F3A	<a href="#">Samples</a>
CD74HC4351E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4351E	<a href="#">Samples</a>
CD74HC4351EE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4351E	<a href="#">Samples</a>
CD74HC4351M	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4351M	<a href="#">Samples</a>
CD74HC4351M96	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4351M	<a href="#">Samples</a>
CD74HC4352E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4352E	<a href="#">Samples</a>
CD74HCT4351E	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4351E	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF CD54HC4351, CD74HC4351 :**

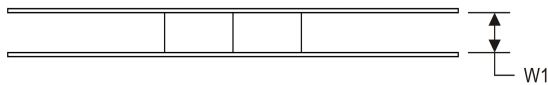
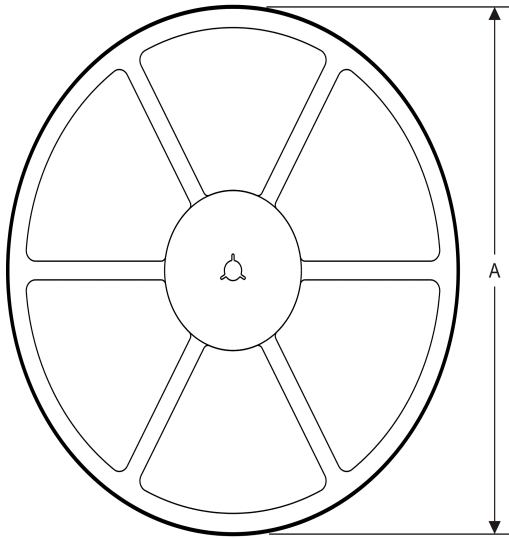
- Catalog: [CD74HC4351](#)
- Military: [CD54HC4351](#)

NOTE: Qualified Version Definitions:

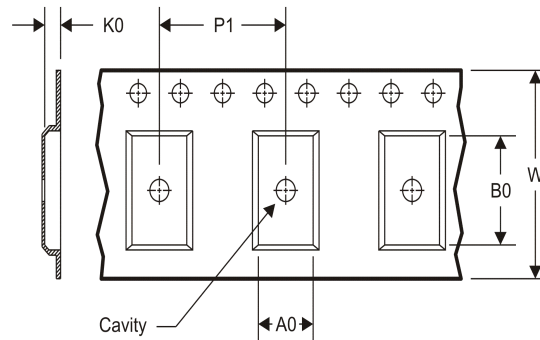
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4351M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4351M96	SOIC	DW	20	2000	367.0	367.0	45.0

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View CD74HC4351M96](#) on WIN SOURCE

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management