



**THE DATASHEET OF
74CBTLV3257BQ,115**



74CBTLV3257

Quad 1-of-2 multiplexer/demultiplexer

Rev. 7 — 9 April 2019

Product data sheet

1. General description

The 74CBTLV3257 provides a quad 1-of-2 high-speed multiplexer/demultiplexer with common select (S) and output enable (\overline{OE}) inputs. The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. When pin \overline{OE} = LOW, one of the two switches is selected (low-impedance ON-state) with pin S. When pin \overline{OE} = HIGH, all switches are in the high-impedance OFF-state, independent of pin S.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

To ensure the high-impedance OFF-state during power-up or power-down, \overline{OE} should be tied to the V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V
 - CDM AEC-Q100-011 revision B exceeds 1000 V
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLV3257D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74CBTLV3257DS	-40 °C to +125 °C	SSOP16 [1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
74CBTLV3257PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74CBTLV3257BQ	-40 °C to +125 °C	DHVQFN16	plastic dual-in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm	SOT763-1
74CBTLV3257GU	-40 °C to +125 °C	XQFN16	plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm	SOT1161-1

[1] Also known as QSOP16.

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74CBTLV3257D	74CBTLV3257D
74CBTLV3257DS	TLV3257
74CBTLV3257PW	TLV3257
74CBTLV3257BQ	TV3257
74CBTLV3257GU	b57

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

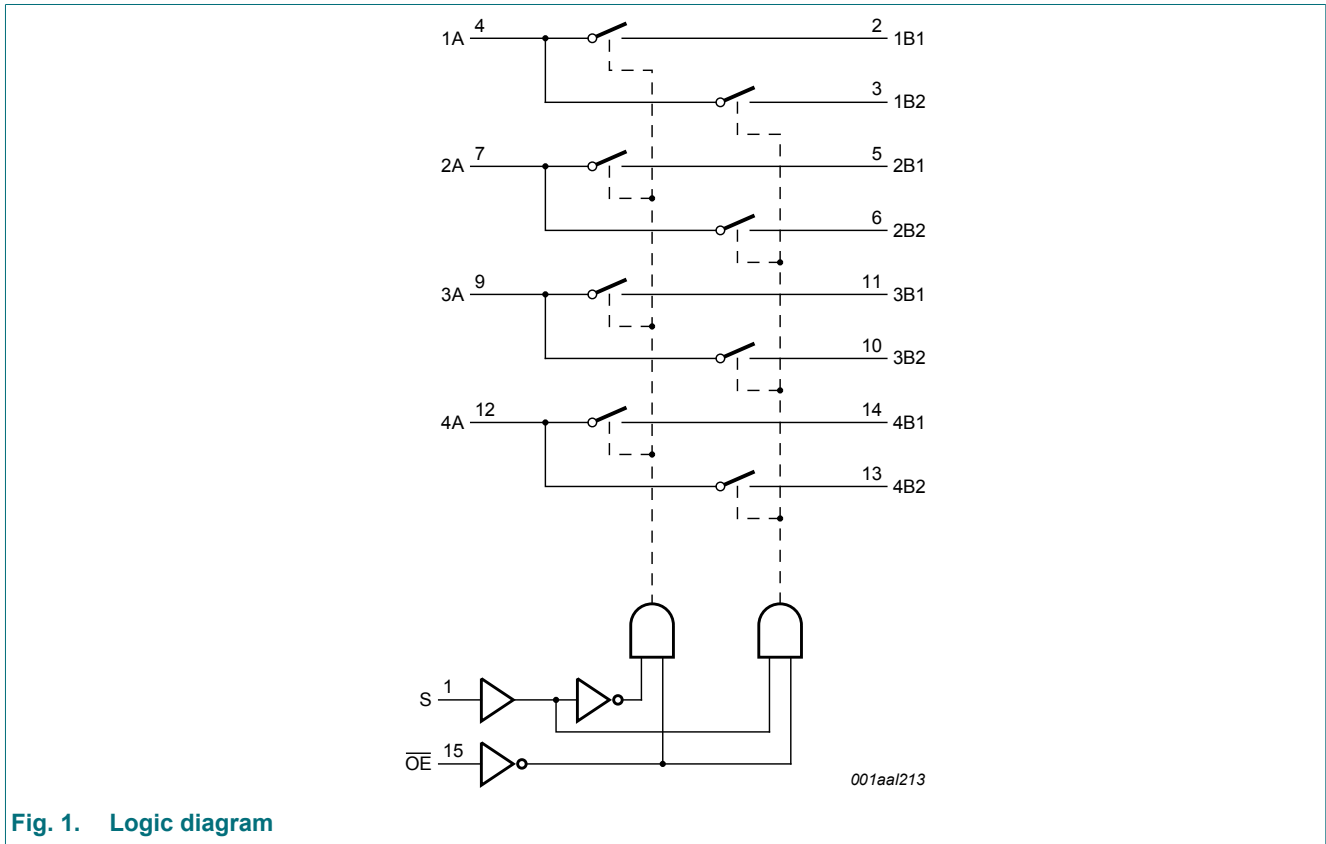


Fig. 1. Logic diagram

6. Pinning information

6.1. Pinning

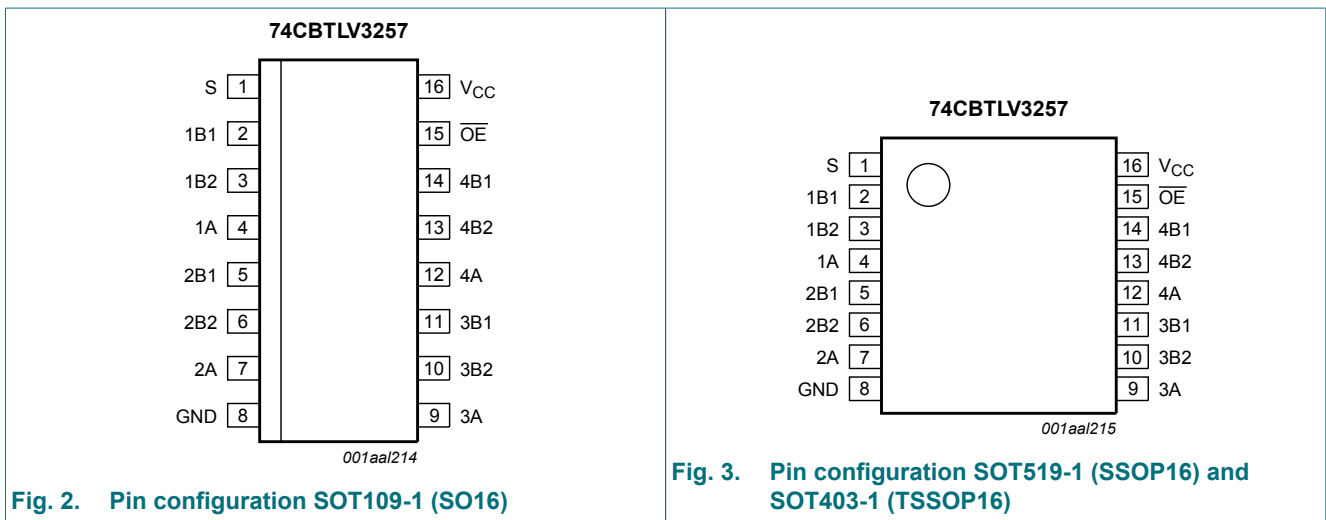


Fig. 2. Pin configuration SOT109-1 (SO16)

Fig. 3. Pin configuration SOT519-1 (SSOP16) and SOT403-1 (TSSOP16)

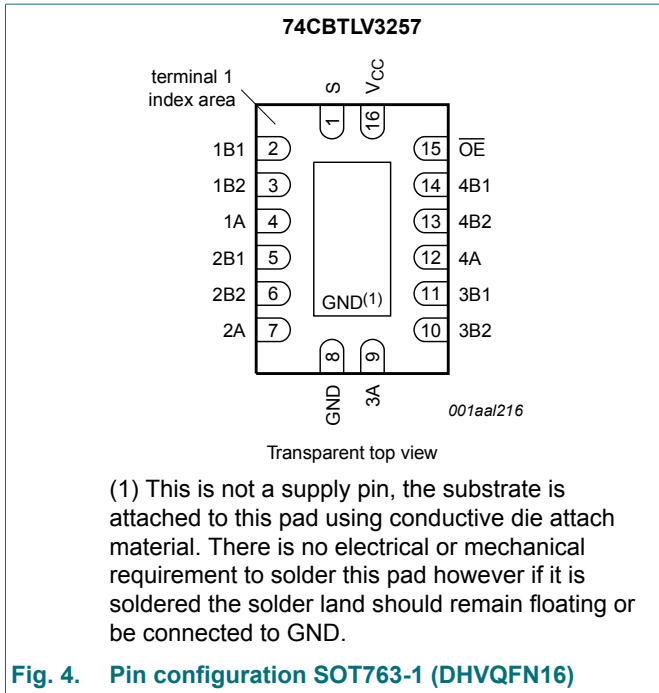


Fig. 4. Pin configuration SOT763-1 (DHVQFN16)

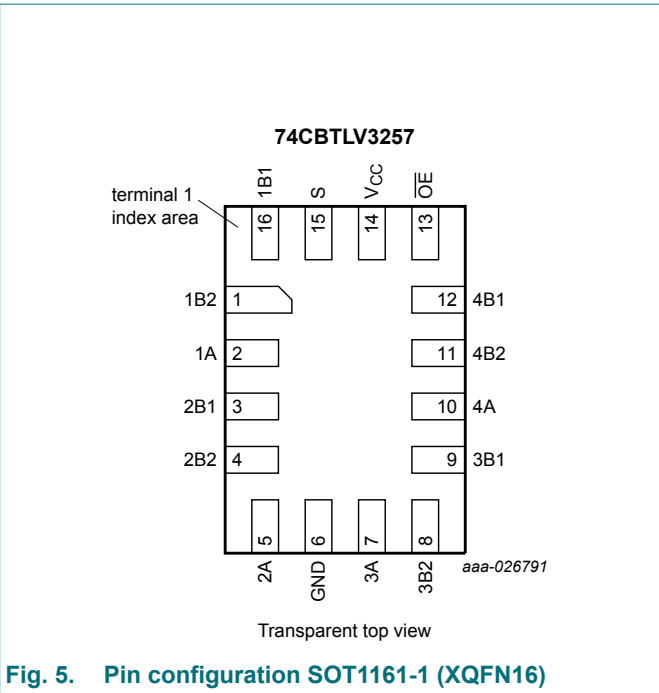


Fig. 5. Pin configuration SOT1161-1 (XQFN16)

6.2. Pin description

Table 3. Pin description

Symbol	Pin		Description
	SO16, (T)SSOP16 and DHVQFN16	XQFN16	
S	1	15	select input
1B1 to 4B1	2, 5, 11, 14	16, 3, 9, 12	B1 input/output
1B2 to 4B2	3, 6, 10, 13	1, 4, 8, 11	B2 input/output
1A to 4A	4, 7, 9, 12	2, 5, 7, 10	A input/output
GND	8	6	ground (0 V)
OE	15	13	output enable input (active LOW)
VCC	16	14	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care

Inputs		Function switch
OE	S	
L	L	nA = nB1
L	H	nA = nB2
H	X	disconnect nA and nBn

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	control inputs [1]	-0.5	+4.6	V
V_{SW}	switch voltage	enable and disable mode [2]	-0.5	$V_{CC} + 0.5$	V
I_{IK}	input clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5$ V	-50	-	mA
I_{SW}	switch current	$V_{SW} = 0$ V to V_{CC}	-	± 128	mA
I_{CC}	supply current		-	+100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C			
		SO16, (T)SSOP16 and DHVQFN16 packages [3]	-	500	mW
		XQFN16 package	-	250	mW

[1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.

[2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed

[3] For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

For DHVQFN16 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		2.3	3.6	V
V_I	input voltage		0	3.6	V
V_{SW}	switch voltage	enable and disable mode	0	V_{CC}	V
T_{amb}	ambient temperature		-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.3$ V to 3.6 V [1]	0	200	ns/V

[1] Applies to control signal levels.

10. Static characteristics

Table 7. Static characteristics

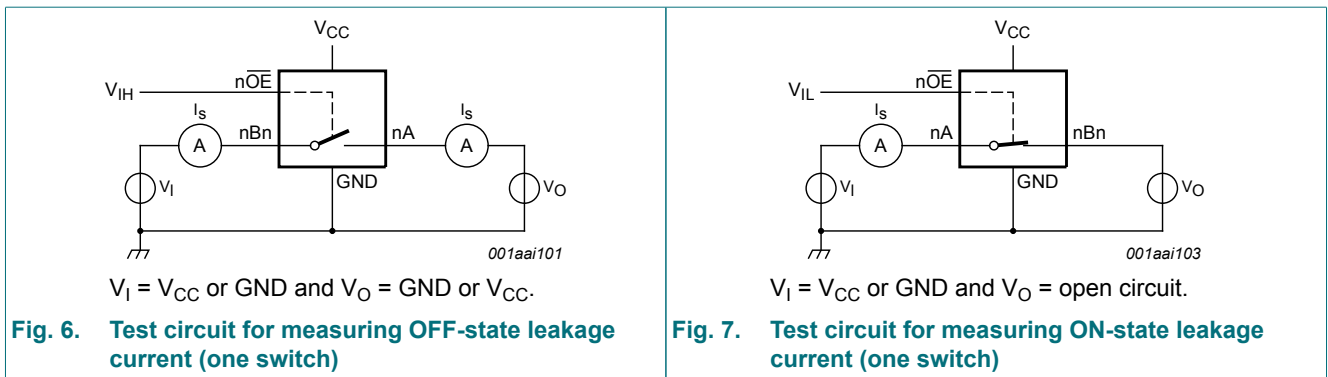
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I _I	input leakage current	pin $\overline{\text{OE}}$, S; V _{CC} = 3.6 V; V _I = GND to V _{CC}	-	-	±1	-	±20	µA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 3.6 V; see Fig. 6	-	-	±1	-	±20	µA
I _{S(ON)}	ON-state leakage current	V _{CC} = 3.6 V; see Fig. 7	-	-	±1	-	±20	µA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±10	-	±50	µA
I _{CC}	supply current	V _I = GND or V _{CC} ; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V; I _O = 0 A	-	-	10	-	50	µA
ΔI _{CC}	additional supply current	pin $\overline{\text{OE}}$, S; V _{CC} = 3.6 V; V _I = V _{CC} - 0.6 V; V _{SW} = GND or V _{CC}	[2]	-	300	-	2000	µA
C _I	input capacitance	pin $\overline{\text{OE}}$, S; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	0.9	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	5.2	-	-	-	pF
C _{S(ON)}	ON-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	14.3	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] One input at 3 V, other inputs at V_{CC} or GND.

10.1. Test circuits



10.2. ON resistance

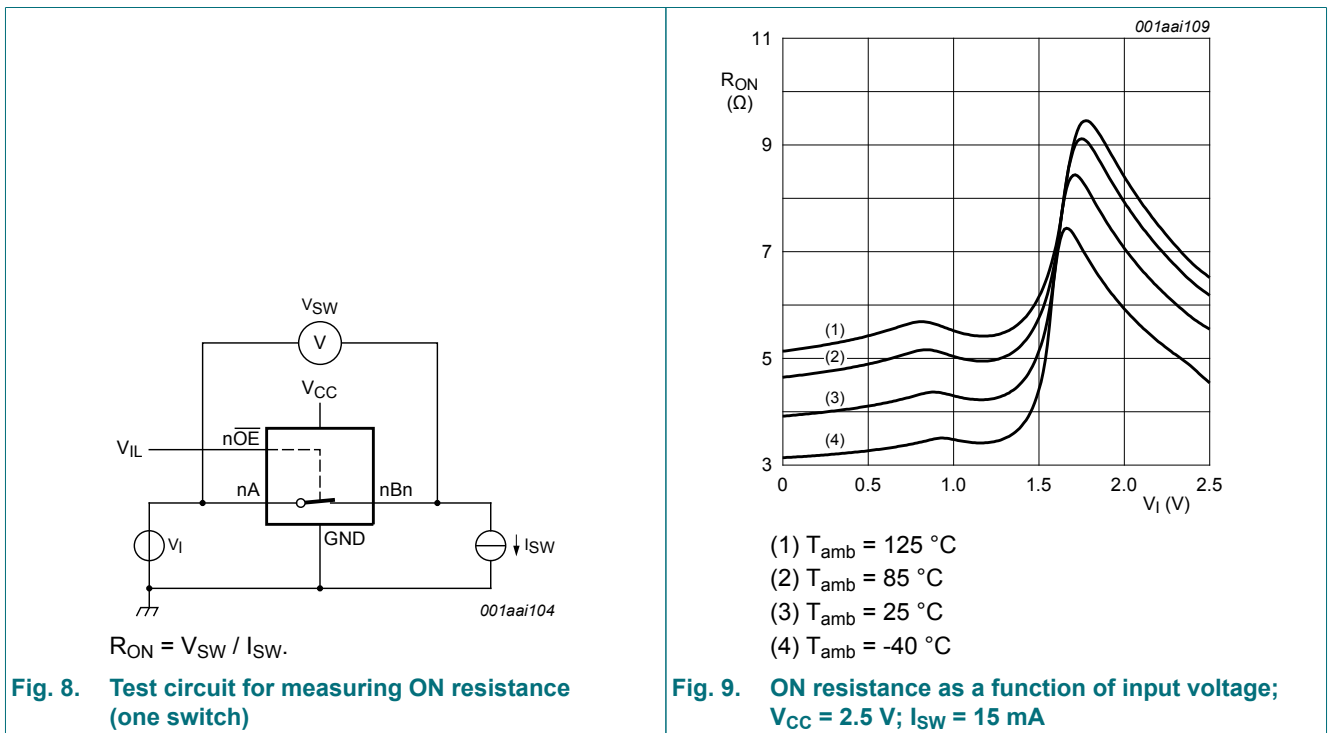
Table 8. Resistance R_{ON}

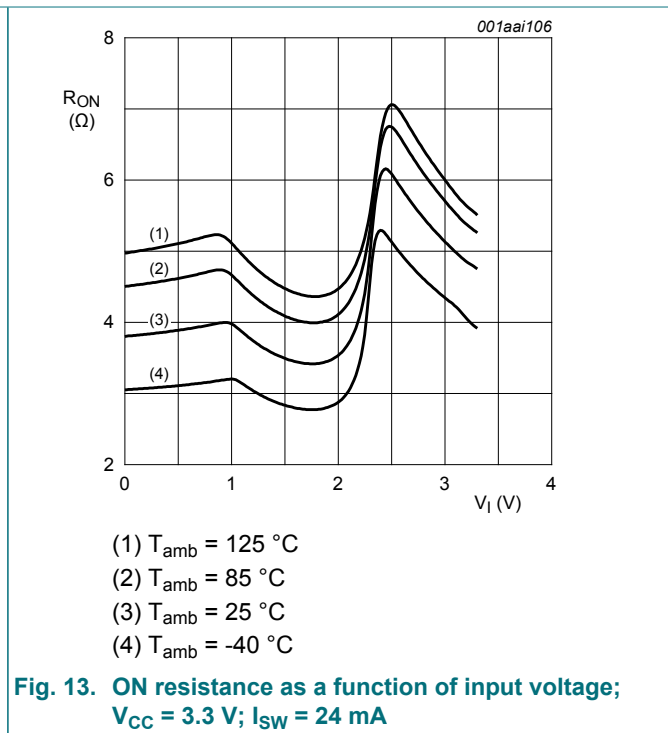
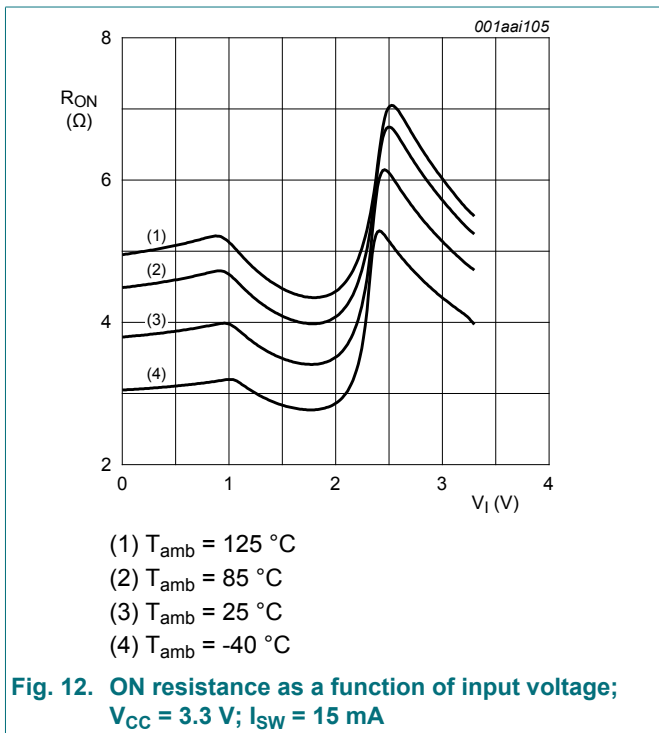
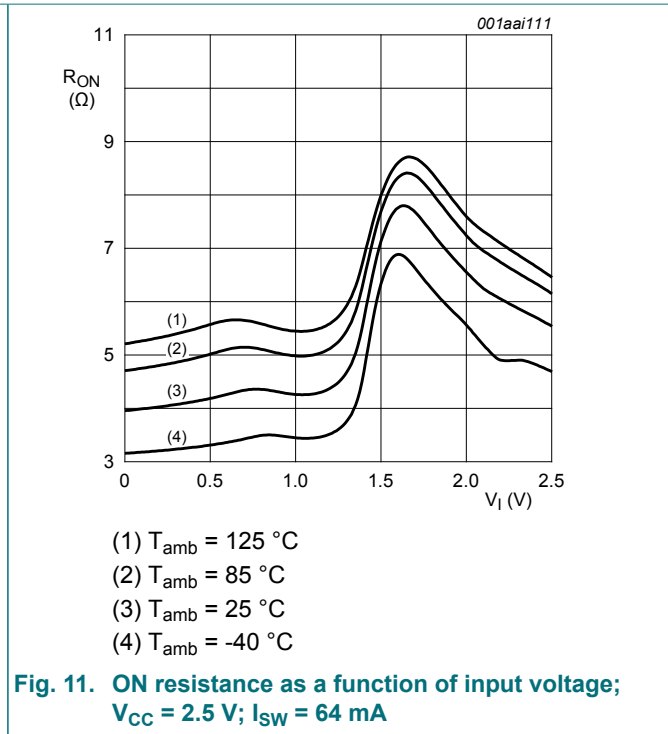
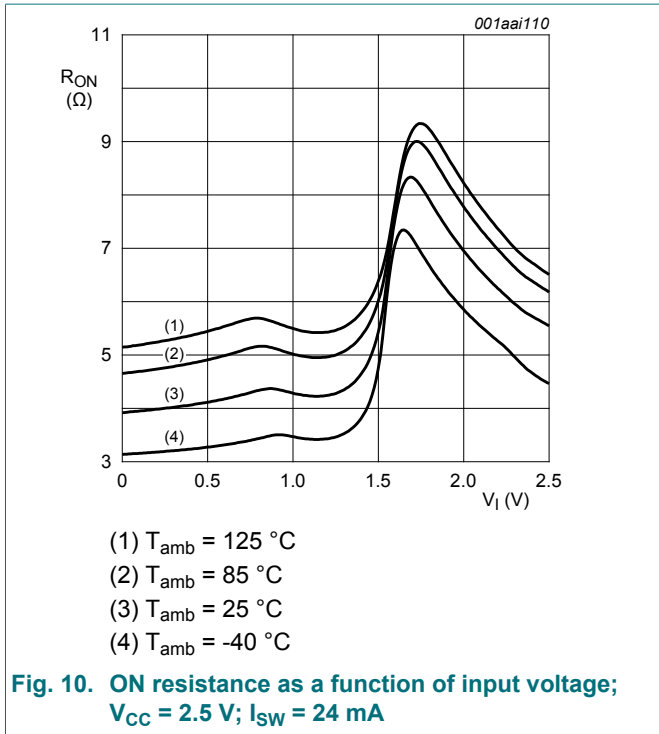
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 8.

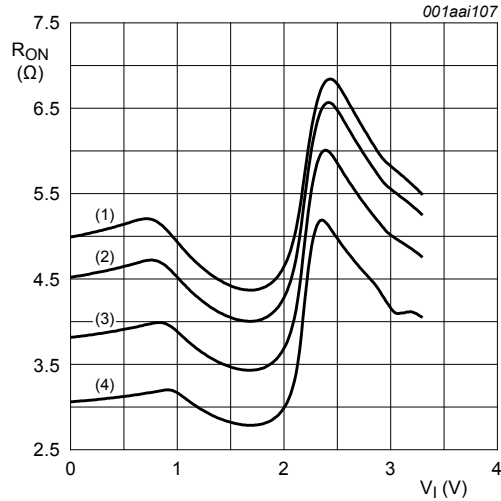
Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$			$T_{amb} = -40\text{ }^{\circ}\text{C to }+125\text{ }^{\circ}\text{C}$		Unit
			Min	Typ[1]	Max	Min	Max	
R_{ON}	ON resistance	$V_{CC} = 2.3\text{ V to }2.7\text{ V};$ see Fig. 9 to Fig. 11 [2]						
		$I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$	-	4.2	8.0	-	15.0	Ω
		$I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$	-	4.2	8.0	-	15.0	Ω
		$I_{SW} = 15\text{ mA}; V_I = 1.7\text{ V}$	-	8.4	40.0	-	60.0	Ω
		$V_{CC} = 3.0\text{ V to }3.6\text{ V};$ see Fig. 12 to Fig. 14						
		$I_{SW} = 64\text{ mA}; V_I = 0\text{ V}$	-	4.0	7.0	-	11.0	Ω
		$I_{SW} = 24\text{ mA}; V_I = 0\text{ V}$	-	4.0	7.0	-	11.0	Ω
$I_{SW} = 15\text{ mA}; V_I = 2.4\text{ V}$	-	6.2	15.0	-	25.5	Ω		

- [1] Typical values are measured at $T_{amb} = 25\text{ }^{\circ}\text{C}$ and nominal V_{CC} .
- [2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

10.3. ON resistance test circuit and graphs







- (1) $T_{amb} = 125\text{ °C}$
- (2) $T_{amb} = 85\text{ °C}$
- (3) $T_{amb} = 25\text{ °C}$
- (4) $T_{amb} = -40\text{ °C}$

Fig. 14. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$; $I_{SW} = 64\text{ mA}$

11. Dynamic characteristics

Table 9. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit see Fig. 17

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ °C to }+85\text{ °C}$			$T_{amb} = -40\text{ °C to }+125\text{ °C}$		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nBn or nBn to nA; see Fig. 15 [2] [3]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.15	-	0.25	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	-	-	0.15	-	0.25	ns
		S to nA; see Fig. 15 [3]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.8	6.1	1.0	6.7	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.2	5.3	1.0	5.8	ns
t_{en}	enable time	\overline{OE} to nA or nBn; see Fig. 16 [4]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	2.2	5.6	1.0	6.2	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	2.0	5.0	1.0	5.5	ns
		S to nBn; see Fig. 16 [4]						
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.0	3.5	6.1	1.0	6.7	ns
		$V_{CC} = 3.0\text{ V to }3.6\text{ V}$	1.0	3.0	5.3	1.0	5.8	ns

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t _{dis}	disable time	OĒ to nA or nBn; see Fig. 16 [5]						
		V _{CC} = 2.3 V to 2.7 V	1.0	2.6	5.5	1.0	6.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.1	5.5	1.0	6.1	ns
		S to nBn; see Fig. 16 [5]						
		V _{CC} = 2.3 V to 2.7 V	1.0	2.6	4.8	1.0	5.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.2	4.5	1.0	5.0	ns

- [1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.
- [2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
- [3] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [4] t_{en} is the same as t_{PZH} and t_{PZL}.
- [5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

11.1. Waveforms and test circuit

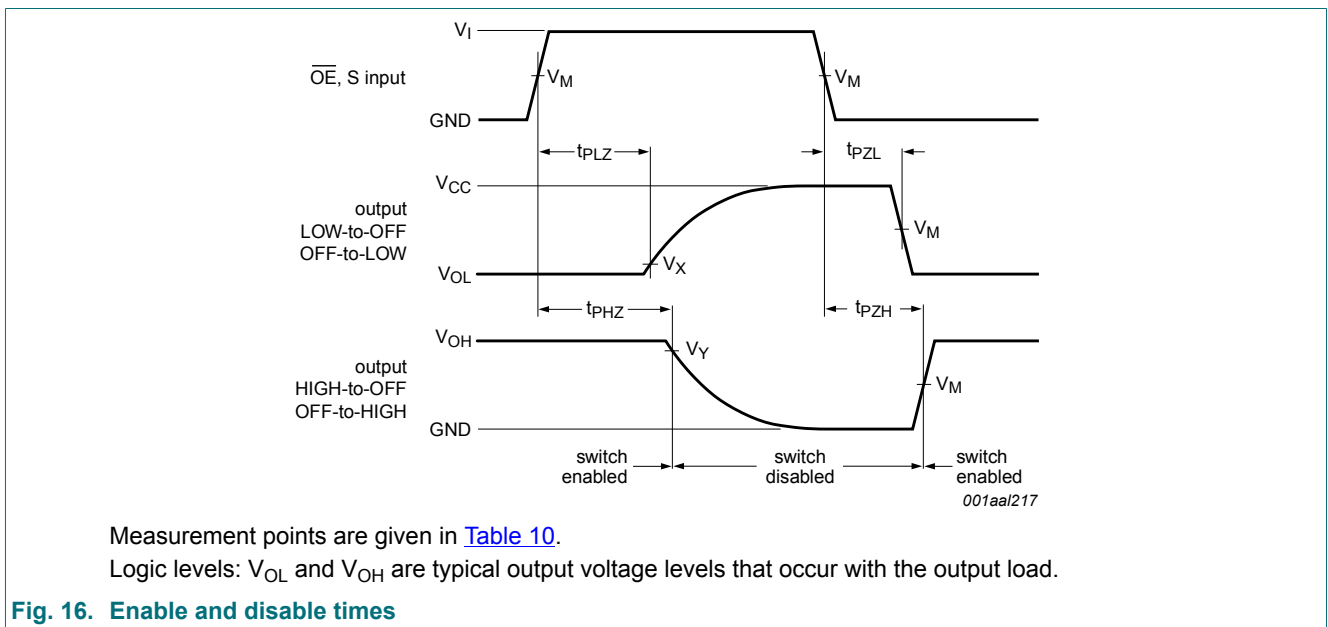
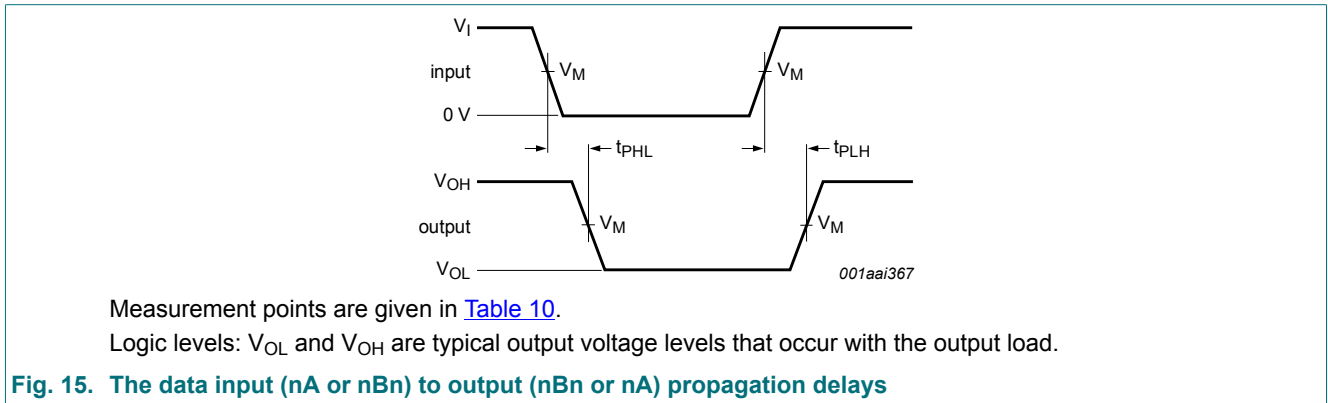
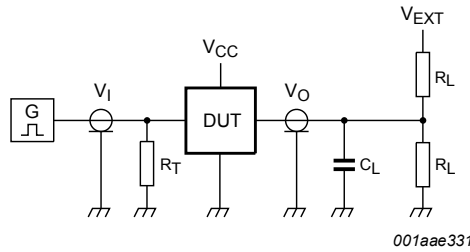
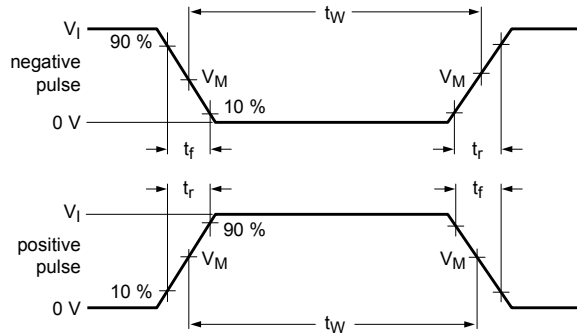


Table 10. Measurement points

Supply voltage	Input			Output		
V _{CC}	V _M	V _I	t _r = t _f	V _M	V _X	V _Y
2.3 V to 2.7 V	0.5V _{CC}	V _{CC}	≤ 2.0 ns	0.5V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
3.0 V to 3.6 V	0.5V _{CC}	V _{CC}	≤ 2.0 ns	0.5V _{CC}	V _{OL} + 0.3 V	V _{OH} - 0.3 V



Test data is given in [Table 11](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 17. Test circuit for measuring switching times

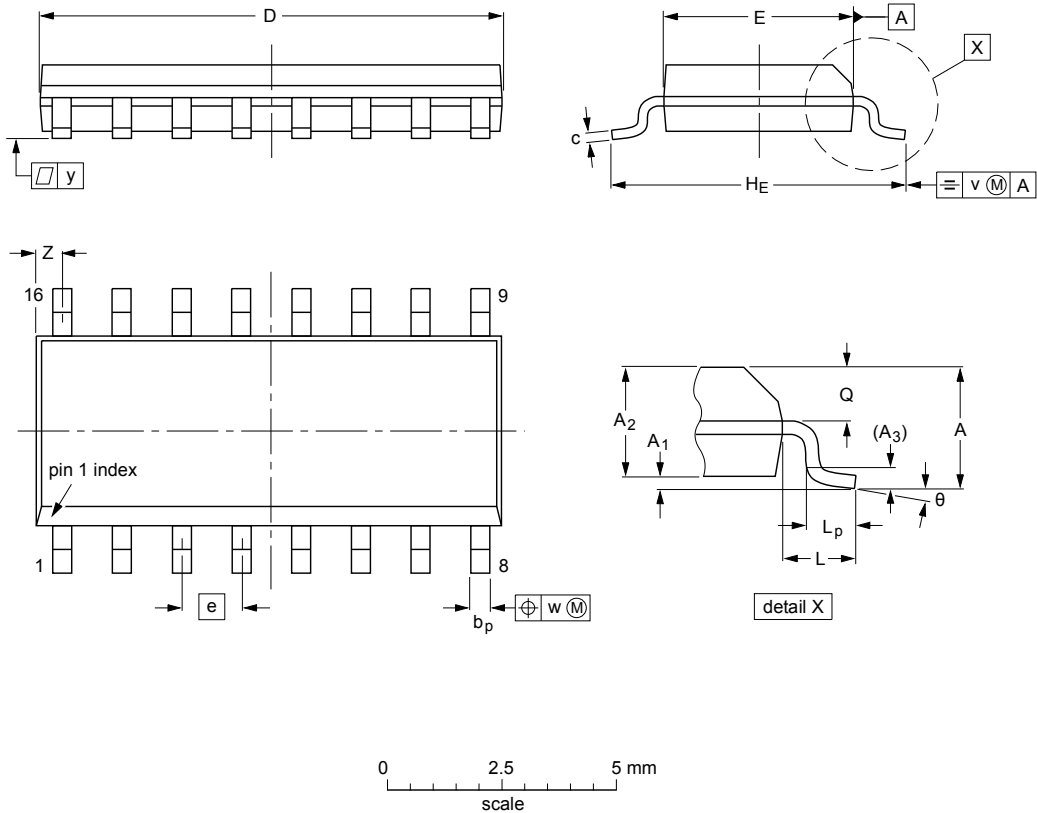
Table 11. Test data

Supply voltage	Load		V _{EXT}		
V _{CC}	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
2.3 V to 2.7 V	30 pF	500 Ω	open	GND	2V _{CC}
3.0 V to 3.6 V	50 pF	500 Ω	open	GND	2V _{CC}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

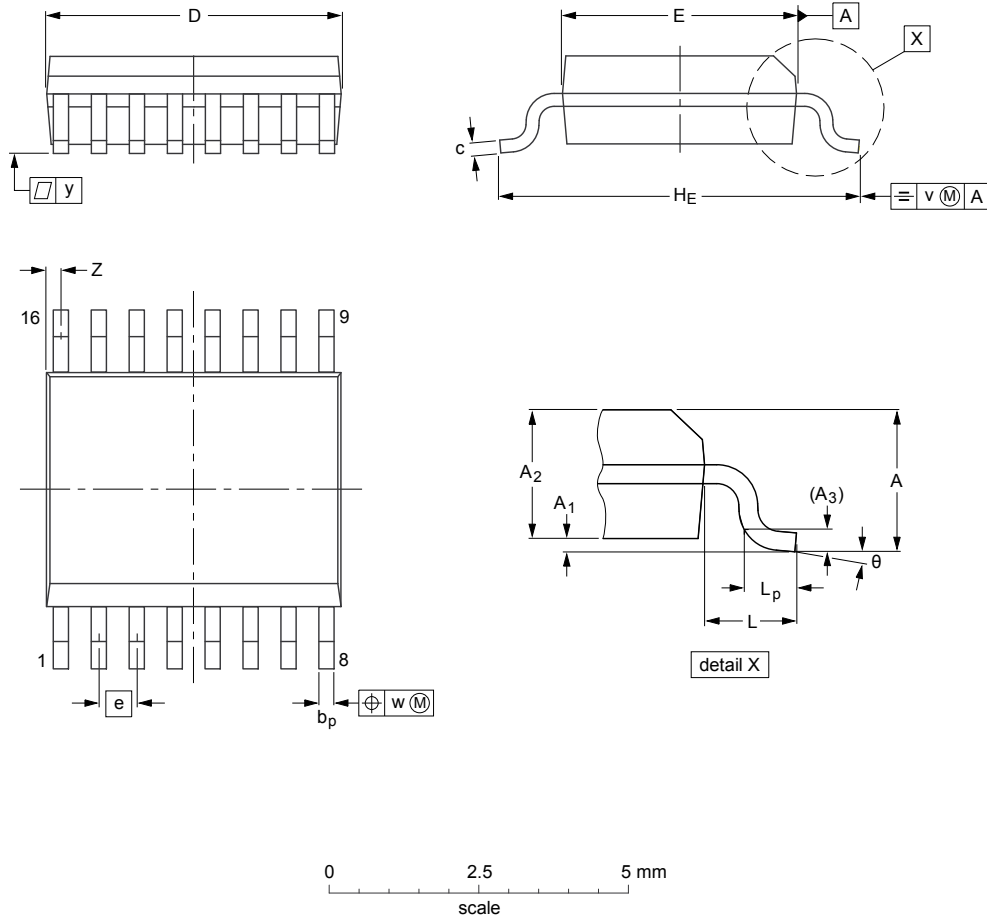
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig. 19. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	v	w	y	Z ⁽¹⁾	θ
mm	1.73	0.25 0.10	1.55 1.40	0.25	0.31 0.20	0.25 0.18	5.0 4.8	4.0 3.8	0.635	6.2 5.8	1	0.89 0.41	0.2	0.18	0.09	0.18 0.05	8° 0°

Note

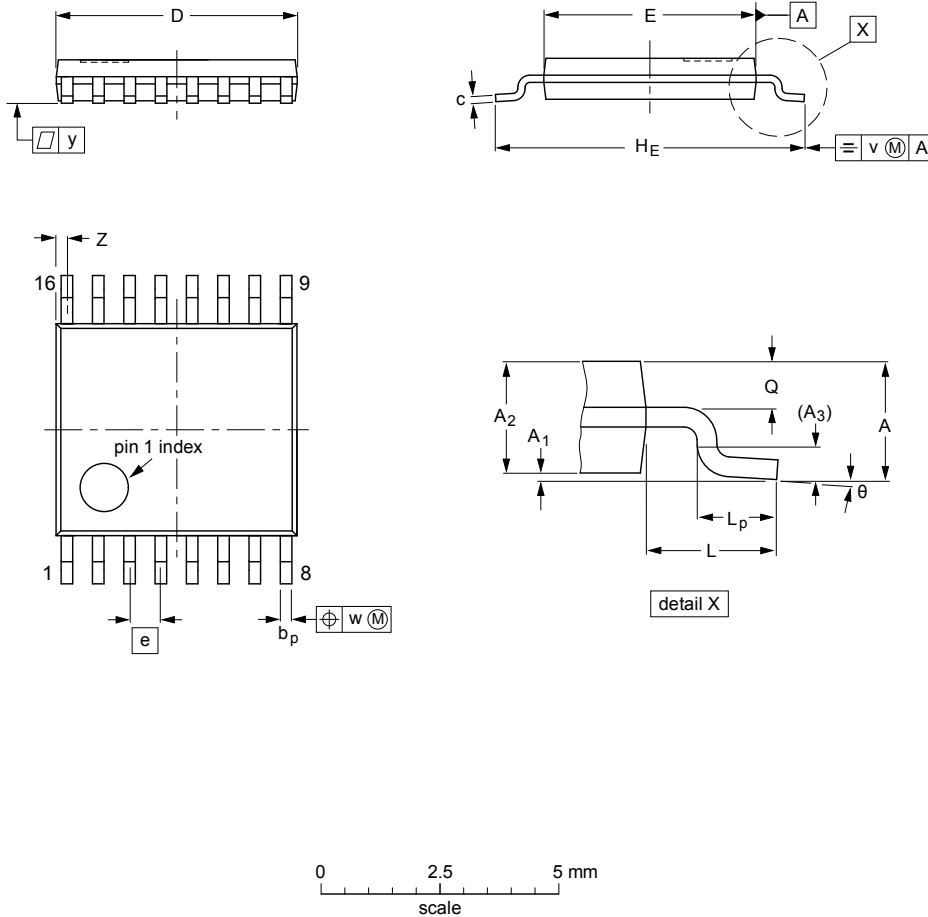
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT519-1						-99-05-04- 03-02-18

Fig. 20. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				99-12-27 03-02-18

Fig. 21. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

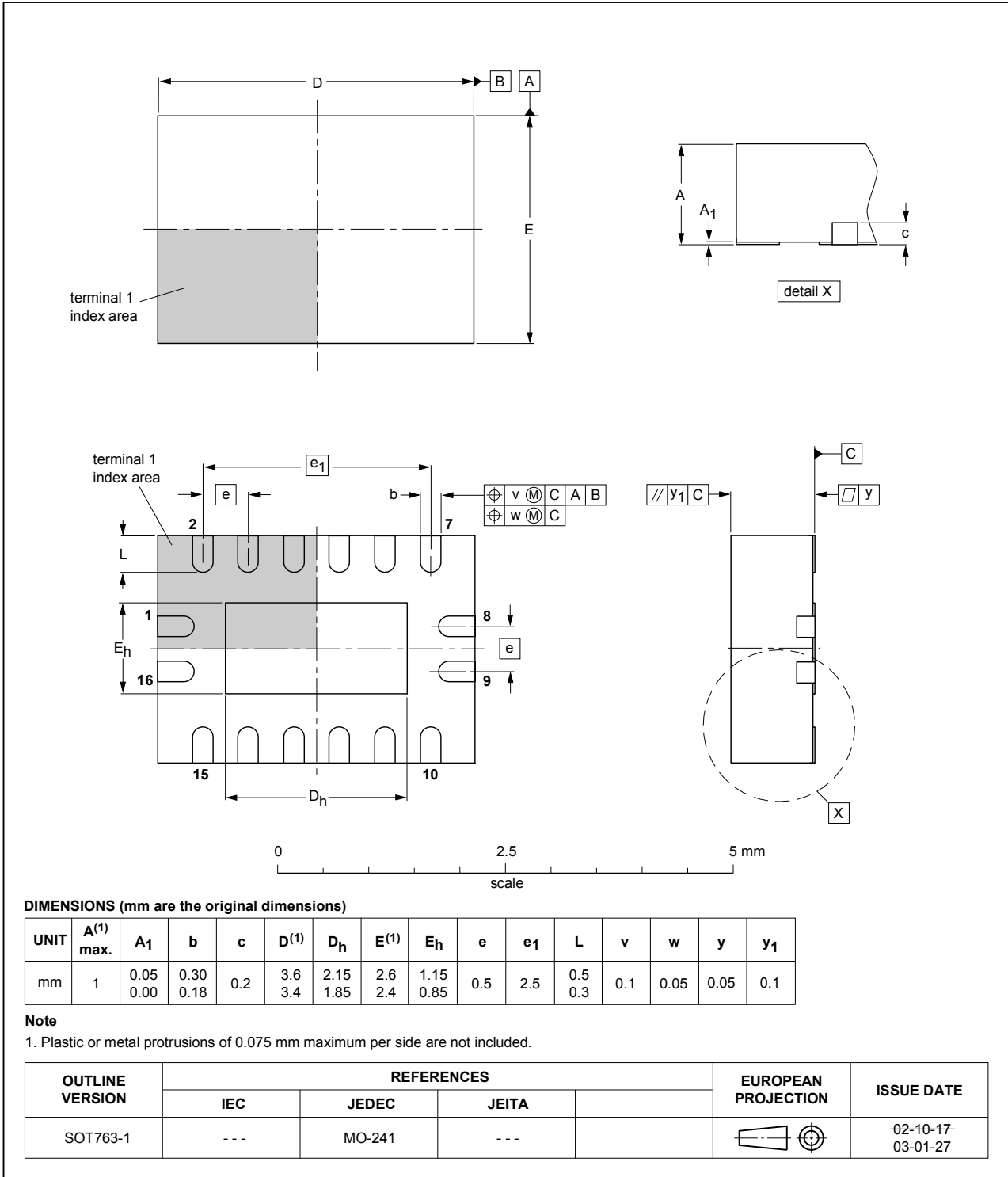
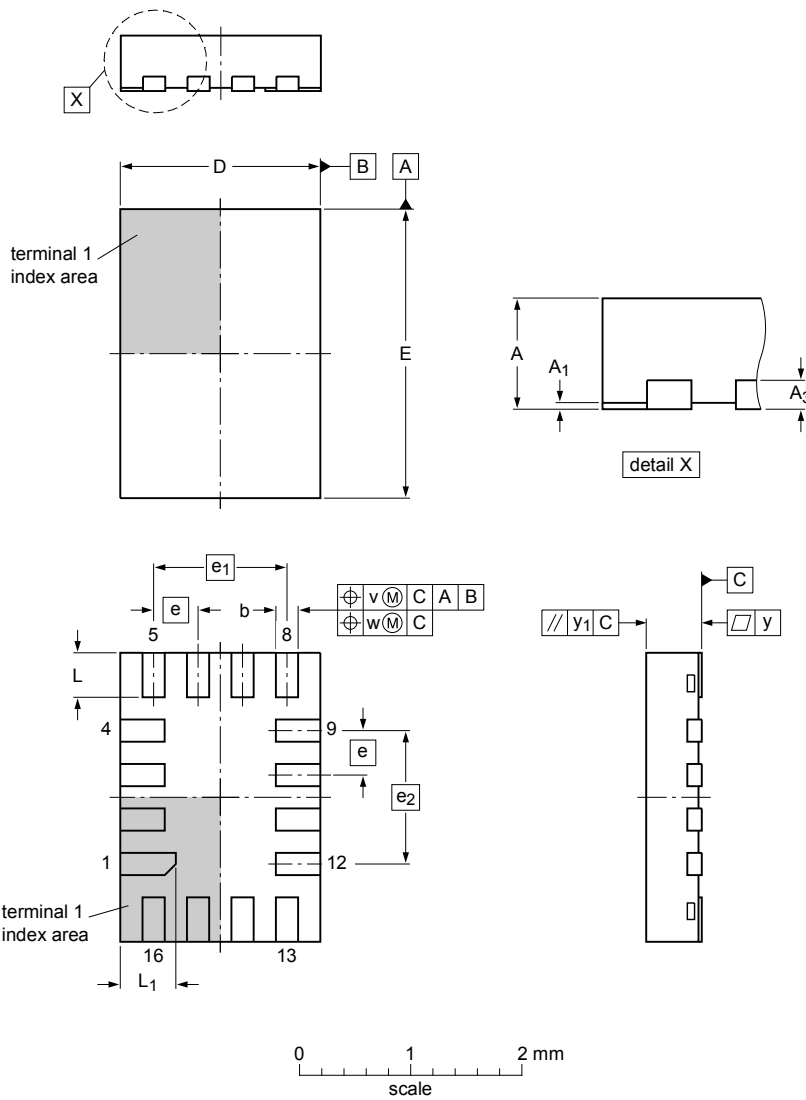


Fig. 22. Package outline SOT763-1 (DHVQFN16)

XQFN16: plastic, extremely thin quad flat package; no leads; 16 terminals; body 1.80 x 2.60 x 0.50 mm

SOT1161-1



Dimensions

Unit ⁽¹⁾	A	A ₁	A ₃	b	D	E	e	e ₁	e ₂	L	L ₁	v	w	y	y ₁
max	0.5	0.05		0.25	1.9	2.7				0.45	0.55				
mm nom			0.127	0.20	1.8	2.6	0.4	1.2	1.2	0.40	0.50	0.1	0.05	0.05	0.05
min		0.00		0.15	1.7	2.5				0.35	0.45				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot1161-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1161-1	---	---	---			09-12-28 09-12-29

Fig. 23. Package outline SOT1161-1 (XQFN16)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLV3257 v.7	20190409	Product data sheet	-	74CBTLV3257 v.6
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Link corrected in Section 11. 			
74CBTLV3257 v.6	20171211	Product data sheet	-	74CBTLV3257 v.5
Modifications:	<ul style="list-style-type: none"> Type number 74CBTLV3257GU (SOT1161-1 / XQFN16) added. 			
74CBTLV3257 v.5	20161111	Product data sheet	-	74CBTLV3257 v.4
Modifications:	<ul style="list-style-type: none"> Section 11.2 added. 			
74CBTLV3257 v.4	20111216	Product data sheet	-	74CBTLV3257 v.3
Modifications:	<ul style="list-style-type: none"> Legal pages updated. 			
74CBTLV3257 v.3	20110106	Product data sheet	-	74CBTLV3257 v.2
74CBTLV3257 v.2	20101126	Product data sheet	-	74CBTLV3257 v.1
74CBTLV3257 v.1	20100112	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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