# THE DATASHEET OF

# 74ALVT162245DL,112

# 74ALVT162245

## 16-bit transceiver with 30 Ω termination resistors; 3-state

Rev. 3 — 29 January 2018 Product data sheet

## 1 General description

The 74ALVT162245 is a high-performance BiCMOS product designed for $V_{CC}$ operation at 2.5 V or 3.3 V with I/O compatibility up to 5 V.

This device is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an output enable input ($n\overline{OE}$) for easy cascading and a direction control input (nDIR) for direction control.

The 74ALVT162245 is designed with 30 Ω series resistance in both the HIGH-state and LOW-state of the output. This design reduces line noise in applications such as memory address drivers, clock drivers and bus transceivers and transmitters.

## 2 Features and benefits

- 16-bit bidirectional bus interface
- 3-State buffers
- 5V I/O compatible
- Output capability: +12 mA/–12 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30 Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5 V bus
- Latch-up protection:
  - JESD17: exceeds 500 mA
- ESD protection:
  - MIL STD 883 method 3015: exceeds 2000 V
  - MM: exceeds 200 V

## 3 Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74ALVT162245DL | -40 °C to +85 °C | SSOP48 | plastic shrink small outline package; 48 leads; body width 7.5 mm | SOT370-1 |
| 74ALVT162245DGG | -40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |

## 4 Functional diagram

**Table 2.**

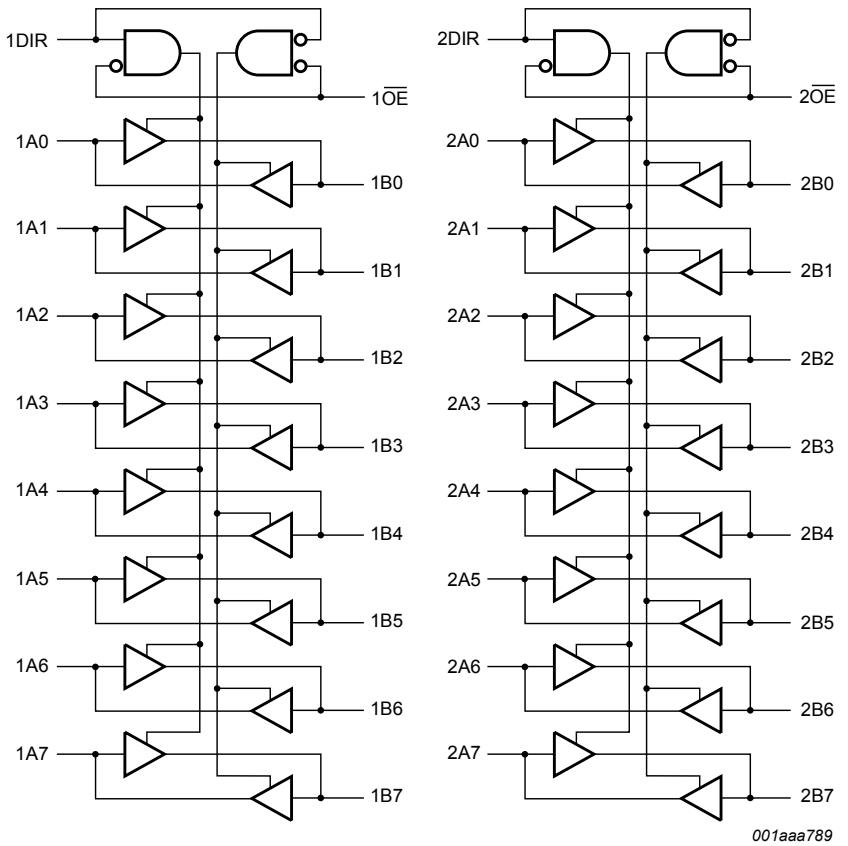



**Figure 1. Logic symbol**

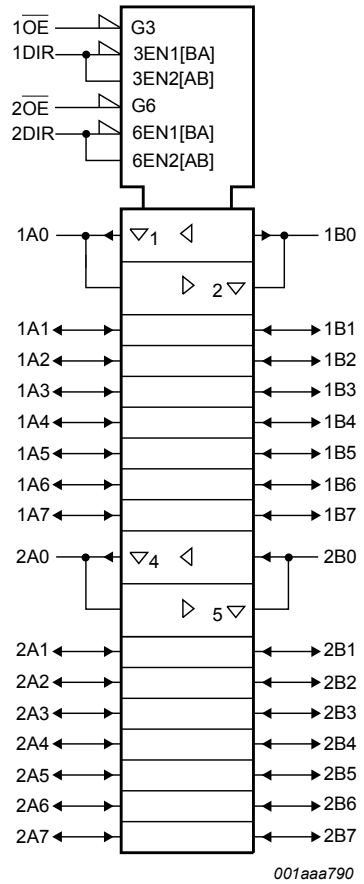



**Figure 2. IEC logic symbol**

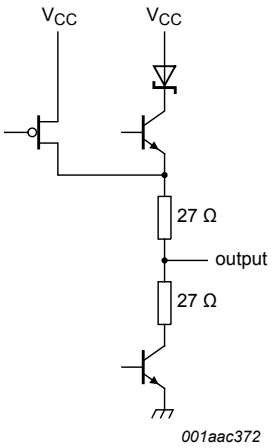



Figure 3. Schematic of each output

# 5 Pinning information

## 5.1 Pinning

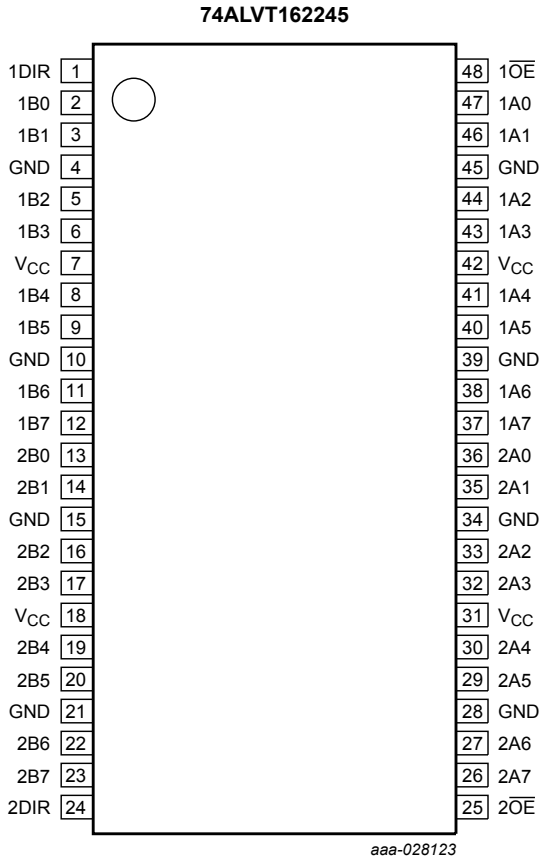



Figure 4. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)

### 5.2 Pin description

**Table 3. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| 1DIR, 2DIR | 1, 24 | direction control input |
| 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7 | 47, 46, 44, 43, 41, 40, 38, 37 | data input/output |
| 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7 | 36, 35, 33, 32, 30, 29, 27, 26 | data input/output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| 1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7 | 2, 3, 5, 6, 8, 9, 11, 12 | data input/output |
| 2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7 | 13, 14, 16, 17, 19, 20, 22, 23 | data input/output |
| $1\overline{OE}$, $2\overline{OE}$ | 48, 25 | output enable input (active-LOW) |
| $V_{CC}$ | 7, 18, 31, 42 | supply voltage |

## 6 Functional description

**Table 4. Function table**

*H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.*

| Control | | Input/output | |
|---|---|---|---|
| **$n\overline{OE}$** | **nDIR** | **nAn** | **nBn** |
| L | L | output nAn = nBn | input |
| L | H | input | output nBn = nAn |
| H | X | Z | Z |

# 7 Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | −0.5 | +4.6 | V |
| $V_I$ | input voltage | | [1] | −0.5 | +7.0 | V |
| $V_O$ | output voltage | output in OFF-state or HIGH-state | [1] | −0.5 | +7.0 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | −50 | - | mA |
| $I_{OK}$ | output clamping current | $V_O < 0$ V | | −50 | - | mA |
| $I_O$ | output current | output in LOW-state | | - | 128 | mA |
| | | output in HIGH-state | | −64 | - | mA |
| $T_{stg}$ | storage temperature | | | −65 | +150 | °C |
| $T_j$ | junction temperature | | [2] | - | +150 | °C |

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

# 8 Recommended operating conditions

**Table 6. Recommended operating conditions**

| Symbol | Parameter | Conditions | $V_{CC}$ = 2.5 V ± 0.2 V | | $V_{CC}$ = 3.3 V ± 0.3 V | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $V_{CC}$ | supply voltage | | 2.3 | 2.7 | 3.0 | 3.6 | V |
| $V_I$ | input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $I_{OH}$ | HIGH-level output current | | - | −8 | - | −12 | mA |
| $I_{OL}$ | LOW-level output current | | - | 12 | - | 12 | mA |
| $\Delta t/\Delta V$ | input transition rise and fall rate | outputs enabled | - | 10 | - | 10 | ns/V |
| $T_{amb}$ | ambient temperature | free-air | −40 | +85 | −40 | +85 | °C |

# 9 Static characteristics

**Table 7. Static characteristics**

*At recommended operating conditions; $T_{amb}$ = -40 °C to +85 °C; voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| **$V_{CC}$ = 2.5 V ± 0.2 V** | | | | | | |
| $V_{IK}$ | input clamping voltage | $V_{CC}$ = 2.3 V; $I_{IK}$ = -18 mA | - | -0.85 | -1.2 | V |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 2.5 V ± 0.2 V | 1.7 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 2.5 V ± 0.2 V | - | - | 0.7 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_{CC}$ = 2.3 V; $I_O$ = -8 mA | 1.7 | - | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_{CC}$ = 2.3 V; $I_O$ = 12 mA | - | 0.6 | 0.7 | V |
| $I_I$ | input leakage current | all input pins [2] | | | | |
| | | $V_{CC}$ = 0 V or 2.7 V; $V_I$ = 5.5 V | - | 0.1 | 10 | µA |
| | | control pins | | | | |
| | | $V_{CC}$ = 2.7 V; $V_I$ = $V_{CC}$ or GND | - | 0.1 | ±1 | µA |
| | | I/O data pins [2] | | | | |
| | | $V_{CC}$ = 2.7 V; $V_I$ = $V_{CC}$ | - | 0.1 | 1 | µA |
| | | $V_{CC}$ = 2.7 V; $V_I$ = 0 V | - | 0.1 | -5 | µA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 0 V to 4.5 V | - | 0.1 | ±100 | µA |
| $I_{BHL}$ | bus hold LOW current | data inputs; $V_{CC}$ = 2.3 V; $V_I$ = 0.7 V [3] | - | 90 | - | µA |
| $I_{BHH}$ | bus hold HIGH current | data inputs; $V_{CC}$ = 2.3 V; $V_I$ = 1.7 V [3] | - | -75 | - | µA |
| $I_{EX}$ | external current | output in HIGH-state when $V_O$ > $V_{CC}$; $V_O$ = 5.5 V; $V_{CC}$ = 2.3 V | - | 20 | 125 | µA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC}$ ≤ 1.2 V; $V_O$ = 0.5 V to $V_{CC}$; $V_I$ = GND or $V_{CC}$; $n\overline{OE}$ = don't care [4] | - | 40 | 100 | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 2.7 V; $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A | | | | |
| | | outputs HIGH | - | 0.04 | 0.1 | mA |
| | | outputs LOW | - | 2.5 | 4.5 | mA |
| | | outputs disabled [5] | - | 0.04 | 0.1 | mA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 2.3 V to 2.7 V; one input at $V_{CC}$ - 0.6 V; other inputs at $V_{CC}$ or GND [6] | - | 0.05 | 0.4 | mA |
| $C_I$ | input capacitance | nDIR and $n\overline{OE}$; $V_I$ = 0 V or $V_{CC}$ | - | 3 | - | pF |
| $C_{I/O}$ | input/output capacitance | $V_{I/O}$ = 0 V or $V_{CC}$ | - | 9 | - | pF |

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| **$V_{CC}$ = 3.3 V ± 0.3 V** | | | | | | |
| $V_{IK}$ | input clamping voltage | $V_{CC}$ = 3.0 V; $I_{IK}$ = -18 mA | - | -0.85 | -1.2 | V |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 3.3 V ± 0.3 V | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 3.3 V ± 0.3 V | - | - | 0.8 | V |
| $V_{OH}$ | HIGH-level output voltage | $V_{CC}$ = 3.0 V; $I_O$ = -12 mA | 2.0 | 2.3 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_{CC}$ = 3.0 V; $I_O$ = 12 mA | - | 0.6 | 0.8 | V |
| $I_I$ | input leakage current | all input pins [2] | | | | |
| | | $V_{CC}$ = 0 V or 3.6 V; $V_I$ = 5.5 V | - | 0.1 | 10 | µA |
| | | control pins | | | | |
| | | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ or GND | - | 0.1 | ±1 | µA |
| | | I/O data pins [2] | | | | |
| | | $V_{CC}$ = 3.6 V; $V_I$ = $V_{CC}$ | - | 0.5 | 1 | µA |
| | | $V_{CC}$ = 3.6 V; $V_I$ = 0 V | - | 0.1 | -5 | µA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ = 0 V to 4.5 V | - | 0.1 | ±100 | µA |
| $I_{BHL}$ | bus hold LOW current | data inputs; $V_{CC}$ = 3 V; $V_I$ = 0.8 V | 75 | 130 | - | µA |
| $I_{BHH}$ | bus hold HIGH current | data inputs; $V_{CC}$ = 3 V; $V_I$ = 2.0 V | -75 | -140 | - | µA |
| $I_{BHLO}$ | bus hold LOW overdrive current | data inputs; $V_{CC}$ = 3.6 V; $V_I$ = 0 V to 3.6 V [7] | 500 | - | - | µA |
| $I_{BHHO}$ | bus hold HIGH overdrive current | data inputs; $V_{CC}$ = 3.6 V; $V_I$ = 0 V to 3.6 V [7] | -500 | - | - | µA |
| $I_{EX}$ | external current | output in HIGH-state when $V_O > V_{CC}$; $V_O$ = 5.5 V; $V_{CC}$ = 3.0 V | - | 50 | 125 | µA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} \leq$ 1.2 V; $V_O$ = 0.5 V to $V_{CC}$; $V_I$ = GND or $V_{CC}$; n$\overline{OE}$ = don't care [8] | - | 40 | ±100 | µA |
| $I_{CC}$ | supply current | $V_{CC}$ = 3.6 V; $V_I$ = GND or $V_{CC}$; $I_O$ = 0 A | | | | |
| | | outputs HIGH | - | 0.07 | 0.1 | mA |
| | | outputs LOW | - | 3.5 | 5 | mA |
| | | outputs disabled [5] | - | 0.07 | 0.1 | mA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 3 V to 3.6 V; one input at $V_{CC}$ - 0.6 V; other inputs at $V_{CC}$ or GND [6] | - | 0.04 | 0.4 | mA |
| $C_I$ | input capacitance | nDIR and n$\overline{OE}$; $V_I$ = 0 V or $V_{CC}$ | - | 3 | - | pF |
| $C_{I/O}$ | input/output capacitance | $V_{I/O}$ = 0 V or $V_{CC}$ | - | 9 | - | pF |

[1] Typical values for $V_{CC}$ = 2.3 V to 2.7 V are measured at $V_{CC}$ = 2.5 V and $T_{amb}$ = 25 °C.
Typical values for $V_{CC}$ = 3.0 V to 3.6 V are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.
[2] Unused pins at $V_{CC}$ or GND.
[3] Not guaranteed.
[4] This parameter is valid for any $V_{CC}$ between 0 V and 1.2 V with a transition time of up to 10 ms.
From $V_{CC}$ = 1.2 V to $V_{CC}$ = 2.5 V ± 0.2 V a transition time of 100 µs is permitted. This parameter is valid for $T_{amb}$ = 25 °C only.
[5] $I_{CC}$ with outputs disabled is measured with outputs pulled to $V_{CC}$ or GND.
[6] This is the increase in supply current for each input at the specified voltage level other than $V_{CC}$ or GND.
[7] This is the bus hold overdrive current required to force the input to the opposite logic state.
[8] This parameter is valid for any $V_{CC}$ between 0 V and 1.2 V with a transition time of up to 10 ms.
From $V_{CC}$ = 1.2 V to $V_{CC}$ = 3.0 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for $T_{amb}$ = 25 °C only.

# 10 Dynamic characteristics

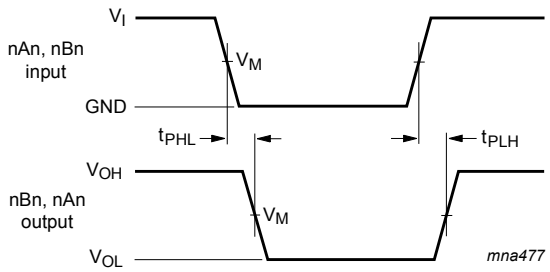
**Table 8. Dynamic characteristics**

*Voltages are referenced to GND (ground = 0 V); $T_{amb}$ = -40 °C to +85 °C; for test circuit see Figure 7.*

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---|---|---|---|---|---|---|
| **$V_{CC}$ = 2.5 V ± 0.2 V** | | | | | | |
| $t_{PLH}$ | LOW to HIGH propagation delay | nAn to nBn or nBn to nAn; see Figure 5 | 1.5 | 2.9 | 5.3 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | nAn to nBn or nBn to nAn; see Figure 5 | 1.5 | 2.4 | 4.7 | ns |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | n$\overline{OE}$ to nAn or n$\overline{OE}$ to nBn; see Figure 6 | 1.5 | 4.3 | 6.3 | ns |
| $t_{PZL}$ | OFF-state to LOW propagation delay | n$\overline{OE}$ to nAn or n$\overline{OE}$ to nBn; see Figure 6 | 1.5 | 3.1 | 4.6 | ns |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | n$\overline{OE}$ to nAn or n$\overline{OE}$ to nBn; see Figure 6 | 1.5 | 4.2 | 6.2 | ns |
| $t_{PLZ}$ | LOW to OFF-state propagation delay | n$\overline{OE}$ to nAn or n$\overline{OE}$ to nBn; see Figure 6 | 1.5 | 3.3 | 5.1 | ns |
| **$V_{CC}$ = 3.3 V ± 0.3 V** | | | | | | |
| $t_{PLH}$ | LOW to HIGH propagation delay | nAn to nBn or nBn to nAn; see Figure 5 | 0.5 | 2.3 | 3.6 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | nAn to nBn or nBn to nAn; see Figure 5 | 0.5 | 2.0 | 3.1 | ns |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | n$\overline{OE}$ to nAn or n$\overline{OE}$ to nBn; see Figure 6 | 1.0 | 3.0 | 5.0 | ns |
| $t_{PZL}$ | OFF-state to LOW propagation delay | n$\overline{OE}$ to nAn or n$\overline{OE}$ to nBn; see Figure 6 | 1.0 | 2.6 | 3.9 | ns |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | n$\overline{OE}$ to nAn or n$\overline{OE}$ to nBn; see Figure 6 | 1.0 | 3.6 | 5.2 | ns |
| $t_{PLZ}$ | LOW to OFF-state propagation delay | n$\overline{OE}$ to nAn or n$\overline{OE}$ to nBn; see Figure 6 | 1.0 | 3.0 | 4.6 | ns |

[1] Typical values for $V_{CC}$ = 2.3 V to 2.7 V are measured at $V_{CC}$ = 2.5 V and $T_{amb}$ = 25 °C.
Typical values for $V_{CC}$ = 3.0 V to 3.6 V are measured at $V_{CC}$ = 3.3 V and $T_{amb}$ = 25 °C.

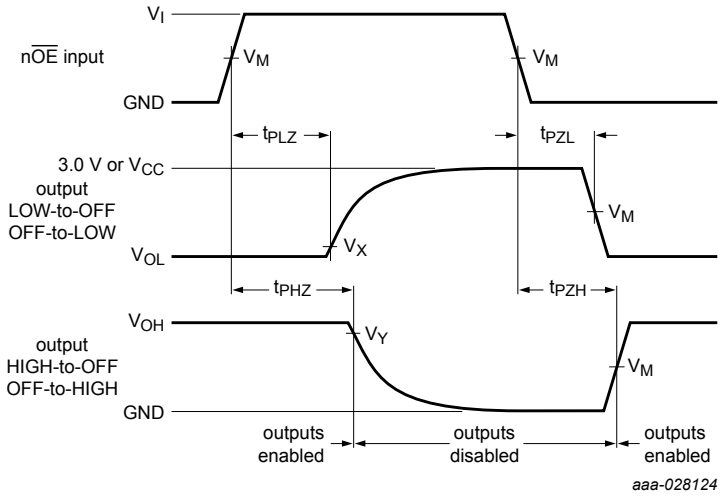
## 10.1 Waveforms and test circuit




Measurement points are given in Table 9.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Figure 5. Input (nAn or nBn) to output (nBn or nAn) propagation delays**



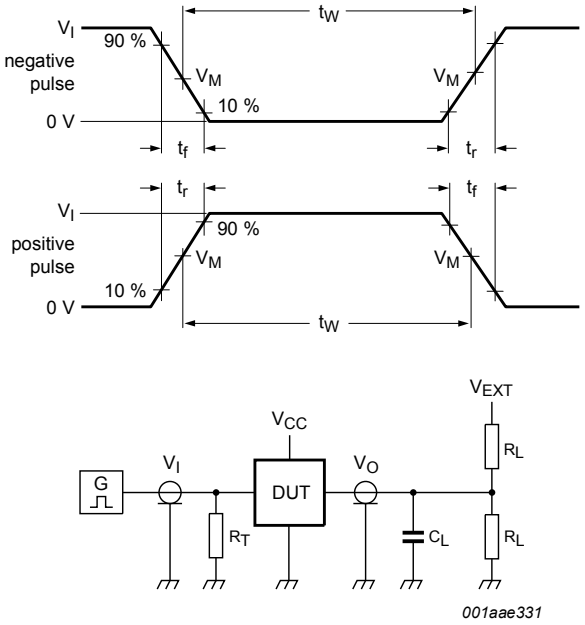

Measurement points are given in Table 9.

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Figure 6. 3-state output enable and disable times**

**Table 9. Measurement points**

| $V_{CC}$ | Input | Output | | | |
|---|---|---|---|---|---|
| | $V_I$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| $V_{CC} \leq 2.7$ V | $V_{CC}$ | 0.5 x $V_{CC}$ | 0.5 x $V_{CC}$ | $V_{OL}$ + 0.1 V | $V_{OH}$ - 0.1 V |
| $V_{CC} \geq 3.0$ V | 3.0 V | 1.5 V | 1.5 V | $V_{OL}$ + 0.3 V | $V_{OH}$ - 0.3 V |




Test data is given in Table 10.

Definitions test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$V_{EXT}$ = Test voltage for switching times.

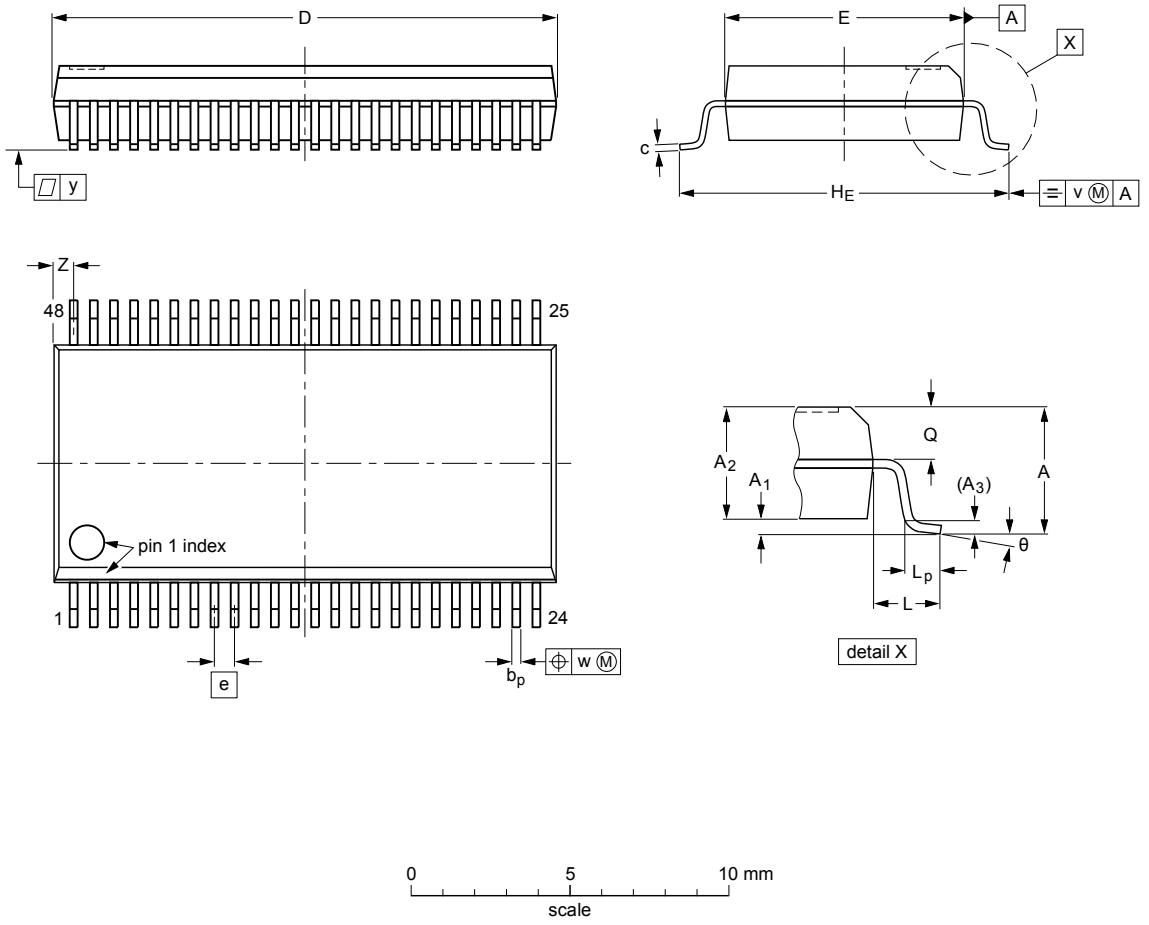
**Figure 7. Test circuit for measuring switching times**

**Table 10. Test data**

| Input | | | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|---|
| $V_I$ | $f_i$ | $t_W$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHZ}$, $t_{PZH}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PLH}$, $t_{PHL}$ |
| 3.0 V or $V_{CC}$ whichever is less | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V or $V_{CC}$ x 2 | open |

## 11 Package outline

**SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm** **SOT370-1**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.8 | 0.4<br>0.2 | 2.35<br>2.20 | 0.25 | 0.3<br>0.2 | 0.22<br>0.13 | 16.00<br>15.75 | 7.6<br>7.4 | 0.635 | 10.4<br>10.1 | 1.4 | 1.0<br>0.6 | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40 | $8^o$<br>$0^o$ |

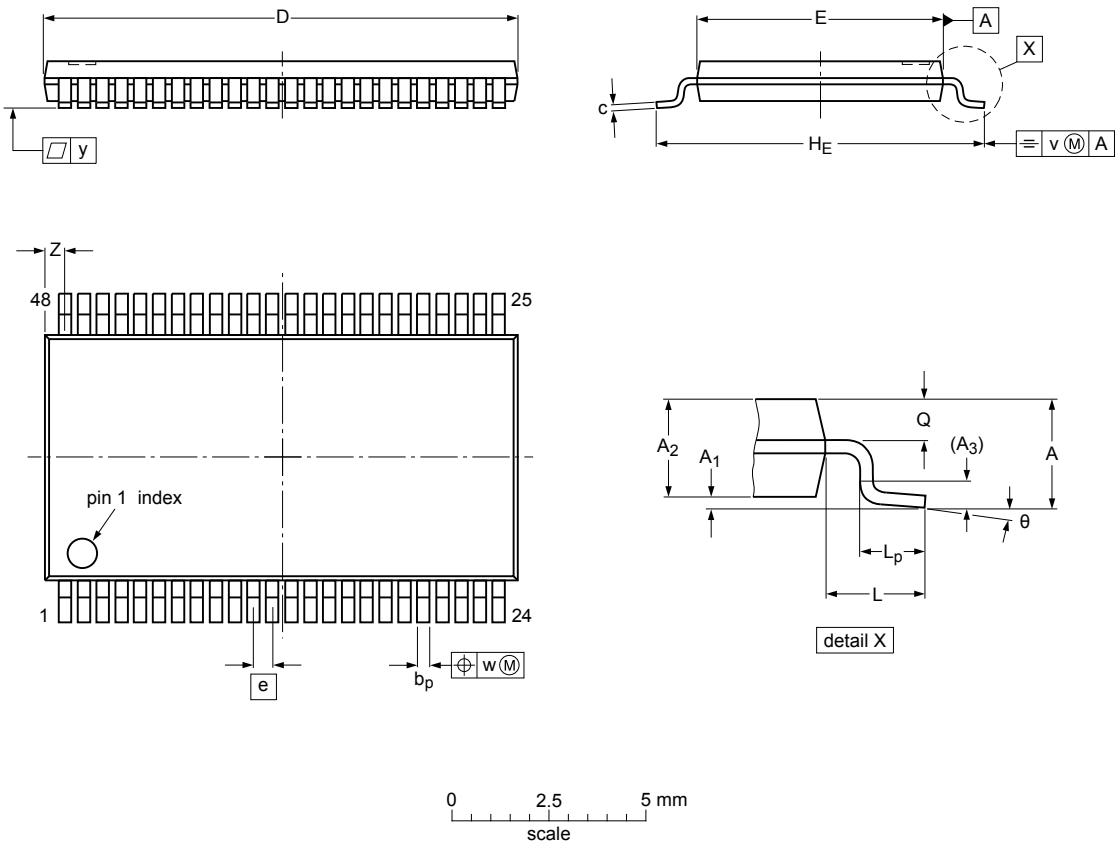
**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT370-1 | | MO-118 | | | | ~~99-12-27~~<br>03-02-19 |

**Figure 8. Package outline SOT370-1 (SSOP48)**

**TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm** **SOT362-1**




Dimensions (mm are the original dimensions)

| Unit | A | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| max | | 0.15 | 1.05 | | 0.28 | 0.2 | 12.6 | 6.2 | | 8.3 | | 0.8 | 0.50 | | | | 0.8 | 8° |
| mm nom | 1.2 | | | 0.25 | | | | | 0.5 | | 1 | | | 0.25 | 0.08 | 0.1 | | |
| min | | 0.05 | 0.85 | | 0.17 | 0.1 | 12.4 | 6.0 | | 7.9 | | 0.4 | 0.35 | | | | 0.4 | 0° |

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

*sot362-1_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT362-1 | | MO-153 | | | | ~~03-02-19~~ 13-08-05 |

**Figure 9. Package outline SOT362-1 (TSSOP48)**

## 12 Abbreviations

**Table 11. Abbreviations**

| Acronym | Description |
|---|---|
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| MIL | Military |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

## 13 Revision history

**Table 12. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74ALVT162245 v.3 | 20180129 | Product data sheet | - | 74ALVT162245 v.2 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.<br>• Legal texts have been adapted to the new company name where appropriate. | | | |
| 74ALVT162245 v.2 | 19980213 | Product specification | - | 74ALVT162245 v.1 |
| 74ALVT162245 v.1 | 19960305 | Product specification | - | - |

# 14 Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

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## Contents





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