



**THE DATASHEET OF
74ABT74PW,118**



74ABT74

Dual D-type flip-flop with set and reset; positive edge-trigger

Rev. 2 — 12 August 2016

Product data sheet

1. General description

The 74ABT74 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT74 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set, and reset inputs; also true and complementary outputs. Set (\overline{nSD}) and reset (\overline{nRD}) are asynchronous active low inputs and operate independently of the clock input. When set and reset are inactive (HIGH), data at the nD input is transferred to the nQ and \overline{nQ} outputs on the LOW-to-HIGH clock transition. Data must be stable just one setup time prior to the LOW-to-HIGH clock transition for predictable operation. Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the nD input may be changed without affecting the levels of the output.

2. Features and benefits

- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------|--|---------|---|----------|
| | Temperature range | Name | Description | Version |
| 74ABT74D | $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74ABT74DB | $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ | SSOP14 | plastic shrink small outline package; 14 leads; body width 5.3 mm | SOT337-1 |
| 74ABT74PW | $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |

4. Functional diagram

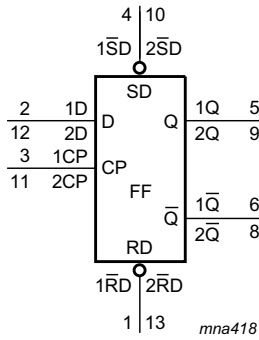


Fig 1. Logic symbol

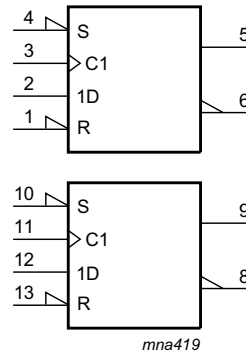


Fig 2. IEC logic symbol

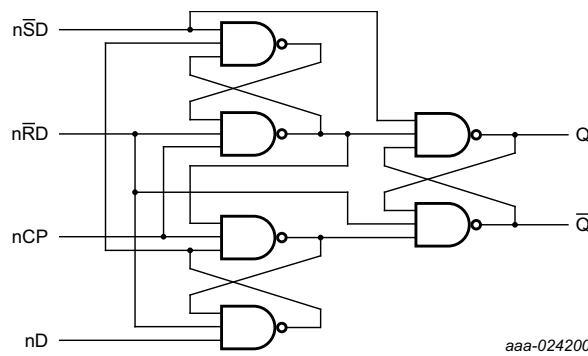


Fig 3. Logic diagram for one flip-flop

5. Pinning information

5.1 Pinning

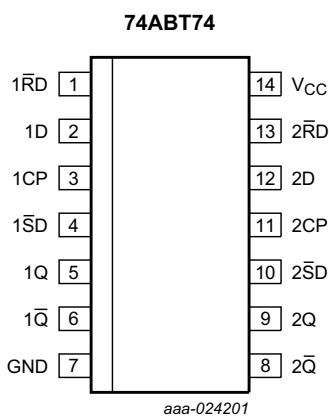


Fig 4. Pin configuration for SO14

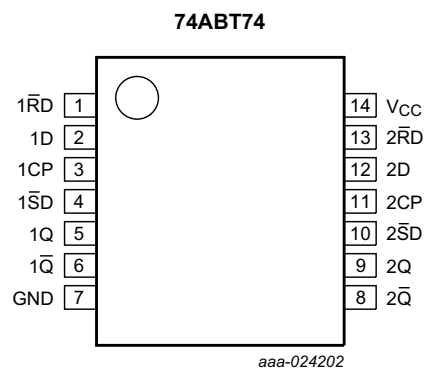


Fig 5. Pin configuration for SSOP14 and TSSOP14

5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|----------------------------------|-------|--|
| $1\overline{RD}, 2\overline{RD}$ | 1, 13 | asynchronous reset-direct input (active LOW) |
| 1D, 2D | 2, 12 | data input |
| 1CP, 2CP | 3, 11 | clock input (LOW-to-HIGH, edge-triggered) |
| $1\overline{SD}, 2\overline{SD}$ | 4, 10 | asynchronous set-direct input (active LOW) |
| 1Q, 2Q | 5, 9 | output |
| $1\overline{Q}, 2\overline{Q}$ | 6, 8 | complement output |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Input | | | | Output | | Operating mode |
|------------------|------------------|-----|----|--------|-----------------|-----------------------------|
| $n\overline{SD}$ | $n\overline{RD}$ | nCP | nD | nQ | $n\overline{Q}$ | |
| L | H | X | X | H | L | Asynchronous set |
| H | L | X | X | L | H | Asynchronous reset |
| L | L | X | X | H | H | Undetermined ^[2] |
| H | H | ↑ | h | H | L | Load "1" |
| H | H | ↑ | l | L | H | Load "0" |

- [1] H = HIGH voltage level
 h = HIGH voltage level one setup time prior to low-to-high clock transition
 L = LOW voltage level
 l = LOW voltage level one setup time prior to low-to-high clock transition
 X = don't care
 ↑ = LOW-to-HIGH clock transition

- [2] This setup is unstable and changes when either set or reset returns to the high level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|---------------------------------------|------|------|------|
| V_{CC} | supply voltage | | -0.5 | +7.0 | V |
| V_I | input voltage | [1] | -1.2 | +7.0 | V |
| V_O | output voltage | output in OFF-state or HIGH-state [1] | -0.5 | +5.5 | V |
| I_{IK} | input clamping current | $V_I < 0$ V | -18 | - | mA |
| I_{OK} | output clamping current | $V_O < 0$ V | -50 | - | mA |
| I_O | output current | output in LOW-state | - | 40 | mA |
| T_j | junction temperature | [2] | - | 150 | °C |
| T_{stg} | storage temperature | | -65 | +150 | °C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------|-------------------------------------|-------------|-----|-----|----------|------|
| V_{CC} | supply voltage | | 4.5 | - | 5.5 | V |
| V_I | input voltage | | 0 | - | V_{CC} | V |
| V_{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| I_{OH} | HIGH-level output current | | -15 | - | - | mA |
| I_{OL} | LOW-level output current | | - | - | 20 | mA |
| $\Delta t/\Delta V$ | input transition rise and fall rate | | 0 | - | 10 | ns/V |
| T_{amb} | ambient temperature | in free air | -40 | - | +85 | °C |

9. Static characteristics

Table 6. Static characteristics

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | Unit |
|-----------------|-----------------------------|---|-------|------------|-----------|------------------|-----------|---------------|
| | | | Min | Typ | Max | Min | Max | |
| V_{IK} | input clamping voltage | $V_{CC} = 4.5 \text{ V}$; $I_{IK} = -18 \text{ mA}$ | -1.2 | -0.9 | - | -1.2 | - | V |
| V_{OH} | HIGH-level output voltage | $V_{CC} = 4.5 \text{ V}$; $I_{OH} = -15 \text{ mA}$; $V_I = V_{IL}$ or V_{IH} | 2.5 | 2.9 | - | 2.5 | - | V |
| V_{OL} | LOW-level output voltage | $V_{CC} = 4.5 \text{ V}$; $I_{OL} = 20 \text{ mA}$; $V_I = V_{IL}$ or V_{IH} | - | 0.35 | 0.5 | - | 0.5 | V |
| I_I | input leakage current | $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or 5.5 V | - | ± 0.01 | ± 1.0 | - | ± 1.0 | μA |
| I_{OFF} | power-off leakage current | $V_{CC} = 0 \text{ V}$; V_I or $V_O \leq 4.5 \text{ V}$ | - | ± 5.0 | ± 100 | - | ± 100 | μA |
| I_{CEX} | output high leakage current | HIGH-state; $V_O = 5.5 \text{ V}$; $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC} | - | 5.0 | 50 | - | 50 | μA |
| I_O | output current | $V_{CC} = 5.5 \text{ V}$; $V_O = 2.5 \text{ V}$ [1] | -50 | -75 | -180 | -50 | -180 | mA |
| I_{CC} | supply current | $V_{CC} = 5.5 \text{ V}$; $V_I = \text{GND}$ or V_{CC} | - | 2 | 50 | - | 50 | μA |
| ΔI_{CC} | additional supply current | per input pin; $V_{CC} = 5.5 \text{ V}$; one input at 3.4 V ; other inputs at V_{CC} or GND [2] | - | 0.25 | 500 | - | 500 | μA |
| C_I | input capacitance | $V_I = 0 \text{ V}$ or V_{CC} | - | 3 | - | - | - | pF |

[1] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[2] This is the increase in supply current for each input at 3.4 V .

10. Dynamic characteristics

Table 7. Dynamic characteristics

$\text{GND} = 0 \text{ V}$; for test circuit, see [Figure 9](#).

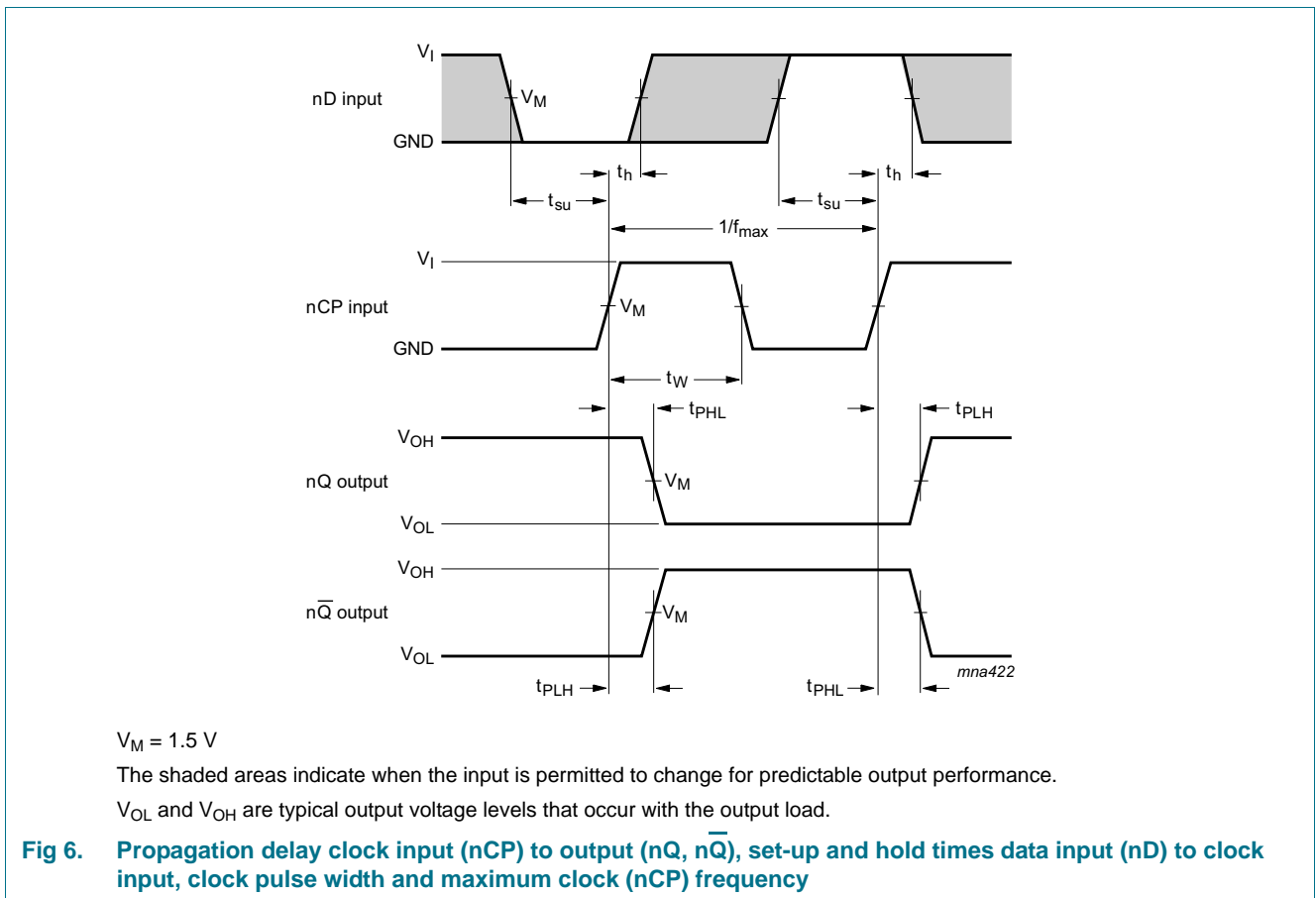
| Symbol | Parameter | Conditions | 25 °C; $V_{CC} = 5.0 \text{ V}$ | | | -40 °C to +85 °C; $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$ | | Unit |
|-------------|-------------------------------|---|---------------------------------|-----|-----|---|-----|------|
| | | | Min | Typ | Max | Min | Max | |
| f_{\max} | maximum frequency | nCP; see Figure 6 | 180 | 250 | - | 150 | - | MHz |
| t_{PLH} | LOW to HIGH propagation delay | nCP to nQ, n \bar{Q} ; see Figure 6 | 1.0 | 3.0 | 4.2 | 1.0 | 4.7 | ns |
| t_{PHL} | HIGH to LOW propagation delay | nCP to nQ, n \bar{Q} ; see Figure 6 | 1.0 | 2.5 | 3.5 | 1.0 | 4.0 | ns |
| t_{PLH} | LOW to HIGH propagation delay | n $\bar{S}D$, n $\bar{R}D$ to nQ, n \bar{Q} ; see Figure 7 | 1.0 | 3.4 | 4.9 | 1.0 | 6.2 | ns |
| t_{PHL} | HIGH to LOW propagation delay | n $\bar{S}D$, n $\bar{R}D$ to nQ, n \bar{Q} ; see Figure 7 | 1.0 | 2.9 | 4.5 | 1.0 | 5.2 | ns |
| $t_{sk(o)}$ | output skew time | [1] | - | 0.5 | 0.6 | - | 0.6 | ns |

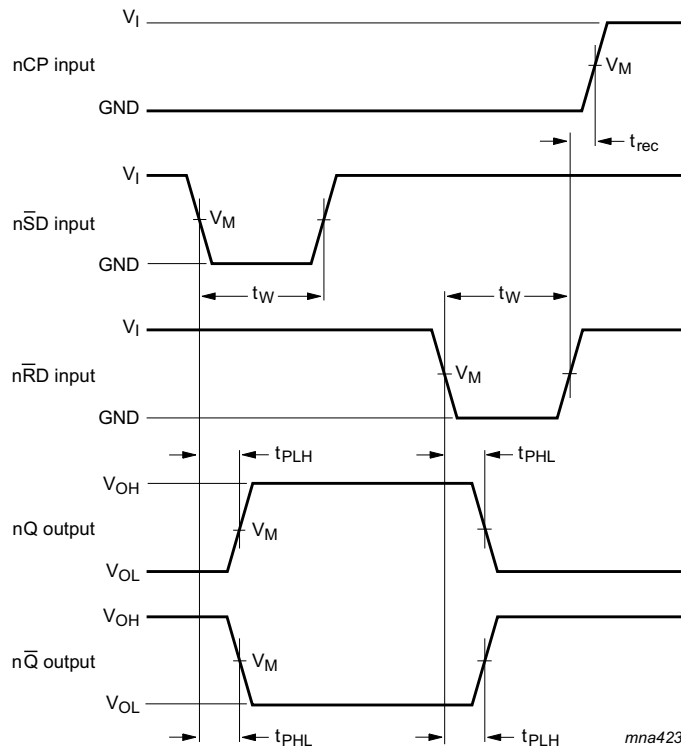
Table 7. Dynamic characteristics ...continued
GND = 0 V; for test circuit, see Figure 9.

| Symbol | Parameter | Conditions | 25 °C; V _{CC} = 5.0 V | | | -40 °C to +85 °C; V _{CC} = 5.0 V ± 0.5 V | | Unit |
|------------------|---------------|---|--------------------------------|------|-----|--|-----|------|
| | | | Min | Typ | Max | Min | Max | |
| t _{su} | set-up time | nD to nCP HIGH; see Figure 6 | 2.6 | 1.4 | - | 2.6 | - | ns |
| | | nD to nCP LOW; see Figure 6 | 2.4 | 1.4 | - | 2.4 | - | ns |
| t _h | hold time | nD to nCP HIGH or LOW; see Figure 6 | 0 | -1.4 | - | 0 | - | ns |
| t _w | pulse width | nCP HIGH or LOW; see Figure 6 | 1.7 | 1.0 | - | 2.1 | - | ns |
| | | n \overline{S} D, n \overline{R} D LOW; see Figure 7 | 2.0 | 1.3 | - | 2.2 | - | ns |
| t _{rec} | recovery time | n \overline{S} D, n \overline{R} D to nCP; see Figure 8 | 2.1 | 1.4 | - | 2.4 | - | ns |

[1] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

11. Waveforms

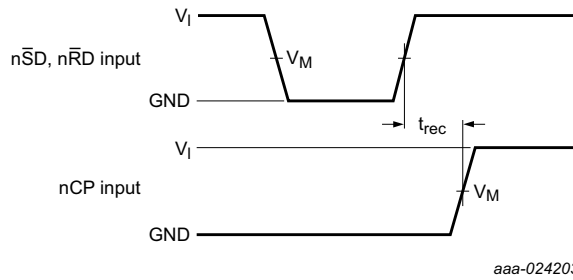




$V_M = 1.5\text{ V}$

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load

Fig 7. Propagation delay set (\overline{nSD}) and reset (\overline{nRD}) input to output (nQ , \overline{nQ}), and set (\overline{nSD}) and reset (\overline{nRD}) pulse width.



$V_M = 1.5\text{ V}$

Fig 8. Recovery time set (\overline{nSD}) and reset (\overline{nRD}) to nCP

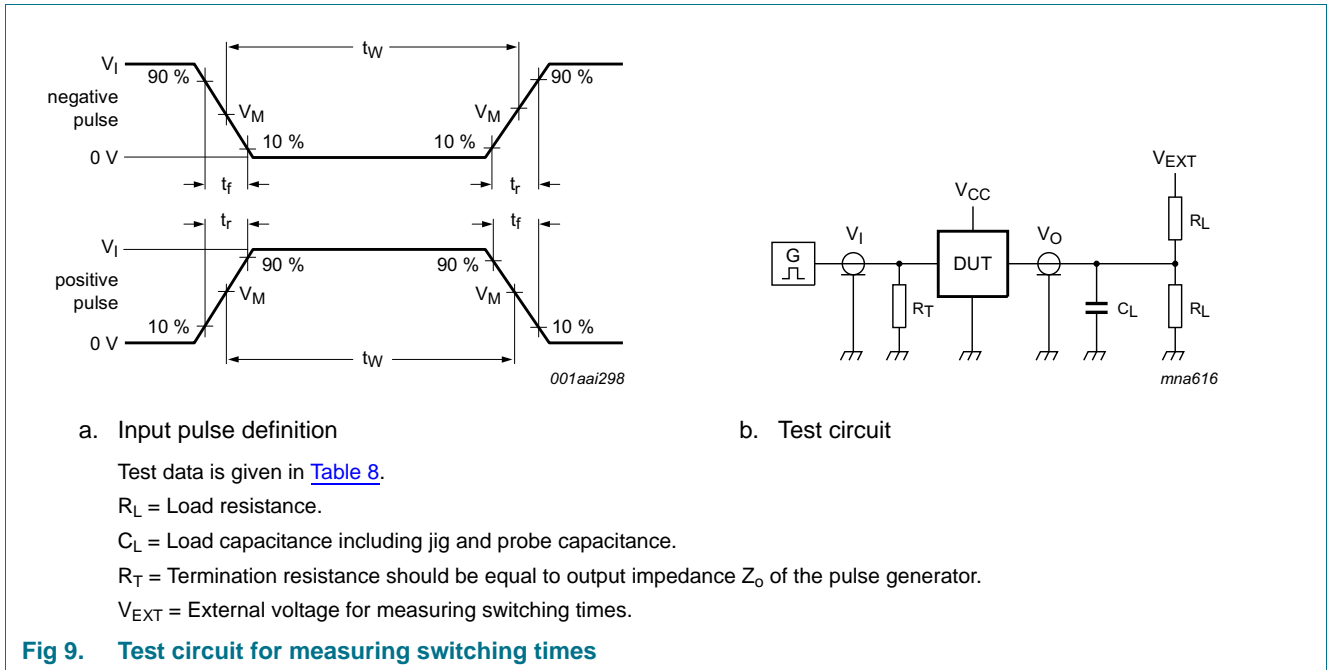


Fig 9. Test circuit for measuring switching times

Table 8. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------|-------|--------|---------------|-------|--------------|--------------------|--------------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 3.0 V | 1 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | open | open | 7.0 V |

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

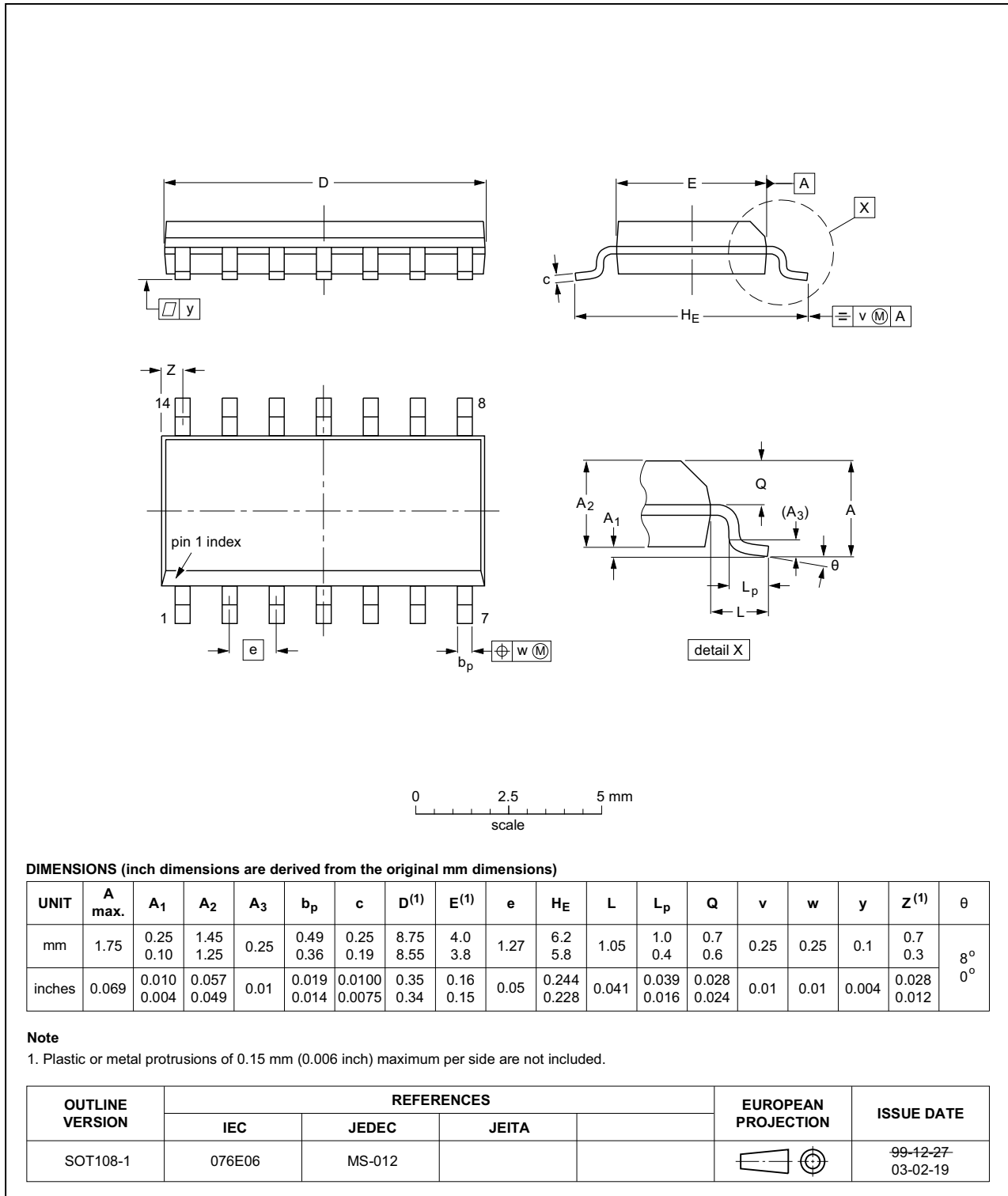


Fig 10. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



Fig 11. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig 12. Package outline SOT402-1 (TSSOP14)

13. Abbreviations

Table 9. Abbreviations

| Acronym | Description |
|---------|---|
| BiCMOS | Bipolar Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |

14. Revision history

Table 10. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|-----------------------|---------------|--------------|
| 74ABT74A v.2 | 20160812 | Product data sheet | - | 74ABT74A v.1 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. | | | |
| 74ABT74A v.1 | 19950922 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Dual D-type flip-flop with set and reset; positive edge-trigger

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nexperia.com>



For sales office addresses, please send an email to: salesaddresses@nexperia.com

17. Contents

| | | |
|-----------|---|-----------|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Ordering information | 1 |
| 4 | Functional diagram | 2 |
| 5 | Pinning information | 2 |
| 5.1 | Pinning | 2 |
| 5.2 | Pin description | 3 |
| 6 | Functional description | 3 |
| 7 | Limiting values | 4 |
| 8 | Recommended operating conditions | 4 |
| 9 | Static characteristics | 5 |
| 10 | Dynamic characteristics | 5 |
| 11 | Waveforms | 6 |
| 12 | Package outline | 9 |
| 13 | Abbreviations | 12 |
| 14 | Revision history | 12 |
| 15 | Legal information | 13 |
| 15.1 | Data sheet status | 13 |
| 15.2 | Definitions | 13 |
| 15.3 | Disclaimers | 13 |
| 15.4 | Trademarks | 14 |
| 16 | Contact information | 14 |
| 17 | Contents | 15 |

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View 74ABT74PW,118 on WIN SOURCE](#)
-  [Nexperia USA Inc. Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management