



**THE DATASHEET OF
AT91SAM7S64C-AU-999**



SAM7S512 SAM7S256 SAM7S128 SAM7S64
SAM7S321 SAM7S32 SAM7S161 SAM7S16
Summary

Features

- Incorporates the ARM7TDMI® ARM® Thumb® Processor
 - High-performance 32-bit RISC Architecture
 - High-density 16-bit Instruction Set
 - Leader in MIPS/Watt
 - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
- Internal High-speed Flash
 - 512 Kbytes (SAM7S512) Organized in Two Contiguous Banks of 1024 Pages of 256 Bytes (Dual Plane)
 - 256 Kbytes (SAM7S256) Organized in 1024 Pages of 256 Bytes (Single Plane)
 - 128 Kbytes (SAM7S128) Organized in 512 Pages of 256 Bytes (Single Plane)
 - 64 Kbytes (SAM7S64) Organized in 512 Pages of 128 Bytes (Single Plane)
 - 32 Kbytes (SAM7S321/32) Organized in 256 Pages of 128 Bytes (Single Plane)
 - 16 Kbytes (SAM7S161/16) Organized in 256 Pages of 64 Bytes (Single Plane)
 - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
 - Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
 - Page Programming Time: 6 ms, Including Page Auto-erase, Full Erase Time: 15 ms
 - 10,000 Write Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
 - Fast Flash Programming Interface for High Volume Production
- Internal High-speed SRAM, Single-cycle Access at Maximum Speed
 - 64 Kbytes (SAM7S512/256)
 - 32 Kbytes (SAM7S128)
 - 16 Kbytes (SAM7S64)
 - 8 Kbytes (SAM7S321/32)
 - 4 Kbytes (SAM7S161/16)
- Memory Controller (MC)
 - Embedded Flash Controller, Abort Status and Misalignment Detection
- Reset Controller (RSTC)
 - Based on Power-on Reset and Low-power Factory-calibrated Brown-out Detector
 - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
 - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and one PLL
- Power Management Controller (PMC)
 - Software Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
 - Three Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
 - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
 - Two (SAM7S512/256/128/64/321/161) or One (SAM7S32/16) External Interrupt Source(s) and One Fast Interrupt Source, Spurious Interrupt Protected

This is a summary document.
The complete document is
available on the Atmel website
at www.atmel.com.

- **Debug Unit (DBGU)**
 - 2-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
 - Mode for General Purpose 2-wire UART Serial Communication
- **Periodic Interval Timer (PIT)**
 - 20-bit Programmable Counter plus 12-bit Interval Counter
- **Windowed Watchdog (WDT)**
 - 12-bit key-protected Programmable Counter
 - Provides Reset or Interrupt Signals to the System
 - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- **Real-time Timer (RTT)**
 - 32-bit Free-running Counter with Alarm
 - Runs Off the Internal RC Oscillator
- **One Parallel Input/Output Controller (PIOA)**
 - Thirty-two (SAM7S512/256/128/64/321/161) or twenty-one (SAM7S32/16) Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
 - Input Change Interrupt Capability on Each I/O Line
 - Individually Programmable Open-drain, Pull-up resistor and Synchronous Output
- **Eleven (SAM7S512/256/128/64/321/161) or Nine (SAM7S32/16) Peripheral DMA Controller (PDC) Channels**
- **One USB 2.0 Full Speed (12 Mbits per Second) Device Port (Except for the SAM7S32/16).**
 - On-chip Transceiver, 328-byte Configurable Integrated FIFOs
- **One Synchronous Serial Controller (SSC)**
 - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
 - I²S Analog Interface Support, Time Division Multiplex Support
 - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- **Two (SAM7S512/256/128/64/321/161) or One (SAM7S32/16) Universal Synchronous/Asynchronous Receiver Transmitters (USART)**
 - Individual Baud Rate Generator, IrDA[®] Infrared Modulation/Demodulation
 - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
 - Full Modem Line Support on USART1 (SAM7S512/256/128/64/321/161)
- **One Master/Slave Serial Peripheral Interface (SPI)**
 - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- **One Three-channel 16-bit Timer/Counter (TC)**
 - Three External Clock Input and Two Multi-purpose I/O Pins per Channel (SAM7S512/256/128/64/321/161)
 - One External Clock Input and Two Multi-purpose I/O Pins for the first Two Channels Only (SAM7S32/16)
 - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- **One Four-channel 16-bit PWM Controller (PWMC)**
- **One Two-wire Interface (TWI)**
 - Master Mode Support Only, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported (SAM7S512/256/128/64/321/32)
 - Master, Multi-Master and Slave Mode Support, All Two-wire Atmel EEPROMs and I²C Compatible Devices Supported (SAM7S161/16)
- **One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os**
- **SAM-BA™ Boot Assistant**
 - Default Boot program
 - Interface with SAM-BA Graphic User Interface
- **IEEE[®] 1149.1 JTAG Boundary Scan on All Digital Pins**
- **5V-tolerant I/Os, including Four High-current Drive I/O lines, Up to 16 mA Each (SAM7S161/16 I/Os Not 5V-tolerant)**
- **Power Supplies**
 - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
 - 3.3V or 1.8V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
 - 1.8V VDDCORE Core Power Supply with Brown-out Detector

- **Fully Static Operation: Up to 55 MHz at 1.65V and 85- C Worst Case Conditions**
- **Available in 64-lead LQFP Green or 64-pad QFN Green Package (SAM7S512/256/128/64/321/161) and 48-lead LQFP Green or 48-pad QFN Green Package (SAM7S32/16)**

1. Description

Atmel's SAM7S is a series of low pincount Flash microcontrollers based on the 32-bit ARM RISC processor. It features a high-speed Flash and an SRAM, a large set of peripherals, including a USB 2.0 device (except for the SAM7S32 and SAM7S16), and a complete set of system functions minimizing the number of external components. The device is an ideal migration path for 8-bit microcontroller users looking for additional performance and extended memory.

The embedded Flash memory can be programmed in-system via the JTAG-ICE interface or via a parallel interface on a production programmer prior to mounting. Built-in lock bits and a security bit protect the firmware from accidental overwrite and preserves its confidentiality.

The SAM7S Series system controller includes a reset controller capable of managing the power-on sequence of the microcontroller and the complete system. Correct device operation can be monitored by a built-in brownout detector and a watchdog running off an integrated RC oscillator.

The SAM7S Series are general-purpose microcontrollers. Their integrated USB Device port makes them ideal devices for peripheral applications requiring connectivity to a PC or cellular phone. Their aggressive price point and high level of integration pushes their scope of use far into the cost-sensitive, high-volume consumer market.

1.1 Configuration Summary of the SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16

The SAM7S512, SAM7S256, SAM7S128, SAM7S64, SAM7S321, SAM7S32, SAM7S161 and SAM7S16 differ in memory size, peripheral set and package. [Table 1-1](#) summarizes the configuration of the six devices.

Except for the SAM7S32/16, all other SAM7S devices are package and pinout compatible.

Table 1-1. Configuration Summary

| Device | Flash | SRAM | Flash Plane | SRAM | UART | USART1 | USART2 | USART3 | USART4 | USART5 | USART6 | Package |
|----------|------------|------------------|--------------|-----------|-------------|----------------------|--------|--------|------------------|--------|--------|-----------------|
| SAM7S512 | 512 Kbytes | Master | dual plane | 64 Kbytes | 1 | 2 ^{(1) (2)} | 2 | 11 | 3 | Yes | 32 | LQFP/ QFN 64 |
| SAM7S256 | 256 Kbytes | Master | single plane | 64 Kbytes | 1 | 2 ^{(1) (2)} | 2 | 11 | 3 | Yes | 32 | LQFP/ QFN 64 |
| SAM7S128 | 128 Kbytes | Master | single plane | 32 Kbytes | 1 | 2 ^{(1) (2)} | 2 | 11 | 3 | Yes | 32 | LQFP/ QFN 64 |
| SAM7S64 | 64 Kbytes | Master | single plane | 16 Kbytes | 1 | 2 ⁽²⁾ | 2 | 11 | 3 | Yes | 32 | LQFP/ QFN 64 |
| SAM7S321 | 32 Kbytes | Master | single plane | 8 Kbytes | 1 | 2 ⁽²⁾ | 2 | 11 | 3 | Yes | 32 | LQFP/ QFN 64 |
| SAM7S32 | 32 Kbytes | Master | single plane | 8 Kbytes | not present | 1 | 1 | 9 | 3 ⁽³⁾ | Yes | 21 | LQFP/ QFN 48 |
| SAM7S161 | 16 Kbytes | Master/ Slave | single plane | 4 Kbytes | 1 | 2 ⁽²⁾ | 2 | 11 | 3 | No | 32 | LQFP |
| SAM7S16 | 16 Kbytes | Master/ Slave | single plane | 4 Kbytes | not present | 1 | 1 | 9 | 3 ⁽³⁾ | No | 21 | LQFP/ QFN 48 |

- Notes:
1. Fractional Baud Rate.
 2. Full modem line support on USART1.
 3. Only two TC channels are accessible through the PIO.

2. Block Diagram

Figure 2-1. SAM7S512/256/128/64/321/161 Block Diagram

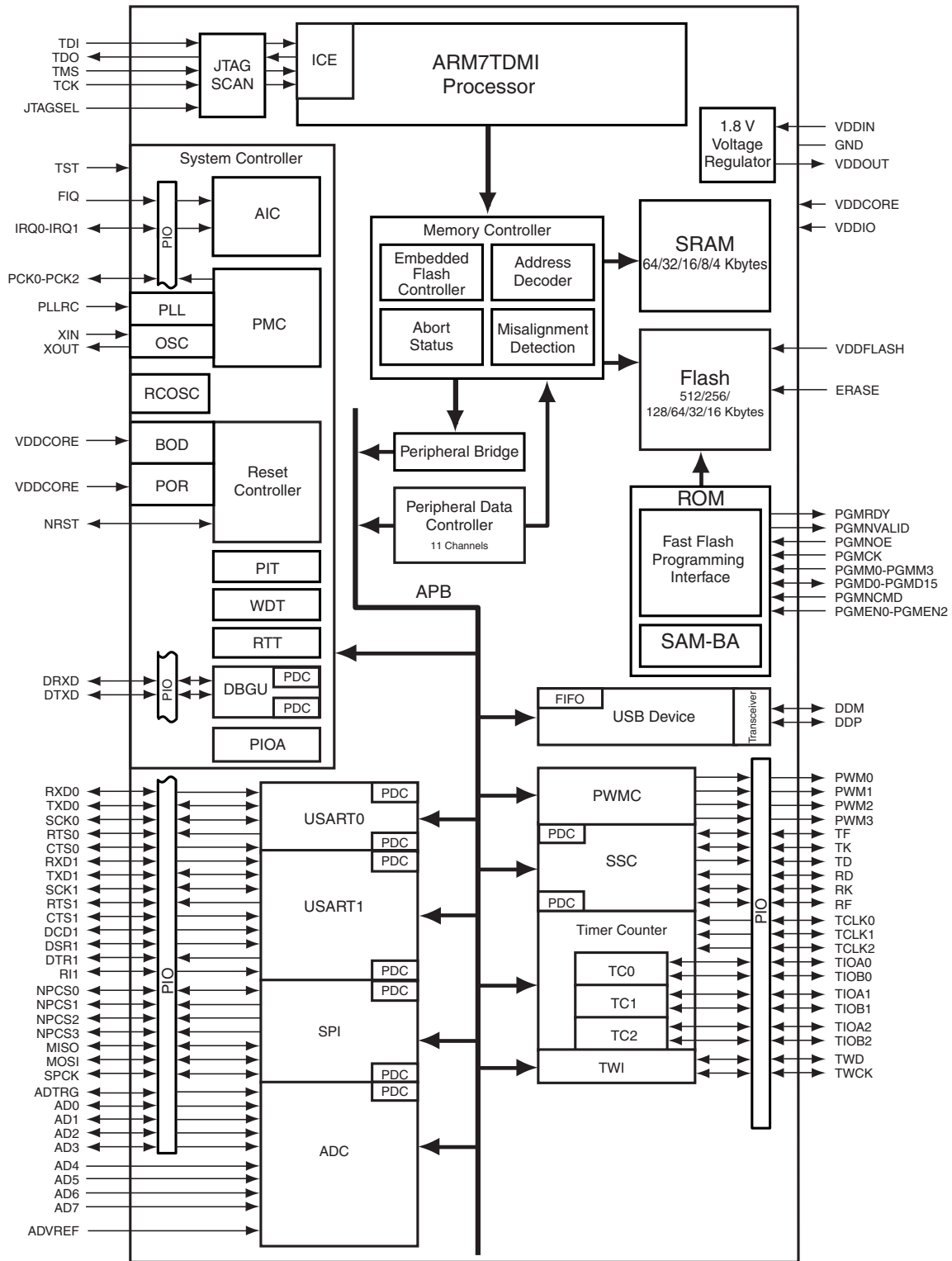
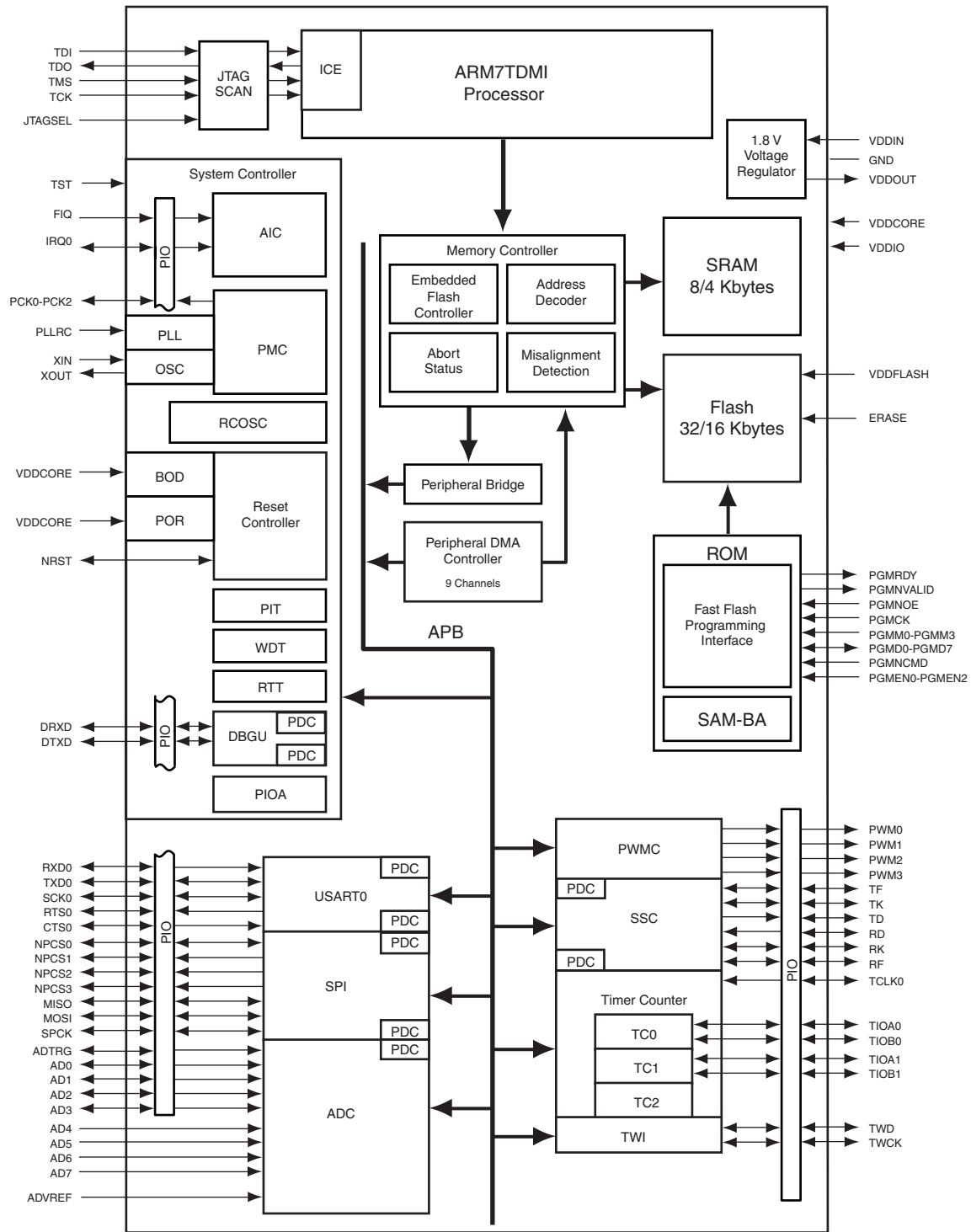


Figure 2-2. SAM7S32/16 Block Diagram



3. Signal Description

Table 3-1. Signal Description List

| | | | | |
|-------------|--|--------|------|---|
| | | | | |
| VDDIN | Voltage and ADC Regulator Power Supply Input | Power | | 3.0 to 3.6V |
| VDDOUT | Voltage Regulator Output | Power | | 1.85V nominal |
| VDDFLASH | Flash Power Supply | Power | | 3.0V to 3.6V |
| VDDIO | I/O Lines Power Supply | Power | | 3.0V to 3.6V or 1.65V to 1.95V |
| VDDCORE | Core Power Supply | Power | | 1.65V to 1.95V |
| VDDPLL | PLL | Power | | 1.65V to 1.95V |
| GND | Ground | Ground | | |
| XIN | Main Oscillator Input | Input | | |
| XOUT | Main Oscillator Output | Output | | |
| PLLRC | PLL Filter | Input | | |
| PCK0 - PCK2 | Programmable Clock Output | Output | | |
| TCK | Test Clock | Input | | No pull-up resistor |
| TDI | Test Data In | Input | | No pull-up resistor |
| TDO | Test Data Out | Output | | |
| TMS | Test Mode Select | Input | | No pull-up resistor |
| JTAGSEL | JTAG Selection | Input | | Pull-down resistor ⁽¹⁾ |
| ERASE | Flash and NVM Configuration Bits Erase Command | Input | High | Pull-down resistor ⁽¹⁾ |
| NRST | Microcontroller Reset | I/O | Low | Open-drain with pull-Up resistor |
| TST | Test Mode Select | Input | High | Pull-down resistor ⁽¹⁾ |
| DRXD | Debug Receive Data | Input | | |
| DTXD | Debug Transmit Data | Output | | |
| IRQ0 - IRQ1 | External Interrupt Inputs | Input | | IRQ1 not present on SAM7S32/16 |
| FIQ | Fast Interrupt Input | Input | | |
| PA0 - PA31 | Parallel IO Controller A | I/O | | Pulled-up input at reset PA0 - PA20 only on SAM7S32/16 |

Table 3-1. Signal Description List (Continued)

| | | | | |
|---------------|-----------------------------------|--------|-----|---|
| | | | | |
| DDM | USB Device Port Data - | Analog | | not present on SAM7S32/16 |
| DDP | USB Device Port Data + | Analog | | not present on SAM7S32/16 |
| SCK0 - SCK1 | Serial Clock | I/O | | SCK1 not present on SAM7S32/16 |
| TXD0 - TXD1 | Transmit Data | I/O | | TXD1 not present on SAM7S32/16 |
| RXD0 - RXD1 | Receive Data | Input | | RXD1 not present on SAM7S32/16 |
| RTS0 - RTS1 | Request To Send | Output | | RTS1 not present on SAM7S32/16 |
| CTS0 - CTS1 | Clear To Send | Input | | CTS1 not present on SAM7S32/16 |
| DCD1 | Data Carrier Detect | Input | | not present on SAM7S32/16 |
| DTR1 | Data Terminal Ready | Output | | not present on SAM7S32/16 |
| DSR1 | Data Set Ready | Input | | not present on SAM7S32/16 |
| RI1 | Ring Indicator | Input | | not present on SAM7S32/16 |
| TD | Transmit Data | Output | | |
| RD | Receive Data | Input | | |
| TK | Transmit Clock | I/O | | |
| RK | Receive Clock | I/O | | |
| TF | Transmit Frame Sync | I/O | | |
| RF | Receive Frame Sync | I/O | | |
| TCLK0 - TCLK2 | External Clock Inputs | Input | | TCLK1 and TCLK2 not present on SAM7S32/16 |
| TIOA0 - TIOA2 | I/O Line A | I/O | | TIOA2 not present on SAM7S32/16 |
| TIOB0 - TIOB2 | I/O Line B | I/O | | TIOB2 not present on SAM7S32/16 |
| PWM0 - PWM3 | PWM Channels | Output | | |
| MISO | Master In Slave Out | I/O | | |
| MOSI | Master Out Slave In | I/O | | |
| SPCK | SPI Serial Clock | I/O | | |
| NPCS0 | SPI Peripheral Chip Select 0 | I/O | Low | |
| NPCS1-NPCS3 | SPI Peripheral Chip Select 1 to 3 | Output | Low | |

Table 3-1. Signal Description List (Continued)

| | | | | |
|---------------|-----------------------|--------|------|-----------------------------------|
| | | | | |
| TWD | Two-wire Serial Data | I/O | | |
| TWCK | Two-wire Serial Clock | I/O | | |
| AD0-AD3 | Analog Inputs | Analog | | Digital pulled-up inputs at reset |
| AD4-AD7 | Analog Inputs | Analog | | Analog Inputs |
| ADTRG | ADC Trigger | Input | | |
| ADVREF | ADC Reference | Analog | | |
| PGMEN0-PGMEN2 | Programming Enabling | Input | | |
| PGMM0-PGMM3 | Programming Mode | Input | | |
| PGMD0-PGMD15 | Programming Data | I/O | | PGMD0-PGMD7 only on SAM7S32/16 |
| PGMRDY | Programming Ready | Output | High | |
| PGMNVALID | Data Direction | Output | Low | |
| PGMNOE | Programming Read | Input | Low | |
| PGMCK | Programming Clock | Input | | |
| PGMNCMD | Programming Command | Input | Low | |

Note: 1. Refer to [Section 6. "I/O Lines Considerations"](#) on page 14.

4. Package and Pinout

The SAM7S512/256/128/64/321 are available in a 64-lead LQFP or 64-pad QFN package.

The SAM7S161 is available in a 64-Lead LQFP package.

The SAM7S32/16 are available in a 48-lead LQFP or 48-pad QFN package.

4.1 64-lead LQFP and 64-pad QFN Package Outlines

Figure 4-1 and Figure 4-2 show the orientation of the 64-lead LQFP and the 64-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-1. 64-lead LQFP Package (Top View)

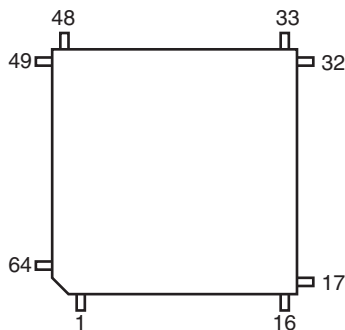
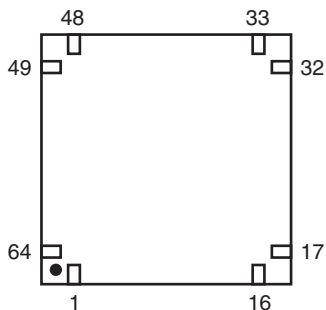


Figure 4-2. 64-pad QFN Package (Top View)



4.2 64-lead LQFP and 64-pad QFN Pinout

Table 4-1. SAM7S512/256/128/64/321/161 Pinout⁽¹⁾

| | | | | | | | |
|----|----------------|----|---------------|----|-------------|----|-----------|
| 1 | ADVREF | 17 | GND | 33 | TDI | 49 | TDO |
| 2 | GND | 18 | VDDIO | 34 | PA6/PGMNOE | 50 | JTAGSEL |
| 3 | AD4 | 19 | PA16/PGMD4 | 35 | PA5/PGMRDY | 51 | TMS |
| 4 | AD5 | 20 | PA15/PGMD3 | 36 | PA4/PGMNCMD | 52 | PA31 |
| 5 | AD6 | 21 | PA14/PGMD2 | 37 | PA27/PGMD15 | 53 | TCK |
| 6 | AD7 | 22 | PA13/PGMD1 | 38 | PA28 | 54 | VDDCORE |
| 7 | VDDIN | 23 | PA24/PGMD12 | 39 | NRST | 55 | ERASE |
| 8 | VDDOUT | 24 | VDDCORE | 40 | TST | 56 | DDM |
| 9 | PA17/PGMD5/AD0 | 25 | PA25/PGMD13 | 41 | PA29 | 57 | DDP |
| 10 | PA18/PGMD6/AD1 | 26 | PA26/PGMD14 | 42 | PA30 | 58 | VDDIO |
| 11 | PA21/PGMD9 | 27 | PA12/PGMD0 | 43 | PA3 | 59 | VDDFLASH |
| 12 | VDDCORE | 28 | PA11/PGMM3 | 44 | PA2/PGMEN2 | 60 | GND |
| 13 | PA19/PGMD7/AD2 | 29 | PA10/PGMM2 | 45 | VDDIO | 61 | XOUT |
| 14 | PA22/PGMD10 | 30 | PA9/PGMM1 | 46 | GND | 62 | XIN/PGMCK |
| 15 | PA23/PGMD11 | 31 | PA8/PGMM0 | 47 | PA1/PGMEN1 | 63 | PLLRC |
| 16 | PA20/PGMD8/AD3 | 32 | PA7/PGMNVALID | 48 | PA0/PGMEN0 | 64 | VDDPLL |

Note: 1. The bottom pad of the QFN package must be connected to ground.

4.3 48-lead LQFP and 48-pad QFN Package Outlines

Figure 4-3 and Figure 4-4 show the orientation of the 48-lead LQFP and the 48-pad QFN package. A detailed mechanical description is given in the section Mechanical Characteristics of the full datasheet.

Figure 4-3. 48-lead LQFP Package (Top View)

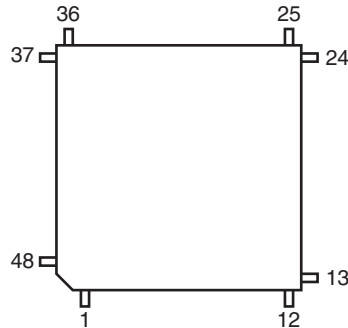
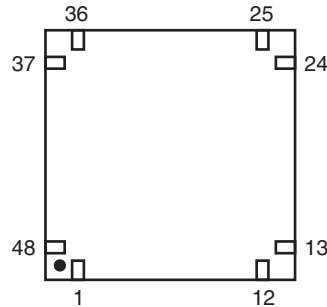


Figure 4-4. 48-pad QFN Package (Top View)



4.4 48-lead LQFP and 48-pad QFN Pinout

Table 4-2. SAM7S32/16 Pinout⁽¹⁾

| | | | | | | | |
|----|----------------|----|---------------|----|-------------|----|-----------|
| 1 | ADVREF | 13 | VDDIO | 25 | TDI | 37 | TDO |
| 2 | GND | 14 | PA16/PGMD4 | 26 | PA6/PGMNOE | 38 | JTAGSEL |
| 3 | AD4 | 15 | PA15/PGMD3 | 27 | PA5/PGMRDY | 39 | TMS |
| 4 | AD5 | 16 | PA14/PGMD2 | 28 | PA4/PGMNCMD | 40 | TCK |
| 5 | AD6 | 17 | PA13/PGMD1 | 29 | NRST | 41 | VDDCORE |
| 6 | AD7 | 18 | VDDCORE | 30 | TST | 42 | ERASE |
| 7 | VDDIN | 19 | PA12/PGMD0 | 31 | PA3 | 43 | VDDFLASH |
| 8 | VDDOUT | 20 | PA11/PGMM3 | 32 | PA2/PGMEN2 | 44 | GND |
| 9 | PA17/PGMD5/AD0 | 21 | PA10/PGMM2 | 33 | VDDIO | 45 | XOUT |
| 10 | PA18/PGMD6/AD1 | 22 | PA9/PGMM1 | 34 | GND | 46 | XIN/PGMCK |
| 11 | PA19/PGMD7/AD2 | 23 | PA8/PGMM0 | 35 | PA1/PGMEN1 | 47 | PLLRC |
| 12 | PA20/AD3 | 24 | PA7/PGMNVALID | 36 | PA0/PGMEN0 | 48 | VDDPLL |

Note: 1. The bottom pad of the QFN package must be connected to ground.

5. Power Considerations

5.1 Power Supplies

The SAM7S Series has six types of power supply pins and integrates a voltage regulator, allowing the device to be supplied with only one voltage. The six power supply pin types are:

- VDDIN pin. It powers the voltage regulator and the ADC; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDOUT pin. It is the output of the 1.8V voltage regulator.
- VDDIO pin. It powers the I/O lines and the USB transceivers; dual voltage range is supported. Ranges from 3.0V to 3.6V, 3.3V nominal or from 1.65V to 1.95V, 1.8V nominal. Note that supplying less than 3.0V to VDDIO prevents any use of the USB transceivers.
- VDDFLASH pin. It powers a part of the Flash and is required for the Flash to operate correctly; voltage ranges from 3.0V to 3.6V, 3.3V nominal.
- VDDCORE pins. They power the logic of the device; voltage ranges from 1.65V to 1.95V, 1.8V typical. It can be connected to the VDDOUT pin with decoupling capacitor. VDDCORE is required for the device, including its embedded Flash, to operate correctly.

During startup, core supply voltage (VDDCORE) slope must be superior or equal to 6V/ms.

- VDDPLL pin. It powers the oscillator and the PLL. It can be connected directly to the VDDOUT pin.

No separate ground pins are provided for the different power supplies. Only GND pins are provided and should be connected as shortly as possible to the system ground plane.

In order to decrease current consumption, if the voltage regulator and the ADC are not used, VDDIN, ADVREF, AD4, AD5, AD6 and AD7 should be connected to GND. In this case VDDOUT should be left unconnected.

5.2 Power Consumption

The SAM7S Series has a static current of less than 60 μ A on VDDCORE at 25°C, including the RC oscillator, the voltage regulator and the power-on reset. When the brown-out detector is activated, 20 μ A static current is added.

The dynamic power consumption on VDDCORE is less than 50 mA at full speed when running out of the Flash. Under the same conditions, the power consumption on VDDFLASH does not exceed 10 mA.

5.3 Voltage Regulator

The SAM7S Series embeds a voltage regulator that is managed by the System Controller.

In Normal Mode, the voltage regulator consumes less than 100 μ A static current and draws 100 mA of output current.

The voltage regulator also has a Low-power Mode. In this mode, it consumes less than 25 μ A static current and draws 1 mA of output current.

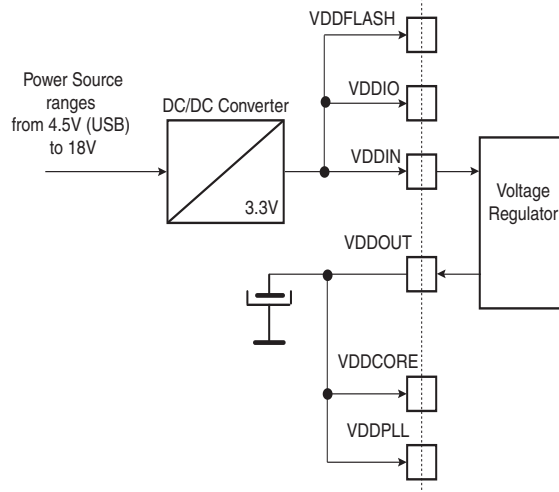
Adequate output supply decoupling is mandatory for VDDOUT to reduce ripple and avoid oscillations. The best way to achieve this is to use two capacitors in parallel: one external 470 pF (or 1 nF) NPO capacitor must be connected between VDDOUT and GND as close to the chip as possible. One external 2.2 μ F (or 3.3 μ F) X7R capacitor must be connected between VDDOUT and GND.

Adequate input supply decoupling is mandatory for VDDIN in order to improve startup stability and reduce source voltage drop. The input decoupling capacitor should be placed close to the chip. For example, two capacitors can be used in parallel: 100 nF NPO and 4.7 μ F X7R.

5.4 Typical Powering Schematics

The SAM7S Series supports a 3.3V single supply mode. The internal regulator is connected to the 3.3V source and its output feeds VDDCORE and the VDDPLL. [Figure 5-1](#) shows the power schematics to be used for USB bus-powered systems.

Figure 5-1. 3.3V System Single Power Supply Schematic



6. I/O Lines Considerations

6.1 JTAG Port Pins

TMS, TDI and TCK are schmitt trigger inputs. TMS and TCK are 5-V tolerant, TDI is not. TMS, TDI and TCK do not integrate a pull-up resistor.

TDO is an output, driven at up to VDDIO, and has no pull-up resistor.

The JTAGSEL pin is used to select the JTAG boundary scan when asserted at a high level. The JTAGSEL pin integrates a permanent pull-down resistor of about 15 k Ω to GND, so that it can be left unconnected for normal operations.

6.2 Test Pin

The TST pin is used for manufacturing test, fast programming mode or SAM-BA Boot Recovery of the SAM7S Series when asserted high. The TST pin integrates a permanent pull-down resistor of about 15 k Ω to GND, so that it can be left unconnected for normal operations.

To enter fast programming mode, the TST pin and the PA0 and PA1 pins should be tied high and PA2 tied to low.

To enter SAM-BA Boot Recovery, the TST pin and the PA0, PA1 and PA2 pins should be tied high for at least 10 seconds. Then a power cycle of the board is mandatory.

Driving the TST pin at a high level while PA0 or PA1 is driven at 0 leads to unpredictable results.

6.3 Reset Pin

The NRST pin is bidirectional with an open drain output buffer. It is handled by the on-chip reset controller and can be driven low to provide a reset signal to the external components or asserted low externally to reset the microcontroller. There is no constraint on the length of the reset pulse, and the reset controller can guarantee a minimum pulse length. This allows connection of a simple push-button on the pin NRST as system user reset, and the use of the signal NRST to reset all the components of the system.

The NRST pin integrates a permanent pull-up resistor to VDDIO.

6.4 ERASE Pin

The ERASE pin is used to re-initialize the Flash content and some of its NVM bits. It integrates a permanent pull-down resistor of about 15 k Ω to GND, so that it can be left unconnected for normal operations.

6.5 PIO Controller A Lines

- All the I/O lines PA0 to PA31 on SAM7S512/256/128/64/321 (PA0 to PA20 on SAM7S32) are 5V-tolerant and all integrate a programmable pull-up resistor.
- All the I/O lines PA0 to PA31 on SAM7S161 (PA0 to PA20 on SAM7S16) are **not** 5V-tolerant and all integrate a programmable pull-up resistor.

Programming of this pull-up resistor is performed independently for each I/O line through the PIO controllers.

5V-tolerant means that the I/O lines can drive voltage level according to VDDIO, but can be driven with a voltage of up to 5.5V. However, driving an I/O line with a voltage over VDDIO while the programmable pull-up resistor is enabled will create a current path through the pull-up resistor from the I/O line to VDDIO. Care should be taken, in particular at reset, as all the I/O lines default to input with the pull-up resistor enabled at reset.

6.6 I/O Line Drive Levels

The PIO lines PA0 to PA3 are high-drive current capable. Each of these I/O lines can drive up to 16 mA permanently.

The remaining I/O lines can draw only 8 mA.

However, the total current drawn by all the I/O lines cannot exceed 150 mA (100 mA for SAM7S32/16).

7. Processor and Architecture

7.1 ARM7TDMI Processor

- RISC processor based on ARMv4T Von Neumann architecture
 - Runs at up to 55 MHz, providing 0.9 MIPS/MHz
- Two instruction sets
 - ARM® high-performance 32-bit instruction set
 - Thumb® high code density 16-bit instruction set
- Three-stage pipeline architecture
 - Instruction Fetch (F)
 - Instruction Decode (D)
 - Execute (E)

7.2 Debug and Test Features

- Integrated EmbeddedICE™ (embedded in-circuit emulator)
 - Two watchpoint units
 - Test access port accessible through a JTAG protocol
 - Debug communication channel
- Debug Unit
 - Two-pin UART
 - Debug communication channel interrupt handling
 - Chip ID Register
- IEEE1149.1 JTAG Boundary-scan on all digital pins

7.3 Memory Controller

- Bus Arbiter
 - Handles requests from the ARM7TDMI and the Peripheral DMA Controller
- Address decoder provides selection signals for
 - Three internal 1 Mbyte memory areas
 - One 256 Mbyte embedded peripheral area
- Abort Status Registers
 - Source, Type and all parameters of the access leading to an abort are saved
 - Facilitates debug by detection of bad pointers
- Misalignment Detector
 - Alignment checking of all data accesses
 - Abort generation in case of misalignment
- Remap Command
 - Remaps the SRAM in place of the embedded non-volatile memory
 - Allows handling of dynamic exception vectors
- Embedded Flash Controller
 - Embedded Flash interface, up to three programmable wait states
 - Prefetch buffer, buffering and anticipating the 16-bit requests, reducing the required wait states
 - Key-protected program, erase and lock/unlock sequencer
 - Single command for erasing, programming and locking operations
 - Interrupt generation in case of forbidden operation

7.4 Peripheral DMA Controller

- Handles data transfer between peripherals and memories
- Eleven channels: SAM7S512/256/128/64/321/161
- Nine channels: SAM7S32/16
 - Two for each USART
 - Two for the Debug Unit
 - Two for the Serial Synchronous Controller
 - Two for the Serial Peripheral Interface
 - One for the Analog-to-digital Converter
- Low bus arbitration overhead
 - One Master Clock cycle needed for a transfer from memory to peripheral
 - Two Master Clock cycles needed for a transfer from peripheral to memory
- Next Pointer management for reducing interrupt latency requirements
- Peripheral DMA Controller (PDC) priority is as follows (from the highest priority to the lowest):

| | |
|----------|--------|
| Receive | DBGU |
| Receive | USART0 |
| Receive | USART1 |
| Receive | SSC |
| Receive | ADC |
| Receive | SPI |
| Transmit | DBGU |
| Transmit | USART0 |
| Transmit | USART1 |
| Transmit | SSC |
| Transmit | SPI |

8. Memories

8.1 SAM7S512

- 512 Kbytes of Flash Memory, dual plane
 - 2 contiguous banks of 1024 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 32 lock bits, protecting 32 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
 - Single-cycle access at full speed

8.2 SAM7S256

- 256 Kbytes of Flash Memory, single plane
 - 1024 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 16 lock bits, protecting 16 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 64 Kbytes of Fast SRAM
 - Single-cycle access at full speed

8.3 SAM7S128

- 128 Kbytes of Flash Memory, single plane
 - 512 pages of 256 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 8 lock bits, protecting 8 sectors of 64 pages
 - Protection Mode to secure contents of the Flash
- 32 Kbytes of Fast SRAM
 - Single-cycle access at full speed

8.4 SAM7S64

- 64 Kbytes of Flash Memory, single plane
 - 512 pages of 128 bytes

- Fast access time, 30 MHz single-cycle access in Worst Case conditions
- Page programming time: 6 ms, including page auto-erase
- Page programming without auto-erase: 3 ms
- Full chip erase time: 15 ms
- 10,000 write cycles, 10-year data retention capability
- 16 lock bits, protecting 16 sectors of 32 pages
- Protection Mode to secure contents of the Flash
- 16 Kbytes of Fast SRAM
 - Single-cycle access at full speed

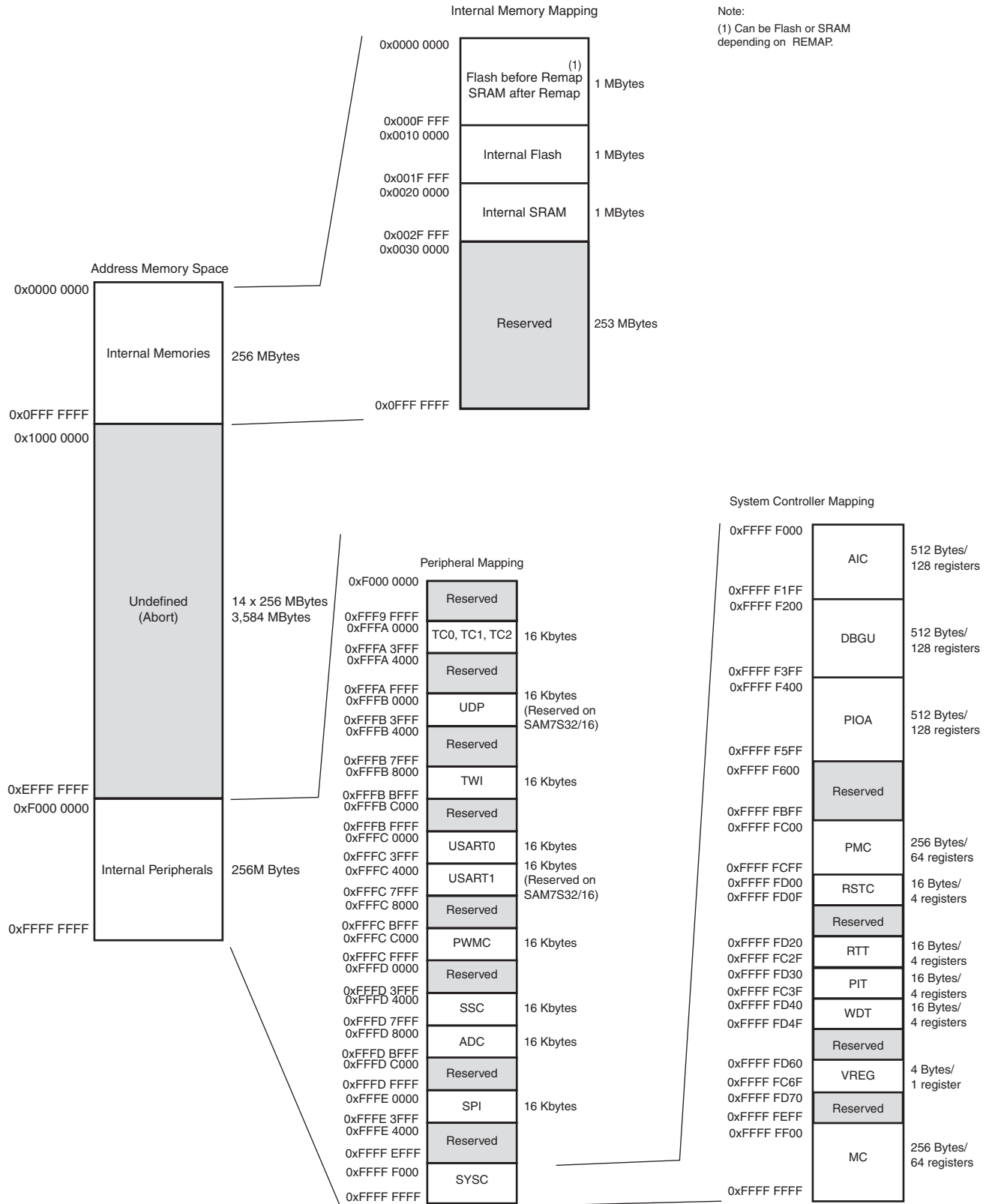
8.5 SAM7S321/32

- 32 Kbytes of Flash Memory, single plane
 - 256 pages of 128 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 8 lock bits, protecting 8 sectors of 32 pages
 - Protection Mode to secure contents of the Flash
- 8 Kbytes of Fast SRAM
 - Single-cycle access at full speed

8.6 SAM7S161/16

- 16 Kbytes of Flash Memory, single plane
 - 256 pages of 64 bytes
 - Fast access time, 30 MHz single-cycle access in Worst Case conditions
 - Page programming time: 6 ms, including page auto-erase
 - Page programming without auto-erase: 3 ms
 - Full chip erase time: 15 ms
 - 10,000 write cycles, 10-year data retention capability
 - 8 lock bits, protecting 8 sectors of 32 pages
 - Protection Mode to secure contents of the Flash
- 4 Kbytes of Fast SRAM
 - Single-cycle access at full speed

Figure 8-1. SAM SAM7S512/256/128/64/321/32/161/16 Memory Mapping



8.7 Memory Mapping

8.7.1 Internal SRAM

- The SAM7S512 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S256 embeds a high-speed 64-Kbyte SRAM bank.
- The SAM7S128 embeds a high-speed 32-Kbyte SRAM bank.
- The SAM7S64 embeds a high-speed 16-Kbyte SRAM bank.
- The SAM7S321 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S32 embeds a high-speed 8-Kbyte SRAM bank.
- The SAM7S161 embeds a high-speed 4-Kbyte SRAM bank.
- The SAM7S16 embeds a high-speed 4-Kbyte SRAM bank.

After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x0020 0000. After Remap, the SRAM also becomes available at address 0x0.

8.7.2 Internal ROM

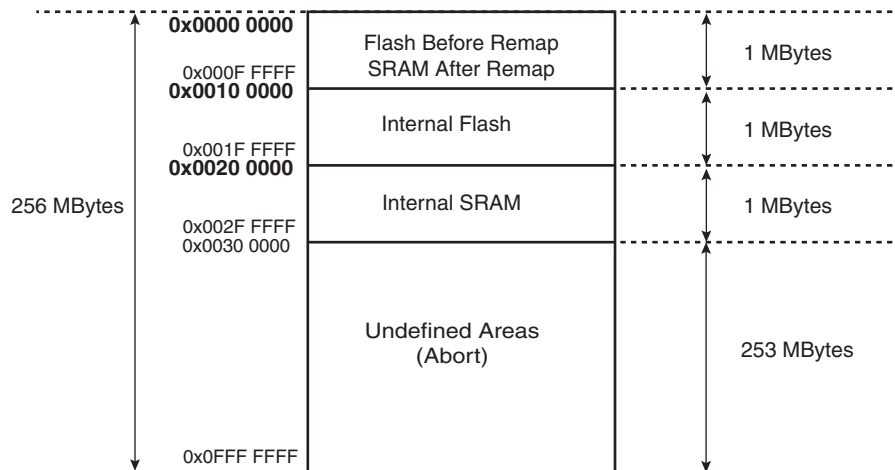
The SAM7S Series embeds an Internal ROM. The ROM contains the FFPI and the SAM-BA program. The internal ROM is not mapped by default.

8.7.3 Internal Flash

- The SAM7S512 features two contiguous banks (dual plane) of 256 Kbytes of Flash.
- The SAM7S256 features one bank (single plane) of 256 Kbytes of Flash.
- The SAM7S128 features one bank (single plane) of 128 Kbytes of Flash.
- The SAM7S64 features one bank (single plane) of 64 Kbytes of Flash.
- The SAM7S321/32 features one bank (single plane) of 32 Kbytes of Flash.
- The SAM7S161/16 features one bank (single plane) of 16 Kbytes of Flash.

At any time, the Flash is mapped to address 0x0010 0000. It is also accessible at address 0x0 after the reset and before the Remap Command.

Figure 8-2. Internal Memory Mapping



8.8 Embedded Flash

8.8.1 Flash Overview

- The Flash of the SAM7S512 is organized in two banks (dual plane) of 1024 pages of 256 bytes. The 524,288 bytes are organized in 32-bit words.
- The Flash of the SAM7S256 is organized in 1024 pages (single plane) of 256 bytes. The 262,144 bytes are organized in 32-bit words.
- The Flash of the SAM7S128 is organized in 512 pages (single plane) of 256 bytes. The 131,072 bytes are organized in 32-bit words.
- The Flash of the SAM7S64 is organized in 512 pages (single plane) of 128 bytes. The 65,536 bytes are organized in 32-bit words.
- The Flash of the SAM7S321/32 is organized in 256 pages (single plane) of 128 bytes. The 32,768 bytes are organized in 32-bit words.
- The Flash of the SAM7S161/16 is organized in 256 pages (single plane) of 64 bytes. The 16,384 bytes are organized in 32-bit words.
- The Flash of the SAM7S512/256/128 contains a 256-byte write buffer, accessible through a 32-bit interface.
- The Flash of the SAM7S64/321/32/161/16 contains a 128-byte write buffer, accessible through a 32-bit interface.

The Flash benefits from the integration of a power reset cell and from the brownout detector. This prevents code corruption during power supply changes, even in the worst conditions.

When Flash is not used (read or write access), it is automatically placed into standby mode.

8.8.2 Embedded Flash Controller

The Embedded Flash Controller (EFC) manages accesses performed by the masters of the system. It enables reading the Flash and writing the write buffer. It also contains a User Interface, mapped within the Memory Controller on the APB. The User Interface allows:

- programming of the access parameters of the Flash (number of wait states, timings, etc.)
- starting commands such as full erase, page erase, page program, NVM bit set, NVM bit clear, etc.
- getting the end status of the last command
- getting error status
- programming interrupts on the end of the last commands or on errors

The Embedded Flash Controller also provides a dual 32-bit prefetch buffer that optimizes 16-bit access to the Flash. This is particularly efficient when the processor is running in Thumb mode.

Two EFCs are embedded in the SAM7S512 to control each bank of 256 Kbytes. Dual plane organization allows concurrent Read and Program. Read from one memory plane may be performed even while program or erase functions are being executed in the other memory plane.

One EFC is embedded in the SAM7S256/128/64/32/321/161/16 to control the single plane 256/128/64/32/16 Kbytes.

8.8.3 Lock Regions

8.8.3.1 SAM7S512

Two Embedded Flash Controllers each manage 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S512 contains 32 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits (or 32 NVM bits) are software programmable through the corresponding EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.2 SAM7S256

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S256 contains 16 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.3 SAM7S128

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S128 contains 8 lock regions and each lock region contains 64 pages of 256 bytes. Each lock region has a size of 16 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.4 SAM7S64

The Embedded Flash Controller manages 16 lock bits to protect 16 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S64 contains 16 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 16 NVM bits are software programmable through the EFC User Interface. The command "Set Lock Bit" enables the protection. The command "Clear Lock Bit" unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.5 SAM7S321/32

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S321/32 contains 8 lock regions and each lock region contains 32 pages of 128 bytes. Each lock region has a size of 4 Kbytes.

If a locked-region's erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

8.8.3.6 SAM7S161/16

The Embedded Flash Controller manages 8 lock bits to protect 8 regions of the flash against inadvertent flash erasing or programming commands. The SAM7S161/16 contains 8 lock regions and each lock region contains 32 pages of 64 bytes. Each lock region has a size of 2 Kbytes.

If a locked-region’s erase or program command occurs, the command is aborted and the LOCKE bit in the MC_FSR register rises and the interrupt line rises if the LOCKE bit has been written at 1 in the MC_FMR register.

The 8 NVM bits are software programmable through the EFC User Interface. The command “Set Lock Bit” enables the protection. The command “Clear Lock Bit” unlocks the lock region.

Asserting the ERASE pin clears the lock bits, thus unlocking the entire Flash.

Table 8-1 summarizes the configuration of the eight devices.

Table 8-1. Flash Configuration Summary

| Device | Lock Regions | Pages per Region | Region Size |
|-------------|--------------|------------------|-------------|
| SAM7S512 | 32 | 64 | 256 bytes |
| SAM7S256 | 16 | 64 | 256 bytes |
| SAM7S128 | 8 | 64 | 256 bytes |
| SAM7S64 | 16 | 32 | 128 bytes |
| SAM7S321/32 | 8 | 32 | 128 bytes |
| SAM7S161/16 | 8 | 32 | 64 bytes |

8.8.4 Security Bit Feature

The SAM7S Series features a security bit, based on a specific NVM Bit. When the security is enabled, any access to the Flash, either through the ICE interface or through the Fast Flash Programming Interface, is forbidden. This ensures the confidentiality of the code programmed in the Flash.

This security bit can only be enabled, through the Command “Set Security Bit” of the EFC User Interface. Disabling the security bit can only be achieved by asserting the ERASE pin at 1, and after a full flash erase is performed. When the security bit is deactivated, all accesses to the flash are permitted.

It is important to note that the assertion of the ERASE pin should always be longer than 50 ms.

As the ERASE pin integrates a permanent pull-down, it can be left unconnected during normal operation. However, it is safer to connect it directly to GND for the final application.

8.8.5 Non-volatile Brownout Detector Control

Two general purpose NVM (GPNVM) bits are used for controlling the brownout detector (BOD), so that even after a power loss, the brownout detector operations remain in their state.

These two GPNVM bits can be cleared or set respectively through the commands “Clear General-purpose NVM Bit” and “Set General-purpose NVM Bit” of the EFC User Interface.

- GPNVM Bit 0 is used as a brownout detector enable bit. Setting the GPNVM Bit 0 enables the BOD, clearing it disables the BOD. Asserting ERASE clears the GPNVM Bit 0 and thus disables the brownout detector by default.
- The GPNVM Bit 1 is used as a brownout reset enable signal for the reset controller. Setting the GPNVM Bit 1 enables the brownout reset when a brownout is detected, Clearing the GPNVM Bit 1 disables the brownout reset. Asserting ERASE disables the brownout reset by default.

8.8.6 Calibration Bits

Eight NVM bits are used to calibrate the brownout detector and the voltage regulator. These bits are factory configured and cannot be changed by the user. The ERASE pin has no effect on the calibration bits.

8.9 Fast Flash Programming Interface

The Fast Flash Programming Interface allows programming the device through either a serial JTAG interface or through a multiplexed fully-handshaked parallel port. It allows gang-programming with market-standard industrial programmers.

The FFPI supports read, page program, page erase, full erase, lock, unlock and protect commands.

The Fast Flash Programming Interface is enabled and the Fast Programming Mode is entered when the TST pin and the PA0 and PA1 pins are all tied high and PA2 is tied low.

8.10 SAM-BA Boot Assistant

The SAM-BA[®] Boot Recovery restores the SAM-BA Boot in the first two sectors of the on-chip Flash memory. The SAM-BA Boot recovery is performed when the TST pin and the PA0, PA1 and PA2 pins are all tied high for 10 seconds. Then, a power cycle of the board is mandatory.

The SAM-BA Boot Assistant is a default Boot Program that provides an easy way to program in situ the on-chip Flash memory.

The SAM-BA Boot Assistant supports serial communication through the DBGU or through the USB Device Port. (The SAM7S32/16 have no USB Device Port.)

- Communication through the DBGU supports a wide range of crystals from 3 to 20 MHz via software auto-detection.
- Communication through the USB Device Port is limited to an 18.432 MHz crystal. (

The SAM-BA Boot provides an interface with SAM-BA Graphic User Interface (GUI).

9. System Controller

The System Controller manages all vital blocks of the microcontroller: interrupts, clocks, power, time, debug and reset.

The System Controller peripherals are all mapped to the highest 4 Kbytes of address space, between addresses 0xFFFF F000 and 0xFFFF FFFF.

[Figure 9-1 on page 26](#) and [Figure 9-2 on page 27](#) show the product specific System Controller Block Diagrams.

[Figure 8-1 on page 20](#) shows the mapping of the of the User Interface of the System Controller peripherals. Note that the memory controller configuration user interface is also mapped within this address space.

Figure 9-1. System Controller Block Diagram (SAM7S512/256/128/64/321/161)

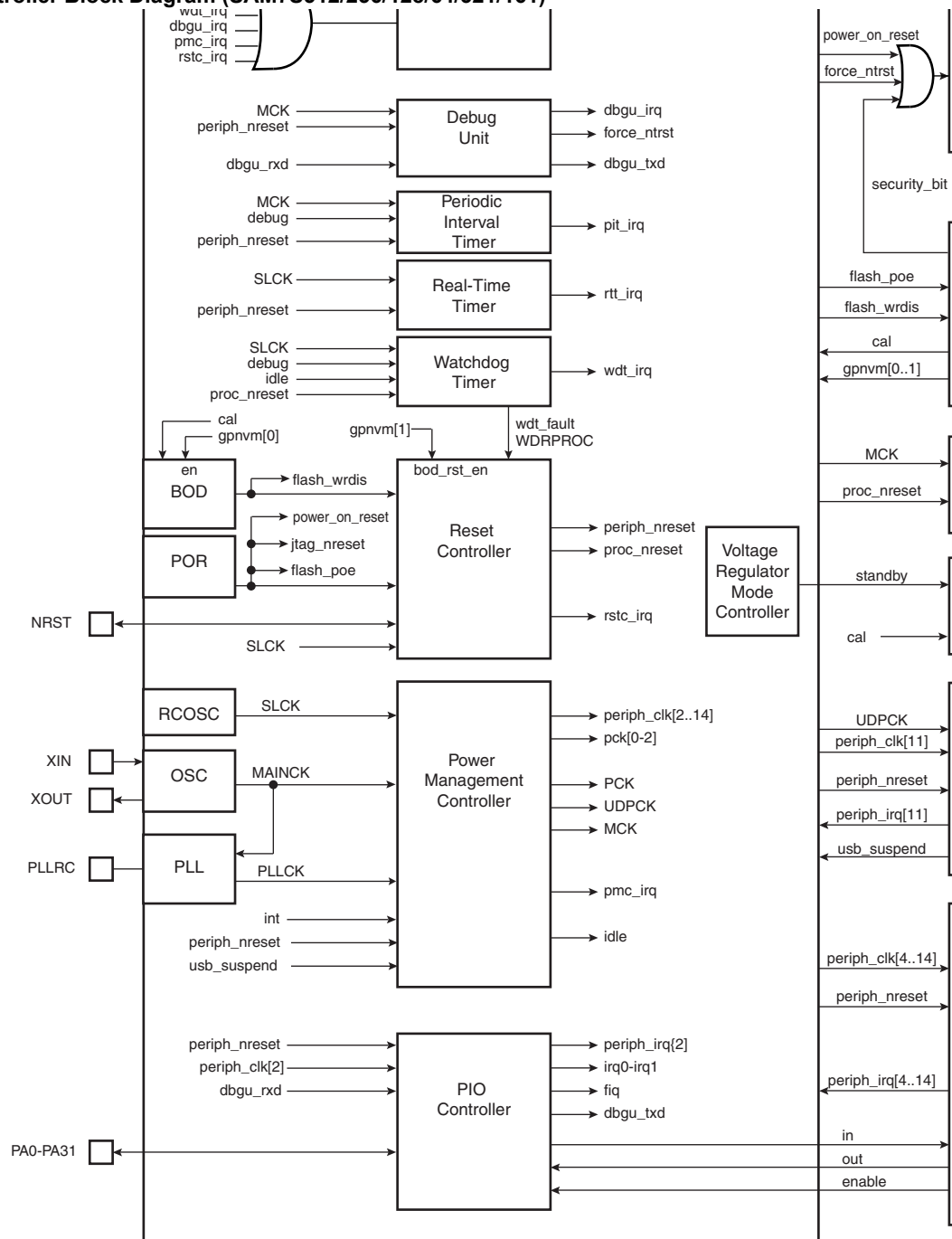
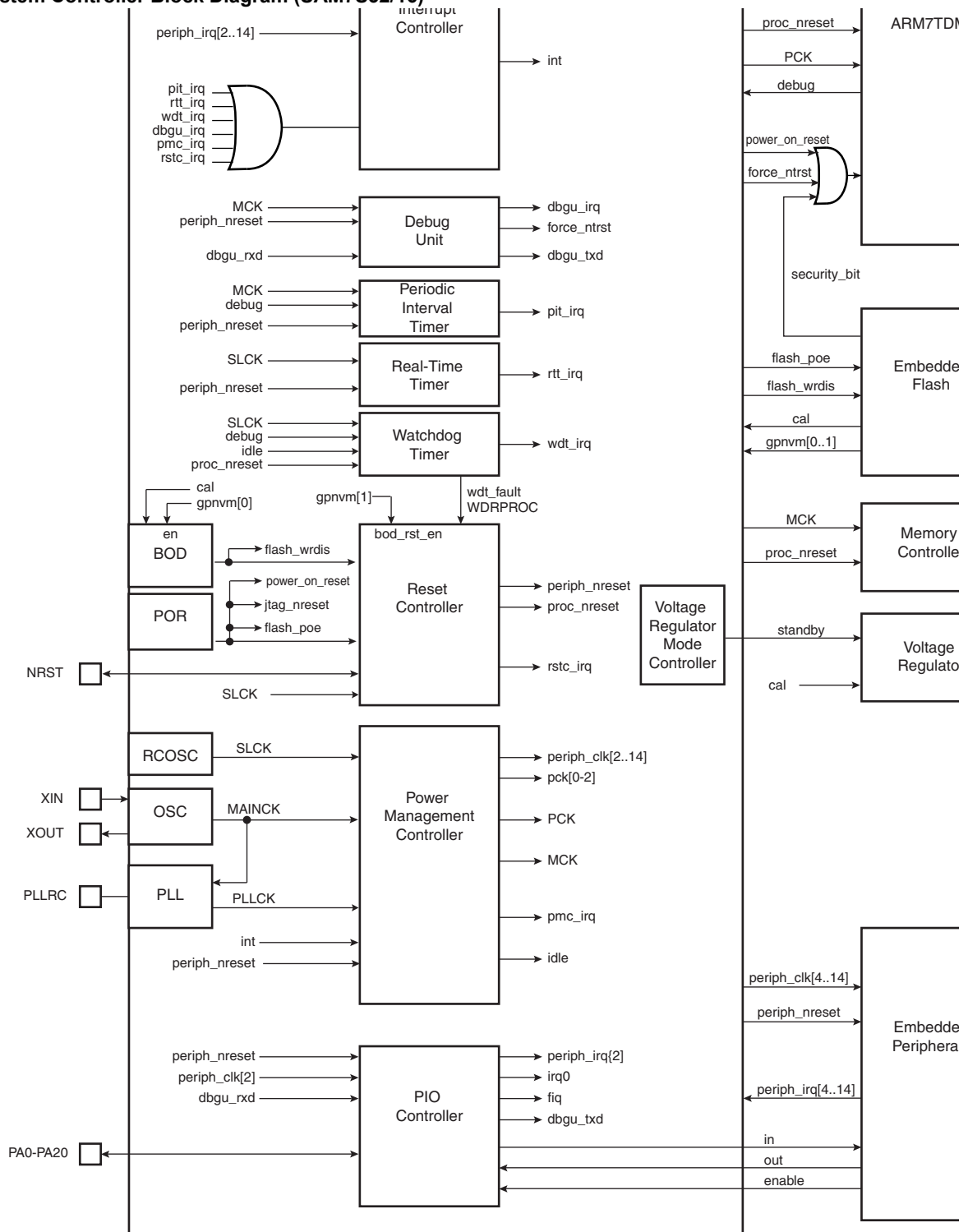


Figure 9-2. System Controller Block Diagram (SAM7S32/16)



9.1 Reset Controller

The Reset Controller is based on a power-on reset cell and one brownout detector. It gives the status of the last reset, indicating whether it is a power-up reset, a software reset, a user reset, a watchdog reset or a brownout reset. In addition, it controls the internal resets and the NRST pin open-drain output. It allows to shape a signal on the NRST line, guaranteeing that the length of the pulse meets any requirement.

Note that if NRST is used as a reset output signal for external devices during power-off, the brownout detector must be activated.

9.1.1 Brownout Detector and Power-on Reset

The SAM7S Series embeds a brownout detection circuit and a power-on reset cell. Both are supplied with and monitor VDDCORE. Both signals are provided to the Flash to prevent any code corruption during power-up or power-down sequences or if brownouts occur on the VDDCORE power supply.

The power-on reset cell has a limited-accuracy threshold at around 1.5V. Its output remains low during power-up until VDDCORE goes over this voltage level. This signal goes to the reset controller and allows a full re-initialization of the device.

The brownout detector monitors the VDDCORE level during operation by comparing it to a fixed trigger level. It secures system operations in the most difficult environments and prevents code corruption in case of brownout on the VDDCORE.

Only VDDCORE is monitored.

When the brownout detector is enabled and VDDCORE decreases to a value below the trigger level (V_{bot-} , defined as $V_{bot} - hyst/2$), the brownout output is immediately activated.

When VDDCORE increases above the trigger level (V_{bot+} , defined as $V_{bot} + hyst/2$), the reset is released. The brownout detector only detects a drop if the voltage on VDDCORE stays below the threshold voltage for longer than about 1 μ s.

The threshold voltage has a hysteresis of about 50 mV, to ensure spike free brownout detection. The typical value of the brownout detector threshold is 1.68V with an accuracy of $\pm 2\%$ and is factory calibrated.

The brownout detector is low-power, as it consumes less than 20 μ A static current. However, it can be deactivated to save its static current. In this case, it consumes less than 1 μ A. The deactivation is configured through the GPNVM bit 0 of the Flash.

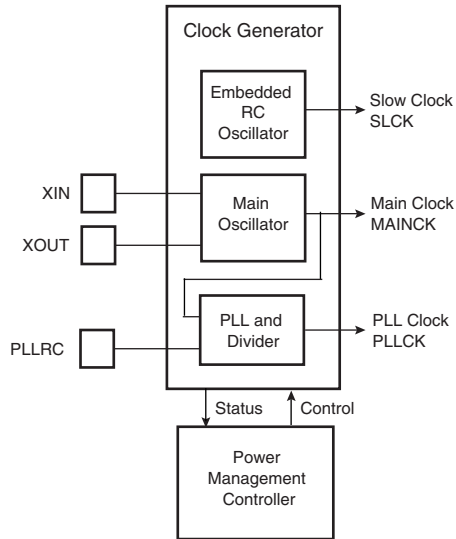
9.2 Clock Generator

The Clock Generator embeds one low-power RC Oscillator, one Main Oscillator and one PLL with the following characteristics:

- RC Oscillator ranges between 22 kHz and 42 kHz
- Main Oscillator frequency ranges between 3 and 20 MHz
- Main Oscillator can be bypassed
- PLL output ranges between 80 and 220 MHz

It provides SLCK, MAINCK and PLLCK.

Figure 9-3. Clock Generator Block Diagram



9.3 Power Management Controller

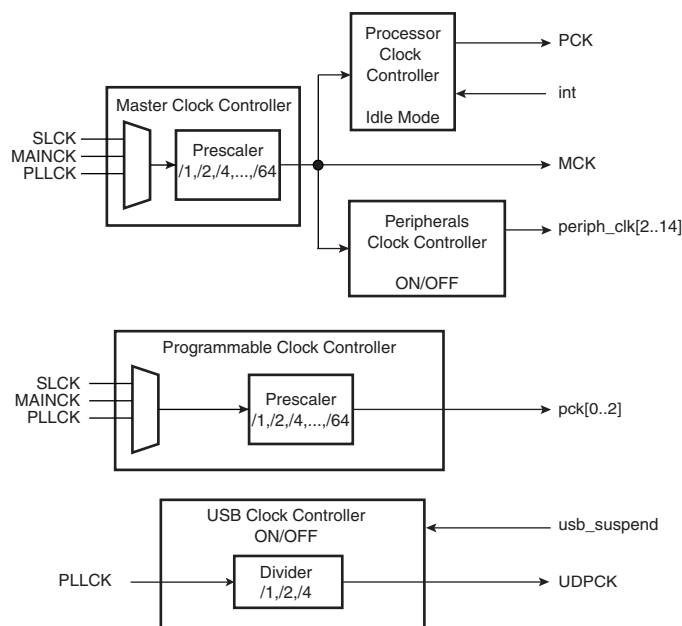
The Power Management Controller uses the Clock Generator outputs to provide:

- the Processor Clock PCK
- the Master Clock MCK
- the USB Clock UDPCK (not present on SAM7S32/16)
- all the peripheral clocks, independently controllable
- three programmable clock outputs

The Master Clock (MCK) is programmable from a few hundred Hz to the maximum operating frequency of the device.

The Processor Clock (PCK) switches off when entering processor idle mode, thus allowing reduced power consumption while waiting for an interrupt.

Figure 9-4. Power Management Controller Block Diagram



9.4 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Individually maskable and vectored interrupt sources
 - Source 0 is reserved for the Fast Interrupt Input (FIQ)
 - Source 1 is reserved for system peripherals RTT, PIT, EFC, PMC, DBGU, etc.)
 - Other sources control the peripheral interrupts or external interrupts
 - Programmable edge-triggered or level-sensitive internal sources
 - Programmable positive/negative edge-triggered or high/low level-sensitive external sources
- 8-level Priority Controller
 - Drives the normal interrupt of the processor
 - Handles priority of the interrupt sources
 - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
 - Optimizes interrupt service routine branch and execution
 - One 32-bit vector register per interrupt source
 - Interrupt vector register reads the corresponding current interrupt vector
- Protect Mode
 - Easy debugging by preventing automatic operations
- Fast Forcing
 - Permits redirecting any interrupt source on the fast interrupt
- General Interrupt Mask
 - Provides processor synchronization on events without triggering an interrupt

9.5 Debug Unit

- Comprises:
 - One two-pin UART
 - One Interface for the Debug Communication Channel (DCC) support

- One set of Chip ID Registers
- One Interface providing ICE Access Prevention
- Two-pin UART
 - Implemented features are compatible with the USART
 - Programmable Baud Rate Generator
 - Parity, Framing and Overrun Error
 - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
- Debug Communication Channel Support
 - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
- Chip ID Registers
 - Identification of the device revision, sizes of the embedded memories, set of peripherals
 - Chip ID is 0x270B0A40 for AT91SAM7S512 Rev A
 - Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B
 - Chip ID is 0x270D0940 for AT91SAM7S256 Rev A
 - Chip ID is 0x270B0941 for AT91SAM7S256 Rev B
 - Chip ID is 0x270B0942 for AT91SAM7S256 Rev C
 - Chip ID is TBD for AT91SAM7S256 Rev D
 - Chip ID is 0x270C0740 for AT91SAM7S128 Rev A
 - Chip ID is 0x270A0741 for AT91SAM7S128 Rev B
 - Chip ID is 0x270A0742 for AT91SAM7S128 Rev C
 - Chip ID is TBD for AT91SAM7S128 Rev D
 - Chip ID is 0x27090540 for AT91SAM7S64 Rev A
 - Chip ID is 0x27090543 for AT91SAM7S64 Rev B
 - Chip ID is 0x27090544 for AT91SAM7S64 Rev C
 - Chip ID is 0x27080342 for AT91SAM7S321 Rev A
 - Chip ID is 0x27080340 for AT91SAM7S32 Rev A
 - Chip ID is 0x27080341 for AT91SAM7S32 Rev B
 - Chip ID is 0x27050241 for AT91SAM7S161 Rev A
 - Chip ID is 0x27050240 for AT91SAM7S16 Rev A

Note: Refer to the errata section of the datasheet for updates on chip ID.

9.6 Periodic Interval Timer

- 20-bit programmable counter plus 12-bit interval counter

9.7 Watchdog Timer

- 12-bit key-protected Programmable Counter running on prescaled SCLK
- Provides reset or interrupt signals to the system
- Counter may be stopped while the processor is in debug state or in idle mode

9.8 Real-time Timer

- 32-bit free-running counter with alarm running on prescaled SCLK
- Programmable 16-bit prescaler for SCLK accuracy compensation

9.9 PIO Controller

- One PIO Controller, controlling 32 I/O lines (21 for SAM7S32/16)
- Fully programmable through set/clear registers
- Multiplexing of two peripheral functions per I/O line
- For each I/O line (whether assigned to a peripheral or used as general-purpose I/O)
 - Input change interrupt
 - Half a clock period glitch filter
 - Multi-drive option enables driving in open drain
 - Programmable pull-up on each I/O line
 - Pin data status register, supplies visibility of the level on the pin at any time
- Synchronous output, provides Set and Clear of several I/O lines in a single write

9.10 Voltage Regulator Controller

The aim of this controller is to select the Power Mode of the Voltage Regulator between Normal Mode (bit 0 is cleared) or Standby Mode (bit 0 is set).

10. Peripherals

10.1 User Interface

The User Peripherals are mapped in the 256 MBytes of address space between 0xF000 0000 and 0xFFFF EFFF. Each peripheral is allocated 16 Kbytes of address space.

A complete memory map is provided in [Figure 8-1 on page 20](#).

10.2 Peripheral Identifiers

The SAM7S Series embeds a wide range of peripherals. [Table 10-1](#) defines the Peripheral Identifiers of the SAM7S512/256/128/64/321/161. [Table 10-2](#) defines the Peripheral Identifiers of the SAM7S32/16. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. Peripheral Identifiers (SAM7S512/256/128/64/321/161)

| | | | |
|---------|---------------------|-------------------------------|------|
| 0 | AIC | Advanced Interrupt Controller | FIQ |
| 1 | SYSC ⁽¹⁾ | System | |
| 2 | PIOA | Parallel I/O Controller A | |
| 3 | Reserved | | |
| 4 | ADC ⁽¹⁾ | Analog-to Digital Converter | |
| 5 | SPI | Serial Peripheral Interface | |
| 6 | US0 | USART 0 | |
| 7 | US1 | USART 1 | |
| 8 | SSC | Synchronous Serial Controller | |
| 9 | TWI | Two-wire Interface | |
| 10 | PWMC | PWM Controller | |
| 11 | UDP | USB Device Port | |
| 12 | TC0 | Timer/Counter 0 | |
| 13 | TC1 | Timer/Counter 1 | |
| 14 | TC2 | Timer/Counter 2 | |
| 15 - 29 | Reserved | | |
| 30 | AIC | Advanced Interrupt Controller | IRQ0 |
| 31 | AIC | Advanced Interrupt Controller | IRQ1 |

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

Note: 1. Setting SYSC and ADC bits in the clock set/clear registers of the PMC has no effect. The System Controller is continuously clocked. The ADC clock is automatically started for the first conversion. In Sleep Mode the ADC clock is automatically stopped after each conversion.

Table 10-2. Peripheral Identifiers (SAM7S32/16)

| | | | |
|---------|---------------------|-------------------------------|------|
| 0 | AIC | Advanced Interrupt Controller | FIQ |
| 1 | SYSC ⁽¹⁾ | System | |
| 2 | PIOA | Parallel I/O Controller A | |
| 3 | Reserved | | |
| 4 | ADC ⁽¹⁾ | Analog-to Digital Converter | |
| 5 | SPI | Serial Peripheral Interface | |
| 6 | US | USART | |
| 7 | Reserved | | |
| 8 | SSC | Synchronous Serial Controller | |
| 9 | TWI | Two-wire Interface | |
| 10 | PWMC | PWM Controller | |
| 11 | Reserved | | |
| 12 | TC0 | Timer/Counter 0 | |
| 13 | TC1 | Timer/Counter 1 | |
| 14 | TC2 | Timer/Counter 2 | |
| 15 - 29 | Reserved | | |
| 30 | AIC | Advanced Interrupt Controller | IRQ0 |
| 31 | Reserved | | |

10.3 Peripheral Multiplexing on PIO Lines

The SAM7S Series features one PIO controller, PIOA, that multiplexes the I/O lines of the peripheral set.

PIO Controller A controls 32 lines (21 lines for SAM7S32/16). Each line can be assigned to one of two peripheral functions, A or B. Some of them can also be multiplexed with the analog inputs of the ADC Controller.

[Table 10-3, “Multiplexing on PIO Controller A \(SAM7S512/256/128/64/321/161\),” on page 35](#) and [Table 10-4, “Multiplexing on PIO Controller A \(SAM7S32/16\),” on page 36](#) define how the I/O lines of the peripherals A, B or the analog inputs are multiplexed on the PIO Controller A. The two columns “Function” and “Comments” have been inserted for the user’s own comments; they may be used to track how pins are defined in an application.

Note that some peripheral functions that are output only may be duplicated in the table.

All pins reset in their Parallel I/O lines function are configured as input with the programmable pull-up enabled, so that the device is maintained in a static state as soon as a reset is detected.

10.4 PIO Controller A Multiplexing

Table 10-3. Multiplexing on PIO Controller A (SAM7S512/256/128/64/321/161)

| PA | Function | Function | Drive | | |
|------|----------|----------|------------|--|--|
| PA0 | PWM0 | TIOA0 | High-Drive | | |
| PA1 | PWM1 | TIOB0 | High-Drive | | |
| PA2 | PWM2 | SCK0 | High-Drive | | |
| PA3 | TWD | NPCS3 | High-Drive | | |
| PA4 | TWCK | TCLK0 | | | |
| PA5 | RXD0 | NPCS3 | | | |
| PA6 | TXD0 | PCK0 | | | |
| PA7 | RTS0 | PWM3 | | | |
| PA8 | CTS0 | ADTRG | | | |
| PA9 | DRXD | NPCS1 | | | |
| PA10 | DTXD | NPCS2 | | | |
| PA11 | NPCS0 | PWM0 | | | |
| PA12 | MISO | PWM1 | | | |
| PA13 | MOSI | PWM2 | | | |
| PA14 | SPCK | PWM3 | | | |
| PA15 | TF | TIOA1 | | | |
| PA16 | TK | TIOB1 | | | |
| PA17 | TD | PCK1 | AD0 | | |
| PA18 | RD | PCK2 | AD1 | | |
| PA19 | RK | FIQ | AD2 | | |
| PA20 | RF | IRQ0 | AD3 | | |
| PA21 | RXD1 | PCK1 | | | |
| PA22 | TXD1 | NPCS3 | | | |
| PA23 | SCK1 | PWM0 | | | |
| PA24 | RTS1 | PWM1 | | | |
| PA25 | CTS1 | PWM2 | | | |
| PA26 | DCD1 | TIOA2 | | | |
| PA27 | DTR1 | TIOB2 | | | |
| PA28 | DSR1 | TCLK1 | | | |
| PA29 | RI1 | TCLK2 | | | |
| PA30 | IRQ1 | NPCS2 | | | |
| PA31 | NPCS1 | PCK2 | | | |

Table 10-4. Multiplexing on PIO Controller A (SAM7S32/16)

| PA0 | PWM0 | TIOA0 | High-Drive | | |
|------|-------|-------|------------|--|--|
| PA1 | PWM1 | TIOB0 | High-Drive | | |
| PA2 | PWM2 | SCK0 | High-Drive | | |
| PA3 | TWD | NPCS3 | High-Drive | | |
| PA4 | TWCK | TCLK0 | | | |
| PA5 | RXD0 | NPCS3 | | | |
| PA6 | TXD0 | PCK0 | | | |
| PA7 | RTS0 | PWM3 | | | |
| PA8 | CTS0 | ADTRG | | | |
| PA9 | DRXD | NPCS1 | | | |
| PA10 | DTXD | NPCS2 | | | |
| PA11 | NPCS0 | PWM0 | | | |
| PA12 | MISO | PWM1 | | | |
| PA13 | MOSI | PWM2 | | | |
| PA14 | SPCK | PWM3 | | | |
| PA15 | TF | TIOA1 | | | |
| PA16 | TK | TIOB1 | | | |
| PA17 | TD | PCK1 | AD0 | | |
| PA18 | RD | PCK2 | AD1 | | |
| PA19 | RK | FIQ | AD2 | | |
| PA20 | RF | IRQ0 | AD3 | | |

10.5 Serial Peripheral Interface

- Supports communication with external serial devices
 - Four chip selects with external decoder allow communication with up to 15 peripherals
 - Serial memories, such as DataFlash[®] and 3-wire EEPROMs
 - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
 - External co-processors
- Master or slave serial peripheral bus interface
 - 8- to 16-bit programmable data length per chip select
 - Programmable phase and polarity per chip select
 - Programmable transfer delays between consecutive transfers and between clock and data per chip select
 - Programmable delay between consecutive transfers
 - Selectable mode fault detection
 - Maximum frequency at up to Master Clock

10.6 Two-wire Interface

- Master Mode only (SAM7S512/256/128/64/321/32)
- Master, Multi-Master and Slave Mode support (SAM7S161/16)
- General Call supported in Slave Mode (SAM7S161/16)
- Compatibility with I²C compatible devices (refer to the TWI sections of the datasheet)
- One, two or three bytes internal address registers for easy Serial Memory access
- 7-bit or 10-bit slave addressing
- Sequential read/write operations

10.7 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
 - 1, 1.5 or 2 stop bits in Asynchronous Mode
 - 1 or 2 stop bits in Synchronous Mode
 - Parity generation and error detection
 - Framing error detection, overrun error detection
 - MSB or LSB first
 - Optional break generation and detection
 - By 8 or by 16 over-sampling receiver frequency
 - Hardware handshaking RTS - CTS
 - Modem Signals Management DTR-DSR-DCD-RI on USART1 (not present on SAM7S32/16)
 - Receiver time-out and transmitter timeguard
 - Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
 - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
 - Communication at up to 115.2 Kbps
- Test Modes
 - Remote Loopback, Local Loopback, Automatic Echo

10.8 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.9 Timer Counter

- Three 16-bit Timer Counter Channels
 - Two output compare or one input capture per channel (except for SAM7S32/16 which have only two channels connected to the PIO)
- Wide range of functions including:
 - Frequency measurement
 - Event counting
 - Interval measurement
 - Pulse generation
 - Delay timing
 - Pulse Width Modulation
 - Up/down capabilities
- Each channel is user-configurable and contains:
 - Three external clock inputs (The SAM7S32/16 have one)
 - Five internal clock inputs, as defined in [Table 10-5](#)

Table 10-5. Timer Counter Clocks Assignment

| | |
|--------------|----------|
| TIMER_CLOCK1 | MCK/2 |
| TIMER_CLOCK2 | MCK/8 |
| TIMER_CLOCK3 | MCK/32 |
| TIMER_CLOCK4 | MCK/128 |
| TIMER_CLOCK5 | MCK/1024 |

- Two multi-purpose input/output signals
- Two global registers that act on all three TC channels

10.10 PWM Controller

- Four channels, one 16-bit counter per channel
- Common clock generator, providing thirteen different clocks
 - One Modulo n counter providing eleven clocks
 - Two independent linear dividers working on modulo n counter outputs
- Independent channel programming
 - Independent enable/disable commands
 - Independent clock selection
 - Independent period and duty cycle, with double buffering
 - Programmable selection of the output waveform polarity

- Programmable center or left aligned output waveform

10.11 USB Device Port (Does not pertain to SAM7S32/16)

- USB V2.0 full-speed compliant, 12 Mbits per second.
- Embedded USB V2.0 full-speed transceiver
- Embedded 328-byte dual-port RAM for endpoints
- Four endpoints
 - Endpoint 0: 8 bytes
 - Endpoint 1 and 2: 64 bytes ping-pong
 - Endpoint 3: 64 bytes
 - Ping-pong Mode (two memory banks) for isochronous and bulk endpoints
- Suspend/resume logic

10.12 Analog-to-digital Converter

- 8-channel ADC
- 10-bit 384 Ksamples/sec. or 8-bit 583 Ksamples/sec. Successive Approximation Register ADC
- ± 2 LSB Integral Non Linearity, ± 1 LSB Differential Non Linearity
- Integrated 8-to-1 multiplexer, offering eight independent 3.3V analog inputs
- External voltage reference for better accuracy on low voltage inputs
- Individual enable and disable of each channel
- Multiple trigger source
 - Hardware or software trigger
 - External trigger pin
 - Timer Counter 0 to 2 outputs TIOA0 to TIOA2 trigger
- Sleep Mode and conversion sequencer
 - Automatic wakeup on trigger and back to sleep mode after conversions of all enabled channels
- Four of eight analog inputs shared with digital signals

11. Package Drawings

The SAM7S series devices are available in LQFP and QFN package types.

11.1 LQFP Packages

Figure 11-1. 48-and 64-lead LQFP Package Drawing

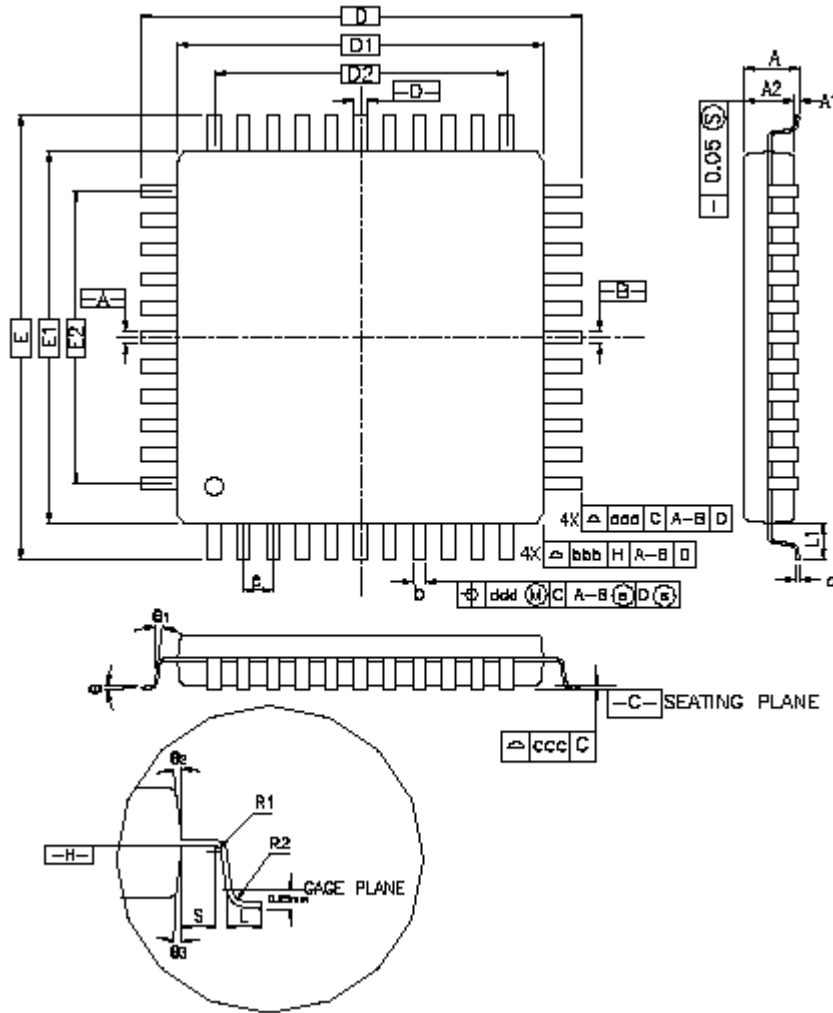


Table 11-1. 48-lead LQFP Package Dimensions (in mm)

| Symbol | | | | | | |
|---------------------------------|-----------|------|------|------------|-------|-------|
| | | | | | | |
| A | – | – | 1.60 | – | – | 0.063 |
| A1 | 0.05 | – | 0.15 | 0.002 | – | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 9.00 BSC | | | 0.354 BSC | | |
| D1 | 7.00 BSC | | | 0.276 BSC | | |
| E | 9.00 BSC | | | 0.354 BSC | | |
| E1 | 7.00 BSC | | | 0.276 BSC | | |
| R2 | 0.08 | – | 0.20 | 0.003 | – | 0.008 |
| R1 | 0.08 | – | – | 0.003 | – | – |
| q | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ_1 | 0° | – | – | 0° | – | – |
| θ_2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ_3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | – | 0.20 | 0.004 | – | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | – | – | 0.008 | – | – |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 5.50 | | | 0.217 | | |
| E2 | 5.50 | | | 0.217 | | |
| Tolerances of Form and Position | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

Table 11-2. 64-lead LQFP Package Dimensions (in mm)

| Symbol | | | | | | |
|---------------------------------|-----------|------|------|------------|-------|-------|
| A | – | – | 1.60 | – | – | 0.063 |
| A1 | 0.05 | – | 0.15 | 0.002 | – | 0.006 |
| A2 | 1.35 | 1.40 | 1.45 | 0.053 | 0.055 | 0.057 |
| D | 12.00 BSC | | | 0.472 BSC | | |
| D1 | 10.00 BSC | | | 0.383 BSC | | |
| E | 12.00 BSC | | | 0.472 BSC | | |
| E1 | 10.00 BSC | | | 0.383 BSC | | |
| R2 | 0.08 | – | 0.20 | 0.003 | – | 0.008 |
| R1 | 0.08 | – | – | 0.003 | – | – |
| q | 0° | 3.5° | 7° | 0° | 3.5° | 7° |
| θ_1 | 0° | – | – | 0° | – | – |
| θ_2 | 11° | 12° | 13° | 11° | 12° | 13° |
| θ_3 | 11° | 12° | 13° | 11° | 12° | 13° |
| c | 0.09 | – | 0.20 | 0.004 | – | 0.008 |
| L | 0.45 | 0.60 | 0.75 | 0.018 | 0.024 | 0.030 |
| L1 | 1.00 REF | | | 0.039 REF | | |
| S | 0.20 | – | – | 0.008 | – | – |
| b | 0.17 | 0.20 | 0.27 | 0.007 | 0.008 | 0.011 |
| e | 0.50 BSC. | | | 0.020 BSC. | | |
| D2 | 7.50 | | | 0.285 | | |
| E2 | 7.50 | | | 0.285 | | |
| Tolerances of Form and Position | | | | | | |
| aaa | 0.20 | | | 0.008 | | |
| bbb | 0.20 | | | 0.008 | | |
| ccc | 0.08 | | | 0.003 | | |
| ddd | 0.08 | | | 0.003 | | |

11.2 QFN Packages

Figure 11-2. 48-pad QFN Package

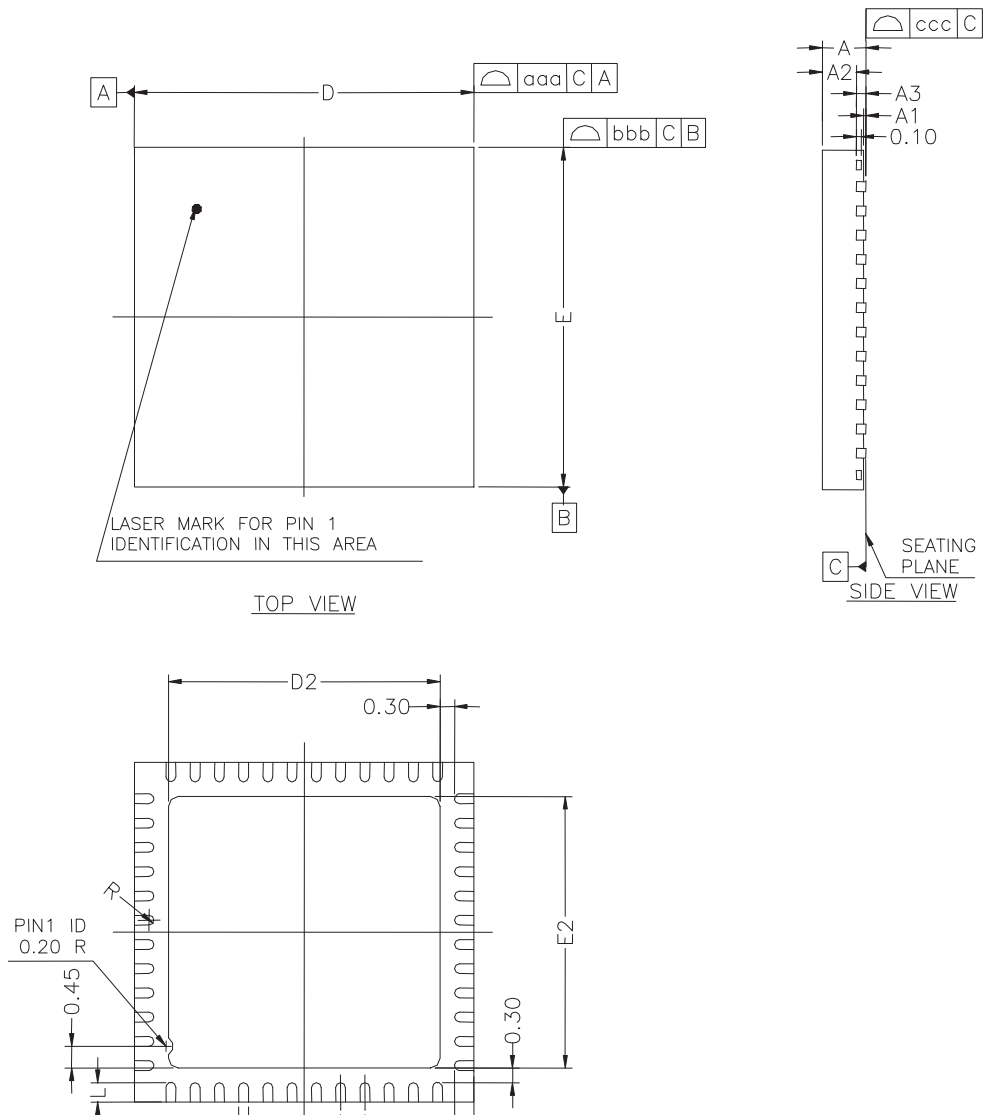


Table 11-3. 48-pad QFN Package Dimensions (in mm)

| Symbol | | | | | | |
|---------------------------------|----------|------|-------|-----------|-------|-------|
| | | | | | | |
| A | – | – | 090 | – | – | 0.035 |
| A1 | – | – | 0.050 | – | – | 0.002 |
| A2 | – | 0.65 | 0.70 | – | 0.026 | 0.028 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.18 | 0.20 | 0.23 | 0.007 | 0.008 | 0.009 |
| D | 7.00 bsc | | | 0.276 bsc | | |
| D2 | 5.45 | 5.60 | 5.75 | 0.215 | 0.220 | 0.226 |
| E | 7.00 bsc | | | 0.276 bsc | | |
| E2 | 5.45 | 5.60 | 5.75 | 0.215 | 0.220 | 0.226 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| e | 0.50 bsc | | | 0.020 bsc | | |
| R | 0.09 | – | – | 0.004 | – | – |
| Tolerances of Form and Position | | | | | | |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.10 | | | 0.004 | | |
| ccc | 0.05 | | | 0.002 | | |

Figure 11-3. 64-pad QFN Package Drawing

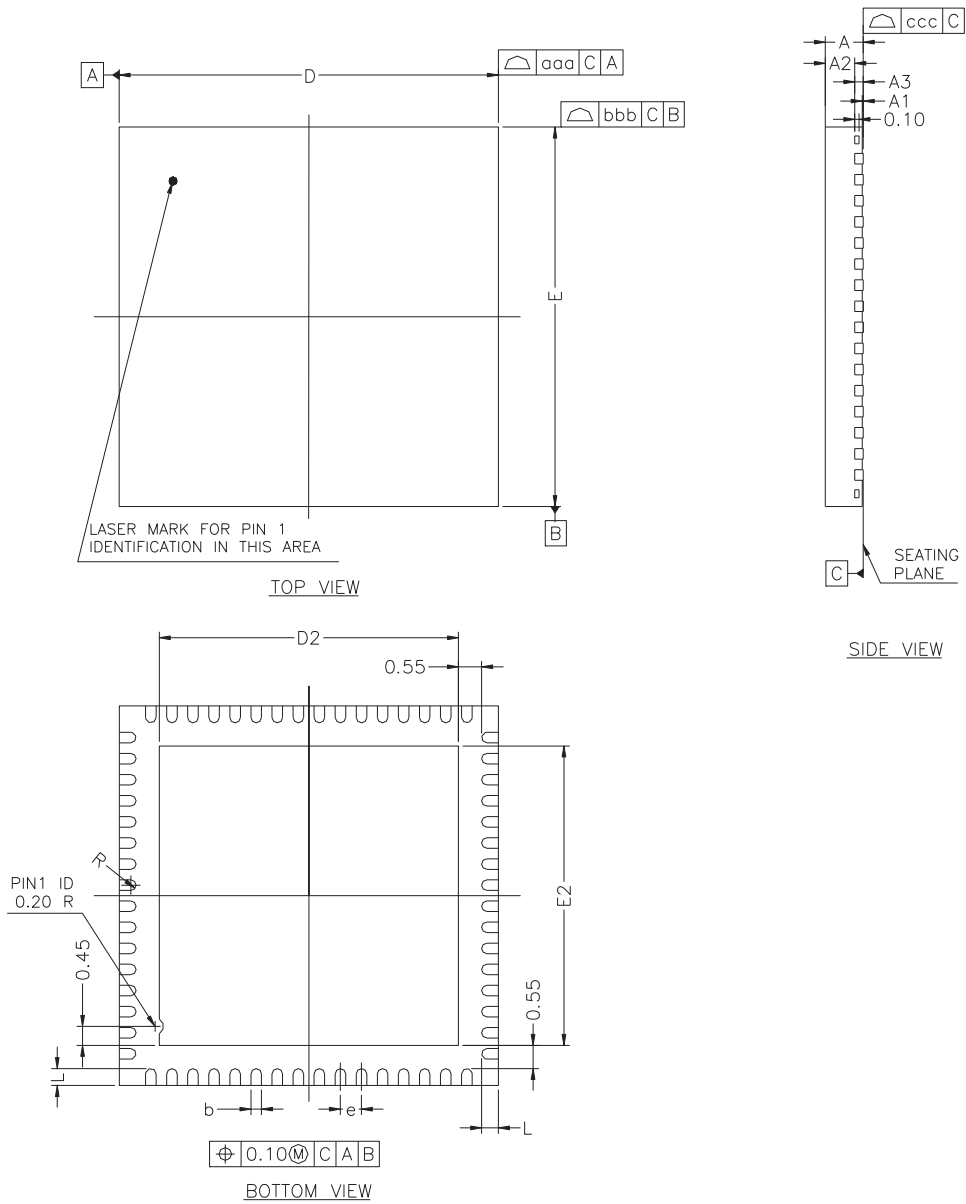


Table 11-4. 64-pad QFN Package Dimensions (in mm)

| Symbol | | | | | | |
|---------------------------------|----------|------|------|-----------|-------|-------|
| A | – | – | 090 | – | – | 0.035 |
| A1 | – | – | 0.05 | – | – | 0.001 |
| A2 | – | 0.65 | 0.70 | – | 0.026 | 0.028 |
| A3 | 0.20 REF | | | 0.008 REF | | |
| b | 0.23 | 0.25 | 0.28 | 0.009 | 0.010 | 0.011 |
| D | 9.00 bsc | | | 0.354 bsc | | |
| D2 | 6.95 | 7.10 | 7.25 | 0.274 | 0.280 | 0.285 |
| E | 9.00 bsc | | | 0.354 bsc | | |
| E2 | 6.95 | 7.10 | 7.25 | 0.274 | 0.280 | 0.285 |
| L | 0.35 | 0.40 | 0.45 | 0.014 | 0.016 | 0.018 |
| e | 0.50 bsc | | | 0.020 bsc | | |
| R | 0.125 | – | – | 0.0005 | – | – |
| Tolerances of Form and Position | | | | | | |
| aaa | 0.10 | | | 0.004 | | |
| bbb | 0.10 | | | 0.004 | | |
| ccc | 0.05 | | | 0.002 | | |

12. SAM7S Ordering Information

Table 12-1. SAM7S Series Ordering Information

| MLR A Ordering Code | MLR B Ordering Code | MLR C Ordering Code | MLR D Ordering Code | Package | Package Type | Temperature Operating Range |
|--------------------------------------|--|--------------------------------------|--------------------------------------|-------------------|--------------|-------------------------------|
| AT91SAM7S16-AU AT91SAM7S16-MU | – | – | – | LQFP 48 QFN 48 | Green | Industrial (-40 C to 85 C) |
| AT91SAM7S161-AU | – | – | – | LQFP 64 | Green | Industrial (-40 C to 85 C) |
| AT91SAM7S32-AU-001 AT91SAM7S32-MU | AT91SAM7S32B-AU AT91SAM7S32B-MU | | | LQFP 48 QFN 48 | Green | Industrial (-40 C to 85 C) |
| AT91SAM7S321-AU AT91SAM7S321-MU | – | – | – | LQFP 64 QFN 64 | Green | Industrial (-40 C to 85 C) |
| – | AT91SAM7S64B-AU AT91SAM7S64B-MU | AT91SAM7S64C-AU AT91SAM7S64C-MU | – | LQFP 64 QFN 64 | Green | Industrial (-40 C to 85 C) |
| – | AT91SAM7S128-AU-001 AT91SAM7S128-MU | AT91SAM7S128C-AU AT91SAM7S128C-MU | AT91SAM7S128D-AU AT91SAM7S128D-MU | LQFP 64 QFN 64 | Green | Industrial (-40 C to 85 C) |
| – | AT91SAM7S256-AU-001 AT91SAM7S256-MU | AT91SAM7S256C-AU AT91SAM7S256C-MU | AT91SAM7S256D-AU AT91SAM7S256D-MU | LQFP 64 QFN 64 | Green | Industrial (-40 C to 85 C) |
| AT91SAM7S512-AU AT91SAM7S512-MU | AT91SAM7S512B-AU AT91SAM7S512B-MU | – | – | LQFP 64 QFN 64 | Green | Industrial (-40 C to 85 C) |

Revision History

| | | |
|--------|---|--|
| | | |
| 6175AS | First issue - Unqualified on Intranet Corresponds to 6175A full datasheet approval loop. Qualified on Intranet. | |
| 6175BS | Section 8. "Memories" on page 18 updated: 2 ms => 3 ms, 10 ms => 15 ms, 4 ms => 6 ms | CSR05-529 |
| 6175CS | Section 12. "SAM7S Ordering Information" AT91SAM7S321 changed in Table 12-1 on page 47 | #2342 |
| 6175DS | "Features", Table 1-1, "Configuration Summary," on page 3 , Section 4. "Package and Pinout" Section 12. "SAM7S Ordering Information" QFN package information added | #2444 |
| 6175ES | Section 10.11 on page 39 USB Device port, Ping-pong Mode includes Isochronous endpoints. "Features" on page 1 , and global: AT91SAM7S512 added to series. Reference to Manchester Encoder removed from USART. Section 8. "Memories" Reformatted Memories, Consolidated Memory Mapping in Figure 8-1 on page 20 Section 10. "Peripherals" Reordered sub sections. Section 11. "Package Drawings" QFN, LQFP package drawings added. "ice_nreset" signals changed to "power_on_reset" in System Controller block diagrams, Figure 9-1 on page 26 and Figure 9-2 on page 27 . Section 4. "Package and Pinout" LQFP and QFN Package Outlines replace Mechanical Overview. Section 10.1 "User Interface" , User peripherals are mapped between 0xF000 0000 and 0xFFFF EFFF. SYSIRQ changed to SYSC in "Peripheral Identifiers" Table 10-1 and Table 10-2 | specs #2748 #2832 (DBGU IP) rfo review |
| 6175FS | AT91SAM7S161 and AT91SAM7S16 added to product family Features: Timer Counter, on page 2 product specific information rewritten, Table 1-1, "Configuration Summary," on page 3 , footnote explains TC on AT91SAM7S32/16 has only two channels accessible via PIO, and in Section 10.9 "Timer Counter" , precisions added to "compare and capture" output/input. Section 10.6 "Two-wire Interface" , updated reference to I ² C compatibility, internal address registers, slave addressing, Modes for AT91SAM7S161/16 "One Two-wire Interface (TWI)" on page 2 , updated in Features Section 10.12 "Analog-to-digital Converter" , updated Successive Approximation Register ADC and the INL, DNL ± values of LSB. Section 8.8.3 "Lock Regions" , locked-region's erase or program command updated Section 9.5 "Debug Unit" , Chip ID updated. Section 6. "I/O Lines Considerations" , JTAG Port Pin, Test Pin, Erase Pin, updated. | BDs 4208 rfo review 4325 5063 |

| | | |
|--------|---|--|
| | | |
| 6175GS | <p>“Features” ,“Debug Unit (DBGU)” updated with “Mode for General Purpose 2-wire UART Serial Communication”</p> <p>Section 7.4 “Peripheral DMA Controller”, added list of PDC priorities.</p> <p>Section 9. “System Controller”, Figure 9-1 and Figure 9-2 RTT is reset by “power_on_reset”.</p> <p>Section 9.1.1 “Brownout Detector and Power-on Reset”, fourth paragraph reduced.</p> <p>Section 9.5 “Debug Unit”, the list; Section I “Chip ID Registers”, chip IDs updated, added SAM7S32 Rev B and SAM7S64 Rev B to the list.</p> <p>Section 12. “SAM7S Ordering Information”, Updated product ordering information by MRL A and MRL B versions.</p> | <p>5846</p> <p>5913</p> <p>5224</p> <p>5685</p> <p>rfo</p> |
| 6175HS | <p>Section 6.2 “Test Pin”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory.</p> <p>Section 8.10 “SAM-BA Boot Assistant”, added to SAM-BA Boot recovery procedure, a power cycle of the board is mandatory.</p> | 6068 |
| 6175IS | <p>Section 9.5 “Debug Unit”, Chip ID Registers list updated.</p> <p>MRL C column added to Table 12-1, “SAM7S Series Ordering Information”.</p> | 7185 |
| 6175JS | <p>Product Series Naming Convention</p> <p>Except for part ordering and library references, AT91 prefix dropped from most nomenclature.</p> <p>AT91SAM7S becomes SAM7S.</p> <p>Debug Unit:</p> <p>“Chip ID Registers” on page 31, Chip ID is 0x270B0A4F for AT91SAM7S512 Rev B</p> | <p>rfo</p> <p>7945</p> |
| 6175KS | <p>Section 9.5 “Debug Unit”, Chip ID Registers list updated. Added Chip ID for SAM7S128 Rev D and SAM7S256 Rev D</p> <p>Table 12-1, “SAM7S Series Ordering Information”.Added SAM7S128 Rev D and SAM7S256 Rev D</p> | 8380/8467 |



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