



**THE DATASHEET OF  
ISL59837IAZ-EVALZ**



ISL59837

200MHz Single Supply Video Driver With Charge Pump and Power Down

FN6335  
Rev 1.00  
March 5, 2007

The ISL59837 is a revolutionary device that allows true single-supply operation of video amplifiers. Designed for systems requiring output swing below ground but lacking a negative power supply, the ISL59837 generates the required negative rail internally from a +3.3V power supply. This allows for DC-accurate coupling of video onto a 75Ω double-terminated line. The buffers have an integrated 6dB, eliminating the need for external gain-setting resistors. An external reference voltage can be applied to the REF pin to shift the analog video level down by the desired amount. The charge pump and amplifiers can be placed in a power down mode, consuming less than 1mA of current.

**Ordering Information**

PART NUMBER (Note)	PART MARKING	TAPE & REEL	PACKAGE (Pb-free)	PKG. DWG. #
ISL59837IAZ	59837 IAZ	-	16 Ld QSOP	MDP0040
ISL59837IAZ-T7	59837 IAZ	7"	16 Ld QSOP	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

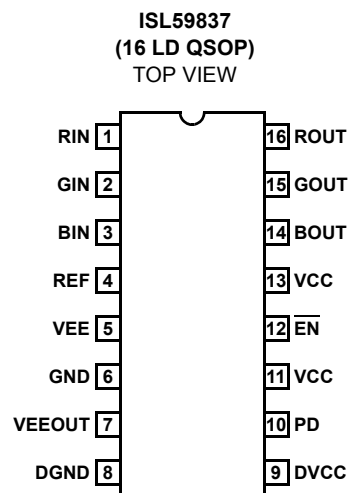
**Features**

- Triple single-supply buffer
- Generates negative rail from from single +3.3V supply
- No output DC blocking capacitor needed
- 200MHz -3dB bandwidth
- 50MHz 0.1dB bandwidth
- Fixed gain of 2 output buffer
- Charge pump power down function (0.1mA typical)
- Outputs are high impedance in power-down mode
- Amplifier enable/disable function control
- Pb-free plus anneal available (RoHS compliant)

**Applications**

- Driving video

**Pinout**



**Absolute Maximum Ratings**

$V_{CC}$ , Supply Voltage between $V_S$ and GND	.5V
$V_{IN}$ , $V_{REF}$	$V_{CC} + 0.3V$ , $V_{EE} - 0.3V$
Voltage between $V_{IN}$ and $V_{REF}$	$\pm 2V$
Maximum Continuous Output Current	30mA
ESD Classification	
Human Body Model	2000V
Machine Model	200V

**Thermal Information**

Operating Temperature	-40°C to +85°C
Maximum Die Temperature	+150°C
Storage Temperature	-65°C to +150°C
Lead Temperature	+260°C
Power Dissipation	See Curves
Pb-free reflow profile	see link below <a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

**AC Electrical Specifications**  $V_{CC} = DV_{CC} = +3.3V$ , REF = GND,  $T_A = +25^\circ C$ ,  $R_L = 150\Omega$ , unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
BW - 3dB	3dB Bandwidth	$V_{OUT} = 200mV_{PP}$		200		MHz
		$V_{OUT} = 2V_{PP}$		100		MHz
BW 0.1dB	0.1dB Bandwidth	$V_{OUT} = 2V_{PP}$		50		MHz
$S_R$	Slew Rate	$V_{IN} = 2V_{PP}$	500			V/ $\mu s$
$d_G$	Differential Gain			0.07		%
$d_P$	Differential Phase			0.06		°
$X_T$	Hostile Crosstalk	6MHz		-90		dB
I	Input to Output Isolation	6MHz		-70		dB
$V_N$	Input Noise Voltage			20		nV/ $\sqrt{Hz}$
$f_{CP}$	Charge Pump Switching Frequency			168		MHz
Load Reg	$V_{EE}$ Load Regulation	$I_{EE} = 0mA$ to 10mA		9	30	mV
$V_{RIPPLE}$	Output Amp Ripple Voltage			30		mV
		With Bead Core to $DV_{CC}$		10		mV

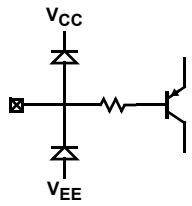
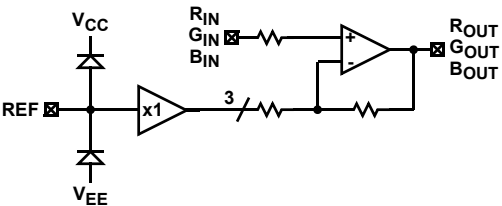
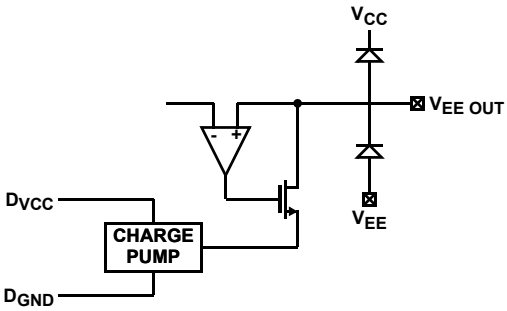
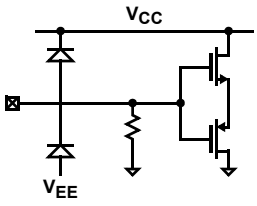
**DC Electrical Specifications**  $V_{CC} = DV_{CC} = +3.3V$ , REF = GND,  $T_A = +25^\circ C$ ,  $R_L = 150\Omega$ , unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V+	Supply Range		3.0		3.6	V
$V_G\%$	Gain Error	$R_L = 150\Omega$ , $V_{OUT} = -1V$ to +2.5V			1.5	%
$\Delta G$	Gain Matching	$R_L = 150\Omega$		0.5		%
$I_{IN}$	Analog Input Leakage Current	$V_{IN} = 0V$ to 1.5V		$\pm 0.1$	$\pm 1$	$\mu A$
$V_{OS}$	Output Offset Voltage	$V_{REF} = 0$	-25	7	+25	mV
$V_{OUT+}$	Maximum Output Voltage	$R_L = 75\Omega$	2.4	2.5		V
		$R_L = 150\Omega$	2.7	2.9		V
$V_{OUT-}$	Minimum Output Voltage	$R_L = 75\Omega$			-1	V
		$R_L = 150\Omega$			-1.2	V
$I_{OUT+}$	Output Current	$R_L = 10\Omega$ , $V_{IN} = 1.2V$	50	80		mA
$I_{OUT-}$	Output Current	$R_L = 10\Omega$ , $V_{IN} = -0.3V$		-40	-18	mA
$Z_{OUT}$	Disabled Output Impedance	$\overline{EN} = 3.3V$ and/or PD = 3.3V (Amp Disabled)		500		k $\Omega$
$I_{REF}$	Reference Input Leakage Current		1	2.3	3.5	$\mu A$
PSRR	Power Supply Rejection Ratio		50	62		dB

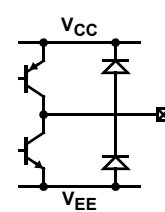
**DC Electrical Specifications**  $V_{CC} = DV_{CC} = +3.3V$ ,  $REF = GND$ ,  $T_A = +25^{\circ}C$ ,  $R_L = 150\Omega$ , unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$I_S$	Supply Current	$\overline{EN} = PD = GND$ (Amp Enabled)		97	130	mA
		$\overline{EN} = 3.3V$ (Amp Disabled)		60	90	mA
$I_{S\_PD}$	Power Down Supply Current	$\overline{EN} = PD = 3.3V$		0.1	1	mA

**Pin Descriptions**

PIN NUMBER	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
1	RIN	Analog input	 <p>CIRCUIT 1</p>
2	GIN	Analog input	Reference Circuit 1
3	BIN	Analog input	Reference Circuit 1
4	REF	Reference input High impedance input controlling offset of amplifiers	 <p>CIRCUIT 2</p>
5	VEE	Chip substrate (negative power supply for amplifiers)	 <p>CIRCUIT 3</p>
6	GND	Analog ground	
7	VEE OUT	Charge pump output	Reference Circuit 3
8	DGND	Charge pump ground	Reference Circuit 3
9	DVCC	Charge pump supply voltage	Reference Circuit 3
10	PD	Power-down Input Low: Normal Operation High: Power-down Charge Pump and Amplifiers	 <p>CIRCUIT 4</p>

**Pin Descriptions** (Continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	EQUIVALENT CIRCUIT
11, 13	VCC	Positive power supply	
12	$\overline{\text{EN}}$	Chip Enable Low: Normal Operation High: Power Down Amplifiers	Reference Circuit 4
14	BOUT	Analog output	 <p>CIRCUIT 5</p>
15	GOUT	Analog output	Reference Circuit 5
16	ROUT	Analog output	Reference Circuit 5

**Typical Performance Curves**

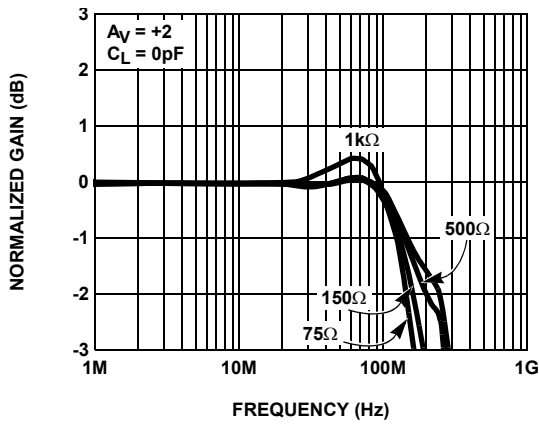


FIGURE 1. GAIN vs FREQUENCY FOR VARIOUS  $R_{LOAD}$

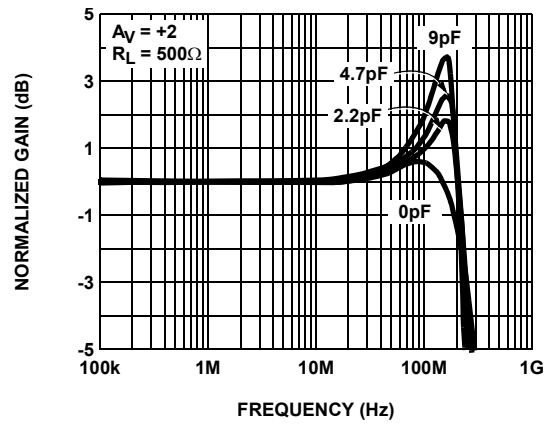


FIGURE 2. GAIN vs FREQUENCY FOR VARIOUS  $C_{LOAD}$

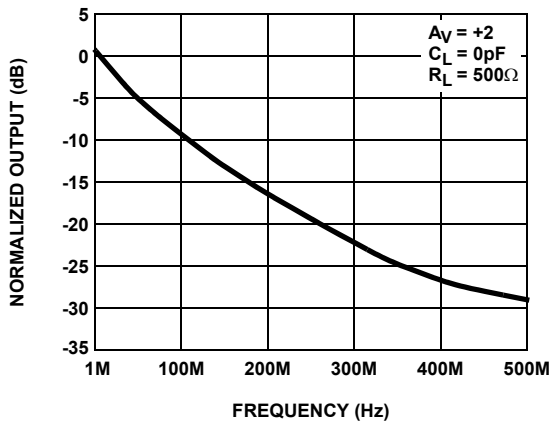


FIGURE 3.  $V_{REF}$  PIN OUTPUT FREQUENCY RESPONSE

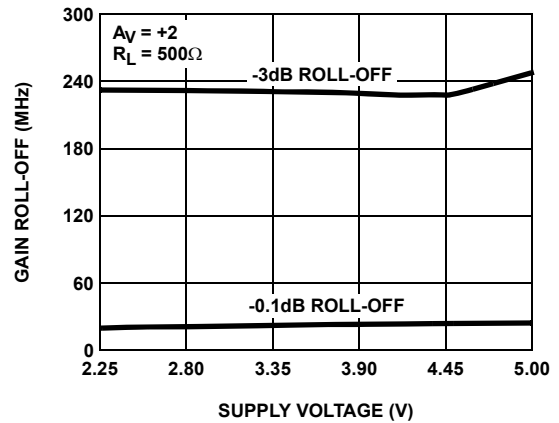


FIGURE 4. GAIN ROLL-OFF vs FREQUENCY

Typical Performance Curves (Continued)

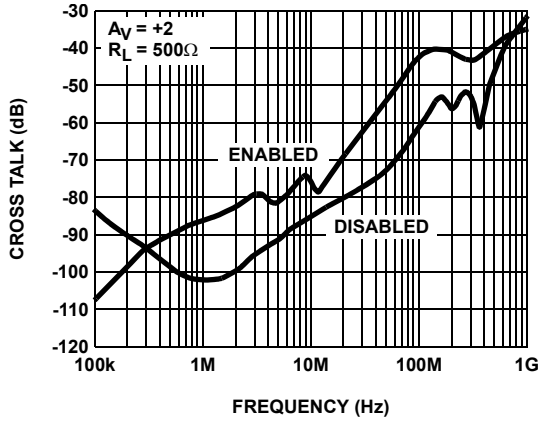


FIGURE 5. CROSS TALK CHANNEL TO CHANNEL (TYPICAL)

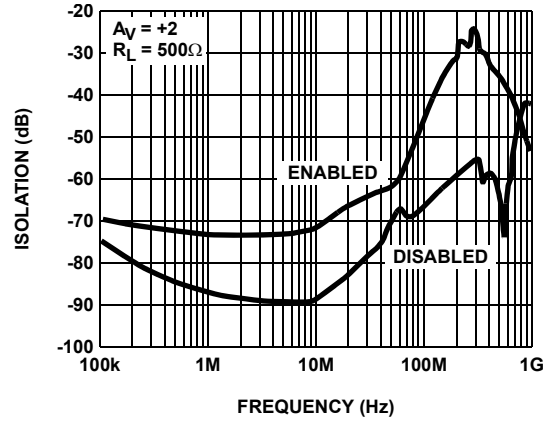


FIGURE 6. INPUT TO OUTPUT ISOLATION vs FREQUENCY

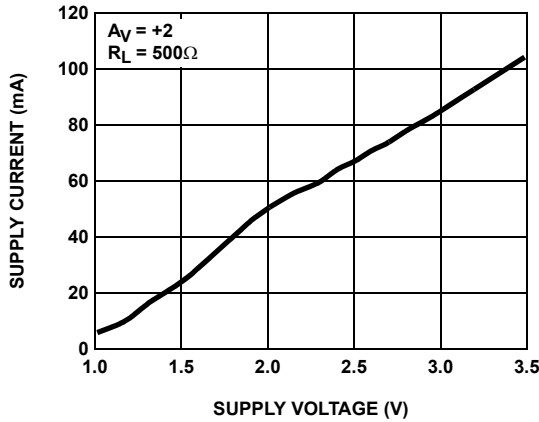


FIGURE 7. SUPPLY CURRENT vs SUPPLY VOLTAGE

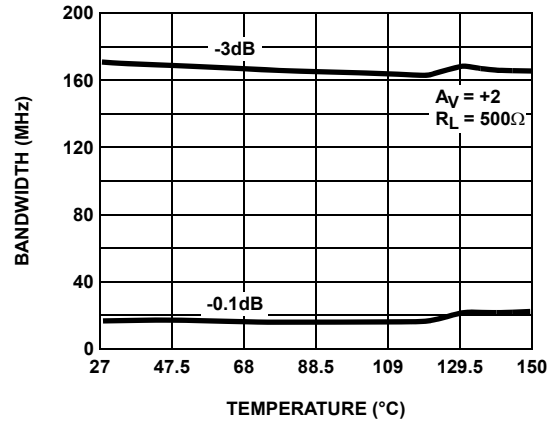


FIGURE 8. BANDWIDTH vs TEMPERATURE

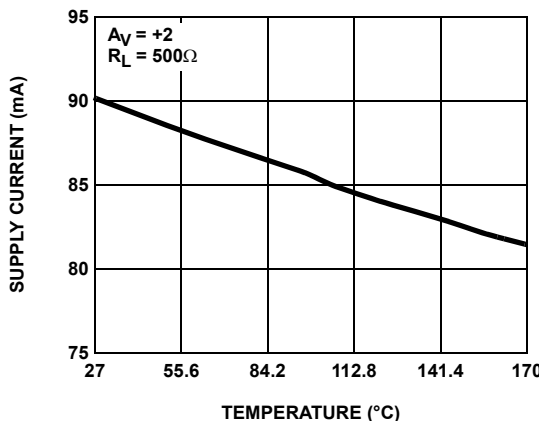


FIGURE 9. SUPPLY CURRENT vs TEMPERATURE

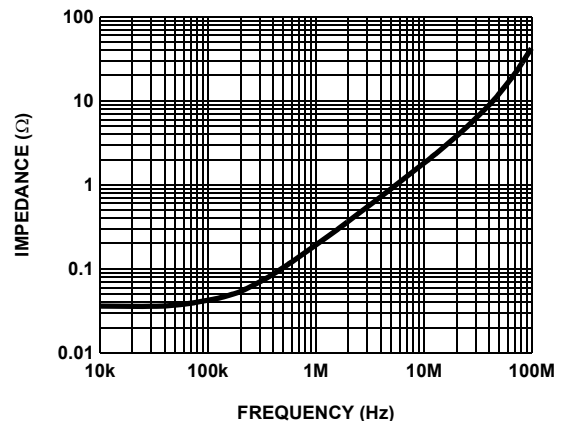


FIGURE 10. OUTPUT IMPEDANCE vs FREQUENCY

Typical Performance Curves (Continued)

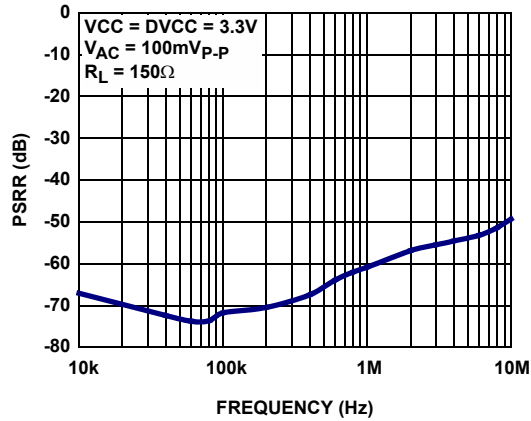


FIGURE 11. POWER SUPPLY REJECTION RATIO vs FREQUENCY

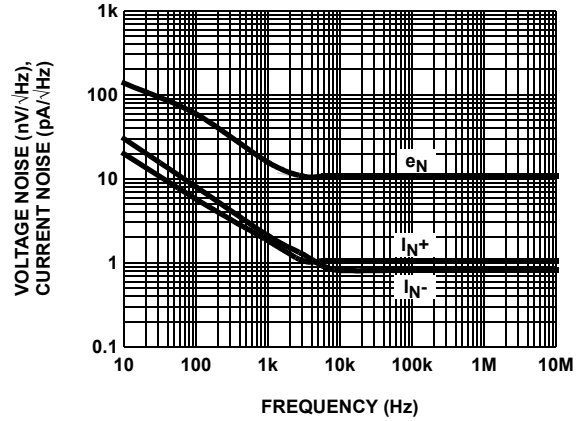


FIGURE 12. VOLTAGE AND CURRENT NOISE vs FREQUENCY

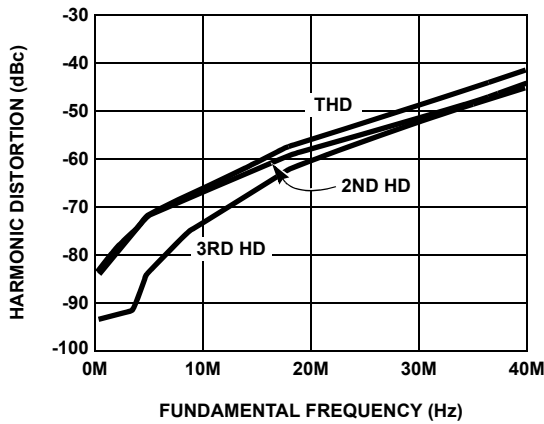


FIGURE 13. HARMONIC DISTORTION vs FREQUENCY

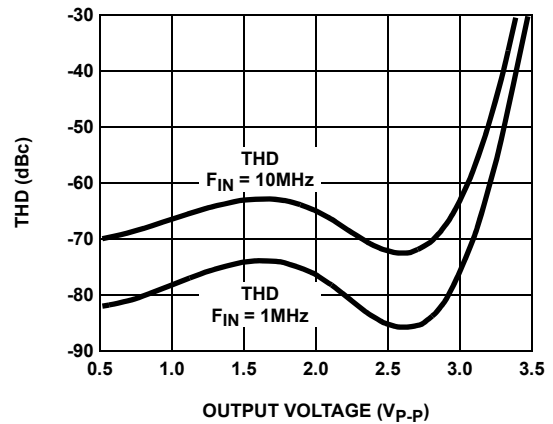


FIGURE 14. THD vs OUTPUT VOLTAGE

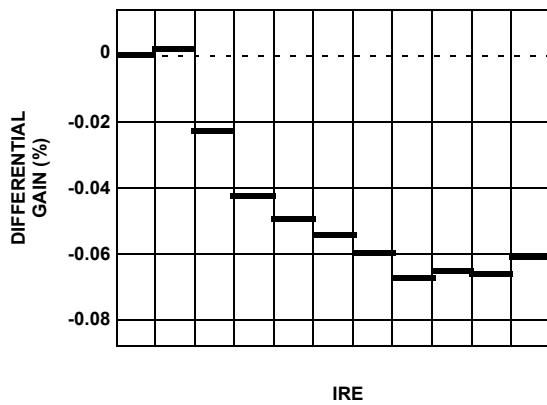


FIGURE 15. DIFFERENTIAL GAIN

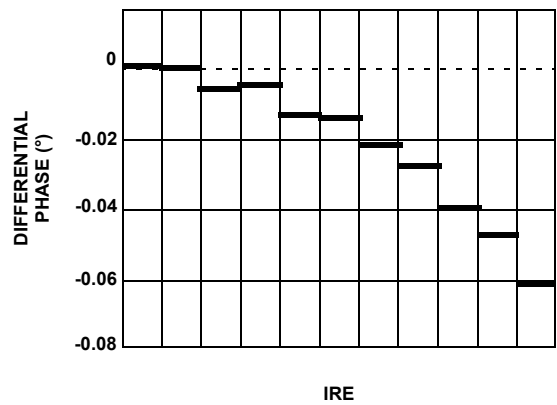


FIGURE 16. DIFFERENTIAL PHASE

Typical Performance Curves (Continued)

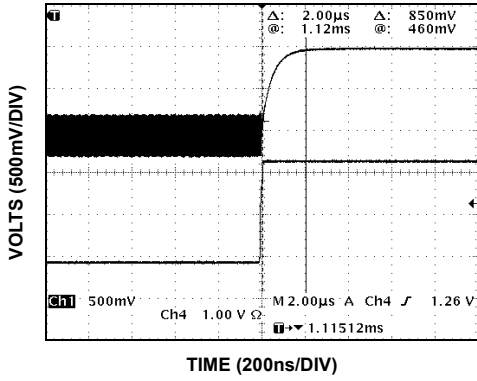


FIGURE 17. DISABLE TIME

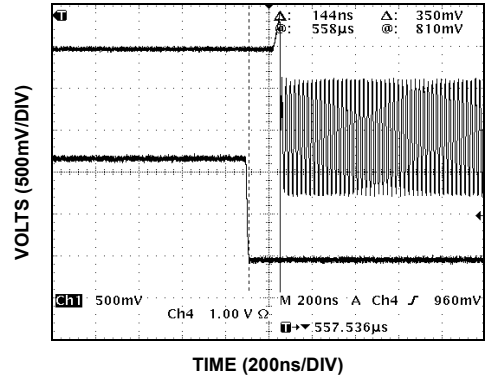


FIGURE 18. ENABLE TIME

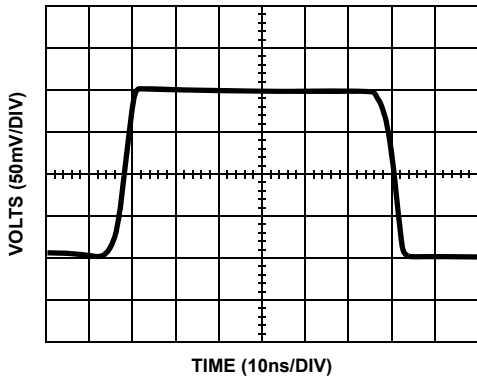


FIGURE 19. SMALL SIGNAL RISE AND FALL TIME

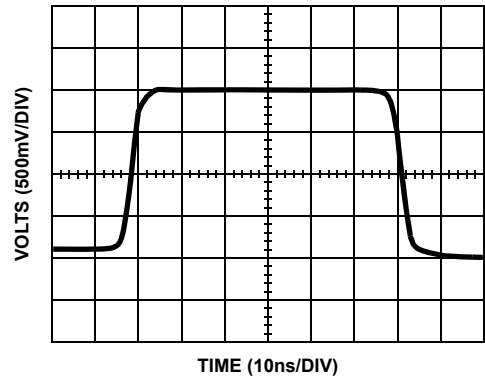


FIGURE 20. LARGE SIGNAL RISE AND FALL TIMES

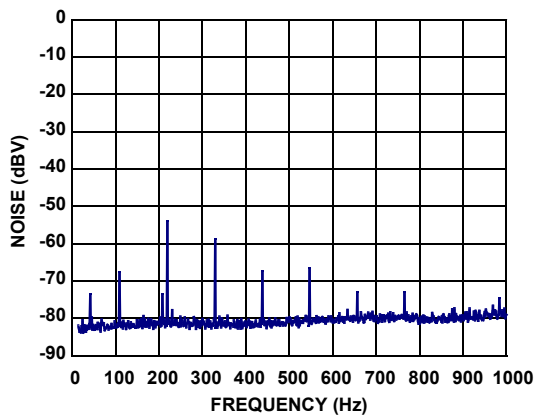


FIGURE 21. NOISE FLOOR WITH CHARGE PUMP HARMONICS

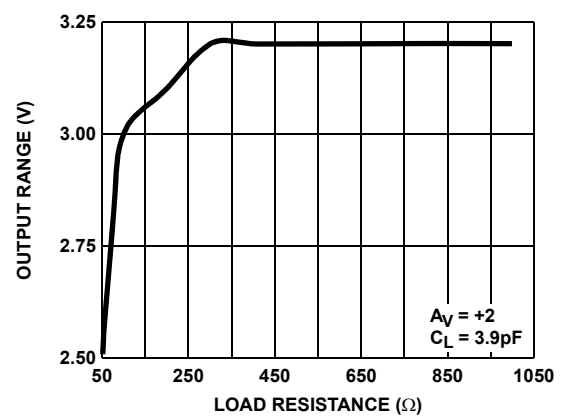


FIGURE 22. MAXIMUM OUTPUT MAGNITUDE vs LOAD RESISTANCE

**Typical Performance Curves** (Continued)

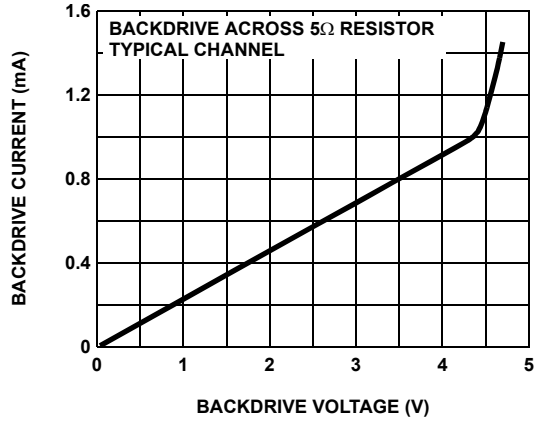


FIGURE 23. BACKDRIVE VOLTAGE vs CURRENT

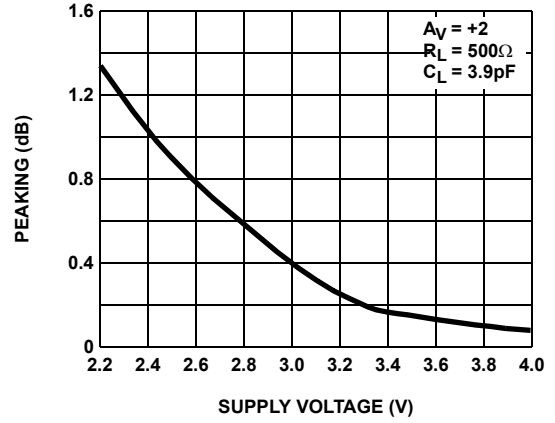


FIGURE 24. PEAKING vs SUPPLY VOLTAGE

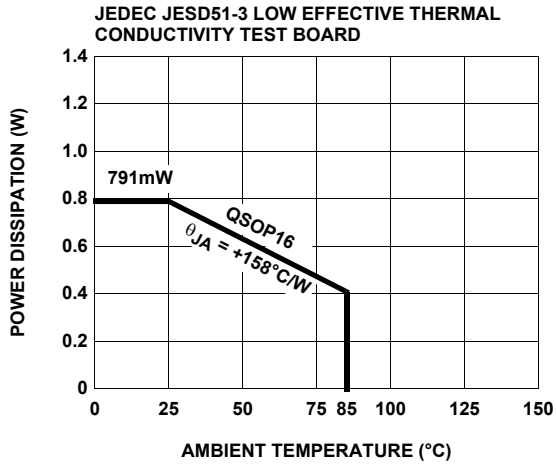


FIGURE 25. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

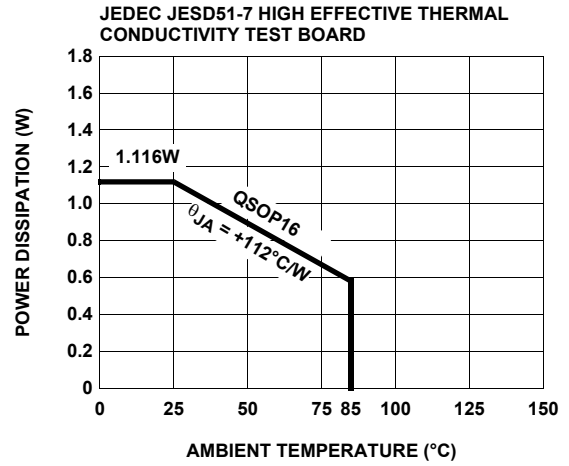
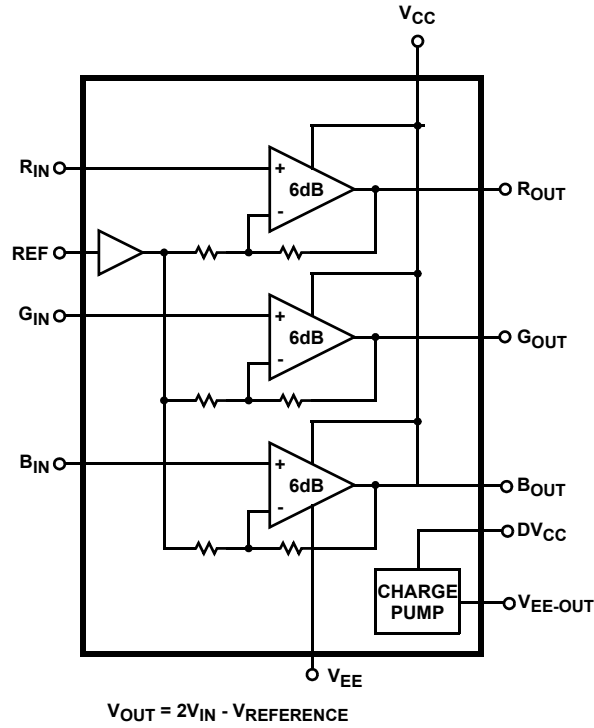
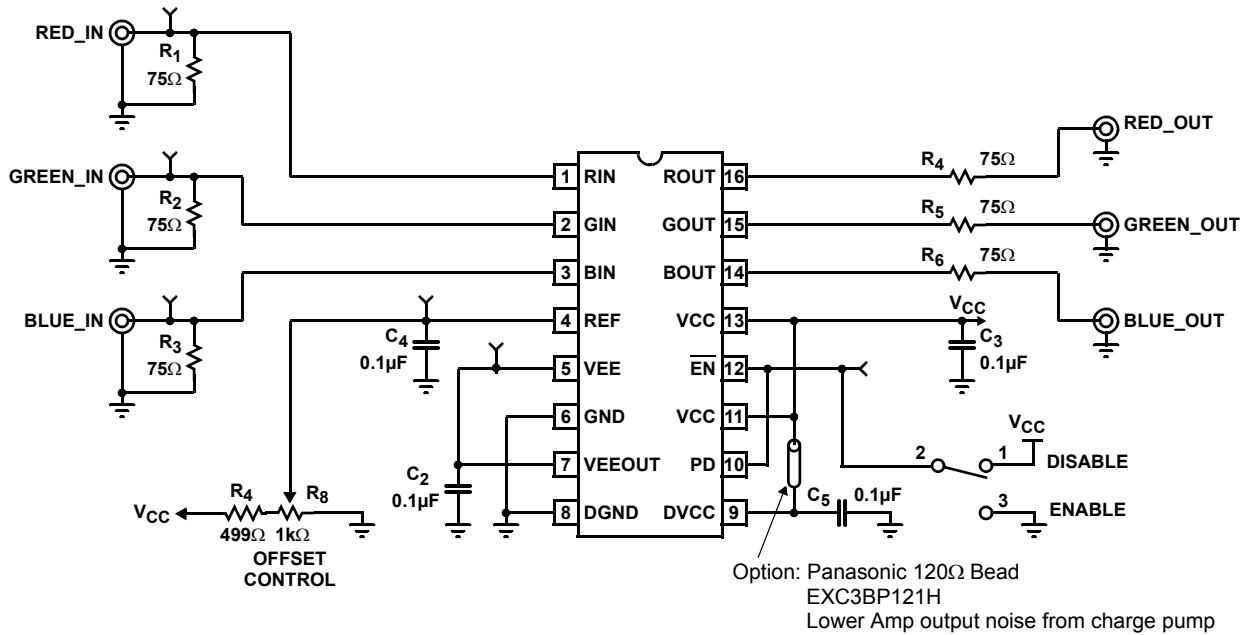


FIGURE 26. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

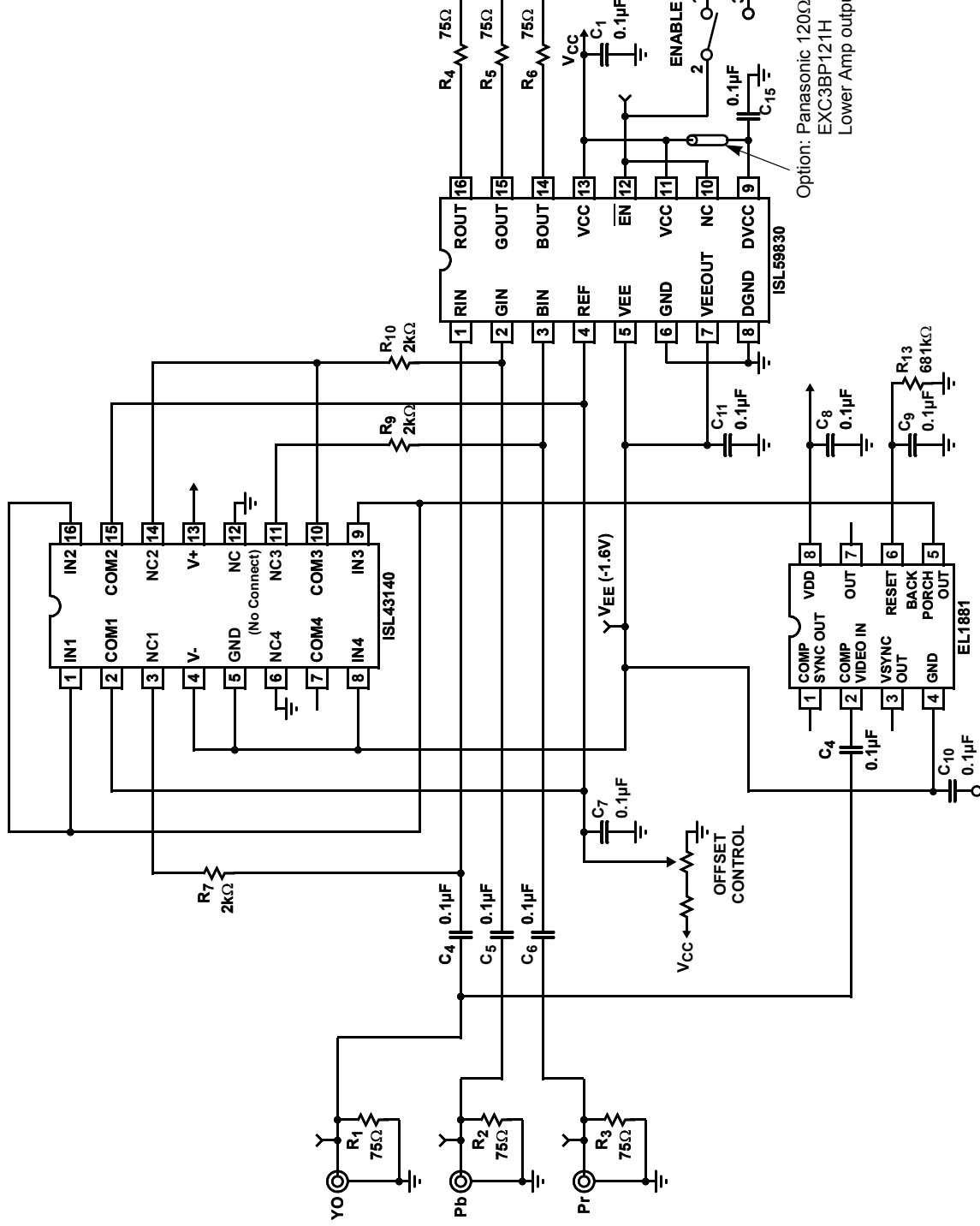
**Block Diagram**



**Demo Board Schematic**



# ISL59837 + DC-Restore Solution



## Description of Operation and Application Information

### Theory Of Operation

The ISL59837 is a highly practical and robust marriage of three high bandwidth, high speed, low power, rail-to-rail voltage feedback amplifiers with a charge pump to provide a negative rail without an additional power supply. Designed to operate with a single supply voltage range from 0V to 3.3V, the ISL59837 eliminates the need for a split supply with the incorporation of a charge pump capable of generating a bottom rail as much as 1.6V below ground for a 4.9V range on a single 3.3V supply. This performance is ideal for NTSC video with its negative-going sync pulses.

### THE AMPLIFIER

The ISL59837 fabricated on a di-electrically isolated high speed 5V Bi-CMOS process with 4GHz PNPs and NPN transistor exceeding 20GHz - perfect for low distortion, low power demand and high frequency circuits. While the ISL59837 utilizes somewhat standard voltage mode feedback topologies, there are many non-standard analog features providing its outstanding bandwidth, rail-to-rail operation, and output drive capabilities. The input signal initially passes through a folded cascode, a topology providing enhanced frequency response by essentially fixing the base collector voltage at the junction of the input and gain stage. The collector of each input device looks directly into an emitter that is tied closely to ground through a resistor and biased with a very stable DC source. Since the voltage of this collector is "locked stable," the effective bandwidth limiting of the Miller capacitance is greatly reduced. The signal is then passed through a second fully-realized differential gain stage and finally through a proprietary common emitter output stage for improved rail-to-rail output performance. The result is a highly-stable, low

distortion, low power, and high frequency amplifier capable of driving moderately capacitive loads with near rail-to-rail performance.

### INPUT OUTPUT RANGE

The three amplifier channels have an input common mode voltage range from 0.15V below the bottom rail to within 100mV of the positive supply,  $V_{S+}$  pin (Note: bottom rail is established by the charge pump at negative one half the positive supply). As the input signal moves outside the specified range, the output signal will exhibit increasingly higher levels of harmonic distortion. And of course, as load resistance becomes lower, the current drive capability of the device will be challenged and its ability to drive close to each rail is reduced. For instance, with a load resistance of 1k $\Omega$  the output swing is within 100mV of the rails, while a load resistance of 150 $\Omega$  limits the output swing to within around 300mV of the rails.

### AMPLIFIER OUTPUT IMPEDANCE

To achieve near rail-to-rail performance, the output stage of the ISL59837 uses transistors in the common emitter configuration, typically producing higher output impedance than the standard emitter follower output stage. The exceptionally high open loop gain of the ISL59837 and local feedback reduces output impedance to less than 2 $\Omega$  at low frequency. However, since output impedance of the device is exponentially modulated by the magnitude of the open loop gain, output impedance increases with frequency as the open loop gain decreases with frequency. This inductive-like effect of the output impedance is countered in the ISL59837 with proprietary output stage topology, keeping the output impedance low over a wide frequency range and making it possible to easily and effectively drive relatively heavy capacitive loads (see Figure 10).

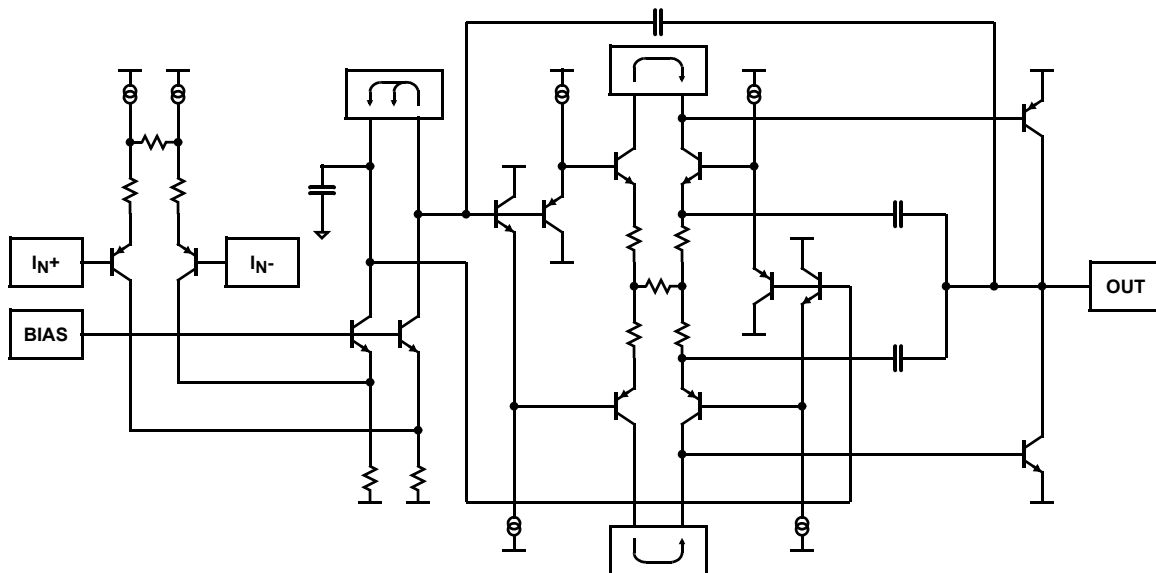


FIGURE 27. SIMPLIFIED SCHEMATIC

## THE CHARGE PUMP

The ISL59837 charge pump provides a bottom rail up to 1.6V below ground while operating on a 0V to 3.3V power supply. The charge pump is internally regulated to one-half the potential of the positive supply. This internal multi-phase charge pump is driven by a 110MHz differential ring oscillator driving a series of inverters and charge storage circuitry. Each series inverter charges and places parallel adjoining charge circuitry slightly out of phase with the immediately preceding block. This generates a negative rail of about -1.6V with a low amplitude ripple voltage from the charge pump action. Some of this ripple is coupled into the output signals at a very low amplitude, as seen in Figure 21. The ripple on the outputs is typically well below the noise floor of the signal.

There are two ways to further reduce the output supply noise:

- Add a 120Ω bead in series between  $V_{CC}$  and  $DV_{CC}$ . This reduces the coupling between the charge pump and the analog amplifier supplies.
- Add a 20pF capacitor between the back load 75Ω resistor and ground (see “ISL59837 + DC-Restore Solution” on page 10). This will attenuate frequencies above 100MHz.

The system operates at sufficiently high frequencies that any related charge pump noise is far beyond standard video bandwidth requirements. Still, appropriate bypassing discipline must be observed, and all pins related to either the power supply or the charge pump must be properly bypassed. See “Power Supply Bypassing and Printed Circuit Board Layout” on page 13.

## THE VREF PIN

Applying a voltage to the VREF pin simply places that voltage on what would usually be the ground side of the gain resistor of the amplifier, resulting in a DC-level shift of the output signal. Applying 100mV to the VREF pin would apply a 100mV DC level shift to the outgoing signal. The charge pump provides sufficient bottom room to accommodate the shifted signal.

The ISL59837 buffers the VREF voltage before applying it to the triple amplifiers, isolating the input from the amplifiers and allowing it to be driven by moderate-impedance voltage sources.

## THE VEE PIN

The VEE pin is the output pin for the charge pump. A voltmeter applied to this pin will display the output of the charge pump. This pin does not affect the functionality of the part. One may use this pin as an additional voltage source. Keep in mind that the output of this pin is generated by the internal charge pump and a fully regulated supply that must be properly bypassed. We recommend a 0.1μF ceramic capacitor placed as close to the pin and connected to the ground plane of the board.

## INPUT, OUTPUT AND SUPPLY VOLTAGE RANGE

The ISL59837 is designed to operate with a single supply voltage range of from 0V to 3.3V. The need for a split supply

has been eliminated with the incorporation of a charge pump capable of generating a bottom rail as much as 1.6V below ground, for a 4.9V range on a single 3.3V supply. This performance is ideal for NTSC video with its negative-going sync pulses.

## VIDEO PERFORMANCE

For good video performance, an amplifier is required to maintain the same output impedance and the same frequency and phase response as DC levels are changed at the output. This is especially difficult when driving a standard video load of 150Ω because of the change in output current with changing DC levels. Special circuitry has been incorporated into the ISL59837 for the reduction of output impedance variation with the current output. This results in outstanding differential gain and differential phase specifications of 0.06% and 0.1°, while driving 150Ω at a gain of +2. Driving higher impedance loads would result in similar or better differential gain and differential phase performance.

## NTSC

The ISL59837 (generating a negative rail internally) is ideally suited for NTSC video with its accompanying negative-going sync signals, which is easily handled by the ISL59837 without the need for an additional supply as the ISL59837 generates a negative rail with an internal charge pump referenced at negative 1/2 the positive supply.

## YPbPr

YPbPr signals originating from a DVD player requiring three channels of very tightly-controlled amplifier gain accuracy present no difficulty for the ISL59837. Specifically, this standard encodes sync on the Y-Channel and it is a negative-going signal, which is easily handled by the ISL59837 without the need for an additional supply as the ISL59837 generates a negative rail placed at negative 1/2 the positive supply. Additionally, the Pb and Pr are bipolar analog signals and the video signals are negative-going, and again, easily handled by the ISL59837.

## DRIVING CAPACITIVE LOADS AND CABLES

The ISL59837 (internally-compensated to drive 75Ω cables) will drive 10pF loads in parallel with 1kΩ with less than 5dB of peaking. If less peaking is required, a small series resistor, usually between 5Ω to 50Ω, can be placed in series with the output. This will reduce peaking at the expense of a slight closed loop gain reduction. When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking. The ISL59837 is a triple amplifier designed to drive three channels; simply deal with each channel separately as described in this section.

## DC-RESTORE

When the ISL59837 is AC-coupled it becomes necessary to restore the DC reference for the signal. This is accomplished with a DC-restore system applied between the capacitive "AC" coupling and the input of the device. Refer to "ISL59837 + DC-Restore Solution" on page 10.

## DISABLE/POWER-DOWN

The ISL59837 can be disabled and its output placed in a high impedance state. The turn-off time is around 25ns and the turn-on time is around 200ns. When the PD pin is taken high, the chip's total supply current is reduced to 0.1mA typically, all but eliminating the power used by the part. Taking the  $\overline{\text{EN}}$  pin high powers down the amplifiers, leaving the charge pump running. Both pins can be controlled by standard TTL or CMOS signal levels (0.8V  $V_{IL}$ , 2.0V  $V_{IH}$  relative to GND).

## OUTPUT DRIVE CAPABILITY

The ISL59837 does not have internal short-circuit protection circuitry. A short-circuit current of 80mA sourcing and 150mA sinking for the output is connected half way between the rails with a 10 $\Omega$  resistor. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds  $\pm 40\text{mA}$ , after which the electro-migration limit of the process will be exceeded and the part will be damaged. This limit is set by the design of the internal metal interconnections.

## POWER DISSIPATION

With the high output drive capability of the ISL59837, it is possible to exceed the +150°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$P_{D_{MAX}} = \frac{T_{J_{MAX}} - T_{A_{MAX}}}{\theta_{JA}} \quad (\text{EQ. 1})$$

Where:

$T_{J_{MAX}}$  = Maximum junction temperature

$T_{A_{MAX}}$  = Maximum ambient temperature

$\theta_{JA}$  = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

for sourcing:

$$P_{D_{MAX}} = V_S \times I_{S_{MAX}} + (V_S - V_{OUTi}) \times \frac{V_{OUTi}}{R_{Li}} \quad (\text{EQ. 2})$$

for sinking:

$$P_{D_{MAX}} = V_S \times I_{S_{MAX}} + (V_{OUTi} - V_S) \times I_{LOADi} \quad (\text{EQ. 3})$$

Where:

$V_S$  = Supply voltage

$I_{S_{MAX}}$  = Maximum quiescent supply current

$V_{OUT}$  = Maximum output voltage of the application

$R_{LOAD}$  = Load resistance tied to ground

$I_{LOAD}$  = Load current

$i$  = Number of output channels

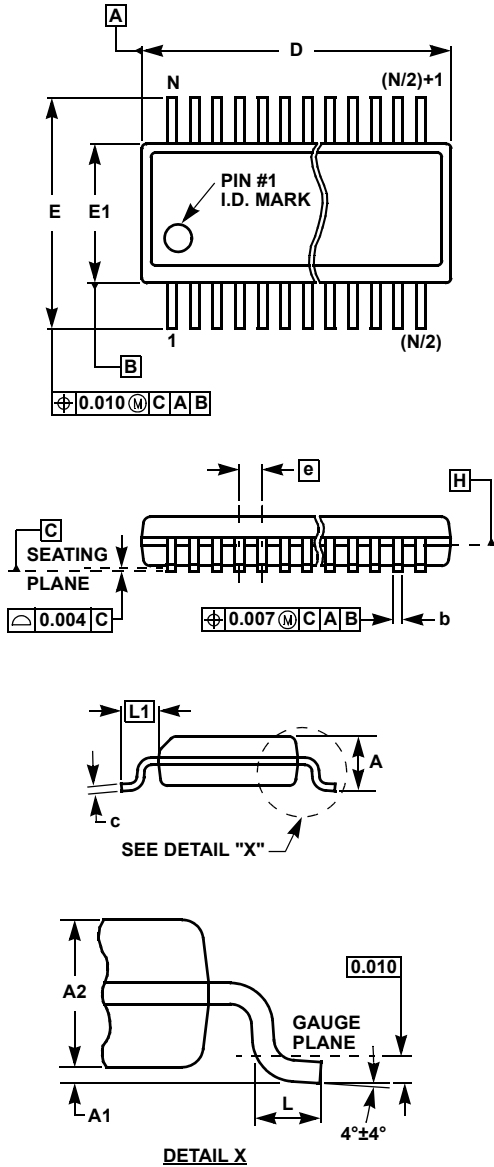
By setting the two  $P_{D_{MAX}}$  equations equal to each other, we can solve the output current and  $R_{LOAD}$  to avoid the device overheat.

## Power Supply Bypassing and Printed Circuit Board Layout

Strip line design techniques are recommended for the input and output signal traces. As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as short as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the  $V_{S-}$  pin is connected to the ground plane, a single 4.7 $\mu\text{F}$  tantalum capacitor in parallel with a 0.1 $\mu\text{F}$  ceramic capacitor from  $V_{S+}$  to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split-internal supplies are to be used. In this case, the  $V_{S-}$  pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to a minimum. Use of wire-wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is also very important.

**Quarter Size Outline Plastic Packages Family (QSOP)**



**MDP0040**

**QUARTER SIZE OUTLINE PLASTIC PACKAGES FAMILY**

SYMBOL	INCHES			TOLERANCE	NOTES
	QSOP16	QSOP24	QSOP28		
A	0.068	0.068	0.068	Max.	-
A1	0.006	0.006	0.006	$\pm 0.002$	-
A2	0.056	0.056	0.056	$\pm 0.004$	-
b	0.010	0.010	0.010	$\pm 0.002$	-
c	0.008	0.008	0.008	$\pm 0.001$	-
D	0.193	0.341	0.390	$\pm 0.004$	1, 3
E	0.236	0.236	0.236	$\pm 0.008$	-
E1	0.154	0.154	0.154	$\pm 0.004$	2, 3
e	0.025	0.025	0.025	Basic	-
L	0.025	0.025	0.025	$\pm 0.009$	-
L1	0.041	0.041	0.041	Basic	-
N	16	24	28	Reference	-

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**NOTES:**

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994.

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