## Features

- Compatible with MCS®-51 Products
- 4K Bytes of In-System Programmable (ISP) Flash Memory
  - Endurance: 10,000 Write/Erase Cycles
- 4.0V to 5.5V Operating Range
- Fully Static Operation: 0 Hz to 33 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Full Duplex UART Serial Channel
- Low-power Idle and Power-down Modes
- Interrupt Recovery from Power-down Mode
- Watchdog Timer
- Dual Data Pointer
- Power-off Flag
- Fast Programming Time
- Flexible ISP Programming (Byte and Page Mode)
- Green (Pb/Halide-free) Packaging Option

# 8-bit Microcontroller with 4K Bytes In-System Programmable Flash

# AT89S51

## 1. Description

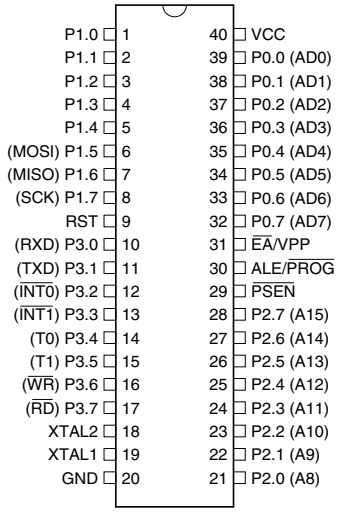
The AT89S51 is a low-power, high-performance CMOS 8-bit microcontroller with 4K bytes of In-System Programmable Flash memory. The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard 80C51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with In-System Programmable Flash on a monolithic chip, the Atmel AT89S51 is a powerful microcontroller which provides a highly-flexible and cost-effective solution to many embedded control applications.

The AT89S51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, Watchdog timer, two data pointers, two 16-bit timer/counters, a five-vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator, and clock circuitry. In addition, the AT89S51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port, and interrupt system to continue functioning. The Power-down mode saves the RAM contents but freezes the oscillator, disabling all other chip functions until the next external interrupt or hardware reset.

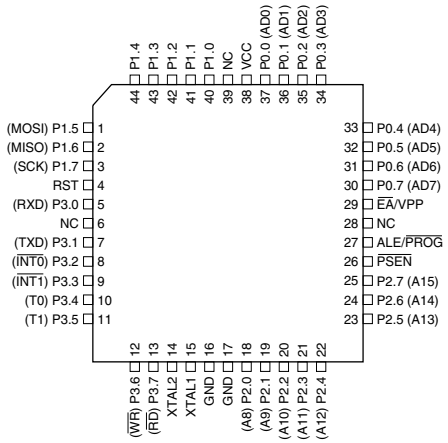
2487D–MICRO–6/08

# 2. Pin Configurations

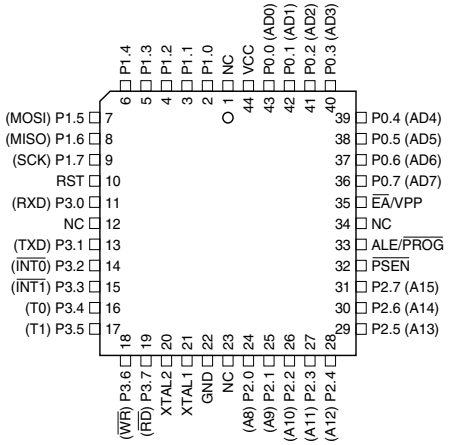
## 2.1 40-lead PDIP



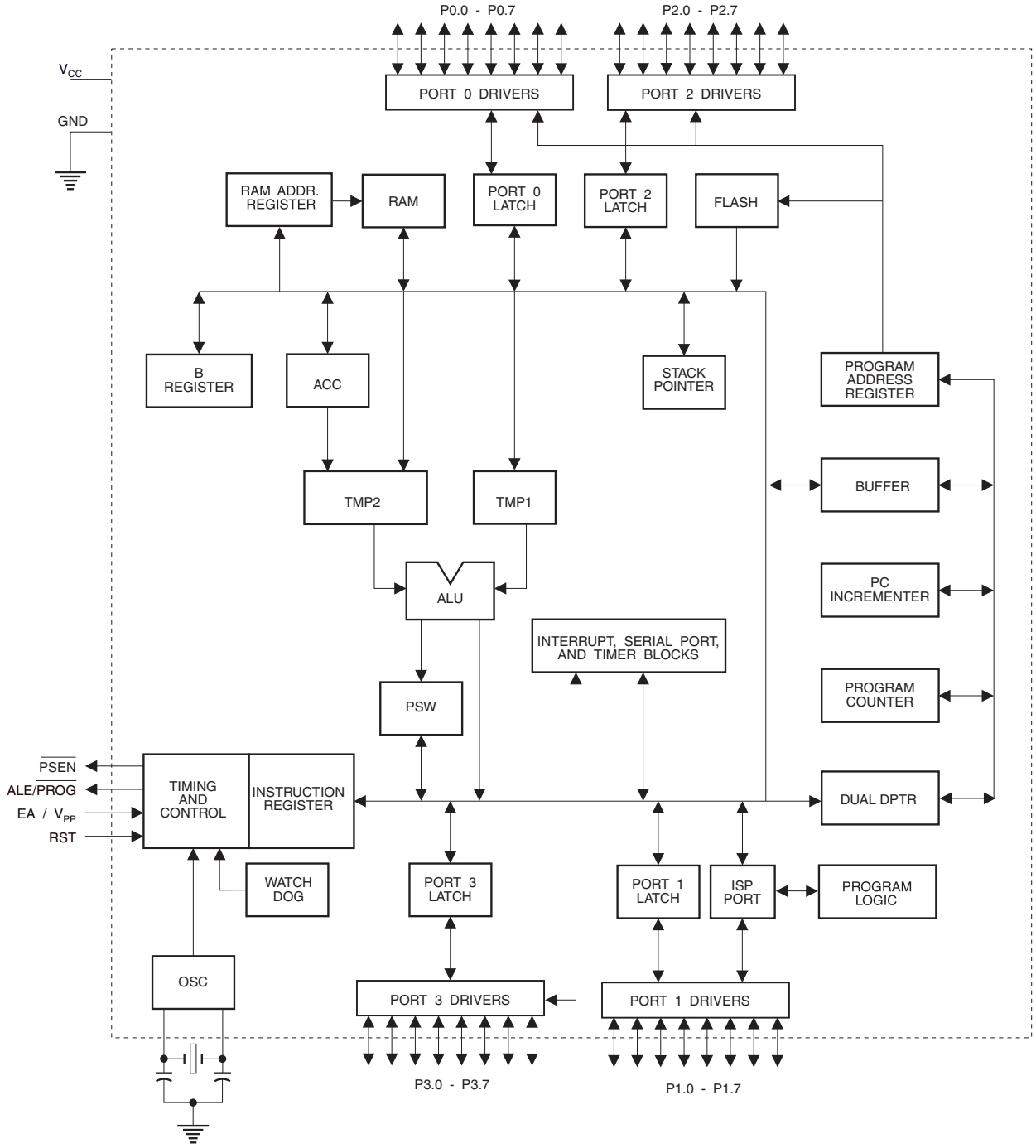

## 2.2 44-lead TQFP




## 2.3 44-lead PLCC



## 3. Block Diagram



# 4. Pin Description

## 4.1 VCC

Supply voltage.

## 4.2 GND

Ground.

## 4.3 Port 0

Port 0 is an 8-bit open drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 can also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode, P0 has internal pull-ups.

Port 0 also receives the code bytes during Flash programming and outputs the code bytes during program verification. **External pull-ups are required during program verification**.

## 4.4 Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ($I_{IL}$) because of the internal pull-ups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

| Port Pin | Alternate Functions |
|---|---|
| P1.5 | MOSI (used for In-System Programming) |
| P1.6 | MISO (used for In-System Programming) |
| P1.7 | SCK (used for In-System Programming) |

## 4.5 Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins, they are pulled high by the internal pull-ups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current ($I_{IL}$) because of the internal pull-ups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, Port 2 uses strong internal pull-ups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

## 4.6 Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pull-ups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins, they are pulled high by the inter-

nal pull-ups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ($I_{IL}$) because of the pull-ups.

Port 3 receives some control signals for Flash programming and verification.

Port 3 also serves the functions of various special features of the AT89S51, as shown in the following table.

| Port Pin | Alternate Functions |
|---|---|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{\text{INT0}}$ (external interrupt 0) |
| P3.3 | $\overline{\text{INT1}}$ (external interrupt 1) |
| P3.4 | T0 (timer 0 external input) |
| P3.5 | T1 (timer 1 external input) |
| P3.6 | $\overline{\text{WR}}$ (external data memory write strobe) |
| P3.7 | $\overline{\text{RD}}$ (external data memory read strobe) |

## 4.7 RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device. This pin drives High for 98 oscillator periods after the Watchdog times out. The DISRTO bit in SFR AUXR (address 8EH) can be used to disable this feature. In the default state of bit DISRTO, the RESET HIGH out feature is enabled.

## 4.8 ALE/$\overline{\text{PROG}}$

Address Latch Enable (ALE) is an output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation, ALE is emitted at a constant rate of 1/6 the oscillator frequency and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external data memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

## 4.9 $\overline{\text{PSEN}}$

Program Store Enable ($\overline{\text{PSEN}}$) is the read strobe to external program memory.

When the AT89S51 is executing code from external program memory, $\overline{\text{PSEN}}$ is activated twice each machine cycle, except that two $\overline{\text{PSEN}}$ activations are skipped during each access to external data memory.

## 4.10 $\overline{\text{EA}}$/VPP

External Access Enable. $\overline{\text{EA}}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{\text{EA}}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to $V_{CC}$ for internal program executions.

This pin also receives the 12-volt programming enable voltage ($V_{PP}$) during Flash programming.

### 4.11 XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

### 4.12 XTAL2

Output from the inverting oscillator amplifier

## 5. Special Function Registers

A map of the on-chip memory area called the Special Function Register (SFR) space is shown in Table 5-1.

Note that not all of the addresses are occupied, and unoccupied addresses may not be implemented on the chip. Read accesses to these addresses will in general return random data, and write accesses will have an indeterminate effect.

**Table 5-1.** AT89S51 SFR Map and Reset Values

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 0F8H | | | | | | | | | 0FFH |
| 0F0H | B<br>00000000 | | | | | | | | 0F7H |
| 0E8H | | | | | | | | | 0EFH |
| 0E0H | ACC<br>00000000 | | | | | | | | 0E7H |
| 0D8H | | | | | | | | | 0DFH |
| 0D0H | PSW<br>00000000 | | | | | | | | 0D7H |
| 0C8H | | | | | | | | | 0CFH |
| 0C0H | | | | | | | | | 0C7H |
| 0B8H | IP<br>XX000000 | | | | | | | | 0BFH |
| 0B0H | P3<br>11111111 | | | | | | | | 0B7H |
| 0A8H | IE<br>0X000000 | | | | | | | | 0AFH |
| 0A0H | P2<br>11111111 | | AUXR1<br>XXXXXXX0 | | | | WDTRST<br>XXXXXXXX | | 0A7H |
| 98H | SCON<br>00000000 | SBUF<br>XXXXXXXX | | | | | | | 9FH |
| 90H | P1<br>11111111 | | | | | | | | 97H |
| 88H | TCON<br>00000000 | TMOD<br>00000000 | TL0<br>00000000 | TL1<br>00000000 | TH0<br>00000000 | TH1<br>00000000 | AUXR<br>XXX00XX0 | | 8FH |
| 80H | P0<br>11111111 | SP<br>00000111 | DP0L<br>00000000 | DP0H<br>00000000 | DP1L<br>00000000 | DP1H<br>00000000 | | PCON<br>0XXX0000 | 87H |

User software should not write 1s to these unlisted locations, since they may be used in future products to invoke new features. In that case, the reset or inactive values of the new bits will always be 0.

**Interrupt Registers:** The individual interrupt enable bits are in the IE register. Two priorities can be set for each of the five interrupt sources in the IP register.

**Table 5-2.** AUXR: Auxiliary Register

AUXR Address = 8EH Reset Value = XXX00XX0B

Not Bit Addressable

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| | – | – | – | WDIDLE | DISRTO | – | – | DISALE |

| | | |
|---|---|---|
| – | Reserved for future expansion | |
| DISALE | Disable/Enable ALE | |
| | DISALE<br>Operating Mode | |
| | 0 | ALE is emitted at a constant rate of 1/6 the oscillator frequency |
| | 1 | ALE is active only during a MOVX or MOVC instruction |
| DISRTO | Disable/Enable Reset-out | |
| | DISRTO | |
| | 0 | Reset pin is driven High after WDT times out |
| | 1 | Reset pin is input only |
| WDIDLE | Disable/Enable WDT in IDLE mode | |
| WDIDLE | | |
| 0 | WDT continues to count in IDLE mode | |
| 1 | WDT halts counting in IDLE mode | |

**Dual Data Pointer Registers:** To facilitate accessing both internal and external data memory, two banks of 16-bit Data Pointer Registers are provided: DP0 at SFR address locations 82H-83H and DP1 at 84H-85H. Bit DPS = 0 in SFR AUXR1 selects DP0 and DPS = 1 selects DP1. The user should **ALWAYS** initialize the DPS bit to the appropriate value before accessing the respective Data Pointer Register.

**Power Off Flag:** The Power Off Flag (POF) is located at bit 4 (PCON.4) in the PCON SFR. POF is set to “1” during power up. It can be set and rest under software control and is not affected by reset.

**Table 5-3.** AUXR1: Auxiliary Register 1

AUXR1 Address = A2H Reset Value = XXXXXXX0B

Not Bit Addressable

| | – | – | – | – | – | – | – | DPS |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |

– Reserved for future expansion

DPS Data Pointer Register Select

DPS

0 Selects DPTR Registers DP0L, DP0H

1 Selects DPTR Registers DP1L, DP1H

# 6. Memory Organization

MCS-51 devices have a separate address space for Program and Data Memory. Up to 64K bytes each of external Program and Data Memory can be addressed.

## 6.1 Program Memory

If the $\overline{EA}$ pin is connected to GND, all program fetches are directed to external memory.

On the AT89S51, if $\overline{EA}$ is connected to $V_{CC}$, program fetches to addresses 0000H through FFFH are directed to internal memory and fetches to addresses 1000H through FFFFH are directed to external memory.

## 6.2 Data Memory

The AT89S51 implements 128 bytes of on-chip RAM. The 128 bytes are accessible via direct and indirect addressing modes. Stack operations are examples of indirect addressing, so the 128 bytes of data RAM are available as stack space.

# 7. Watchdog Timer (One-time Enabled with Reset-out)

The WDT is intended as a recovery method in situations where the CPU may be subjected to software upsets. The WDT consists of a 14-bit counter and the Watchdog Timer Reset (WDTRST) SFR. The WDT is defaulted to disable from exiting reset. To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, it will increment every machine cycle while the oscillator is running. The WDT timeout period is dependent on the external clock frequency. There is no way to disable the WDT except through reset (either hardware reset or WDT overflow reset). When WDT overflows, it will drive an output RESET HIGH pulse at the RST pin.

## 7.1 Using the WDT

To enable the WDT, a user must write 01EH and 0E1H in sequence to the WDTRST register (SFR location 0A6H). When the WDT is enabled, the user needs to service it by writing 01EH and 0E1H to WDTRST to avoid a WDT overflow. The 14-bit counter overflows when it reaches 16383 (3FFFH), and this will reset the device. When the WDT is enabled, it will increment every machine cycle while the oscillator is running. This means the user must reset the WDT at least

every 16383 machine cycles. To reset the WDT the user must write 01EH and 0E1H to WDTRST. WDTRST is a write-only register. The WDT counter cannot be read or written. When WDT overflows, it will generate an output RESET pulse at the RST pin. The RESET pulse duration is 98xTOSC, where TOSC = 1/FOSC. To make the best use of the WDT, it should be serviced in those sections of code that will periodically be executed within the time required to prevent a WDT reset.

### 7.2 WDT During Power-down and Idle

In Power-down mode the oscillator stops, which means the WDT also stops. While in Power-down mode, the user does not need to service the WDT. There are two methods of exiting Power-down mode: by a hardware reset or via a level-activated external interrupt, which is enabled prior to entering Power-down mode. When Power-down is exited with hardware reset, servicing the WDT should occur as it normally does whenever the AT89S51 is reset. Exiting Power-down with an interrupt is significantly different. The interrupt is held low long enough for the oscillator to stabilize. When the interrupt is brought high, the interrupt is serviced. To prevent the WDT from resetting the device while the interrupt pin is held low, the WDT is not started until the interrupt is pulled high. It is suggested that the WDT be reset during the interrupt service for the interrupt used to exit Power-down mode.

To ensure that the WDT does not overflow within a few states of exiting Power-down, it is best to reset the WDT just before entering Power-down mode.

Before going into the IDLE mode, the WDIDLE bit in SFR AUXR is used to determine whether the WDT continues to count if enabled. The WDT keeps counting during IDLE (WDIDLE bit = 0) as the default state. To prevent the WDT from resetting the AT89S51 while in IDLE mode, the user should always set up a timer that will periodically exit IDLE, service the WDT, and reenter IDLE mode.

With WDIDLE bit enabled, the WDT will stop to count in IDLE mode and resumes the count upon exit from IDLE.

## 8. UART

The UART in the AT89S51 operates the same way as the UART in the AT89C51. For further information on the UART operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

## 9. Timer 0 and 1

Timer 0 and Timer 1 in the AT89S51 operate the same way as Timer 0 and Timer 1 in the AT89C51. For further information on the timers' operation, please click on the document link below:

http://www.atmel.com/dyn/resources/prod_documents/DOC4316.PDF

# 10. Interrupts

The AT89S51 has a total of five interrupt vectors: two external interrupts ($\overline{INT0}$ and $\overline{INT1}$), two timer interrupts (Timers 0 and 1), and the serial port interrupt. These interrupts are all shown in Figure 10-1.

Each of these interrupt sources can be individually enabled or disabled by setting or clearing a bit in Special Function Register IE. IE also contains a global disable bit, EA, which disables all interrupts at once.

Note that Table 10-1 shows that bit positions IE.6 and IE.5 are unimplemented. User software should not write 1s to these bit positions, since they may be used in future AT89 products.

The Timer 0 and Timer 1 flags, TF0 and TF1, are set at S5P2 of the cycle in which the timers overflow. The values are then polled by the circuitry in the next cycle.

**Table 10-1.** Interrupt Enable (IE) Register

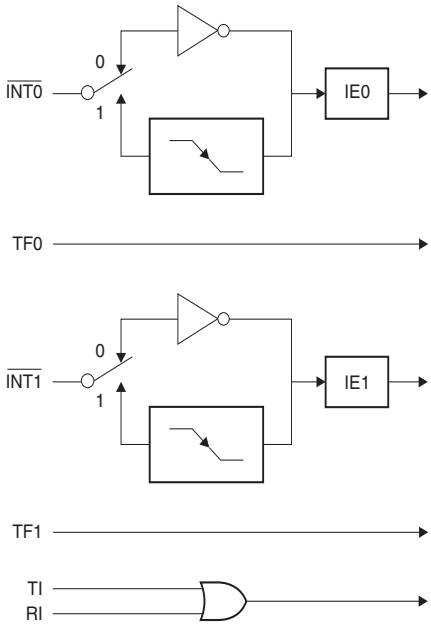
| (MSB) | | | | | | | (LSB) |
|---|---|---|---|---|---|---|---|
| EA | – | – | ES | ET1 | EX1 | ET0 | EX0 |

Enable Bit = 1 enables the interrupt.

Enable Bit = 0 disables the interrupt.

| Symbol | Position | Function |
|---|---|---|
| EA | IE.7 | Disables all interrupts. If EA = 0, no interrupt is acknowledged. If EA = 1, each interrupt source is individually enabled or disabled by setting or clearing its enable bit. |
| – | IE.6 | Reserved |
| – | IE.5 | Reserved |
| ES | IE.4 | Serial Port interrupt enable bit |
| ET1 | IE.3 | Timer 1 interrupt enable bit |
| EX1 | IE.2 | External interrupt 1 enable bit |
| ET0 | IE.1 | Timer 0 interrupt enable bit |
| EX0 | IE.0 | External interrupt 0 enable bit |
| User software should never write 1s to reserved bits, because they may be used in future AT89 products. | | |

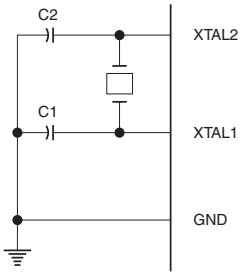
**Figure 10-1.** Interrupt Sources




## 11. Oscillator Characteristics

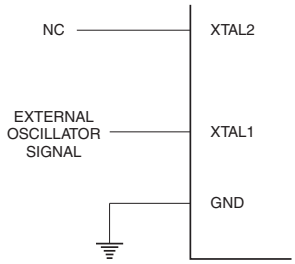
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier that can be configured for use as an on-chip oscillator, as shown in Figure 11-1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven, as shown in Figure 11-2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

**Figure 11-1.** Oscillator Connections




Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

**Figure 11-2.** External Clock Drive Configuration




## 12. Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special function registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

Note that when idle mode is terminated by a hardware reset, the device normally resumes program execution from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when idle mode is terminated by a reset, the instruction following the one that invokes idle mode should not write to a port pin or to external memory.

## 13. Power-down Mode

In the Power-down mode, the oscillator is stopped, and the instruction that invokes Power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the Power-down mode is terminated. Exit from Power-down mode can be initiated either by a hardware reset or by activation of an enabled external interrupt ($\overline{INT0}$ or $\overline{INT1}$). Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before $V_{CC}$ is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

**Table 13-1.** Status of External Pins During Idle and Power-down Modes

| Mode | Program Memory | ALE | $\overline{PSEN}$ | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power-down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power-down | External | 0 | 0 | Float | Data | Data | Data |

# 14. Program Memory Lock Bits

The AT89S51 has three lock bits that can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in Table 14-1.

**Table 14-1.** Lock Bit Protection Modes

| Program Lock Bits | | | | |
|---|---|---|---|---|
| | LB1 | LB2 | LB3 | Protection Type |
| 1 | U | U | U | No program lock features |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash memory is disabled |
| 3 | P | P | U | Same as mode 2, but verify is also disabled |
| 4 | P | P | P | Same as mode 3, but external execution is also disabled |

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value and holds that value until reset is activated. The latched value of $\overline{EA}$ must agree with the current logic level at that pin in order for the device to function properly.

# 15. Programming the Flash – Parallel Mode

The AT89S51 is shipped with the on-chip Flash memory array ready to be programmed. The programming interface needs a high-voltage (12-volt) program enable signal and is compatible with conventional third-party Flash or EPROM programmers.

The AT89S51 code memory array is programmed byte-by-byte.

**Programming Algorithm:** Before programming the AT89S51, the address, data, and control signals should be set up according to the Flash Programming Modes table (Table 17-1) and Figure 17-1 and Figure 17-2. To program the AT89S51, take the following steps:

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 50 µs. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

**$\overline{Data}$ Polling:** The AT89S51 features $\overline{Data}$ Polling to indicate the end of a byte write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written data on P0.7. Once the write cycle has been completed, true data is valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

**Ready/$\overline{Busy}$:** The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.0 is pulled low after ALE goes high during programming to indicate $\overline{BUSY}$. P3.0 is pulled high again when programming is done to indicate READY.

**Program Verify:** If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. **The status of the individual lock bits can be verified directly by reading them back.**

**Reading the Signature Bytes:** The signature bytes are read by the same procedure as a normal verification of locations 000H, 100H, and 200H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(000H) = 1EH indicates manufactured by Atmel
(100H) = 51H indicates AT89S51
(200H) = 06H

**Chip Erase:** In the parallel programming mode, a chip erase operation is initiated by using the proper combination of control signals and by pulsing ALE/$\overline{\text{PROG}}$ low for a duration of 200 ns - 500 ns.

In the serial programming mode, a chip erase operation is initiated by issuing the Chip Erase instruction. In this mode, chip erase is self-timed and takes about 500 ms.

During chip erase, a serial read from any address location will return 00H at the data output.

# 16. Programming the Flash – Serial Mode

The Code memory array can be programmed using the serial ISP interface while RST is pulled to $V_{CC}$. The serial interface consists of pins SCK, MOSI (input) and MISO (output). After RST is set high, the Programming Enable instruction needs to be executed first before other operations can be executed. Before a reprogramming sequence can occur, a Chip Erase operation is required.

The Chip Erase operation turns the content of every memory location in the Code array into FFH.

Either an external system clock can be supplied at pin XTAL1 or a crystal needs to be connected across pins XTAL1 and XTAL2. The maximum serial clock (SCK) frequency should be less than 1/16 of the crystal frequency. With a 33 MHz oscillator clock, the maximum SCK frequency is 2 MHz.

## 16.1 Serial Programming Algorithm

To program and verify the AT89S51 in the serial programming mode, the following sequence is recommended:

1. Power-up sequence:
   a. Apply power between VCC and GND pins.
   b. Set RST pin to “H”.

If a crystal is not connected across pins XTAL1 and XTAL2, apply a 3 MHz to 33 MHz clock to XTAL1 pin and wait for at least 10 milliseconds.

2. Enable serial programming by sending the Programming Enable serial instruction to pin MOSI/P1.5. The frequency of the shift clock supplied at pin SCK/P1.7 needs to be less than the CPU clock at XTAL1 divided by 16.
3. The Code array is programmed one byte at a time in either the Byte or Page mode. The write cycle is self-timed and typically takes less than 0.5 ms at 5V.
4. Any memory location can be verified by using the Read instruction that returns the content at the selected address at serial output MISO/P1.6.

5. At the end of a programming session, RST can be set low to commence normal device operation.

Power-off sequence (if needed):

1. Set XTAL1 to “L” (if a crystal is not used).
2. Set RST to “L”.
3. Turn $V_{CC}$ power off.

**Data Polling:** The $\overline{\text{Data}}$ Polling feature is also available in the serial mode. In this mode, during a write cycle an attempted read of the last byte written will result in the complement of the MSB of the serial output byte on MISO.

### 16.2 Serial Programming Instruction Set

The Instruction Set for Serial Programming follows a 4-byte protocol and is shown in the ”Serial Programming Instruction Set” on page 20.

## 17. Programming Interface – Parallel Mode

Every code byte in the Flash array can be programmed by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

Most major worldwide programming vendors offer worldwide support for the Atmel AT89 microcontroller series. Please contact your local programming vendor for the appropriate software revision.

**Table 17-1.** Flash Programming Modes

| Mode | $V_{CC}$ | RST | $\overline{\text{PSEN}}$ | ALE/ $\overline{\text{PROG}}$ | $\overline{\text{EA}}$/ $V_{PP}$ | P2.6 | P2.7 | P3.3 | P3.6 | P3.7 | P0.7-0 Data | P2.3-0 Address | P1.7-0 Address |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Write Code Data | 5V | H | L | (2) | 12V | L | H | H | H | H | $D_{IN}$ | A11-8 | A7-0 |
| Read Code Data | 5V | H | L | H | H | L | L | L | H | H | $D_{OUT}$ | A11-8 | A7-0 |
| Write Lock Bit 1 | 5V | H | L | (3) | 12V | H | H | H | H | H | X | X | X |
| Write Lock Bit 2 | 5V | H | L | (3) | 12V | H | H | H | L | L | X | X | X |
| Write Lock Bit 3 | 5V | H | L | (3) | 12V | H | L | H | H | L | X | X | X |
| Read Lock Bits 1, 2, 3 | 5V | H | L | H | H | H | H | L | H | L | P0.2, P0.3, P0.4 | X | X |
| Chip Erase | 5V | H | L | (1) | 12V | H | L | H | L | L | X | X | X |
| Read Atmel ID | 5V | H | L | H | H | L | L | L | L | L | 1EH | 0000 | 00H |
| Read Device ID | 5V | H | L | H | H | L | L | L | L | L | 51H | 0001 | 00H |
| Read Device ID | 5V | H | L | H | H | L | L | L | L | L | 06H | 0010 | 00H |

Notes:
1. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Chip Erase.
2. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Code Data.
3. Each $\overline{\text{PROG}}$ pulse is 200 ns - 500 ns for Write Lock Bits.
4. RDY/$\overline{\text{BSY}}$ signal is output on P3.0 during programming.
5. X = don’t care.

**Figure 17-1.** Programming the Flash Memory (Parallel Mode)

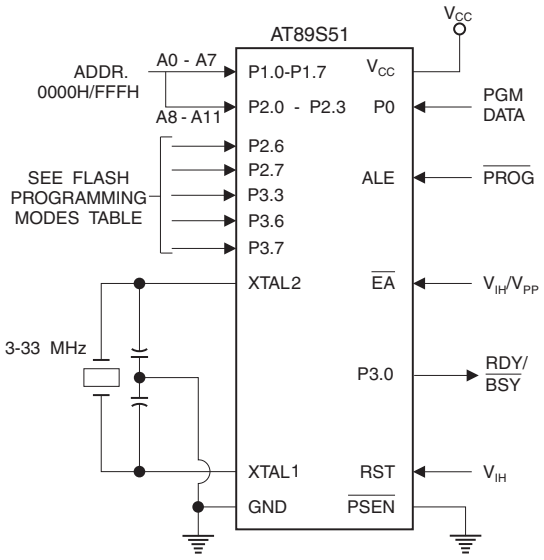
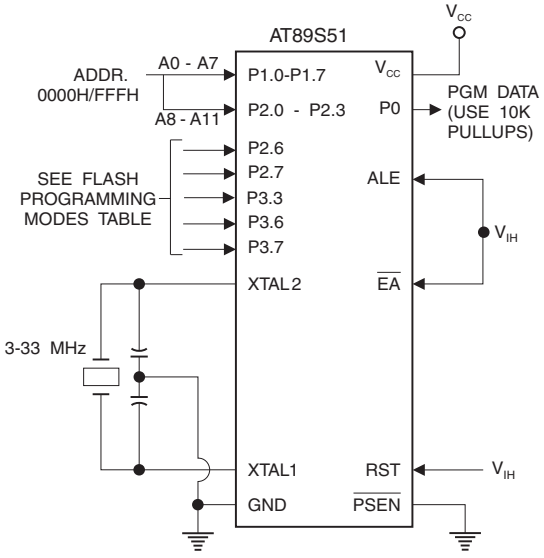



**Figure 17-2.** Verifying the Flash Memory (Parallel Mode)



# 18. Flash Programming and Verification Characteristics (Parallel Mode)

$T_A$ = 20°C to 30°C, $V_{CC}$ = 4.5 to 5.5V

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{PP}$ | Programming Supply Voltage | 11.5 | 12.5 | V |
| $I_{PP}$ | Programming Supply Current | | 10 | mA |
| $I_{CC}$ | $V_{CC}$ Supply Current | | 30 | mA |
| $1/t_{CLCL}$ | Oscillator Frequency | 3 | 33 | MHz |
| $t_{AVGL}$ | Address Setup to $\overline{PROG}$ Low | 48 $t_{CLCL}$ | | |
| $t_{GHAX}$ | Address Hold After $\overline{PROG}$ | 48 $t_{CLCL}$ | | |
| $t_{DVGL}$ | Data Setup to $\overline{PROG}$ Low | 48 $t_{CLCL}$ | | |
| $t_{GHDX}$ | Data Hold After $\overline{PROG}$ | 48 $t_{CLCL}$ | | |
| $t_{EHSH}$ | P2.7 ($\overline{ENABLE}$) High to $V_{PP}$ | 48 $t_{CLCL}$ | | |
| $t_{SHGL}$ | $V_{PP}$ Setup to $\overline{PROG}$ Low | 10 | | µs |
| $t_{GHSL}$ | $V_{PP}$ Hold After $\overline{PROG}$ | 10 | | µs |
| $t_{GLGH}$ | $\overline{PROG}$ Width | 0.2 | 1 | µs |
| $t_{AVQV}$ | Address to Data Valid | | 48$t_{CLCL}$ | |
| $t_{ELQV}$ | $\overline{ENABLE}$ Low to Data Valid | | 48$t_{CLCL}$ | |
| $t_{EHQZ}$ | Data Float After $\overline{ENABLE}$ | 0 | 48$t_{CLCL}$ | |
| $t_{GHBL}$ | $\overline{PROG}$ High to $\overline{BUSY}$ Low | | 1.0 | µs |
| $t_{WC}$ | Byte Write Cycle Time | | 50 | µs |

**Figure 18-1.** Flash Programming and Verification Waveforms – Parallel Mode

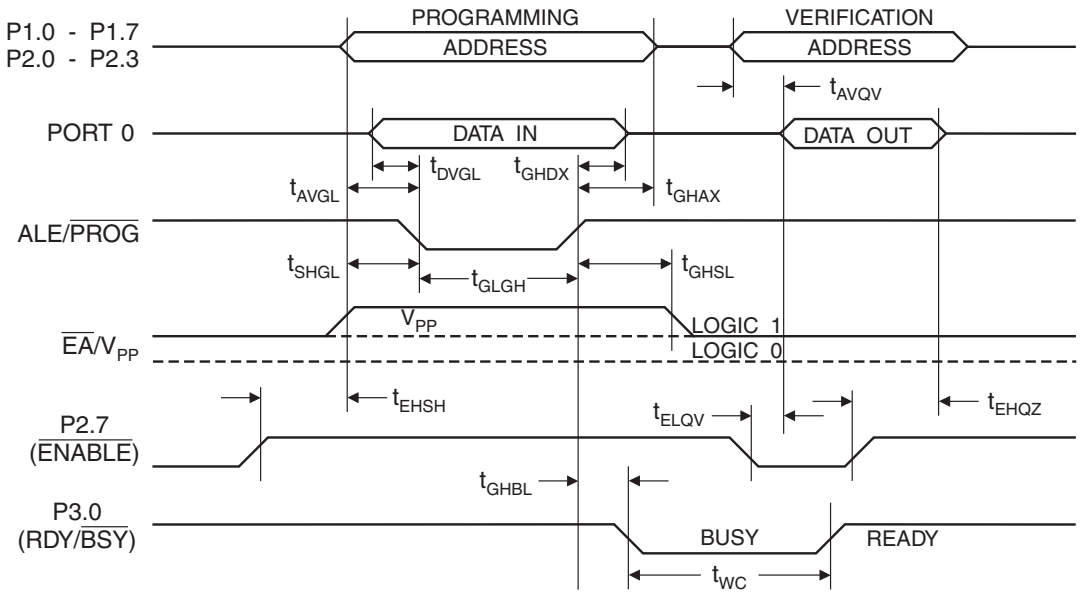
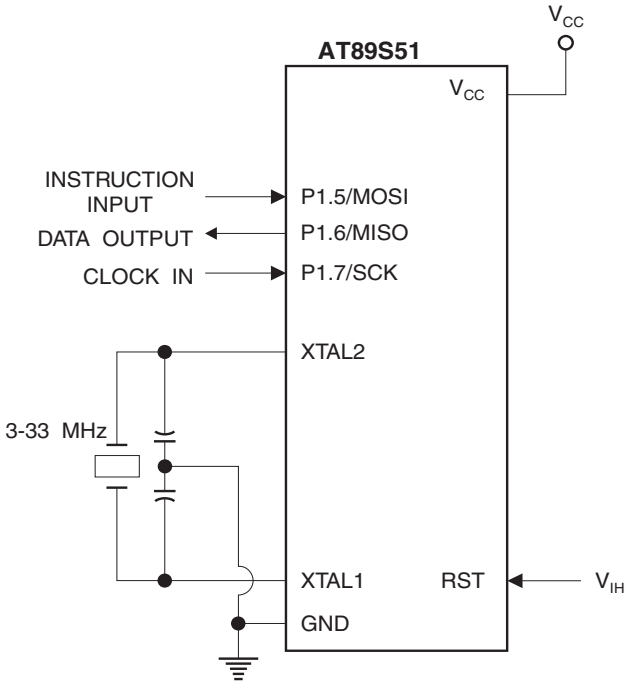
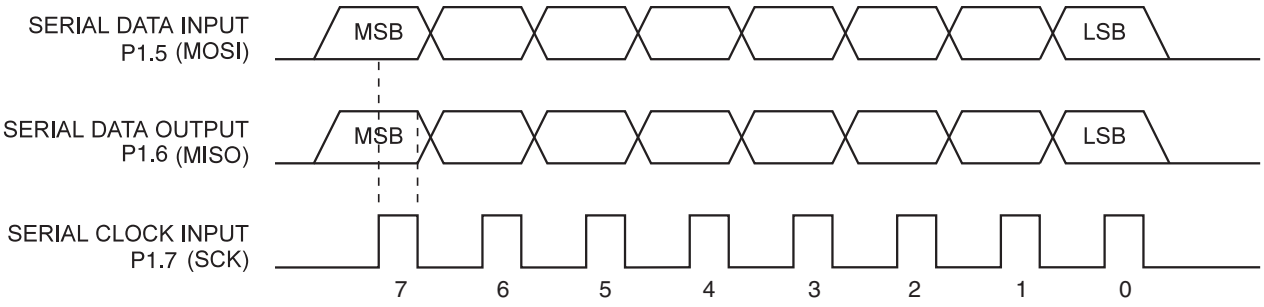


**Figure 18-2.** Flash Memory Serial Downloading




## 19. Flash Programming and Verification Waveforms – Serial Mode

**Figure 19-1.** Serial Programming Waveforms



## 20. Serial Programming Instruction Set

| Instruction | Instruction Format | | | | Operation |
|---|---|---|---|---|---|
| | Byte 1 | Byte 2 | Byte 3 | Byte 4 | |
| Programming Enable | 1010 1100 | 0101 0011 | xxxx xxxx | xxxx xxxx<br>0110 1001<br>(Output on MISO) | Enable Serial Programming while RST is high |
| Chip Erase | 1010 1100 | 100x xxxx | xxxx xxxx | xxxx xxxx | Chip Erase Flash memory array |
| Read Program Memory (Byte Mode) | 0010 0000 | xxxx A11 A10 A9 A8 | A7 A6 A5 A4 A3 A2 A1 A0 | D7 D6 D5 D4 D3 D2 D1 D0 | Read data from Program memory in the byte mode |
| Write Program Memory (Byte Mode) | 0100 0000 | xxxx A11 A10 A9 A8 | A7 A6 A5 A4 A3 A2 A1 A0 | D7 D6 D5 D4 D3 D2 D1 D0 | Write data to Program memory in the byte mode |
| Write Lock Bits[1] | 1010 1100 | 1110 00 B1 B2 | xxxx xxxx | xxxx xxxx | Write Lock bits. See Note (1). |
| Read Lock Bits | 0010 0100 | xxxx xxxx | xxxx xxxx | xx LB3 LB2 LB1 xx | Read back current status of the lock bits (a programmed lock bit reads back as a “1”) |
| Read Signature Bytes | 0010 1000 | xxxx A11 A10 A9 A8 | A7 xxx xxx0 | Signature Byte | Read Signature Byte |
| Read Program Memory (Page Mode) | 0011 0000 | xxxx A11 A10 A9 A8 | Byte 0 | Byte 1...<br>Byte 255 | Read data from Program memory in the Page Mode (256 bytes) |
| Write Program Memory (Page Mode) | 0101 0000 | xxxx A11 A10 A9 A8 | Byte 0 | Byte 1...<br>Byte 255 | Write data to Program memory in the Page Mode (256 bytes) |

Note: 1. B1 = 0, B2 = 0 → Mode 1, no lock protection
B1 = 0, B2 = 1 → Mode 2, lock bit 1 activated
B1 = 1, B2 = 0 → Mode 3, lock bit 2 activated
B1 = 1, B2 = 1 → Mode 4, lock bit 3 activated

} Each of the lock bit modes need to be activated sequentially before Mode 4 can be executed.

After Reset signal is high, SCK should be low for at least 64 system clocks before it goes high to clock in the enable data bytes. No pulsing of Reset signal is necessary. SCK should be no faster than 1/16 of the system clock at XTAL1.

For Page Read/Write, the data always starts from byte 0 to 255. After the command byte and upper address byte are latched, each byte thereafter is treated as data until all 256 bytes are shifted in/out. Then the next instruction will be ready to be decoded.

## 21. Serial Programming Characteristics

**Figure 21-1.** Serial Programming Timing

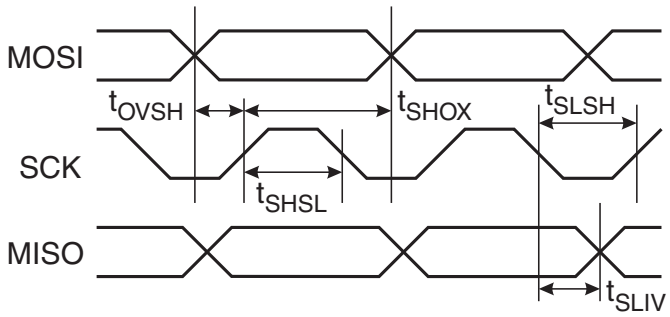



**Table 21-1.** Serial Programming Characteristics, $T_A$ = -40· C to 85· C, $V_{CC}$ = 4.0 - 5.5V (Unless Otherwise Noted)

| Symbol | Parameter | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| $1/t_{CLCL}$ | Oscillator Frequency | 3 | | 33 | MHz |
| $t_{CLCL}$ | Oscillator Period | 30 | | | ns |
| $t_{SHSL}$ | SCK Pulse Width High | 8 $t_{CLCL}$ | | | ns |
| $t_{SLSH}$ | SCK Pulse Width Low | 8 $t_{CLCL}$ | | | ns |
| $t_{OVSH}$ | MOSI Setup to SCK High | $t_{CLCL}$ | | | ns |
| $t_{SHOX}$ | MOSI Hold after SCK High | 2 $t_{CLCL}$ | | | ns |
| $t_{SLIV}$ | SCK Low to MISO Valid | 10 | 16 | 32 | ns |
| $t_{ERASE}$ | Chip Erase Instruction Cycle Time | | | 500 | ms |
| $t_{SWC}$ | Serial Byte Write Cycle Time | | | 64 $t_{CLCL}$ + 400 | µs |

## 22. Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -1.0V to +7.0V |
| Maximum Operating Voltage | 6.6V |
| DC Output Current | 15.0 mA |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

# 23. DC Characteristics

The values shown in this table are valid for $T_A$ = -40°C to 85°C and $V_{CC}$ = 4.0V to 5.5V, unless otherwise noted.

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | (Except $\overline{EA}$) | -0.5 | 0.2 $V_{CC}$-0.1 | V |
| $V_{IL1}$ | Input Low Voltage ($\overline{EA}$) | | -0.5 | 0.2 $V_{CC}$-0.3 | V |
| $V_{IH}$ | Input High Voltage | (Except XTAL1, RST) | 0.2 $V_{CC}$+0.9 | $V_{CC}$+0.5 | V |
| $V_{IH1}$ | Input High Voltage | (XTAL1, RST) | 0.7 $V_{CC}$ | $V_{CC}$+0.5 | V |
| $V_{OL}$ | Output Low Voltage[1] (Ports 1,2,3) | $I_{OL}$ = 1.6 mA | | 0.45 | V |
| $V_{OL1}$ | Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$) | $I_{OL}$ = 3.2 mA | | 0.45 | V |
| $V_{OH}$ | Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$) | $I_{OH}$ = -60 µA, $V_{CC}$ = 5V ±10% | 2.4 | | V |
| | | $I_{OH}$ = -25 µA | 0.75 $V_{CC}$ | | V |
| | | $I_{OH}$ = -10 µA | 0.9 $V_{CC}$ | | V |
| $V_{OH1}$ | Output High Voltage (Port 0 in External Bus Mode) | $I_{OH}$ = -800 µA, $V_{CC}$ = 5V ±10% | 2.4 | | V |
| | | $I_{OH}$ = -300 µA | 0.75 $V_{CC}$ | | V |
| | | $I_{OH}$ = -80 µA | 0.9 $V_{CC}$ | | V |
| $I_{IL}$ | Logical 0 Input Current (Ports 1,2,3) | $V_{IN}$ = 0.45V | | -50 | µA |
| $I_{TL}$ | Logical 1 to 0 Transition Current (Ports 1,2,3) | $V_{IN}$ = 2V, $V_{CC}$ = 5V ±10% | | -300 | µA |
| $I_{LI}$ | Input Leakage Current (Port 0, $\overline{EA}$) | 0.45 < $V_{IN}$ < $V_{CC}$ | | ±10 | µA |
| RRST | Reset Pulldown Resistor | | 50 | 300 | KΩ |
| $C_{IO}$ | Pin Capacitance | Test Freq. = 1 MHz, $T_A$ = 25°C | | 10 | pF |
| $I_{CC}$ | Power Supply Current | Active Mode, 12 MHz | | 25 | mA |
| | | Idle Mode, 12 MHz | | 6.5 | mA |
| | Power-down Mode[2] | $V_{CC}$ = 5.5V | | 50 | µA |

Notes:
1. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
   Maximum $I_{OL}$ per port pin: 10 mA
   Maximum $I_{OL}$ per 8-bit port:
   Port 0: 26 mA  Ports 1, 2, 3: 15 mA
   Maximum total $I_{OL}$ for all output pins: 71 mA
   If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum $V_{CC}$ for Power-down is 2V.

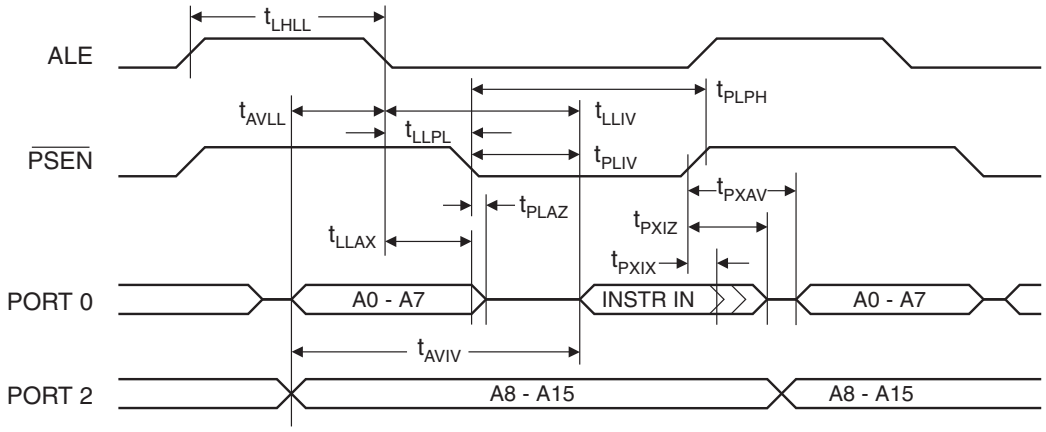
# 24. AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

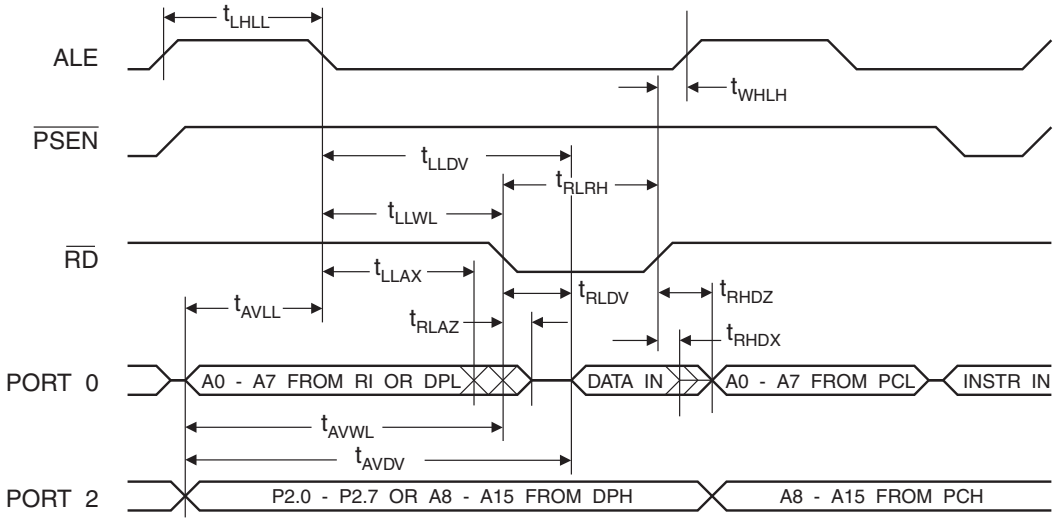
## 24.1 External Program and Data Memory Characteristics

| Symbol | Parameter | 12 MHz Oscillator | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | Oscillator Frequency | | | 0 | 33 | MHz |
| $t_{LHLL}$ | ALE Pulse Width | 127 | | $2\ t_{CLCL}-40$ | | ns |
| $t_{AVLL}$ | Address Valid to ALE Low | 43 | | $t_{CLCL}-25$ | | ns |
| $t_{LLAX}$ | Address Hold After ALE Low | 48 | | $t_{CLCL}-25$ | | ns |
| $t_{LLIV}$ | ALE Low to Valid Instruction In | | 233 | | $4\ t_{CLCL}-65$ | ns |
| $t_{LLPL}$ | ALE Low to $\overline{PSEN}$ Low | 43 | | $t_{CLCL}-25$ | | ns |
| $t_{PLPH}$ | $\overline{PSEN}$ Pulse Width | 205 | | $3\ t_{CLCL}-45$ | | ns |
| $t_{PLIV}$ | $\overline{PSEN}$ Low to Valid Instruction In | | 145 | | $3\ t_{CLCL}-60$ | ns |
| $t_{PXIX}$ | Input Instruction Hold After $\overline{PSEN}$ | 0 | | 0 | | ns |
| $t_{PXIZ}$ | Input Instruction Float After $\overline{PSEN}$ | | 59 | | $t_{CLCL}-25$ | ns |
| $t_{PXAV}$ | $\overline{PSEN}$ to Address Valid | 75 | | $t_{CLCL}-8$ | | ns |
| $t_{AVIV}$ | Address to Valid Instruction In | | 312 | | $5\ t_{CLCL}-80$ | ns |
| $t_{PLAZ}$ | $\overline{PSEN}$ Low to Address Float | | 10 | | 10 | ns |
| $t_{RLRH}$ | $\overline{RD}$ Pulse Width | 400 | | $6\ t_{CLCL}-100$ | | ns |
| $t_{WLWH}$ | $\overline{WR}$ Pulse Width | 400 | | $6\ t_{CLCL}-100$ | | ns |
| $t_{RLDV}$ | $\overline{RD}$ Low to Valid Data In | | 252 | | $5\ t_{CLCL}-90$ | ns |
| $t_{RHDX}$ | Data Hold After $\overline{RD}$ | 0 | | 0 | | ns |
| $t_{RHDZ}$ | Data Float After $\overline{RD}$ | | 97 | | $2\ t_{CLCL}-28$ | ns |
| $t_{LLDV}$ | ALE Low to Valid Data In | | 517 | | $8\ t_{CLCL}-150$ | ns |
| $t_{AVDV}$ | Address to Valid Data In | | 585 | | $9\ t_{CLCL}-165$ | ns |
| $t_{LLWL}$ | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | 200 | 300 | $3\ t_{CLCL}-50$ | $3\ t_{CLCL}+50$ | ns |
| $t_{AVWL}$ | Address to $\overline{RD}$ or $\overline{WR}$ Low | 203 | | $4\ t_{CLCL}-75$ | | ns |
| $t_{QVWX}$ | Data Valid to $\overline{WR}$ Transition | 23 | | $t_{CLCL}-30$ | | ns |
| $t_{QVWH}$ | Data Valid to $\overline{WR}$ High | 433 | | $7\ t_{CLCL}-130$ | | ns |
| $t_{WHQX}$ | Data Hold After $\overline{WR}$ | 33 | | $t_{CLCL}-25$ | | ns |
| $t_{RLAZ}$ | $\overline{RD}$ Low to Address Float | | 0 | | 0 | ns |
| $t_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE High | 43 | 123 | $t_{CLCL}-25$ | $t_{CLCL}+25$ | ns |

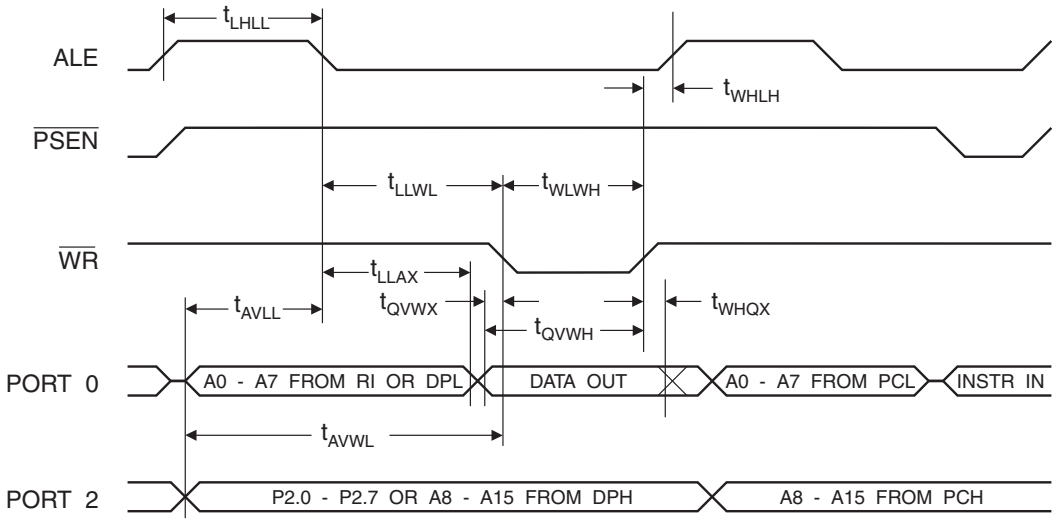
## 25. External Program Memory Read Cycle



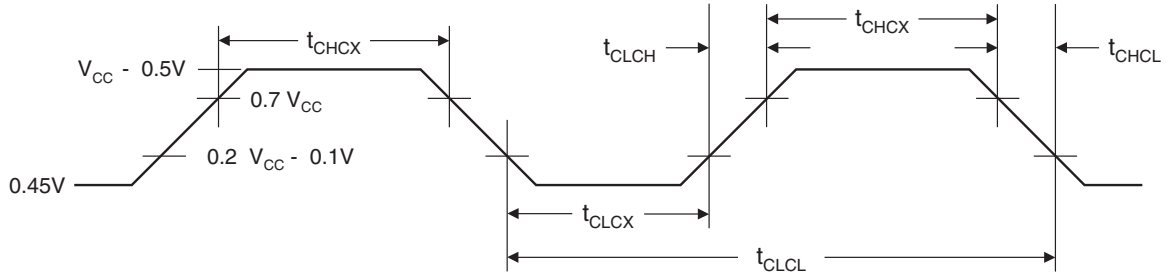

## 26. External Data Memory Read Cycle



## 27. External Data Memory Write Cycle




## 28. External Clock Drive Waveforms




## 29. External Clock Drive

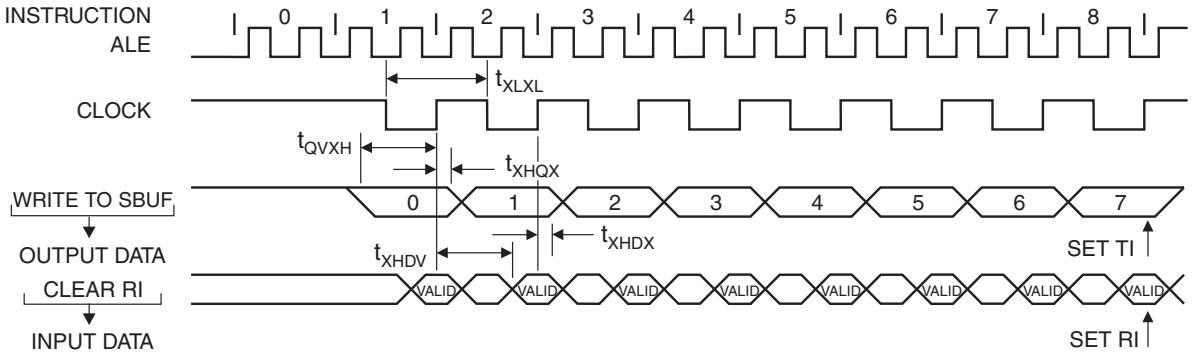
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $1/t_{CLCL}$ | Oscillator Frequency | 0 | 33 | MHz |
| $t_{CLCL}$ | Clock Period | 30 | | ns |
| $t_{CHCX}$ | High Time | 12 | | ns |
| $t_{CLCX}$ | Low Time | 12 | | ns |
| $t_{CLCH}$ | Rise Time | | 5 | ns |
| $t_{CHCL}$ | Fall Time | | 5 | ns |

## 30. Serial Port Timing: Shift Register Mode Test Conditions

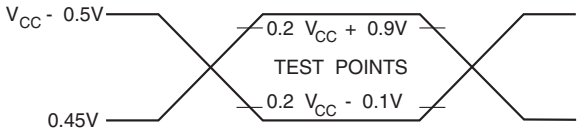
The values in this table are valid for $V_{CC}$ = 4.0V to 5.5V and Load Capacitance = 80 pF.

| Symbol | Parameter | 12 MHz Osc | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{XLXL}$ | Serial Port Clock Cycle Time | 1.0 | | 12 $t_{CLCL}$ | | µs |
| $t_{QVXH}$ | Output Data Setup to Clock Rising Edge | 700 | | 10 $t_{CLCL}$-133 | | ns |
| $t_{XHQX}$ | Output Data Hold After Clock Rising Edge | 50 | | 2 $t_{CLCL}$-80 | | ns |
| $t_{XHDX}$ | Input Data Hold After Clock Rising Edge | 0 | | 0 | | ns |
| $t_{XHDV}$ | Clock Rising Edge to Input Data Valid | | 700 | | 10 $t_{CLCL}$-133 | ns |

## 31. Shift Register Mode Timing Waveforms

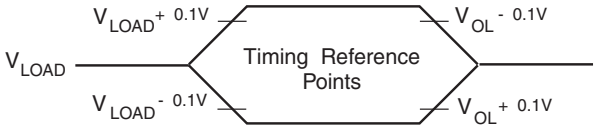



## 32. AC Testing Input/Output Waveforms[1]




Note: 1. AC Inputs during testing are driven at $V_{CC}$ - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at $V_{IH}$ min. for a logic 1 and $V_{IL}$ max. for a logic 0.

## 33. Float Waveforms[1]




Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded $V_{OH}$/$V_{OL}$ level occurs.

# 34. Ordering Information

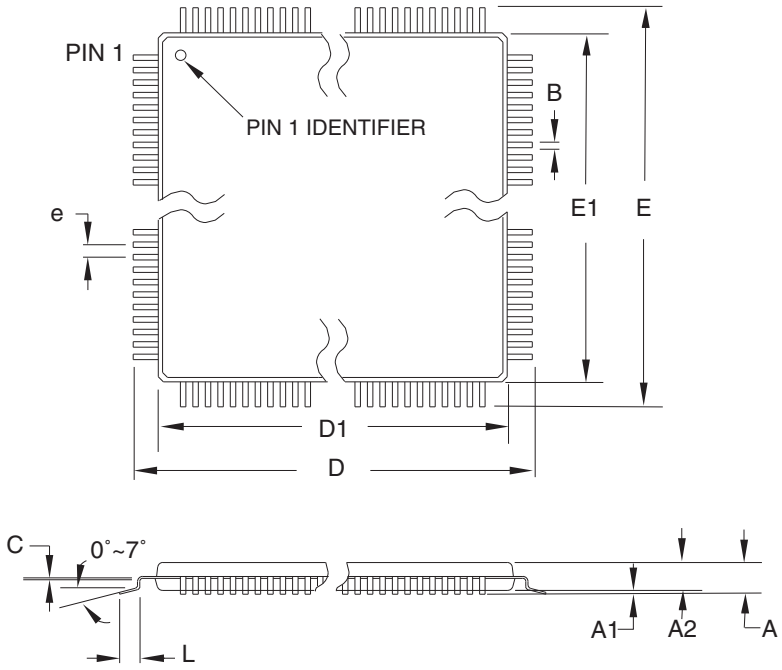
## 34.1 Green Package Option (Pb/Halide-free)

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|---|---|---|---|---|
| 24 | 4.0V to 5.5V | AT89S51-24AU<br>AT89S51-24JU<br>AT89S51-24PU | 44A<br>44J<br>40P6 | Industrial<br>(-40° C to 85° C) |
| 33 | 4.5V to 5.5V | AT89S51-33AU<br>AT89S51-33JU<br>AT89S51-33PU | 44A<br>44J<br>40P6 | Industrial<br>(-40° C to 85° C) |

| Package Type | |
|---|---|
| **44A** | 44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP) |
| **44J** | 44-lead, Plastic J-leaded Chip Carrier (PLCC) |
| **40P6** | 40-pin, 0.600" Wide, Plastic Dual Inline Package (PDIP) |

# 35. Packaging Information

## 35.1 44A – TQFP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

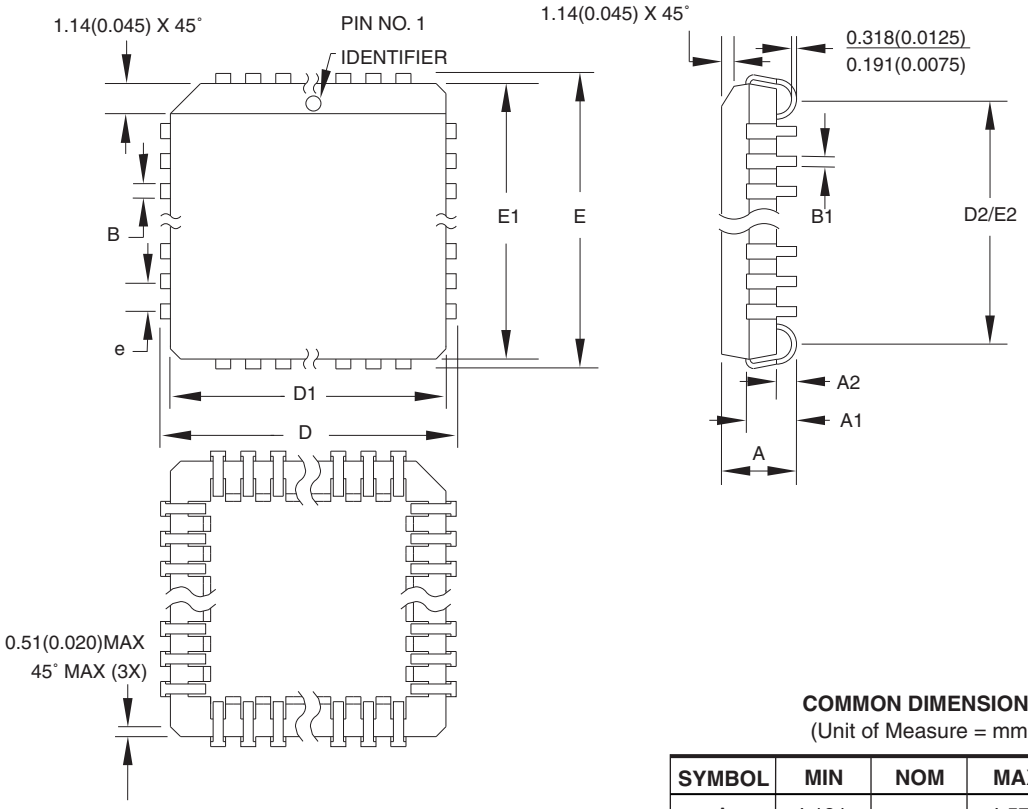
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 11.75 | 12.00 | 12.25 | |
| D1 | 9.90 | 10.00 | 10.10 | Note 2 |
| E | 11.75 | 12.00 | 12.25 | |
| E1 | 9.90 | 10.00 | 10.10 | Note 2 |
| B | 0.30 | – | 0.45 | |
| C | 0.09 | – | 0.20 | |
| L | 0.45 | – | 0.75 | |
| e | 0.80 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10 mm maximum.

10/5/2001

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **44A,** 44-lead, 10 x 10 mm Body Size, 1.0 mm Body Thickness, 0.8 mm Lead Pitch, Thin Profile Plastic Quad Flat Package (TQFP) | 44A | B |

## 35.2 44J – PLCC




**COMMON DIMENSIONS**
(Unit of Measure = mm)

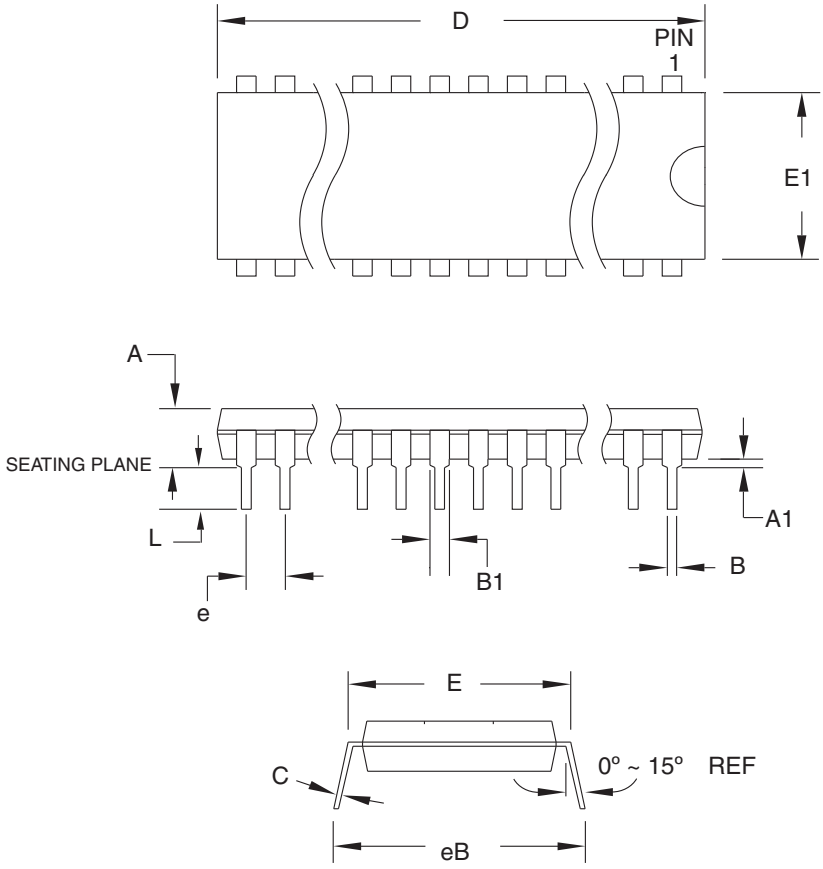
| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | 4.191 | – | 4.572 | |
| A1 | 2.286 | – | 3.048 | |
| A2 | 0.508 | – | – | |
| D | 17.399 | – | 17.653 | |
| D1 | 16.510 | – | 16.662 | Note 2 |
| E | 17.399 | – | 17.653 | |
| E1 | 16.510 | – | 16.662 | Note 2 |
| D2/E2 | 14.986 | – | 16.002 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **44J**, 44-lead, Plastic J-leaded Chip Carrier (PLCC) | 44J | B |

## 35.3 40P6 – PDIP




**COMMON DIMENSIONS**
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|---|---|---|---|---|
| A | – | – | 4.826 | |
| A1 | 0.381 | – | – | |
| D | 52.070 | – | 52.578 | Note 2 |
| E | 15.240 | – | 15.875 | |
| E1 | 13.462 | – | 13.970 | Note 2 |
| B | 0.356 | – | 0.559 | |
| B1 | 1.041 | – | 1.651 | |
| L | 3.048 | – | 3.556 | |
| C | 0.203 | – | 0.381 | |
| eB | 15.494 | – | 17.526 | |
| e | 2.540 TYP | | | |

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

| | TITLE | DRAWING NO. | REV. |
|---|---|---|---|
| 2325 Orchard Parkway<br>San Jose, CA 95131 | **40P6**, 40-lead (0.600"/15.24 mm Wide) Plastic Dual Inline Package (PDIP) | 40P6 | B |

## Headquarters

***Atmel Corporation***
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

## International

***Atmel Asia***
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

***Atmel Europe***
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

***Atmel Japan***
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

## Product Contact

***Web Site***
www.atmel.com

***Technical Support***
mcu@atmel.com

***Sales Contact***
www.atmel.com/contacts

***Literature Requests***
www.atmel.com/literature

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View AT89S51-24PI on WIN SOURCE
- Atmel Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management