8-BIT MICROCONTROLLER

Table of Contents-

1 GENERAL DESCRIPTION

The W79E4051/2051 series are an 8-bit Turbo 51 microcontroller which has an in-system programmable Flash EPROM which Flash EPROM can program by **ICP (In Circuit Program) Writer**. The instruction set of the W79E4051/2051 series are fully compatible with the standard 8052. The W79E4051/2051 series contain a **4K/2K** bytes of program Flash EPROM; a **256** bytes of RAM; **128** bytes data Flash EPROM for customer data storage; two 8-bit bi-directional and bit-addressable I/O ports; two 16-bit timer/counters; an enhanced full duplex serial port; 1 channel PWM by 10-bit counter, Brownout voltage detection/reset, Power on reset detection and one analog comparator. These peripherals are supported by **9** sources of four-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W79E4051/2051 series allow the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

2 FEATURES

- Fully static design 8-bit Turbo 51 CMOS microcontroller up to 24MHz
- Single power: 2.4~5.5V Up to 12MHz, 4.5~5.5V up to 24MHz
- Flexible CPU clock source configurable by config bit and software:
  - High speed external oscillator: upto 24MHz Crystal and resonator (enabled by config bit).
  - Internal RC oscillator: 22.1184/11.0592MHz with ±2% accuracy (selectable by config bit), at 5.0 voltage and 25℃condition, for W79E2051R and W79E4051R
- Instruction-set compatible with MCS-51
- **4K/2K** bytes of Program Flash EPROM, with ICP and external writer programmable mode.
- **256** bytes of on-chip RAM
- W79E4051/2051 supports **128** bytes Data Flash EPROM for customer data storage used and 10K writer cycles.
  - 8 pages. Page size is 16 bytes.
  - Data Flash program/erase V_{DD}=3.0V to 5.5V
- **One 8-bit** bi-directional port(Port1), **one 7-bit** bi-directional port(Port3) and **one 2-bit** bi-directional port(P2.0 and P2.1 shared with XT1 and XT2 pins)
- I/O capable of driving LED max. 20mA per pin, max to 80mA for total pins.
- **Two** 16-bit timer/counters
- **9** Interrupt source with four levels of priority
- **One** enhanced full duplex serial port with framing error detection and automatic address recognition
- **One** channel 10-bit PWM output
- **One** analog Comparator
- Built-in Power Management
  - Power on reset flag
  - Brownout voltage detect/reset
- Operating Temperature: -40~85℃
- Packages:
  - Lead Free (RoHS) PDIP 20: W79E4051AKG
  - Lead Free (RoHS) SOP 20: W79E4051ASG
  - Lead Free (RoHS) SSOP 20: W79E4051ARG
  - Lead Free (RoHS) PDIP 20: W79E2051AKG
  - Lead Free (RoHS) SOP 20: W79E2051ASG
  - Lead Free (RoHS) SSOP 20: W79E2051ARG
  - Lead Free (RoHS) PDIP 20: W79E4051RAKG
  - Lead Free (RoHS) SOP 20: W79E4051RASG
  - Lead Free (RoHS) SSOP 20: W79E4051RARG

- Lead Free (RoHS) PDIP 20: W79E2051RAKG
- Lead Free (RoHS) SOP 20: W79E2051RASG
- Lead Free (RoHS) SSOP 20: W79E2051RARG

3 PARTS INFORMATION LIST

3.1 Lead Free (RoHS) Parts information list

Table 3-1: Lead Free (RoHS) Parts information list

PART NO.	PROGRAM FLASH EPROM	RAM	DATA FLASH EPROM	INTERNAL RC OSCILLATOR ACCURACY[1]	PACKAGE
W79E4051AKG	4KB	256B	128B	22MHz ± 25%	PDIP-20 Pin
W79E4051ASG	4KB	256B	128B	22MHz ± 25%	SOP-20 Pin
W79E4051ARG	4KB	256B	128B	22MHz ± 25%	SSOP-20 Pin
W79E2051AKG	2KB	256B	128B	22MHz ± 25%	PDIP-20 Pin
W79E2051ASG	2KB	256B	128B	22MHz ± 25%	SOP-20 Pin
W79E2051ARG	2KB	256B	128B	22MHz ± 25%	SSOP-20 Pin
W79E4051RAKG	4KB	256B	128B	22.1184MHz ± 2%	PDIP-20 Pin
W79E4051RASG	4KB	256B	128B	22.1184MHz ± 2%	SOP-20 Pin
W79E4051RARG	4KB	256B	128B	22.1184MHz ± 2%	SSOP-20 Pin
W79E2051RAKG	2KB	256B	128B	22.1184MHz ± 2%	PDIP-20 Pin
W79E2051RASG	2KB	256B	128B	22.1184MHz ± 2%	SOP-20 Pin
W79E2051RARG	2KB	256B	128B	22.1184MHz ± 2%	SSOP-20 Pin

Note:

1. Factory calibration condition: V_{DD}=5.0V, TA = 25°C

4 PIN CONFIGURATION

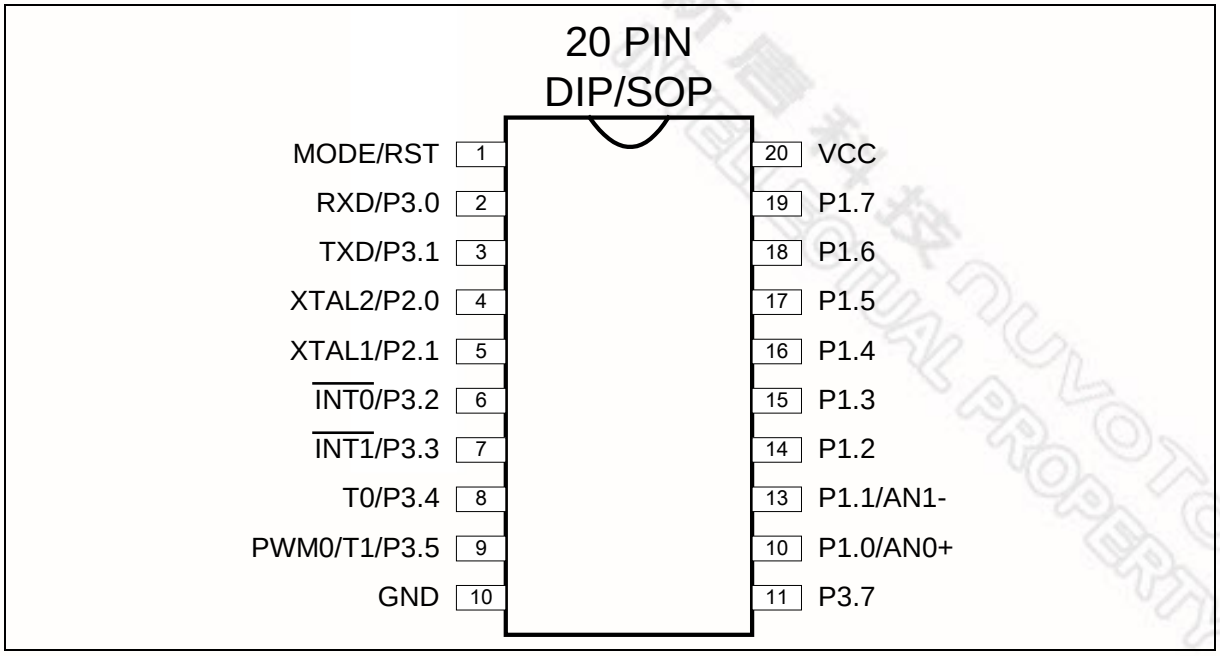


Table 4-1: Pin Configuration

5 PIN DESCRIPTION

SYMBOL	Alternate Function 1	Alternate function 2	Alternate function 3 (ICP mode)	Type		DESCRIPTIONS
P2.1	X1			I/O	I	**CRYSTAL1**: This is the crystal oscillator input. This pin may be driven by an external clock or configurable i/o pin.
P2.0	X2/CLKOUT			I/O	O	**CRYSTAL2**: This is the crystal oscillator output. It is the inversion of XTAL1. Also a configurable i/o pin.
VDD	-			P		**POWER SUPPLY**: Supply voltage for operation.
VSS	-			P		**GROUND**: Ground potential.
RST			MODE	I		**RESET**: A high on this pin for two machine cycles while the oscillator is running resets the device. MODE: used in ICP mode.
P1.0	AN0+			I/O, D		**Port1**: 8-bit bi-directional I/O port with internal weakly pull-ups. P1.0~P1.1 are open-drain mode after reset. Multifunction pins: AN0+ and AN1- are analog comparator inputs. Data and SCK are used in ICP mode.
P1.1	AN1-			I/O, D		
P1.2				I/O		
P1.3				I/O		
P1.4				I/O		
P1.5				I/O		
P1.6			Data	I/O		
P1.7			SCK	I/O		
P3.0	RXD			I/O		**Port3**: 7-bit bi-directional I/O port, P3.0~P3.7 except P3.6, with internal weakly pull-ups. P3.6 is internal wired to analog comparator output. Multifunction pins for TXD & RXD (UART),/INT0-1, T0, T1/PWM0.
P3.1	TXD			I/O		
P3.2	/INT0			I/O		
P3.3	/INT1			I/O		
P3.4	T0			I/O		
P3.5	T1	PWM0		I/O		
P3.6				S		
P3.7				I/O		

* Note : **TYPE P**: Power, I: input, **O**: output, **I/O**: bi-directional, **S**: internal Signal.

6 FUNCTIONAL DESCRIPTION

The W79E4051/2051 architecture consist of a 4T 8051 core controller surrounded by various registers, **4K/2K** bytes AP Flash EPROM, **256** bytes of RAM, **128** bytes Data Flash EPROM, three general purpose I/O ports, two timer/counters, one serial port, Flash EPROM program by Writer and ICP.

6.1 On-Chip Flash EPROM

The W79E4051/2051 includes one **4K/2K** bytes of main Flash EPROM for application program. A Writer or ICP programming board is required to program the AP Flash EPROM and Data Flash EPROM.

This ICP (In-Circuit Programming) feature makes the job easy and efficient when the application's firmware needs to be updated frequently. In some applications, the in-circuit programming feature makes it possible for the end-user to easily update the system firmware without opening the chassis.

6.2 I/O Ports

W79E4051/2051 has one 8-bit, one 7-bit and one 2-bit ports using on-chip oscillator by reset options. Except P1.0 and P1.1, all ports are in quasi-bidirectional structure that the internal weakly pull-ups are present as the port registers are set to logic one. P1.0~P1.1, the alternate function are analog comparator inputs, stays in PMOS-off open-drain mode after CPU reset.

6.3 Serial I/O

The W79E4051/2051 has one serial port that is functionally similar to the serial port of the original 8051 family. However the serial port on the W79E4051/2051 can operate in different modes in order to obtain timing similarity as well. The Serial port has the enhanced features of Automatic Address recognition and Frame Error detection.

6.4 Timers

The W79E4051/2051 has two 16-bit timers that are functionally and similar to the timers of the 8051 family. When used as timers, user has a choice to set 12 or 6 clocks per count that emulates the timing of the original 8051. Each timer's count value is stored in two SFR locations that can be written or read by software. There are also some other SFRs associated with the timers that control their mode and operation.

6.5 Interrupts

The Interrupt structure in the W79E4051/2051 is slightly different from that of the standard 8051. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased.

6.6 Data Pointers

The data pointer of W79E4051/2051 is similar to standard 8051 but has dual 16-bit Data Pointers (DPTR) by setting DPS of AUXR2.0. In addition there is an added instruction, DEC DPTR (op-code A5H), which helps in improving programming flexibility for the user.

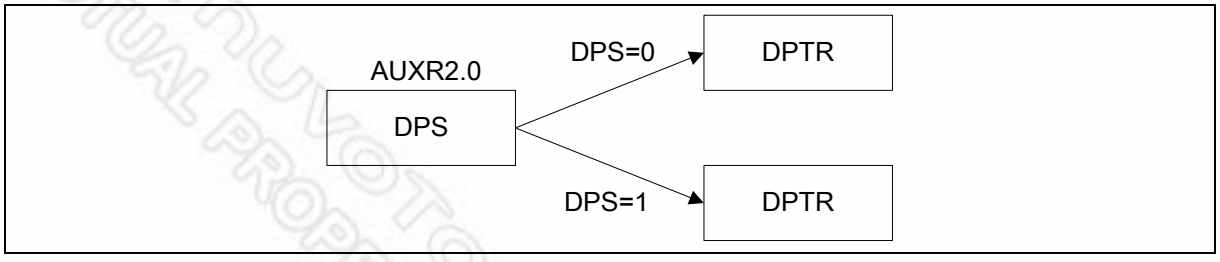


Table 6-1: Data Pointer

6.7 Architecture

The W79E4051/2051 is based on the standard MCS-51 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard MCS-51 instruction set.

6.7.1 ALU

The ALU is the heart of the W79E4051/2051. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump address. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used in Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

6.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W79E4051/2051. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

6.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

6.7.4 Program Status Word:

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

6.7.5 Scratch-pad RAM

The W79E4051/2051 has a 256 byte on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit addressable, and can be directly addressed for this purpose.

6.7.6 Stack Pointer

The W79E4051/2051 has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W79E4051/2051. Hence the size of the stack is limited by the size of this RAM.

7 MEMORY ORGANIZATION

The W79E4051/2051 series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

7.1 Program Memory (on-chip Flash)

The Program Memory on the W79E4051/2051 series can be up to **4K/2K** bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

7.2 Data Flash Memory

The Data Flash EPROM on the W79E4051/2051 series is **128** bytes long with page size of **16** bytes. The W79E4051/2051 series read the content of data memory by using "MOVC A, @A+DPTR". To write data is by NVMADDRL, NVMDATA and NVMCON SFR's registers.

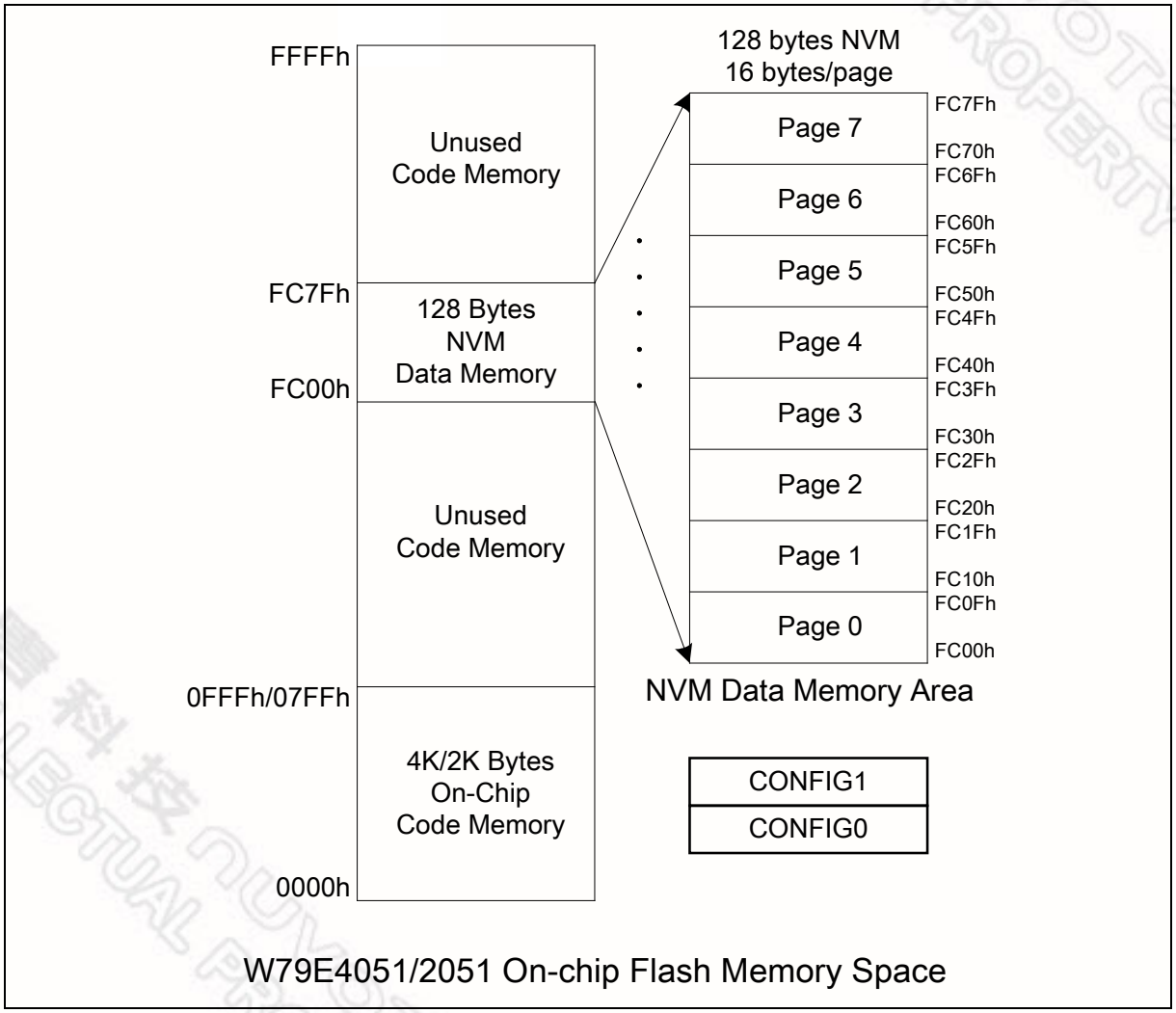


Table 7-1 W79E4051/2051 On-chip Flash Memory Map

7.3 Scratch-pad RAM and Register Map

As mentioned before the W79E4051/2051 series have separate Program and Data Memory areas. The on-chip **256** bytes scratch pad RAM is built in W79E4051/2051. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

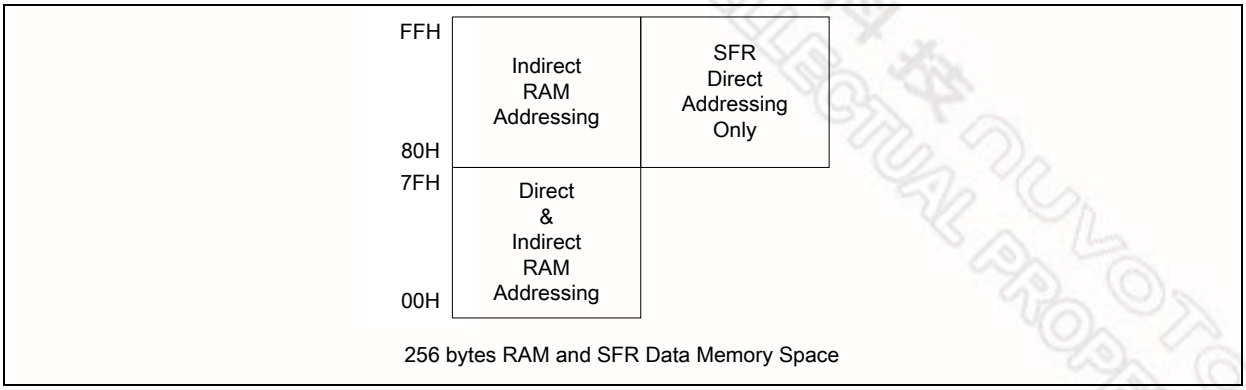


Table 7-2 W79E4051/2051 256 bytes RAM and SFR memory map

Since the scratch-pad RAM is **256** bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

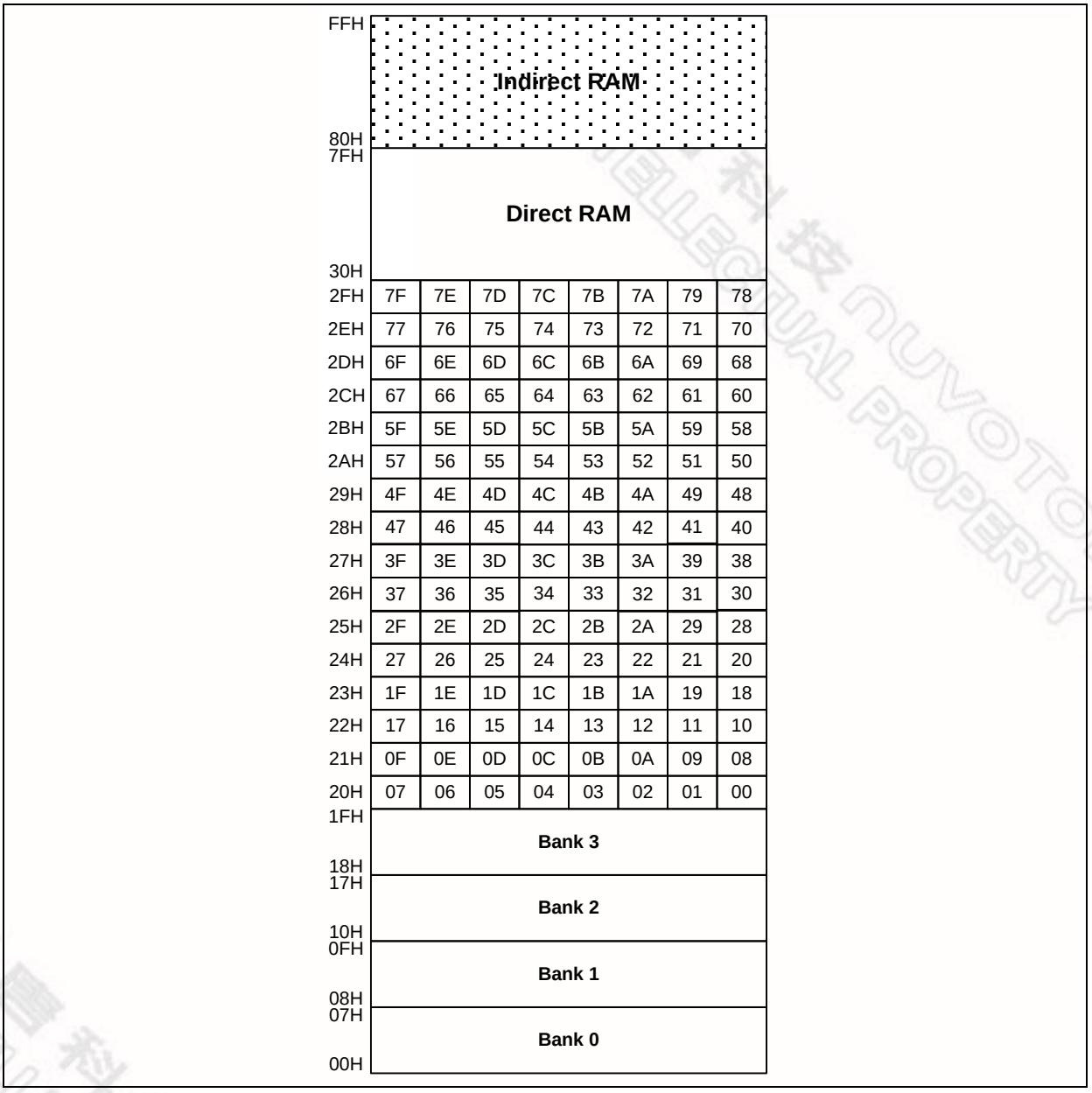


Table 7-3 Scratch-pad RAM

7.4 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W79E4051/2051 series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

7.5 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

7.6 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

8 SPECIAL FUNCTION REGISTERS

The W79E4051/2051 series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W79E4051/2051 series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

F8	**IP1**							
F0	**B**						PCMPIDS	IP1H
E8	**EIE**							
E0	**ACC**							
D8	**WDCON**	PWMPL	PWM0L		PWMCON1			
D0	**PSW**	PWMPH	PWM0H					PWMCON3
C8							NVMCON	NVMDATA
C0							NVMADDRL	TA
B8	**IP0**	SADEN						
B0	**P3**			P1M1				IP0H
A8	**IE**	SADDR						
A0	**P2**		AUXR1	AUXR2				
98	**SCON**	SBUF						
90	**P1**						ACCK	ACSR
88	**TCON**	TMOD	TL0	TL1	TH0	TH1	CKCON	CLKREG
80		SP	DPL	DPH				PCON

Table 8-1: Special Function Register Location Table

Note:
1. The SFRs in the column with dark borders are bit-addressable
2. The table is condensed with eight locations per row. Empty locations indicate that these are no registers at these addresses.

Special Function Registers:

SYMBOL	DEFINITION	ADDRESS	MSB	BIT ADDRESS, SYMBOL						LSB	RESET
IP1	Interrupt priority 1	F8H	(FF) -	(FE) PBOV	(FD) PPWM	(FC) PWDI	(FB) -	(FA) -	(F9) -	(F8) -	x000 xxxxB
IP1H	Interrupt high priority 1	F7H	-	PBOVH	PPWMH	PWDIH	-	-	-	-	x000 xxxxB
PCMPIDS	Port Comparator Input Disable	F6H	-	-	-	-	-	-	B1	B0	xxxx 0000B
B	B register	F0H	(F7)	(F6)	(F5)	(F4)	(F3)	(F2)	(F1)	(F0)	00000000B
EIE	Interrupt enable 1	E8H	(EF) -	(EE) EBOV	(ED) EPWM	(EC) EWDI	(EB) -	(EA) -	(E9) -	(E8) -	xx000 xxxxB
ACC	Accumulator	E0H	(E7)	(E6)	(E5)	(E4)	(E3)	(E2)	(E1)	(E0)	00000000B
PWMCON1	PWM CONTROL REGISTER 1	DCH	PWMRUN	load	PWMF	CLRPWM	-	-	-	PWM0I	0000 0000B
PWM0L	PWM 0 LOW BITS REGISTER	DAH	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.0	0000 0000B
PWMPL	PWM COUNTER LOW REGISTER	D9H	PWMP0.7	PWMP0.6	PWMP0.5	PWMP0.4	PWMP0.3	PWMP0.2	PWMP0.1	PWMP0.0	0000 0000B
WDCON	WATCH-DOG CONTROL	D8H	(DF) WDRUN	(DE) -	(DD) WD1	(DC) WD0	(DB) WDIF	(DA) WTRF	(D9) EWRST	(D8) WDCLR	0X00 0000B
PWMCON3	PWM CONTROL REGISTER 3	D7H	-	-	-	PWM0OE	-	-	FP1	FP0	0000 XX00B
PWM0H	PWM 0 HIGH BITS REGISTER	D2H	-	-	-	-	-	-	PWM0.9	PWM0.8	XXXX XX00B
PWMPH	PWM COUNTER HIGH REGISTER	D1H	-	-	-	-	-	-	PWMP0.9	PWMP0.8	XXXX XX00B
PSW	Program Status word	D0H	(D7) CY	(D6) AC	(D5) F0	(D4) RS1	(D3) RS0	(D2) OV	(D1) F1	(D0) P	00000000B
NVMDATA	NVM Data	CFH									00000000B
NVMCON	NVM Control	CEH	EER	EWR	-	-	-	-	-		00xxxxxxB
TA	Timed Access Protection	C7H	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0	11111111B
NVMADDRL	NVM byte address	C6H	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0	00000000B
SADEN	Slave address mask	B9H									00000000B
IP0	Interrupt priority 0	B8H	(BF) -	(BE) PC	(BD) -	(BC) PS	(BB) PT1	(BA) PX1	(B9) PT0	(B8) PX0	x0x00000B
IP0H	Interrupt high priority 0	B7H	-	PCH	-	PSH	PT1H	PX1H	PT0H	PX0H	x0x00000B
P1M1	Port1 Mode 1	B3H	-	-	-	-	-	-	P1M1.1	P1M1.0	xxxx xx00B
P3	Port 3	B0H	(B7)	(B6)	(B5) T1	(B4) T0	(B3) INT1	(B2) INT0	(B1) TXD	(B0) RXD	11111111B
SADDR	Slave address	A9H									00000000B
IE	Interrupt enable	A8H	(AF) EA	(AE) EC	(AD) -	(AC) ES	(AB) ET1	(AA) EX1	(A9) ET0	(A8) EX0	00x00000B
AUXR2	AUX function register 2	A3H								DPS	xxxx xxx0B
AUXR1	AUX function register 1	A2H	BOF	BOD[2]	BOI	LPBOV	SRST	BOV1[3]	BOV0[3]	BOS	0x00 0xx0B
P2	Port 2	A0H	(A7) -	(A6) -	(A5) -	(A4) -	(A3) -	(A2) -	(A1) P2.1 XTAL1	(A0) P2.0 XTAL2 CLKOUT	xxxx xxxxB
SBUF	Serial buffer	99H									xxxxxxxxB
SCON	Serial control	98H	(9F) SM0/FE	(9E) SM1	(9D) SM2	(9C) REN	(9B) TB8	(9A) RB8	(99) TI	(98) RI	00000000B
ACSR	Analog Comparator Control & Status Register	97H	-	-	CIPE	CF	CEN	CM2	CM1	CM0	xx000000B
ACCK	Analog Comparator Debounce Clock Control	96H	ENCLK	-	-	-	-	CPCK2	CPCK1	CPCK0	0000 0000B
P1	Port 1	90H	(97)	(96)	(95)	(94)	(93)	(92)	(91)	(90)	11111111B
CLKREG		8FH						PWDEX1	PWDEX0		Xxxx x00xB
CKCON	**Clock control**	**8EH**	**-**	**-**	**-**	**T1M**	**T0M**	**-**	**-**	**-**	**xxx00xxxB**
TH1	Timer high 1	8DH									00000000B
TH0	Timer high 0	8CH									00000000B
TL1	Timer low 1	8BH									00000000B
TL0	Timer low 0	8AH									00000000B
TMOD	Timer mode	89H	GATE	C/T1#	M1	M0	GATE	C/T0#	M1	M0	00000000B
TCON	Timer control	88H	(8F) TF1	(8E) TR1	(8D) TF0	(8C) TR0	(8B) IE1	(8A) IT1	(89) IE0	(88) IT0	00000000B
PCON	Power control	87H	SMOD	SMOD0		POR	GF1	GF0	PD	IDL	00xx0000B
DPH	Data pointer high	83H									00000000B
DPL	Data pointer low	82H									00000000B
SP	Stack pointer	81H									00000111B

Table 8-2: Special Function Registers

Note :
1. In column **BIT_ADDRESS, SYMBOL**, containing ( ) item means the bit address.
2. BOD is initialized at reset with the inversed value of bit CBOD in config0-bits.
3. (BOV1,BOV0) are initialized at reset with the reversed value of config0-bits (CBOV1,CBOV0)

STACK POINTER

Bit:	7	6	5	4	3	2	1	0
	SP.7	SP.6	SP.5	SP.4	SP.3	SP.2	SP.1	SP.0

Mnemonic: SP Address: 81h

BIT	NAME	FUNCTION
7-0	SP.[7:0]	The Stack Pointer stores the Scratch-pad RAM address where the stack begins. In other words it always points to the top of the stack.

DATA POINTER LOW

Bit:	7	6	5	4	3	2	1	0
	DPL.7	DPL.6	DPL.5	DPL.4	DPL.3	DPL.2	DPL.1	DPL.0

Mnemonic: DPL Address: 82h

BIT	NAME	FUNCTION
7-0	DPL.[7:0]	This is the low byte of the standard 8052 16-bit data pointer.

DATA POINTER HIGH

Bit:	7	6	5	4	3	2	1	0
	DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer.

POWER CONTROL

Bit:	7	6	5	4	3	2	1	0
	SMOD	SMOD0	-	POR	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3.
6	SMOD0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as Frame Error (FE) status flag.
5	-	Reserved
4	POR	0: Cleared by software. 1: Set automatically when a power-on reset has occurred.
3	GF1	General purpose user flags.
2	GF0	General purpose user flags.
1	PD	1: The CPU goes into the POWER DOWN mode. In this mode, all the clocks are stopped and program execution is frozen.

0	IDL	1: The CPU goes into the IDLE mode. In this mode, the clocks CPU clock stopped, so program execution is frozen. But the clock to the serial, timer and interrupt blocks is not stopped, and these blocks continue operating.

TIMER CONTROL

Bit:	7	6	5	4	3	2	1	0
	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0

Mnemonic: TCON Address: 88h

BIT	NAME	FUNCTION
7	TF1	Timer 1 Overflow Flag. This bit is set when Timer 1 overflows. It is cleared automatically when the program does a timer 1 interrupt service routine. Software can also set or clear this bit.
6	TR1	Timer 1 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
5	TF0	Timer 0 Overflow Flag. This bit is set when Timer 0 overflows. It is cleared automatically when the program does a timer 0 interrupt service routine. Software can also set or clear this bit.
4	TR0	Timer 0 Run Control. This bit is set or cleared by software to turn timer/counter on or off.
3	IE1	Interrupt 1 Edge Detect Flag: Set by hardware when an edge/level is detected on $\overline{INT1}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
2	IT1	Interrupt 1 Type Control. Set/cleared by software to specify falling edge/ low level triggered external inputs.
1	IE0	Interrupt 0 Edge Detect Flag. Set by hardware when an edge/level is detected on $\overline{INT0}$. This bit is cleared by hardware when the service routine is vectored to only if the interrupt was edge triggered. Otherwise it follows the inverse of the pin.
0	IT0	Interrupt 0 Type Control: Set/cleared by software to specify falling edge/ low level triggered external inputs.

TIMER MODE CONTROL

Bit:	7	6	5	4	3	2	1	0
	GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
	TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.

4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

TIMER 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

TIMER 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

TIMER 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

TIMER 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	-	-	-	T1M	T0M	-	-	-

Mnemonic: CKCON Address: 8Eh

BIT	NAME	FUNCTION
7-5	-	Reserved.
4	T1M	Timer 1 clock select: 0: Timer 1 uses a divide by 12 clocks. 1: Timer 1 uses a divide by 6 clocks.
3	T0M	Timer 0 clock select: 0: Timer 0 uses a divide by 12 clocks. 1: Timer 0 uses a divide by 6 clocks.
2-0	-	Reserved.

CLOCK REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	PWDEX1	PWDEX0	-

Mnemonic: CLDREG Address: 8Fh

BIT	NAME	FUNCTION
7-5	-	Reserved.
2	PWDEX1	Power Down Exit Mode.
1	PWDEX0	Power Down Exit Mode.
0	-	Reserved.

Power Down Exit Mode:

PWDEX1	PWDEX0	Power Down Exit Mode
0	0	Wake up from Power Down is internally timed. $\overline{INT0}$ or $\overline{INT1}$ must be configured for low-level trigger mode.
0	1	Wake up from Power Down is externally controlled. $\overline{INT0}$ or $\overline{INT1}$ must be configured for low-level trigger mode.
1	x	Wake up from Power Down immediately. $\overline{INT0}$ or $\overline{INT1}$ can be configured for low-level or edge trigger mode.

PORT 1

Bit:	7	6	5	4	3	2	1	0
	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

Mnemonic: P1 Address: 90h

P1.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
1	P1.1	AN1+
0	P1.0	AN0-

ANALOG COMPARATOR DEBOUNCE CLOCK CONTROL

Bit:	7	6	5	4	3	2	1	0
	ENCLK	-	-	-	-	CPCK2	CPCK1	CPCK0

Mnemonic: ACCK Address: 96h

BIT	NAME	FUNCTION
7	ENCLK	1: Enable clock output to the XTAL2 pin (P2.0) when CPU clock is from the external OSC or on-chip RC oscillator. The frequency of the clock output is 1/4 of the CPU clock rate.
6-3	-	Reserved.
2	CPCK2	See as below table.
1	CPCK1	See as below table.
0	CPCK0	See as below table.

Comparator Debouncing Time Setting:

CPCK2	CPCK 1	CPCK 0	Debouncing Time
0	0	0	$(3/F_{DB})*2$~$(4/F_{DB})*2$
0	0	1	$(3/F_{DB})*4$~$(4/F_{DB})*4$
0	1	0	$(3/F_{DB})*8$~$(4/F_{DB})*8$
0	1	1	$(3/F_{DB})*16$~$(4/F_{DB})*16$
1	0	0	$(3/F_{DB})*32$~$(4/F_{DB})*32$
1	0	1	$(3/F_{DB})*64$~$(4/F_{DB})*64$
1	1	0	$(3/F_{DB})*128$~$(4/F_{DB})*128$

ANALOG COMPARATOR CONTROL & STATUS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	CIPE	CF	CEN	CM2	CM1	CM0

Mnemonic: ACSR Address: 97h

BIT	NAME	FUNCTION
7-6	-	Reserved.
5	CIPE	Comparator Enabled in Idle and Power down Mode. 0: Comparator disabled in idle and power down mode. (default) 1: Comparator enabled in idle and power down mode.
4	CF	Comparator Interrupt Flag. Set by hardware when the comparator output meet the conditions specified by the CM[2:0] bits and CEN is set. The flag must be cleared by software. The interrupt may be enabled/disabled by setting/clearing bit 6 of IE.
3	CEN	Enable Comparator. Set this bit to enable the comparator. Clearing this bit will force the comparator output low and prevent further events from setting CF.
2	CM2	See as below table.
1	CM1	See as below table.
0	CM0	See as below table.

Comparator Interrupt Mode Setting:

CM2	CM1	CM0	Interrupt Mode
0	0	0	Negative (Low) level
0	0	1	Positive edge
0	1	0	Toggle with debounce
0	1	1	Positive edge with debounce
1	0	0	Negative edge
1	0	1	Toggle
1	1	0	Negative edge with debounce
1	1	1	Positive (High) level

SERIAL PORT CONTROL

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiple processors communication. Setting this bit to 1 enables the multiprocessor communication feature in mode 2 and 3. In mode 2 or 3, if SM2 is set to 1, then RI will not be activated if the received 9th data bit (RB8) is 0. In mode 1, if SM2 = 1, then RI will not be activated if a valid stop bit was not received. In mode 0, the SM2 bit controls the serial port clock. If set to 0, then the serial port runs at a divide by 12 clock of the oscillator. This gives compatibility with the standard 8052. When set to 1, the serial clock become

		divide by 4 of the oscillator clock. This results in faster synchronous serial communication.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

SERIAL DATA BUFFER

Bit:	7	6	5	4	3	2	1	0
	SBUF.7	SBUF.6	SBUF.5	SBUF.4	SBUF.3	SBUF.2	SBUF.1	SBUF.0

Mnemonic: SBUF Address: 99h

BIT	NAME	FUNCTION
7~0	SBUF	Serial data on the serial port is read from or written to this location. It actually consists of two separate internal 8-bit registers. One is the receive resister, and the other is the transmit buffer. Any read access gets data from the receive data buffer, while write access is to the transmit data buffer.

PORT 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P2.1	P2.0

Mnemonic: P2 Address: A0h

BIT	NAME	ALTERNATE FUNCTION
7-2	-	Reserved
1	P2.1	XTAL1 clock input pin.
0	P2.0	XTAL2 or CLKOUT pin by alternative.

AUX FUNCTION REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	BOF	BOD	BOI	LPBOV	SRST	BOV1	BOV0	BOS

Mnemonic: AUXR1 Address: A2h

BIT	NAME	FUNCTION
7	BOF	Brown Out Flag 0: Cleared by software. 1: Set automatically when a brownout reset or interrupt has occurred. Also set at power on.
6	BOD	Brown Out Disable: BOD is initialized at reset with the inversed value of bit CBOD in config0-bits. 0: Enable Brownout Detect function. 1: Disable Brownout Detect function and save power.
5	BOI	Brown Out Interrupt: 0: Disable Brownout Detect Interrupt function and it will cause chip reset when BOF is set. 1: This prevents Brownout Detection from causing a chip reset and allows the Brownout Detect function to be used as an interrupt.
4	LPBOV	Low Power Brown Out Detect control: 0: If bit BOD=0, the Brown Out detection is always active. 1: If bit BOD=0, the Brown Out detection repeats to senses the voltage for $64/f_{BRC}$ then turn off detector for $960/f_{BRC}$, therefore, it saves 15/16 of the Brownout circuit power.
3	SRST	Software reset: This bit has TA(Time Accessed) protection in write access. 1: reset the chip as if a hardware reset occurred.
2~1	BOV1, BOV0	Brownout voltage selection bits: (BOV1,BOV0) are initialized at reset with the reversed value of bits (CBOV1,CBOV0) in config0-bits
0	BOS	Brownout Status bit(Read only) 0: V_{DD} is above V_{BOR+} 1: V_{DD} is below V_{BOR-}

BOV.1	BOV.0	Brownout Voltage
0	0	Brownout voltage is 2.4V
0	1	Brownout voltage is 2.7V
1	0	Brownout voltage is 3.8V
1	1	Brownout voltage is 4.5V

Brownout Voltage Selection

BOV1	BOV0	Brownout Voltage
0	0	Brownout voltage is 2.4V
0	1	Brownout voltage is 2.7V
1	0	Brownout voltage is 3.8V

1	1	Brownout voltage is 4.5V

All the bits in this SFR have unrestricted read access. **SRST** require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

AUX FUNCTION REGISTER 2

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	DPS

Mnemonic: AUXR2 Address: A3h

BIT	NAME	FUNCTION
7-1	-	Reserved
0	DPS	Dual Data Pointer Select 0: To select DPTR of standard 8051. 1: To select DPTR1

INTERRUPT ENABLE

Bit:	7	6	5	4	3	2	1	0
	EA	EC	-	ES	ET1	EX1	ET0	EX0

Mnemonic: IE Address: A8h

BIT	NAME	FUNCTION
7	EA	Global enable. Enable/Disable all interrupts.
6	EC	Enable analog comparator interrupt.
5	-	Reserved.
4	ES	Enable Serial Port 0 interrupt.
3	ET1	Enable Timer 1 interrupt.
2	EX1	Enable external interrupt 1.
1	ET0	Enable Timer 0 interrupt.
0	EX0	Enable external interrupt 0.

SLAVE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	SADDR.7	SADDR.6	SADDR.5	SADDR.4	SADDR.3	SADDR.2	SADDR.1	SADDR.0

Mnemonic: SADDR Address: A9h

BIT	NAME	FUNCTION
7~0	SADDR	The SADDR should be programmed to the given or broadcast address for serial port to which the slave processor is designated.

PORT 3

Bit:	7	6	5	4	3	2	1	0

P3.7	CMP_O	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P3.7	-
6	CMP_O	Read only. This bit stores the hardware comparator result.
5	P3.5	T1 or PWM output
4	P3.4	T0
3	P3.3	$\overline{INT1}$
2	P3.2	$\overline{INT0}$
1	P3.1	TX
0	P3.0	RX

Port1 Output Mode 1

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	P1M1.1	P1M1.0

Mnemonic: P1M1 Address: B3h

BIT	NAME	FUNCTION
7-2	Reserved	
1	P1M1.1	0: P1.1 is in open drain mode. (Default) 1: P1.1 is in Quasi-bidirection mode
0	P1M1.0	0: P1.0 is in open drain mode. (Default) 1: P1.0 is in Quasi-bidirection mode

Interrupt High Priority 0

Bit:	7	6	5	4	3	2	1	0
	-	PCH	-	PSH	PT1H	PX1H	PT0H	PX0H

Mnemonic: IP0H Address: B7h

BIT	NAME	FUNCTION
7	-	Reserved
6	PCH	1: To set interrupt high priority of analog comparator is highest priority level.
5	-	Reserved.
4	PSH	1: To set interrupt high priority of Serial port 0 is highest priority level.
3	PT1H	1: To set interrupt high priority of Timer 1 is highest priority level.
2	PX1H	1: To set interrupt high priority of External interrupt 1 is highest priority level.
1	PT0H	1: To set interrupt high priority of Timer 0 is highest priority level.
0	PX0H	1: To set interrupt high priority of External interrupt 0 is highest priority level.

Interrupt Priority 0

Bit:	7	6	5	4	3	2	1	0
	-	PC	-	PS	PT1	PX1	PT0	PX0

Mnemonic: IP0 Address: B8h

BIT	NAME	FUNCTION
7	-	This bit is un-implemented and will read high.
6	PC	1: To set interrupt priority of analog comparator is higher priority level.
5	-	This bit is un-implemented and will read high.
4	PS	1: To set interrupt priority of Serial port 0 is higher priority level.
3	PT1	1: To set interrupt priority of Timer 1 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

SLAVE ADDRESS MASK ENABLE

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	-

Mnemonic: SADEN Address: B9h

BIT	NAME	FUNCTION
7~0	SADEN	This register enables the Automatic Address Recognition feature of the Serial port 0. When a bit in the SADEN is set to 1, the same bit location in SADDR will be compared with the incoming serial data. When SADEN is 0, then the bit becomes a "don't care" in the comparison. This register enables the Automatic Address Recognition feature of the Serial port 0. When all the bits of SADEN are 0, interrupt will occur for any incoming address.

NVM BYTE ADDRESS

Bit:	7	6	5	4	3	2	1	0
	NVMADDR.7	NVMADDR.6	NVMADDR.5	NVMADDR.4	NVMADDR.3	NVMADDR.2	NVMADDR.1	NVMADDR.0

Mnemonic: NVMADDRL Address: C6h

BIT	NAME	FUNCTION
7	NVMADDR.7	Must be 0.
6~0	NVMADDR.[6:0]	The NVM low byte address: The register indicates NVM data memory address on On-Chip code memory space.

TIMED ACCESS

Bit:	7	6	5	4	3	2	1	0
	TA.7	TA.6	TA.5	TA.4	TA.3	TA.2	TA.1	TA.0

Mnemonic: TA Address: C7h

BIT	NAME	FUNCTION
7-0	TA.[7:0]	The Timed Access register: The Timed Access register controls the access to protected bits. To access protected bits, the user must first write AAH to the TA. This must be immediately followed by a write of 55H to TA. Now a window is opened in the protected bits for three machine cycles, during which the user can write to these bits.

NVM CONTROL

Bit:	7	6	5	4	3	2	1	0
	EER	EWR	-	-	-	-	-	-

Mnemonic: NVMCON Address: CEh

BIT	NAME	FUNCTION
7	EER	NVM page(n) erase bit: 0: Without erase NVM page(n). 1: Set this bit to erase page(n) of NVM. The NVM has 8 pages and each page have 16 bytes data memory. Initiate page select by programming NVMADDRL registers, which will automaticly enable page area. When user set this bit, the page erase process will begin and program counter will halt at this instruction. After the erase process is completed, program counter will continue executing next instruction.
6	EWR	NVM data write bit: 0: Without write NVM data. 1: Set this bit to write NVM bytes and program counter will halt at this instruction. After write is finished, program counter will kept next instruction then executed.
5-0	-	Reserved.

NVM DATA

Bit:	7	6	5	4	3	2	1	0
	NVMDATA.7	NVMDATA.6	NVMDATA.5	NVMDATA.4	NVMDATA3	NVMDATA.2	NVMDATA.1	NVMDATA.0

Mnemonic: NVMDATA Address: CFh

BIT	NAME	FUNCTION
7~0	NVMDATA[7:0]	The NVM data write register. The read NVM data is by MOVC instruction.

PROGRAM STATUS WORD

Bit:	7	6	5	4	3	2	1	0
	CY	AC	F0	RS1	RS0	OV	F1	P

Mnemonic: PSW Address: D0h

BIT	NAME	FUNCTION
7	CY	Carry flag: Set for an arithmetic operation which results in a carry being generated from the ALU. It is also used as the accumulator for the bit operations.
6	AC	Auxiliary carry: Set when the previous operation resulted in a carry from the high order nibble.
5	F0	User flag 0: The General purpose flag that can be set or cleared by the user.
4	RS1	Register bank select bits:
3	RS0	Register bank select bits:
2	OV	Overflow flag: Set when a carry was generated from the seventh bit but not from the 8th bit as a result of the previous operation, or vice-versa.
1	F1	User Flag 1: The General purpose flag that can be set or cleared by the user by software.
0	P	Parity flag: Set/cleared by hardware to indicate odd/even number of 1's in the accumulator.

RS.1-0: Register bank selection bits:

RS1	RS0	Register bank	Address
0	0	0	00-07h
0	1	1	08-0Fh
1	0	2	10-17h
1	1	3	18-1Fh

PWM COUNTER HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWMP.9	PWMP.8

Mnemonic: PWMPH Address: D1h

BIT	NAME	FUNCTION
7-2	-	Reserved.
1-0	PWMP.[9:8]	The PWM Counter Register bits 9~8.

PWM 0 HIGH BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	PWM0.9	PWM0.8

Mnemonic: PWM0H Address: D2h

BIT	NAME	FUNCTION

7~2	-	Reserved.
1~0	PWM0.9~8	The PWM 0 Register bit 9~8.

PWM CONTROL REGISTER 3

Bit:	7	6	5	4	3	2	1	0
	-	-	-	PWM0OE	-	-	FP1	FP0

Mnemonic: PWMCON3 Address: D7h

Bit	Name	Function
7		
6		
5		
4	PWM0OE	PWM0 output enable bit. 0: PWM0 output disabled. 1: PWM0 output enabled. If P3.5 is set to high PWM0 will output through P3.5.
3~2	-	Reserved.
1~0	FP1~0	Select PWM frequency pre-scale select bits. The clock source of pre-scaler is in phase with Fosc if PWMRUN=1, otherwise it is disabled.

FP1~0: PWM Prescaler select bits:

FP[1:0]	Fpwm
00	FOSC
01	FOSC/2
10	FOSC/4
11	FOSC/16

WATCHDOG CONTROL

Bit:	7	6	5	4	3	2	1	0
	WDRUN	-	WD1	WD0	WDIF	WTRF	EWRST	WDCLR

Mnemonic: WDCON Address: D8h

BIT	NAME	FUNCTION
7	WDRUN	0: The Watchdog is stopped. 1: The Watchdog is running.
6	-	Reserved.

<table>
<tr><td>5~4</td><td>WD1~WD0</td><td>Watchdog Timer Time-out Select bits. These bits determine the time-out period of the watchdog timer. The reset time-out period is 512 clocks longer than the watchdog time-out.
<table>
<tr><th>WD1</th><th>WD0</th><th>Interrupt time-out</th><th>Reset time-out</th></tr>
<tr><td>0</td><td>0</td><td>2^{17}</td><td>2^{17} + 512</td></tr>
<tr><td>0</td><td>1</td><td>2^{20}</td><td>2^{20} + 512</td></tr>
<tr><td>1</td><td>0</td><td>2^{23}</td><td>2^{23} + 512</td></tr>
<tr><td>1</td><td>1</td><td>2^{26}</td><td>2^{26} + 512</td></tr>
</table></td></tr>
<tr><td>3</td><td>WDIF</td><td>Watchdog Timer Interrupt flag:
0: If the interrupt is not enabled, then this bit indicates that the time-out period has elapsed. This bit must be cleared by software.
1: If the watchdog interrupt is enabled, hardware will set this bit to indicate that the watchdog interrupt has occurred.</td></tr>
<tr><td>2</td><td>WTRF</td><td>Watchdog Timer Reset flag:
1: Hardware will set this bit when the watchdog timer causes a reset. Software can read it but must clear it manually. A power-fail reset will also clear the bit. This bit helps software in determining the cause of a reset. If EWRST = 0, the watchdog timer will have no affect on this bit.</td></tr>
<tr><td>1</td><td>EWRST</td><td>0: Disable Watchdog Timer Reset.
1: Enable Watchdog Timer Reset.</td></tr>
<tr><td>0</td><td>WDCLR</td><td>Reset Watchdog Timer:
This bit helps in putting the watchdog timer into a know state. It also helps in resetting the watchdog timer before a time-out occurs. Failing to set the EWRST before time-out will cause an interrupt (if EWDI (EIE.4) is set), and 512 clocks after that a watchdog timer reset will be generated (if EWRST is set). This bit is self-clearing by hardware.</td></tr>
</table>

The WDCON SFR is set to a 0x000000B on a power-on-reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by an external reset. EWRST (WDCON.1) is set to 0 on all resets.

All the bits in this SFR have unrestricted read access. WDRUN, EWRST, WDIF and WDCLR require Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

```
TA      REG     C7H
WDCON   REG     D8H
MOV     TA, #AAH                ; To access protected bits
MOV     TA, #55H
SETB    WDCON.0                 ; Reset watchdog timer
ORL     WDCON, #00110000B       ; Select 26 bits watchdog timer
MOV     TA, #AAH
MOV     TA, #55H
ORL     WDCON, #00000010B       ; Enable watchdog
```

PWM COUNTER LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWMP.7	PWMP.6	PWMP.5	PWP.4	PWMP.3	PWMP.2	PWMP.1	PWMP.1

Mnemonic: PWMPL Address: D9h

Bit	Name	Function
7~0	PWMP	PWM Counter Low Bits Register.

PWM 0 LOW BITS REGISTER

Bit:	7	6	5	4	3	2	1	0
	PWM0.7	PWM0.6	PWM0.5	PWM0.4	PWM0.3	PWM0.2	PWM0.1	PWM0.1

Mnemonic: PWM0L Address: DAh

Bit	Name	Function
7~0	PWM0	PWM 0 Low Bits Register.

PWM CONTROL REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	PWMRUN	Load	PWMF	CLRPWM	-	-	-	PWM0I

Mnemonic: PWMCON1 Address: DCh

Bit	Name	Function
7	PWMRUN	Enable PWM running bit 0: The PWM is not running. 1: The PWM counter is running.
6	Load	Enable PWM counter and register re-load 0: The registers value of PWMP and Comparators are never loaded to counter and Comparator registers. 1: The PWMP register will be load value to counter register after counter underflow and hardware will clear by next clock cycle.
5	PWMF	PWM underflow flag. 0: No underflow. 1: PWM 10-bit down counter underflows (PWM interrupt is requested if PWM interrupt is enabled).
4	CLRPWM	Clear PWM counter 1: Clear 10-bit PWM counter to 000H. It is automatically cleared by hardware.
3~1	-	Reserved
0	PWM0I	Inverse PWM output level 0: PWM0 output is non-inverted. 1: PWM0 output is inverted.

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0
	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

Bit	Name	Function
7-0	ACC	The A or ACC register is the standard 8052 accumulator.

INTERRUPT ENABLE REGISTER 1

Bit:	7	6	5	4	3	2	1	0
	-	EBOV	EPWM	EWDI	-	-	-	-

Mnemonic: EIE Address: E8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	EBOV	0: Disable Brownout interrupt. 1: Enable Brownout interrupt.
5	EPWM	0: Disable PWM underflow interrupt. 1: Enable PWM underflow interrupt.
4	EWDI	0: Disable Watchdog Timer Interrupt. 1: Enable Watchdog Timer Interrupt.
3-0	-	Reserved.

B REGISTER

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

Bit	Name	Function
7-0	B	The B register is the standard 8052 register that serves as a second accumulator.

PORT COMPARATOR INPUT DISABLE

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	Bit1	Bit0

Mnemonic: PCMPIDS Address: F6h

Bit	Name	Function
7-2	-	Reserved
1	PCMPIDS.1	P1.1 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of Comparator Input 1(Negative end)

0	PCMPIDS.0	P1.0 digital input disable bit. 0: Default (With digital/analog input). 1: Disable Digital Input of Comparator Input 1(Positive end)

INTERRUPT HIGH PRIORITY 1

Bit:	7	6	5	4	3	2	1	0
	-	PBOVH	PPWMH	PWDIH	-	-	-	-

Mnemonic: IP1H Address: F7h

BIT	NAME	FUNCTION
7	-	Reserved.
6	PBOVH	1: To set interrupt priority of Brownout interrupt is highest priority level.
5	PPWMH	1: To set interrupt priority of PWM underflow is highest priority level.
4	PWDIH	1: To set interrupt high priority of Watchdog is highest priority level.
3-0	-	Reserved.

EXTENDED INTERRUPT PRIORITY

Bit:	7	6	5	4	3	2	1	0
	-	PBOV	PPWM	PWDI	-	-	-	-

Mnemonic: IP1 Address: F8h

BIT	NAME	FUNCTION
7	-	Reserved.
6	PBOV	1: To set interrupt priority of Brownout interrupt is higher priority level.
5	PPWM	1: To set interrupt priority of PWM underflow is higher priority level.
4	PWDI	1: To set interrupt priority of Watchdog is higher priority level.
3-0	-	Reserved.

9 INSTRUCTION

The W79E4051/2051 series execute all the instructions of the standard 8052 family. The operations of these instructions, as well as their effects on flag and status bits, are exactly same. However, the timing of these instructions is different in two ways. Firstly, the machine cycle is four clock periods, while the standard-8051/52 machine cycle is twelve clock periods. Secondly, it can fetch only once per machine cycle (i.e., four clocks per fetch), while the standard 8051/52 can fetch twice per machine cycle (i.e., six clocks per fetch).

The timing differences create an advantage for the W79E4051/2051 series. There is only one fetch per machine cycle, so the number of machine cycles is usually equal to the number of operands in the instruction. (Jumps and calls do require an additional cycle to calculate the new address.) As a result, the W79E4051/2051 series reduces the number of dummy fetches and wasted cycles, and therefore improves overall efficiency, compared to the standard 8051/52.

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/205 1 series vs. 8032 Speed Ratio
NOP	00	1	1	4	12	3
ADD A, R0	28	1	1	4	12	3
ADD A, R1	29	1	1	4	12	3
ADD A, R2	2A	1	1	4	12	3
ADD A, R3	2B	1	1	4	12	3
ADD A, R4	2C	1	1	4	12	3
ADD A, R5	2D	1	1	4	12	3
ADD A, R6	2E	1	1	4	12	3
ADD A, R7	2F	1	1	4	12	3
ADD A, @R0	26	1	1	4	12	3
ADD A, @R1	27	1	1	4	12	3
ADD A, direct	25	2	2	8	12	1.5
ADD A, #data	24	2	2	8	12	1.5
ADDC A, R0	38	1	1	4	12	3
ADDC A, R1	39	1	1	4	12	3
ADDC A, R2	3A	1	1	4	12	3
ADDC A, R3	3B	1	1	4	12	3
ADDC A, R4	3C	1	1	4	12	3
ADDC A, R5	3D	1	1	4	12	3
ADDC A, R6	3E	1	1	4	12	3
ADDC A, R7	3F	1	1	4	12	3
ADDC A, @R0	36	1	1	4	12	3

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
ADDC A, @R1	37	1	1	4	12	3
ADDC A, direct	35	2	2	8	12	1.5
ADDC A, #data	34	2	2	8	12	1.5
SUBB A, R0	98	1	1	4	12	3
SUBB A, R1	99	1	1	4	12	3
SUBB A, R2	9A	1	1	4	12	3
SUBB A, R3	9B	1	1	4	12	3
SUBB A, R4	9C	1	1	4	12	3
SUBB A, R5	9D	1	1	4	12	3
SUBB A, R6	9E	1	1	4	12	3
SUBB A, R7	9F	1	1	4	12	3
SUBB A, @R0	96	1	1	4	12	3
SUBB A, @R1	97	1	1	4	12	3
SUBB A, direct	95	2	2	8	12	1.5
SUBB A, #data	94	2	2	8	12	1.5
INC A	04	1	1	4	12	3
INC R0	08	1	1	4	12	3
INC R1	09	1	1	4	12	3
INC R2	0A	1	1	4	12	3
INC R3	0B	1	1	4	12	3
INC R4	0C	1	1	4	12	3
INC R5	0D	1	1	4	12	3
INC R6	0E	1	1	4	12	3
INC R7	0F	1	1	4	12	3
INC @R0	06	1	1	4	12	3
INC @R1	07	1	1	4	12	3
INC direct	05	2	2	8	12	1.5
INC DPTR	A3	1	2	8	24	3
DEC A	14	1	1	4	12	3
DEC R0	18	1	1	4	12	3
DEC R1	19	1	1	4	12	3
DEC R2	1A	1	1	4	12	3
DEC R3	1B	1	1	4	12	3
DEC R4	1C	1	1	4	12	3

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
DEC R5	1D	1	1	4	12	3
DEC R6	1E	1	1	4	12	3
DEC R7	1F	1	1	4	12	3
DEC @R0	16	1	1	4	12	3
DEC @R1	17	1	1	4	12	3
DEC direct	15	2	2	8	12	1.5
MUL AB	A4	1	5	20	48	2.4
DIV AB	84	1	5	20	48	2.4
DA A	D4	1	1	4	12	3
ANL A, R0	58	1	1	4	12	3
ANL A, R1	59	1	1	4	12	3
ANL A, R2	5A	1	1	4	12	3
ANL A, R3	5B	1	1	4	12	3
ANL A, R4	5C	1	1	4	12	3
ANL A, R5	5D	1	1	4	12	3
ANL A, R6	5E	1	1	4	12	3
ANL A, R7	5F	1	1	4	12	3
ANL A, @R0	56	1	1	4	12	3
ANL A, @R1	57	1	1	4	12	3
ANL A, direct	55	2	2	8	12	1.5
ANL A, #data	54	2	2	8	12	1.5
ANL direct, A	52	2	2	8	12	1.5
ANL direct, #data	53	3	3	12	24	2
ORL A, R0	48	1	1	4	12	3
ORL A, R1	49	1	1	4	12	3
ORL A, R2	4A	1	1	4	12	3
ORL A, R3	4B	1	1	4	12	3
ORL A, R4	4C	1	1	4	12	3
ORL A, R5	4D	1	1	4	12	3
ORL A, R6	4E	1	1	4	12	3
ORL A, R7	4F	1	1	4	12	3
ORL A, @R0	46	1	1	4	12	3
ORL A, @R1	47	1	1	4	12	3

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
ORL A, direct	45	2	2	8	12	1.5
ORL A, #data	44	2	2	8	12	1.5
ORL direct, A	42	2	2	8	12	1.5
ORL direct, #data	43	3	3	12	24	2
XRL A, R0	68	1	1	4	12	3
XRL A, R1	69	1	1	4	12	3
XRL A, R2	6A	1	1	4	12	3
XRL A, R3	6B	1	1	4	12	3
XRL A, R4	6C	1	1	4	12	3
XRL A, R5	6D	1	1	4	12	3
XRL A, R6	6E	1	1	4	12	3
XRL A, R7	6F	1	1	4	12	3
XRL A, @R0	66	1	1	4	12	3
XRL A, @R1	67	1	1	4	12	3
XRL A, direct	65	2	2	8	12	1.5
XRL A, #data	64	2	2	8	12	1.5
XRL direct, A	62	2	2	8	12	1.5
XRL direct, #data	63	3	3	12	24	2
CLR A	E4	1	1	4	12	3
CPL A	F4	1	1	4	12	3
RL A	23	1	1	4	12	3
RLC A	33	1	1	4	12	3
RR A	03	1	1	4	12	3
RRC A	13	1	1	4	12	3
SWAP A	C4	1	1	4	12	3
MOV A, R0	E8	1	1	4	12	3
MOV A, R1	E9	1	1	4	12	3
MOV A, R2	EA	1	1	4	12	3
MOV A, R3	EB	1	1	4	12	3
MOV A, R4	EC	1	1	4	12	3
MOV A, R5	ED	1	1	4	12	3
MOV A, R6	EE	1	1	4	12	3
MOV A, R7	EF	1	1	4	12	3
MOV A, @R0	E6	1	1	4	12	3

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
MOV A, @R1	E7	1	1	4	12	3
MOV A, direct	E5	2	2	8	12	1.5
MOV A, #data	74	2	2	8	12	1.5
MOV R0, A	F8	1	1	4	12	3
MOV R1, A	F9	1	1	4	12	3
MOV R2, A	FA	1	1	4	12	3
MOV R3, A	FB	1	1	4	12	3
MOV R4, A	FC	1	1	4	12	3
MOV R5, A	FD	1	1	4	12	3
MOV R6, A	FE	1	1	4	12	3
MOV R7, A	FF	1	1	4	12	3
MOV R0, direct	A8	2	2	8	12	1.5
MOV R1, direct	A9	2	2	8	12	1.5
MOV R2, direct	AA	2	2	8	12	1.5
MOV R3, direct	AB	2	2	8	12	1.5
MOV R4, direct	AC	2	2	8	12	1.5
MOV R5, direct	AD	2	2	8	12	1.5
MOV R6, direct	AE	2	2	8	12	1.5
MOV R7, direct	AF	2	2	8	12	1.5
MOV R0, #data	78	2	2	8	12	1.5
MOV R1, #data	79	2	2	8	12	1.5
MOV R2, #data	7A	2	2	8	12	1.5
MOV R3, #data	7B	2	2	8	12	1.5
MOV R4, #data	7C	2	2	8	12	1.5
MOV R5, #data	7D	2	2	8	12	1.5
MOV R6, #data	7E	2	2	8	12	1.5
MOV R7, #data	7F	2	2	8	12	1.5
MOV @R0, A	F6	1	1	4	12	3
MOV @R1, A	F7	1	1	4	12	3
MOV @R0, direct	A6	2	2	8	12	1.5
MOV @R1, direct	A7	2	2	8	12	1.5
MOV @R0, #data	76	2	2	8	12	1.5
MOV @R1, #data	77	2	2	8	12	1.5

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
MOV direct, A	F5	2	2	8	12	1.5
MOV direct, R0	88	2	2	8	12	1.5
MOV direct, R1	89	2	2	8	12	1.5
MOV direct, R2	8A	2	2	8	12	1.5
MOV direct, R3	8B	2	2	8	12	1.5
MOV direct, R4	8C	2	2	8	12	1.5
MOV direct, R5	8D	2	2	8	12	1.5
MOV direct, R6	8E	2	2	8	12	1.5
MOV direct, R7	8F	2	2	8	12	1.5
MOV direct, @R0	86	2	2	8	12	1.5
MOV direct, @R1	87	2	2	8	12	1.5
MOV direct, direct	85	3	3	12	24	2
MOV direct, #data	75	3	3	12	24	2
MOV DPTR, #data 16	90	3	3	12	24	2
MOVC A, @A+DPTR	93	1	2	8	24	3
MOVC A, @A+PC	83	1	2	8	24	3
MOVX A, @R0	E2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @R1	E3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX A, @DPTR	E0	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R0, A	F2	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @R1, A	F3	1	2 - 9	8 - 36	24	3 - 0.66
MOVX @DPTR, A	F0	1	2 - 9	8 - 36	24	3 - 0.66
PUSH direct	C0	2	2	8	24	3
POP direct	D0	2	2	8	24	3
XCH A, R0	C8	1	1	4	12	3
XCH A, R1	C9	1	1	4	12	3
XCH A, R2	CA	1	1	4	12	3
XCH A, R3	CB	1	1	4	12	3
XCH A, R4	CC	1	1	4	12	3
XCH A, R5	CD	1	1	4	12	3
XCH A, R6	CE	1	1	4	12	3
XCH A, R7	CF	1	1	4	12	3
XCH A, @R0	C6	1	1	4	12	3
XCH A, @R1	C7	1	1	4	12	3

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
XCHD A, @R0	D6	1	1	4	12	3
XCHD A, @R1	D7	1	1	4	12	3
XCH A, direct	C5	2	2	8	12	1.5
CLR C	C3	1	1	4	12	3
CLR bit	C2	2	2	8	12	1.5
SETB C	D3	1	1	4	12	3
SETB bit	D2	2	2	8	12	1.5
CPL C	B3	1	1	4	12	3
CPL bit	B2	2	2	8	12	1.5
ANL C, bit	82	2	2	8	24	3
ANL C, /bit	B0	2	2	6	24	3
ORL C, bit	72	2	2	8	24	3
ORL C, /bit	A0	2	2	6	24	3
MOV C, bit	A2	2	2	8	12	1.5
MOV bit, C	92	2	2	8	24	3
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	3	12	24	2
LCALL addr16	12	3	4	16	24	1.5
RET	22	1	2	8	24	3
RETI	32	1	2	8	24	3
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	3	12	24	2
LJMP addr16	02	3	4	16	24	1.5
JMP @A+DPTR	73	1	2	6	24	3
SJMP rel	80	2	3	12	24	2
JZ rel	60	2	3	12	24	2
JNZ rel	70	2	3	12	24	2
JC rel	40	2	3	12	24	2
JNC rel	50	2	3	12	24	2
JB bit, rel	20	3	4	16	24	1.5
JNB bit, rel	30	3	4	16	24	1.5
JBC bit, rel	10	3	4	16	24	1.5

Op-code	HEX Code	Bytes	W79E4051 /2051 series Machine Cycle	W79E4051 /2051 series Clock cycles	8032 Clock cycles	W79E4051/2051 series vs. 8032 Speed Ratio
CJNE A, direct, rel	B5	3	4	16	24	1.5
CJNE A, #data, rel	B4	3	4	16	24	1.5
CJNE @R0, #data, rel	B6	3	4	16	24	1.5
CJNE @R1, #data, rel	B7	3	4	16	24	1.5
CJNE R0, #data, rel	B8	3	4	16	24	1.5
CJNE R1, #data, rel	B9	3	4	16	24	1.5
CJNE R2, #data, rel	BA	3	4	16	24	1.5
CJNE R3, #data, rel	BB	3	4	16	24	1.5
CJNE R4, #data, rel	BC	3	4	16	24	1.5
CJNE R5, #data, rel	BD	3	4	16	24	1.5
CJNE R6, #data, rel	BE	3	4	16	24	1.5
CJNE R7, #data, rel	BF	3	4	16	24	1.5
DJNZ R0, rel	D8	2	3	12	24	2
DJNZ R1, rel	D9	2	3	12	24	2
DJNZ R5, rel	DD	2	3	12	24	2
DJNZ R2, rel	DA	2	3	12	24	2
DJNZ R3, rel	DB	2	3	12	24	2
DJNZ R4, rel	DC	2	3	12	24	2
DJNZ R6, rel	DE	2	3	12	24	2
DJNZ R7, rel	DF	2	3	12	24	2
DJNZ direct, rel	D5	3	4	16	24	1.5

Table 9-1: Instruction Set for W79E4051/2051

9.1 Instruction Timing

In W79E4051/2051 series, each machine cycle is four clock periods long. Each clock period is called a state, and each machine cycle consists of four states: C1, C2 C3 and C4, in order. Both clock edges are used for internal timing, so the duty cycle of the clock should be as close to 50% as possible to avoid timing conflicts.

The W79E4051/2051 series does one op-code fetch per machine cycle, so, in most instructions, the number of machine cycles required is equal to the number of bytes in the instruction. There are 256 available op-codes. 128 of them are single-cycle instructions, so many op-codes are executed in just four clocks period. Some of the other op-codes are two-cycle instructions, and most of these have two-byte op-codes. However, there are some instructions that have one-byte instructions yet take two cycles to execute.

10 POWER MANAGEMENT

The W79E4051/2051 series has several features that help the user to control the power consumption of the device. These modes are discussed in the next two sections.

10.1 Idle Mode

The user can put the device into idle mode by writing 1 to the bit PCON.0. The instruction that sets the idle bit is the last instruction that will be executed before the device goes into Idle Mode. In the Idle mode, the clock to the CPU is halted, but not to the Interrupt, Timer, Watchdog timer, PWM, Analog Comparator(CIPE=1) and Serial port blocks. This forces the CPU state to be frozen; the Program counter, the Stack Pointer, the Program Status Word, the Accumulator and the other registers hold their contents. The port pins hold the logical states they had at the time Idle was activated. The Idle mode can be terminated in two ways. Since the interrupt controller is still active, the activation of any enabled interrupt can wake up the processor. This will automatically clear the Idle bit, terminate the Idle mode, and the Interrupt Service Routine (ISR) will be executed. After the ISR, execution of the program will continue from the instruction which put the device into Idle Mode.

The Idle mode can also be exited by activating the reset. The device can put into reset either by applying a high on the external RST pin, a Power on reset condition or a Watchdog timer reset. The external reset pin has to be held high for at least two machine cycles i.e. 8 clock periods to be recognized as a valid reset. In the reset condition the program counter is reset to 0000h and all the SFRs are set to the reset condition. Since the clock is already running there is no delay and execution starts immediately. In the Idle mode, the Watchdog timer continues to run, and if enabled, a time-out will cause a watchdog timer interrupt which will wake up the device. The software must reset the Watchdog timer in order to preempt the reset which will occur after 512 clock periods of the time-out. When the W79E4051/2051 series are exiting from an Idle Mode with a reset, the instruction following the one which put the device into Idle Mode is not executed. So there is no danger of unexpected writes.

P1.0 and P1.1 should be set to 1 if external pull-ups are applied, or set to 0 if without external pull-ups, or configured to quasi I/O mode by setting P1M1 bit0 and bit1 to high.

10.2 Power Down Mode

The device can be put into Power Down mode by writing 1 to bit PCON.1. The instruction that does this will be the last instruction to be executed before the device goes into Power Down mode. In the Power Down mode, all the clocks are stopped and the device comes to a halt. All activity, exception of Brownout reset, $\overline{INT1}$, $\overline{INT0}$, watchdog timer(Config0.WDTCK=0) and Analog Comparator(CIPE=1), is completely stopped and the power consumption is reduced to the lowest possible value. The port pins output the values held by their respective SFRs.

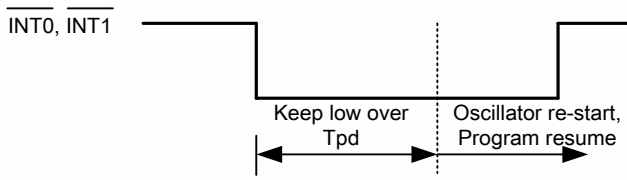
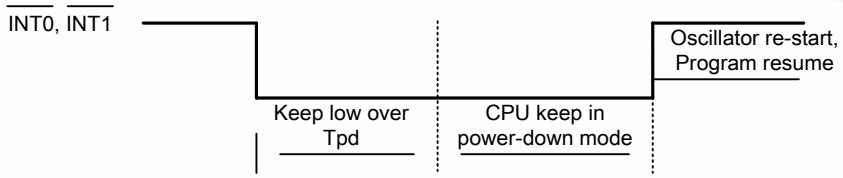
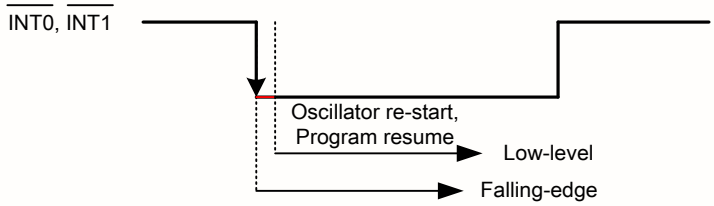
Before CPU enters power-down mode, P1.0 and P1.1 should be set to 1 if external pull-ups are applied, or set to 0 if without external pull-ups, or configured to quasi I/O mode by setting P1M1 bit0 and bit1 to high.

An external reset can be used to exit the Power down state. The high on RST pin terminates the Power Down mode, and restarts the clock. The program execution will restart from 0000h. In the Power down mode, the clock is stopped, so the Watchdog timer cannot be used to provide the reset to exit Power down mode when its clock source is external OSC or crystal.

The sources that can wake up from the power down mode are external interrupts, brownout reset (BOR), watchdog timer interrupt (if Config0 bit WDTCK = 0) and Analog Comparator(if SFR bit

CIPE=1). The W79E4051/2051 series can be waken up from the Power Down mode by forcing the above sources activation, provided the corresponding interrupt is enabled, while the global enable (EA) bit is set. If these conditions are met, then interrupt event will re-start the oscillator. The device will then execute the interrupt service routine for the corresponding external interrupt. After the interrupt service routine is completed, the program execution returns to the instruction after one which put the device into Power Down mode and continues from there. During Power down mode, if AUXR1.LPBOV = 1 and AUXR1.BOD = 0, the internal RC clock will be enabled and hence save power.

In W79E4051/2051 series either a *low-level or a falling-edge at external interrupt pin,* $\overline{\text{INT1}}$ or $\overline{\text{INT0}}$ ***will re-start the oscillator. W79E4051/2051 provides 3 wake-up modes, selected by SFR bits PWDEX1 and PWDEX0, that the external interrupt pins can terminate power-down mode. Refer to the table below.***

PWDEX[1:0]	TRIGGER TYPE	FUNCTION TO TERMINATE POWER-DOWN MODE
0, 0 (Mode1)	Low-level	
0, 1 (Mode2)	Low-level	
1, x (Mode3)	Low-level and Falling-edge	

In mode1 and mode2, the external interrupt pin must keep low longer than Tpd otherwise CPU stays in power-down mode continuously. Tpd is about 2mS counted by built-in RC oscillator.

11 RESET CONDITIONS

The user has several hardware related options for placing the W79E4051/2051 series into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software.

11.1 Sources of reset

11.1.1 External Reset

The device samples the RST pin every machine cycle during state C4. The RST pin must be held high for at least two machine cycles before the reset circuitry applies an internal reset signal. Thus, this reset is a synchronous operation and requires the clock to be running.

The device remains in the reset state as long as RST pin is high and remains high up to two machine cycles after RST is deactivated. Then, the device begins program execution at 0000h. There are no flags associated with the external reset, but, since the other two reset sources do have flags, the external reset is the cause if those flags are clear.

11.1.2 Power-On Reset (POR)

If the power supply falls below V_{RST}, the device goes into the reset state. When the power supply returns to proper levels, the device performs a power-on reset and sets the POR flag. The software should clear the POR flag, or it will be difficult to determine the source of future resets. V_{RST} is about 2.0V.

11.1.3 Brown-Out Reset (BOR)

If the power supply falls below brownout voltage of V_{BOV}, the device goes into the reset state. When the power supply returns to proper levels, the device performs a brownout reset.

11.1.4 Watchdog Timer Reset

The Watchdog Timer is a free-running timer with programmable time-out intervals. The program must clear the Watchdog Timer before the time-out interval is reached to restart the count. If the time-out interval is reached, an interrupt flag is set. 512 clocks later, if the Watchdog Reset is enabled and the Watchdog Timer has not been cleared, the Watchdog Timer generates a reset. The reset condition is maintained by the hardware for two machine cycles, and the WTRF bit in WDCON is set. Afterwards, the device begins program execution at 0000h.

11.2 Reset State

When the device is reset, most registers return to their initial state. The Watchdog Timer is disabled if the reset source was a power-on reset. The port registers are set to FFh, which puts most of the port pins in a high state. The Program Counter is set to 0000h, and the stack pointer is reset to 07h. After this, the device remains in the reset state as long as the reset conditions are satisfied.

Reset does not affect the on-chip RAM, however, so RAM is preserved as long as VDD remains above approximately 2V, the minimum operating voltage for the RAM. If VDD falls below 2V, the RAM contents are also lost. In either case, the stack pointer is always reset, so the stack contents are lost.

The WDCON SFR bits are set/cleared in reset condition depending on the source of the reset. The WDCON SFR is set to a 0x00 0000B on the reset. WTRF (WDCON.2) is set to a 1 on a Watchdog timer reset, but to a 0 on power on/down resets. WTRF (WDCON.2) is not altered by external reset. EWRST (WDCON.1) is cleared by any reset. Software or any reset will clear WDIF (WDCON.3) bit.

Some of the bits in the WDCON SFR (WDRUN, WDCLR, EWRST, WDIF, WD0 and WD1) have unrestricted read access which required Timed Access procedure to write. The remaining bits have unrestricted write accesses. Please refer TA register description.

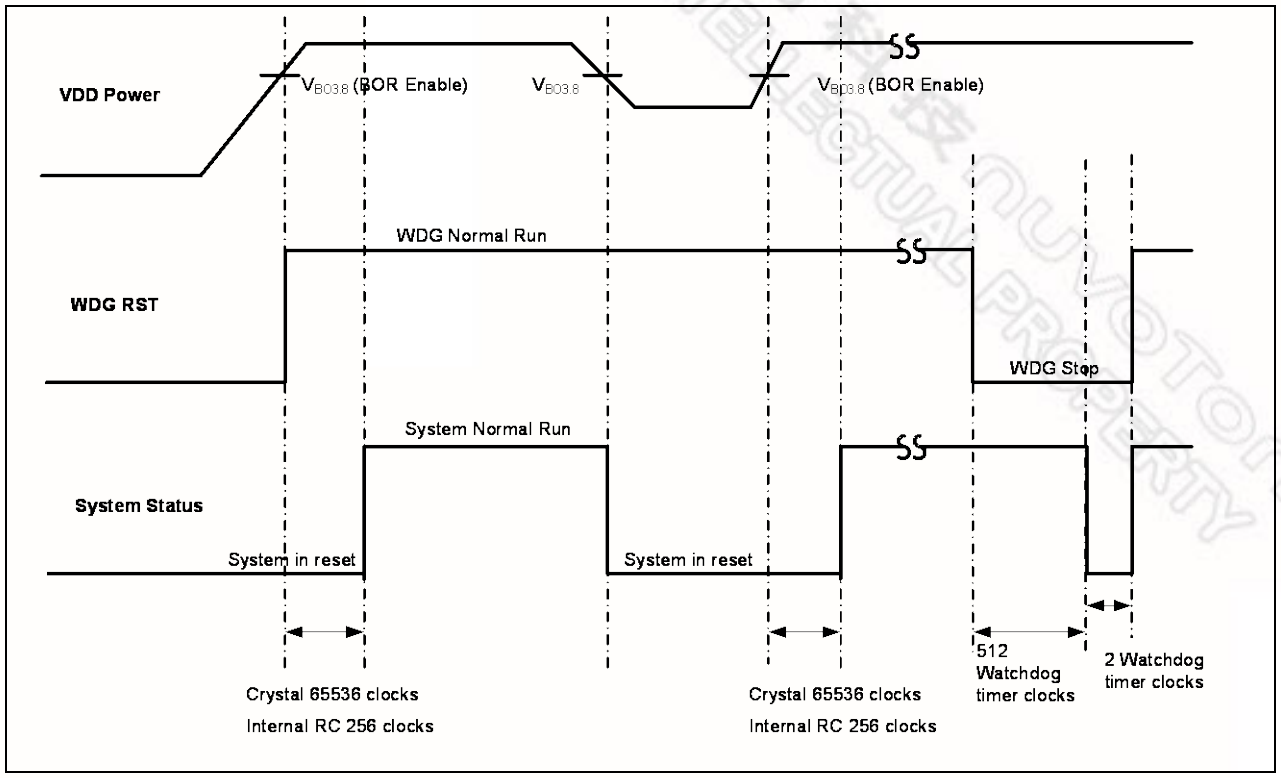


Figure 11-1: Internal reset and VDD monitor timing diagram

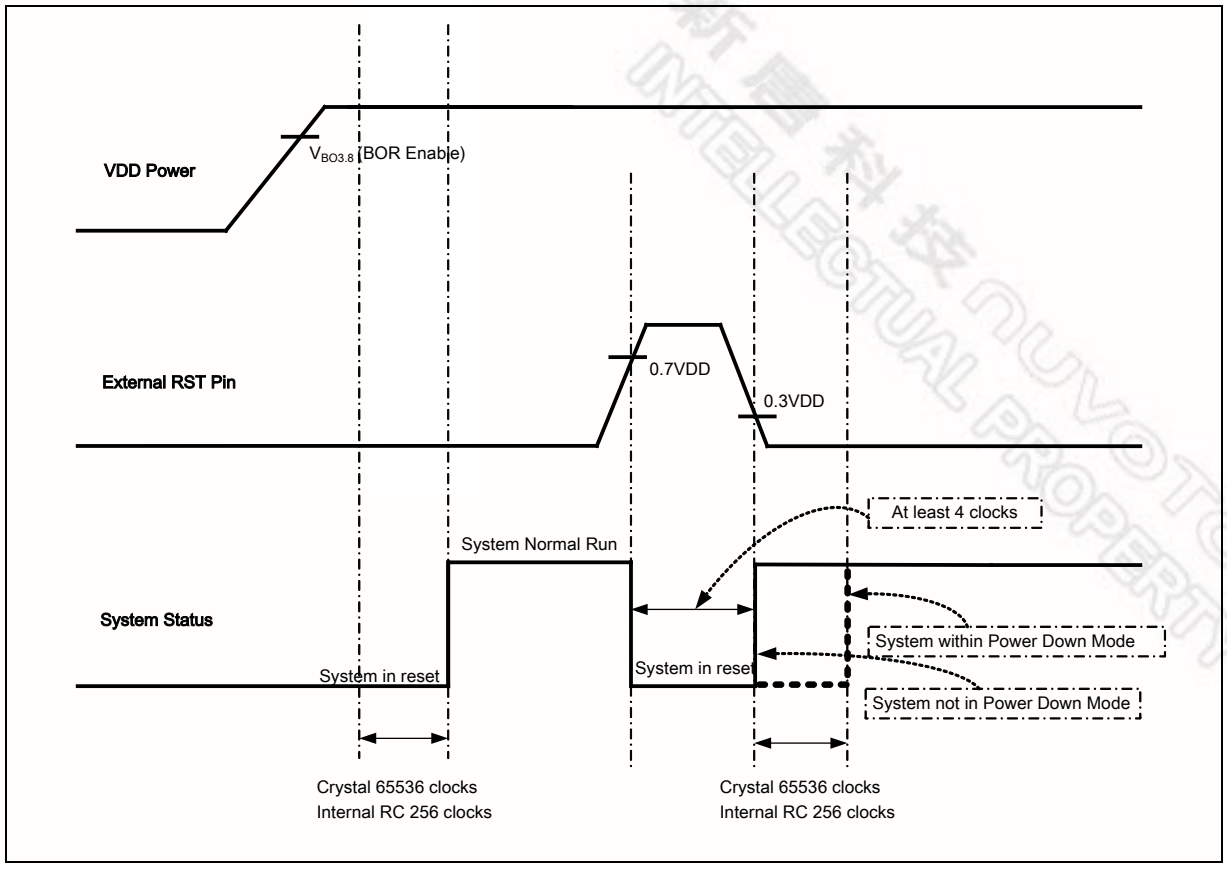


Figure 11-2: External reset timing diagram

12 INTERRUPTS

The W79E4051/2051 series have 9 interrupts source that are **IE0, BOF, WDIF, TF0, CF, IE1, TF1, TI+RI and PWMF**. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

If an external interrupt is requested when the W79E4051/2051 series are put into Power Down or Idle mode, the interrupt will cause the processor to wake up and resume operation.

12.1 Interrupt Sources

The External Interrupts $\overline{\text{INT0}}$ and $\overline{\text{INT1}}$ can be either edge triggered or level triggered, programmable through bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Watchdog timer can be used as a system monitor or a simple timer. In either case, when the time-out count is reached, the Watchdog Timer interrupt flag WDIF (WDCON.3) is set. If the interrupt is enabled by the enable bit EIE.4, then an interrupt will occur.

PWM interrupt is generated when its' 10-bit down counter underflows. PWMF flag is set and PWM interrupt is generated if enabled. PWMF is set by hardware and can only be cleared by software.

The comparator can generate interrupt after comparator output has occurs by CF flag. This bit is not automatically cleared by the hardware, and the user will have to clear this bit using software.

The Serial block can generate interrupt on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

Brownout detect can cause brownout flag, BOF, to be asserted if power voltage drop below brownout voltage level. Interrupt will occur if BOI (AUXR1.5), EBOV (EIE.6) and global interrupt enable are set.

All the bits that generate interrupts can be set or reset by software, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all interrupts.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.
2. The current polling cycle is the last machine cycle of the instruction currently being execute.
3. The current instruction does not involve a write to IE, IP and IPH, registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, INT0 and INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as follows:

VECTOR LOCATIONS FOR INTERRUPT SOURCES

SOURCE	VECTOR ADDRESS	SOURCE	VECTOR ADDRESS
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Brownout Interrupt	002Bh
Analog Comparator	0033h	-	003Bh
-	0043h	-	004Bh
Watchdog Timer	0053h	-	005Bh
-	0063h	PWM Period Interrupt	006Bh

Table 12-1: Vector locations for interrupt sources

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what it was after the hardware LCALL, if the execution is return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

12.2 Priority Level Structure

The W79E4051/2051 series uses a four priority level interrupt structure (highest, high, low and lowest) and supports up to 9 interrupt sources. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as table below. This allows great flexibility in controlling and handling many interrupt sources.

Priority Bits		Interrupt Priority Level
IPxH	IPx	
0	0	Level 0 (lowest priority)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest priority)

Table 12-2: Four-level interrupt priority

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the IPx and IPxH registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

As below Table summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and whether each interrupt may wake up the CPU from Power Down mode.

Source	Flag	Vector address	Interrupt Enable Bits	Interrupt Priority	Flag cleared by	Arbitration Ranking	Power Down Wakeup
External Interrupt 0	IE0	0003H	EX0 (IE0.0)	IP0H.0, IP0.0	Edge: Hardware, Software; Level: Follow the inverse of pin	1(highest)	Yes
Brownout Detect	BOF	002BH	EBOV (EIE.6)	IP1H.6, IP1.6	Software	2	Yes
Watchdog Timer	WDIF	0053H	EWDI (EIE.4)	IP1H.4, IP1.4	Software	3	Yes(1)
Timer 0 Interrupt	TF0	000BH	ET0 (IE.1)	IP0H.1, IP0.1	Hardware, Software	4	No
External Interrupt 1	IE1	0013H	EX1 (IE.2)	IP0H.2, IP0.2	Edge: Hardware, Software; Level:	5	Yes

Source	Flag	Vector address	Interrupt Enable Bits	Interrupt Priority	Flag cleared by	Arbitration Ranking	Power Down Wakeup
					Follow the inverse of pin		
Timer 1 Interrupt	TF1	001BH	ET1 (IE.3)	IP0H.3, IP0.3	Hardware, Software	6	No
Serial Port Tx and Rx	TI & RI	0023H	ES (IE.4)	IP0H.4, IP0.4	Software	7	No
Comparator Interrupt	CF	0033H	EC (IE.6)	IP0H.6, IP0.6	Software	8	Yes(2)
PWM Period Interrupt	PWMF	006BH	EPWM (EIE.5)	IP1H.5, IP1.5	Software	9(lowest)	No

Table 12-3: Vector location for Interrupt sources and power down wakeup

Note:

1. The Watchdog Timer can wake up Power Down Mode when its clock source is from internal RC.
2. The comparator can wake up Power Down Mode when bit ACSR.5(CIPE) is set to high.

12.3 Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{INT0}$ to RI+TI, they are sampled at C3 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the W79E4051/2051 series are performing a write to IE, IP and IPH and then executes a MUL or DIV instruction. From the time an interrupt source is activated, the longest reaction time is 12 machine cycles. This includes 1 machine cycle to detect the interrupt, 2 machine cycles to complete the IE, IP or IPH access, 5 machine cycles to complete the MUL or DIV instruction and 4 machine cycles to complete the hardware LCALL to the interrupt vector location.

Thus in a single-interrupt system the interrupt response time will always be more than 5 machine cycles and not more than 12 machine cycles. The maximum latency of 12 machine cycles is 48 clock cycles. Note that in the standard 8051 the maximum latency is 8 machine cycles which equals 96 machine cycles. This is a 50% reduction in terms of clock periods.

13 PROGRAMMABLE TIMERS/COUNTERS

The W79E4051/2051 series have two 16-bit programmable timer/counters and one programmable Watchdog Timer. The Watchdog Timer is operationally quite different from the other two timers.

13.1 Timer/Counters 0 & 1

W79E4051/2051 has two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock or 1/6 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

13.2 Time-Base Selection

W79E4051/2051 provides users with two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on W79E4051/2051 and the standard 8051 can be matched. This is the default mode of operation of the W79E4051/2051 timers. The user also has the option to count in the 2-times mode, where the timers will increment at the rate of 1/6 clock speed. This will straight-away increase the counting speed three times. This selection is done by the T0M and T1M bit in CKCON SFR. A reset sets these bits to 0, and the timers then operate in the standard 8051 mode. The user should set these bits to 1 if the timers are to operate in turbo mode.

13.2.1 Mode 0

In Mode 0, the timer/counter is a 13-bit counter. The 13-bit counter consists of THx (8 MSB) and the five lower bits of TLx (5 LSB). The upper three bits of TLx are ignored. The timer/counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. When $C/\overline{T}$ is 0, the timer/counter counts clock cycles; when $C/\overline{T}$ is 1, it counts falling edges on T0 (Timer 0) or T1 (Timer 1). For clock cycles, the time base may be 1/12 or 1/6 clock speed, and the falling edge of the clock increments the counter. When the 13-bit value moves from 1FFFh to 0000h, the timer overflow flag TFx is set, and an interrupt occurs if enabled. This is illustrated in next figure below.

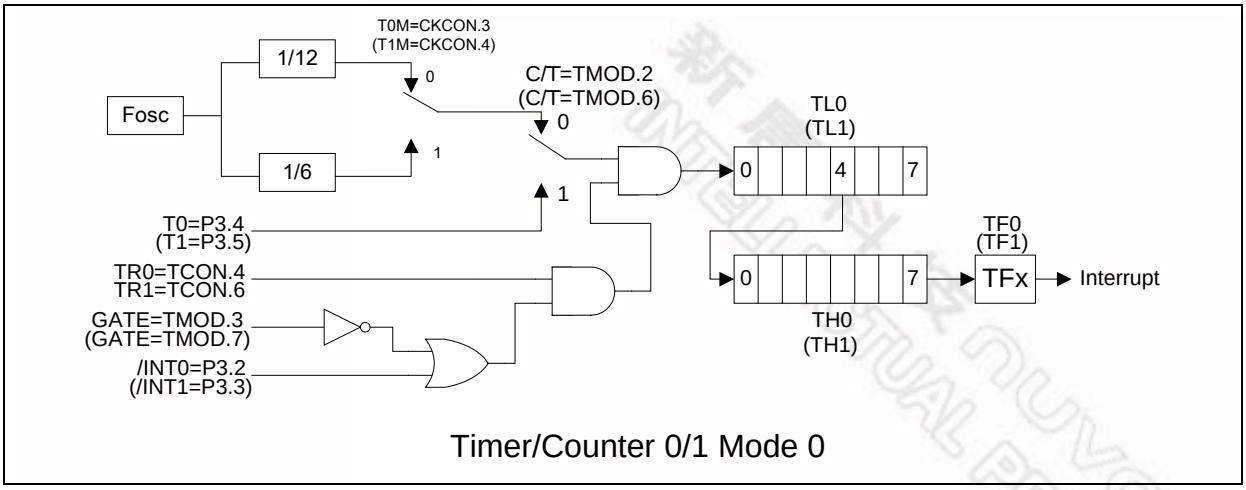


Figure 13-1: Timer/Counters 0 & 1 in Mode 0

13.2.2 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13-bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

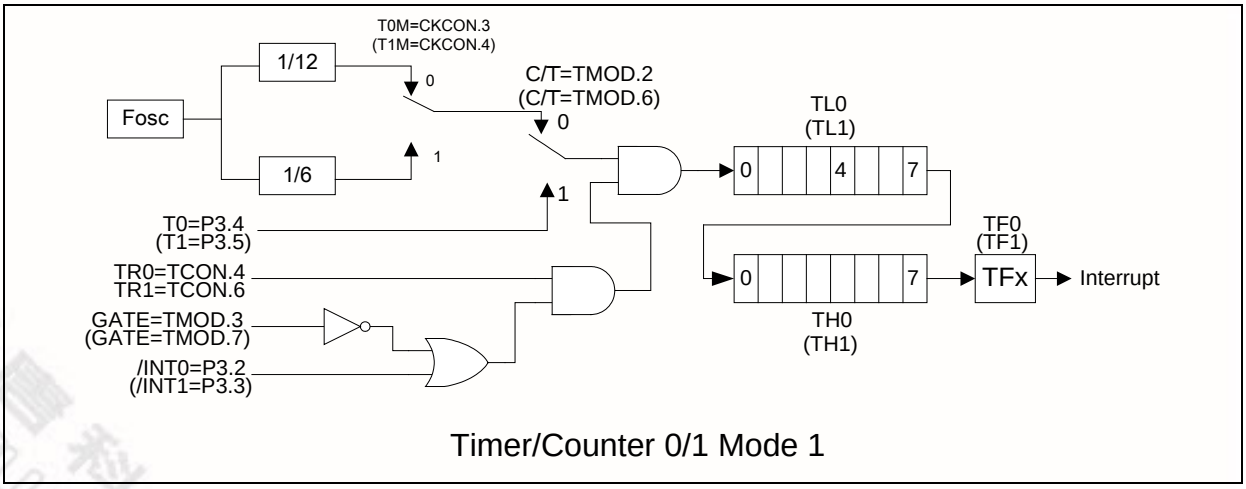


Figure 13-2: Timer/Counters 0 & 1 in Mode 1

13.2.3 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as an 8-bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{\text{INTx}}$ pins. As in the other two modes 0 and 1 mode 2 allows counting of either clock cycles (clock/12 or clock/6) or pulses on pin Tn.

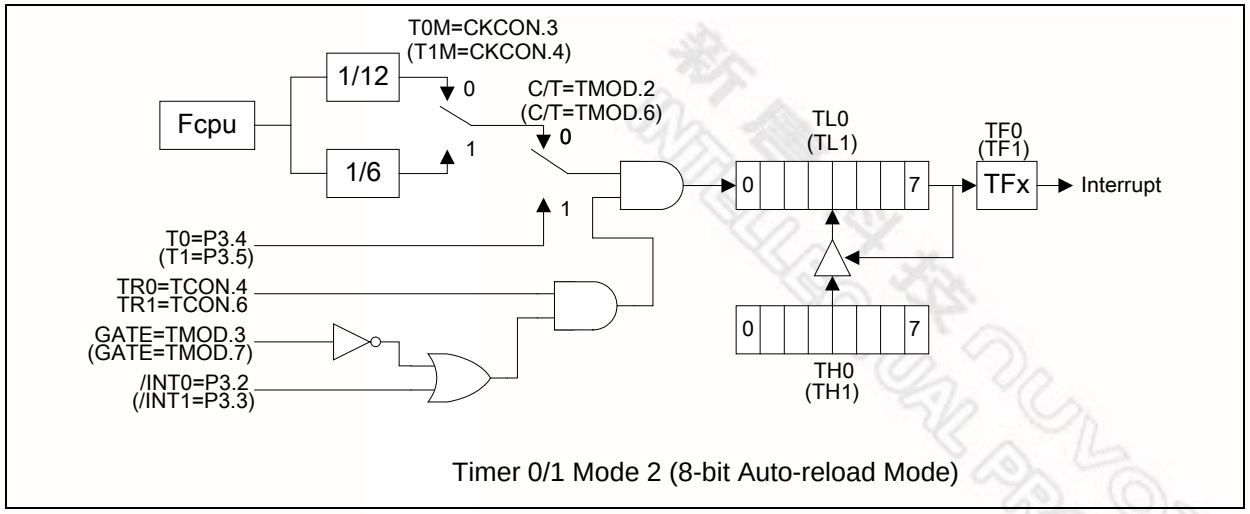


Figure 13-3: Timer/Counter 0 & 1 in Mode 2

13.2.4 Mode 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer/Counter 0 control bits $C/\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2, but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

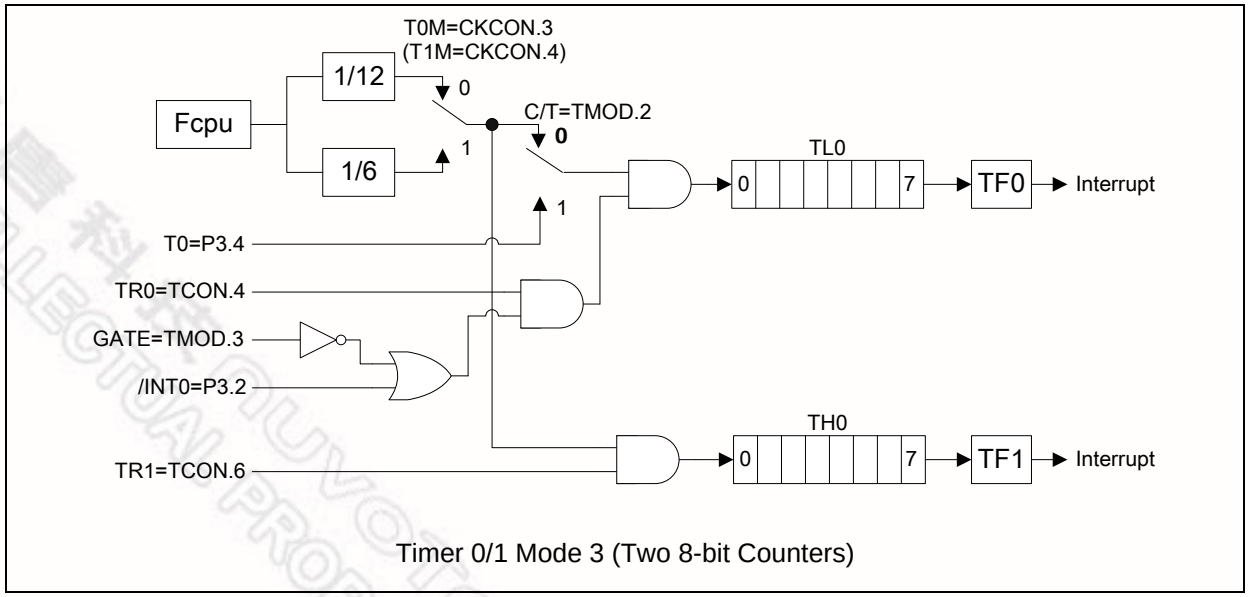


Figure 13-4: Timer/Counter Mode 3

14 NVM MEMORY

The W79E4051/2051 series have NVM data memory of **128** bytes for customer's data store used. The NVM data memory has **8** pages area and each page has **16** bytes. The page addresses are shown on Figure 14-1

The NVM memory can be read/write by customer program to access. Read NVM data is by MOVC A,@A+DPTR instruction, and write data is by SFR of NVMADDRL, NVMDATA and NVMCON. Before write data to NVM memory, the page must be erased by providing page address on NVMADDRL, which high and low byte address of On-Chip Code Memory space will decode, then set EER of NVMCON.7. This will automatically hold fetch program code and PC Counter, and execute page erase. After finished, this bit will be cleared by hardware. The erase time is ~ 5ms.

For writing data to NVM memory, user must set address and data to NVMADDRL and NVMDATA, then set EWR of NVMCON.6 to initiate NVM data write. The uC will hold program code and PC Counter, and then write data to mapping address. Upon write completion, the EWR bit will be cleared by hardware, the uC will continue execute next instruction. The program time is ~50us.

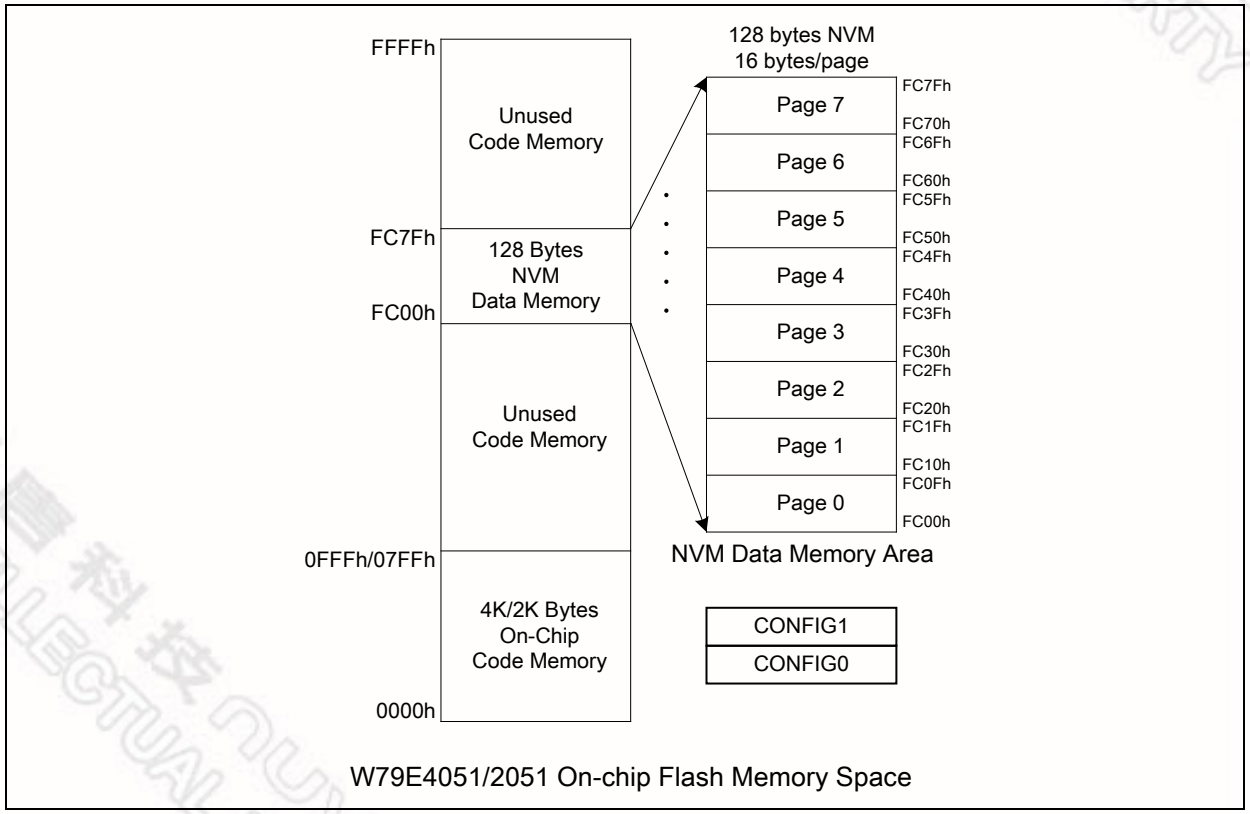


Figure 14-1: W79E4051/2051 Memory Map

15 WATCHDOG TIMER

The Watchdog Timer is a free-running Timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a flag is set, which can cause an interrupt if enabled, and a system reset can also be caused if it is enabled. The interrupt will occur if the individual interrupt enable and the global enable are set. The interrupt and reset functions are independent of each other and may be used separately or together depending on the user's software.

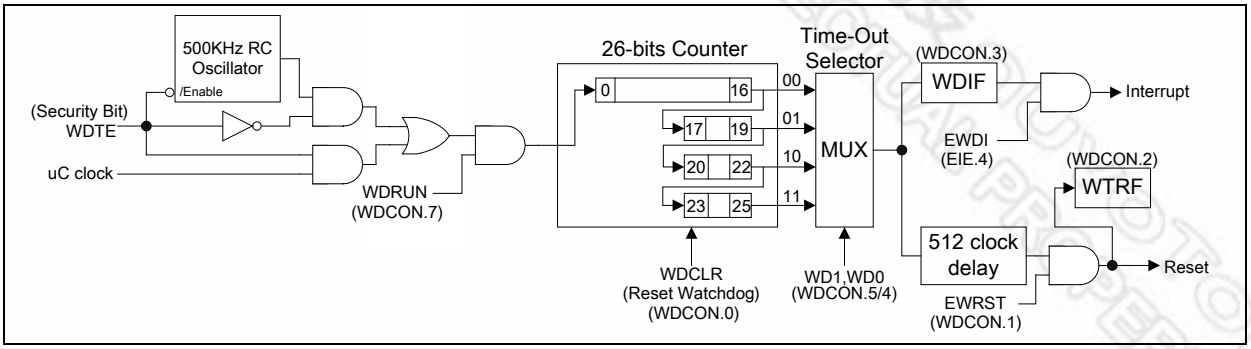


Figure 15-1: Watchdog Timer

The Watchdog Timer should first be restarted by using WDCLR. This ensures that the timer starts from a known state. The WDCLR bit is used to restart the Watchdog Timer. This bit is self clearing, i.e. after writing a 1 to this bit the software will automatically clear it. The Watchdog Timer will now count clock cycles. The time-out interval is selected by the two bits WD1 and WD0 (WDCON.5 and WDCON.4). When the selected time-out occurs, the Watchdog interrupt flag WDIF (WDCON.3) is set. After the time-out has occurred, the Watchdog Timer waits for an additional 512 WDT clock cycles. If the Watchdog Reset EWRST (WDCON.1) is enabled, then 512 clocks after the time-out, if there is no WDCLR, a system reset due to Watchdog Timer will occur. This will last for two machine cycles, and the Watchdog Timer reset flag WTRF (WDCON.2) will be set. This indicates to the software that the Watchdog was the cause of the reset.

When used as a simple timer, the reset and interrupt functions are disabled. The timer will set the WDIF flag each time the timer completes the selected time interval. The WDIF flag is polled to detect a time-out and the WDCLR allows software to restart the timer. The Watchdog Timer can also be used as a very long timer. The interrupt feature is enabled in this case. Every time the time-out occurs an interrupt will occur if the global interrupt enable EA is set.

The main use of the Watchdog Timer is as a system monitor. This is important in real-time control applications. In case of some power glitches or electro-magnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. Using the watchdog timer interrupt during software development will allow the user to select ideal watchdog reset locations. The code is first written without the watchdog interrupt or reset. Then the Watchdog interrupt is enabled to identify code locations where interrupt occurs. The user can now insert instructions to reset the Watchdog Timer, which will allow the code to run without any Watchdog Timer interrupts. Now the Watchdog Timer reset is enabled and the Watchdog interrupt may be disabled. If any errant code is executed now, then the reset Watchdog Timer instructions will not be executed at the required instants and Watchdog reset will occur.

The Watchdog Timer time-out selection will result in different time-out values depending on the clock

speed. The reset, when enabled, will occur when 512 clocks after time-out has occurred.

WD1	WD0	Interrupt time-out	Reset time-out	Number of Clocks	Time @ 10 MHz
0	0	2^{17}	2^{17} + 512	131072	13.11 mS
0	1	2^{20}	2^{20} + 512	1048576	104.86 mS
1	0	2^{23}	2^{23} + 512	8388608	838.86 mS
1	1	2^{26}	2^{26} + 512	67108864	6710.89 mS

Table 15-1: Time-out values for the Watchdog Timer

The Watchdog Timer will be disabled by a power-on/fail reset. The Watchdog Timer reset does not disable the Watchdog Timer, but will restart it. In general, software should restart the timer to put it into a known state. The control bits that support the Watchdog Timer are discussed below.

15.1 WATCHDOG CONTROL

WDIF: WDCON.3 - Watchdog Timer Interrupt flag. This bit is set whenever the time-out occurs in the Watchdog Timer. If the Watchdog interrupt is enabled (EIE.4), then an interrupt will occur (if the global interrupt enable is set and other interrupt requirements are met). Software or any reset can clear this bit.

WTRF: WDCON.2 - Watchdog Timer Reset flag. This bit is set whenever a watchdog reset occurs. This bit is useful for determined the cause of a reset. Software must read it, and clear it manually. A Power-fail reset will clear this bit. If EWRST = 0, then this bit will not be affected by the Watchdog Timer.

EWRST: WDCON.1 - Enable Watchdog Timer Reset. This bit when set to 1 will enable the Watchdog Timer reset function. Setting this bit to 0 will disable the Watchdog Timer reset function, but will leave the timer running.

WDCLR: WDCON.0 - Reset Watchdog Timer. This bit is used to clear the Watchdog Timer and to restart it. This bit is self-clearing, so after the software writes 1 to it the hardware will automatically clear it. If the Watchdog Timer reset is enabled, then the WDCLR has to be set by the user within 512 clocks of the time-out. If this is not done then a Watchdog Timer reset will occur.

15.2 CLOCK CONTROL of Watchdog

WD1, WD0: WDCON.5, WDCON.4 - Watchdog Timer Mode select bits. These two bits select the time-out interval for the watchdog timer. The reset time is 512 clocks longer than the interrupt time-out value.

The default Watchdog time-out is 2^{17} clocks, which is the shortest time-out period. The **WDRUN, WD1, WD0, EWRST, WDIF and WDCLR** bits are protected by the Timed Access procedure. This prevents software from accidentally enabling or disabling the watchdog timer. More importantly, it makes it highly improbable that errant code can enable or disable the Watchdog Timer.

The security bit WDTCK is located at bit 7 of CONFIG register. This bit is used to configure the clock source of watchdog timer from either the internal RC or the uC clock.

When WDTCK bit is cleared and 500KHz clock is used to run the watchdog timer, there is a chance that the watchdog timer would hang as the counter does not increment. This problem arises when the watchdog is set to run, (WDCON.7, WDRUN), the WDCLR bit (WDCON.0) is set to clear the watchdog timer and the next instruction is to set the PCON register for CPU to go into idle or power-down state. The reason this happens because the setting/clearing of WDCLR bit and the watchdog counter are running on different clock domains, CPU clock and internal RC clock respectively. When

WDCLR bit is set, to reset it, the counter must be non-zero. Since the counter is running off a much slower clock, the counter may not have time to increment before the CPU clock halts as it entered the idle/power-down mode. This results in the WDCLR bit is always set & the watchdog counter remaining at zero. The solution to this problem is to monitor the WDCLR bit, ensuring that it's cleared before issue the instruction for the CPU to go into idle/power-down mode.

16 SERIAL PORT (UART)

The UART in this device is a full duplex port. It provides the user with additional features such as the Frame Error Detection and the Automatic Address Recognition. The serial port is capable of synchronous as well as asynchronous communication. In Synchronous mode the device generates the clock and operates in a half duplex mode. In the asynchronous mode, full duplex operation is available. This means that it can simultaneously transmit and receive data. The transmit register and the receive buffer are both addressed as SBUF Special Function Register. However any write to SBUF will be to the transmit register, while a read from SBUF will be from the receiver buffer register. The serial port can operate in four different modes as described below.

16.1 MODE 0

This mode provides synchronous communication with external devices. In this mode serial data is transmitted and received on the RXD line. TXD is used to transmit the shift clock. The TxD clock is provided by the device whether it is transmitting or receiving. This mode is therefore a half duplex mode of serial communication. In this mode, 8 bits are transmitted or received per frame. The LSB is transmitted/received first. The baud rate is fixed at 1/12 or 1/4 of the oscillator frequency. This Baud Rate is determined by the SM2 bit (SCON.5). When this bit is set to 0, then the serial port runs at 1/12 of the clock. When set to 1, the serial port runs at 1/4 of the clock. This additional facility of programmable baud rate in mode 0 is the only difference between the standard 8051 and W79E4051/2051.

The functional block diagram is shown below. Data enters and leaves the Serial port on the RxD line. The TxD line is used to output the shift clock. The shift clock is used to shift data into and out of this device and the device at the other end of the line. Any instruction that causes a write to SBUF will start the transmission. The shift clock will be activated and data will be shifted out on the RxD pin till all 8 bits are transmitted. If SM2 = 1, then the data on RxD will appear 1 clock period before the falling edge of shift clock on TxD. The clock on TxD then remains low for 2 clock periods, and then goes high again. If SM2 = 0, the data on RxD will appear 3 clock periods before the falling edge of shift clock on TxD. The clock on TxD then remains low for 6 clock periods, and then goes high again. This ensures that at the receiving end the data on RxD line can either be clocked on the rising edge of the shift clock on TxD or latched when the TxD clock is low.

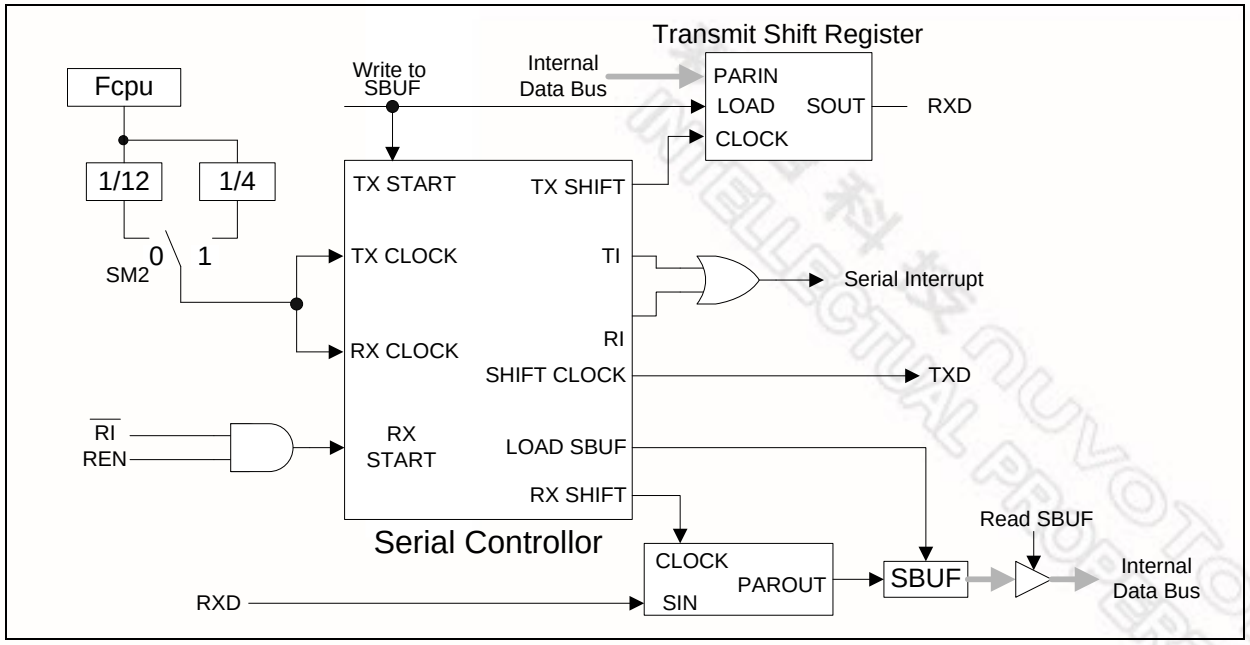


Figure 16-1: Serial Port Mode 0

The TI flag is set high in C1 following the end of transmission of the last bit. The serial port will receive data when REN is 1 and RI is zero. The shift clock (TxD) will be activated and the serial port will latch data on the rising edge of shift clock. The external device should therefore present data on the falling edge on the shift clock. This process continues till all the 8 bits have been received. The RI flag is set in C1 following the last rising edge of the shift clock on TxD. This will stop reception, till the RI is cleared by software.

16.2 MODE 1

In Mode 1, the full duplex asynchronous mode is used. Serial communication frames are made up of 10 bits transmitted on TXD and received on RXD. The 10 bits consist of a start bit (0), 8 data bits (LSB first), and a stop bit (1). On received, the stop bit goes into RB8 in the SFR SCON. The baud rate in this mode is variable. The serial baud can be programmed to be 1/16 or 1/32 of the Timer 1 overflow. Since the Timer 1 can be set to different reload values, a wide variation in baud rates is possible.

Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide-by-16 counter and not directly to the write to SBUF signal. After all 8 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 10th rollover of the divide by 16 counter after a write to SBUF.

Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide–by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

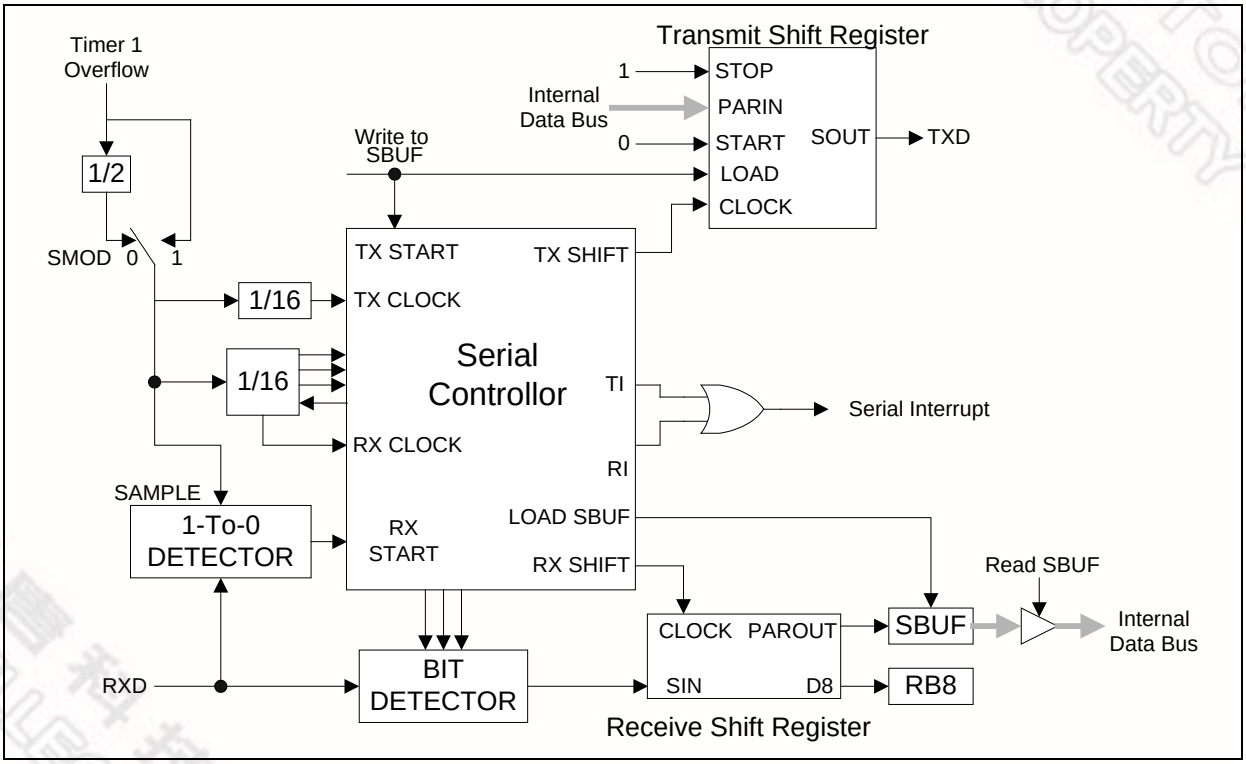


Figure 16-2: Serial Port Mode 1

16.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a programmable 9th bit (TB8) and a stop bit (0). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at C1 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at C1 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide-by-16 counter, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the C1 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide-by-16 counter after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide- by-16 counter is immediately reset. This helps to align the bit boundaries with the rollovers of the divide-by-16 counter. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three bases. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

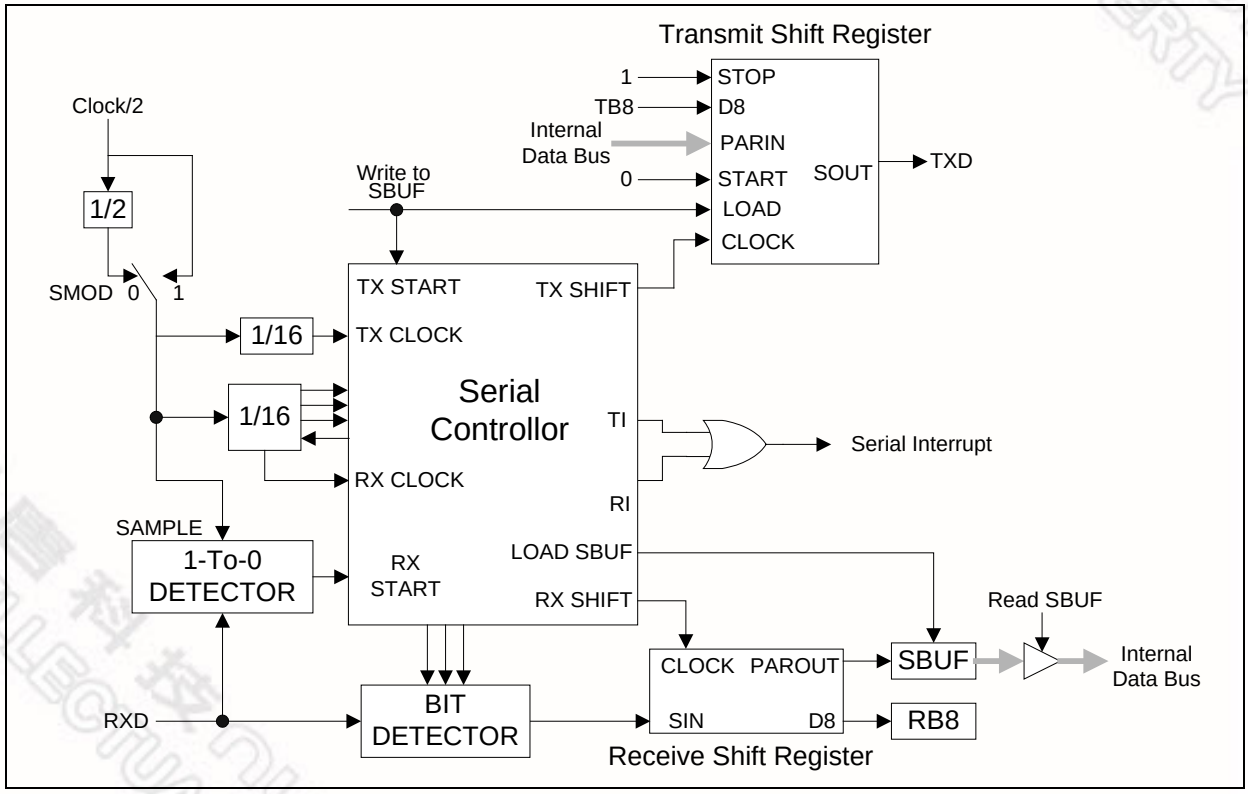


Figure 16-3: Serial Port Mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and

2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

16.4 MODE 3

This mode is similar to Mode 2 in all aspects, except that the baud rate is programmable. The user must first initialize the Serial related SFR SCON before any communication can take place. This involves selection of the Mode and baud rate. The Timer 1 should also be initialized if modes 1 and 3 are used. In all four modes, transmission is started by any instruction that uses SBUF as a destination register. Reception is initiated in Mode 0 by the condition RI = 0 and REN = 1. This will generate a clock on the TxD pin and shift in 8 bits on the RxD pin. Reception is initiated in the other modes by the incoming start bit if REN = 1. The external device will start the communication by transmitting the start bit.

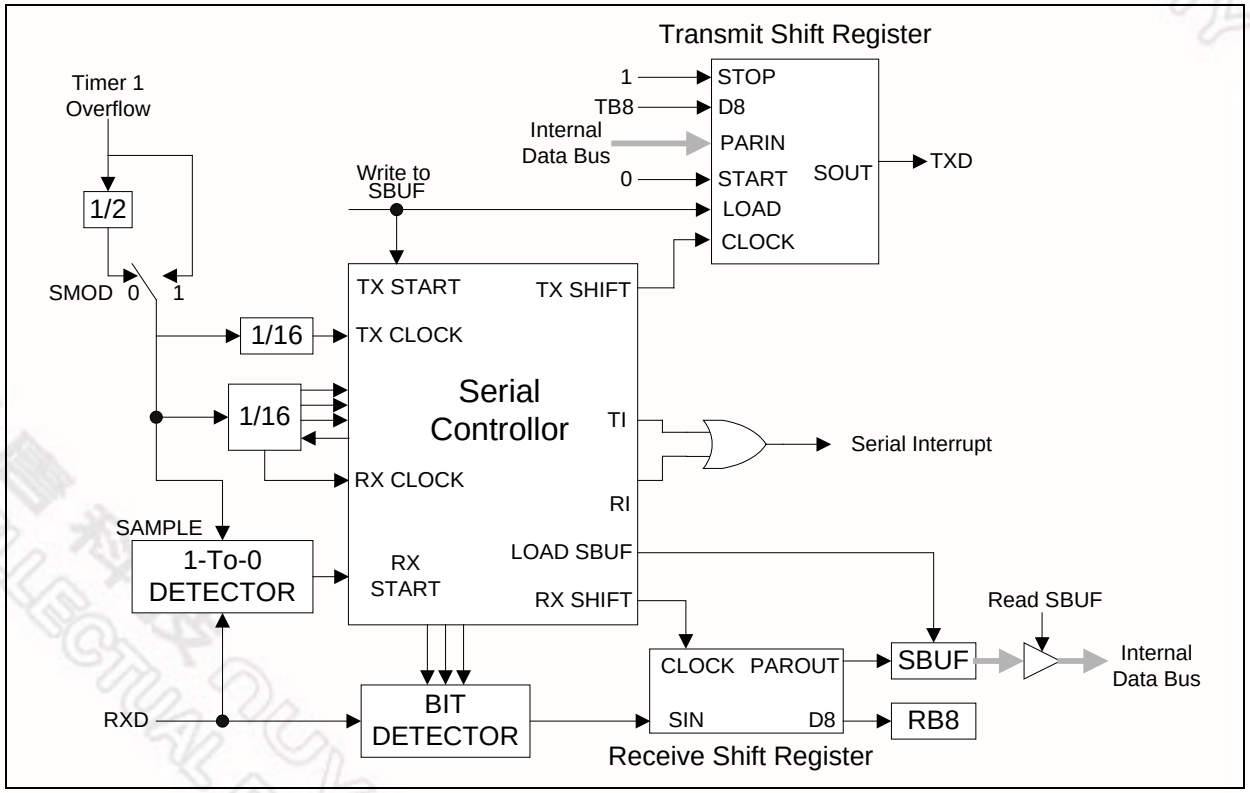


Figure 16-4: Serial Port Mode 3

SM0	SM1	MODE	TYPE	BAUD CLOCK	FRAME SIZE	START BIT	STOP BIT	9TH BIT FUNCTION
0	0	0	SYNCH.	4 OR 12 TCLKS	8 BITS	NO	NO	NONE
0	1	1	ASYNCH.	TIMER 1	10 BITS	1 BIT	1 BIT	NONE
1	0	2	ASYNCH.	32 OR 64 TCLKS	11 BITS	1 BIT	1 BIT	0, 1
1	1	3	ASYNCH.	TIMER 1	11 BITS	1 BIT	1 BIT	0, 1

Table 16-1: Serial Port Mode Summary Table

16.5 Framing Error Detection

A Frame Error occurs when a valid stop bit is not detected. This could indicate incorrect serial data communication. Typically the frame error is due to noise and contention on the serial communication line. The W79E4051/2051 series have the facility to detect such framing errors and set a flag which can be checked by software.

The Frame Error FE bit is located in SCON.7. This bit is normally used as SM0 in the standard 8051 family. However, in the W79E4051/2051 series it serves a dual function and is called SM0/FE. There are actually two separate flags, one for SM0 and the other for FE. The flag that is actually accessed as SCON.7 is determined by SMOD0 (PCON.6) bit. When SMOD0 is set to 1, then the FE flag is indicated in SM0/FE. When SMOD0 is set to 0, then the SM0 flag is indicated in SM0/FE.

The FE bit is set to 1 by hardware but must be cleared by software. Note that SMOD0 must be 1 while reading or writing to FE. If FE is set, then any following frames received without any error will not clear the FE flag. The clearing has to be done by software.

16.6 Multiprocessor Communications

Multiprocessor communications makes use of the 9th data bit in modes 2 and 3. In the W79E4051/2051 series, the RI flag is set only if the received byte corresponds to the Given or Broadcast address. This hardware feature eliminates the software overhead required in checking every received address, and greatly simplifies the software programmer task.

In the multiprocessor communication mode, the address bytes are distinguished from the data bytes by transmitting the address with the 9th bit set high. When the master processor wants to transmit a block of data to one of the slaves, it first sends out the address of the targeted slave (or slaves). All the slave processors should have their SM2 bit set high when waiting for an address byte. This ensures that they will be interrupted only by the reception of an address byte. The Automatic address recognition feature ensures that only the addressed slave will be interrupted. The address comparison is done in hardware not software.

The addressed slave clears the SM2 bit, thereby clearing the way to receive data bytes. With SM2 = 0, the slave will be interrupted on the reception of every single complete frame of data. The unaddressed slaves will be unaffected, as they will be still waiting for their address. In Mode 1, the 9th bit is the stop bit, which is 1 in case of a valid frame. If SM2 is 1, then RI is set only if a valid frame is received and the received byte matches the Given or Broadcast address.

The Master processor can selectively communicate with groups of slaves by using the Given Address.

All the slaves can be addressed together using the Broadcast Address. The addresses for each slave are defined by the SADDR and SADEN SFRs. The slave address is an 8-bit value specified in the SADDR SFR. The SADEN SFR is actually a mask for the byte value in SADDR. If a bit position in SADEN is 0, then the corresponding bit position in SADDR is don't care. Only those bit positions in SADDR whose corresponding bits in SADEN are 1 are used to obtain the Given Address. This gives the user flexibility to address multiple slaves without changing the slave address in SADDR.

The following example shows how the user can define the Given Address to address different slaves.

Slave 1:

SADDR 1010 0100
SADEN 1111 1010
Given 1010 0x0x

Slave 2:

SADDR 1010 0111
SADEN 1111 1001
Given 1010 0xx1

The Given address for slave 1 and 2 differ in the LSB. For slave 1, it is a don't care, while for slave 2 it is 1. Thus to communicate only with slave 1, the master must send an address with LSB = 0 (1010 0000). Similarly the bit 1 position is 0 for slave 1 and don't care for slave 2. Hence to communicate only with slave 2 the master has to transmit an address with bit 1 = 1 (1010 0011). If the master wishes to communicate with both slaves simultaneously, then the address must have bit 0 = 1 and bit 1 = 0. The bit 3 position is don't care for both the slaves. This allows two different addresses to select both slaves (1010 0001 and 1010 0101).

The master can communicate with all the slaves simultaneously with the Broadcast Address. This address is formed from the logical OR of the SADDR and SADEN SFRs. The zeros in the result are defined as don't cares. In most cases the Broadcast Address is FFh. In the previous case, the Broadcast Address is (1111111x) for slave 1 and (11111111) for slave 2.

The SADDR and SADEN SFRs are located at address A9h and B9h respectively. On reset, these two SFRs are initialized to 00h. This results in Given Address and Broadcast Address being set as xxxx xxxx (i.e. all bits don't care). This effectively removes the multiprocessor communications feature, since any selectivity is disabled.

17 PULSE WIDTH MODULATED OUTPUTS (PWM)

The W79E4051/2051 contains one Pulse Width Modulated (PWM) channel which generate pulses of programmable length and interval. The output for PWM0 is on P3.5. After chip reset the internal output of the PWM channel is high. In this case before the pin will reflect the state of the internal PWM output, a "1" must be written to the port bit that serves as a PWM output. A block diagram is shown in Figure 17-1. The interval between successive outputs is controlled by a 10–bit down counter which uses the internal microcontroller clock as its input. The PWM counter clock has the frequency as F_{CPWM} = P_{OSC}/Prescaler. The two pre-scaler selectable bits FP[1:0] are located at PWMCON3[1:0]. When the counter reaches underflow it is reloaded with a user selectable value. This mechanism allows the user to set the PWM frequency at any integer sub–multiple of the microcontroller clock frequency. The repetition frequency of the PWM is given by: f_{PWM} = F_{CPWM} / (PWMP+1) where PWMP is contained in PWMPH and PWMPL SFR.

A compare value greater than the counter reloaded value is in the PWM output being permanently low. In addition there are two special cases. A compare value of all zeroes, 000H, causes the output to remain permanently high. A compare value of all ones, 3FFH, results in the PWM output remaining permanently low. Again the compare value is loaded into a Compare register. The transfer from this holding register to the actual Compare register is under program control.

The PWMP register fact that writes are not into the Counter register that controls the counter; rather they are into a holding register. As described below the transfer of data from this holding register, into the register which contains the actual reload value, is controlled by the user's program.

The width of PWM output pulse is determined by the value in the appropriate Compare registers, PWM0L and PWM0H. When the counter described above reaches underflow the PWM output is forced high. It remains high until the compare value is reached at which point it goes low and keeps low until the next underflow. The number of microcontroller clock pulses that the PWM0 output is high is given by:

t_{HI} = (PWMP – PWM0+1)

Note :

1. A compare value of all zeroes, 000H, causes the PWM output to remain permanently high. A compare value of all ones, 3FFH, results in the PWM output remain permanently low. A compare value greater than the counter reloaded value will result in the PWM output being permanently low.
2. When the PWMRUN is cleared, the PWM outputs take on the state prior to the bit being cleared. In general, this state is not known. In order to place the PWM output in a known state when PWMRUN is cleared;
   - Program Compare Registers to either the "always 1" or "always 0" (see note 1).
   - Set Load (and PWMRUN) bits to 1.
   - Wait for PWMF underflow flag or Load bit (=0).
   - Clear PWMRUN.

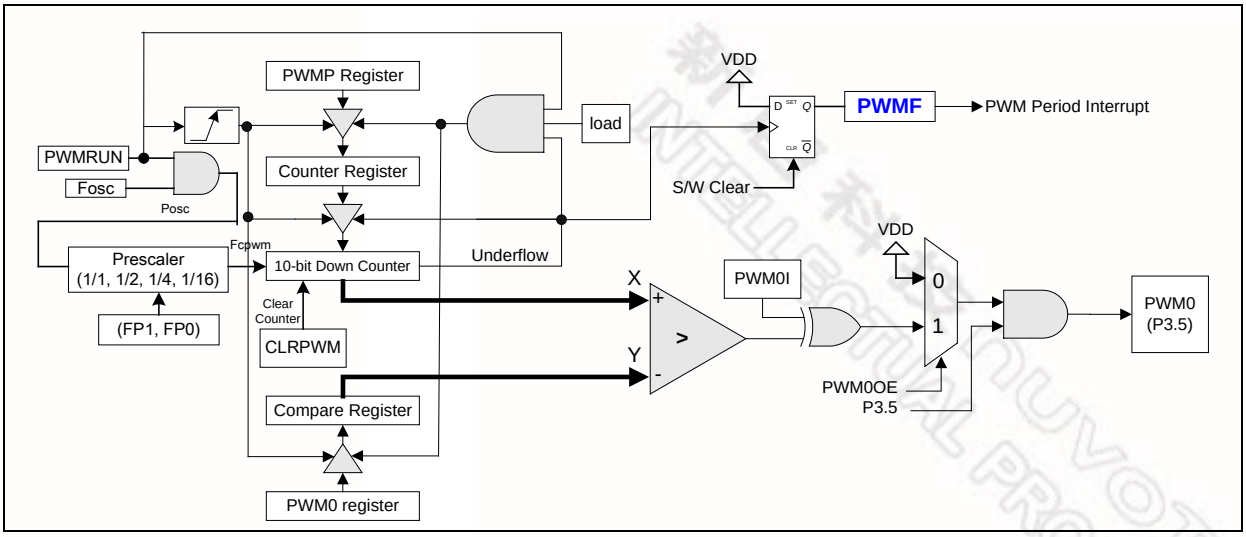


Figure 17-1: PWM block diagram

18 ANALOG COMPARATORS

The W79E4051/2051 is provided an Analog Comparator shown in Figure 18-1. The comparator output is wired to SFR bit P3.6. When the positive input of AIN0(P1.0) is greater than the negative input of AIN1(P1.1), the comparator output is high. Otherwise the output is low.

The comparator may be configured to cause an interrupt under a variety of output value conditions by setting bits CM[2:0] in ACSR(97H) register and bits CPCK[2:0] in ACCK(96H) register. The CF flag is set whenever the comparator output is matched the setting condition by CM[2:0].

Setting bit CIPE(Comparator Idle Power-down Enable) in ACSR.5 to high makes the analog comparator is active in power-down and idle mode, therefore the comparator interrupt can wake up CPU from power down and idle mode.

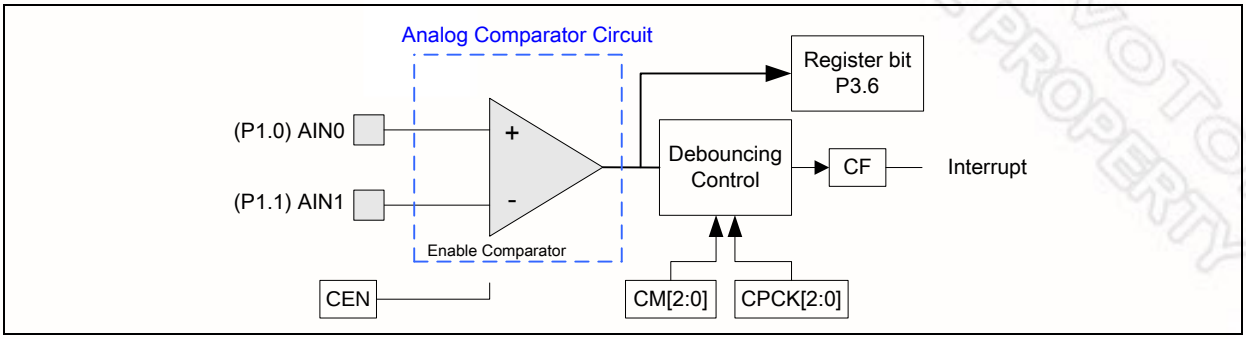


Figure 18-1: Analog Comparator

18.1 Comparator Interrupt with Debouncing

The comparator output is sampled at every State 4 (S4) of every machine cycle. The conditions on the analog inputs maybe cause the comparator output toggle excessively, especially applying slow moving analog inputs. Table 18-2: Comparator Interrupt Mode shows the 8 comparator interrupt modes set by CM[2:0] in ACSR(97H). A built-in configurable debouncing timer provides 8 debouncing timing controlled by CPCK[2:0] for widely applications. The debouncing timing is shown in Table 18-1. If CPU is in normal/Idle mode F_{DB} is from Fosc; if CPU is in power-down mode F_{DB} is from internal RC 22M/11M Hz oscillator.

CPCK2	CPCK 1	CPCK 0	Debouncing Time
0	0	0	$(3/F_{DB})*2$~$(4/F_{DB})*2$
0	0	1	$(3/F_{DB})*4$~$(4/F_{DB})*4$
0	1	0	$(3/F_{DB})*8$~$(4/F_{DB})*8$
0	1	1	$(3/F_{DB})*16$~$(4/F_{DB})*16$
1	0	0	$(3/F_{DB})*32$~$(4/F_{DB})*32$
1	0	1	$(3/F_{DB})*64$~$(4/F_{DB})*64$
1	1	0	$(3/F_{DB})*128$~$(4/F_{DB})*128$
1	1	1	$(3/F_{DB})*256$~$(4/F_{DB})*256$

Table 18-1: Comparator Debouncing Time

CM2	CM1	CM0	Comparator interrupt mode
0	0	0	Negative (Low) level
0	0	1	Positive edge
0	1	0	Toggle with debounce
0	1	1	Positive edge with debounce
1	0	0	Negative edge
1	0	1	Toggle
1	1	0	Negative edge with debounce
1	1	1	Positive (High) level

Table 18-2: Comparator Interrupt Mode

Three debouncing modes are provided to filter out this noise. In debouncing mode when the comparator output matches one of three debouncing mode condition, the debouncing timer resets and starts up-counting. The end of debouncing triggers the hardware to check if the comparator output matches the mode condition or not. If it is compliant with the mode condition the comparator flag CF is set by hardware, otherwise CF keeps low. Refer to Figure 18-2.

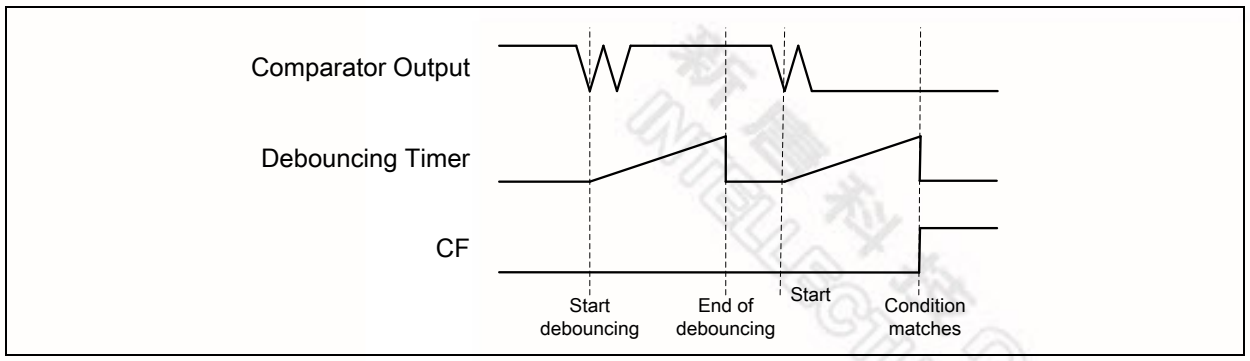


Figure 18-2: Example of Negative Edge Comparator Interrupt with Debouncing

18.2 Application circuit

It is recommended to add a decoupled capacitor as close as port pin for reducing the variation of offset voltage as show in Figure 18-3.

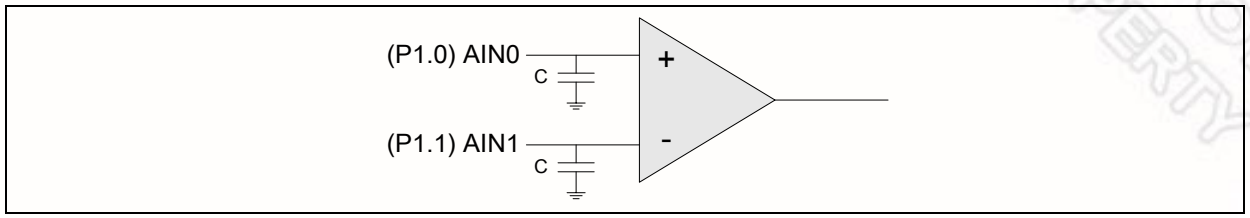


Figure 18-3: Application Circuit of Comparator

19 TIME ACCESS PROCTECTION

The W79E4051/2051 series have a new feature, like the Watchdog Timer which is a crucial to proper operation of the system. If left unprotected, errant code may write to the Watchdog control bits resulting in incorrect operation and loss of control. In order to prevent this, the W79E4051/2051 series have a protection scheme which controls the write access to critical bits. This protection scheme is done using a timed access.

In this method, the bits which are to be protected have a timed write enable window. A write is successful only if this window is active, otherwise the write will be discarded. This write enable window is open for 3 machine cycles if certain conditions are met. After 3 machine cycles, this window automatically closes. The window is opened by writing AAh and immediately 55h to the Timed Access (TA) SFR. This SFR is located at address C7h. The suggested code for opening the timed access window is

```
TA      REG     0C7h            ;Define new register TA, @0C7h
        MOV     TA, #0AAh
        MOV     TA, #055h
```

When the software writes AAh to the TA SFR, a counter is started. This counter waits for 3 machine cycles looking for a write of 55h to TA. If the second write (55h) occurs within 3 machine cycles of the first write (AAh), then the timed access window is opened. It remains open for 3 machine cycles, during which the user may write to the protected bits. Once the window closes the procedure must be repeated to access the other protected bits.

Examples of Timed Assessing are shown below.

Example 1: Valid access

```
        MOV     TA, #0AAh       ;3 M/C  Note: M/C = Machine Cycles
        MOV     TA, #055h       ;3 M/C
        MOV     WDCON, #00h     ;3 M/C
```

Example 2: Valid access

```
        MOV     TA, #0AAh       ;3 M/C
        MOV     TA, #055h       ;3 M/C
        NOP                     ;1 M/C
        SETB    EWRST           ;2 M/C
```

Example 3: Valid access

```
        MOV     TA, #0AAh       ;3 M/C
        MOV     TA, #055h       ;3 M/C
        ORL     WDCON, #00000010B ;3M/C
```

Example 4: Invalid access

```
        MOV     TA, #0AAh       ;3 M/C
        MOV     TA, #055h       ;3 M/C
        NOP                     ;1 M/C
        NOP                     ;1 M/C
        CLR     EWT             ;2 M/C
```

Example 5: Invalid Access

```
        MOV     TA, #0AAh       ;3 M/C
```

```
NOP                                 ;1 M/C
MOV         TA, #055h               ;3 M/C
SETB        EWT                     ;2 M/C
```

In the first three examples, the writing to the protected bits is done before the 3 machine cycles window closes. In Example 4, however, the writing to the protected bit occurs after the window has closed, and so there is effectively no change in the status of the protected bit. In Example 5, the second write to TA occurs 4 machine cycles after the first write, therefore the timed access window is not opened at all, and the write to the protected bit fails.

20 I/O PORT MODE SETTING

W79E4051/2051 has maximum one 8-bit(P1), one 7-bit(P3) and one 2-bit(P2) ports. Except P1.0 and P1.1, all pins are quasi-bidirectional mode, which are common with standard 80C51, that the internal weakly pull-ups are present as the port registers are set to logic one. P1.0 and P1.1, the alternate function are analog comparator inputs, stays in PMOS-off open-drain mode after CPU reset. The P2.0 (XTAL2) can be configured as clock output by setting bit ENCLK to high when CPU clock source is from on-chip RC or external Oscillator, and the frequency of clock output is divided by 4 on on-chip RC clock or external Oscillator.

20.1 Quasi-Bidirectional Output Configuration

After chip was power on or reset, the all ports except P1.0 and P1.1 output are in this mode, and output is common with the MCS-51. This mode can be used as both an input and output without the need to reconfigure the port. P1.0~P1.1 stays in PMOS-off open-drain mode after CPU reset.

P1M1.Y	PORT INPUT/OUTPUT MODE
0	Open Drain
1	Quasi-bidirectional

Table 20-1: I/O port Configuration Table

When the pin is pulled low, it is driven strongly and able to sink a fairly large current. These features are similar to an open drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

This mode has three pull-up resisters that are “strong” pull-up, “weak” pull-up and “very weak” pull-up. The “strong” pull-up is used fast transition from logic “0” change to logic “1”, and it is fast latch and transition. When port pins is occur from logic “0” to logic “1”, the strong pull-up will quickly turn on two CPU clocks to pull high then turn off.

The “weak” pull-up is turned on when the input port pin is logic “1” level or itself is logic “1”, and it provides the most source current for a quasi-bidirectional pin that output is “1” or port latch is logic “0”’.

The “very weak” pull-up is turned on when the port latch is logic “1”. If port latch is logic “0”, it will be turned off. The very weak pull-up is support a very small current that will pull the pin high if it is left floating. And the quasi-bidirectional port configuration is shown as below figure.

If port pin is low, it can drives large sink current up to about 20mA/10mA at V_{DD}=5V/2.7V.

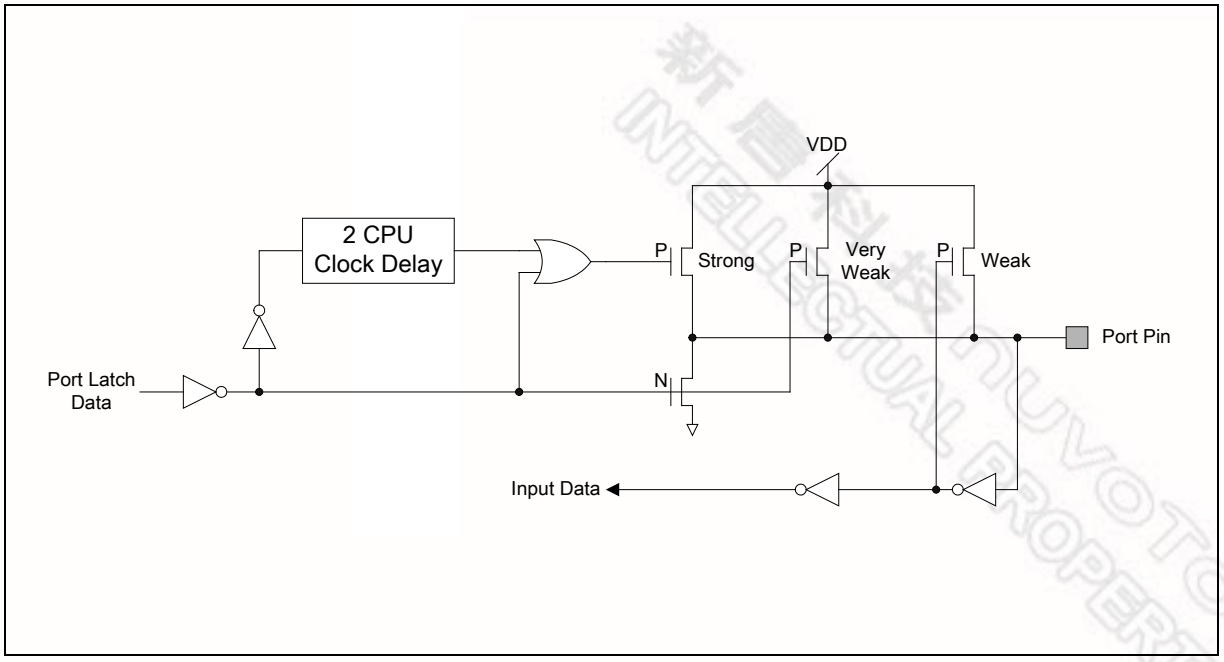


Figure 20-1: Quasi-Bidirectional Output

20.2 Open Drain Output Configuration

P1.0 and P1.1 are in open drain type after chip reset. To configure this mode is turned off all pull-ups. If used similar as a logic output, the port must has an external pull-up resister. The open drain port configuration is shown as below.

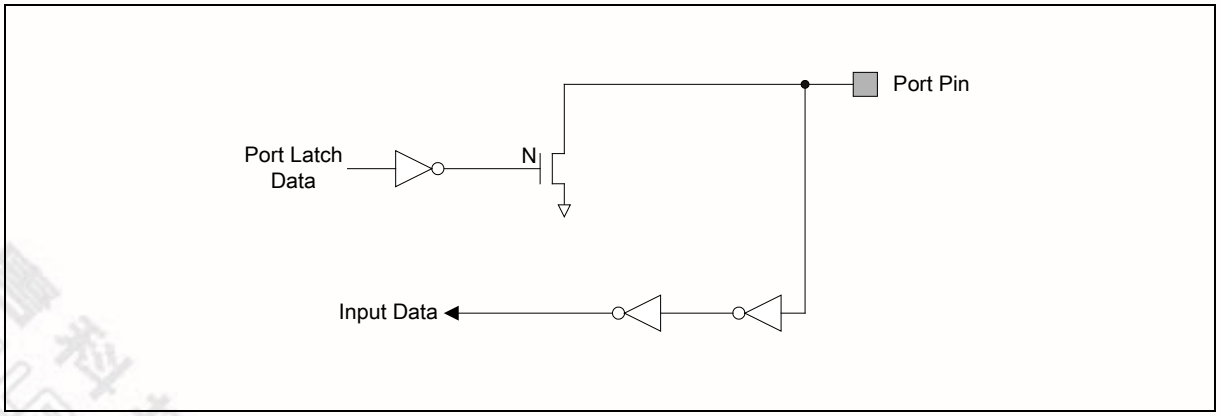


Figure 20-2: Open Drain Output

21 OSCILLATOR

The W79E4051/2051 series provides three oscillator input option. These are configured at CONFIG register (CONFIG0) that include On-Chip RC Oscillator Option, External Clock Input Option and Crystal Oscillator Input Option. The Crystal Oscillator Input frequency may be supported from 4MHz to 24MHz, and without capacitor or resister.

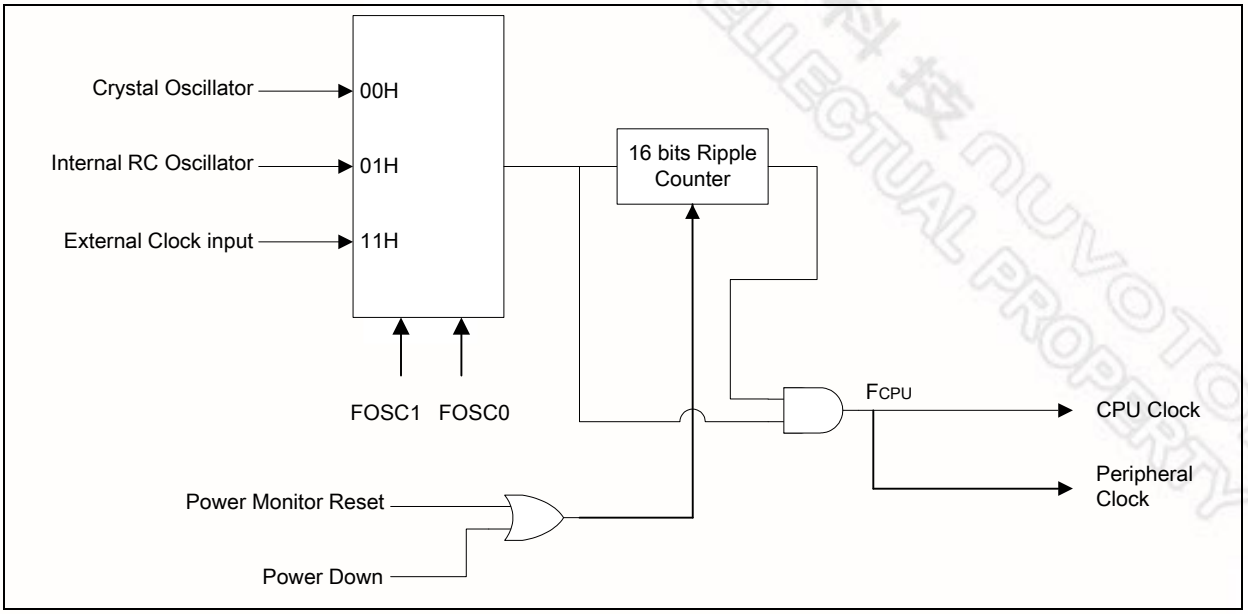


Figure 21-1: Oscillator

21.1 On-Chip RC Oscillator Option

The On-Chip RC Oscillator of W79E4051R and W79E2051R is trimmed by factory and is configurable to **11.0592MHz/22.1184MHz ± 2%** (through Configuration-bit FS1 bit) frequency to support clock source. When FOSC1, FOSC0 = 01H, the On-Chip RC Oscillator is enabled. A clock output on P2.0 (XTAL2) may be enabled when On-Chip RC oscillator is used.

Note:

For the untrimmed parts of W79E2051 and W79E4051, the untrimmed frequency of internal RC oscillator may have ± 25% deviation compared to the nominal frequency in 22.1184Mhz. It maybe has an potential risk that CPU runs over specified speed if the untrimmed frequency is over 24MHz.

21.2 External Clock Input Option

The clock source pin (XTAL1) is from External Clock Input by FOSC1, FOSC0 = 11H, and frequency range is form 4MHz up to 24MHz. A clock output on P2.0 (XTAL2) may be enabled when External Clock Input is used.

The W79E4051/2051 series supports a clock output function when either the on-chip RC oscillator or the external clock input options is selected. This allows external devices to synchronize to the W79E4051/2051 serial. When enabled, via the ENCLK bit in the ACCK.7, the clock output appears on the XTAL2/CLKOUT pin whenever the on-chip oscillator is running, including in Idle Mode. The frequency of the clock output is 1/4 of the CPU clock rate. If the clock output is not needed in Idle Mode, it may be turned off prior to entering Idle mode for saving additional power. The clock output may also be enabled when the external clock input option is selected.

22 POWER MONITORING FUNCTION

In order to prevent incorrect operation during power up and power drop, the W79E4051/2051 is provided a power monitor function, Brownout Detect.

22.1 Brownout Detect and Reset

The W79E4051/2051 has an on-chip Brown-out Detection circuit for monitoring the V_{DD} level during operation by comparing it to a programmable brownout trigger level. There are 4 brownout trigger levels available for wider voltage applications. The 4 nominal levels are 2.4V, 2.7V, 3.8V and 4.5V (programmable through BOV.1-0 bits). When V_{DD} drops to the selected brownout trigger level (V_{BOR}), the brownout detection logics will either reset the CPU until the V_{DD} voltage raises above V_{BOR} or requests a brownout interrupt at the moment that V_{DD} falls and raises through V_{BOR}. The brownout detection circuits also provides a low power brownout detection mode for power saving. When LPBOV=1, the brownout detection repeatedly senses the voltage for 64/f_{BRC} then turn off detector for 960/ f_{BRC} if V_{DD} voltage still below brownout trigger level. f_{BRC}, the frequency of built-in RC oscillator, is approximately 100K* V_{DD} HZ ±50%. The relative control bits are located in SFR AUXR1 @A2h. The Brownout Detect block is shown in Figure 22-1.

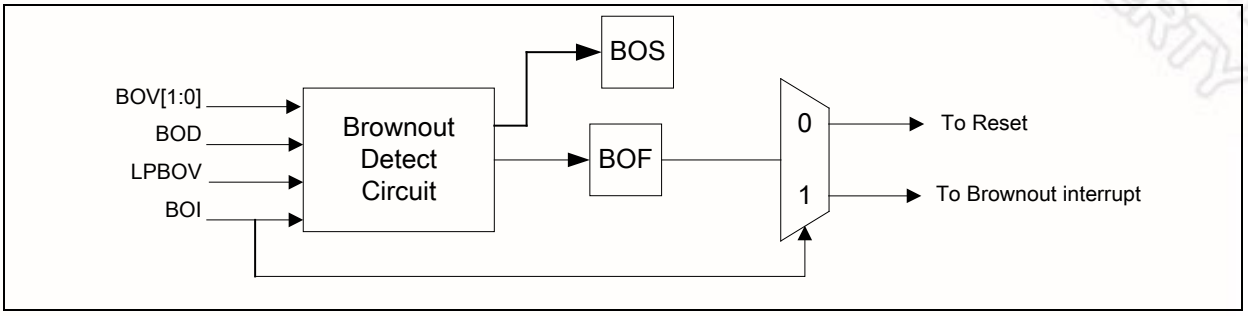


Figure 22-1: Brown-out Detect Block

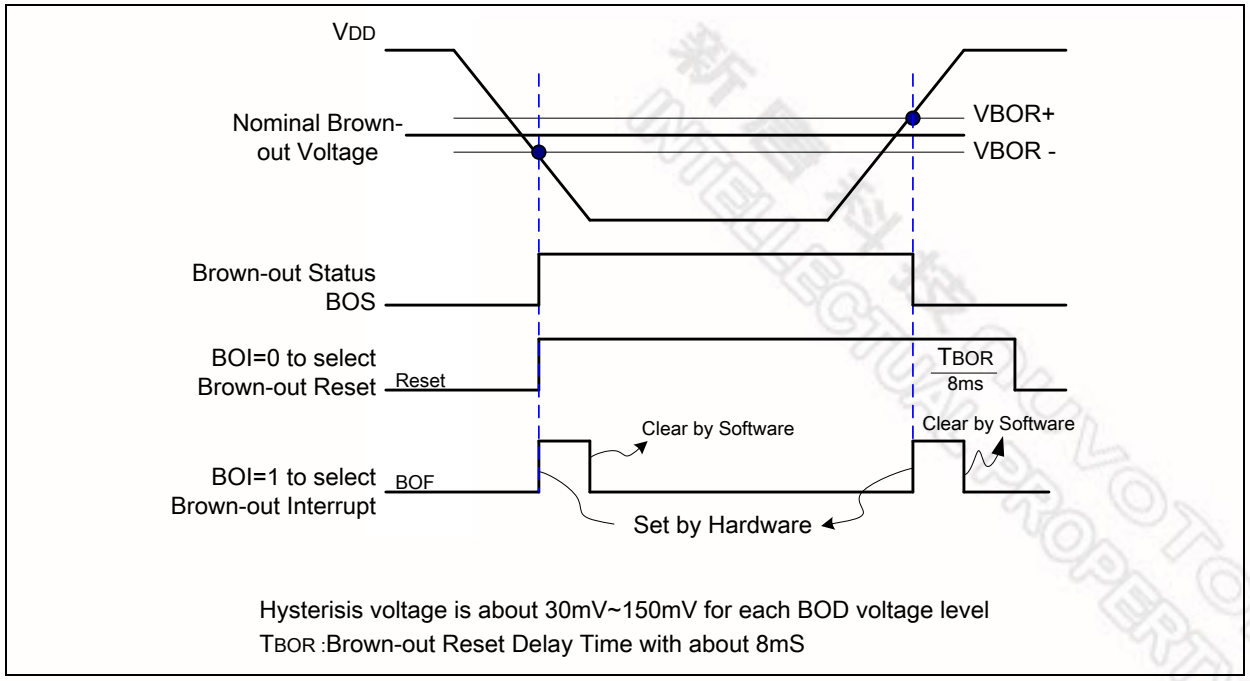


Figure 22-2: Brown-out Voltage Detection

Hysterisis range of brownout detect voltage is about 30mV to 150mV

23 ICP (IN-CIRCUIT PROGRAM) FLASH MODE

The ICP(In-Circuit-Program) mode is another approach to access the Flash EPROM. There are only 3 pins needed to perform the ICP function. One is mode input, shared with RST pin, which must be kept in Vdd voltage in the entire ICP working period. One is clock input, shared with P1.7, which accepts serial clock from external device. Another is data I/O pin, shared with P1.6, that an external ICP program tool shifts in/out data via P1.6 synchronized with clock(P1.7) to access the Flash EPROM of W79E4051/2051. User may refer to http://www.manley.com.cn/english/index.asp for ICP Program Tool.

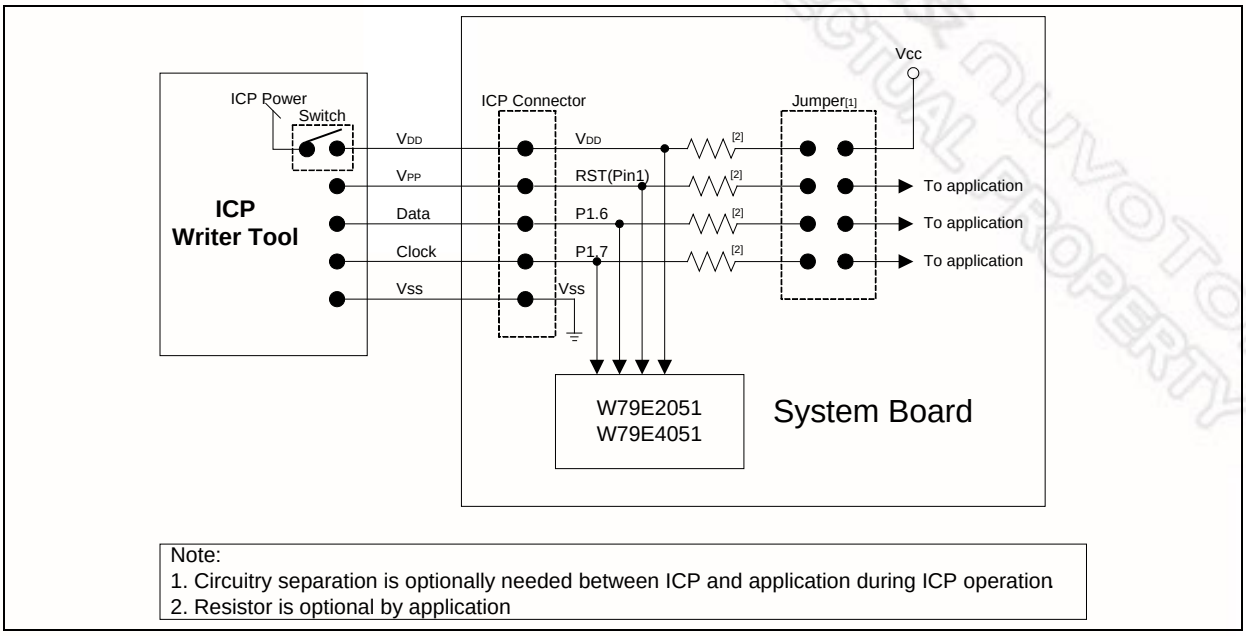


Figure 23-1: ICP Writer Tool connector pin assign

Note: 1. When using ICP to upgrade code, the RST, P1.6 and P1.7 must be taken within design system board.

2. After program finished by ICP, to suggest system power must power off and remove ICP connector then power on.

3. It is recommended that user performs erase function and programming configure bits continuously without any interruption.

24 CONFIG BITS

The W79E4051/2051 has two CONFIG bits (CONFIG0 located at FB00h, CONFIG1 located at FB01h) that must be defined at power up and can not be set by the program after start of execution. Those features are configured through the use of two flash EPROM bytes, and the flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of flash EPROM (CONFIG1) and those operations on it are described below.

24.1 CONFIG0

Config0

WDTCK	CBOV1	CBOV0	0	-	BPFR	Fosc1	Fosc0

Figure 24-1: Config0 register bits

Bit	Name	Function
7	WDTCK	Clock source of Watchdog Timer select bit: 0: The internal 500KHz RC oscillator clock is for Watchdog Timer clock used. 1: The uC clock is for Watchdog Timer clock used.
6~5	CBOV1 CBOV0	Brownout voltage selection bits: SFR bits (BOV1,BOV0) are initialized at reset with the inversed value of config0-bits (CBOV1,CBOV0)
2	BPFR	Bypass Clock Filter. 0: Disable Clock Filter. 1: Enable Clock Filter.
1	Fosc1	CPU Oscillator Type Select bit 1.
0	Fosc0	CPU Oscillator Type Select bit 0.

CBOV.1	**CBOV.0**	**Brownout Voltage**
1	1	Brownout voltage is 2.4V
1	0	Brownout voltage is 2.7V
0	1	Brownout voltage is 3.8V
0	0	Brownout voltage is 4.5V

Oscillator Configuration bits:

Fosc1	Fosc0	OSC source
0	0	4MHz ~ 24MHz crystal
0	1	Internal RC Oscillator (FS1 bit in CONFIG1.5 will determine either 11MHz or 22MHZ) XT1 and XT2 function as P2.1 and P2.0
1	0	Reserved
1	1	External Oscillator in XTAL1; XT2 is in Tri-state

24.2 CONFIG1

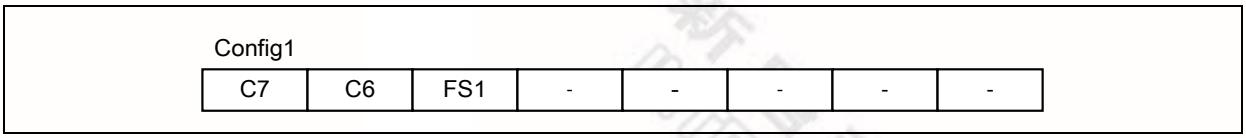


Figure 24-2: Config1 register bits

Bit	Name	Function
7	C7	4K/2K Program Flash EPROM Lock bit This bit is used to protect the customer's program code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and CONFIG Registers can not be accessed again.
6	C6	128 byte Data Flash EPROM Lock bit This bit is used to protect the customer's 128 bytes of data code. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the 128 bytes of Flash EPROM data and CONFIG Registers can not be accessed again.
5	FS1	Internal Oscillator 11MHz/22MHz selection bit This bit is used to select 11MHz or 22MHz internal oscillator. 1: Internal oscillator is set to 22MHz 0: Internal oscillator is set to 11MHz
0~4	-	Reserved.

Lock bits C7 and C6:

Bit 7	Bit 6	Function Description
1	1	Both security of **4K/2KB** program code and **128** Bytes data area are not locked. They can be erased, programmed or read by Writer or ICP.
0	1	The **4K/2KB** program code area is locked. It can not be read and written by Writer or ICP. The **128** Bytes data area can be program one time or read.
1	0	Not supported.
0	0	Both security of **4K/2KB** program code and **128** Bytes data area are locked. They can not be read and written by Writer or ICP.

25 ELECTRICAL CHARACTERISTICS

25.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITION	MINIMUM	MAXIMUM	UNIT
DC Power Supply	V_{DD}	V_{DD}–V_{SS}	-0.3	+7.0	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	TA		-40	+85	°C
Storage Temperature	Tst		-55	+150	°C
Sink current	ISK		-	95	mA
RAM Keep Alive Voltage	V_{RAM}		1.4	+7.0	V
Maximum Current into V_{DD}		-		120	mA
Maximum Current out of V_{SS}				120	mA
Maximum Current suck by a I/O pin				25	mA
Maximum Current sourced by a I/O pin				25	mA
Maximum Current suck by total I/O pins				80	mA
Maximum Current sourced by total I/O pins				80	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability

25.2 DC ELECTRICAL CHARACTERISTICS

(VSS = 0V, TA =-40~85° C, unless otherwise specified; Typical value is test at TA=25° C)

PARAMETER	SYM.	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Operating Voltage	V_{DD}	2.4		5.5	V	V_{DD}=2.4V ~ 5.5V @ 12MHz V_{DD}=4.5V ~ 5.5V @ 24MHz
		3.0		5.5		Program and erase Data Flash.
Operating Current	I_{DD1}		2	3.5	mA	No load, RST = V_{DD}, V_{DD}= 3.0V @ 12MHz
	I_{DD2}		8	12	mA	No load, RST = V_{DD}, V_{DD}= 5.0V @ 24MHz
Idle Current	I_{IDLE1}		1.6	2.5	mA	No load, V_{DD} = 3.0V @ 12MHz
	I_{IDLE2}		6.5	7.5	mA	No load, V_{DD} = 5.0V @ 24MHz
Power Down Current	I_{PWDN1}		0.5	10	µA	No load, V_{DD} = 5.0/3.0V (Brownout detection is disabled)
INPUT / OUTPUT						
Input Current P1, P2, P3	I_{IN1}	-50	-	+10	µA	V_{DD} = 5.5V, V_{IN} = 0V or V_{IN}=V_{DD}
Input Current RST pin[1]	I_{IN2}	-55	-	-30	µA	V_{DD} = 5.5V, V_{IN} = 0.45V
Input Leakage Current P1.0, P1.1(Open Drain)	I_{LK}	-1	-	+1	µA	V_{DD} = 5.5V, 0<V_{IN}<V_{DD}
Logic 1 to 0 Transition Current P1, P2, P3	I_{TL} [*3]	-450	-	-200	µA	V_{DD} = 5.5V, V_{IN}<2.0V
		-93	-	-56		V_{DD} =2.4 Vin = 1.3v
Input Low Voltage P1, P2, P3 (TTL input)	V_{IL1}	0	-	1.0	V	V_{DD} = 4.5V
		0	-	0.6		V_{DD} = 2.4V
Input High Voltage P1, P2, P3 (TTL input)	V_{IH1}	2.0	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		1.5	-	V_{DD} +0.2		V_{DD} = 2.4V
Input Low Voltage XTAL1[*2]	V_{IL3}	0	-	0.8	V	V_{DD} = 4.5V
		0	-	0.4		V_{DD} = 3.0V
Input High Voltage XTAL1[*2]	V_{IH3}	3.5	-	V_{DD} +0.2	V	V_{DD} = 5.5V
		2.4	-	V_{DD} +0.2		V_{DD} = 3.0V
Negative going threshold (RST Schmitt input)	V_{ILS}	-0.5	-	0.3V_{DD}	V	
Positive going threshold (RST Schmitt input)	V_{IHS}	0.7V_{DD}	-	V_{DD}+0.5	V	
Hysteresis voltage (RST Schmitt input)	V_{HY}		0.2V_{DD}		V	
Source Current P1, P2, P3 (Quasi-bidirectional Mode)	I_{SR1}	-150	-210	-360	µA	V_{DD} = 4.5V, V_S = 2.4V
		-18	-27	-40	µA	V_{DD} = 2.4V, V_S = 2.0V

Sink Current P1, P2, P3 (Quasi-bidirectional Mode)	I_{SK1}	13	20	24	mA	V_{DD} = 4.5V, V_S = 0.45V
		8	13	17	mA	V_{DD} = 2.4V, V_S = 0.45V
Brownout voltage with BOV[1:0]=00	$V_{BO2.4}$	2.25	2.4	2.55	V	
Brownout voltage with BOV[1:0]=01	$V_{BO2.7}$	2.55	2.7	2.75	V	
Brownout voltage with BOV[1:0]=10	$V_{BO3.8}$	3.65	3.8	3.90	V	
Brownout voltage with BOV[1:0]=11	$V_{BO4.5}$	4.30	4.5	4.65	V	
Brownout detection current	I_{BO1}		160/135	210/170	μA	No load, V_{DD} = 5.0/3.0V Average current at Brownout detection active (LPBOV=0)
	I_{BO2}		24/11	32/15	μA	No load, V_{DD} = 5.0/3.0V Average current at Brownout detection active (LPBOV=1, 1/16 mode)
Hysterisis range of BOD voltage	V_{Bh}	35	-	150	mV	V_{DD} = 2.4V~5.5V, (LPBOD,BOI) = (0,x) or (1,0)
		10	-	60	mV	V_{DD} = 2.4V~5.5V, (LPBOD,BOI)=(1,1)
Power On Reset Voltage	V_{POR}	1.45	2.0	2.10	V	With Hysterisis ~= 450mV

Notes: *1. RST pin is a Schmitt trigger input.

*2. XTAL1 is a CMOS input.

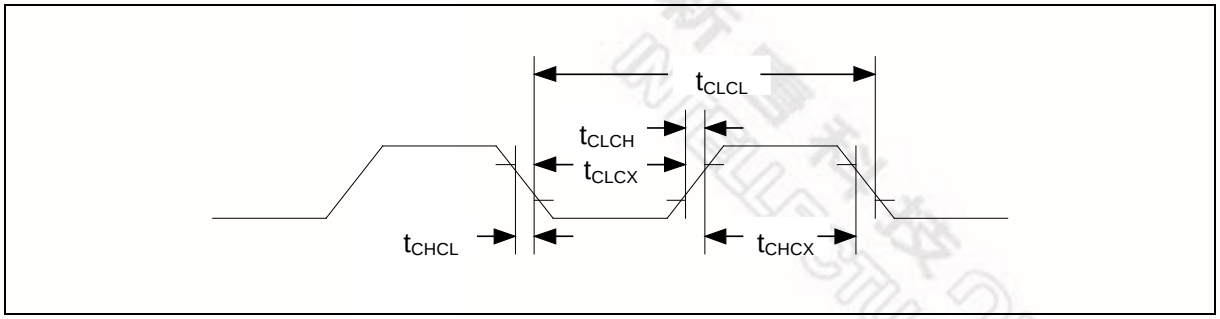
*3. Pins of P1, P2 and P3 can source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when Vin approximates to 2V.

25.3 The COMPARATOR ELECTRICAL CHARACTERISTICS

(VDD–VSS = 3.0~5V±10%, TA = -40~85°C, Fosc = 24MHz, unless otherwise specified.)

PARAMETER	SYMBOL	SPECIFICATION				TEST CONDITIONS
		MIN.	TYP.	MAX.	UNIT	
Common mode range comparator inputs	V_{CR}	0		V_{DD}-0.3	V	
Common mode rejection ratio	CMRR			-50	dB	
Response time	t_{RS}	-	50	100	ns	
Comparator enable to output valid time	t_{EN}	-	1	5	us	
Input leakage current, comparator	I_{IL}	-10	0	10	uA	0< V_{IN} <V_{DD}
Comparator offset voltage	V_{OFF}			20	mV	With decoupled capacitors on inputs

25.4 AC ELECTRICAL CHARACTERISTICS



Note: Duty cycle is 50%.

25.5 EXTERNAL CLOCK CHARACTERISTICS

PARAMETER	SYMBOL	VARIABLE CLOCK MIN.	VARIABLE CLOCK MAX.	UNITS
Oscillator Frequency	$1/t_{CLCL}$	0	24	MHz

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	NOTES
Clock High Time	t_{CHCX}	18.8	-	-	nS	
Clock Low Time	t_{CLCX}	18.8	-	-	nS	
Clock Rise Time	t_{CLCH}	-	-	10	nS	
Clock Fall Time	t_{CHCL}	-	-	10	nS	

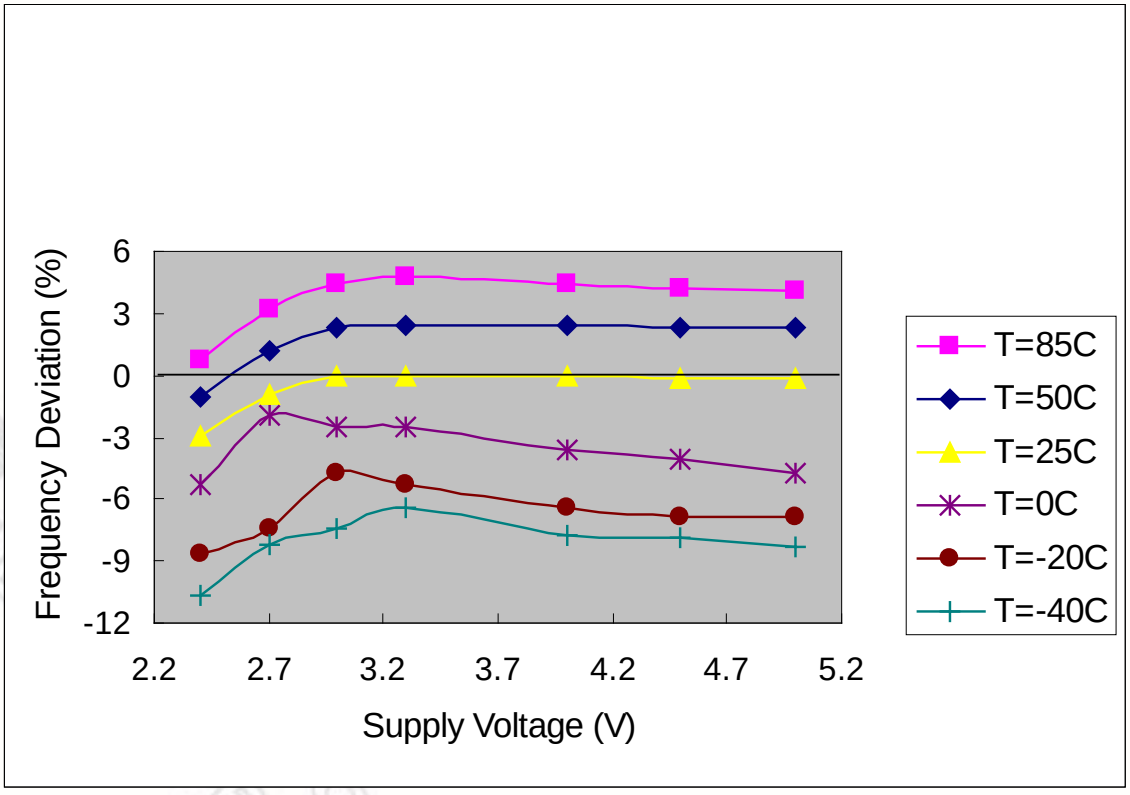
25.6 RC OSC AND AC CHARACTERISTICS

(VDD–VSS = 2.4~5V, TA = -40~85°C.)

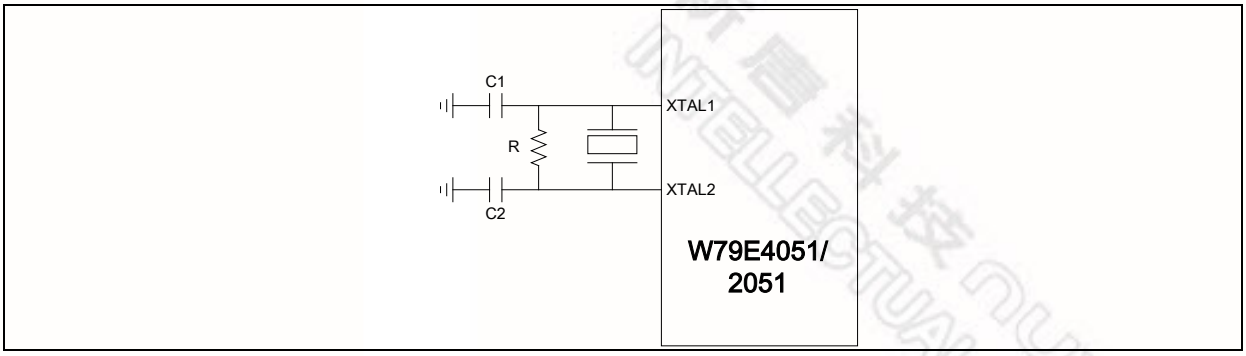
Parameter	Specification (reference)				Test Conditions
	Min.	Typ.	Max.	Unit	
W79E2051/W79E4051 Frequency accuracy of On-chip RC oscillator (Without calibration)	-25		25	%	V_{DD}=2.4V~5.5V, TA = -40°C ~85°C
W79E2051R/W79E4051R On-chip RC oscillator with calibration[1,2] (Fosc = 22.1184MHz with factory calibration)	-2		2	%	V_{DD}=5.0V, TA = 25°C
	-5		5	%	V_{DD}=2.7V~5.5V, TA = 0~85°C
	-7		7	%	V_{DD}=2.7V~5.5V, TA = -20~85°C
	-9		7	%	V_{DD}=2.7V~5.5V, TA = -40~85°C
Wakeup time		256		clk	

Note:

1. These values are for design guidance only and are not tested.
2. RC frequency deviation vs. V_{DD} and Temperature is shown below



26 TYPICAL APPLICATION CIRCUITS

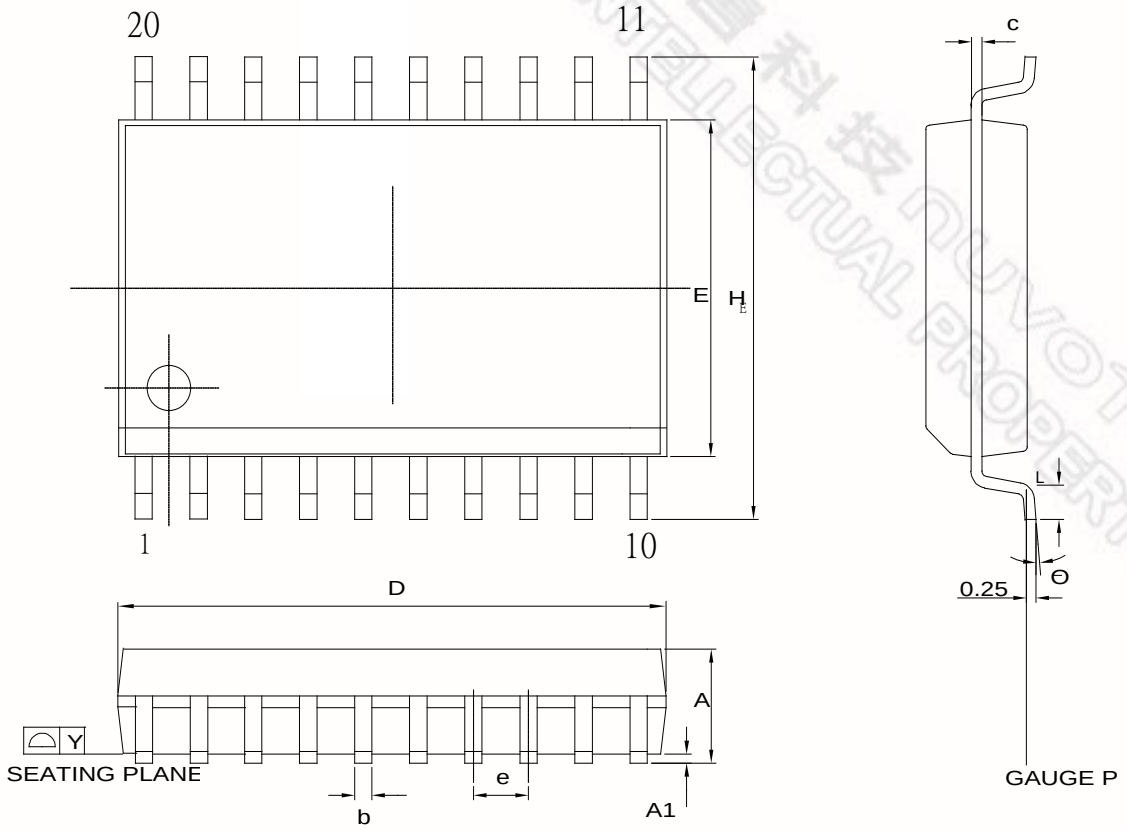


The table below shows the reference values for crystal applications.

CRYSTAL	C1	C2	R
4MHz ~ 24 MHz	without	without	without

27 PACKAGE DIMENSIONS

27.1 20-pin SOP

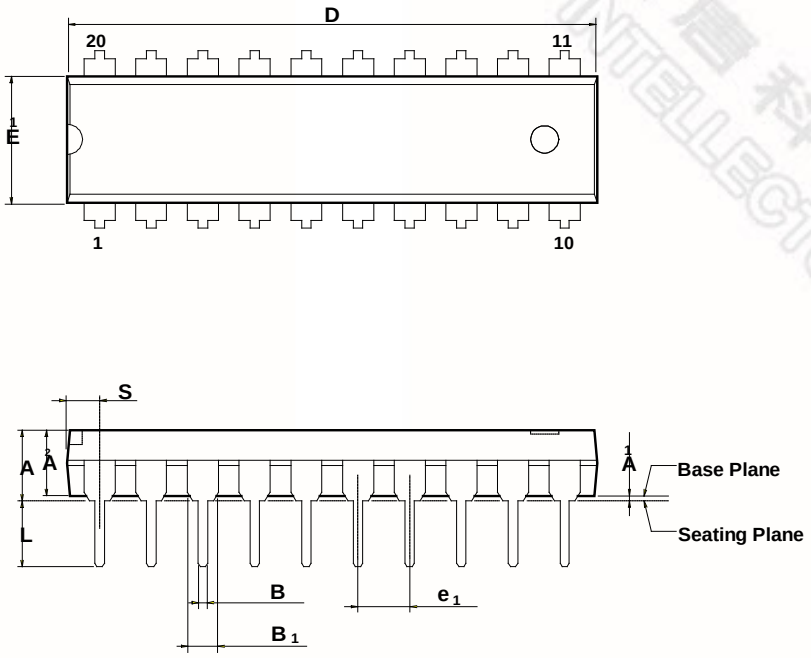


Control demensions are in milmeters .

SYMBOL	DIMENSION IN MM		DIMENSION IN INCH	
	MIN.	MAX.	MIN.	MAX.
A	2.35	2.65	0.093	0.104
A1	0.10	0.30	0.004	0.012
b	0.33	0.51	0.013	0.020
c	0.23	0.32	0.009	0.013
E	7.40	7.60	0.291	0.299
D	12.60	13.00	0.496	0.512
e	1.27 BSC		0.050 BSC	
H_E	10.00	10.65	0.394	0.419
Y	—	0.10	—	0.004
L	0.40	1.27	0.016	0.050
θ	0	8	0	8

Figure 27-1: 20L SOP-300mil

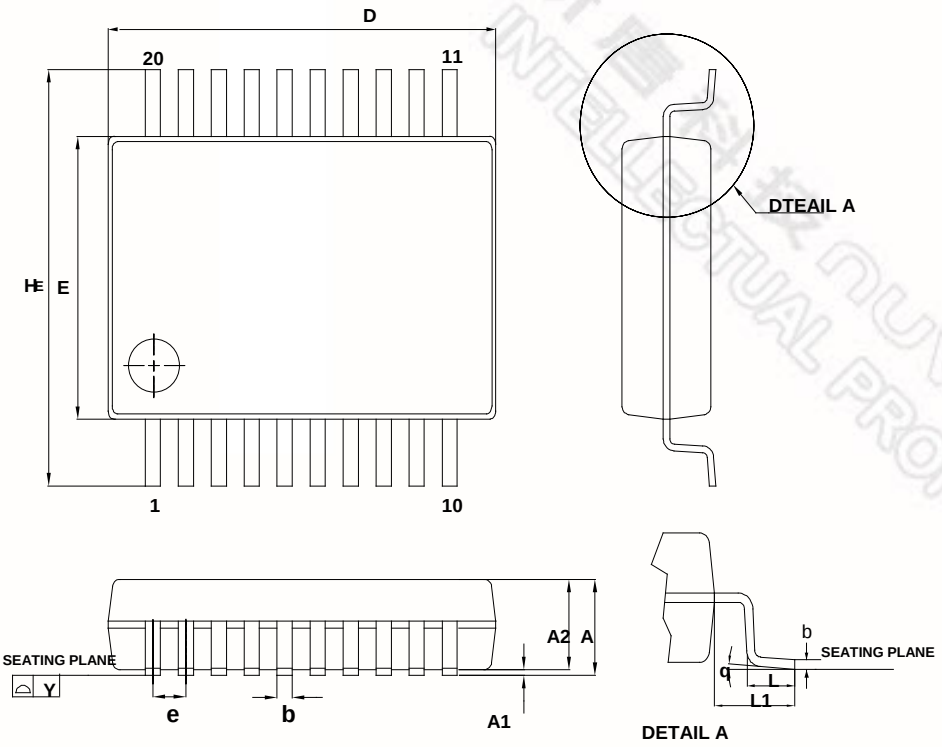
27.2 20-pin DIP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.175	—	—	4.45
A_1	0.010	—	—	0.25	—	—
A_2	0.125	0.130	0.135	3.18	3.30	3.43
B	0.016	0.018	0.022	0.41	0.46	0.56
B_1	0.058	0.060	0.064	1.47	1.52	1.63
c	0.008	0.010	0.014	0.20	0.25	0.36
D	—	1.026	1.040	—	20.06	26.42
E	0.290	0.300	0.310	7.37	7.62	7.87
E_1	0.245	0.250	0.255	6.22	6.35	6.48
e_1	0.090	0.100	0.110	2.29	2.54	2.79
L	0.120	0.130	0.140	3.05	3.30	3.56
α	0	—	15	0	—	15
e_A	0.335	0.355	0.375	8.51	9.02	9.53
S	—	—	0.075	—	—	1.91

Figure 27-2: 20L DIP-300mil

27.3 20-pin SSOP



SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A	—	—	2.00	—	—	0.079
A1	0.05	—	—	0.002	—	—
A2	1.65	1.75	1.85	0.065	0.069	0.073
b	0.22	—	0.38	0.009	—	0.015
c	0.09	—	0.25	0.004	—	0.010
D	6.90	7.20	7.50	0.272	0.283	0.295
E	5.00	5.30	5.60	0.197	0.209	0.220
HE	7.40	7.80	8.20	0.291	0.307	0.323
e	—	0.65	—	—	0.0256	—
L	0.55	0.75	0.95	0.021	0.030	0.037
L1	—	1.25	—	—	0.050	—
Y	—	—	0.10	—	—	0.004
q	0	—	8	0	—	8

Figure 27-3: 20-Pin SSOP

28 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	July 9, 2008	-	Initial Issued
A02	August 4, 2008	78 86 85	1. Add a notice for the untrimmed internal RC OSC. 2. Modify the test condition of “Hysterisis range of BOD voltage” in DC spec. 3. Modify the Max value of power down current.
A03	August 29, 2008	86 91	1. Revised Maximum Current suck by total I/O pins from 75mA to 80mA. 2. Modify “24.6 RC OSC AND AC CHARACTERISTICS”
A04	December 22, 2008	25 88 83	1. Revise the description of SFR bit LPBOV 2. Correct I_{BO2} 3215 with 32/15. 3. Add Chapter 23 ICP
A05	February 25, 2009	5, 84	1. Add DC spec of Data Flash program/erase voltage
A06	April 16, 2009	5,6,7 94	1. Add SSOP20 parts of W79E4051ARG/RARG and W79E2051ARG/RARG. 2. Add SSOP-20 package dimension diagram.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View W79E2051AKG on WIN SOURCE
- Nuvoton Technology Corporation of America Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management