THE DATASHEET OF

TMP816PWR

TMP816 Variable-Speed Single-Phase Full-Wave Fan-Motor Predriver

1 Features

- Predriver for Single-Phase Full-Wave Drive
  - PNP-NMOS is used as an external power TR, enabling high-efficiency low-consumption drive by means of the low-saturation output and single-phase full-wave drive. (PMOS-NMOS also applicable)
- External PWM Input Enables Variable-Speed Control
  - Separately-excited upper direct PWM (f = 25 kHz) control method, enabling highly silent speed control
- Current Limiter Circuit
  - Chopper-type current limit at start
- Reactive Current-Cut Circuit
  - Reactive current before phase change is cut to enable silent and low-consumption drive
- Minimum Speed Setting Pin
  - Minimum speed can be set with external resistor. The start assistance circuit enables start at extremely low speed.
- Constant-Voltage Output Pin for Hall Bias
- Lock Protection and Automatic Reset Functions
- Rotation Speed Detection (FG) and Lock Detection (RD) Outputs

2 Applications

- Server Fans
- Appliance Fans

3 Description

The TMP816 is a single-phase bipolar variable-speed fan-motor predriver that works with an external PWM signal. A highly efficient, quiet, and low-power consumption motor driver circuit with a large variable speed can be implemented by adding a small number of external components.

The TMP816 device is optimal for driving large-scale fan motors (with large air volume and large current) such as those used in servers and consumer products.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TMP816	TSSOP (PW)	4.40 mm × 6.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

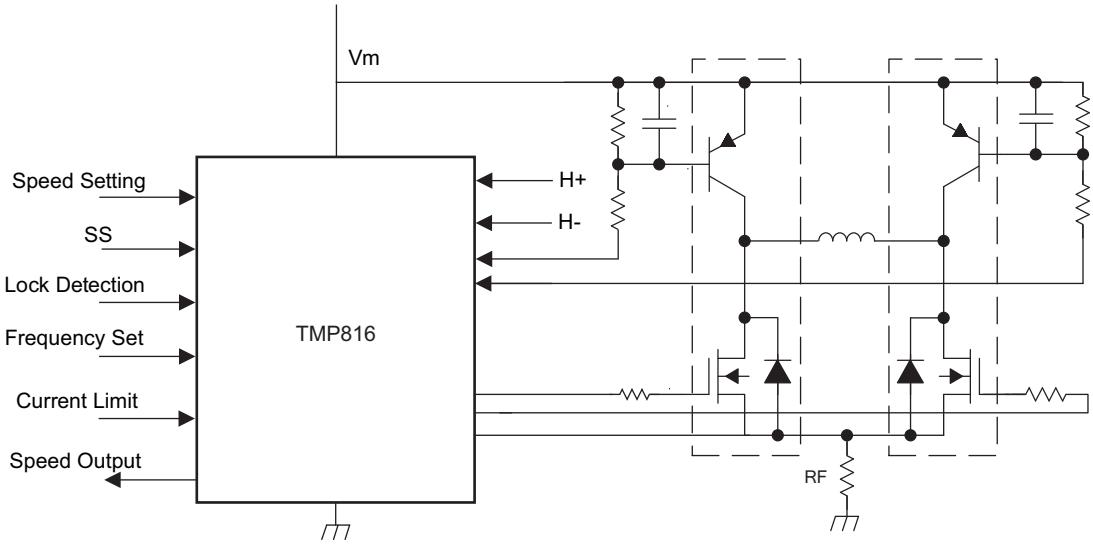


Table of Contents

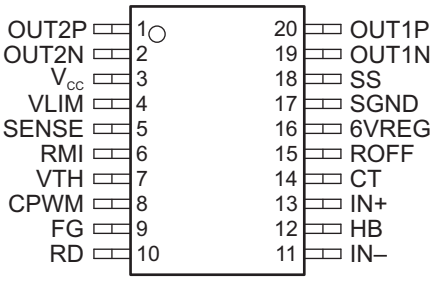
4 Revision History

Changes from Original (May 2009) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

5 Pin Configuration and Functions

PW Package
20-Pin TSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT2P	1	O	Upper-side driver output
OUT2N	2	O	Lower-side driver output
VCC	3		Power supply. For the CM capacitor that is a power stabilization capacitor for PWM drive and for absorption of kickback, the capacitance of 0.1 µF to 1 µF is used. In this device, the lower TR performs current regeneration by switching the upper TR. Connect CM between V_{CC} and GND, with the thick pattern and along the shortest route. Use a Zener diode if kickback causes excessive increase of the supply voltage, because such increase may damage the device.
VLIM	4	I	Activates the current limiter when SENSE voltage is higher than VLIM voltage. Connect to 6VREG when not used.
SENSE	5	I	Sense input. Connect to GND when not used.
RMI	6	I	Minimum speed setting. Connect to 6VREG when not used. If device power can be removed before power is removed from RMI, insert a current limiting resistor to prevent inflow of large current.
VTH	7	I	VTH voltage is generated by filtering the PWM-IN input. If device power can be removed before power is removed from VTH, insert a current limiting resistor to prevent inflow of large current.
CPWM	8	O	Connect to capacitor CP to set the PWM oscillation frequency. With CP = 100 pF, oscillation occurs at 25 kHz and provides the basic frequency of PWM.
FG	9	O	Open collector output, which can detect the rotation speed using the FG output according to the phase shift. Leave open when not used.
RD	10	O	Open collector output. Outputs low during rotation and high at stop. Leave open when not used.
IN–	11	I	Hall input
HB	12	O	This is a Hall element bias, that is, the 1.5-V constant-voltage output.
IN+	13	I	Hall input. Make connecting traces as short as possible to prevent carrying of noise. To futher limit noise, insert a capacitor between IN+ and IN–. The Hall input circuit is a comparator having a hysteresis of 20 mV. The application should ensure that the Hall input level more than three times (60 mVp-p) this hysteresis.
CT	14	O	Lock detection time setting. Capacitor CT is connected.
ROFF	15	I	Sets the soft switching time to cut the reactive current before phase change. Connect to 6VREG when not used.
6VREG	16	O	6-V regulator output
SGND	17		Connected to the control circuit power supply system.
SS	18	O	Connect to soft-start setting capacitor. Connect the capacitor between 6VREG and SS. Enables setting of the soft-start time according to the capacity of the capacitor (see Figure 3 and Figure 4). Connect to ground if not used.
OUT1N	19	O	Lower-side driver output
OUT1P	20	O	Upper-side driver output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage			18	V
V_{OUT}	Output voltage	OUT1P, OUT1N, OUT2P, OUT2N		18	
I_{OUT}	Continuous output current	OUT1P, OUT1N, OUT2P, OUT2N		50	mA
I_{HB}	Continuous output current	HB		10	
V_{TH}	Input voltage	VTH		8	
V_{RD} V_{FG}	Output voltage	RD, FG		18	V
I_{RD} I_{FG}	Continuous output current	RD, FG		10	mA
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

T_A = 25°C

			MIN	MAX	UNIT
V_{CC}	Supply voltage		6	16	V
V_{TH}	VTH input voltage	Full-speed mode	0	7	V
V_{ICM}	Hall input common phase input voltage		0.2	3	V
T_A	Operating free-air temperature		–30	95	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMP816 PW (TSSOP) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	90.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	42.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	24.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	0.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	51.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{CC} = 12 V, T_A = 25°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{6VREG}	Output voltage	6VREG	I_{HB} = 5 mA	5.8	6	6.15	V
V_{CRH}	High-level output voltage	CPWM		4.35	4.55	4.75	V
V_{CRL}	Low-level output voltage			1.45	1.65	1.85	V
f_{PWM}	Oscillation frequency		CP = 100 pF	18	25	32	kHz
V_{CTH}	High-level output voltage	CT		3.4	3.6	3.8	V
V_{CTL}	Low-level output voltage			1.4	1.6	1.8	V
I_{CT1}	Charge current			1.6	2	2.5	µA
I_{CT2}	Discharge current			0.16	0.2	0.28	µA
R_{CT}	Charge/discharge current ratio			8	10	12	
V_{ON}	Output voltage	OUT_N	I_O = 20 mA	4	10		V
I_{OP}	Sink current	OUT_P		15	20		mA
V_{HN}	Hall input sensitivity	H+, H-	Zero peak value (including offset and hysteresis)		10	20	mV
V_{RD} V_{FG}	Low-level output voltage	RD, FG	I_{RD} = 5 mA or I_{FG} = 5 mA		0.15	0.3	V
I_{RDL} I_{FGL}	Output leakage current		V_{RD} = 16 V or V_{FG} = 16 V			30	µA
I_{SS}	Discharge current	SS	V_{SS} = 1 V	0.4	0.5	0.6	µA
I_{CC}	Supply current		During drive	4	10	14	mA
			During lock protection	4	10	14	

6.6 Typical Characteristics

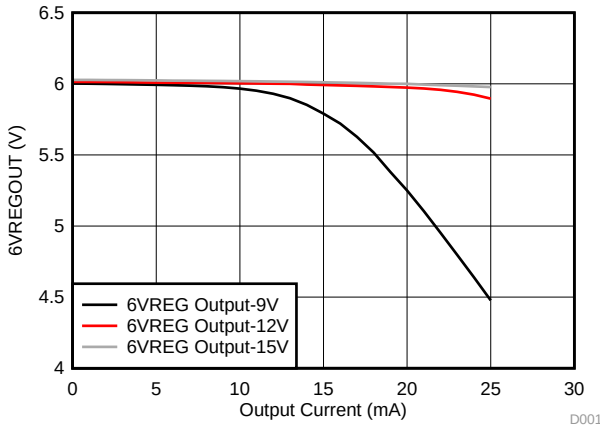


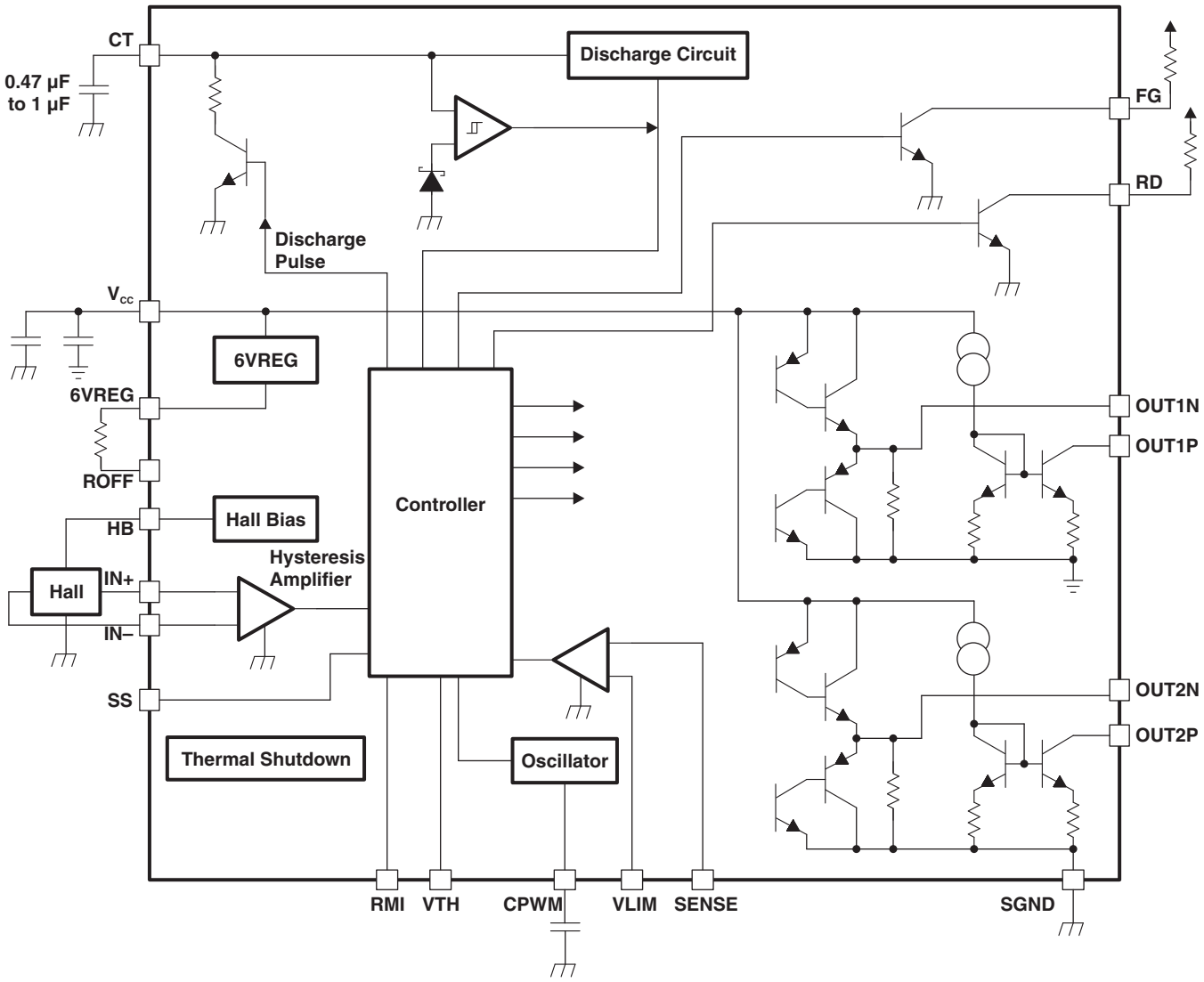
Figure 1. 6VREGOUT Load Regulation

7 Detailed Description

7.1 Overview

The TMP816 device is a single phase bipolar predriver which uses the hall sensor & speed control inputs for driving the single phase motor connected through H Bridge. The predriver outputs are designed for driving top side P-type devices and bottom side N-channel FETs in the bridge. Multiple protections like overcurrent, soft-start, speed control, lock detect, speed feedback and minimum speed are incorporated in the device.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Speed Control

The speed control functionality is obtained by VTH pin of the device. For pulsed inputs user can supply a 20-kHz to 100-kHz frequency input (20 kHz to 50 kHz recommended on the pin with a current limiting resistor in between. If not used, this pin needs to be connected to ground for full speed.)

Feature Description (continued)

7.3.2 Soft-Start

Soft-Start Time can be adjusted using the S-S pin. Connect this capacitor between 6VREG and S-S Pin. Connected to GND if not used.

7.3.3 Lock Detection

When the rotor is locked by external means or load conditions, The Lock detection feature helps to protect the circuit by not allowing the current to rise beyond control. A hiccup mechanism is also provided. The Lock detection is enabled by a connection to the lock detection capacitor. The constant current charge and discharge circuits cause drive stop when the pin voltage rises to 3.8V and enabling it back when voltage reached to 1.8V.

If lock detection feature is not desired in the application, this pin needs to be connected to ground.

7.3.4 Current Limit

Current limit resistor is connected in a return path of H Bridge connection. This input is connected to the SENSE pin where the Current is limited when the voltage across this resistor crosses the voltage at VLIM Pin.

If not used, this pin needs to be connected to ground.

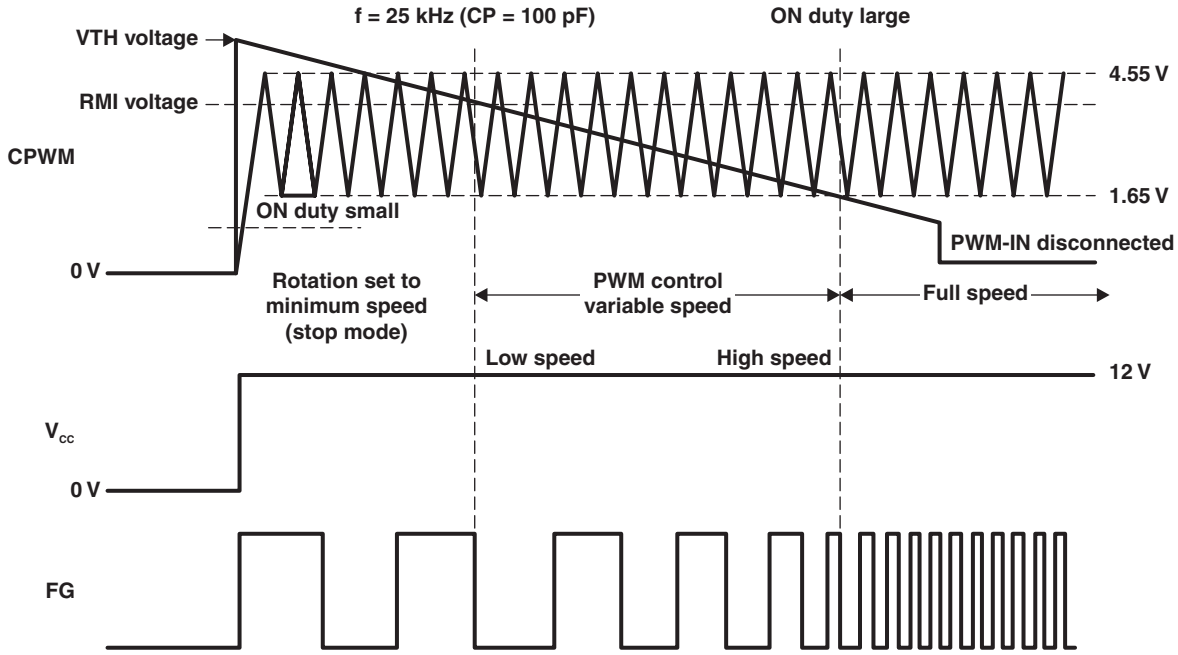
7.3.5 Speed Output

The speed of the motor while running can be observed at the FG pin which is an open collector output and needs to be pulled high for using it.

7.3.6 Drive Frequency Selection

The P-channel switches in the device are switched with higher frequency whose duty cycle is decided by the speed control input. The frequency of the operation can be decided by the capacitor connected at the CPWM pin.

Feature Description (continued)



A. Minimum speed setting (stop) mode

PWM-IN input is filtered to generate the VTH voltage. At low speed, the fan rotates with the minimum speed set with RMI during low speed. If the minimum speed is not set (RMI = 6VREG), the fan stops.

B. Low ↔ high-speed mode

PWM control is made through comparison of oscillation and VTH voltages with CPWM changing between 1.6 V ↔ 4.6 V.

Upper and lower TRs are turned ON when the VTH voltage is higher. The upper output TR is turned OFF when the VTH voltage is lower, and the coil current is regenerated in the lower TR. Therefore, as the VTH voltage lowers, the output ON duty increases, increasing the coil current and raising the motor speed. The rotation speed is fed back by the FG output.

C. Full speed mode

The full-speed mode becomes effective with the VTH voltage of 1.65 V or less. (VTH must be equal to GND when the speed control is not used.)

D. PWM-IN input disconnection mode

When the PWM-IN input pin is disconnected, VTH becomes 1.65 V or less and the output enables full drive at 100%. The fan runs at full speed (see Figure 5).

Figure 2. Control Timing

Feature Description (continued)

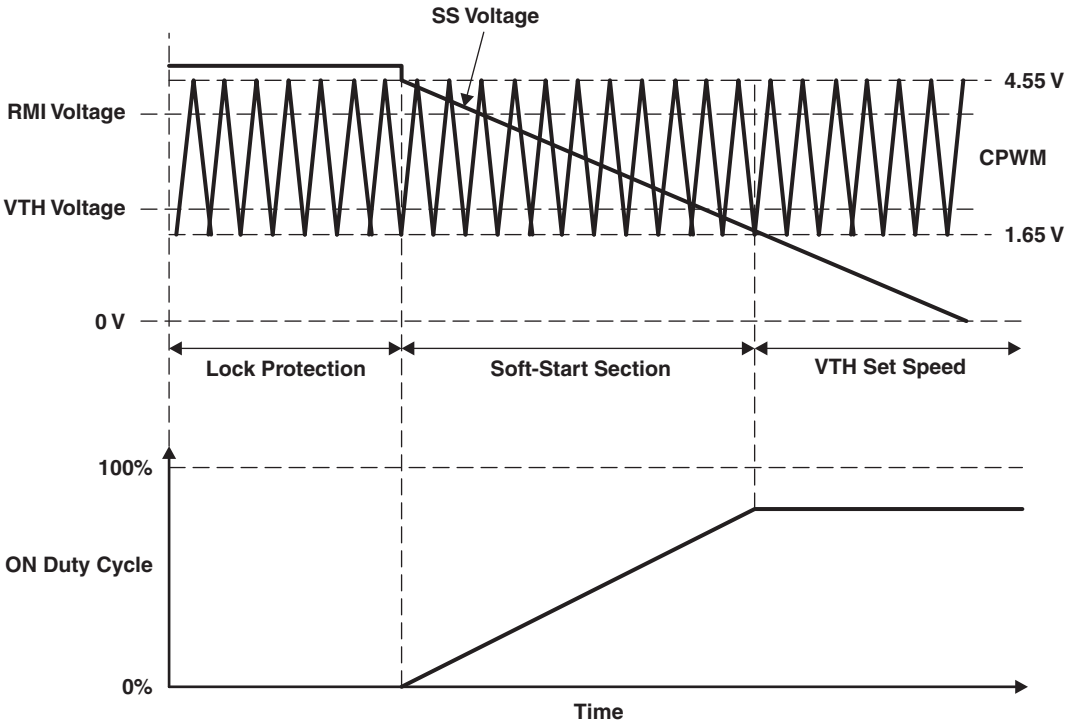


Figure 3. Soft-Start Control Timing (VTH < RMI Voltage)

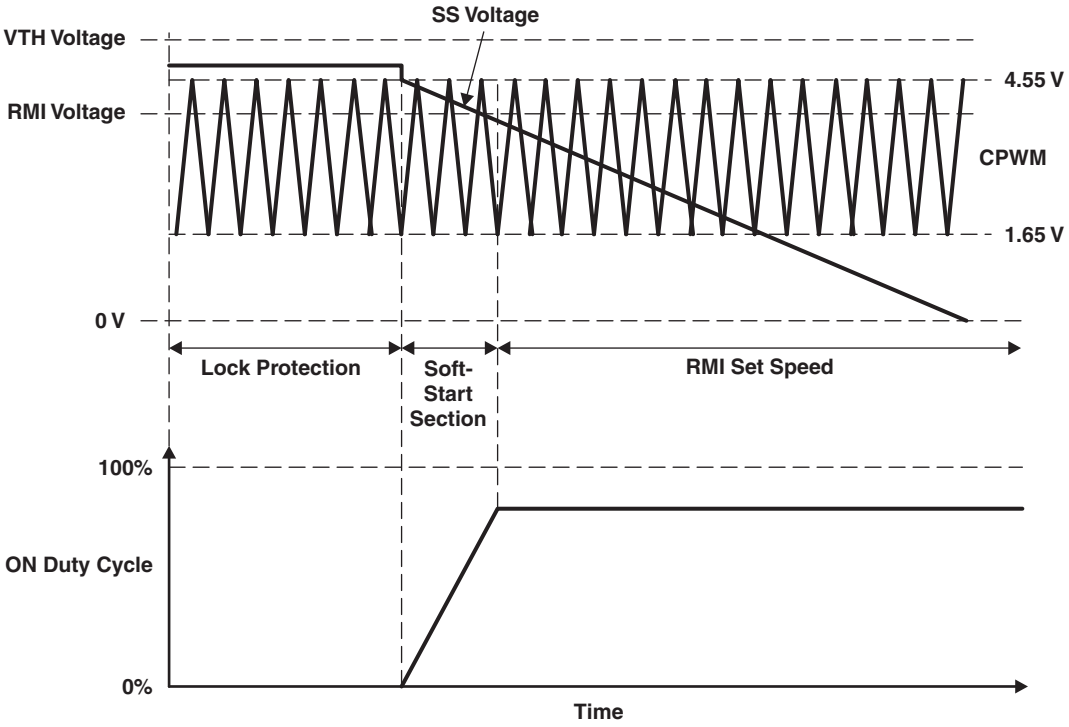


Figure 4. Soft-Start Control Timing (VTH > RMI Voltage)

7.4 Device Functional Modes

Table 1. Truth Table

IN–	IN+	CT	OUT1P	OUT1N	OUT2P	OUT2N	FG	RD	MODE
H	L	L	L	–	–	H	L	L	OUT1 → 2 drive
L	H		–	H	L	–	OFF		OUT2 → 1 drive
H	L	H	OFF	–	–	H	L	OFF	Lock protection
L	H		–	H	OFF	–	OFF		

VTH	CPWM	IN–	IN+	OUT1P	OUT1N	OUT2P	OUT2N	MODE
L	H	H	L	L	–	–	H	OUT1 → 2 Drive
		L	H	–	H	L	–	OUT2 → 1 Drive
H	L	H	L	OFF	–	–	H	During rotation, regeneration in lower TR
		L	H	–	H	OFF	–	

8 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TMP816 device needs few external components for the features described in *Feature Description*. The device needs a 1-µF or more capacitor connected at VCC. The device generates 6-V regulated output, which can be used for pullups in the circuit as well as the Hall sensor.

8.2 Typical Application

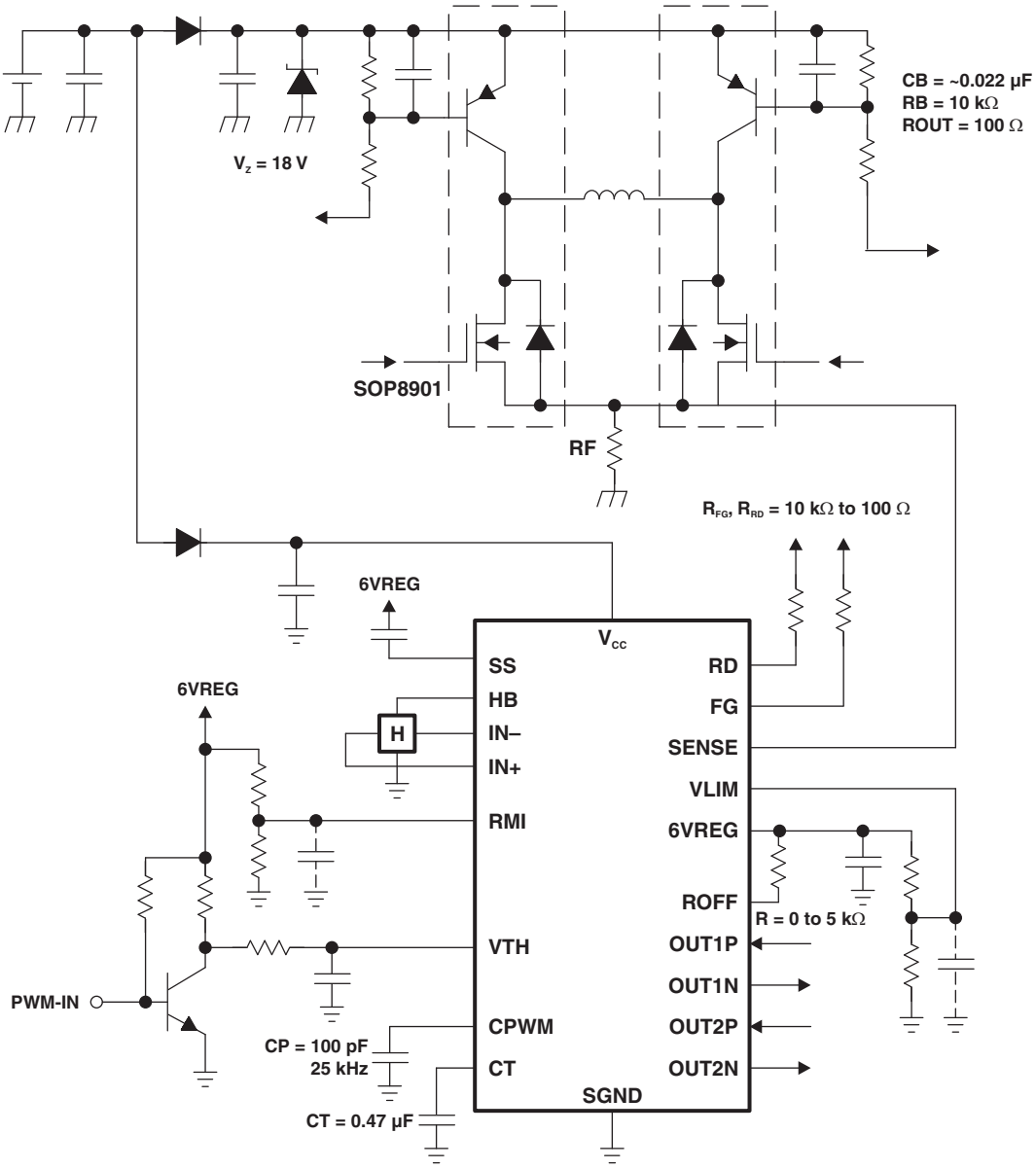


Figure 5. 12-V Sample Application Circuit

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the following parameters:

- Input Voltage: 6 to 16 V
- VCC capacitor: 1 µF or more
- H Bridge Top side: P-channel FETs or PNP transistors
- Bottom side: N-channel FETs

8.2.2 Detailed Design Procedure

Pins:

- CPWM Capacitor: 100 pF for 25-kHz switching or appropriate.
- VTH Pin connected to Ground for full-speed or supplied with pulsed input.
- RMI Pin Pulled high to 6VREG output or external connection if required.
- ROFF pulled to 6VREG.
- 6VREG connected to Hall Sensor. Hall sensor differential inputs connected to IN+ and IN-.
- SENSE pin or GND.
- CT connected to Lock Detection capacitor (0.47 µF or calculated values) or to GND.
- Drive outputs connected to the Gates of the H bridge switches.
- Pullup on FG.

Power Supply:

- Make sure the power supply has set with sufficient current limit at the decided at the motor voltage.

Build the circuit with previously recommended connections at the pins.

Test the motor circuit with hardware connected to it.

8.2.3 Application Curves

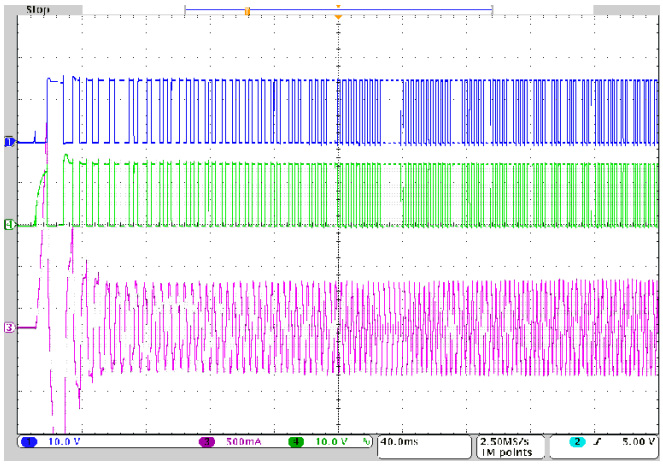


Figure 6. Start-up at 12 V

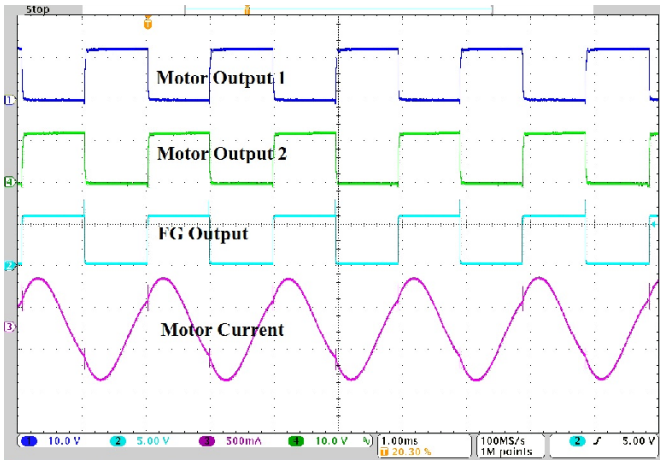


Figure 7. Motor Outputs and Phase Current at 100% Duty Cycle

Typical Application (continued)

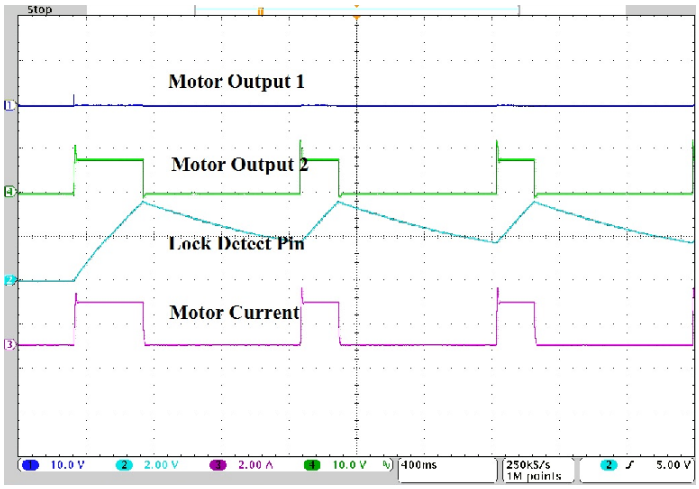


Figure 8. Lock Detection Waveform

9 Power Supply Recommendations

For testing purposes, a current limited source can be connected with voltage between 6-to 16-V on the printed-circuit-board. Use a 1-µF capacitor (minimum) to meet load transient requirements.

10 Layout

10.1 Layout Guidelines

Connect a minimum of 1-uF or greater capacitor close to power supply pins. Connect other capacitors and resistors according to the calculations (for example, pullup resistors should be connected at various pins, the c capacitors should be connected at lock detect, and so forth.)

10.2 Layout Example

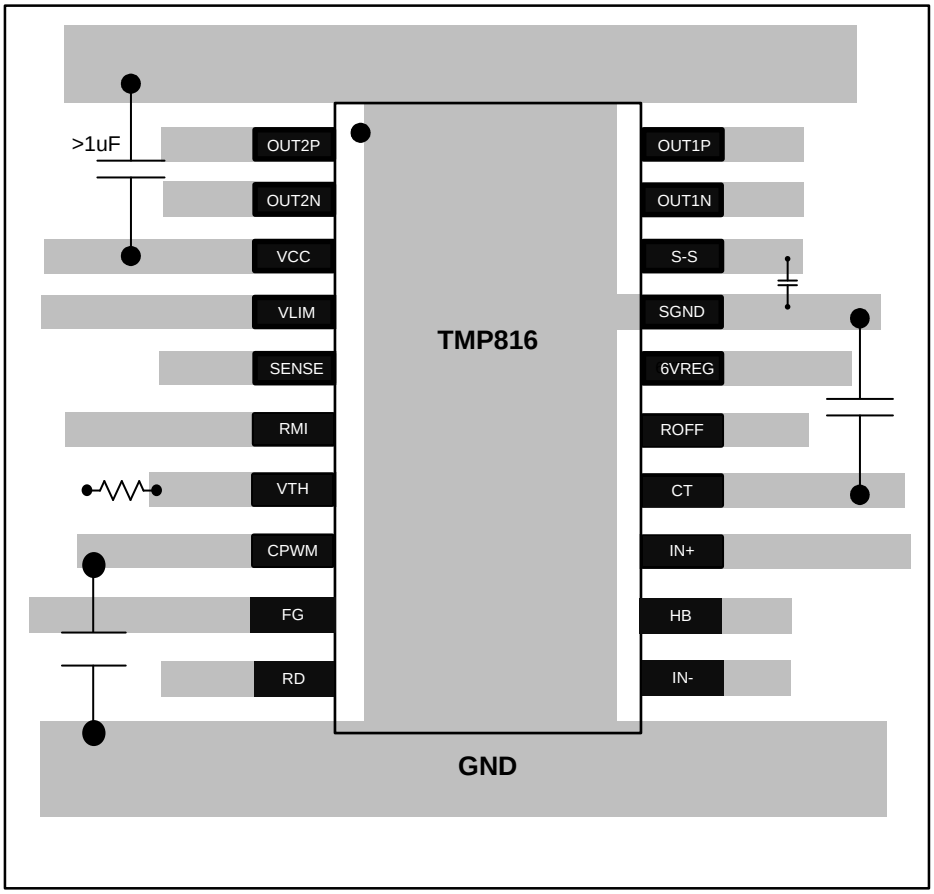


Figure 9. Recommended Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

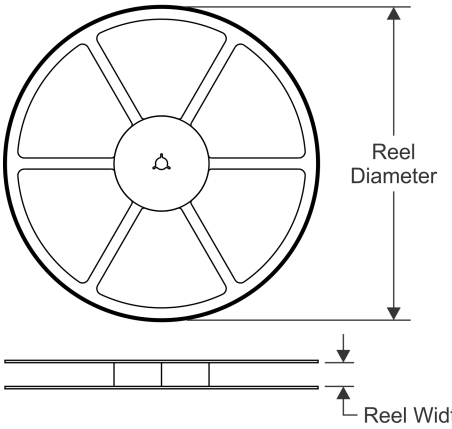
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

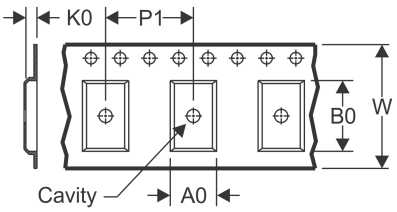
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

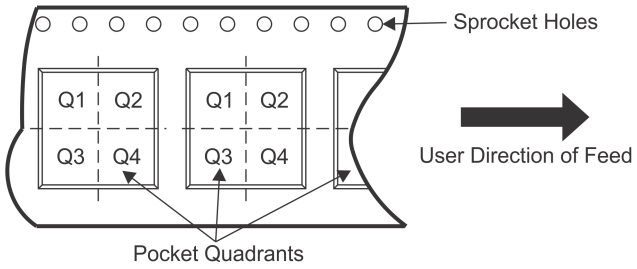


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

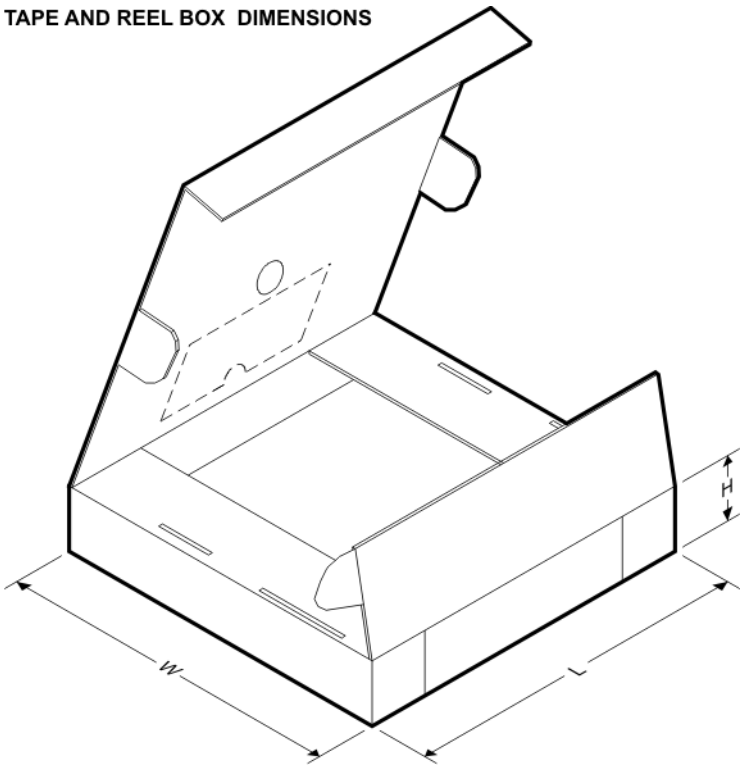
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMP816PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

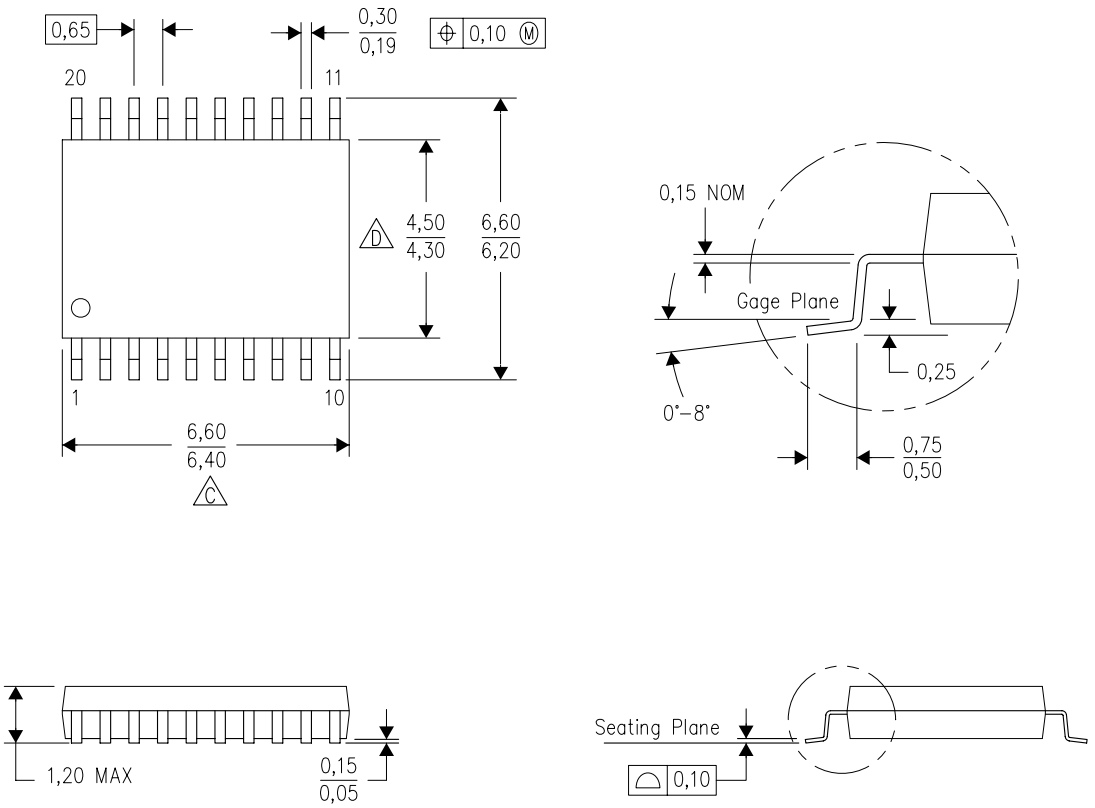
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMP816PWR	TSSOP	PW	20	2000	367.0	367.0	38.0

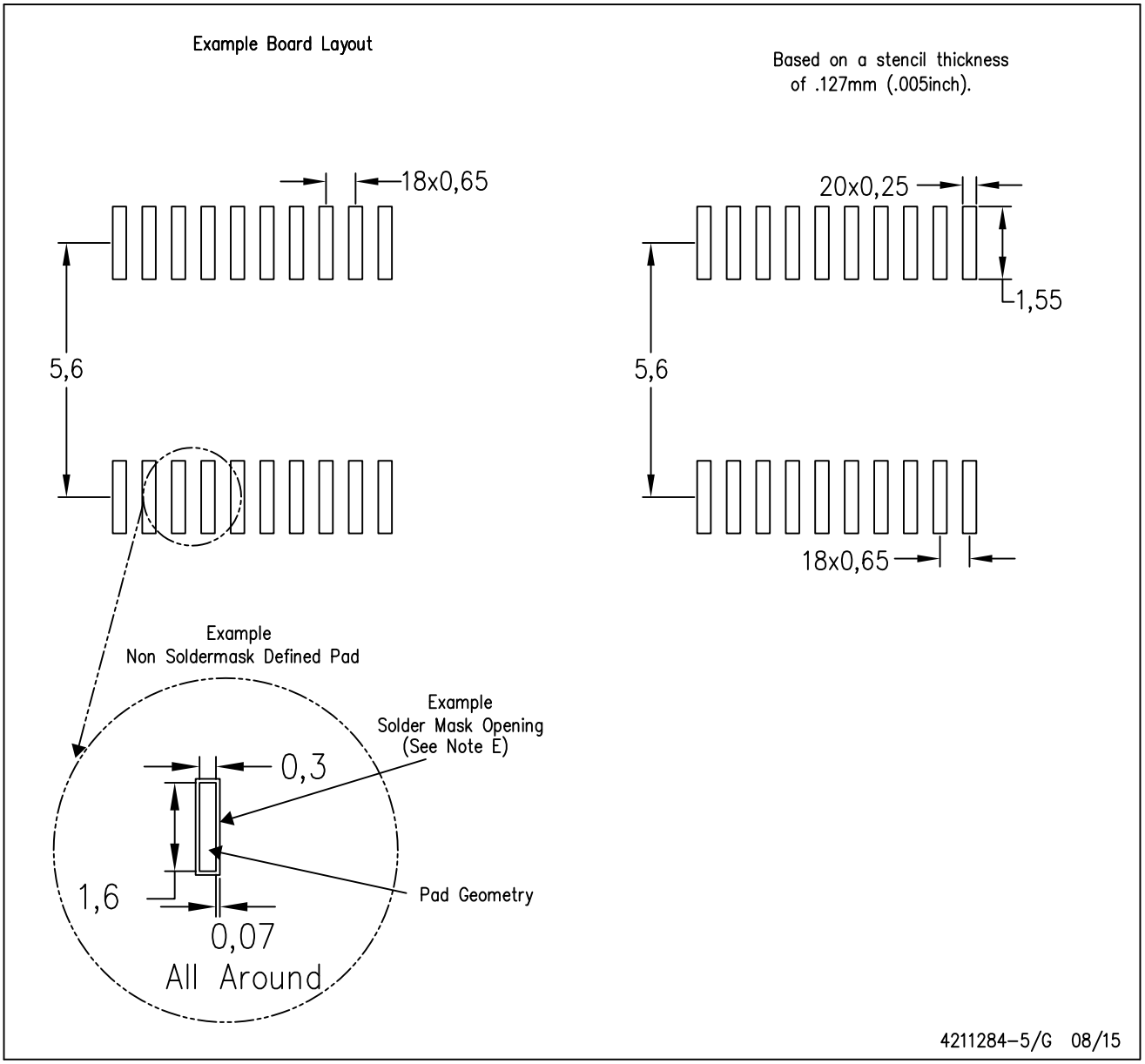
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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