

Features

- Single-voltage Operation Read/Write Operation: 2.7V to 3.6V (BV), 3.0V to 3.6V(LV)
- Fast Read Access Time – 45 ns
- Internal Program Control and Timer
- 8K Word Boot Block with Lockout
- Fast Erase Cycle Time – 1.5 Seconds
- Word-by-word Programming – 20 μ s/Word Typical
- Hardware Data Protection
- Data Polling for End of Program Detection
- Small 10 x 14 mm VSOP Package
- Typical 10,000 Write Cycles
- Lead-free Packaging Option

1. Description

The AT49BV/LV1024A is a 3-volt only in-system Flash memory. The 1-megabit of memory is organized as 65,536 words by 16 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the devices offer access times to 45 ns with power dissipation of just 72 mW over the commercial temperature range.

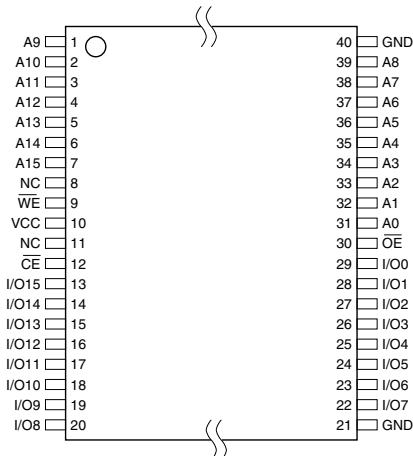
To allow for simple in-system reprogrammability, the AT49BV/LV1024A does not require high input voltages for programming. Three-volt-only commands determine the read and programming operation of the device. Reading data out of the device is similar to reading from an EPROM. Reprogramming the AT49BV/LV1024A is performed by erasing a block of data (entire chip or main memory block) and then programming on a word-by-word basis. The typical word programming time is a fast 20 μ s. The end of a program cycle can be optionally detected by the Data Polling feature. Once the end of a word program cycle has been detected, a new access for a read or program can begin. The typical number of program and erase cycles is in excess of 10,000 cycles.

The optional 8K word boot block section includes a reprogramming write lock out feature to provide data integrity. The boot sector is designed to contain user secure code, and when the feature is enabled, the boot sector is permanently protected from being erased or reprogrammed.

2. Pin Configurations

| Pin Name | Function |
|-----------------|---------------------|
| A0 - A15 | Addresses |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |
| \overline{WE} | Write Enable |
| I/O0 - I/O15 | Data Inputs/Outputs |
| NC | No Connect |

2.1 40VSOP (Type 1)

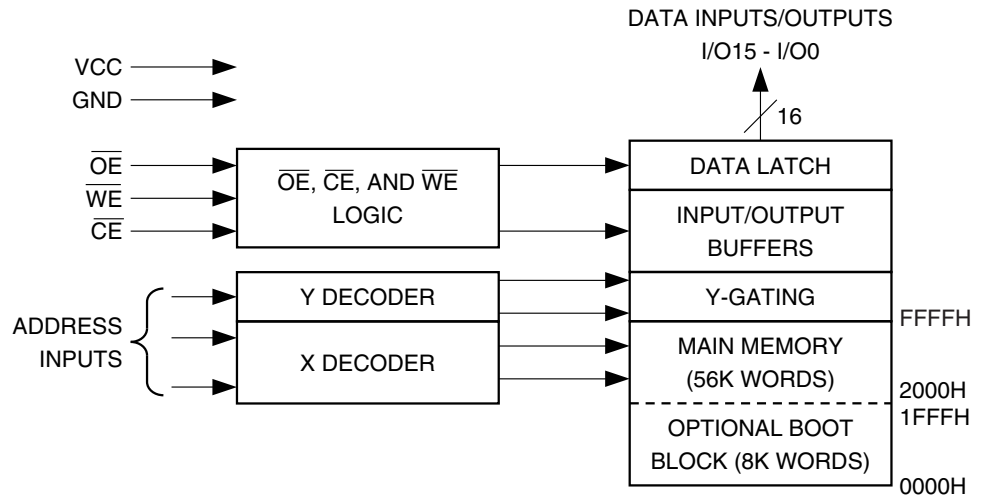


**1-megabit
(64K x 16)
3-volt Only
Flash Memory**

**AT49BV1024A
AT49LV1024A**



3. Block Diagram



4. Device Operation

4.1 Read

The AT49BV/LV1024A is accessed like an EPROM. When \overline{CE} and \overline{OE} are low and \overline{WE} is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high-impedance state whenever \overline{CE} or \overline{OE} is high. This dual-line control gives designers flexibility in preventing bus contention.

4.2 Chip Erase

When the boot block programming lockout feature is not enabled, the boot block and the main memory block will erase together from the same Chip Erase command (See [“Command Definition Table” on page 5](#)). If the boot block lockout function has been enabled, data in the boot section will not be erased. However, data in the main memory section will be erased. After a chip erase, the device will return to the read mode.

4.3 Main Memory Erase

As an alternative to the chip erase, a main memory block erase can be performed, which will erase all words not located in the boot block region to an FFFFH. Data located in the boot region will not be changed during a main memory block erase. The Main Memory Erase command is a six-bus cycle operation. The address (555H) is latched on the falling edge of the sixth cycle while the 30H data input is latched on the rising edge of \overline{WE} . The main memory erase starts after the rising edge of \overline{WE} of the sixth cycle. Please see [“Main Memory or Chip Erase Cycle Waveforms” on page 10](#). The main memory erase operation is internally controlled; it will automatically time to completion.

4.4 Word Programming

Once the memory array is erased, the device is programmed (to a logic “0”) on a word-by-word basis. Please note that a data “0” cannot be programmed back to a “1”; only erase operations can convert “0”s to “1”s. Programming is accomplished via the internal device command register and is a four-bus cycle operation (please refer to the “[Command Definition Table](#)” on page 5). The device will automatically generate the required internal program pulses.

The program cycle has addresses latched on the falling edge of \overline{WE} or \overline{CE} , whichever occurs last, and the data latched on the rising edge of \overline{WE} or \overline{CE} , whichever occurs first. Programming is completed after the specified t_{BP} cycle time. The \overline{Data} Polling feature may also be used to indicate the end of a program cycle.

4.5 Boot Block Programming Lockout

The device has one designated block that has a programming lockout feature. This feature prevents programming of data in the designated block once the feature has been enabled. The size of the block is 8K words. This block, referred to as the boot block, can contain secure code that is used to bring up the system. Enabling the lockout feature will allow the boot code to stay in the device while data in the rest of the device is updated. This feature does not have to be activated; the boot block’s usage as a write-protected region is optional to the user. The address range of the boot block is 0000H to 1FFFH.

Once the feature is enabled, the data in the boot block can no longer be erased or programmed. Data in the main memory block can still be changed through the regular programming method and can be erased using either the Chip Erase or the Main Memory Block Erase command. To activate the lockout feature, a series of six program commands to specific addresses with specific data must be performed. Please refer to the “[Command Definition Table](#)” on page 5.

4.5.1 Boot Block Lockout Detection

A software method is available to determine if programming of the boot block section is locked out. When the device is in the software product identification mode (see Software Product Identification Entry/Exit on [page 12](#)) a read from address location 0002H will show if programming the boot block is locked out. If the data on I/O0 is low, the boot block can be programmed; if the data on I/O0 is high, the program lockout feature has been activated and the block cannot be programmed. The software product identification exit code should be used to return to standard operation.

4.6 Product Identification

The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by hardware or software operation. The hardware operation mode can be used by an external programmer to identify the correct programming algorithm for the Atmel product.

For details, see “[Operating Modes](#)” on [page 6](#) (for hardware operation) or “[Software Product Identification Entry/Exit](#)” on [page 12](#). The manufacturer and device code is the same for both modes.

4.7 $\overline{\text{Data}}$ Polling

The AT49BV/LV1024A features $\overline{\text{Data}}$ Polling to indicate the end of a program or erase cycle. During a program cycle an attempted read of the last byte loaded will result in the complement of the loaded data on I/O7. Once the program cycle has been completed, true data is valid on all outputs and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin at any time during the program cycle.

4.8 Toggle Bit

In addition to $\overline{\text{Data}}$ Polling, the AT49BV/LV1024A provides another method for determining the end of a program or erase cycle. During a program or erase operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the program cycle has completed, I/O6 will stop toggling and valid data will be read. Examining the toggle bit may begin at any time during a program cycle.

4.9 Hardware Data Protection

Hardware features protect against inadvertent writes to the AT49BV/LV1024A in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) Program inhibit: holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits program cycles. (c) Noise filter: pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a program cycle.

5. Command Definition Table

| Command Sequence | Bus Cycles | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | | 4th Bus Cycle | | 5th Bus Cycle | | 6th Bus Cycle | |
|-----------------------------------|------------|---------------|------------------|--------------------|------|---------------|------|---------------|-----------------|---------------|------|---------------|------|
| | | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data | Addr | Data |
| Read | 1 | Addr | D _{OUT} | | | | | | | | | | |
| Chip Erase | 6 | 555 | AA | AAA ⁽²⁾ | 55 | 555 | 80 | 555 | AA | AAA | 55 | 555 | 10 |
| Main Memory Erase | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | 555 | 30 |
| Word Program | 4 | 555 | AA | AAA | 55 | 555 | A0 | Addr | D _{IN} | | | | |
| Boot Block Lockout ⁽³⁾ | 6 | 555 | AA | AAA | 55 | 555 | 80 | 555 | AA | AAA | 55 | 555 | 40 |
| Product ID Entry | 3 | 555 | AA | AAA | 55 | 555 | 90 | | | | | | |
| Product ID Exit ⁽⁴⁾ | 3 | 555 | AA | AAA | 55 | 555 | F0 | | | | | | |
| Product ID Exit ⁽⁴⁾ | 1 | xxx | F0 | | | | | | | | | | |

- Notes:
1. The DATA FORMAT in each bus cycle is as follows: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex).
The ADDRESS FORMAT in each bus cycle is as follows: A11 - A0 (Hex); A11 - A15 (Don't Care).
 2. Since A11 is a Don't Care, AAA can be replaced with 2AA.
 3. The 8K word boot sector has the address range 0000H to 1FFFH.
 4. Either one of the Product ID Exit commands can be used.

6. Absolute Maximum Ratings*

| | |
|---|---------------------------------|
| Temperature under Bias | -55°C to +125°C |
| Storage Temperature..... | -65°C to +150°C |
| All Input Voltages (including NC Pins) with Respect to Ground | -0.6V to +6.25V |
| All Output Voltages with Respect to Ground | -0.6V to V _{CC} + 0.6V |
| Voltage on \overline{OE} with Respect to Ground | -0.6V to +13.5V |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7. DC and AC Operating Range

| | AT49LV1024A-45 |
|------------------------------|----------------|
| Operating Temperature (Case) | 0°C - 70°C |
| V _{CC} Power Supply | 3.0V to 3.6V |

8. Operating Modes

| Mode | \overline{CE} | \overline{OE} | \overline{WE} | Ai | I/O |
|-------------------------|-----------------|------------------|-----------------|--|----------------------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | Ai | D _{OUT} |
| Program ⁽²⁾ | V _{IL} | V _{IH} | V _{IL} | Ai | D _{IN} |
| Standby/Write Inhibit | V _{IH} | X ⁽¹⁾ | X | X | High-Z |
| Program Inhibit | X | X | V _{IH} | | |
| Program Inhibit | X | V _{IL} | X | | |
| Output Disable | X | V _{IH} | X | | High-Z |
| Product Identification | | | | | |
| Hardware | V _{IL} | V _{IL} | V _{IH} | A1 - A15 = V _{IL} , A9 = V _H ⁽³⁾ , A0 = V _{IL} | Manufacturer Code ⁽⁴⁾ |
| | | | | A1 - A15 = V _{IL} , A9 = V _H ⁽³⁾ , A0 = V _{IH} | Device Code ⁽⁴⁾ |
| Software ⁽⁵⁾ | | | | A0 = V _{IL} , A1 - A15 = V _{IL} | Manufacturer Code ⁽⁴⁾ |
| | | | | A0 = V _{IH} , A1 - A15 = V _{IL} | Device Code ⁽⁴⁾ |

- Notes:
1. X can be V_{IL} or V_{IH}.
 2. Refer to AC Programming Waveforms.
 3. V_H = 12.0V ± 0.5V.
 4. Manufacturer Code: 001FH; Device Code: 0087H.
 5. See details under "Software Product Identification Entry/Exit" on [page 12](#).

9. DC Characteristics

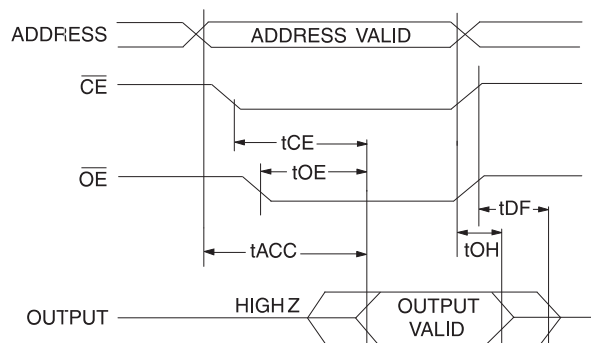
| Symbol | Parameter | Condition | Min | Max | Units |
|--------------------------------|--------------------------------------|--|-----|------|-------|
| I _{LI} | Input Load Current | V _{IN} = 0V to V _{CC} | | 10.0 | μA |
| I _{LO} | Output Leakage Current | V _{I/O} = 0V to V _{CC} | | 10.0 | μA |
| I _{SB1} | V _{CC} Standby Current CMOS | $\overline{CE} = V_{CC} - 0.3V$ to V _{CC} | | 50.0 | μA |
| I _{SB2} | V _{CC} Standby Current TTL | $\overline{CE} = 2.0V$ to V _{CC} | | 0.5 | mA |
| I _{CC} ⁽¹⁾ | V _{CC} Active Current | f = 5 MHz; I _{OUT} = 0 mA | | 20.0 | mA |
| V _{IL} | Input Low Voltage | | | 0.6 | V |
| V _{IH} | Input High Voltage | | 2.0 | | V |
| V _{OL} | Output Low Voltage | I _{OL} = 2.1 mA | | 0.45 | V |
| V _{OH1} | Output High Voltage | I _{OH} = -400 μA | 2.4 | | V |

- Note:
1. In the erase mode, I_{CC} is 40 mA.

10. AC Read Characteristics

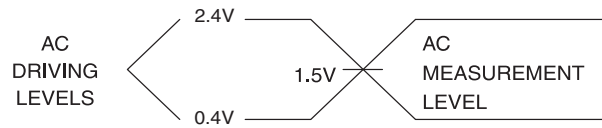
| Symbol | Parameter | AT49LV1024A-45 | | Units |
|-------------------|---|----------------|-----|-------|
| | | Min | Max | |
| t_{ACC} | Address to Output Delay | | 45 | ns |
| $t_{CE}^{(1)}$ | \overline{CE} to Output Delay | | 45 | ns |
| $t_{OE}^{(2)}$ | \overline{OE} to Output Delay | 0 | 25 | ns |
| $t_{DF}^{(3)(4)}$ | \overline{CE} or \overline{OE} to Output Float | 0 | 25 | ns |
| t_{OH} | Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first | 0 | | ns |

11. AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾



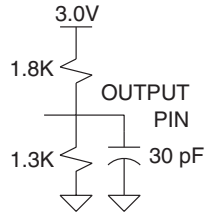
- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} , whichever occurs first ($C_L = 5$ pF).
 - This parameter is characterized and is not 100% tested.

12. Input Test Waveforms and Measurement Level



$t_R, t_F < 5 \text{ ns}$

13. Output Test Load



14. Pin Capacitance

$f = 1 \text{ MHz}, T = 25^\circ\text{C}^{(1)}$

| Symbol | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 4 | 6 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 8 | 12 | pF | $V_{OUT} = 0V$ |

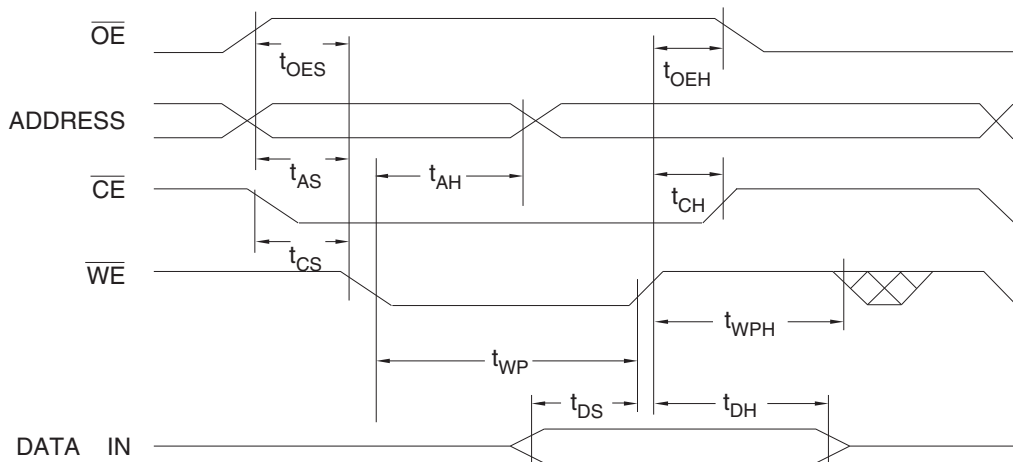
Note: 1. This parameter is characterized and is not 100% tested.

15. AC Word Load Characteristics

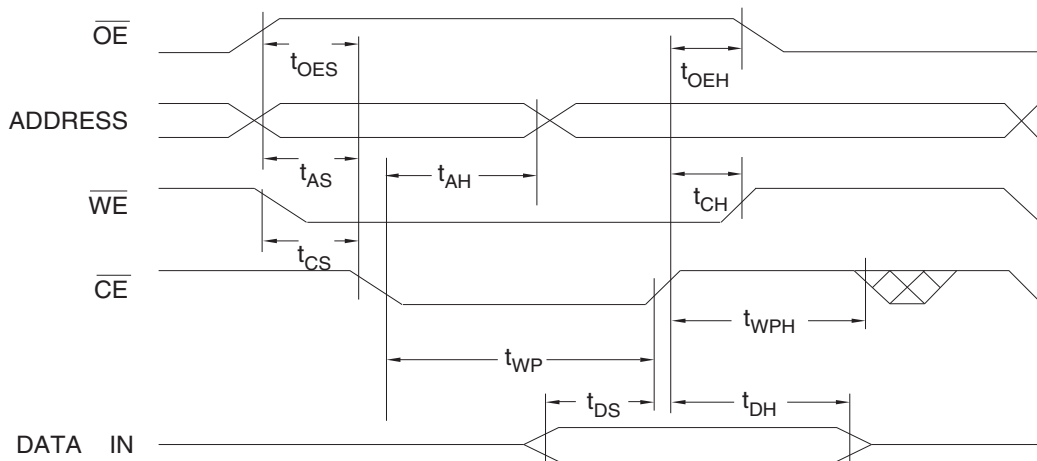
| Symbol | Parameter | Min | Max | Units |
|-------------------|--|-----|-----|-------|
| t_{AS}, t_{OES} | Address, \overline{OE} Setup Time | 0 | | ns |
| t_{AH} | Address Hold Time | 35 | | ns |
| t_{CS} | Chip Select Setup Time | 0 | | ns |
| t_{CH} | Chip Select Hold Time | 0 | | ns |
| t_{WP} | Write Pulse Width (\overline{WE} or \overline{CE}) | 35 | | ns |
| t_{DS} | Data Setup Time | 35 | | ns |
| t_{DH}, t_{OEH} | Data, \overline{OE} Hold Time | 0 | | ns |
| t_{WPH} | Write Pulse Width High | 35 | | ns |

16. AC Word Load Waveforms

16.1 \overline{WE} Controlled



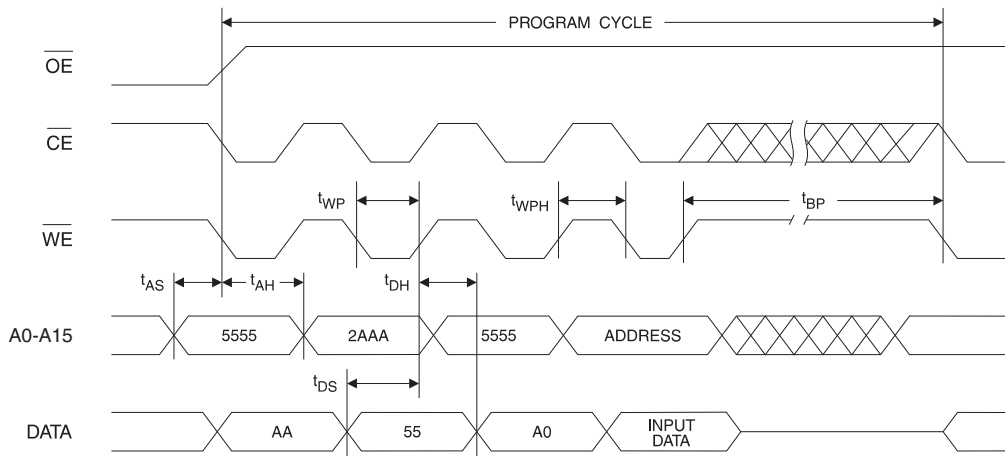
16.2 \overline{CE} Controlled



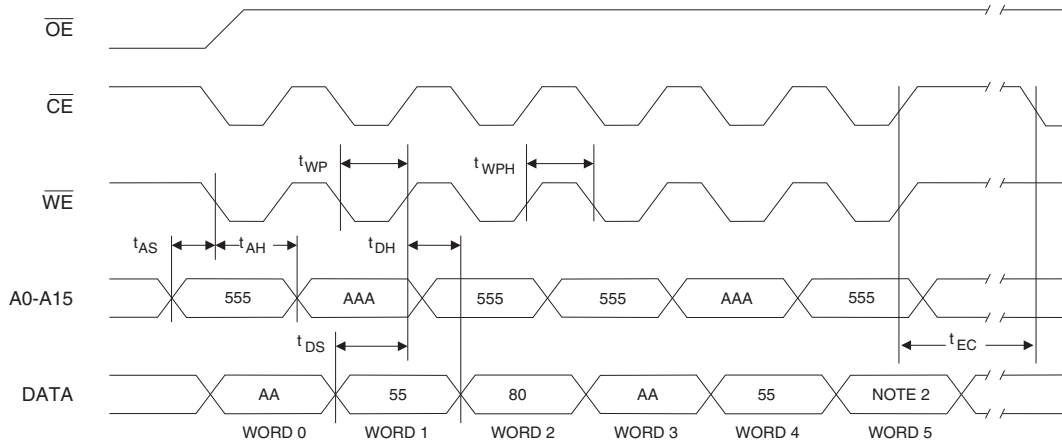
17. Program Cycle Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|-----------|------------------------|-----|-----|-----|---------|
| t_{BP} | Word Programming Time | | 20 | 50 | μ s |
| t_{AS} | Address Setup Time | 0 | | | ns |
| t_{AH} | Address Hold Time | 35 | | | ns |
| t_{DS} | Data Setup Time | 35 | | | ns |
| t_{DH} | Data Hold Time | 0 | | | ns |
| t_{WP} | Write Pulse Width | 35 | | | ns |
| t_{WPH} | Write Pulse Width High | 35 | | | ns |
| t_{EC} | Erase Cycle Time | | 1.5 | 3 | seconds |

18. Program Cycle Waveforms



19. Main Memory or Chip Erase Cycle Waveforms



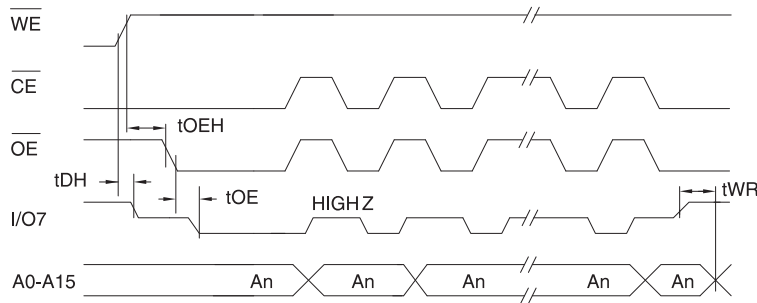
- Notes:
- \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.
 - For chip erase, the address should be 10H. For a main memory erase, the data should be 30H.

20. Data Polling Characteristics⁽¹⁾

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|--|-----|-----|-----|-------|
| t_{DH} | Data Hold Time | 10 | | | ns |
| $t_{OE\overline{H}}$ | \overline{OE} Hold Time | 10 | | | ns |
| t_{OE} | \overline{OE} to Output Delay ⁽²⁾ | | | | ns |
| t_{WR} | Write Recovery Time | 0 | | | ns |

- Notes: 1. These parameters are characterized and not 100% tested.
 2. See t_{OE} spec in “AC Read Characteristics” on page 7.

21. Data Polling Waveforms

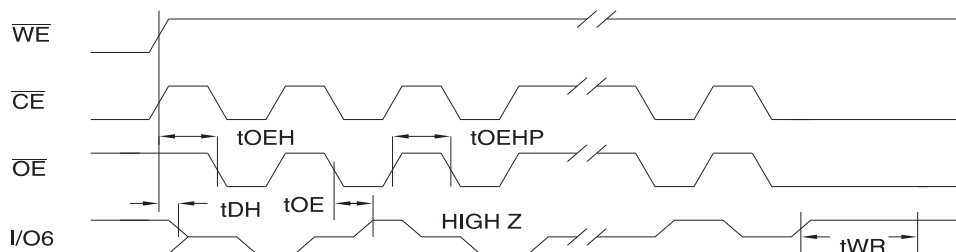


22. Toggle Bit Characteristics⁽¹⁾

| Symbol | Parameter | Min | Typ | Max | Units |
|----------------------|--|-----|-----|-----|-------|
| t_{DH} | Data Hold Time | 10 | | | ns |
| $t_{OE\overline{H}}$ | \overline{OE} Hold Time | 10 | | | ns |
| t_{OE} | \overline{OE} to Output Delay ⁽²⁾ | | | | ns |
| t_{OEHP} | \overline{OE} High Pulse | 150 | | | ns |
| t_{WR} | Write Recovery Time | 0 | | | ns |

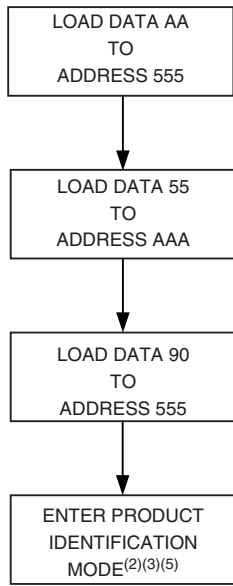
- Notes: 1. These parameters are characterized and not 100% tested.
 2. See t_{OE} spec in “AC Read Characteristics” on page 7.

23. Toggle Bit Waveforms⁽¹⁾⁽²⁾⁽³⁾

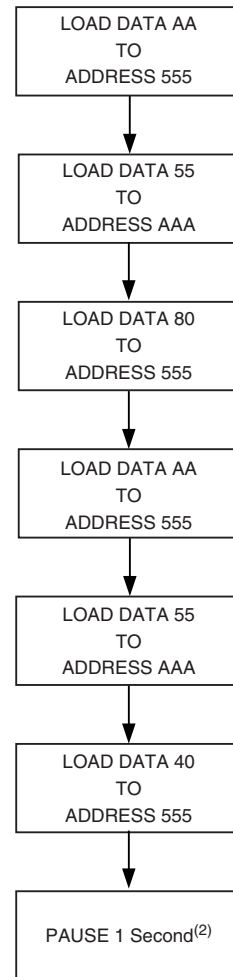


- Notes: 1. Toggling either \overline{OE} or \overline{CE} or both \overline{OE} and \overline{CE} will operate toggle bit. The t_{OEHP} specification must be met by the toggling input(s).
 2. Beginning and ending state of $I/O6$ will vary.
 3. Any address location may be used but the address should not vary.

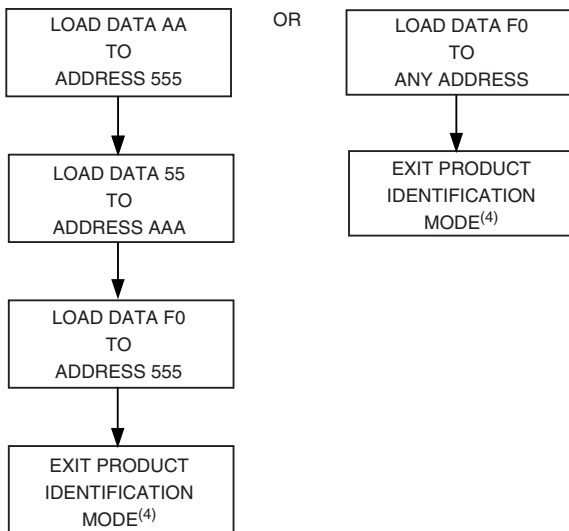
23.1 Software Product Identification Entry⁽¹⁾



23.3 Boot Block Lockout Enable Algorithm⁽¹⁾



23.2 Software Product Identification Exit⁽¹⁾



- Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex); Address Format: A11 - A0 (Hex); A11 - A15 (Don't Care).
 2. Boot Block Lockout feature enabled.

- Notes:
1. Data Format: I/O15 - I/O8 (Don't Care); I/O7 - I/O0 (Hex); Address Format: A11 - A0 (Hex); A11 - A15 (Don't Care).
 2. A1 - A15 = V_{IL} .
Manufacturer Code is read for A0 = V_{IL} ;
Device Code is read for A0 = V_{IH} .
 3. The device does not remain in identification mode if powered down.
 4. The device returns to standard operation mode.
 5. Manufacturer Code: 001FH
Device Code: 0087H

24. Ordering Information

24.1 Standard Package Option

| t _{ACC} (ns) | I _{CC} (mA) | | Ordering Code | Package | Operation Range |
|--------------------------|----------------------|---------|------------------|---------|----------------------------|
| | Active | Standby | | | |
| 45 | 20 | 0.05 | AT49LV1024A-45VC | 40V | Commercial (0° to 70°C) |

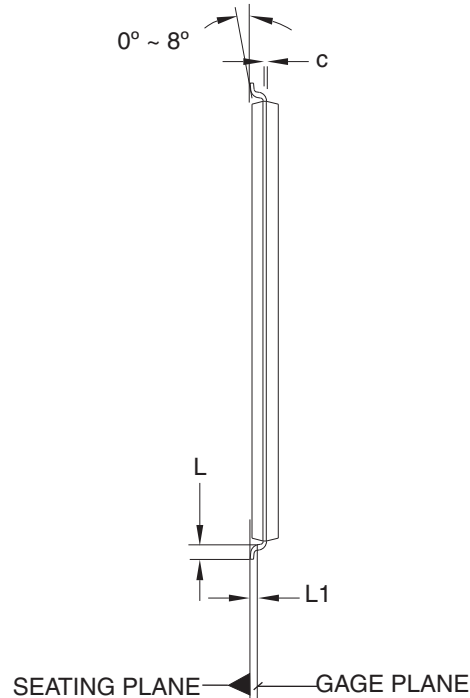
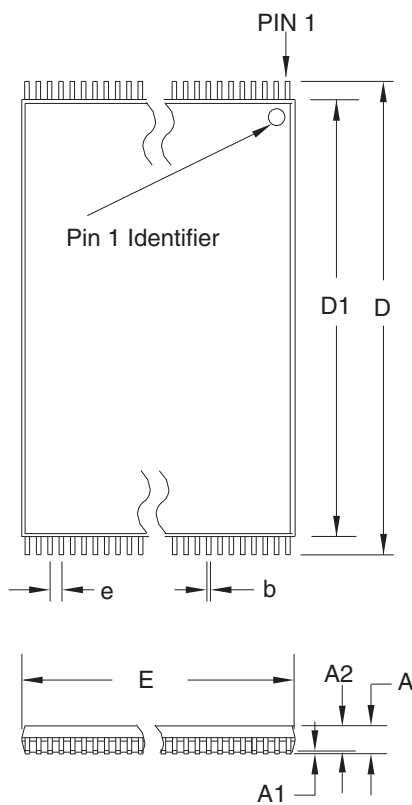
24.2 Lead-Free Option

| t _{ACC} (ns) | I _{CC} (mA) | | Ordering Code | Package | Operation Range |
|--------------------------|----------------------|---------|------------------|---------|----------------------------|
| | Active | Standby | | | |
| 45 | 20 | 0.05 | AT49LV1024A-45VL | 40V | Commercial (0° to 70°C) |

| Package Type | |
|--------------|--|
| 40V | 40-lead, Thin Small Outline Package (VSOP) (10 mm x 14 mm) |

25. Packaging Information

25.1 40V – VSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------------|-------|-------|--------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 13.80 | 14.00 | 14.20 | |
| D1 | 12.30 | 12.40 | 12.50 | Note 2 |
| E | 9.90 | 10.00 | 10.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.50 BASIC | | | |

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation CA.
 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
 3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

40V, 40-lead (10 x 14 mm Package) Plastic Thin Small Outline Package, Type I (VSOP)

DRAWING NO.

40V

REV.

B



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