



**THE DATASHEET OF
AT49BV320D-70TU**



Features

- Single Voltage Read/Write Operation: 2.65V to 3.6V
- Access Time – 70 ns
- Sector Erase Architecture
 - Sixty-three 32K Word (64K Bytes) Sectors with Individual Write Lockout
 - Eight 4K Word (8K Bytes) Sectors with Individual Write Lockout
- Fast Word Program Time – 10 μ s
- Fast Sector Erase Time – 100 ms
- Suspend/Resume Feature for Erase and Program
 - Supports Reading and Programming from Any Sector by Suspending Erase of a Different Sector
 - Supports Reading Any Word by Suspending Programming of Any Other Word
- Low-power Operation
 - 10 mA Active
 - 15 μ A Standby
- VPP Pin for Write Protection and Accelerated Program Operation
- \overline{WP} Pin for Sector Protection
- \overline{RESET} Input for Device Initialization
- Flexible Sector Protection
- TSOP and CBGA Package Options
- Top or Bottom Boot Block Configuration Available
- 128-bit Protection Register
- Minimum 100,000 Erase Cycles
- Common Flash Interface (CFI)
- Green (Pb/Halide-free) Packaging

1. Description

The AT49BV320D(T) is a 2.7-volt 32-megabit Flash memory organized as 2,097,152 words of 16 bits each. The memory is divided into 71 sectors for erase operations. The device is offered in a 48-lead TSOP package and a 47-ball CBGA package. The device has \overline{CE} and \overline{OE} control signals to avoid any bus contention. This device can be read or reprogrammed using a single power supply, making it ideally suited for in-system programming.

The device powers on in the read mode. Command sequences are used to place the device in other operation modes such as program and erase. The device has the capability to protect the data in any sector (see “[Flexible Sector Protection](#)” on page 6).

To increase the flexibility of the device, it contains an Erase Suspend and Program Suspend feature. This feature will put the erase or program on hold for any amount of time and let the user read data from or program data to any of the remaining sectors within the memory.

The VPP pin provides data protection. When the V_{PP} input is below 0.4V, the program and erase functions are inhibited. When V_{PP} is at 1.65V or above, normal program and erase operations can be performed. With V_{PP} at 10.0V, the program (Dual-word Program command) operation is accelerated.



**32-megabit
(2M x 16)
3-volt Only
Flash Memory**

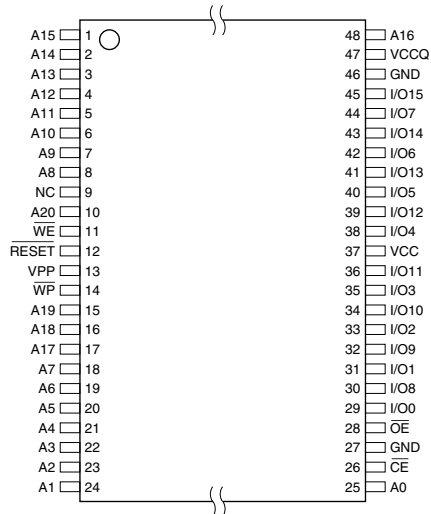
**AT49BV320D
AT49BV320DT**



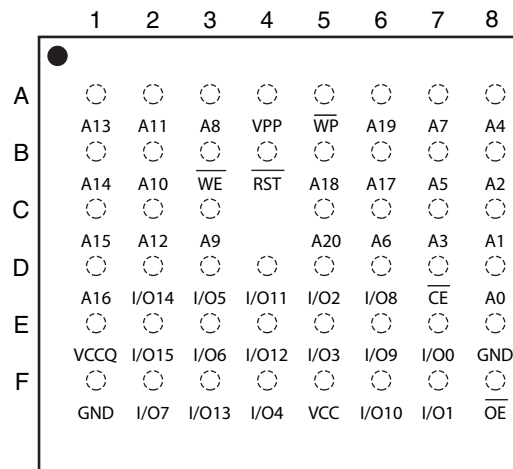
2. Pin Configurations

| Pin Name | Function |
|--------------------|---------------------|
| A0 - A20 | Addresses |
| \overline{CE} | Chip Enable |
| \overline{OE} | Output Enable |
| \overline{WE} | Write Enable |
| \overline{RESET} | Reset |
| VPP | Write Protection |
| I/O0 - I/O15 | Data Inputs/Outputs |
| NC | No Connect |
| VCCQ | Output Power Supply |
| \overline{WP} | Write Protect |

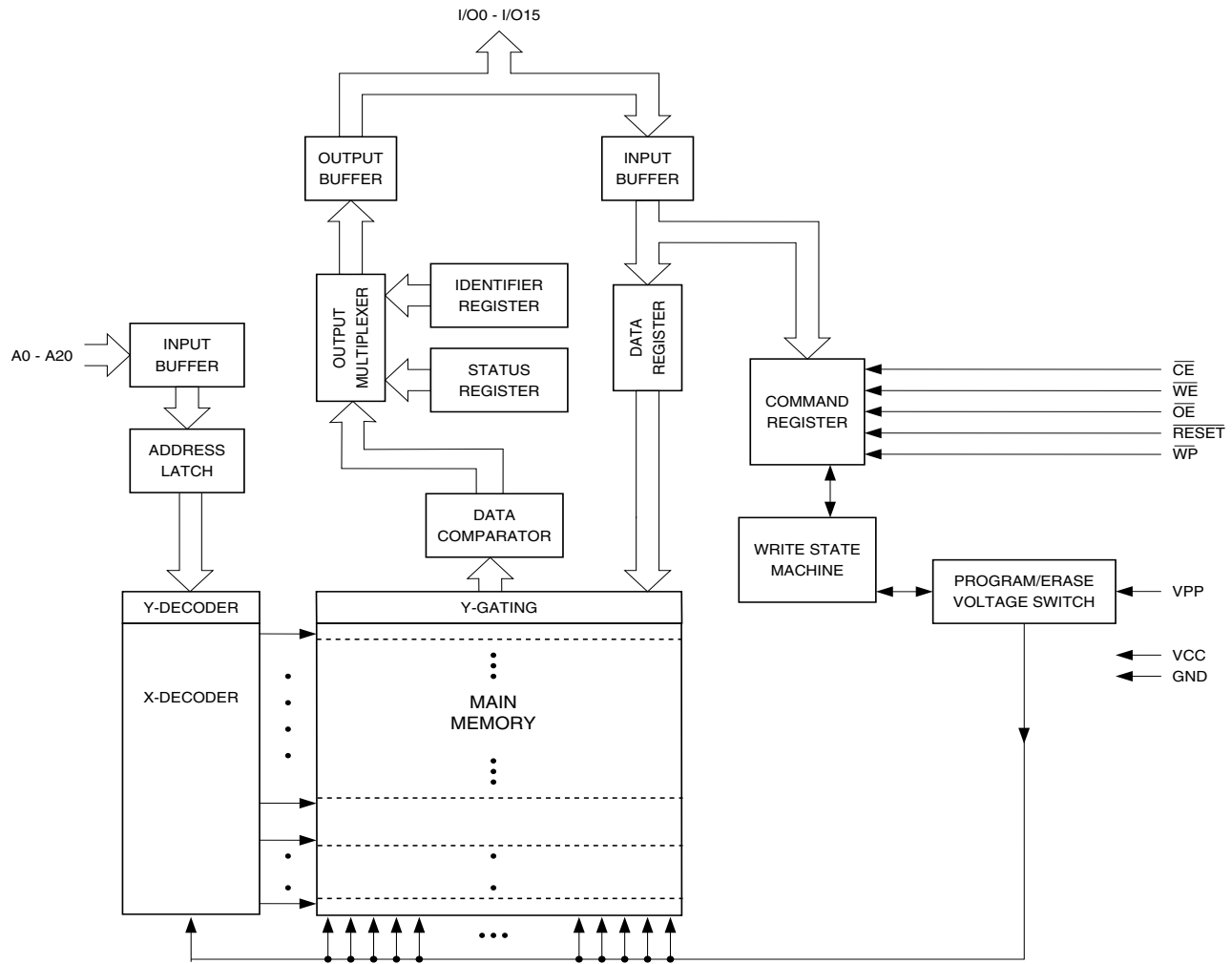
2.1 TSOP Top View (Type 1)



2.2 CBGA Top View (Ball Down)



3. Block Diagram



4. Device Operation

4.1 Command Sequences

When the device is first powered on, it will be in the read mode. In order to perform other device functions, a series of command sequences are entered into the device. The command sequences are shown in the “[Command Definition Table](#)” on page 15 (I/O8 - I/O15 are don't care inputs for the command codes). The command sequences are written by applying a low pulse on the \overline{WE} or \overline{CE} input with \overline{CE} or \overline{WE} low (respectively) and \overline{OE} high. The address and data are latched by the first rising edge of \overline{CE} or \overline{WE} . Standard microprocessor write timings are used. The address locations used in the command sequences are not affected by entering the command sequences.

4.2 Read

When the AT49BV320D(T) is in the read mode, with \overline{CE} and \overline{OE} low and \overline{WE} high, the data stored at the memory location determined by the address pins are asserted on the outputs. The

outputs are put in the high impedance state whenever \overline{CE} or \overline{OE} is high. This dual-line control gives designers flexibility in preventing bus contention.

4.3 Reset

A \overline{RESET} input pin is provided to ease some system applications. When \overline{RESET} is at a logic high level, the device is in its standard operating mode. A low level on the \overline{RESET} input halts the present device operation and puts the outputs of the device in a high impedance state. When a high level is reasserted on the \overline{RESET} pin, the device returns to the read mode, depending upon the state of the control inputs.

4.4 Erase

Before a word can be reprogrammed, it must be erased. The erased state of memory bits is a logical "1". The individual sectors can be erased by using the Sector Erase command.

4.4.1 Sector Erase

The device is organized into 71 sectors (SA0 - SA70) that can be individually erased. The Sector Erase command is a two-bus cycle operation. The sector address and the D0H Data Input command are latched on the rising edge of \overline{WE} . The sector erase starts after the rising edge of \overline{WE} of the second cycle provided the given sector has not been protected. The erase operation is internally controlled; it will automatically time to completion. The maximum time to erase a sector is t_{SEC} . An attempt to erase a sector that has been protected will result in the operation terminating immediately.

4.5 Word Programming

Once a memory sector is erased, it is programmed (to a logical "0") on a word-by-word basis. Programming is accomplished via the Internal Device command register and is a two-bus cycle operation. The device will automatically generate the required internal program pulses.

Any commands, except Read Status Register, Program Suspend and Program Resume, written to the chip during the embedded programming cycle will be ignored. If a hardware reset happens during programming, the data at the location being programmed will be corrupted. Please note that a data "0" cannot be programmed back to a "1"; only erase operations can convert "0"s to "1"s. Programming is completed after the specified t_{BP} cycle time. If the program status bit is a "1", the device was not able to verify that the program operation was performed successfully. The status register indicates the programming status. While the program sequence executes, status bit I/O7 is "0".

4.6 VPP Pin

The circuitry of the AT49BV320D(T) is designed so that the device cannot be programmed or erased if the V_{PP} voltage is less than 0.4V. When V_{PP} is at 1.65V or above, normal program and erase operations can be performed. The VPP pin cannot be left floating.

4.7 Read Status Register

The status register indicates the status of device operations and the success/failure of that operation. The Read Status Register command causes subsequent reads to output data from the status register until another command is issued. To return to reading from the memory, issue a Read command.

The status register bits are output on I/O7 - I/O0. The upper byte, I/O15 - I/O8, outputs 00H when a Read Status Register command is issued.

The contents of the status register [SR7:SR0] are latched on the falling edge of \overline{OE} or \overline{CE} (whichever occurs last), which prevents possible bus errors that might occur if status register contents change while being read. \overline{CE} or \overline{OE} must be toggled with each subsequent status read, or the status register will not indicate completion of a Program or Erase operation.

When the Write State Machine (WSM) is active, SR7 will indicate the status of the WSM; the remaining bits in the status register indicate whether the WSM was successful in performing the preferred operation (see Table 4-1).

Table 4-1. Status Register Bit Definition

| WSMS | ESS | ES | PS | VPPS | PSS | SLS | R |
|-----------------------------------------------------------------------------------------------------------------------------------------|-----|----|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|--------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| | | | | | | | Notes |
| SR7 WRITE STATE MACHINE STATUS (WSMS) 1 = Ready 0 = Busy | | | | Check Write State Machine bit first to determine Word Program or Sector Erase completion, before checking program or erase status bits. | | | |
| SR6 = ERASE SUSPEND STATUS (ESS) 1 = Erase Suspended 0 = Erase In Progress/Completed | | | | When Erase Suspend is issued, WSM halts execution and sets both WSMS and ESS bits to "1" – ESS bit remains set to "1" until an Erase Resume command is issued. | | | |
| SR5 = ERASE STATUS (ES) 1 = Error in Sector Erase 0 = Successful Sector Erase | | | | When this bit is set to "1", WSM has applied the max number of erase pulses to the sector and is still unable to verify successful sector erasure. | | | |
| SR4 = PROGRAM STATUS (PS) 1 = Error in Programming 0 = Successful Programming | | | | When this bit is set to "1", WSM has attempted but failed to program a word | | | |
| SR3 = VPP STATUS (VPPS) 1 = VPP Low Detect, Operation Abort 0 = VPP OK | | | | The V _{PP} status bit does not provide continuous indication of VPP level. The WSM interrogates V _{PP} level only after the Program or Erase command sequences have been entered and informs the system if V _{PP} has not been switched on. The V _{PP} is also checked before the operation is verified by the WSM. | | | |
| SR2 = PROGRAM SUSPEND STATUS (PSS) 1 = Program Suspended 0 = Program in Progress/Completed | | | | When Program Suspend is issued, WSM halts execution and sets both WSMS and PSS bits to "1". PSS bit remains set to "1" until a Program Resume command is issued. | | | |
| SR1 = SECTOR LOCK STATUS (SLS) 1 = Prog/Erase attempted on a locked sector; Operation aborted. 0 = No operation to locked sectors | | | | If a Program or Erase operation is attempted to one of the locked sectors, this bit is set by the WSM. The operation specified is aborted and the device is returned to read status mode. | | | |
| SR0 = RESERVED FOR FUTURE ENHANCEMENTS (R) | | | | This bit is reserved for future use and should be masked out when polling the status register. | | | |

Note: 1. A Command Sequence Error is indicated when SR1, SR3, SR4 and SR5 are set.

4.7.1 Clear Status Register

The WSM can set status register bits 1 through 7 and can clear bits 2, 6 and 7; but, the WSM cannot clear status register bits 1, 3, 4 or 5. Because bits 1, 3, 4 and 5 indicate various error conditions, these bits can be cleared only through the Clear Status Register command. By allowing the system software to control the resetting of these bits, several operations may be performed (such as cumulatively programming several addresses or erasing multiple sectors in sequence) before reading the status register to determine if an error occurred during those operations. The status register should be cleared before beginning another operation. The Read command must be issued before data can be read from the memory array. The status register can also be cleared by resetting the device.

4.8 Flexible Sector Protection

The AT49BV320D(T) offers two sector protection modes, the Softlock and the Hardlock. The Softlock mode is optimized as sector protection for sectors whose content changes frequently. The Hardlock protection mode is recommended for sectors whose content changes infrequently. Once either of these two modes is enabled, the contents of the selected sector is read-only and cannot be erased or programmed. Each sector can be independently programmed for either the Softlock or Hardlock sector protection mode. At power-up and reset, all sectors have their Softlock protection mode enabled.

4.8.1 Softlock and Unlock

The Softlock protection mode can be disabled by issuing a two-bus cycle Unlock command to the selected sector. Once a sector is unlocked, its contents can be erased or programmed. To enable the Softlock protection mode, a two-bus cycle Softlock command must be issued to the selected sector.

4.8.2 Hardlock and Write Protect

The Hardlock sector protection mode operates in conjunction with the Write Protect (\overline{WP}) pin. The Hardlock sector protection mode can be enabled by issuing a two-bus cycle Hardlock Software command to the selected sector. The state of the Write Protect pin affects whether the Hardlock protection mode can be overridden.

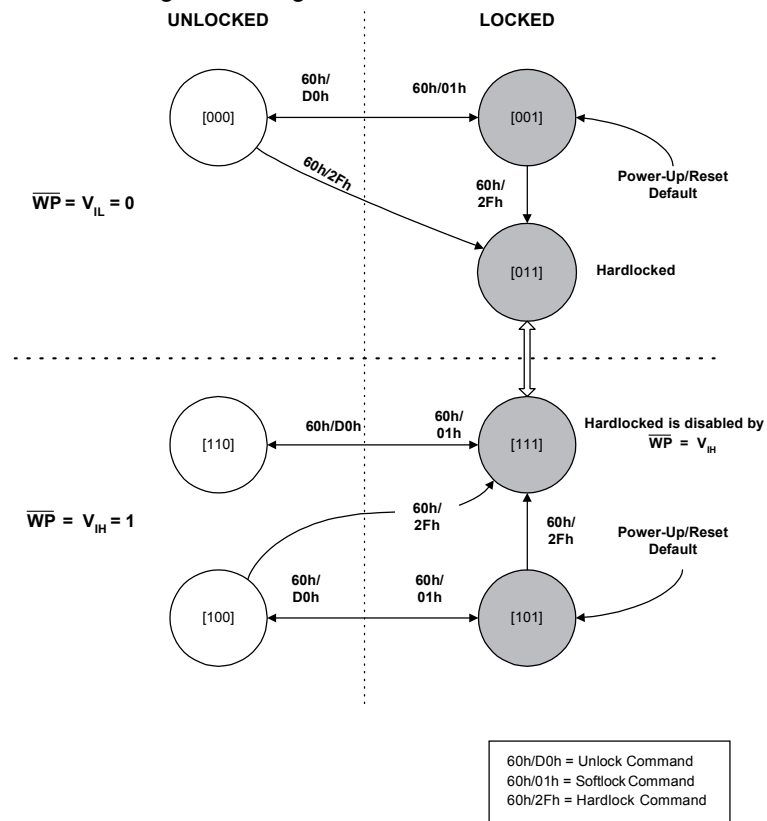
- When the \overline{WP} pin is low and the Hardlock protection mode is enabled, the sector cannot be unlocked and the contents of the sector is read-only.
- When the \overline{WP} pin is high, the Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command.

To disable the Hardlock sector protection mode, the chip must be either reset or power cycled.

Table 4-2. Hardlock and Softlock Protection Configurations in Conjunction with \overline{WP}

| V_{PP} | \overline{WP} | Hard-lock | Soft-lock | Erase/Prog Allowed? | Comments |
|-------------|-----------------|-----------|-----------|---------------------|-----------------------------------------------------------------------------------------------|
| $V_{CC}/5V$ | 0 | 0 | 0 | Yes | No sector is locked |
| $V_{CC}/5V$ | 0 | 0 | 1 | No | Sector is Softlocked. The Unlock command can unlock the sector. |
| $V_{CC}/5V$ | 0 | 1 | 1 | No | Hardlock protection mode is enabled. The sector cannot be unlocked. |
| $V_{CC}/5V$ | 1 | 0 | 0 | Yes | No sector is locked. |
| $V_{CC}/5V$ | 1 | 0 | 1 | No | Sector is Softlocked. The Unlock command can unlock the sector. |
| $V_{CC}/5V$ | 1 | 1 | 0 | Yes | Hardlock protection mode is overridden and the sector is not locked. |
| $V_{CC}/5V$ | 1 | 1 | 1 | No | Hardlock protection mode is overridden and the sector can be unlocked via the Unlock command. |
| V_{IL} | x | x | x | No | Erase and Program Operations cannot be performed. |

Figure 4-1. Sector Locking State Diagram



Note: 1. The notation [X, Y, Z] denotes the locking state of a sector. The current locking state of a sector is defined by the state of \overline{WP} and the two bits of the sector-lock status D[1:0].

4.8.3 Sector Protection Detection

A software method is available to determine if the sector protection Softlock or Hardlock features are enabled. When the device is in the software product identification mode, a read from the I/O0 and I/O1 at address location 00002H within a sector will show if the sector is unlocked, soft-locked, or hardlocked.

Table 4-3. Sector Protection Status

| I/O1 | I/O0 | Sector Protection Status |
|------|------|------------------------------------|
| 0 | 0 | Sector Not Locked |
| 0 | 1 | Softlock Enabled |
| 1 | 0 | Hardlock Enabled |
| 1 | 1 | Both Hardlock and Softlock Enabled |

4.9 Erase Suspend/Erase Resume

The Erase Suspend command allows the system to interrupt a sector erase operation and then program or read data from a different sector within the memory. After the Erase Suspend command is given, the device requires a maximum time of 15 μ s to suspend the erase operation. After the erase operation has been suspended, the system can then read data or program data to any other sector within the device. An address is not required during the Erase Suspend command. During a sector erase suspend, another sector cannot be erased. To resume the sector erase operation, the system must write the Erase Resume command. The Erase Resume command is a one-bus cycle command. The only valid commands while erase is suspended are Read Status Register, Product ID Entry, CFI Query, Program, Program Resume, Erase Resume, Sector Softlock/Hardlock, Sector Unlock.

4.10 Program Suspend/Program Resume

The Program Suspend command allows the system to interrupt a programming operation and then read data from a different word within the memory. After the Program Suspend command is given, the device requires a maximum of 20 μ s to suspend the programming operation. After the programming operation has been suspended, the system can then read data from any other word within the device. An address is not required during the program suspend operation. To resume the programming operation, the system must write the Program Resume command. The program suspend and resume are one-bus cycle commands. The command sequence for the erase suspend and program suspend are the same and the command sequence for the erase resume and program resume are the same. The only other valid commands while program is suspended are Read Status Register, Product ID Entry, CFI Query and Program Resume.

4.11 Product Identification

The product identification mode identifies the device and manufacturer as Atmel. It may be accessed by a software operation. For details, see [“Operating Modes” on page 21](#).

4.12 128-bit Protection Register

The AT49BV320D(T) contains a 128-bit register that can be used for security purposes in system design. The protection register is divided into two 64-bit sectors. The two sectors are designated as sector A and sector B. The data in sector A is non-changeable and is programmed at the factory with a unique number. The data in sector B is programmed by the user and can be locked out such that data in the sector cannot be reprogrammed. To program sector

B in the protection register, the two-bus cycle Program Protection Register command must be used as shown in the “[Command Definition Table](#)” on page 15. To lock out sector B, the two-bus cycle Lock Protection Register command must be used as shown in the “[Command Definition Table](#)”. Data bit D1 must be zero during the second bus cycle. All other data bits during the second bus cycle are don't cares. To determine whether sector B is locked out, use the status of sector B protection command. If data bit D1 is zero, sector B is locked. If data bit D1 is one, sector B can be reprogrammed. Please see the “[Protection Register Addressing Table](#)” on page 16 for the address locations in the protection register. To read the protection register, the Product ID Entry command is given followed by a normal read operation from an address within the protection register. After determining whether sector B is protected or not, or reading the protection register, the Read command must be given to return to the read mode.

4.13 Common Flash Interface (CFI)

CFI is a published, standardized data structure that may be read from a flash device. CFI allows system software to query the installed device to determine the configurations, various electrical and timing parameters and functions supported by the device. CFI is used to allow the system to learn how to interface to the flash device most optimally. The two primary benefits of using CFI are ease of upgrading and second source availability. The command to enter the CFI Query mode is a one-bus cycle command which requires writing data 98h to any address. The CFI Query command can be written when the device is ready to read data or can also be written when the part is in the product ID mode. Once in the CFI Query mode, the system can read CFI data at the addresses given in “[Common Flash Interface Definition Table](#)” on page 27. To return to the read mode, issue the Read command.

4.14 Hardware Data Protection

The Hardware Data Protection feature protects against inadvertent programs to the AT49BV320D(T) in the following ways: (a) V_{CC} sense: if V_{CC} is below 1.8V (typical), the program function is inhibited. (b) V_{CC} power-on delay: once V_{CC} has reached the V_{CC} sense level, the device will automatically time out 10 ms (typical) before programming. (c) Program inhibit: holding any one of \overline{OE} low, \overline{CE} high or \overline{WE} high inhibits program cycles. (d) Program inhibit: V_{PP} is less than V_{LPP} .

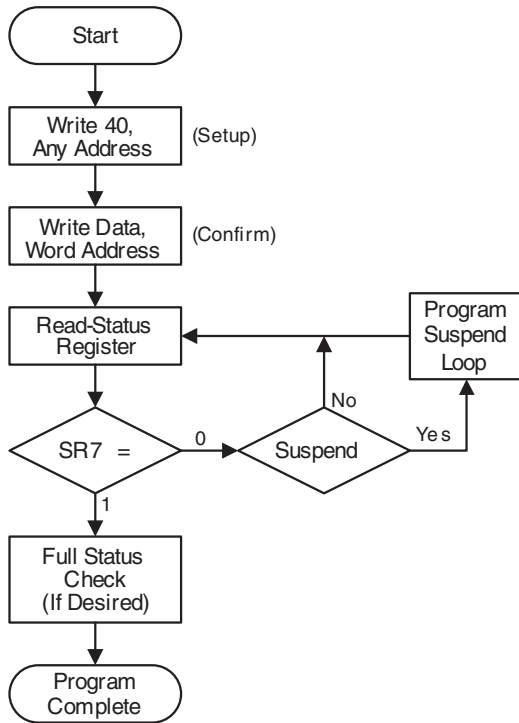
4.15 Input Levels

While operating with a 2.65V to 3.6V power supply, the address inputs and control inputs (\overline{OE} , \overline{CE} and \overline{WE}) may be driven from 0 to 5.5V without adversely affecting the operation of the device. The I/O lines can only be driven from 0 to $V_{CCQ} + 0.6V$.

4.16 Output Levels

For the AT49BV320D(T), output high levels (V_{OH}) are equal to $V_{CCQ} - 0.1V$ (not V_{CC}). For 2.65V - 3.6V output levels, V_{CCQ} must be tied to V_{CC} .

5. Word Program Flowchart

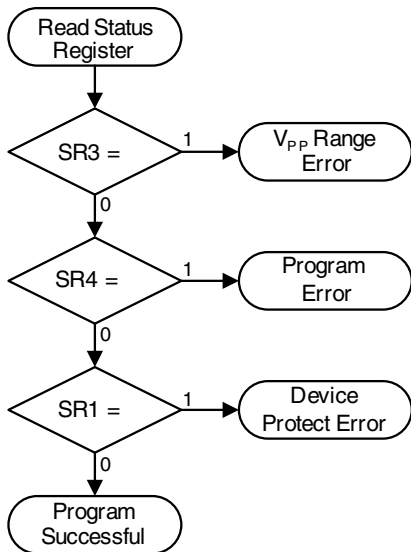


6. Word Program Procedure

| Bus Operation | Command | Comments |
|---------------|---------------|-------------------------------------------------------------------------------------------|
| Write | Program Setup | Data = 40 Addr = Any Address |
| Write | Data | Data = Data to program Addr = Location to program |
| Read | None | Status register data: Toggle \overline{CE} or \overline{OE} to update status register |
| Idle | None | Check SR7 1 = WSM Ready 0 = WSM Busy |

Repeat for subsequent Word Program operations.
Full status register check can be done after each program, or after a sequence of program operations.
Write FF after the last operation to set to the Read state.

7. Full Status Check Flowchart

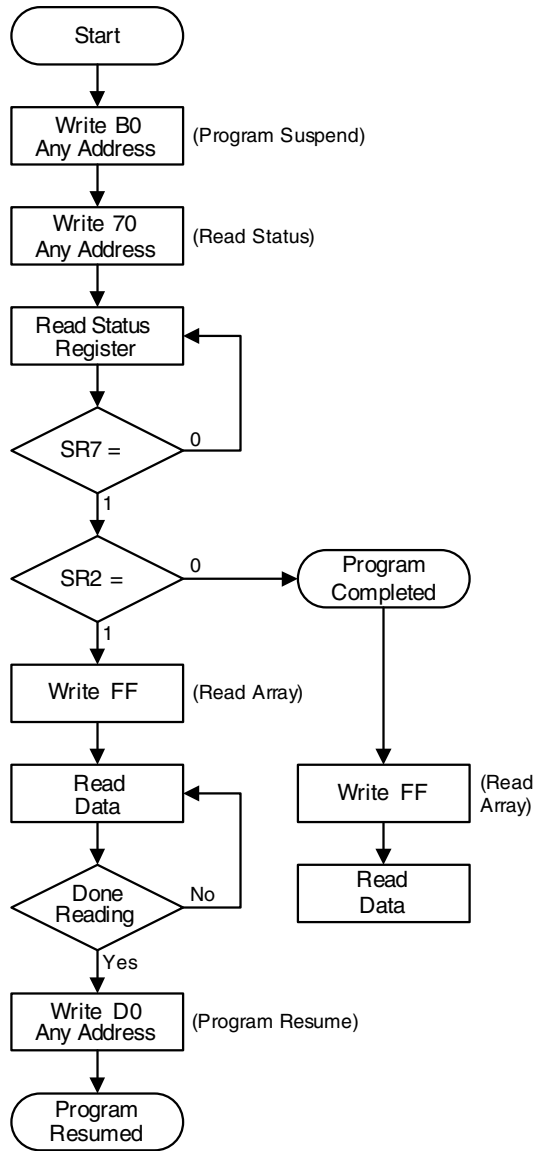


8. Full Status Check Procedure

| Bus Operation | Command | Comments |
|---------------|---------|-------------------------------------------------------|
| Idle | None | Check SR3: 1 = V_{PP} Error |
| Idle | None | Check SR4: 1 = Data Program Error |
| Idle | None | Check SR1: 1 = Sector locked; operation aborted |

SR3 MUST be cleared before the Write State Machine allows further program attempts.
If an error is detected, clear the status register before continuing operations – only the Clear Status Register command clears the status register error bits.

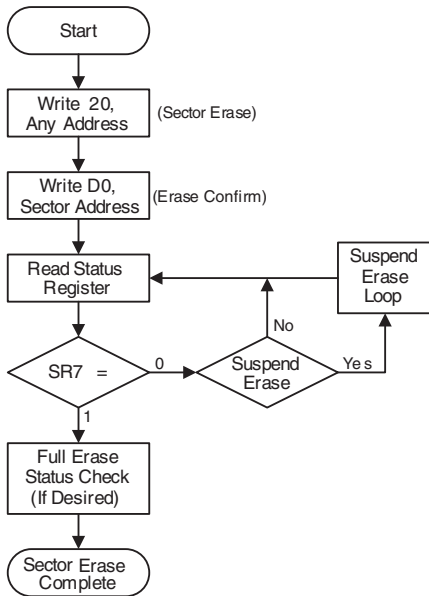
9. Program Suspend/Resume Flowchart



10. Program Suspend/Resume Procedure

| Bus Operation | Command | Comments |
|---------------|-----------------|-----------------------------------------------------------------------------------------------------------------|
| Write | Program Suspend | Data = B0 Addr = Any address |
| Write | Read Status | Data = 70 Addr = Any address |
| Read | None | Status register data: Toggle \overline{CE} or \overline{OE} to update status register Addr = Any address |
| Idle | None | Check SR7 1 = WSM Ready 0 = WSM Busy |
| Idle | None | Check SR2 1 = Program suspended 0 = Program completed |
| Write | Read Array | Data = FF Addr = Any address |
| Read | None | Read data from any word in the memory |
| Write | Program Resume | Data = D0 Addr = Any address |

11. Sector Erase Flowchart

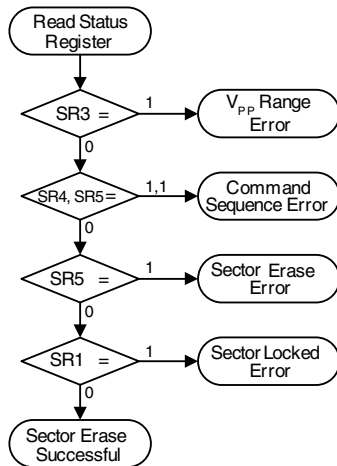


12. Sector Erase Procedure

| Bus Operation | Command | Comments |
|---------------|--------------------|------------------------------------------------------------------------------------------------|
| Write | Sector Erase Setup | Data = 20 Addr = Any address |
| Write | Erase Confirm | Data = D0 Addr = Sector to be erased (SA) |
| Read | None | Status register data: Toggle \overline{CE} or \overline{OE} to update status register data |
| Idle | None | Check SR7 1 = WSM Ready 0 = WSM Busy |

Repeat for subsequent sector erasures.
Full status register check can be done after each sector erase, or after a sequence of sector erasures.
Write FF after the last operation to enter read mode.

13. Full Erase Status Check Flowchart

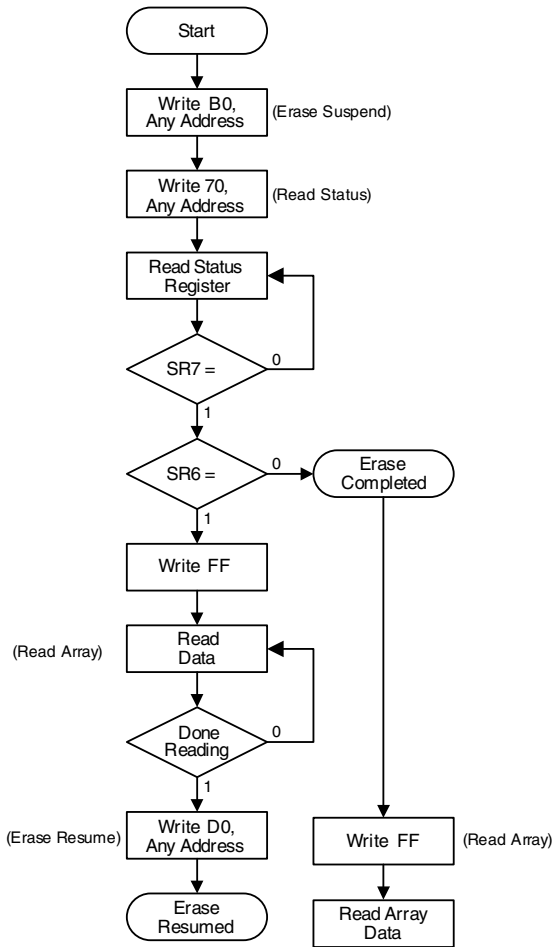


14. Full Erase Status Check Procedure

| Bus Operation | Command | Comments |
|---------------|---------|--------------------------------------------------------------------|
| Idle | None | Check SR3: 1 = V_{PP} Range Error |
| Idle | None | Check SR4, SR5: Both 1 = Command Sequence Error |
| Idle | None | Check SR5: 1 = Sector Erase Error |
| Idle | None | Check SR1: 1 = Attempted erase of locked sector; erase aborted. |

SR1, SR3 must be cleared before the Write State Machine allows further erase attempts.
Only the Clear Status Register command clears SR1, SR3, SR4, SR5.
If an error is detected, clear the status register before attempting an erase retry or other error recovery.

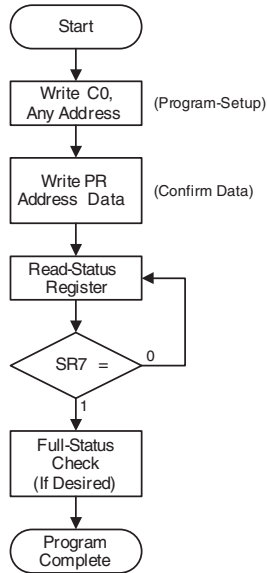
15. Erase Suspend/Resume Flowchart



16. Erase Suspend/Resume Procedure

| Bus Operation | Command | Comments |
|---------------|-----------------|-----------------------------------------------------------------------------------------------------------------|
| Write | Erase Suspend | Data = B0 Addr = Any address |
| Write | Read Status | Data = 70 Addr = Any address |
| Read | None | Status register data: Toggle \overline{CE} or \overline{OE} to update status register Addr = Any address |
| Idle | None | Check SR7 1 = WSM Ready 0 = WSM Busy |
| Idle | None | Check SR6 1 = Erase suspended 0 = Erase completed |
| Write | Read or Program | Data = FF or 40 Addr = Any address |
| Read or Write | None | Read or program data from/to sector other than the one being erased |
| Write | Program Resume | Data = D0 Addr = Any address |

17. Protection Register Programming Flowchart



18. Protection Register Programming Procedure

| Bus Operation | Command | Comments |
|---------------|--------------------|------------------------------------------------------------------------------------------------|
| Write | Program PR Setup | Data = C0 Addr = Any address |
| Write | Protection Program | Data = Data to Program Addr = Location to Program |
| Read | None | Status register data: Toggle \overline{CE} or \overline{OE} to update status register data |
| Idle | None | Check SR7 1 = WSM Ready 0 = WSM Busy |

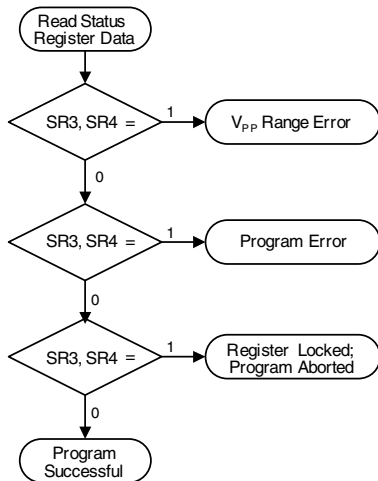
Program Protection Register operation addresses must be within the protection register address space. Addresses outside this space will return an error.

Repeat for subsequent programming operations.

Full status register check can be done after each program, or after a sequence of program operations.

Write FF after the last operation to return to the Read mode.

19. Full Status Check Flowchart



20. Full Status Check Procedure

| Bus Operation | Command | Comments |
|---------------|---------|-------------------------------------------------------------------|
| Idle | None | Check SR1, SR3, SR4: 0,1,1 = V_{PP} Range Error |
| Idle | None | Check SR1, SR3, SR4: 0,0,1 = Programming Error |
| Idle | None | Check SR1, SR3, SR4: 1, 0,1 = Sector locked; operation aborted |

SR3 must be cleared before the Write State Machine allows further program attempts.

Only the Clear Status Register command clears SR1, SR3, SR4.

If an error is detected, clear the status register before attempting a program retry or other error recovery.

21. Command Definition Table

| Command Sequence | Bus Cycles | 1st Bus Cycle | | 2nd Bus Cycle | | 3rd Bus Cycle | |
|-------------------------------------|------------|---------------|-------|---------------------|---------------------------------|---------------|------------------|
| | | Addr | Data | Addr | Data | Addr | Data |
| Read | 1 | XX | FF | | | | |
| Sector Erase/Confirm | 2 | XX | 20 | SA ⁽²⁾ | D0 | | |
| Word Program | 2 | XX | 40/10 | Addr | D _{IN} | | |
| Dual-word Program ⁽³⁾ | 3 | XX | E0 | Addr0 | D _{IN0} | Addr1 | D _{IN1} |
| Erase/Program Suspend | 1 | XX | B0 | | | | |
| Erase/Program Resume | 1 | XX | D0 | | | | |
| Product ID Entry | 1 | XX | 90 | | | | |
| Sector Softlock | 2 | XX | 60 | SA ⁽²⁾ | 01 | | |
| Sector Hardlock | 2 | XX | 60 | SA ⁽²⁾ | 2F | | |
| Sector Unlock | 2 | XX | 60 | SA ⁽²⁾ | D0 | | |
| Read Status Register | 2 | XX | 70 | XX | D _{OUT} ⁽⁴⁾ | | |
| Clear Status Register | 1 | XX | 50 | | | | |
| Program Protection Register | 2 | XX | C0 | Addr ⁽⁵⁾ | D _{IN} | | |
| Lock Protection Register – Sector B | 2 | XX | C0 | 80 | FFFD | | |
| Status of Sector B Protection | 2 | XX | 90 | 80 | D _{OUT} ⁽⁶⁾ | | |
| CFI Query | 1 | XX | 98 | | | | |

- Notes:
1. The DATA FORMAT shown for each bus cycle is as follows; I/O7 - I/O0 (Hex). I/O15 - I/O8 are don't care. The ADDRESS FORMAT shown for each bus cycle is as follows: A7 - A0 (Hex). Address A20 through A8 are don't care.
 2. SA = sector address. Any word address within a sector can be used to designate the sector address (see pages 17 - 20 for details).
 3. This fast programming option enables the user to program two words in parallel only when V_{PP} = 9.5V. The addresses, Addr0 and Addr1, of the two words, D_{IN0} and D_{IN1}, must only differ in address A0. This command should be used during manufacturing purposes only.
 4. The status register bits are output on I/O7 - I/O0.
 5. Any addresses within the user programmable protection register region. Address locations are shown on "Protection Register Addressing Table" on page 16.
 6. If data bit D1 is "0", sector B is locked. If data bit D1 is "1", sector B can be reprogrammed.

22. Absolute Maximum Ratings*

| | |
|---------------------------------------------------------------------------|---------------------------------|
| Temperature under Bias | -55°C to +125°C |
| Storage Temperature..... | -65°C to +150°C |
| All Input Voltages (including NC Pins) with Respect to Ground | -0.6V to +6.25V |
| All Output Voltages with Respect to Ground | -0.6V to V _{CC} + 0.6V |
| Voltage on V _{PP} with Respect to Ground | -0.6V to +10.0V |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

23. Protection Register Addressing Table

| Address | Use | Sector | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|---------|---------|--------|----|----|----|----|----|----|----|----|
| 81 | Factory | A | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| 82 | Factory | A | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 83 | Factory | A | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 84 | Factory | A | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| 85 | User | B | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 |
| 86 | User | B | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| 87 | User | B | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 |
| 88 | User | B | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Note: All address lines not specified in the above table must be "0" when accessing the protection register, i.e., A20 - A8 = 0.

24. AT49BV320D Sector Address Table

| Sector | Size (Bytes/Words) | Address Range (A20 - A0) |
|--------|--------------------|--------------------------|
| SA0 | 8K/4K | 00000 - 00FFF |
| SA1 | 8K/4K | 01000 - 01FFF |
| SA2 | 8K/4K | 02000 - 02FFF |
| SA3 | 8K/4K | 03000 - 03FFF |
| SA4 | 8K/4K | 04000 - 04FFF |
| SA5 | 8K/4K | 05000 - 05FFF |
| SA6 | 8K/4K | 06000 - 06FFF |
| SA7 | 8K/4K | 07000 - 07FFF |
| SA8 | 64K/32K | 08000 - 0FFFF |
| SA9 | 64K/32K | 10000 - 17FFF |
| SA10 | 64K/32K | 18000 - 1FFFF |
| SA11 | 64K/32K | 20000 - 27FFF |
| SA12 | 64K/32K | 28000 - 2FFFF |
| SA13 | 64K/32K | 30000 - 37FFF |
| SA14 | 64K/32K | 38000 - 3FFFF |
| SA15 | 64K/32K | 40000 - 47FFF |
| SA16 | 64K/32K | 48000 - 4FFFF |
| SA17 | 64K/32K | 50000 - 57FFF |
| SA18 | 64K/32K | 58000 - 5FFFF |
| SA19 | 64K/32K | 60000 - 67FFF |
| SA20 | 64K/32K | 68000 - 6FFFF |
| SA21 | 64K/32K | 70000 - 77FFF |
| SA22 | 64K/32K | 78000 - 7FFFF |
| SA23 | 64K/32K | 80000 - 87FFF |
| SA24 | 64K/32K | 88000 - 8FFFF |
| SA25 | 64K/32K | 90000 - 97FFF |
| SA26 | 64K/32K | 98000 - 9FFFF |
| SA27 | 64K/32K | A0000 - A7FFF |
| SA28 | 64K/32K | A8000 - AFFFF |
| SA29 | 64K/32K | B0000 - B7FFF |
| SA30 | 64K/32K | B8000 - BFFFF |
| SA31 | 64K/32K | C0000 - C7FFF |
| SA32 | 64K/32K | C8000 - CFFFF |
| SA33 | 64K/32K | D0000 - D7FFF |
| SA34 | 64K/32K | D8000 - DFFFF |
| SA35 | 64K/32K | E0000 - E7FFF |
| SA36 | 64K/32K | E8000 - EFFFF |
| SA37 | 64K/32K | F0000 - F7FFF |



24. AT49BV320D Sector Address Table (Continued)

| Sector | Size (Bytes/Words) | Address Range (A20 - A0) |
|--------|--------------------|--------------------------|
| SA38 | 64K/32K | F8000 - FFFFF |
| SA39 | 64K/32K | 100000 - 107FFF |
| SA40 | 64K/32K | 108000 - 10FFFF |
| SA41 | 64K/32K | 110000 - 117FFF |
| SA42 | 64K/32K | 118000 - 11FFFF |
| SA43 | 64K/32K | 120000 - 127FFF |
| SA44 | 64K/32K | 128000 - 12FFFF |
| SA45 | 64K/32K | 130000 - 137FFF |
| SA46 | 64K/32K | 138000 - 13FFFF |
| SA47 | 64K/32K | 140000 - 147FFF |
| SA48 | 64K/32K | 148000 - 14FFFF |
| SA49 | 64K/32K | 150000 - 157FFF |
| SA50 | 64K/32K | 158000 - 15FFFF |
| SA51 | 64K/32K | 160000 - 167FFF |
| SA52 | 64K/32K | 168000 - 16FFFF |
| SA53 | 64K/32K | 170000 - 177FFF |
| SA54 | 64K/32K | 178000 - 17FFFF |
| SA55 | 64K/32K | 180000 - 187FFF |
| SA56 | 64K/32K | 188000 - 18FFFF |
| SA57 | 64K/32K | 190000 - 197FFF |
| SA58 | 64K/32K | 198000 - 19FFFF |
| SA59 | 64K/32K | 1A0000 - 1A7FFF |
| SA60 | 64K/32K | 1A8000 - 1AFFFF |
| SA61 | 64K/32K | 1B0000 - 1B7FFF |
| SA62 | 64K/32K | 1B8000 - 1BFFFF |
| SA63 | 64K/32K | 1C0000 - 1C7FFF |
| SA64 | 64K/32K | 1C8000 - 1CFFFF |
| SA65 | 64K/32K | 1D0000 - 1D7FFF |
| SA66 | 64K/32K | 1D8000 - 1DFFFF |
| SA67 | 64K/32K | 1E0000 - 1E7FFF |
| SA68 | 64K/32K | 1E8000 - 1EFFFF |
| SA69 | 64K/32K | 1F0000 - 1F7FFF |
| SA70 | 64K/32K | 1F8000 - 1FFFFF |

25. AT49BV320DT – Sector Address Table

| Sector | Size (Bytes/Words) | Address Range (A20 - A0) |
|--------|--------------------|--------------------------|
| SA0 | 64K/32K | 00000 - 07FFF |
| SA1 | 64K/32K | 08000 - 0FFFF |
| SA2 | 64K/32K | 10000 - 17FFF |
| SA3 | 64K/32K | 18000 - 1FFFF |
| SA4 | 64K/32K | 20000 - 27FFF |
| SA5 | 64K/32K | 28000 - 2FFFF |
| SA6 | 64K/32K | 30000 - 37FFF |
| SA7 | 64K/32K | 38000 - 3FFFF |
| SA8 | 64K/32K | 40000 - 47FFF |
| SA9 | 64K/32K | 48000 - 4FFFF |
| SA10 | 64K/32K | 50000 - 57FFF |
| SA11 | 64K/32K | 58000 - 5FFFF |
| SA12 | 64K/32K | 60000 - 67FFF |
| SA13 | 64K/32K | 68000 - 6FFFF |
| SA14 | 64K/32K | 70000 - 77FFF |
| SA15 | 64K/32K | 78000 - 7FFFF |
| SA16 | 64K/32K | 80000 - 87FFF |
| SA17 | 64K/32K | 88000 - 8FFFF |
| SA18 | 64K/32K | 90000 - 97FFF |
| SA19 | 64K/32K | 98000 - 9FFFF |
| SA20 | 64K/32K | A0000 - A7FFF |
| SA21 | 64K/32K | A8000 - AFFFF |
| SA22 | 64K/32K | B0000 - B7FFF |
| SA23 | 64K/32K | B8000 - BFFFF |
| SA24 | 64K/32K | C0000 - C7FFF |
| SA25 | 64K/32K | C8000 - CFFFF |
| SA26 | 64K/32K | D0000 - D7FFF |
| SA27 | 64K/32K | D8000 - DFFFF |
| SA28 | 64K/32K | E0000 - E7FFF |
| SA29 | 64K/32K | E8000 - EFFFF |
| SA30 | 64K/32K | F0000 - F7FFF |
| SA31 | 64K/32K | F8000 - FFFFF |
| SA32 | 64K/32K | 100000 - 107FFF |
| SA33 | 64K/32K | 108000 - 10FFFF |
| SA34 | 64K/32K | 110000 - 117FFF |
| SA35 | 64K/32K | 118000 - 11FFFF |
| SA36 | 64K/32K | 120000 - 127FFF |
| SA37 | 64K/32K | 128000 - 12FFFF |



25. AT49BV320DT – Sector Address Table (Continued)

| Sector | Size (Bytes/Words) | Address Range (A20 - A0) |
|--------|--------------------|--------------------------|
| SA38 | 64K/32K | 130000 - 137FFF |
| SA39 | 64K/32K | 138000 - 13FFFF |
| SA40 | 64K/32K | 140000 - 147FFF |
| SA41 | 64K/32K | 148000 - 14FFFF |
| SA42 | 64K/32K | 150000 - 157FFF |
| SA43 | 64K/32K | 158000 - 15FFFF |
| SA44 | 64K/32K | 160000 - 167FFF |
| SA45 | 64K/32K | 168000 - 16FFFF |
| SA46 | 64K/32K | 170000 - 177FFF |
| SA47 | 64K/32K | 178000 - 17FFFF |
| SA48 | 64K/32K | 180000 - 187FFF |
| SA49 | 64K/32K | 188000 - 18FFFF |
| SA50 | 64K/32K | 190000 - 197FFF |
| SA51 | 64K/32K | 198000 - 19FFFF |
| SA52 | 64K/32K | 1A0000 - 1A7FFF |
| SA53 | 64K/32K | 1A8000 - 1AFFFF |
| SA54 | 64K/32K | 1B0000 - 1B7FFF |
| SA55 | 64K/32K | 1B8000 - 1BFFFF |
| SA56 | 64K/32K | 1C0000 - 1C7FFF |
| SA57 | 64K/32K | 1C8000 - 1CFFFF |
| SA58 | 64K/32K | 1D0000 - 1D7FFF |
| SA59 | 64K/32K | 1D8000 - 1DFFFF |
| SA60 | 64K/32K | 1E0000 - 1E7FFF |
| SA61 | 64K/32K | 1E8000 - 1EFFFF |
| SA62 | 64K/32K | 1F0000 - 1F7FFF |
| SA63 | 8K/4K | 1F8000 - 1F8FFF |
| SA64 | 8K/4K | 1F9000 - 1F9FFF |
| SA65 | 8K/4K | 1FA000 - 1FAFFF |
| SA66 | 8K/4K | 1FB000 - 1FBFFF |
| SA67 | 8K/4K | 1FC000 - 1FCFFF |
| SA68 | 8K/4K | 1FD000 - 1FDFFF |
| SA69 | 8K/4K | 1FE000 - 1FEFFF |
| SA70 | 8K/4K | 1FF000 - 1FFFFF |

26. DC and AC Operating Range

| | | AT49BV320D(T)-70 |
|------------------------------|------|------------------|
| Operating Temperature (Case) | Ind. | -40°C - 85°C |
| V _{CC} Power Supply | | 2.65V to 3.6V |

27. Operating Modes

| Mode | CE | OE | WE | RESET | V _{PP} ⁽¹⁾ | Ai | I/O |
|---------------------------------|-----------------|------------------|-----------------|-----------------|----------------------------------|---------------------------------------------------|----------------------------------|
| Read | V _{IL} | V _{IL} | V _{IH} | V _{IH} | X ⁽²⁾ | Ai | D _{OUT} |
| Program/Erase ⁽³⁾ | V _{IL} | V _{IH} | V _{IL} | V _{IH} | V _{IHPP} ⁽⁴⁾ | Ai | D _{IN} |
| Standby/Program Inhibit | V _{IH} | X ⁽²⁾ | X | V _{IH} | X | X | High-Z |
| Program Inhibit | X | X | V _{IH} | V _{IH} | X | | |
| | X | V _{IL} | X | V _{IH} | X | | |
| | X | X | X | V _{IH} | V _{ILPP} ⁽⁵⁾ | | |
| Output Disable | X | V _{IH} | X | V _{IH} | X | | High-Z |
| Reset | X | X | X | V _{IL} | X | X | High-Z |
| Product Identification Software | | | | V _{IH} | | A0 = V _{IL} , A1 - A20 = V _{IL} | Manufacturer Code ⁽⁶⁾ |
| | | | | | | A0 = V _{IH} , A1 - A20 = V _{IL} | Device Code ⁽⁶⁾ |

Notes: 1. The VPP pin can be tied to V_{CC}. For faster program operations, V_{PP} can be set to 9.5V ± 0.5V.

2. X can be V_{IL} or V_{IH}.

3. Refer to AC programming waveforms on [page 26](#).

4. V_{IHPP} (min) = 1.65V.

5. V_{ILPP} (max) = 0.4V.

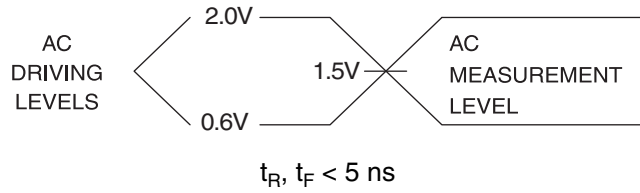
6. Manufacturer Code: 001FH, Device Code: 90C5H – AT49BV320D; 90C4H – AT49BV320DT

28. DC Characteristics

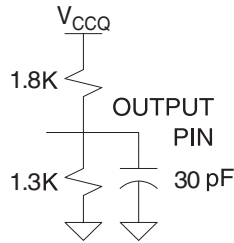
| Symbol | Parameter | Condition | Min | Typ | Max | Units |
|----------------|-------------------------------|---------------------------------------------|-----------------|-----|------|---------|
| I_{LI} | Input Load Current | $V_{IN} = 0V$ to V_{CC} | | | 2 | μA |
| I_{LO} | Output Leakage Current | $V_{IO} = 0V$ to V_{CC} | | | 2 | μA |
| I_{SB} | V_{CC} Standby Current CMOS | $\overline{CE} = V_{CC} - 0.3V$ to V_{CC} | | 15 | 25 | μA |
| $I_{CC}^{(1)}$ | V_{CC} Active Read Current | $f = 5$ MHz; $I_{OUT} = 0$ mA | | 10 | 15 | mA |
| I_{CC1} | V_{CC} Programming Current | | | | 25 | mA |
| I_{PP1} | V_{PP} Input Load Current | | | | 10 | μA |
| V_{IL} | Input Low Voltage | | | | 0.6 | V |
| V_{IH} | Input High Voltage | | $V_{CCQ} - 0.6$ | | | V |
| V_{OL} | Output Low Voltage | $I_{OL} = 2.1$ mA | | | 0.45 | V |
| V_{OH} | Output High Voltage | $I_{OH} = -100$ μA | $V_{CCQ} - 0.1$ | | | V |

Note: 1. In the erase mode, I_{CC} is 25 mA.

29. Input Test Waveforms and Measurement Level



30. Output Test Load



31. Pin Capacitance

f = 1 MHz, T = 25°C⁽¹⁾

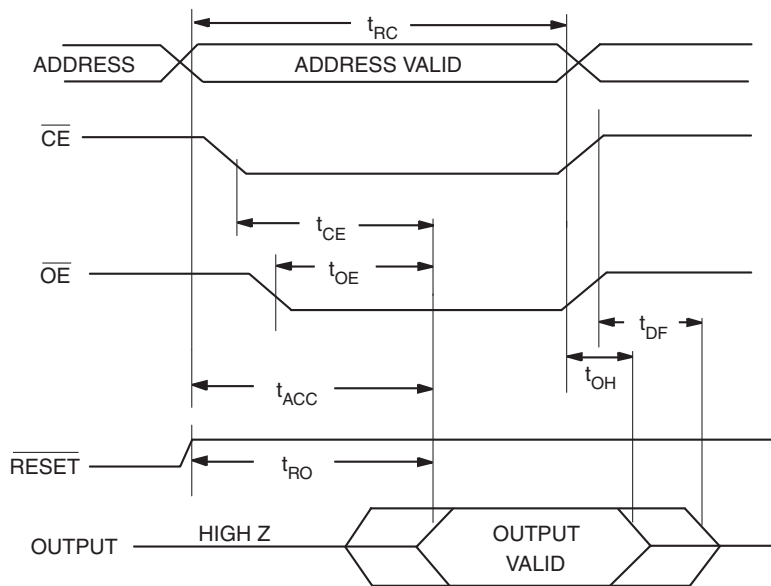
| Symbol | Typ | Max | Units | Conditions |
|------------------|-----|-----|-------|-----------------------|
| C _{IN} | 4 | 6 | pF | V _{IN} = 0V |
| C _{OUT} | 8 | 12 | pF | V _{OUT} = 0V |

Note: This parameter is characterized and is not 100% tested.

32. AC Read Characteristics

| Symbol | Parameter | AT49BV320D(T)-70 | | Units |
|-------------------|-----------------------------------------------------------------------------------------|------------------|-----|-------|
| | | Min | Max | |
| t_{RC} | Read Cycle Time | 70 | | ns |
| t_{ACC} | Address to Output Delay | | 70 | ns |
| $t_{CE}^{(1)}$ | \overline{CE} to Output Delay | | 70 | ns |
| $t_{OE}^{(2)}$ | \overline{OE} to Output Delay | 0 | 20 | ns |
| $t_{DF}^{(3)(4)}$ | \overline{CE} or \overline{OE} to Output Float | 0 | 25 | ns |
| t_{OH} | Output Hold from \overline{OE} , \overline{CE} or Address, whichever occurred first | 0 | | ns |
| t_{RO} | \overline{RESET} to Output Delay | | 100 | ns |

33. AC Read Waveforms⁽¹⁾⁽²⁾⁽³⁾⁽⁴⁾



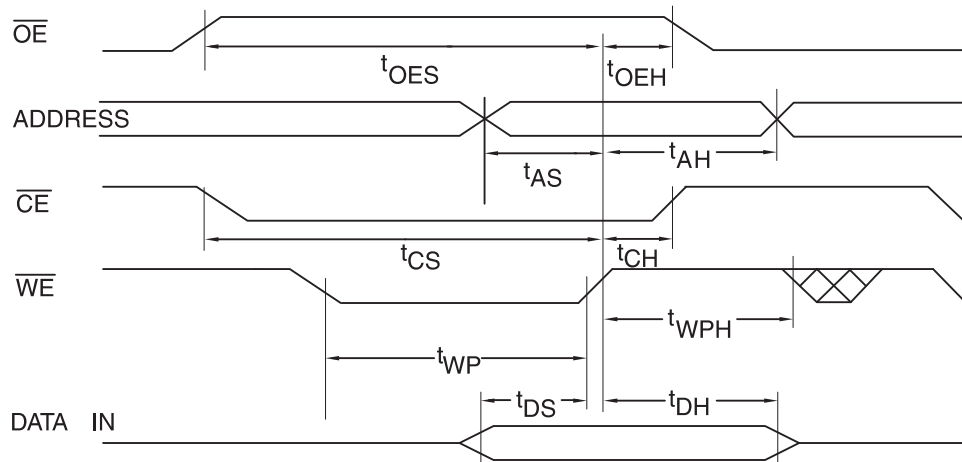
- Notes:
- \overline{CE} may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC} .
 - \overline{OE} may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of \overline{CE} without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC} .
 - t_{DF} is specified from \overline{OE} or \overline{CE} , whichever occurs first (CL = 5 pF).
 - This parameter is characterized and is not 100% tested.

34. AC Word Load Characteristics

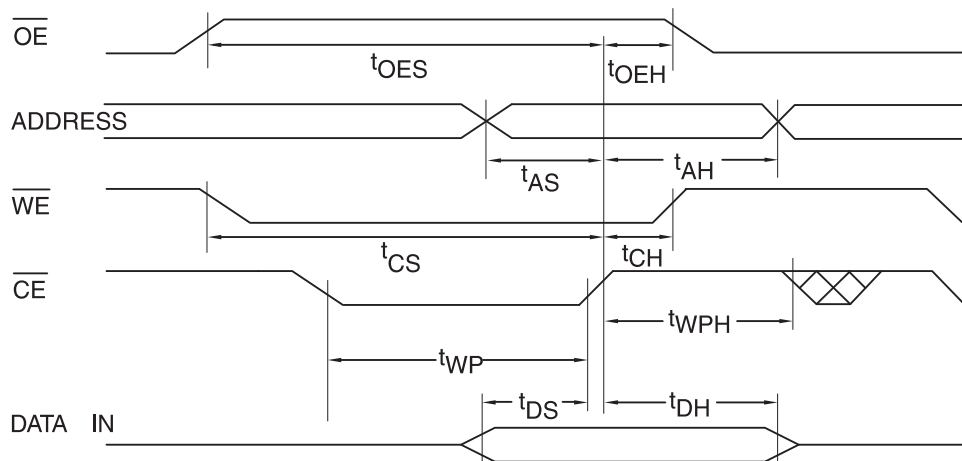
| Symbol | Parameter | Min | Max | Units |
|-------------------|----------------------------------------------------------|-----|-----|-------|
| t_{AS}, t_{OES} | Address, \overline{OE} Setup Time | 20 | | ns |
| t_{AH} | Address Hold Time | 0 | | ns |
| t_{CS} | Chip Select Setup Time | 0 | | ns |
| t_{CH} | Chip Select Hold Time | 0 | | ns |
| t_{WP} | Write Pulse Width (\overline{WE} or \overline{CE}) | 25 | | ns |
| t_{WPH} | Write Pulse Width High | 15 | | ns |
| t_{DS} | Data Setup Time | 25 | | ns |
| t_{DH}, t_{OEH} | Data, \overline{OE} Hold Time | 0 | | ns |

35. AC Word Load Waveforms

35.1 \overline{WE} Controlled



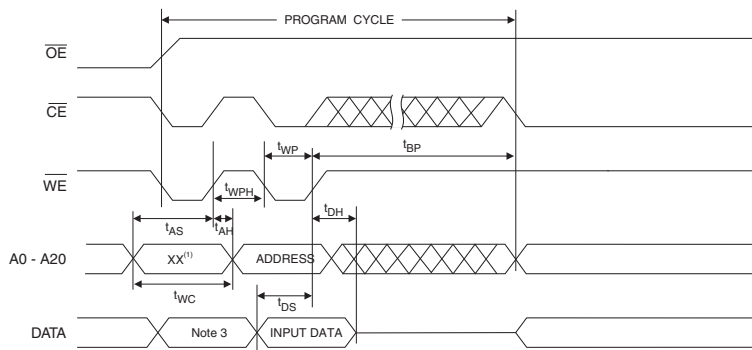
35.2 \overline{CE} Controlled



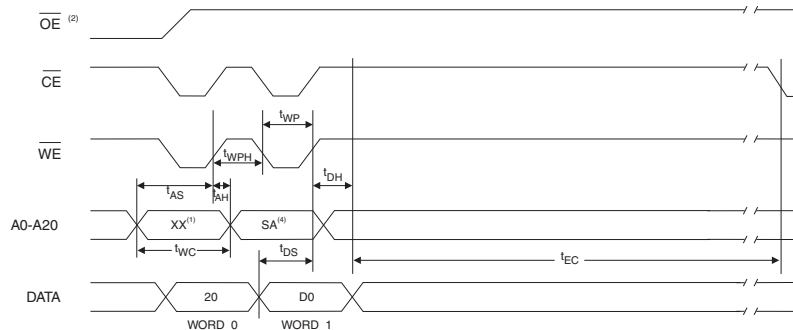
36. Program Cycle Characteristics

| Symbol | Parameter | Min | Typ | Max | Units |
|------------|------------------------------------------------|-----|-----|-----|---------------|
| t_{BP} | Word Programming Time | | 10 | 120 | μs |
| t_{BPD} | Word Programming Time in Dual Programming Mode | | 5 | 60 | μs |
| t_{AS} | Address Setup Time | 20 | | | ns |
| t_{AH} | Address Hold Time | 0 | | | ns |
| t_{DS} | Data Setup Time | 25 | | | ns |
| t_{DH} | Data Hold Time | 0 | | | ns |
| t_{WP} | Write Pulse Width | 25 | | | ns |
| t_{WPH} | Write Pulse Width High | 15 | | | ns |
| t_{WC} | Write Cycle Time | 70 | | | ns |
| t_{RP} | Reset Pulse Width | 500 | | | ns |
| t_{SEC1} | Sector Erase Cycle Time (4K Word Sectors) | | 0.1 | 2 | seconds |
| t_{SEC2} | Sector Erase Cycle Time (32K Word Sectors) | | 0.5 | 6.0 | seconds |
| t_{ES} | Erase Suspend Time | | | 15 | μs |
| t_{PS} | Program Suspend Time | | | 10 | μs |

37. Program Cycle Waveforms



38. Sector Erase Cycle Waveforms



- Notes:
1. Any address can be used to load the data.
 2. \overline{OE} must be high only when \overline{WE} and \overline{CE} are both low.
 3. The data can be 40H or 10H.
 4. The address depends on what sector is to be erased.

39. Common Flash Interface Definition Table

| Address | AT49BV320DT | AT49BV320D | Comments |
|---------|-------------|------------|-----------------------------------------------------|
| 10h | 0051h | 0051h | “Q” |
| 11h | 0052h | 0052h | “R” |
| 12h | 0059h | 0059h | “Y” |
| 13h | 0003h | 0003h | |
| 14h | 0000h | 0000h | |
| 15h | 0041h | 0041h | |
| 16h | 0000h | 0000h | |
| 17h | 0000h | 0000h | |
| 18h | 0000h | 0000h | |
| 19h | 0000h | 0000h | |
| 1Ah | 0000h | 0000h | |
| 1Bh | 0027h | 0027h | VCC min write/erase |
| 1Ch | 0036h | 0036h | VCC max write/erase |
| 1Dh | 0090h | 0090h | VPP min voltage |
| 1Eh | 00A0h | 00A0h | VPP max voltage |
| 1Fh | 0004h | 0004h | Typ word write – 10 μs |
| 20h | 0002h | 0002h | Typ dual word program time – 5 μs |
| 21h | 0009h | 0009h | Typ sector erase, 500 ms |
| 22h | 0000h | 0000h | Typ chip erase, not supported |
| 23h | 0004h | 0004h | Max word write/typ time |
| 24h | 0004h | 0004h | Max dual word program time/typ time |
| 25h | 0004h | 0004h | Max sector erase/typ sector erase |
| 26h | 0000h | 0000h | Max chip erase/ typ chip erase |
| 27h | 0016h | 0016h | Device size |
| 28h | 0001h | 0001h | x16 device |
| 29h | 0000h | 0000h | x16 device |
| 2Ah | 0002h | 0002h | Maximum number of bytes in multiple byte write = 4 |
| 2Bh | 0000h | 0000h | Maximum number of bytes in multiple byte write = 4 |
| 2Ch | 0002h | 0002h | 2 regions, x = 2 |
| 2Dh | 003Eh | 0007h | 64K bytes, Y = 62 (Top); 8K bytes, Y = 7 (Bottom) |
| 2Eh | 0000h | 0000h | 64K bytes, Y = 62 (Top); 8K bytes, Y = 7 (Bottom) |
| 2Fh | 0000h | 0020h | 64K bytes, Z = 256 (Top); 8K bytes, Z = 32 (Bottom) |
| 30h | 0001h | 0000h | 64K bytes, Z = 256 (Top); 8K bytes, Z = 32 (Bottom) |
| 31h | 0007h | 003Eh | 8K bytes, Y = 7 (Top); 64K bytes, Y = 62 (Bottom) |
| 32h | 0000h | 0000h | 8K bytes, Y = 7 (Top); 64K bytes, Y = 62 (Bottom) |
| 33h | 0020h | 0000h | 8K bytes, Z = 32 (Top); 64K bytes, Z = 256 (Bottom) |
| 34h | 0000h | 0001h | 8K bytes, Z = 32 (Top); 64K bytes, Z = 256 (Bottom) |

39. Common Flash Interface Definition Table (Continued)

| Address | AT49BV320DT | AT49BV320D | Comments |
|---------------------------------------|-------------|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VENDOR SPECIFIC EXTENDED QUERY | | | |
| 41h | 0050h | 0050h | "P" |
| 42h | 0052h | 0052h | "R" |
| 43h | 0049h | 0049h | "I" |
| 44h | 0031h | 0031h | Major version number, ASCII |
| 45h | 0030h | 0030h | Minor version number, ASCII |
| 46h | 0086h | 0086h | Bit 0 – chip erase supported, 0 – no, 1 – yes Bit 1 – erase suspend supported, 0 – no, 1 – yes Bit 2 – program suspend supported, 0 – no, 1 – yes Bit 3 – simultaneous operations supported, 0 – no, 1 – yes Bit 4 – burst mode read supported, 0 – no, 1 – yes Bit 5 – page mode read supported, 0 – no, 1 – yes Bit 6 – queued erase supported, 0 – no, 1 – yes Bit 7 – protection bits supported, 0 – no, 1 – yes |
| 47h | 0000h | 0001h | Bit 8 – top ("0") or bottom ("1") boot sector device undefined bits are "0" |
| 48h | 0000h | 0000h | Bit 0 – 4 word linear burst with wrap around, 0 – no, 1 – yes Bit 1 – 8 word linear burst with wrap around, 0 – no, 1 – yes Bit 2 – continuous burst, 0 - no, 1 - yes Undefined bits are "0" |
| 49h | 0000h | 0000h | Bit 0 – 4 word page, 0 – no, 1 – yes Bit 1 – 8 word page, 0 – no, 1 – yes Undefined bits are "0" |
| 4Ah | 0080h | 0080h | Location of protection register lock byte, the section's first byte |
| 4Bh | 0003h | 0003h | # of bytes in the factory prog section of prot register – 2*n |
| 4Ch | 0003h | 0003h | # of bytes in the user prog section of prot register – 2*n |

40. Ordering Information

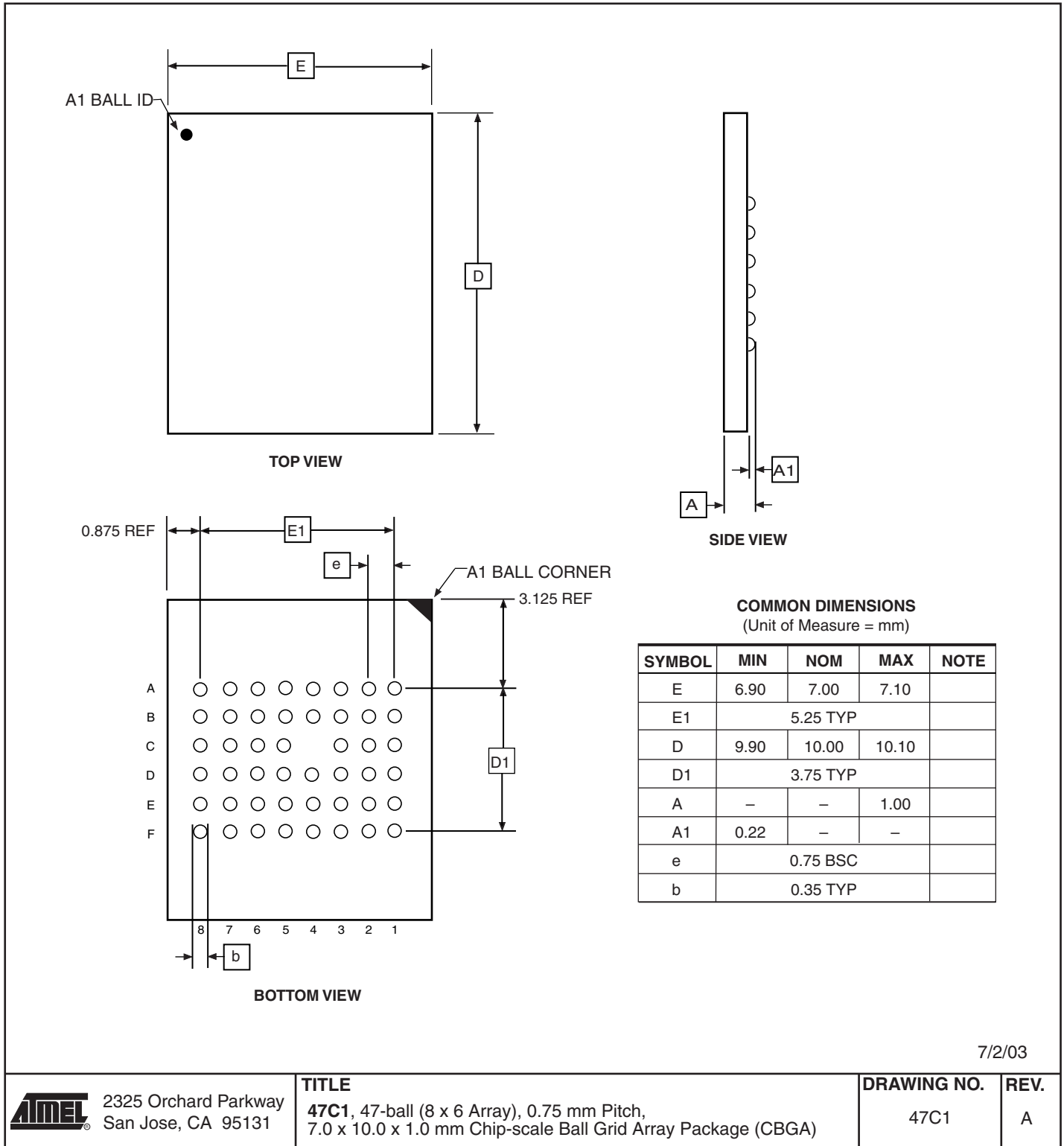
40.1 Green Package (Pb/Halide-free)

| t_{ACC} (ns) | I_{CC} (mA) | | Ordering Code | Package | Operation Range |
|-------------------|---------------|---------|--------------------------------------|-------------|------------------------------|
| | Active | Standby | | | |
| 70 | 25 | 0.025 | AT49BV320D-70CU AT49BV320D-70TU | 47C1 48T | Industrial (-40° to 85°C) |
| | | | AT49BV320DT-70CU AT49BV320DT-70TU | 47C1 48T | |

| Package Type | |
|--------------|-----------------------------------------------------------|
| 47C1 | 47-ball, Plastic Chip-Size Ball Grid Array Package (CBGA) |
| 48T | 48-lead, Plastic Thin Small Outline Package (TSOP) |

41. Packaging Information

41.1 47C1 – CBGA



7/2/03



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San Jose, CA 95131

TITLE

47C1, 47-ball (8 x 6 Array), 0.75 mm Pitch,
7.0 x 10.0 x 1.0 mm Chip-scale Ball Grid Array Package (CBGA)

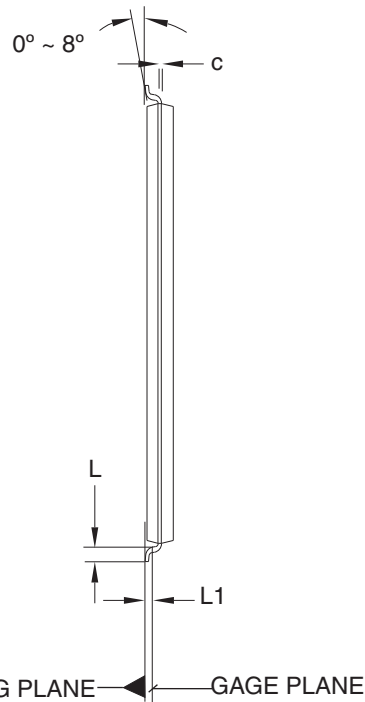
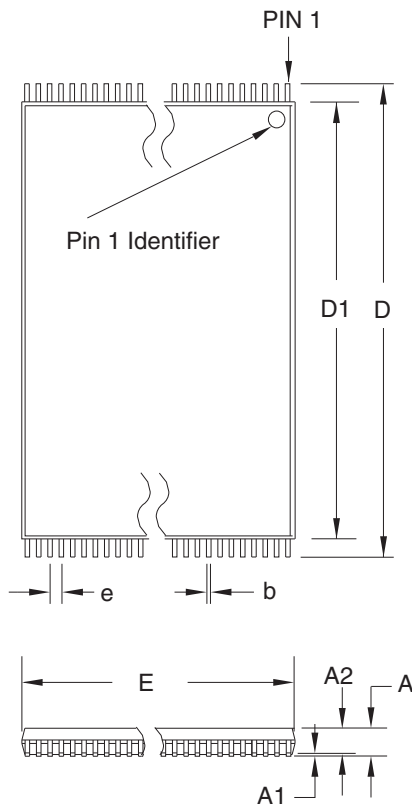
DRAWING NO.

47C1

REV.

A

41.2 48T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|------------|-------|-------|--------|
| A | – | – | 1.20 | |
| A1 | 0.05 | – | 0.15 | |
| A2 | 0.95 | 1.00 | 1.05 | |
| D | 19.80 | 20.00 | 20.20 | |
| D1 | 18.30 | 18.40 | 18.50 | Note 2 |
| E | 11.90 | 12.00 | 12.10 | Note 2 |
| L | 0.50 | 0.60 | 0.70 | |
| L1 | 0.25 BASIC | | | |
| b | 0.17 | 0.22 | 0.27 | |
| c | 0.10 | – | 0.21 | |
| e | 0.50 BASIC | | | |

- Notes:
1. This package conforms to JEDEC reference MO-142, Variation DD.
 2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
 3. Lead coplanarity is 0.10 mm maximum.

10/18/01



2325 Orchard Parkway
San Jose, CA 95131

TITLE

48T, 48-lead (12 x 20 mm Package) Plastic Thin Small Outline Package, Type I (TSOP)

DRAWING NO.

48T

REV.

B



42. Revision History

| Revision No. | History |
|-------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Revision A – Sept. 2005 | <ul style="list-style-type: none">• Initial Release |
| Revision B – Oct. 2005 | <ul style="list-style-type: none">• Added Top Boot version.• Added Sector Address Table for the AT49BV320DT.• Added CFI information for the AT49BV320DT.• Modified Program Suspend/Resume Procedure on page 11 to match the flow chart.• Modified Erase Suspend/Resume Procedure on page 13 to match the flow chart. |
| Revision C – Nov. 2005 | <ul style="list-style-type: none">• Added CBGA Package Option.• Changed the CFI values of addresses 20h & 24h to 0002h and 0004h, respectively. |
| Revision D – Feb. 2006 | <ul style="list-style-type: none">• Changed the AT49BV320DT CFI values of addresses 23h & 25h to 0004h and 0004h, respectively. |



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