



**THE DATASHEET OF  
CY7C136E-25JXCT**



**1K/2K × 8 Dual-Port Static RAM**

### Features

- True dual-ported memory cells, which allow simultaneous reads of the same memory location
- 1K/2K × 8 organization
- 0.35 micron complementary metal oxide semiconductor (CMOS) for optimum speed and power
- High speed access: 15 ns
- Low operating power: I<sub>CC</sub> = 110 mA (typical), Standby: I<sub>SB3</sub> = 0.05 mA (typical)
- Fully asynchronous operation
- Automatic power-down
- $\overline{\text{BUSY}}$  output flag to indicate access to the same location by both ports
- $\overline{\text{INT}}$  flag for port-to-port communication
- Available in 52-pin plastic leaded chip carrier (PLCC), 52-pin plastic quad flat package (PQFP)
- Pb-free packages available

### Functional Description

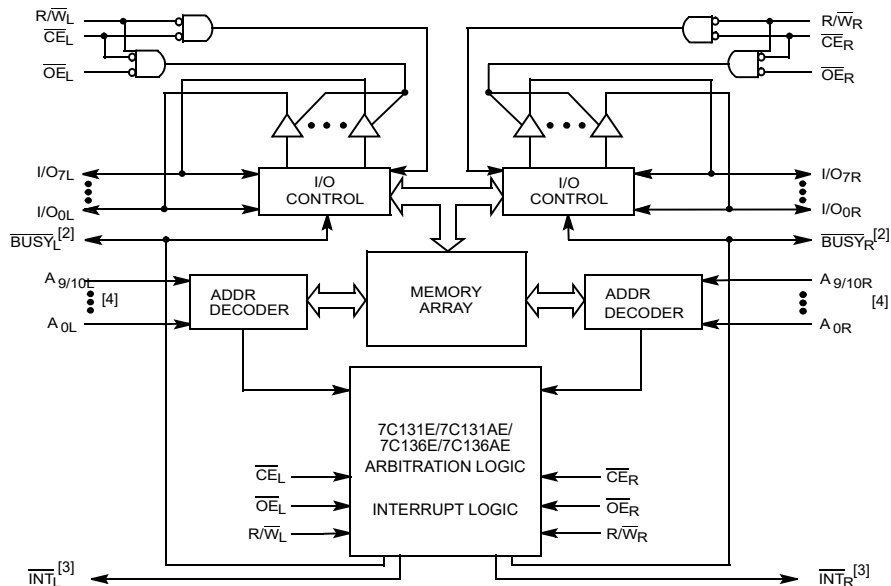
CY7C131E/CY7C131AE/CY7C136E/CY7C136AE are high-speed, low-power CMOS 1K/2K × 8 dual-port static RAMs. Two ports are provided permitting independent access to any location in memory. The CY7C131E/CY7C131AE/CY7C136E/CY7C136AE can be used as a standalone dual-port static RAM. It is the solution to applications requiring shared or buffered data, such as cache memory for DSP, bit-slice, or multiprocessor designs.

Each port has independent control pins; chip enable ( $\overline{\text{CE}}$ ), write enable (R/W), and output enable ( $\overline{\text{OE}}$ ). Two flags are provided on each port,  $\overline{\text{BUSY}}$  and  $\overline{\text{INT}}$ . The  $\overline{\text{BUSY}}$  flag signals that the port is trying to access the same location, which is currently being accessed by the other port. The  $\overline{\text{INT}}$  is an interrupt flag indicating that data is placed in a unique location<sup>[1]</sup>. The  $\overline{\text{BUSY}}$  and  $\overline{\text{INT}}$  flags are push pull outputs. An automatic power-down feature is controlled independently on each port by the chip enable (CE) pins.

The CY7C131E/CY7C131AE/CY7C136E/CY7C136AE are available in 52-pin Pb-free PLCC and 52-pin Pb-free PQFP.

For a complete list of related documentation, click [here](#).

### Logic Block Diagram



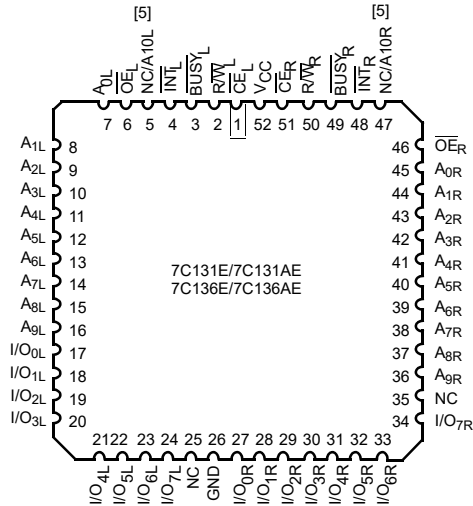
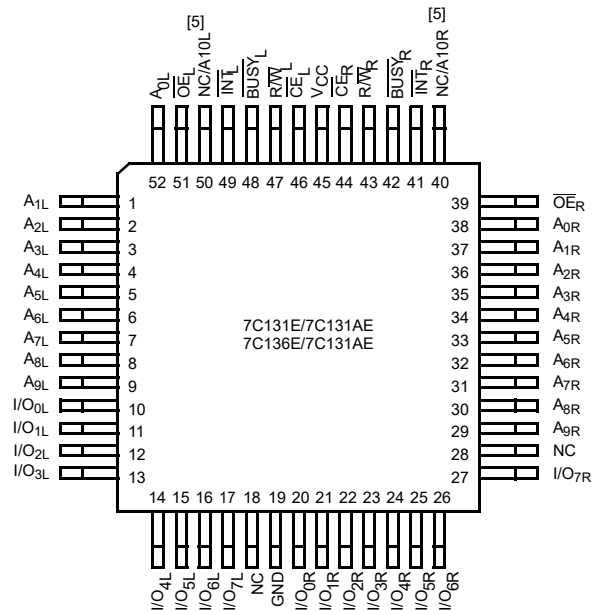
#### Notes

1. Unique location used by interrupt flag: 1K × 8: Left port reads from 3FE, Right port reads from 3FF; 2K × 8: Left port reads from 7FE, Right port reads from 7FF.
2.  $\overline{\text{BUSY}}$  is a push-pull output. No pull-up resistor required.
3.  $\overline{\text{INT}}$ : push-pull output. No pull-up resistor required.
4. 1K × 8: A0–A9, 2K × 8: A0–A10, address lines are for both left and right ports.

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## Pin Configurations

**Figure 1. 52-pin PLCC pinout (Top View)**

**Figure 2. 52-pin PQFP pinout (Top View)**


## Pin Definitions

Left Port	Right Port	Description
$\overline{CE}_L$	$\overline{CE}_R$	Chip Enable
$\overline{R/W}_L$	$\overline{R/W}_R$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
$A_{0L}-A_{9/10L}^{[5]}$	$A_{0R}-A_{9/10R}^{[5]}$	Address
$I/O_{0L}-I/O_{7L}$	$I/O_{0R}-I/O_{7R}$	Data Bus Input/Output
$\overline{INT}_L$	$\overline{INT}_R$	Interrupt Flag
$\overline{BUSY}_L$	$\overline{BUSY}_R$	Busy Flag
$V_{CC}$		Power
GND		Ground

## Selection Guide

Parameter	7C131E-15 7C131AE-15	7C131E-25 7C136E-25	7C131E-55 7C136E-55 7C136AE-55	Unit
Maximum Access Time	15	25	55	ns
Typical Operating Current	110	100	95	mA
Typical Standby Current for $I_{SB1}$ (both ports TTL level)	50	45	45	mA
Typical Standby Current for $I_{SB3}$ (Both ports CMOS level)	0.05	0.05	0.05	mA

**Note**

5. 1K × 8: A0–A9, 2K × 8: A0–A10, address lines are for both left and right ports.

## Maximum Ratings

Exceeding maximum ratings <sup>[6]</sup> may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C  
 Ambient temperature  
 with power applied ..... -55 °C to +125 °C  
 Supply voltage to ground potential ..... -0.3 V to +7.0 V  
 DC voltage applied to outputs  
 in High Z State ..... -0.5 V to +7.0 V  
 DC input voltage <sup>[7]</sup> ..... -0.5 V to +7.0 V

Output current into outputs (LOW) ..... 20 mA  
 Static discharge voltage ..... >1100 V  
 Latch up current ..... >200 mA

## Operating Range

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0 °C to +70 °C	5 V ± 10%
Industrial	-40 °C to +85 °C	5 V ± 10%

## Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	7C131E-15 7C131AE-15			7C131E-25 7C136E-25			7C131E-55 7C136E-55 7C136AE-55			Unit		
			Min	Typ <sup>[8]</sup>	Max	Min	Typ <sup>[8]</sup>	Max	Min	Typ <sup>[8]</sup>	Max			
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> = Min, I <sub>OH</sub> = -4.0 mA	2.4	-	-	2.4	-	-	2.4	-	-	V		
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> = Min, I <sub>OL</sub> = 4.0 mA	-	-	0.4	-	-	0.4	-	-	0.4	V		
V <sub>IH</sub>	Input HIGH Voltage		2.2	-	-	2.2	-	-	2.2	-	-	V		
V <sub>IL</sub>	Input LOW Voltage		-	-	0.8	-	-	0.8	-	-	0.8	V		
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output disabled	-20	-	+20	-20	-	+20	-20	-	+20	µA		
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA Outputs disabled	Commercial		Industrial		Commercial		Industrial		Commercial		Industrial	
I <sub>SB1</sub>	Standby Current, Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R \geq V_{IH}$ , f = f <sub>MAX</sub> <sup>[9]</sup>	-	50	70	-	45	65	-	45	65	mA		
I <sub>SB2</sub>	Standby Current, One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R \geq V_{IH}$ , Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[9]</sup>	-	120	180	-	110	160	-	110	160	mA		
I <sub>SB3</sub>	Standby Current, Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC} - 0.2$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, f = 0	-	0.05	0.5	-	0.05	0.5	-	0.05	0.5	mA		
I <sub>SB4</sub>	Standby Current, One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R \geq V_{CC} - 0.2$ V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2 V or V <sub>IN</sub> ≤ 0.2 V, Active Port Outputs Open, f = f <sub>MAX</sub> <sup>[9]</sup>	-	110	160	-	100	140	-	100	140	mA		

### Notes

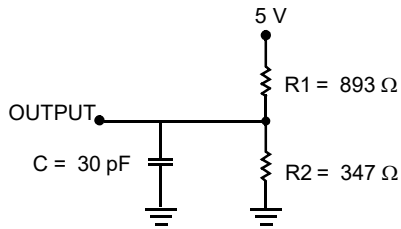
- The voltage on any I/O pin cannot exceed the power pin during power-up.
- Pulse width < 20 ns.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC</sub>(typ.), T<sub>A</sub> = 25 °C.
- At f = f<sub>MAX</sub>, address and data inputs are cycling at the maximum frequency of read cycle of 1/t<sub>RC</sub> and using AC Test Waveforms input levels of GND to 3 V.

## Capacitance

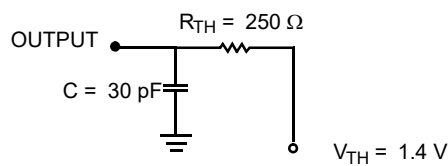
Parameter <sup>[10]</sup>	Description	Test Conditions	Max	Unit
$C_{IN}$	Input capacitance	$T_A = 25\text{ }^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 5.0\text{ V}$	15	pF
$C_{OUT}$	Output capacitance		10	pF

## AC Test Loads and Waveforms

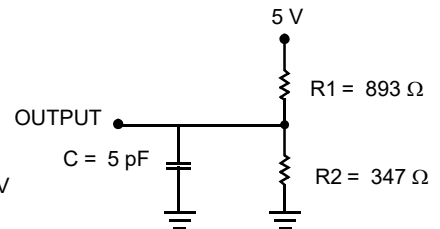
Figure 3. AC Test Loads and Waveforms



(a) Normal Load (Load 1)

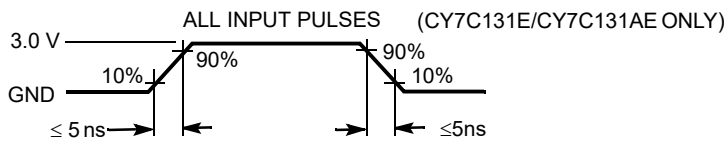


(b) Thévenin Equivalent (Load 1)



(c) Three-State Delay (Load 2)

(Used for  $t_{LZ}$ ,  $t_{HZ}$ ,  $t_{HZWE}$ , and  $t_{LZWE}$  including scope and jig)



### Note

10. Tested initially and after any design or process changes that may affect these parameters.

## Switching Characteristics

Over the Operating Range

Parameter <sup>[11]</sup>	Description	7C131E-15/7C131AE-15		7C131E-25/7C136E-25		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read cycle time	15	–	25	–	ns
$t_{AA}$	Address to data valid <sup>[12]</sup>	–	15	–	25	ns
$t_{OHA}$	Data hold from Address change	3	–	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid <sup>[12]</sup>	–	15	–	25	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid <sup>[12]</sup>	–	10	–	15	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[13, 14, 15]</sup>	3	–	3	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[13, 14, 15]</sup>	–	10	–	15	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[13, 14, 15]</sup>	3	–	5	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[13, 14, 15]</sup>	–	10	–	15	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up <sup>[13]</sup>	0	–	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down <sup>[13]</sup>	–	15	–	25	ns
<b>Write Cycle <sup>[16]</sup></b>						
$t_{WC}$	Write cycle time	15	–	25	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	12	–	20	–	ns
$t_{AW}$	Address setup to write end	12	–	20	–	ns
$t_{HA}$	Address hold from write end	0	–	0	–	ns
$t_{SA}$	Address setup to write start	0	–	0	–	ns
$t_{PWE}$	R/ $\overline{W}$ pulse width	10	–	12	–	ns
$t_{SD}$	Data setup to write end	10	–	15	–	ns
$t_{HD}$	Data hold from write end	0	–	0	–	ns
$t_{HZWE}^{[13]}$	R/ $\overline{W}$ LOW to High Z <sup>[15]</sup>	–	10	–	15	ns
$t_{LZWE}^{[13]}$	R/ $\overline{W}$ HIGH to Low Z <sup>[15]</sup>	3	–	3	–	ns

### Notes

- Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V and output loading of the specified  $I_{OL}/I_{OH}$  and 30 pF load capacitance.
- AC Test Conditions use  $V_{OH} = 1.6$  V and  $V_{OL} = 1.4$  V.
- This parameter is guaranteed but not tested.
- At any given temperature and voltage condition for any given device,  $t_{HZCE}$  is less than  $t_{LZCE}$  and  $t_{HZOE}$  is less than  $t_{LZOE}$ .
- Parameters  $t_{LZCE}$ ,  $t_{LZWE}$ ,  $t_{HZOE}$ ,  $t_{LZOE}$ ,  $t_{HZCE}$  and  $t_{HZWE}$  are tested with  $C_L = 5$  pF as in part (c) of Figure 3 on page 5. Transition is measured  $\pm 500$  mV from steady state voltage.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and R/ $\overline{W}$  LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

## Switching Characteristics (continued)

Over the Operating Range

Parameter <sup>[11]</sup>	Description	7C131E-15/7C131AE-15		7C131E-25/7C136E-25		Unit
		Min	Max	Min	Max	
<b>Busy/Interrupt Timing <sup>[17]</sup></b>						
t <sub>BLA</sub>	BUSY LOW from Address match	–	15	–	20	ns
t <sub>BHA</sub>	BUSY HIGH from Address mismatch <sup>[18]</sup>	–	15	–	20	ns
t <sub>BLC</sub>	BUSY LOW from CE LOW	–	15	–	20	ns
t <sub>BHC</sub>	BUSY HIGH from CE HIGH <sup>[18]</sup>	–	15	–	20	ns
t <sub>PS</sub>	Port setup for priority	5	–	5	–	ns
t <sub>BDD</sub>	BUSY HIGH to valid data	–	15	–	25	ns
t <sub>DDD</sub>	Write data valid to read data valid <sup>[19]</sup>	–	25	–	30	ns
t <sub>WDD</sub>	Write pulse to data delay <sup>[19]</sup>	–	30	–	45	ns
<b>Interrupt Timing</b>						
t <sub>WINS</sub>	R/W to INTERRUPT set time	–	15	–	25	ns
t <sub>EINS</sub>	CE to INTERRUPT set time	–	15	–	25	ns
t <sub>INS</sub>	Address to INTERRUPT set time	–	15	–	25	ns
t <sub>OINR</sub>	OE to INTERRUPT reset time <sup>[18]</sup>	–	15	–	25	ns
t <sub>EINR</sub>	CE to INTERRUPT reset time <sup>[18]</sup>	–	15	–	25	ns
t <sub>INR</sub>	Address to INTERRUPT reset time <sup>[18]</sup>	–	15	–	25	ns

### Notes

17. Test conditions used are Load 2.

18. These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.

19. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:  
 BUSY on Port B goes HIGH.  
 Port B's address toggled.  
 CE for Port B is toggled.

## Switching Characteristics

Over the Operating Range

Parameter	Description	7C131E-55/7C136E-55/ 7C136AE-55		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{RC}$	Read cycle time	55	–	ns
$t_{AA}$	Address to data valid <sup>[20]</sup>	–	55	ns
$t_{OHA}$	Data hold from Address change	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid <sup>[20]</sup>	–	55	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid <sup>[20]</sup>	–	25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to Low Z <sup>[20, 21, 22]</sup>	3	–	ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[20, 21, 22]</sup>	–	25	ns
$t_{LZCE}$	$\overline{CE}$ LOW to Low Z <sup>[20, 21, 22]</sup>	5	–	ns
$t_{HZCE}$	$\overline{CE}$ HIGH to High Z <sup>[20, 21, 22]</sup>	–	25	ns
$t_{PU}$	$\overline{CE}$ LOW to power-up <sup>[21]</sup>	0	–	ns
$t_{PD}$	$\overline{CE}$ HIGH to power-down <sup>[21]</sup>	–	35	ns
<b>Write Cycle</b>				
$t_{WC}$	Write cycle time	55	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	40	–	ns
$t_{AW}$	Address setup to write end	40	–	ns
$t_{HA}$	Address hold from write end	2	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	R/ $\overline{W}$ pulse width	30	–	ns
$t_{SD}$	Data setup to write end	20	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}$	R/ $\overline{W}$ LOW to High Z <sup>[23]</sup>	–	25	ns
$t_{LZWE}$	R/ $\overline{W}$ HIGH to Low Z <sup>[23]</sup>	3	–	ns

### Notes

20. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and R/ $\overline{W}$  LOW. Both signals must be low to initiate a write and either signal can terminate a write by going high. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.

21. AC Test Conditions use  $V_{OH} = 1.6$  V and  $V_{OL} = 1.4$  V.

22. These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.

23. Parameters  $t_{LZCE}$ ,  $t_{LZWE}$ ,  $t_{HZOE}$ ,  $t_{LZOE}$ ,  $t_{HZCE}$  and  $t_{HZWE}$  are tested with C = 5 pF as in part (b) of [Figure 3 on page 5](#). Transition is measured  $\pm 500$  mV from steady state voltage.

## Switching Characteristics (continued)

Over the Operating Range

Parameter	Description	7C131E-55/7C136E-55/ 7C136AE-55		Unit
		Min	Max	
<b>Busy/Interrupt Timing</b> <sup>[24]</sup>				
t <sub>BLA</sub>	BUSY LOW from Address match	–	30	ns
t <sub>BHA</sub>	BUSY HIGH from Address mismatch <sup>[25]</sup>	–	30	ns
t <sub>BLC</sub>	BUSY LOW from $\overline{CE}$ LOW	–	30	ns
t <sub>BHC</sub>	BUSY HIGH from $\overline{CE}$ HIGH <sup>[25]</sup>	–	30	ns
t <sub>PS</sub>	Port setup for priority	5	–	ns
t <sub>BDD</sub>	BUSY HIGH to valid data	–	45	ns
t <sub>DDD</sub>	Write data valid to read data valid <sup>[25]</sup>	–	30	ns
t <sub>WDD</sub>	Write pulse to data delay <sup>[25]</sup>	–	45	ns
<b>Interrupt Timing</b>				
t <sub>WINS</sub>	R/W to $\overline{INTERRUPT}$ set time	–	45	ns
t <sub>EINS</sub>	$\overline{CE}$ to $\overline{INTERRUPT}$ set time	–	45	ns
t <sub>INS</sub>	Address to $\overline{INTERRUPT}$ set time	–	45	ns
t <sub>OINR</sub>	$\overline{OE}$ to $\overline{INTERRUPT}$ reset time <sup>[26]</sup>	–	45	ns
t <sub>EINR</sub>	$\overline{CE}$ to $\overline{INTERRUPT}$ reset time <sup>[26]</sup>	–	45	ns
t <sub>INR</sub>	Address to $\overline{INTERRUPT}$ reset time <sup>[26]</sup>	–	45	ns

### Notes

24. Test conditions used are Load 2.

25. A write operation on Port A, where Port A has priority, leaves the data on Port B's outputs undisturbed until one access time after one of the following:  
 BUSY on Port B goes HIGH.  
 Port B's address toggled.  
 $\overline{CE}$  for Port B is toggled.  
 R/W for Port B is toggled during valid read.

26. These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.

## Switching Waveforms

Figure 4. Read Cycle No. 1 [27, 28]

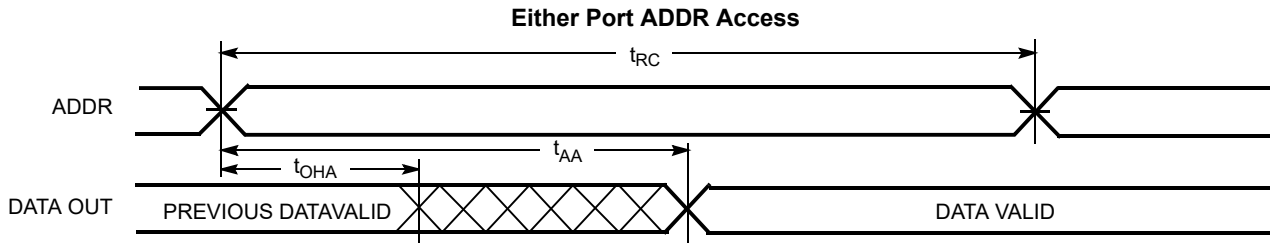


Figure 5. Read Cycle No. 2 [27, 29]

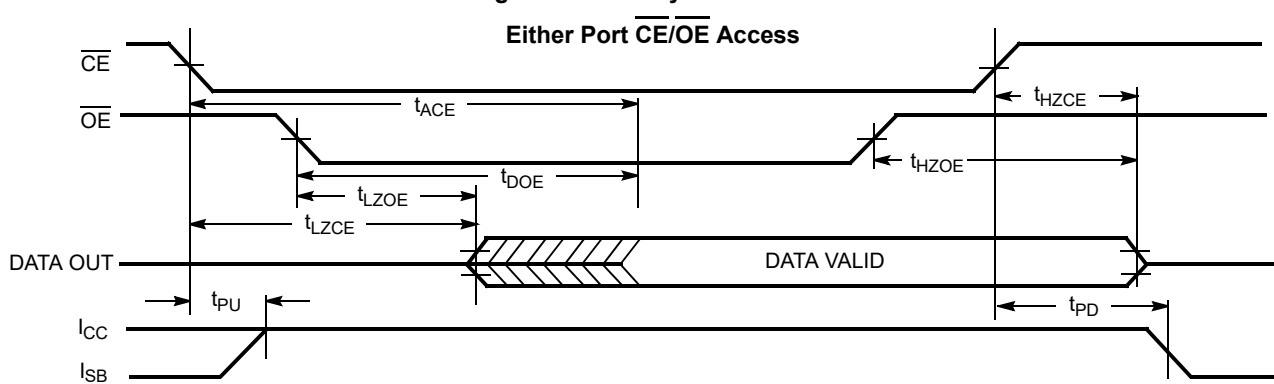
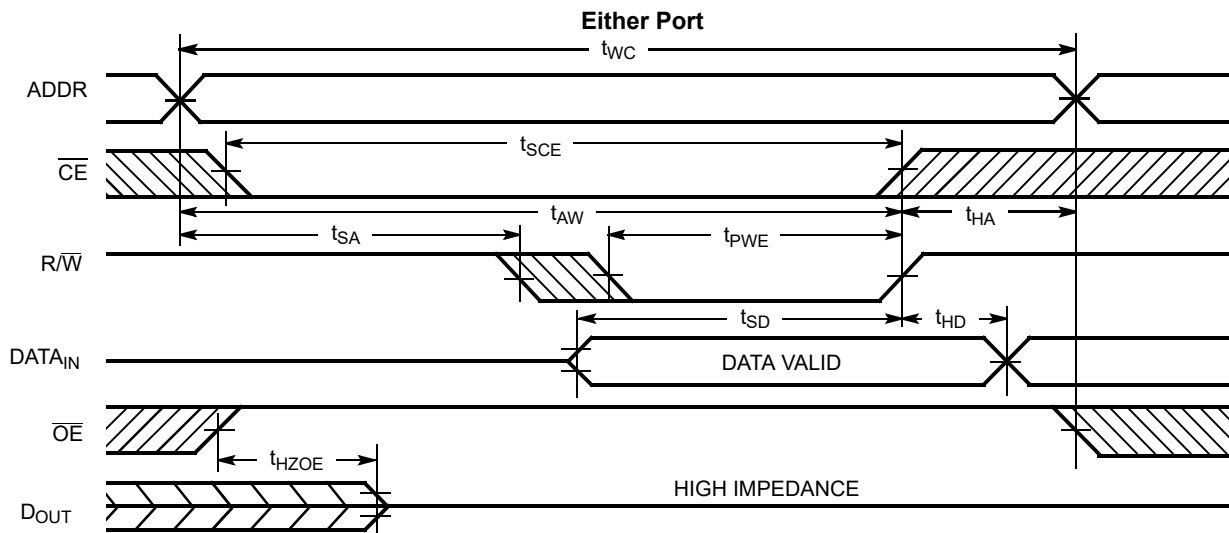


Figure 6. Write Cycle No. 1 ( $\overline{OE}$  Three-States Data I/Os – Either Port) [30, 31]



### Notes

27.  $R/\overline{W}$  is HIGH for read cycle.

28. Device is continuously selected,  $\overline{CE} = V_{IL}$  and  $\overline{OE} = V_{IL}$ .

29. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

30. The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $R/\overline{W}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing must be referenced to the rising edge of the signal that terminates the write.

31. If  $\overline{OE}$  is LOW during a  $R/\overline{W}$  controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or  $t_{HZWE} + t_{SD}$  to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required  $t_{SD}$ .

Switching Waveforms (continued)

Figure 7. Write Cycle No. 2 (R/W Three-States Data I/Os – Either Port) [32, 33]

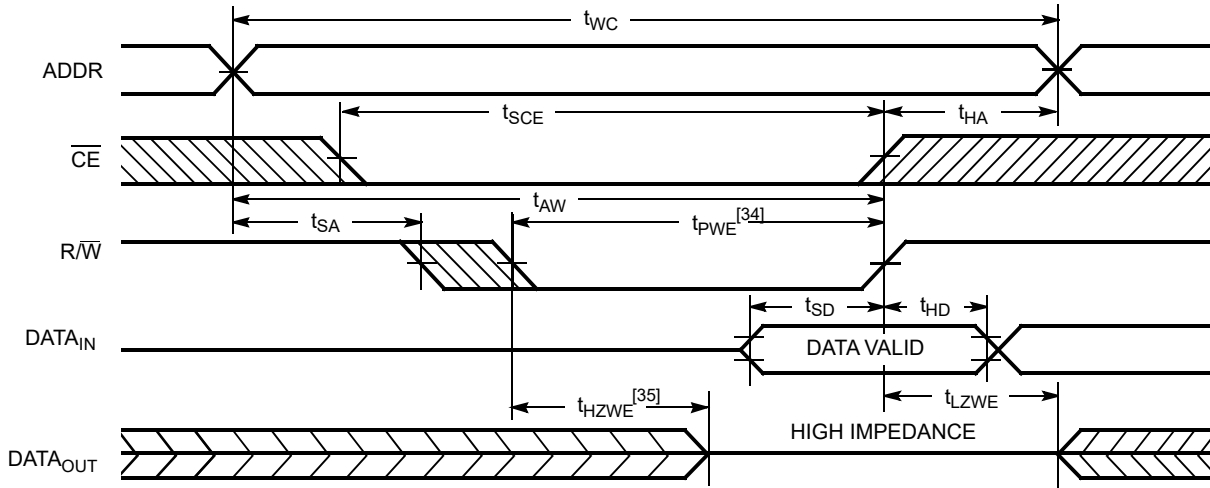
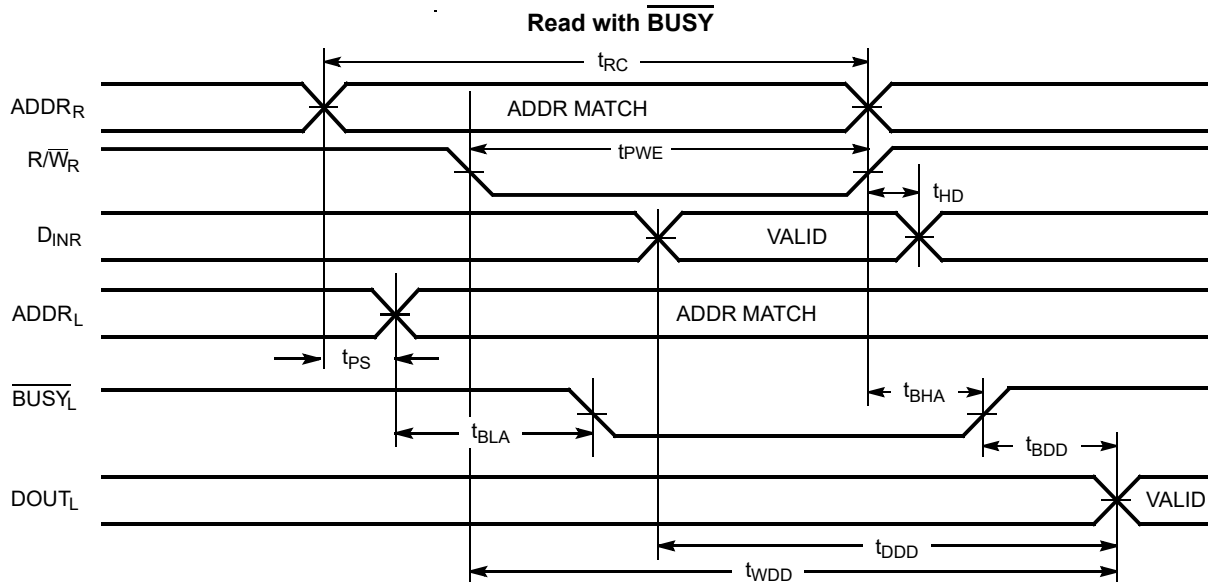


Figure 8. Read Cycle No. 3 [36]



Notes

- 32. These parameters are measured from the input signal changing, until the output pin goes to a high impedance state.
- 33. If the CE LOW transition occurs simultaneously with or after the R/W LOW transition, the outputs remain in a high impedance state.
- 34. If OE is LOW during a R/W controlled write cycle, the write pulse width must be the larger of  $t_{PWE}$  or  $(t_{HZWE} + t_{SD})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{SD}$ . If OE is HIGH during a R/Wn controlled write cycle, this requirements does not apply and the write pulse can be as short as the specified  $t_{PWE}$ .
- 35. Transition is measured  $\pm 500$  mV from steady state with a 5 pF load (including scope and jig). This parameter is sampled and not 100% tested.
- 36. CEL = CER = LOW.

Switching Waveforms (continued)

Figure 9. Busy Timing Diagram No. 1 ( $\overline{CE}$  Arbitration) [37]

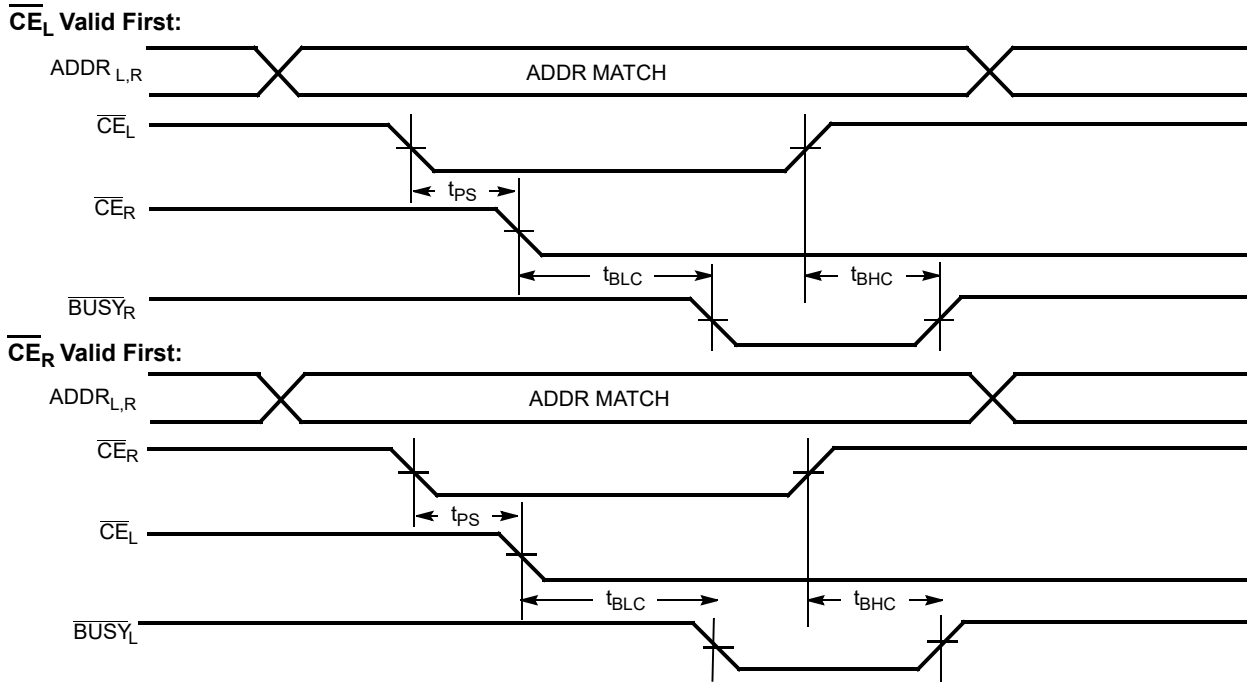
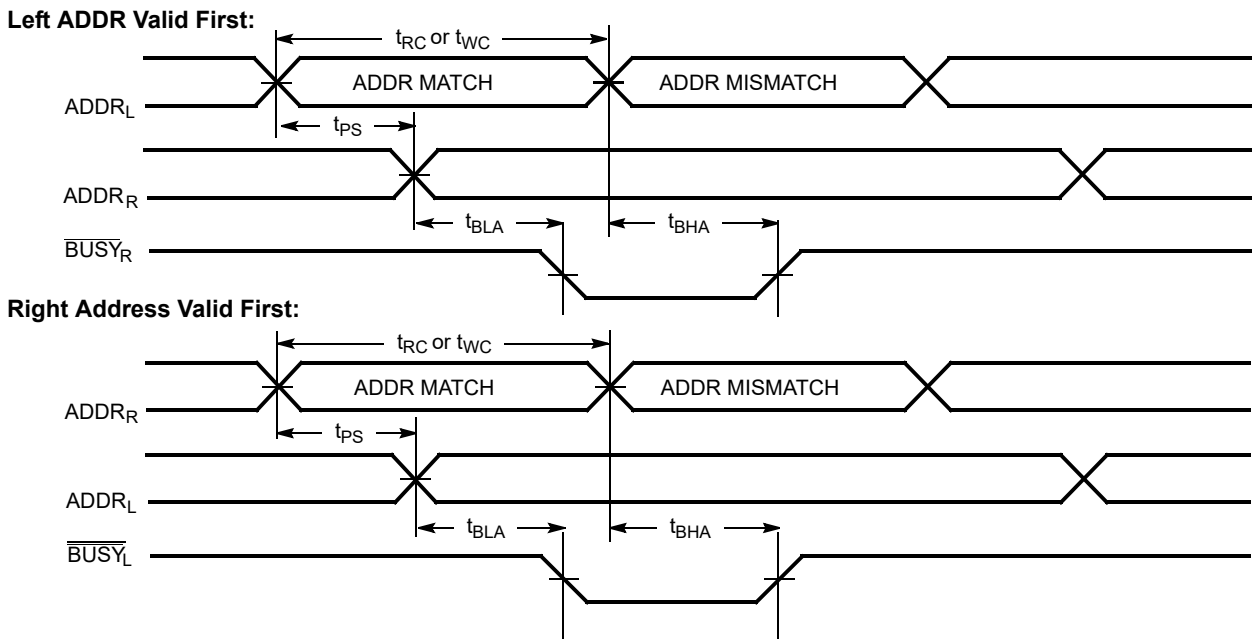


Figure 10. Busy Timing Diagram No. 2 (ADDR Arbitration) [37]

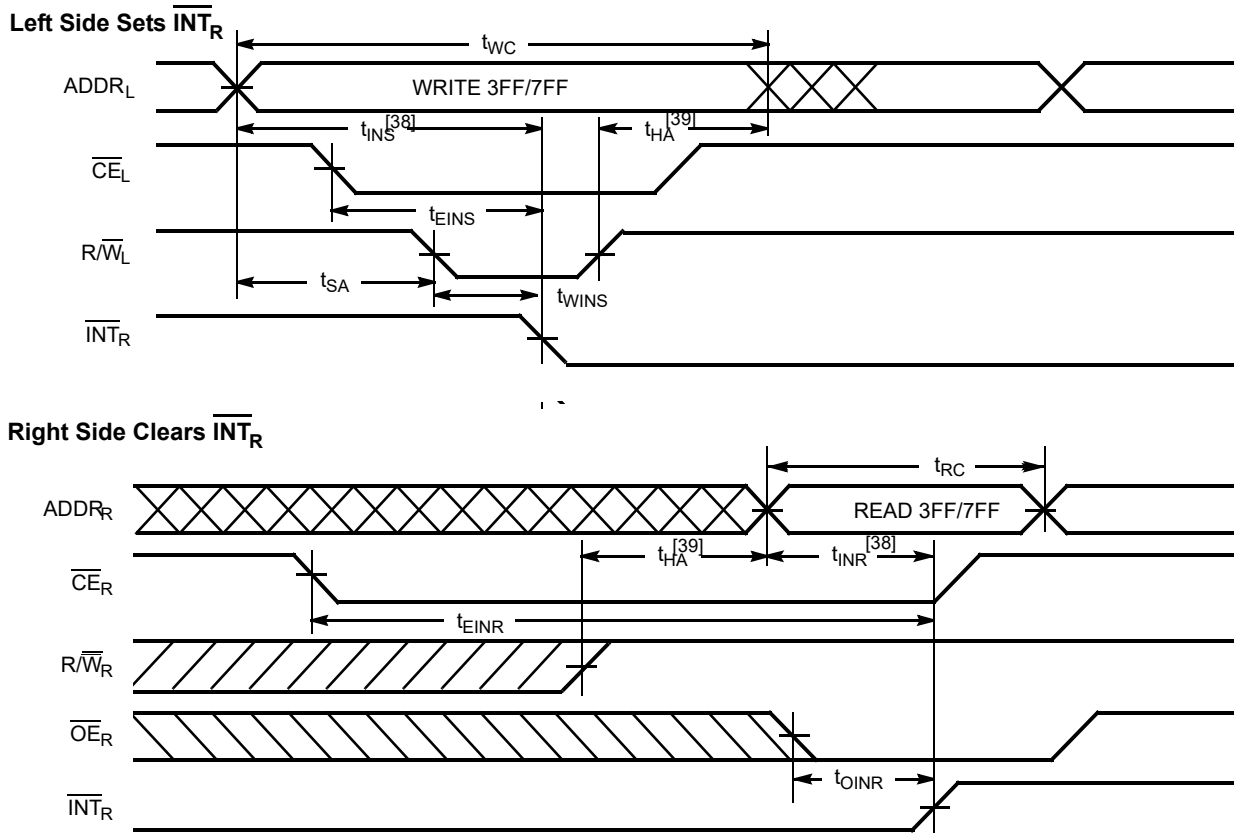


Note

37. If  $t_{PS}$  is violated, the busy signal will be asserted on one side or the other, but there is no guarantee to which side  $\overline{BUSY}$  will be asserted.

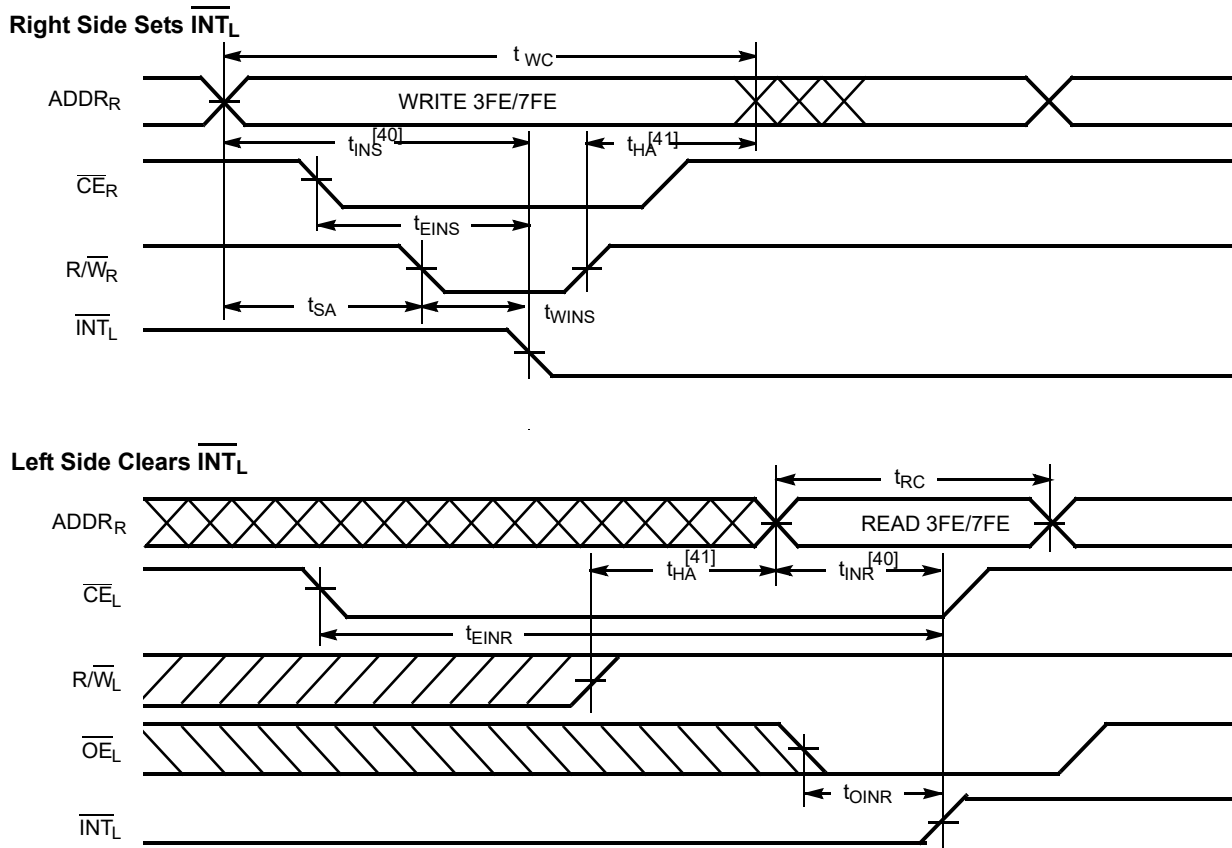
Switching Waveforms (continued)

Figure 11. Interrupt Timing Diagrams



Notes

- 38. Parameter  $t_{INS}$  or  $t_{INR}$  depends on which enable pin ( $\overline{CE}_L$  or  $R/\overline{W}_L$ ) is asserted last.
- 39. Parameter  $t_{HA}$  depends on which enable pin ( $\overline{CE}_L$  or  $R/\overline{W}_L$ ) is deasserted first.

**Switching Waveforms (continued)**
**Figure 12. Interrupt Timing Diagrams**

**Notes**

40. Parameter  $t_{INS}$  or  $t_{INR}$  depends on which enable pin ( $\overline{CE}_L$  or R/ $\overline{W}_L$ ) is asserted last.
41. Parameter  $t_{HA}$  depends on which enable pin ( $\overline{CE}_L$  or R/ $\overline{W}_L$ ) is deasserted first.

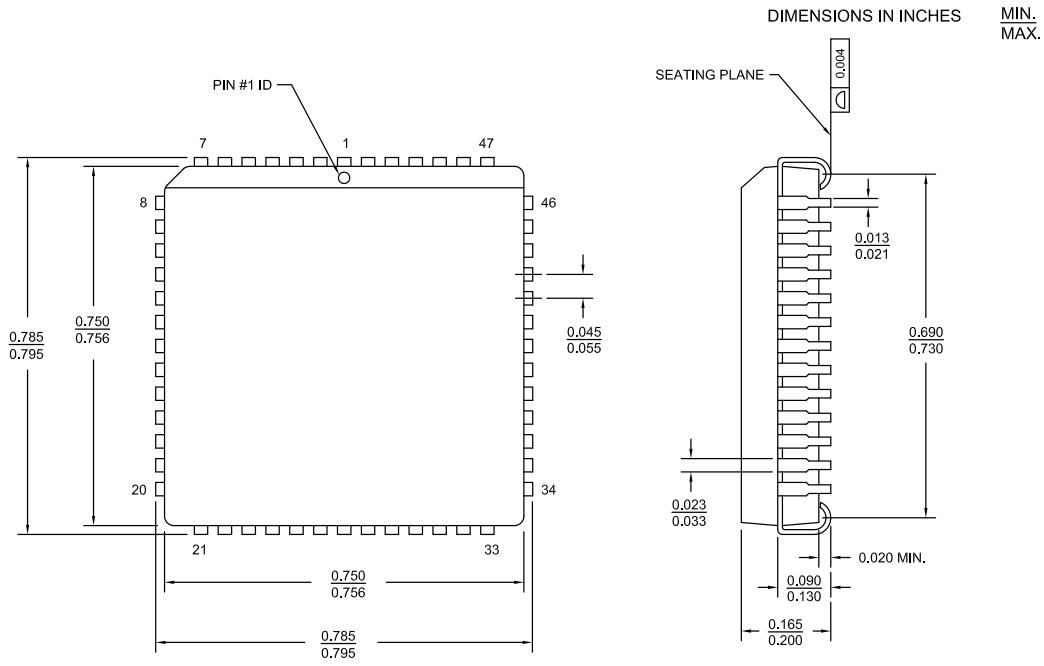
## Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
<b>1K × 8 Dual-port SRAM</b>				
15	CY7C131E-15NXI	51-85042	52-pin PQFP (Pb-free)	Industrial
	CY7C131E-15NXIT	51-85042	52-pin PQFP (Pb-free), Tape and Reel	
25	CY7C131E-25JXC	51-85004	52-pin PLCC (Pb-free)	Commercial
	CY7C131E-25JXCT	51-85004	52-pin PLCC (Pb-free), Tape and Reel	
	CY7C131E-25NXC	51-85042	52-pin PQFP (Pb-free)	
	CY7C131E-25NXCT	51-85042	52-pin PQFP (Pb-free), Tape and Reel	
55	CY7C131E-55JXC	51-85004	52-pin PLCC (Pb-free)	Commercial
	CY7C131E-55JXCT	51-85004	52-pin PLCC (Pb-free), Tape and Reel	
	CY7C131E-55NXC	51-85042	52-pin PQFP (Pb-free)	
	CY7C131E-55NXCT	51-85042	52-pin PQFP (Pb-free), Tape and Reel	
	CY7C131E-55JXI	51-85004	52-pin PLCC (Pb-free)	Industrial
	CY7C131E-55JXIT	51-85004	52-pin PLCC (Pb-free), Tape and Reel	
<b>2K × 8 Dual-port SRAM</b>				
25	CY7C136E-25JXC	51-85004	52-pin PLCC (Pb-free)	Commercial
	CY7C136E-25JXCT	51-85004	52-pin PLCC (Pb-free), Tape and Reel	
	CY7C136E-25NXC	51-85042	52-pin PQFP (Pb-free)	
	CY7C136E-25NXCT	51-85042	52-pin PQFP (Pb-free), Tape and Reel	
	CY7C136E-25JXI	51-85004	52-pin PLCC (Pb-free)	Industrial
	CY7C136E-25JXIT	51-85004	52-pin PLCC (Pb-free), Tape and Reel	
55	CY7C136E-55JXC	51-85004	52-pin PLCC (Pb-free)	Commercial
	CY7C136E-55JXCT	51-85004	52-pin PLCC (Pb-free), Tape and Reel	
	CY7C136E-55NXC	51-85042	52-pin PQFP (Pb-free)	
	CY7C136E-55NXCT	51-85042	52-pin PQFP (Pb-free), Tape and Reel	
	CY7C136AE-55JXI	51-85004	52-pin PLCC (Pb-free)	Industrial
	CY7C136AE-55JXIT	51-85004	52-pin PLCC (Pb-free), Tape and Reel	
	CY7C136AE-55NXI	51-85042	52-pin PQFP (Pb-free)	
	CY7C136AE-55NXIT	51-85042	52-pin PQFP (Pb-free), Tape and Reel	

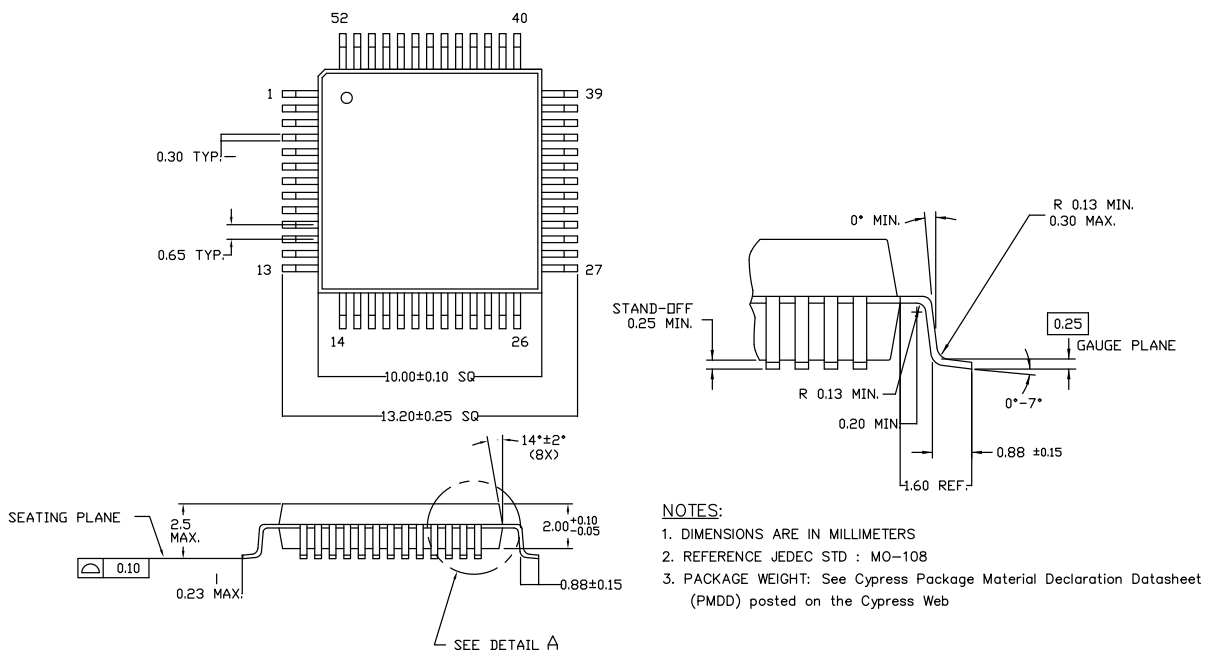


**Package Diagrams**

**Figure 13. 52-pin PLCC (0.756 × 0.756 Inches) J52 Package Outline, 51-85004**



**Figure 14. 52-pin PQFP (10 × 10 × 2.0 mm) N5210 Package Outline, 51-85042**



## Acronyms

Acronym	Description
$\overline{CE}$	Chip Enable
CMOS	Complementary Metal Oxide Semiconductor
I/O	Input/Output
$\overline{OE}$	Output Enable
PLCC	Plastic Leaded Chip Carrier
PQFP	Plastic Quad Flat Package
SRAM	Static Random Access Memory
TTL	Transistor-Transistor Logic
$\overline{WE}$	Write Enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
$^{\circ}C$	degree Celsius
$\mu A$	microampere
mA	milliampere
mV	millivolt
ns	nanosecond
$\Omega$	ohm
%	percent
pF	picofarad
V	volt
W	watt

## Document History Page

Document Title: CY7C131E/CY7C131AE/CY7C136E/CY7C136AE, 1K/2K × 8 Dual-Port Static RAM				
Document Number: 001-64231				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
**	3038037	ADMU	09/24/2010	New data sheet.
*A	3394800	ADMU	10/04/2011	<p>Changed status from Preliminary to Final.</p> <p>Updated <a href="#">Maximum Ratings</a> (Removed (Pin 48 to Pin 24)).</p> <p>Updated <a href="#">Electrical Characteristics</a> (changed minimum value of I<sub>OZ</sub> parameter from -10 μA to -20 μA, changed maximum value of I<sub>OZ</sub> parameter from +10 μA to +20 μA and changed maximum value of I<sub>SB3</sub> from 0.5 mA to 15 mA for both Commercial and Industrial temperature ranges).</p> <p>Updated <a href="#">Package Diagrams</a> (Updated revision of 51-85004 from *B to *C and revision of 51-85042 from *A to *C).</p> <p>Updated in new template.</p>
*B	3403147	ADMU	10/12/2011	No technical updates.
*C	3435230	ADMU	11/17/2011	<p>Updated <a href="#">Features</a> (Removed a feature “Expandable data bus width to 16 bits or more using Master/Slave chip select when using more than one device.” and updated another feature to read as “BUSY output flag to indicate access to the same location by both ports.”).</p> <p>Updated <a href="#">Functional Description</a> (Updated the sentence in the first paragraph to read as “The CY7C131E / CY7C131AE / CY7C136E / CY7C136AE can be used as a standalone dual-port static RAM.”).</p> <p>Updated Note 2 to read as “BUSY is a push-pull output. No pull-up resistor required.”.</p> <p>Updated Note 3 to read as “Interrupt: push-pull output. No pull-up resistor required.”.</p> <p>Updated <a href="#">Maximum Ratings</a> (Removed “(per MIL-STD-883, Method 3015)”).</p> <p>Updated <a href="#">Electrical Characteristics</a> (Removed the Note “See the last page of this specification for Group A subgroup testing information.” and its reference in Parameter column.).</p> <p>Updated <a href="#">Capacitance</a> (Changed maximum value of C<sub>IN</sub> parameter from 10 pF to 15 pF).</p> <p>Updated <a href="#">AC Test Loads and Waveforms</a>.</p> <p>Updated <a href="#">Switching Characteristics</a> (Removed the Note “See the last page of this specification for Group A subgroup testing information.” and its reference in Parameter column.).</p> <p>Updated <a href="#">Switching Characteristics</a> (Changed the minimum value of t<sub>OHA</sub> from 0 ns to 3 ns).</p> <p>Removed the section “Typical DC and AC Characteristics”.</p> <p>Removed the section “Reference Documents”.</p>

**Document History Page (continued)**

Document Title: CY7C131E/CY7C131AE/CY7C136E/CY7C136AE, 1K/2K × 8 Dual-Port Static RAM				
Document Number: 001-64231				
Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
*D	3620277	ADMU	06/15/2012	Updated missing overbars in all instances across the document. Updated <a href="#">Selection Guide</a> : Updated all values of “Typical Operating Current” parameter. Updated <a href="#">Maximum Ratings</a> : Changed value of “Static discharge voltage” from “>2001 V” to “>1100 V”. Updated <a href="#">Electrical Characteristics</a> : Fixed typos. Added Note 8 and referred the same note in “Typ” column. Updated all values of I <sub>CC</sub> parameter. Updated <a href="#">AC Test Loads and Waveforms</a> : Updated <a href="#">Figure 3</a> (Replaced 3 ns with 5 ns). Updated <a href="#">Switching Characteristics</a> : Added Note 17 and referred the same note in “Busy/Interrupt Timing”. Updated <a href="#">Switching Characteristics</a> : Added Note 24 and referred the same note in “Busy/Interrupt Timing”. Updated <a href="#">Switching Waveforms</a> : Added Note 34 and referred the same note in “t <sub>PWE</sub> ” in <a href="#">Figure 7</a> . Added Note 35 and referred the same note in “t <sub>PWE</sub> ” in <a href="#">Figure 7</a> . Added Note 38 and referred the same note in “t <sub>INS</sub> ” in <a href="#">Figure 11</a> . Added Note 39 and referred the same note in “t <sub>HA</sub> ” in <a href="#">Figure 11</a> . Added Note 40 and referred the same note in “t <sub>INS</sub> ” in <a href="#">Figure 12</a> . Added Note 41 and referred the same note in “t <sub>HA</sub> ” in <a href="#">Figure 12</a> . Removed “Busy Timing Diagram No. 3”. Updated <a href="#">Package Diagrams</a> : spec 51-85042 – Changed revision from *C to *D.
*E	3997575	ADMU	05/15/2013	Updated <a href="#">Package Diagrams</a> : spec 51-85004 – Changed revision from *C to *D. Added Appendix: Silicon Errata for CY7C131E/131AE/136E/136AE 1K/2K × 8 Dual Port Static RAM.
*F	4241174	ADMU	01/09/2014	Removed Appendix: Silicon Errata for CY7C131E/131AE/136E/136AE 1K/2K × 8 Dual Port Static RAM. Updated to new template.
*G	4559526	AMDU	11/07/2014	Updated <a href="#">Functional Description</a> : Added “For a complete list of related documentation, click <a href="#">here</a> .” at the end.
*H	5397125	NILE	08/09/2016	Updated <a href="#">Ordering Information</a> : Updated part numbers. Updated <a href="#">Package Diagrams</a> : spec 51-85042 – Changed revision from *D to *E. Updated to new template.
*I	5966445	AESATMP8	11/14/2017	Updated logo and Copyright.
*J	6175372	NILE	07/31/2018	Updated <a href="#">Ordering Information</a> : Added Tube information to part number decoder. Updated Sales page.

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