



**THE DATASHEET OF  
89H16NT16G2ZCHL**





# IDT™ 89EB-LOGAN-19 Evaluation Board Manual

(Evaluation Board: 18-692-001)

February 2011

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# Description of the EB-LOGAN-19 Evaluation Board

## Notes

## Introduction

The 89HPES24NT24G2 switch is a member of the IDT PCI Express® Inter-Domain Switch family of products. It is a PCIe® Base Specification 2.1 compliant (Gen2) 24-lane, 24-port switch. The EB-LOGAN-19 Evaluation Board provides an evaluation platform for the PES24NT24G2 switch and for other members of this switch family including PES16NT16G2 and PES12NT12G2.

Detailed information related to configuration of number of ports and lanes in the switch device can be found in the Device User Manual and the Device Datasheet. The evaluation board, along with additional adapters and daughter boards provided by IDT, can be configured to test every possible combination of the number of lanes and ports offered by the switch. Advanced capabilities such as switch partitioning, NTB, DMA and local port clocking can be evaluated with the evaluation board.

The EB-LOGAN-19 brings out all 24 lanes of the device to two Mezzanine connectors and two SAS connectors (see Figure 1.1) located close to the device - one connector per stack of 4 lanes. Various types of daughter cards (provided by IDT) can then be plugged into the Mezzanine connectors to facilitate connectivity to one x8 or two x4 or four x2 or eight x1 link partners. Link partners may be plugged directly into these daughter cards or they can be connected to these daughter cards via SAS or SATA cables and a different board with PCIe slots known as the 12-PACK board (provided by IDT). Given that majority of the hosts / servers offer PCIe standard slots, IDT provides the necessary adapter cards that may be plugged into these host / server slots as well as the cables that connect such adapters to the daughter cards which in turn are plugged into the main evaluation board on which the IDT PCIe switch device is populated.

The EB-LOGAN-19 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB-LOGAN-19 board.

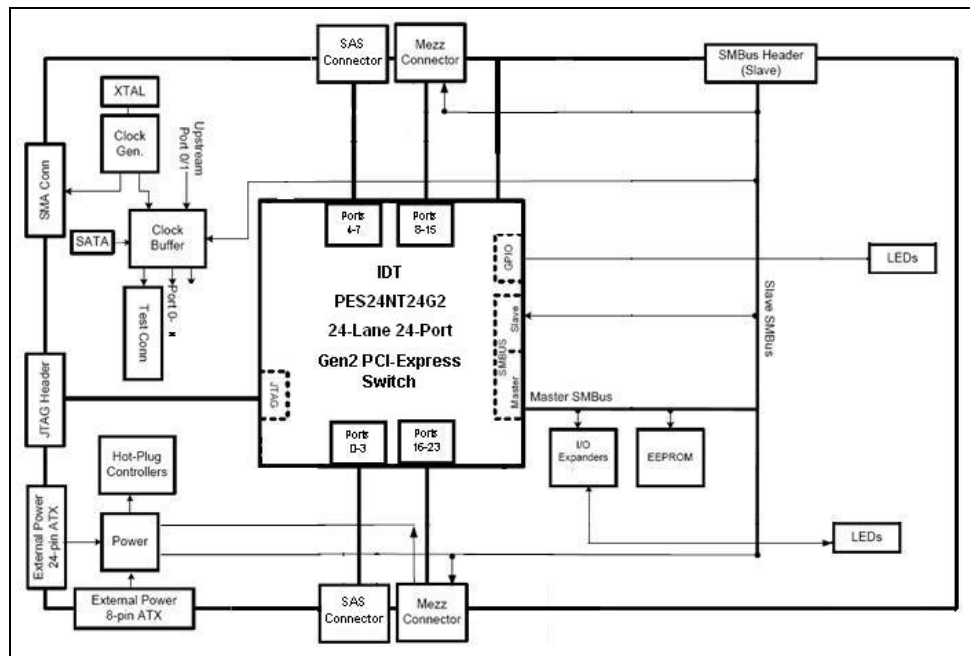


Figure 1.1 Function Block Diagram of the EB-LOGAN-19 Evaluation Board

## Notes

## Board Features

### Hardware

- ◆ **PES24NT24G2 PCIe 24-port switch**
  - *Twenty four ports (each x1) - for port 8 and higher, adjacent ports may be combined to create x2, x4 or x8 ports*
  - *PCIe Base Specification Revision 2.1 compliant (Gen2 SerDes speeds of 5 GT/S)*
  - *Up to 2048 byte maximum Payload Size*
  - *Automatic lane reversal and polarity inversion supported on all lanes*
  - *Automatic per port link width negotiation to x8, x4, x2, x1*
  - *Power on reconfiguration via optional serial EEPROM connected to the SMBUS Master interface*
- ◆ **Upstream, Downstream Ports**
  - *The EB-LOGAN-19 has minimum of one port configured as upstream port to be plugged into a host slot through an adaptor and a cable.*
  - *Up to 23 ports can be configured as downstream ports, for PCIe endpoint add-on cards to be plugged in. The slot connectors can be configured to be x1, x2, x4 or x8, but are mechanically open-ended on one side to allow card widths greater than x8 (e.g. x16) to be populated.*
  - *When used in multi-partition mode, the device can be programmed through the serial EEPROM to generate the appropriate number of upstream and downstream ports per partition.*
- ◆ **Numerous user selectable configurations set using onboard jumpers and DIP-switches**
  - *Source of clock - host clock or onboard clock generator*
  - *Two clock rates (100/125 MHz) from an onboard clock generator*
  - *Flexible clocking modes*
    - *Common clock*
    - *Non-common clock*
    - *Local port clocking on ports that support this feature*
  - *Boot mode selection*
- ◆ **SMBUS Slave Interface (4 pin header)**
- ◆ **SMBUS Master Interface connected to the Serial EEPROMs through I/O expander**
- ◆ **Push button for Warm Reset**
- ◆ **Many LEDs to display status, reset, power, hotplug, etc.**
- ◆ **JTAG connector to the PES24NT24G2 JTAG pins.**

### Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES24NT24G2 within host systems running popular operating systems.

- ◆ **Installation programs**
  - *Operating Systems Supported: WindowsServer200x, WindowsXP, Vista, Linux*
- ◆ **GUI based application for Windows and Linux**
  - *Allows users to view and modify registers in the PES24NT24G2*
  - *Binary file generator for programming the serial EEPROMs attached to the SMBUS.*

### Other

- ◆ **SMBUS cable may be required for certain evaluation exercises.**
- ◆ **SMA connectors are provided on the EB-LOGAN-19 board for clock outputs.**

## Revision History

**April 13, 2010:** Initial publication of evaluation board manual.

## Notes

**April 23, 2010:** Updated Schematics in Chapter 4.

**August 18, 2010:** Updated the manual for Rev. 2.0 board

**February 16, 2011:** Changed default settings from Off to On in Tables 2.3 and 2.4.

Notes



# Installation of the EB-LOGAN-19 Evaluation Board

## Notes

### EB-LOGAN-19 Installation

This chapter discusses the steps required to configure and install the EB-LOGAN-19 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Make sure that the host system (motherboard with root complex chipset) is powered off.
4. Connect the evaluation board to the host system.
5. Apply power to the host system.

The EB-LOGAN-19 board is typically shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup however please visit IDT website and fill out the Technical Support Request form at <http://www.idt.com/?app=TechSupport> for other configurations.

### PCI Express Mezzanine and Edge Adapters

The PCI Express lanes are broken out to four Mezzanine connectors on EB-LOGAN-19 Evaluation Board. The adapter cards are used to convert Mezzanine connector into PCI Express slot connector(s) or Internal mini SAS (iSAS) connectors or both. A Bifurcated Mezzanine Card has two mechanical x8 PCIe Slots (x4 electrically) while a Merged Mezzanine Card has single x8 PCIe Slot. Pictured in Figure 2.1.

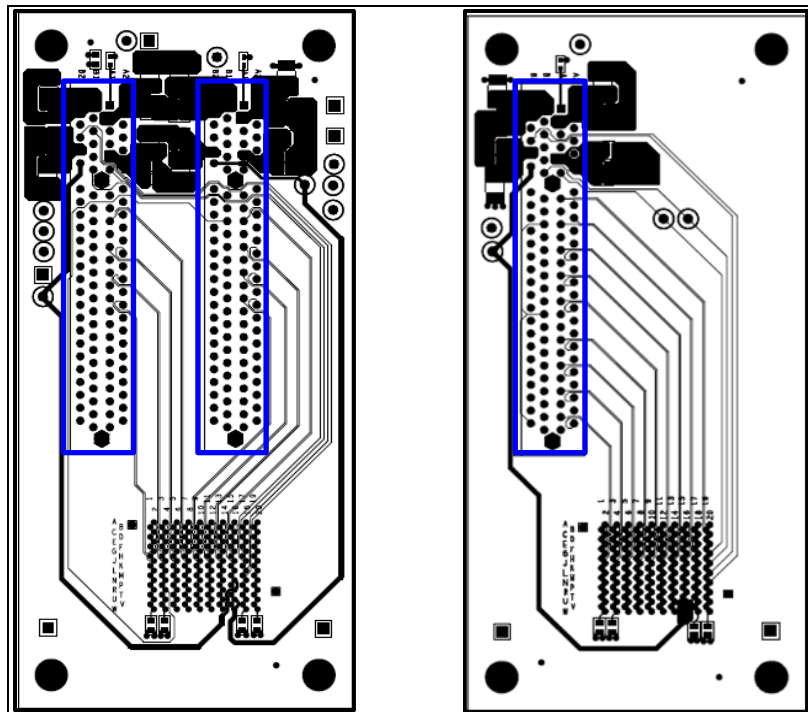


Figure 2.1 Bifurcated and Merged Mezzanine Cards

Notes

Pictured in Figure 2.2 is the mini-SAS Mezzanine card which consists of two iSAS and two SATA connectors. Each iSAS connector supports up to PCI Express x4 width and the SATA connectors are used for clock and reset signals of each x4 or less stack/port. An iSAS-to-SATA breakout cable shown in Figure 2.3 is used connect from iSAS to edge adapter and/or 12PACK.

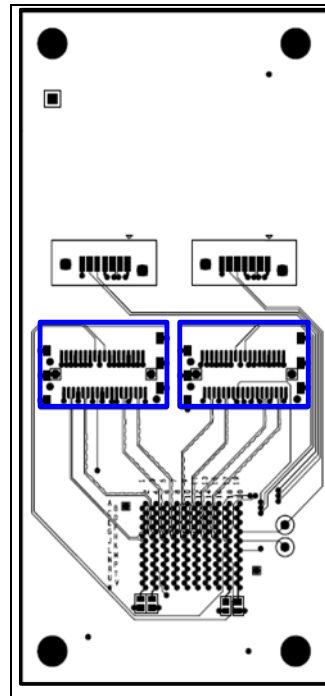


Figure 2.2 MiniSAS Mezzanine Adapter

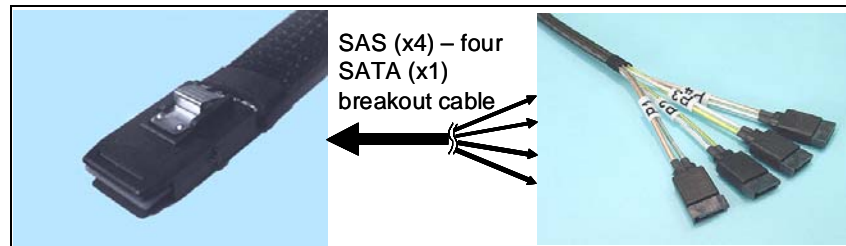


Figure 2.3 EB-LOGAN-19 iSAS-to-SATA Breakout Cable

The PCI Express Edge to SATA Adapter, pictured in Figure 2.4, can be inserted into any physical PCIe slot on a host system and in combination with mini-SAS Mezzanine Card, such as the one in Figure 2.2, to form a link between evaluation main board and the host system. There are 5 SATA connectors which one connector (J7) is for clock and reset, and the rest supports one PCIe lane per SATA connector. The edge adapters can be inserted into a mechanical x1 or greater slot.

Notes

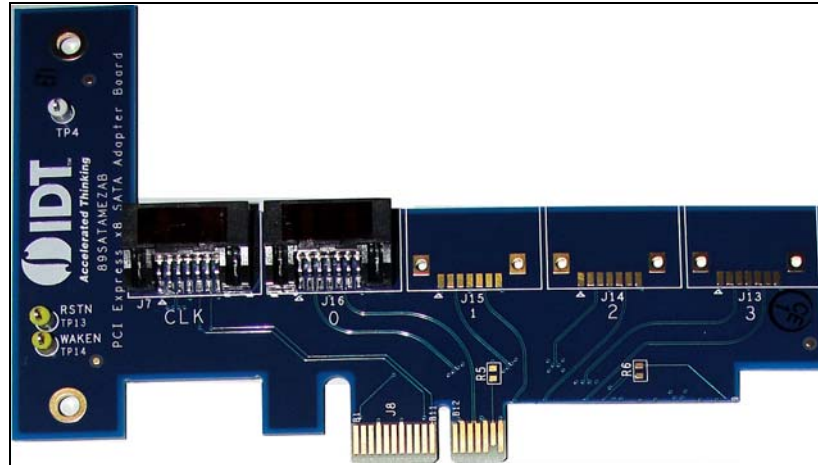


Figure 2.4 PCIe x1 Edge-to-SATA Adapter

Hardware Description

The PES24NT24G2 is a 24-lane, 24-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and downstream ports or peer-to-peer switching between downstream ports. Furthermore, up to eight ports can be configured as NTB ports for multi-root application.

The EB-LOGAN-19 Main Board, shown in Figure 2.5, will support up to 4 PCI Express downstream ports and up to 23 ports when using two 12PACK Daughter Boards.

Basic requirements for the board to run are:

- Host system with a PCI Express root complex supporting x1 configuration through a PCI Express x1 slot.
- - x1, x2, x4, or x8 PCI Express Endpoint Cards.

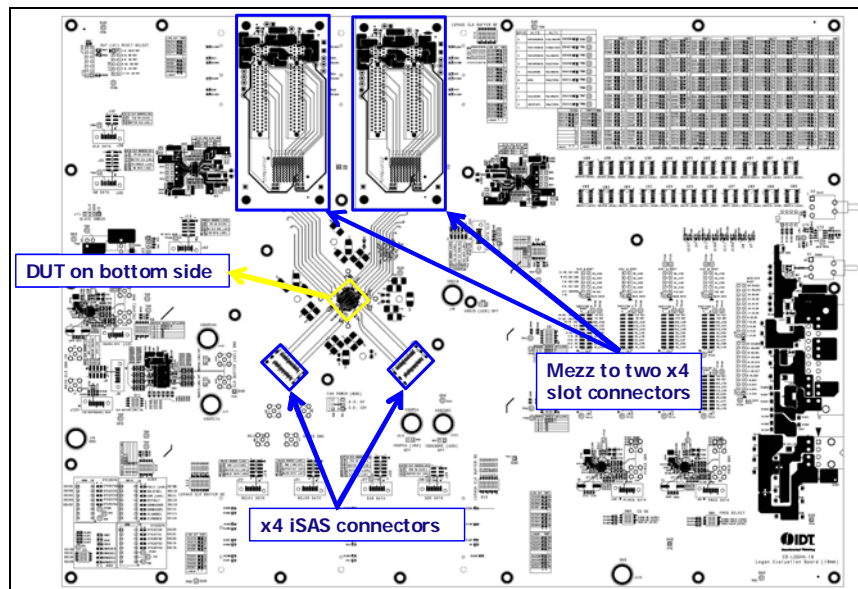


Figure 2.5 EB-LOGAN-19 Evaluation Main Board

Notes

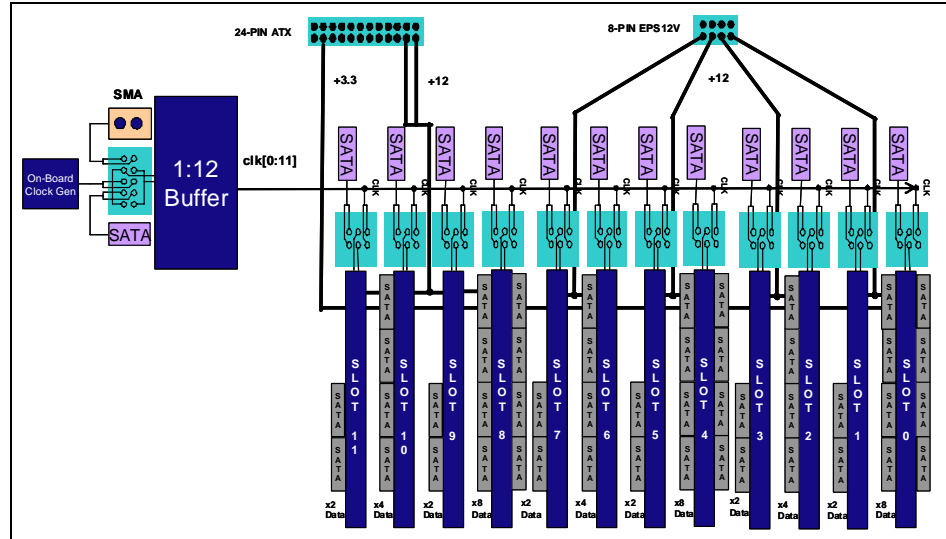


Figure 2.6 12PACK PCIe Slots Breakout Daughter Board

Reference Clocks

Global Reference Input Clocks

The PES24NT24G2 requires two differential reference clocks. The EB-LOGAN-19 derives these clocks from SMA connectors (J17, J20, J66, J67), clock buffer (U50), or SATA connectors (J21, J22) as described in Table 2.1 and Figures 2.7 and 2.8. Both reference clocks are mandatory and must come from the same reference clock source. The switch will not function normally if only one clock is used.

Global Clock#	Jumper	Selection
0	J18	[1-3 / 2-4] SMA (J66/J67) [5-7 / 6-8] From Clock Buffer U51 [7-9 / 8-10] SATA, J21
1	J19	[1-3 / 2-4] SMA (J17/J20) [5-7 / 6-8] From Clock Buffer U51 [7-9 / 8-10] SATA, J22

Table 2.1 EB-LOGAN-19 Global Clock Select

Notes

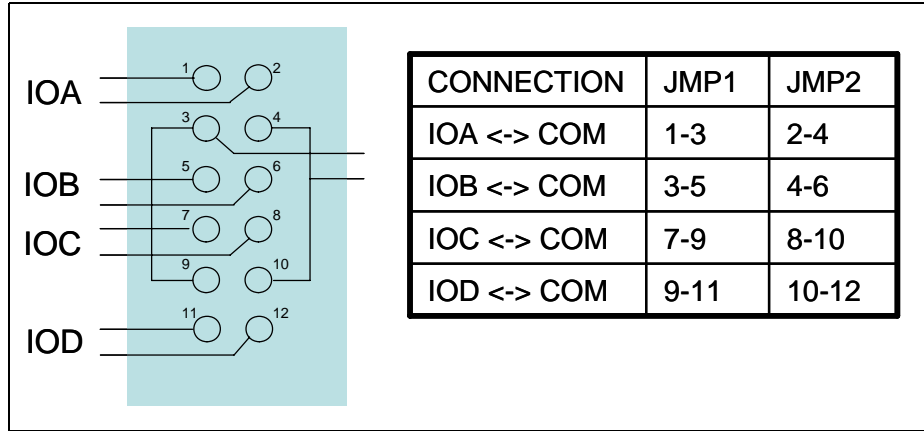


Figure 2.7 Differential Jumper Arrangement

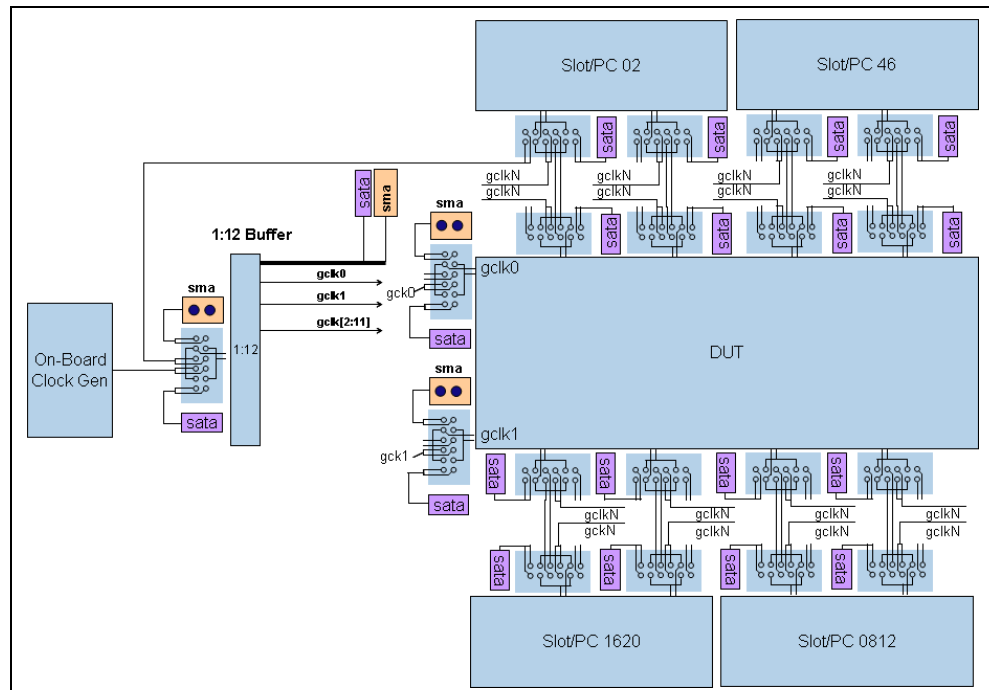


Figure 2.8 Reference Clock Configuration

By default the clock buffer derives its clock from a common source. The common source can be the host system's reference clock, the onboard clock generator, or SATA connector (J8). See Table 2.2.

Jumper	Selection
J6	[1-3 / 2-4] SMA (J5/J7) [5-7 / 6-8] Onboard Clock Generator (U49) [7-9 / 8-10] SATA (J8)

Table 2.2 Clock Buffer Input Sources

The frequency of the global reference clock input may be selected by the Clock Frequency Select (GCLKFEL) pin to be either 100 MHz or 125 MHz as described in Table 2.3.

Notes

Global Clock Frequency Switch - SW10[2]	
SW10[2]	Clock Frequency
ON	100 MHz (Default)
OFF	125 MHz

Table 2.3 Global Reference Input Clock Frequency Select

The source for the onboard clock is the ICS841484 clock generator device (U49) connected to a 25MHz oscillator (X1). When using the onboard clock generator, the output frequency is fixed at 100MHz. Therefore, ICS\_FS (S10, bit 1) is ON as the default setting. See Table 2.4.

Onboard Clock Frequency Switch - S10[1]	
S10[1]	Clock Frequency
ON	100 MHz (Default)
OFF	125 MHz

Table 2.4 Onboard Clock Generator Frequency Select

The output of the onboard clock generator is accessible through two yellow colored loop connectors located on the Evaluation Board. See Table 2.5. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential)	
J119	Positive Reference Clock (SMA)
J120	Negative Reference Clock (SMA)
J121	Differential Reference Clock (SATA)

Table 2.5 Onboard Reference Clock Generator Access Points

Local Port Input Clocks

Associated with some ports is a port reference clock input (PxCLK). Depending on the port clocking mode, a differential reference clock is driven into the device on the corresponding PxCLKP and PxCLKN pins. The frequency of a port reference clock input MUST always be 100 MHz. Table 2.6 and Table 2.7 list the possible sources for ports 8 and 16 reference clock input, and Table 2.8 lists the possible sources for the slot clock input. Additional information on port clocking usage and configuration can be found in the Device User Manuals and in IDT's Application Note AN-715. Local port clock sources for ports 8 and 16 are selected by DIP Switch (S17 and S19) via clock mux/buffer.

Port 8 Clock Source Select - S19[1]	
S19[1]	Clock Source
OFF	SATA J62
ON	Port 8 Clock Generator (U118)

Table 2.6 EB-LOGAN-23 Port 8 Clock Source Select

Notes

Port 16 Clock Source Select - S17[1]	
S17[1]	Clock Source
OFF	SATA J64
ON	Port 16 Clock Generator (U120)

Table 2.7 EB-LOGAN-23 Port 16 Clock Source Select

Slot #	Header	Selection
8	J31	[1-3 / 2-4] Onboard Clock Generator (U118) [3-5 / 4-6] From Clock Buffer [7-9 / 8-10] P16CLK Clock Mux (U16) [9-11 / 10-12] SATA (J35)
12	J32	[1-3 / 2-4] P08CLK Clock Mux (U18) [3-5 / 4-6] From Clock Buffer [7-9 / 8-10] P16CLK Clock Mux (U16) [9-11 / 10-12] SATA (J36)
16	J33	[1-3 / 2-4] P16CLK Clock Mux (U16) [3-5 / 4-6] From Clock Buffer [7-9 / 8-10] Onboard Clock Generator (U120) [9-11 / 10-12] SATA (J37)
20	J34	[1-3 / 2-4] P08CLK Clock Mux (U18) [3-5 / 4-6] From Clock Buffer [7-9 / 8-10] P16CLK Clock Mux (U16) [9-11 / 10-12] SATA (J38)

Table 2.8 EB-LOGAN-19 Slot Clock Select

**CLKMODE Selection**

All ports in the PES24NT24G2 device (upstream and downstream) use global clocked mode. The port clocking mode of a port is determined by the state of the CLKMODE[1:0] pins in the boot configuration vector as shown in Table 2.9. This field determines the initial value of the Slot Clock Configuration (SCLK) field in each port's PCI Express Link Status (PCIELSTS) register. The SCLK field controls the advertisement of whether or not the port uses the same reference clock source as the link partner. A one in the SCLK field indicates that the port and its link partner use the same reference clock source. This is defined as Common Clock Configuration by the PCI Express Base Specification. A zero in the SCLK field indicates that the port and its link partner do not use the same reference clock source.

SW10[8] CLKMODE[0]	SW10[7] CLKMODE[1]	Port 0 SCLK	Port[23:1] SCLK
ON	ON	0	0
OFF	ON	1	0
ON	OFF	0	1
OFF	OFF	1	1

Table 2.9 CLKMODE Selection PES24NT24G2

Notes

Power Sources

Power for the PES24NT24G2 and all downstream ports will be generated from the 12V from an external power connector. See Table 2.10. A 12V to 3.3V DC-DC converter will be used to provide power to five switching regulators to generate  $V_{DDCORE}$ ,  $V_{DDPEA}$ ,  $V_{DDPETA}$ ,  $V_{DDPEHA}$ , and  $V_{DDIO}$  voltages. The 3.3V from the DC-DC converter will be used to power the clock buffers and circuitries.

The external power supply connector is a 24-pin (J69) moxex connector as described in Tables 2.10.

Pin	Signal	Pin	Signal
1	+3.3V	13	+3.3V
2	+3.3V	14	-12V
3	GND	15	GND
4	+5V	16	PS_ON
5	GND	17	GND
6	+5V	18	GND
7	GND	19	GND
8	PWR_OK	20	NC
9	5VSB	21	+5V
10	+12V3	22	+5V
11	+12V3	23	+5V
12	+3.3V	24	GND

Table 2.10 EPS12V 24-pin Power Connector - J69

The power on switch located at S1 can be used to control the supply power from the external power supply connector. Add a shunt to W27 to enable power on switch.

PCI Express Analog Power Voltage Regulator

A voltage regulator (U65) provides a 2.5V PCI Express analog power voltage (shown as VDDPEHA) to the PES24NT24G2.

PCI Express Digital Power Voltage Converter

A separate voltage regulator (U62) provides a 1.0V PCI Express analog power voltage (shown as VDDPEA) to the PES24NT24G2.

PCI Express Transmitter Analog Voltage Converter

A separate voltage regulator (U68) provides a 1.0V PCI Express transmitter analog voltage (shown as VDDPETA) to the PES24NT24G2.

Core Logic Voltage Converter

A separate voltage regulator (U59) provides the 1.0V core voltage (VDDCORE) to the PES24NT24G2.

3.3V I/O Voltage Regulator

A separate voltage regulator (U56) provides the 3.3V I/O voltage (VDDIO) to the PES24NT24G2.

Power-up Sequence for PES24NT24G2

During power supply ramp-up, VDDCORE must remain at least 1.0V below VDDIO at all times. There are no other power-up sequence requirements for the various operating supply voltages.

## Notes

## Heatsink Requirement

The EB-LOGAN-19 evaluation board utilizes a heatsink with integrated fan.

## Reset

The PES24NT24G2 supports two types of reset mechanisms as described in the PCI Express specification:

- *Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES24NT24G2, and the endpoints.*
- *Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the PES24NT24G2 User Manual. The EB-LOGAN-19 evaluation board provides seamless support for Hot Reset.*

### Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB-LOGAN-19 evaluation board:

- *Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES24NT24G2.*
- *Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:*
  - *Pressing a push-button switch (S3) located on EB-LOGAN-19 board*
  - *The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB-LOGAN-19.*

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES24NT24G2 while power is on.

### Downstream Reset

Single Partition Mode without Hot Plug:

When the evaluation board initially powers on it assumes the following:

- ◆ The switch is configured in single partition mode.
- ◆ Port 0 is the root port and controls the downstream port resets.
- ◆ Ports 1-23 are downstream ports.
- ◆ Hot Plug is disabled.

The following behavior should be observed:

- ◆ The resets to slots 1-23 should initially be asserted and remain this way until after the fundamental reset is initially de-asserted.
- ◆ The assertion of a fundamental reset should propagate to slots 1-23.

### Stack Configuration

The PES24NT24G2 contains four stack blocks labeled Stack 0, Stack 1, Stack 2, and Stack 3. Stacks 0 and 1 have four x1 ports each, and stacks 2 and 3 have eight x1 ports each. This provides a total of 24 ports in the device labeled port 0 through port 23. Table 2.11 lists the ports associated with each stack.

Stacks 0 and 1 have non-mergeable x1 ports. Stacks 2 and 3 may be configured as eight x1 ports, four x2 ports, two x4 ports, one x8 port, and any combinations in between. The configuration of each stack is controlled by the Stack Configuration (STK[3:2]CFG) registers. For possible configurations please refer to the device user manual.

Notes

Stack	Ports Associated with the Stack
Stack 0	0, 1, 2, 3
Stack 1	4, 5, 6, 7
Stack 2	8, 9, 10, 11, 12, 13, 14, 15
Stack 3	16, 17, 18, 19, 20, 21, 22, 23

Table 2.11 Ports in Each Stack

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.12 is sampled by the PES24NT24G2 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S5, SW8, SW9 and SW10 as defined in Table 2.13.

Signal	Description
GCLKFSEL	<b>Global Clock Frequency Select.</b> This pin specifies the frequency of the GCLKP and GCLKN signals. <b>Default: low</b>
CLKMODE[1:0]	<b>Clock Mode.</b> These pins specify the clocking mode used by switch ports. See Table 2.9 for a definition of the encoding of these signals. The value of these signals may be overridden by modifying the Port Clocking Mode (PCLKMODE) register.
RSTHALT	<b>Reset Halt.</b> When this pin is asserted during a switch fundamental reset sequence, the switch remains in a quasi-reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the quasi-reset state when the RSTHALT bit is cleared in the SWCTL register by an SMBus master. Refer to section Switch Fundamental Reset on page 3-2 for further details. <b>Default: low</b>
SSMBADDR[2:1]	<b>Slave SMBus Address.</b> SMBus address of the switch on the slave SMBus. <b>Default: 0x3</b>
SWMODE[3:0]	<b>Switch Mode.</b> These pins specify the switch operating mode.
STK2CFG[4:0]	<b>Stack 2 Configuration.</b> These pins select the configuration of stack 2 during a switch fundamental reset.
STK3CFG[4:0]	<b>Stack 3 Configuration.</b> These pins select the configuration of stack 3 during a switch fundamental reset.

Table 2.12 Boot Configuration Vector Signals

Location	Signal	Default
SW10[2]	GCLKFSEL	ON
SW10[4]	RSTHALT	ON
SW10[5]	SSMBADDR[2]	OFF
SW10[6]	SSMBADDR[1]	OFF

Table 2.13 Boot Configuration Vector Switch SW10

Notes

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I<sup>2</sup>C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consists of an SMBus clock pin and an SMBus data pin.

The PES24NT24G2 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device full access to all software-visible registers. The Master SMBus interface provides a connection to the external serial EEPROM used for initialization and the I/O expanders used for hot-plug signals.

SMBus Slave Interface

On the PES24NT24G2 board, the slave SMBus interface is accessible through a 4-pin header as described in Table 2.14.

Slave SMBus Interface Connector J71	
Pin	Signal
1	SDA
2	GND
3	SCL
4	NC

Table 2.14 Slave SMBus Interface Connector

For a fixed address, the SMBus address of the PES24NT24G2 slave interface is **0b1110111** by default and is configurable using DIP Switches SW10[5] and SW10[6] as described in Table 2.15.

Slave Interface Address Configuration	
Address Bit	Signal
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	1
4	0
5	1
6	1
7	1

Table 2.15 SMBus Slave Interface Address Configuration

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- *Byte and Word Write/Read*
- *Block Write/Read*

Notes

SMBus Master Interface

Connected to the master SMBus interface are twenty-two 16-bit I/O Expanders (MAX7311AUG) and a serial EEPROM, U77 (24LC512). The I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The lower three bits of the bus address for the I/O Expander 0 through I/O Expander 20 are fixed through the stuffing resistor as 0x20, 0x22, 0x24, 0x26, 0x28, 0x2A, 0x2C, 0x2E, 0x50, 0x52, 0x54, 0x56, 0x58, 0x5A, 0x5C, 0x5E, 0xB0, 0xA2, 0xA4, 0xA6, 0xA8, and 0xAA, respectively.

**Note:** Hot-plug is not implemented when the PES24NT24G2 is installed.

The seven bits address for the selected EEPROM device is fixed at **0b1010\_000** by default.

JTAG Header

The EB-LOGAN-19 provides a JTAG connector J73 for access to the PES24NT24G2 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 14-pin connector. Refer to Table 2.16 for the JTAG Connector J73 pin out.

JTAG Connector J73					
Pin	Signal	Direction	Pin	Signal	Direction
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—
11	3.3V		12	N/C	—
13	GND	—	14	3.3V	

Table 2.16 JTAG Connector Pin Out

PCI Express Connectors

Pin	Side A		Side B	
	1	+12V	12V power	PRSNT1#
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				

Table 2.17 PCI Express x8 Connector Pinout (Part 1 of 3)

## Notes

Pin	Side A		Side B	
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground

Table 2.17 PCI Express x8 Connector Pinout (Part 2 of 3)

Notes

Pin	Side A		Side B	
	47	GND	Ground	PERp7
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground

Table 2.17 PCI Express x8 Connector Pinout (Part 3 of 3)

Notes

EB-LOGAN-19 Board Figure

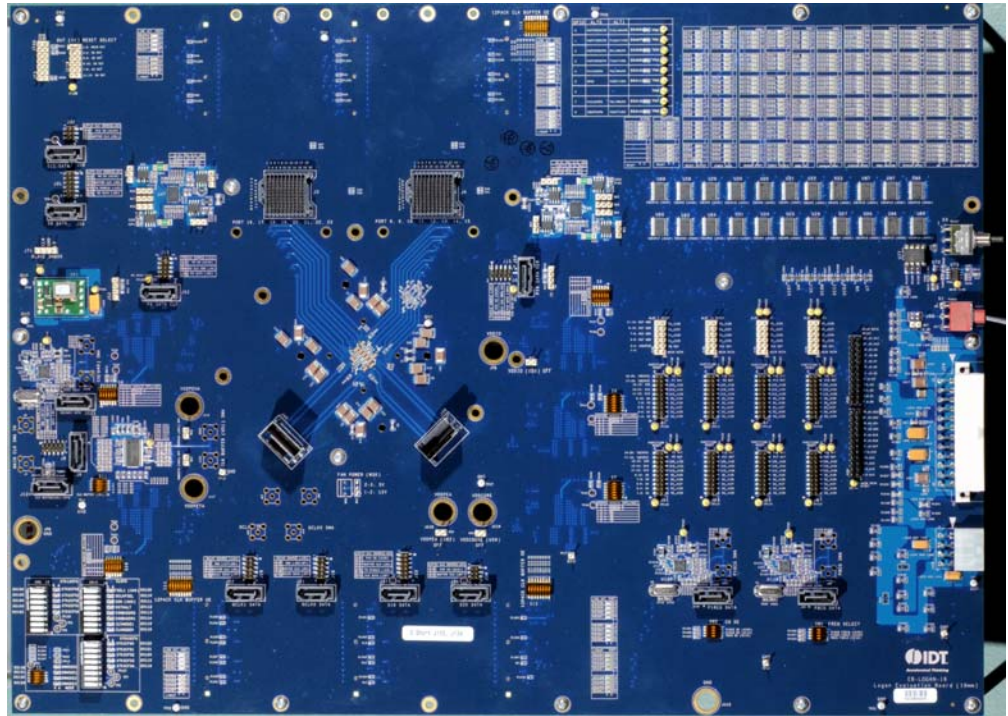


Figure 2.9 EB24NT24G2 Evaluation Board

Notes



# Software for the EB-LOGAN-19 Eval Board

## Notes

### Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB-LOGAN-19 evaluation board using the device management software.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT FTP site and also at [my.idt.com](http://my.idt.com). For more information, please go to: <http://www.idt.com/?app=TechSupport&prodFamily=PCIe%20Switches> or email IDT at [ssdhelp@idt.com](mailto:ssdhelp@idt.com).

### Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES24NT24G2 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES24NT24G2 or through the SMBUS salve interface available on the IDT PCIe switch.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES24NT24G2, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front-end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES24NT24G2 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software is expected to work on Linux (/sys interface) and MS Windows XP. It may function well on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

The actual program name of the Device Management Software is "PCIeBrowser" (an executable file under Windows or Linux). Revision 5.0.1 or later is required for devices in the PES24NT24G2 product family family.

### Device Drivers

The PES24NT24G2 and other members of this switch family offer Non-Transparent Bridging and built-in DMA capability inside the device. Device drivers are needed to take advantage of these features. Sample code for these drivers is available from IDT for the Linux operating system. Additionally, there a few other software packages available from IDT. These packages are not related to the evaluation board per se, and therefore not listed here. However, several of these packages may prove to be useful for specific device or system functionality. For more information, please go to <http://www.idt.com/?app=TechSupport&prodFamily=PCIe%20Switches> or email IDT at [ssdhelp@idt.com](mailto:ssdhelp@idt.com).

Notes



# Schematics


Notes

Schematics

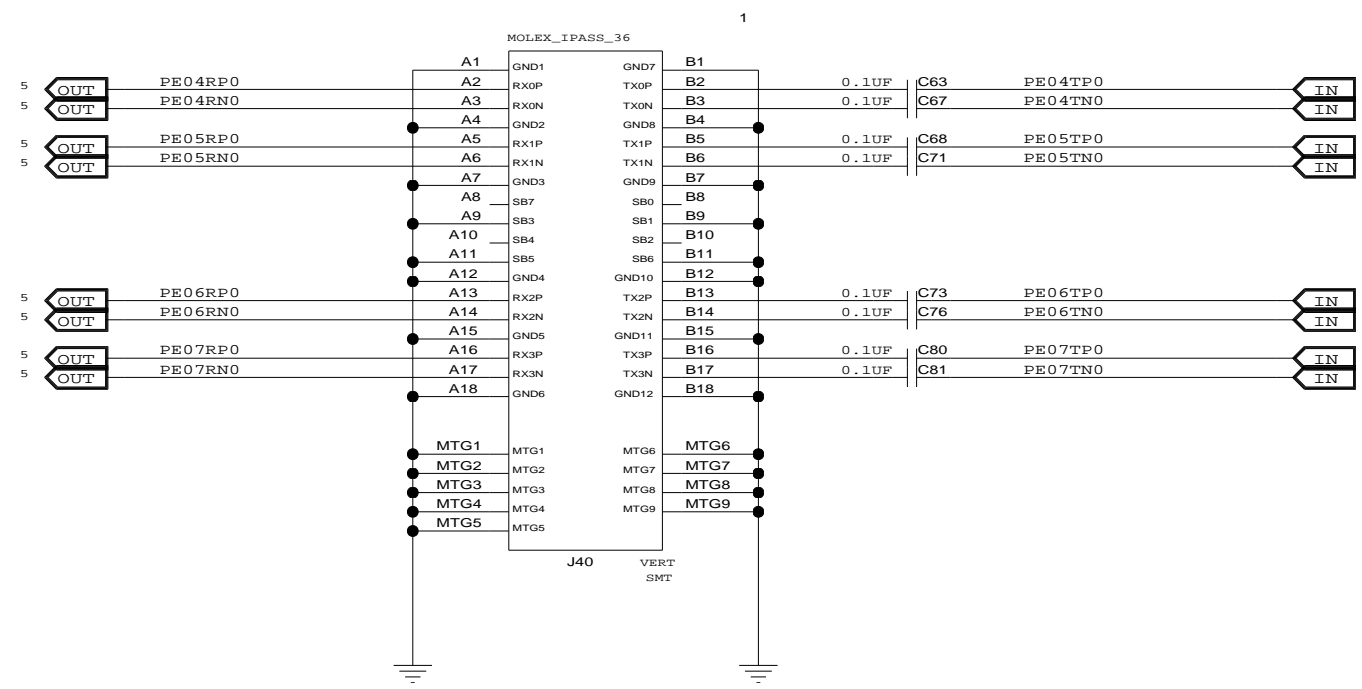
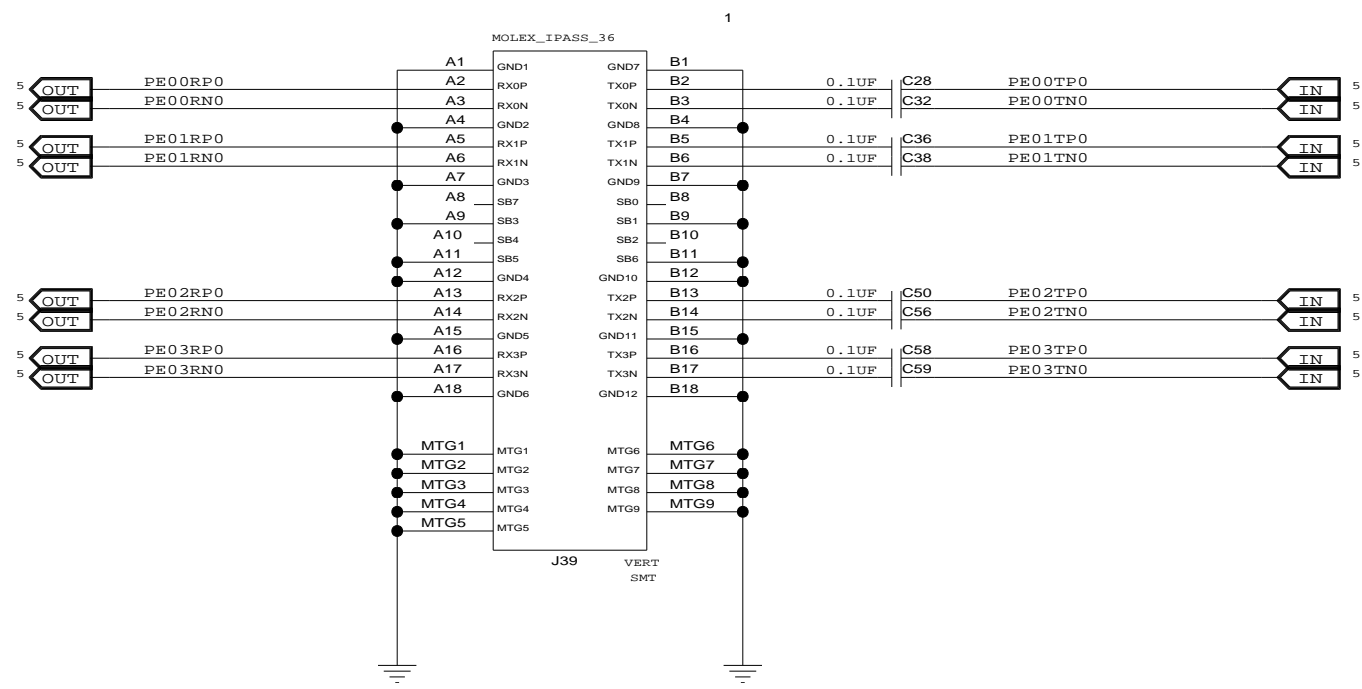
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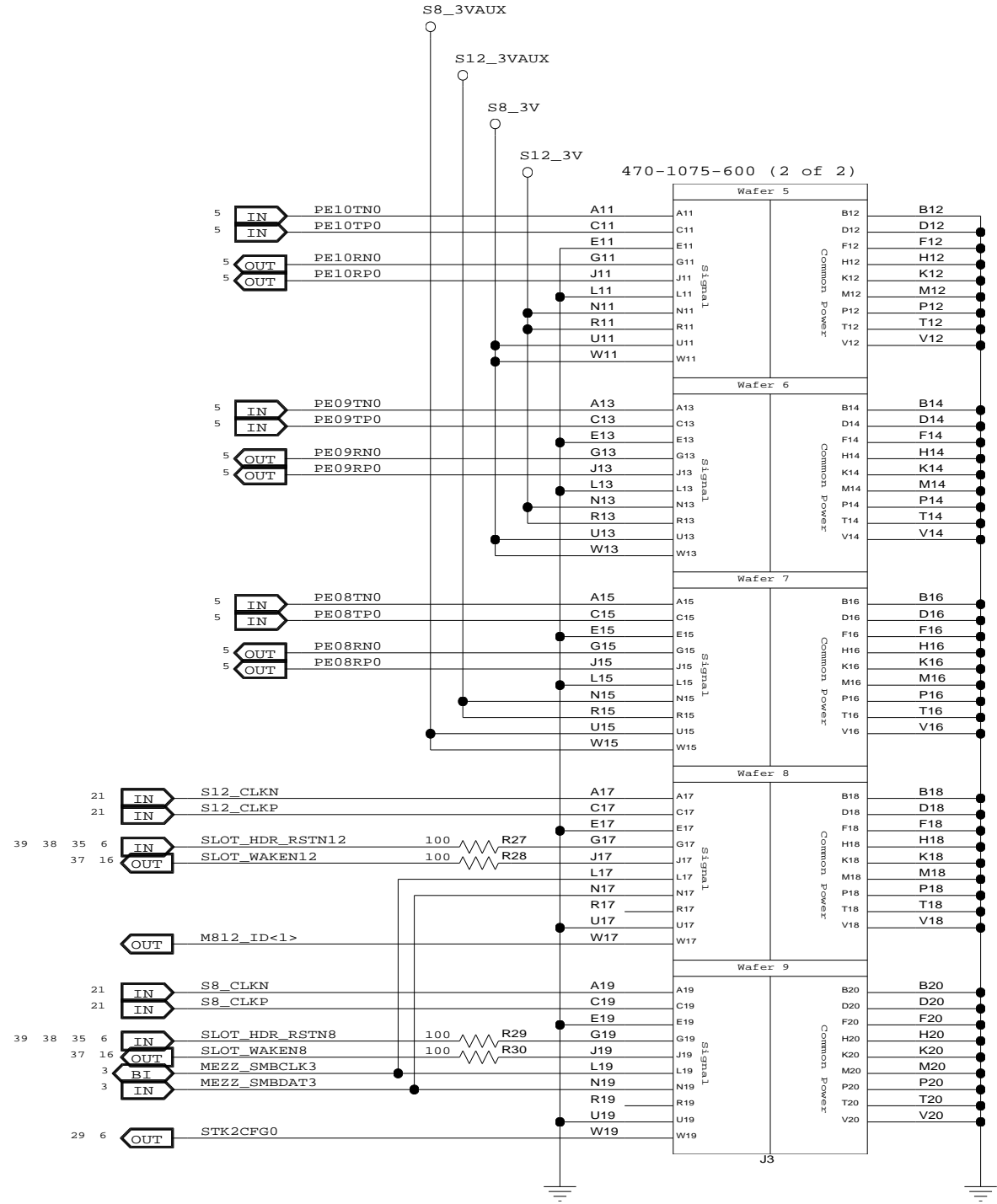
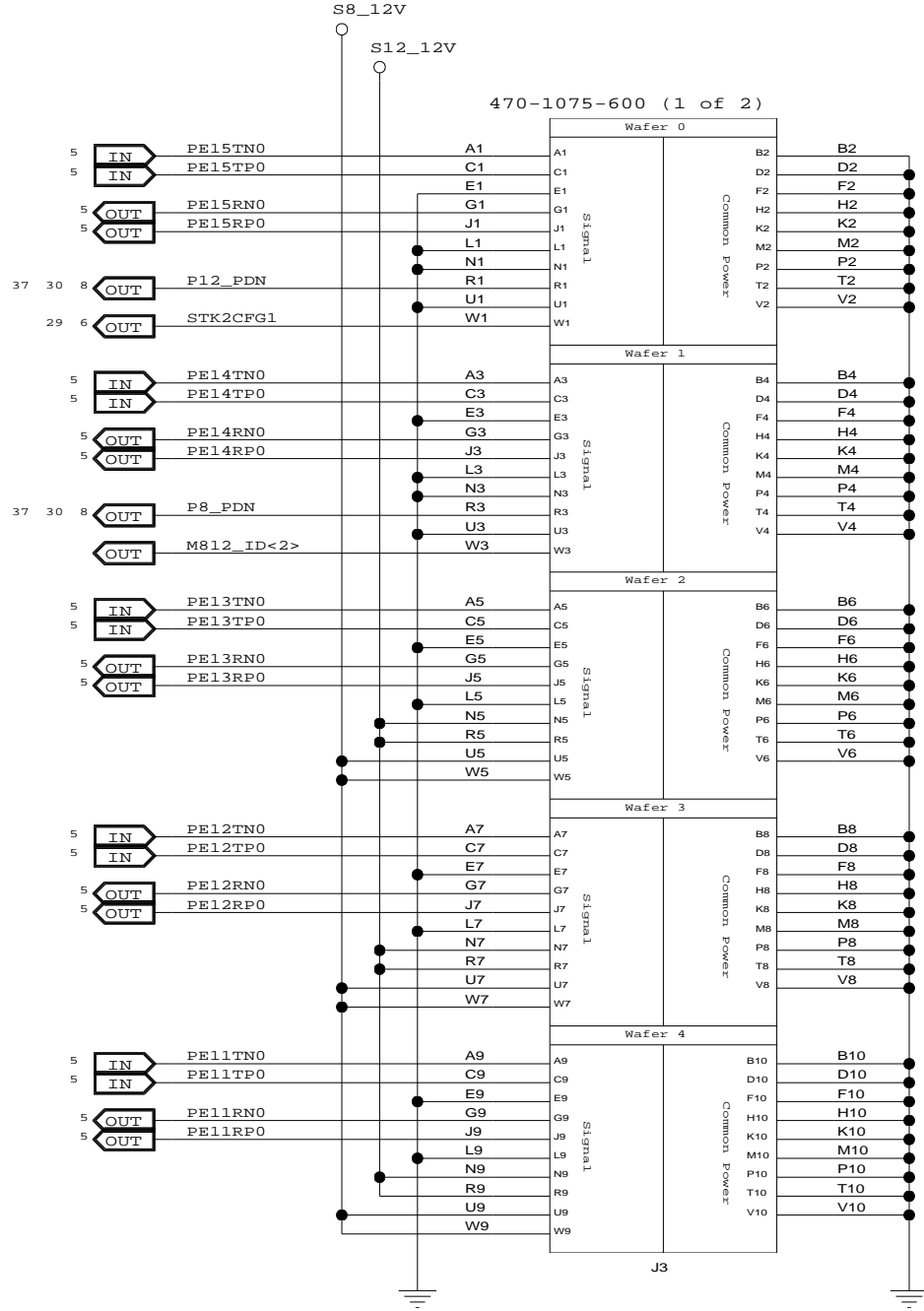
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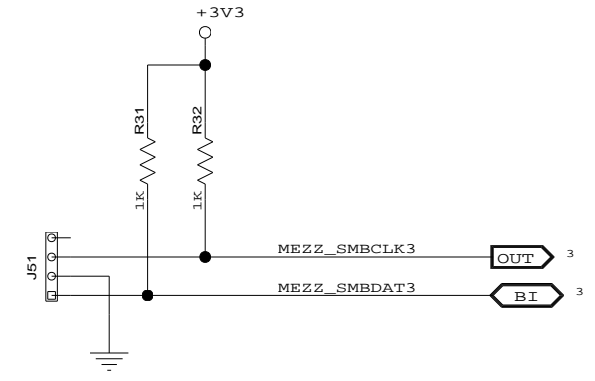


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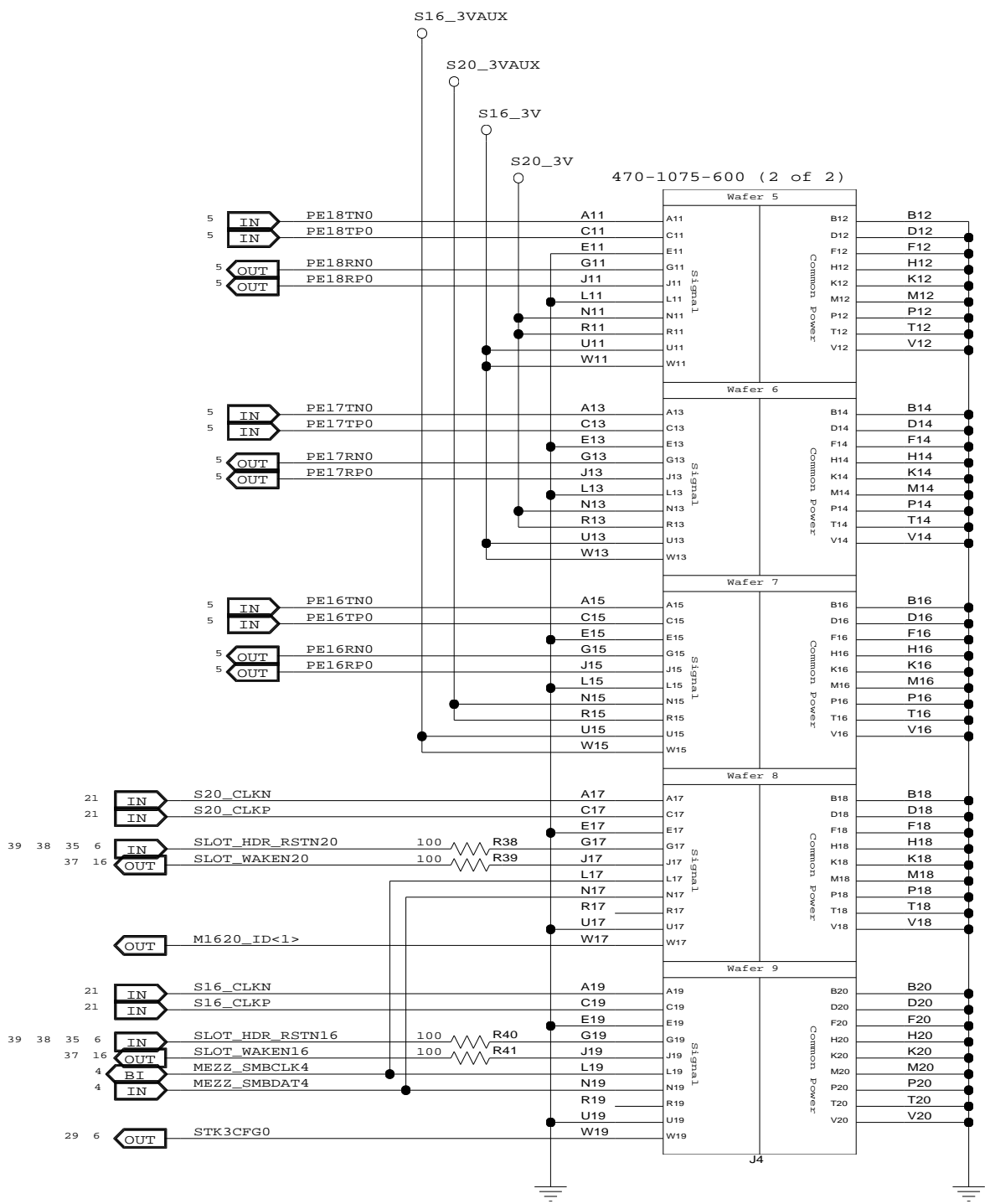
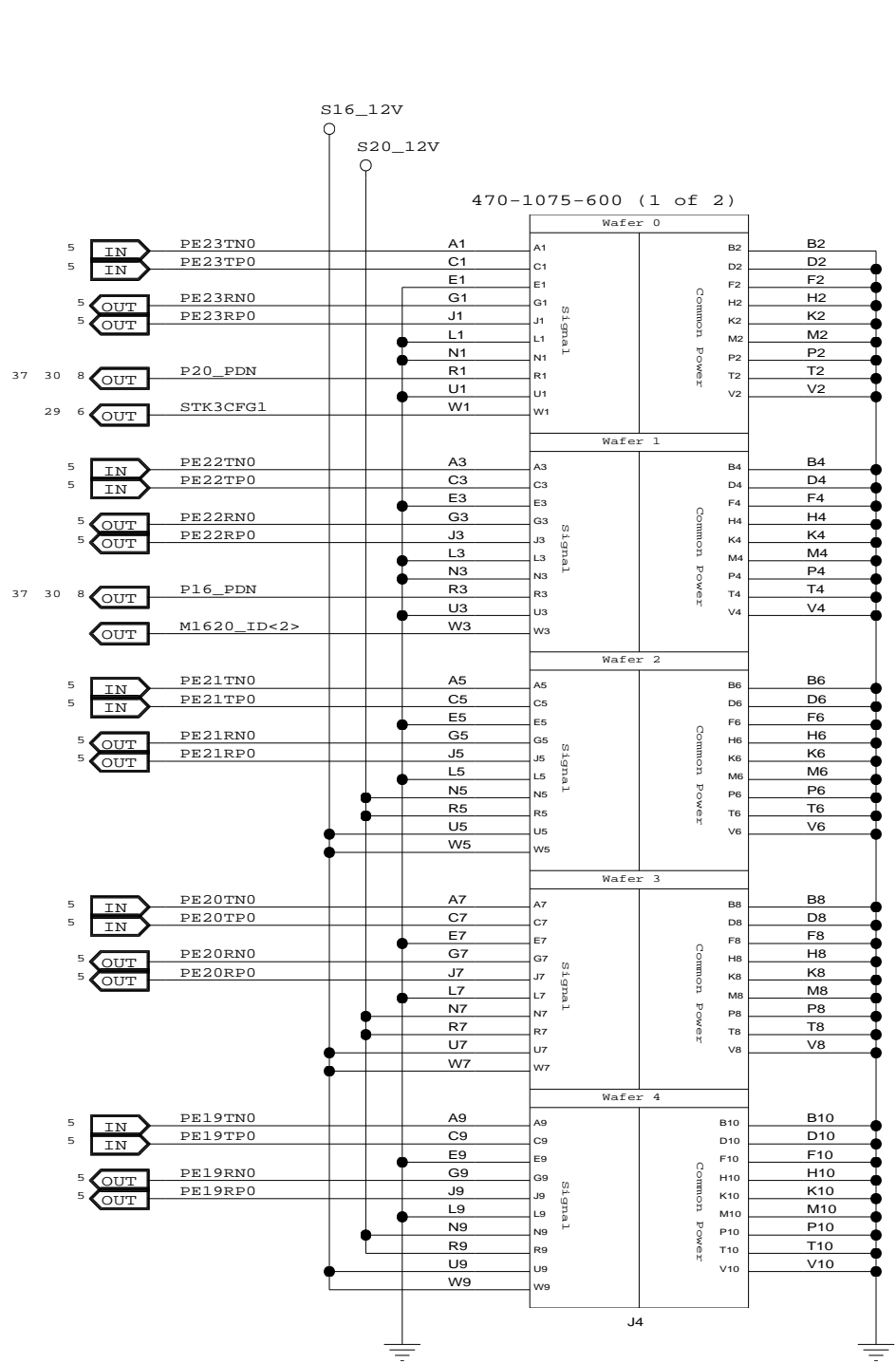


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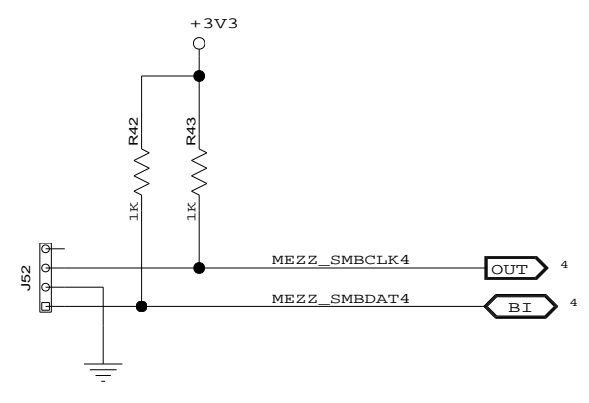


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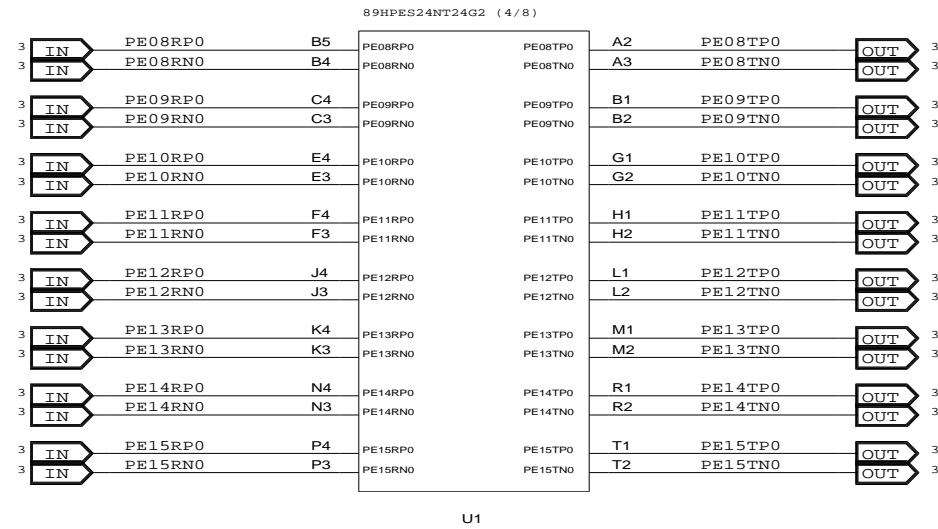
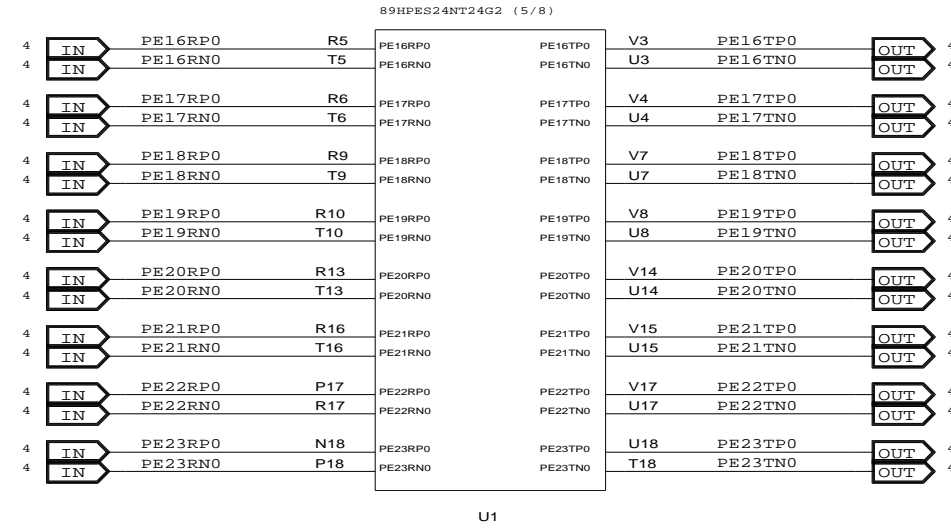
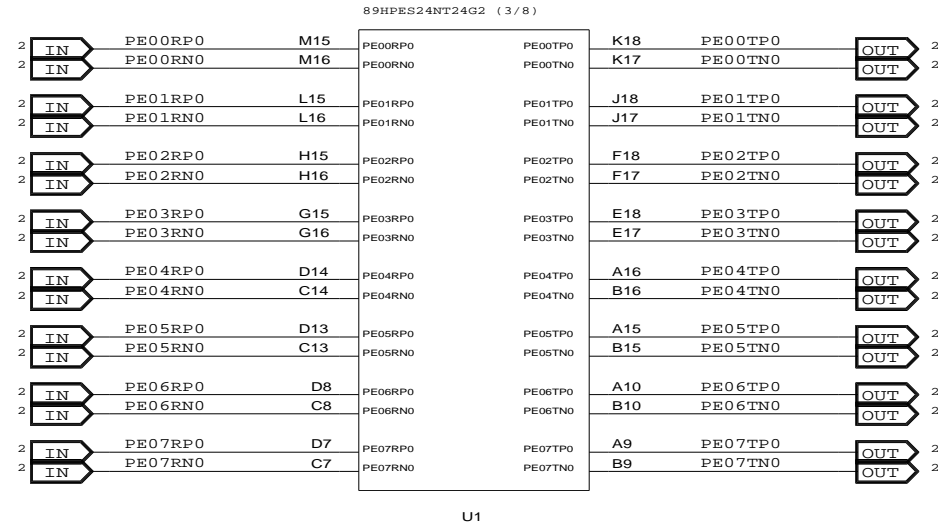


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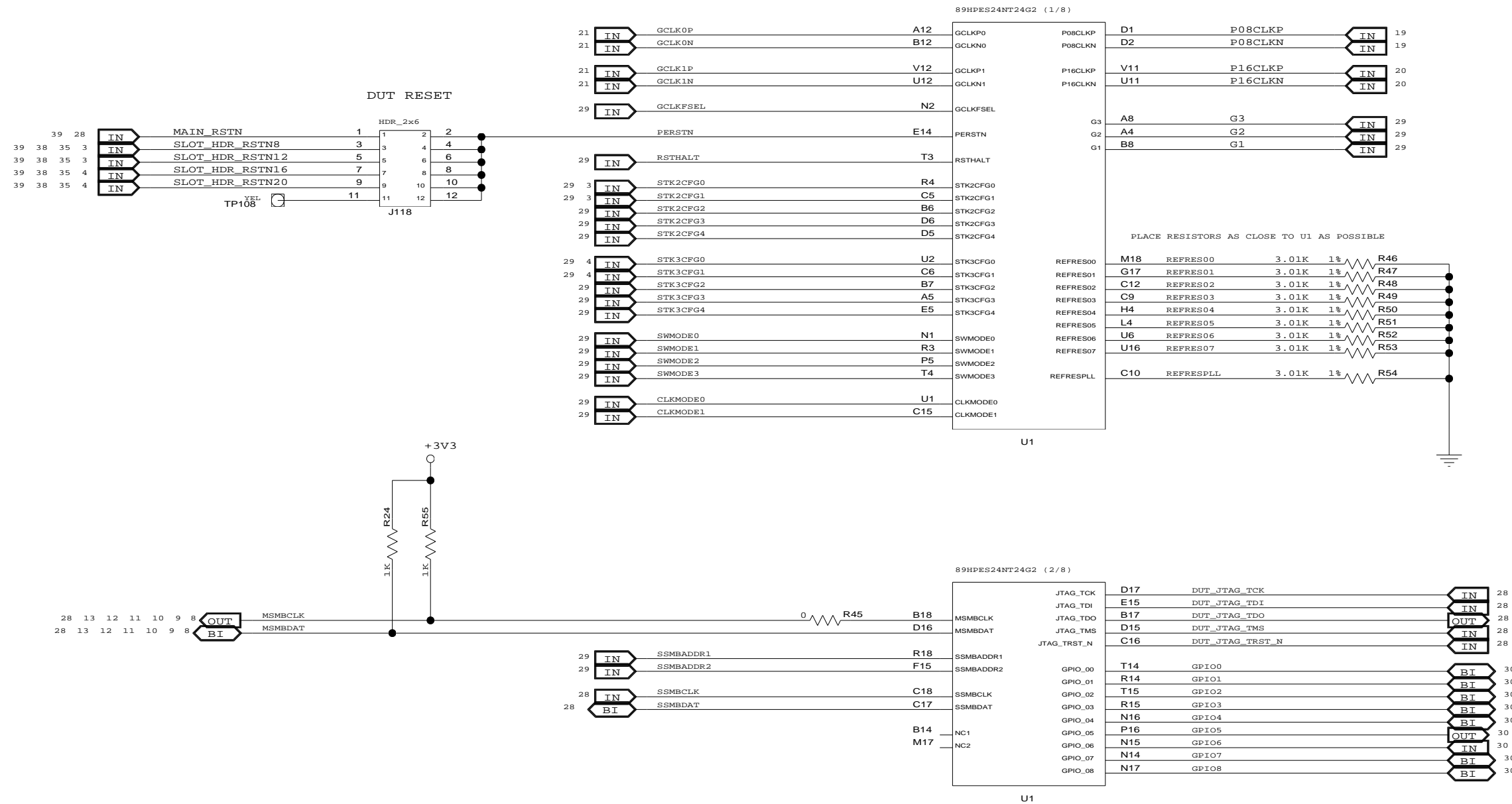
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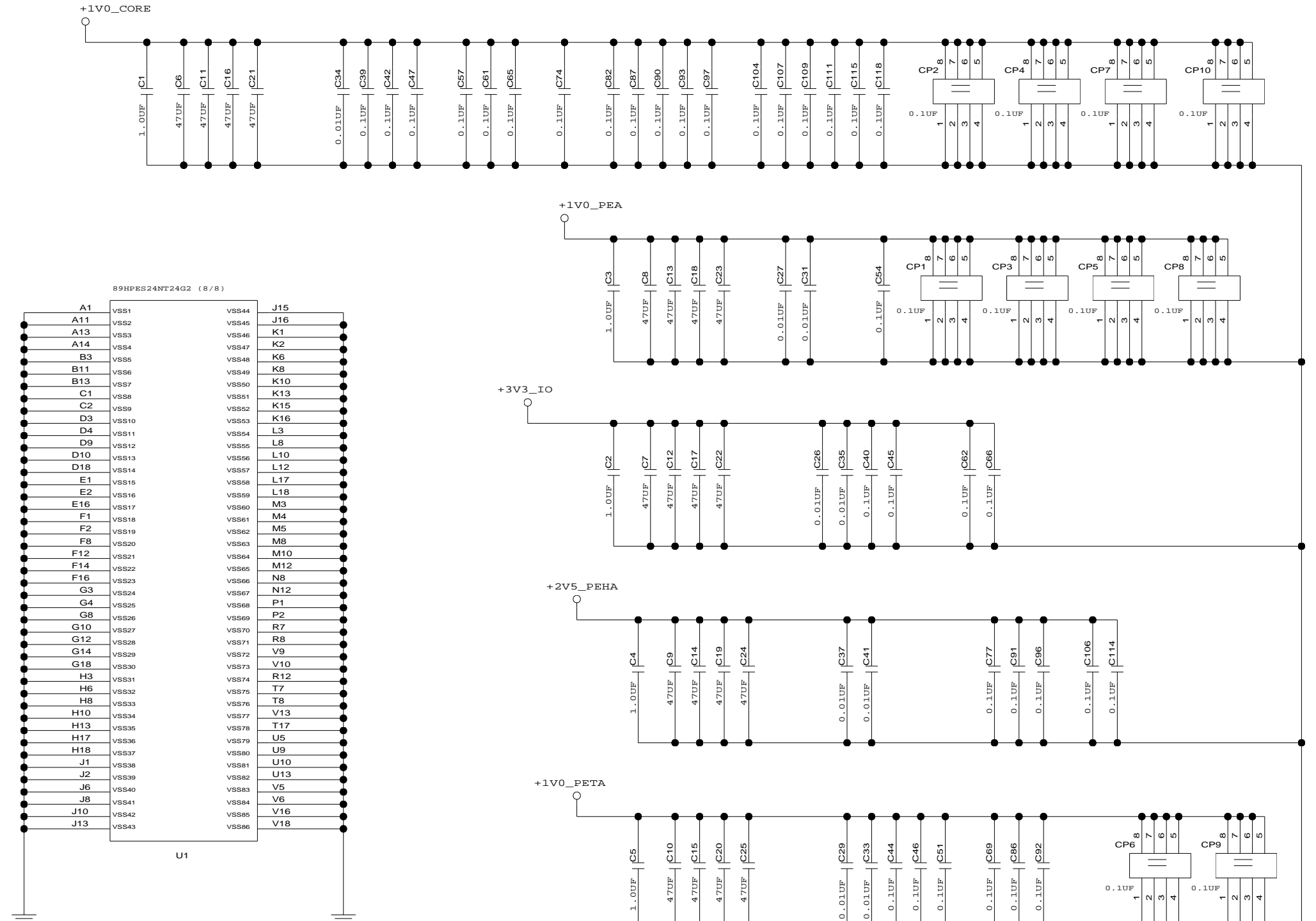
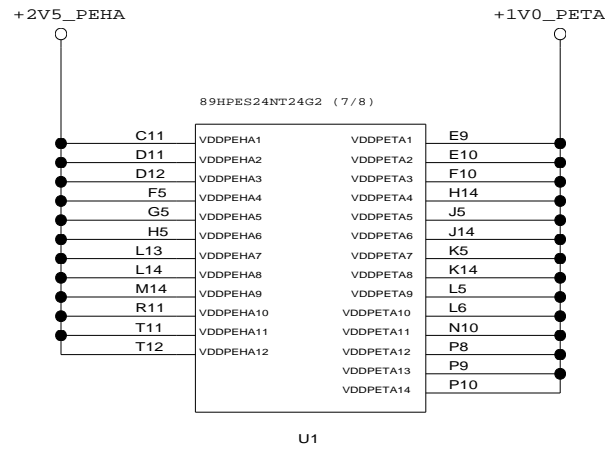
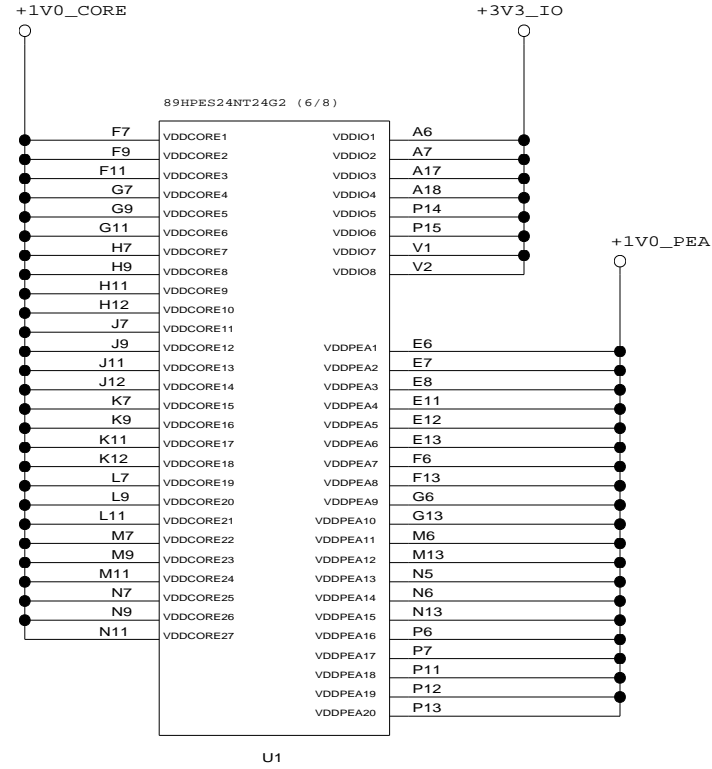
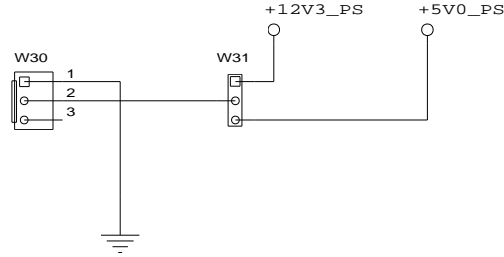
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 2 12V/5V  
 3 NC



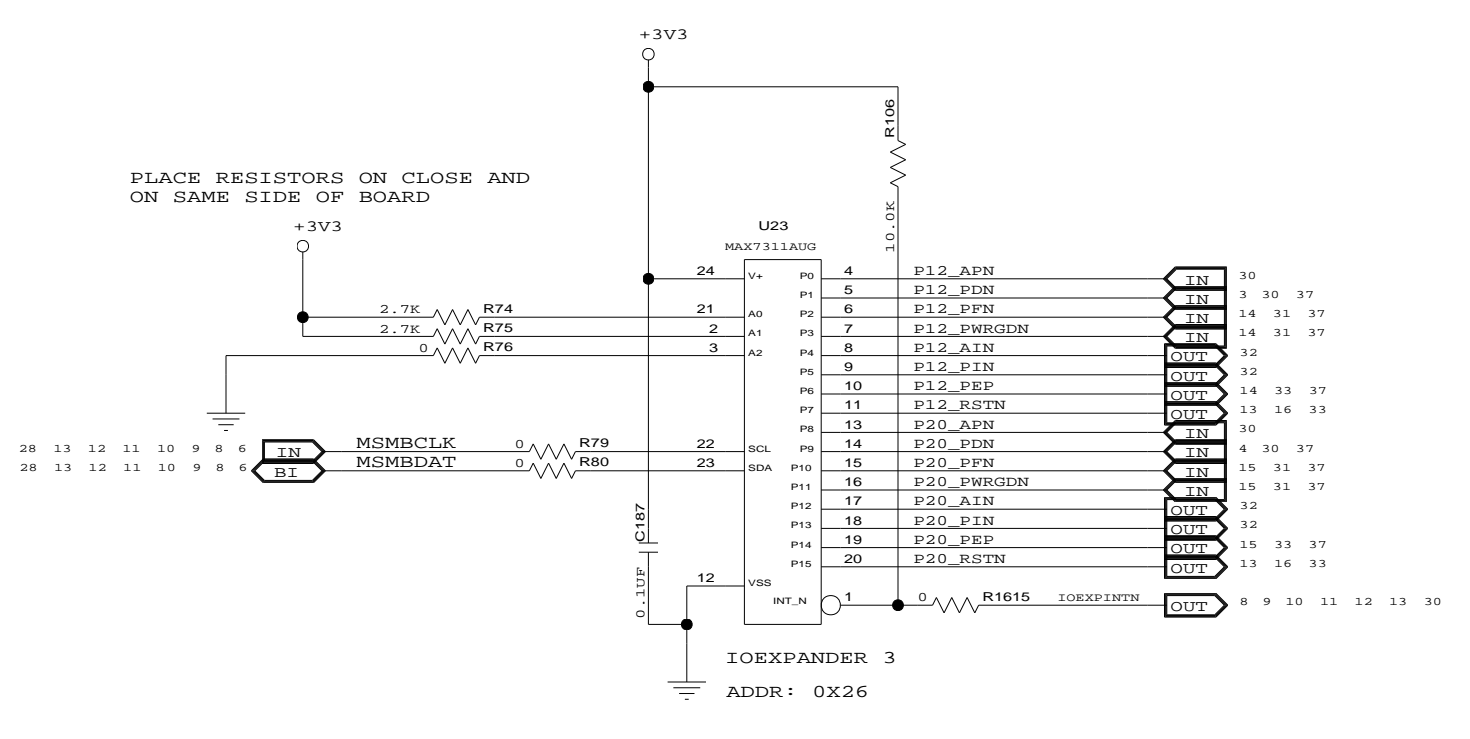
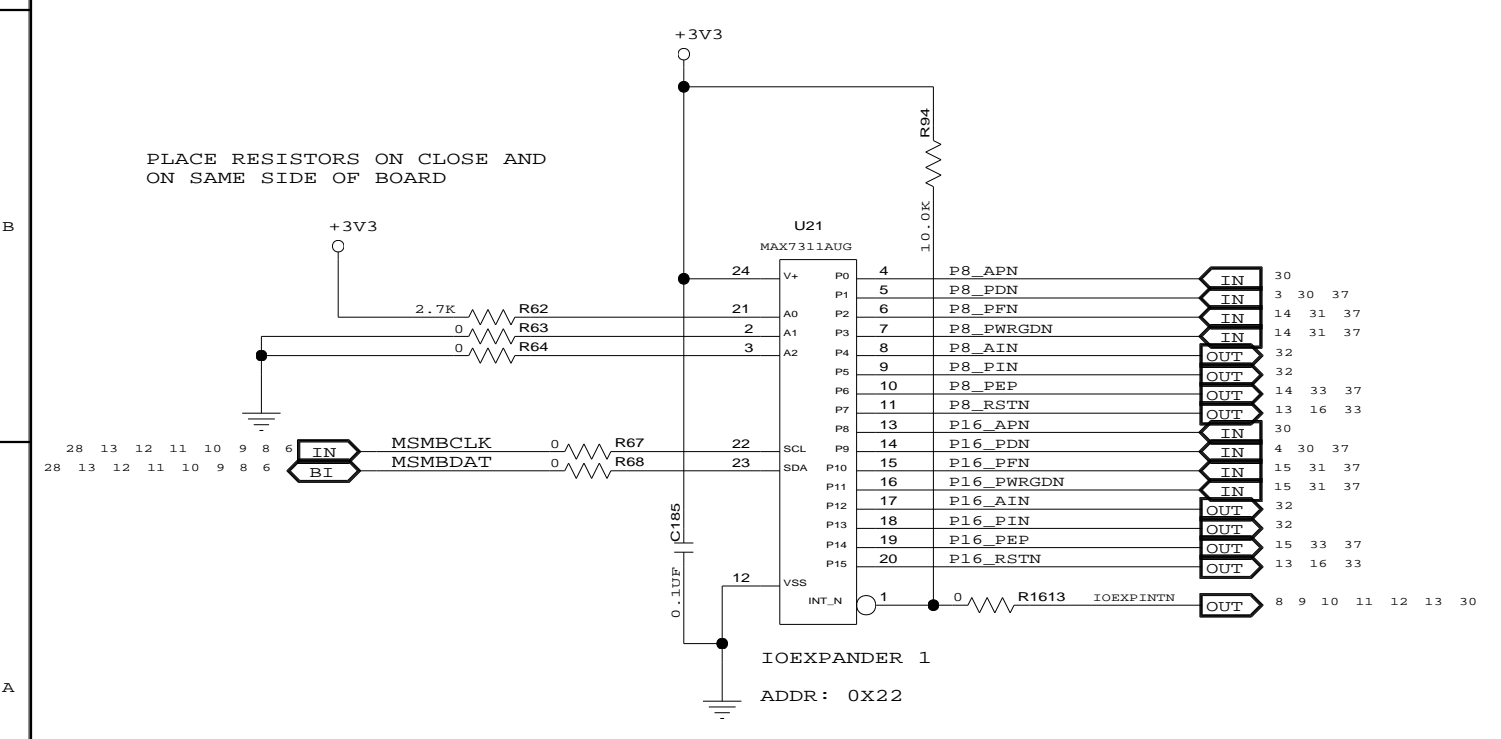
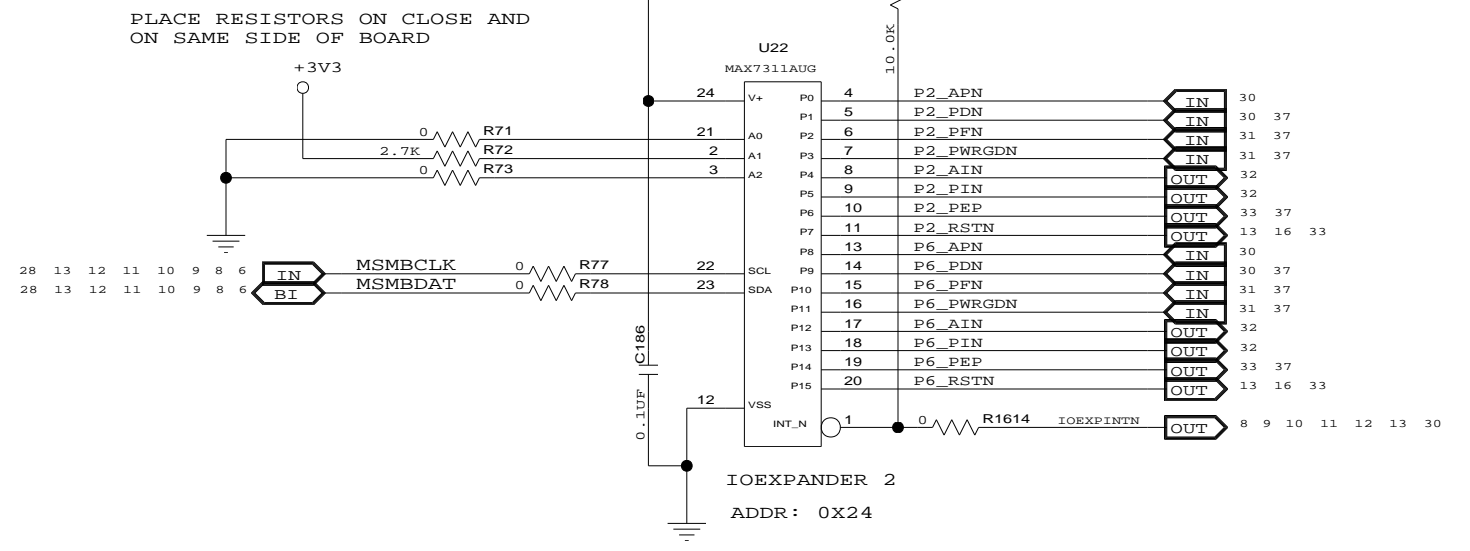
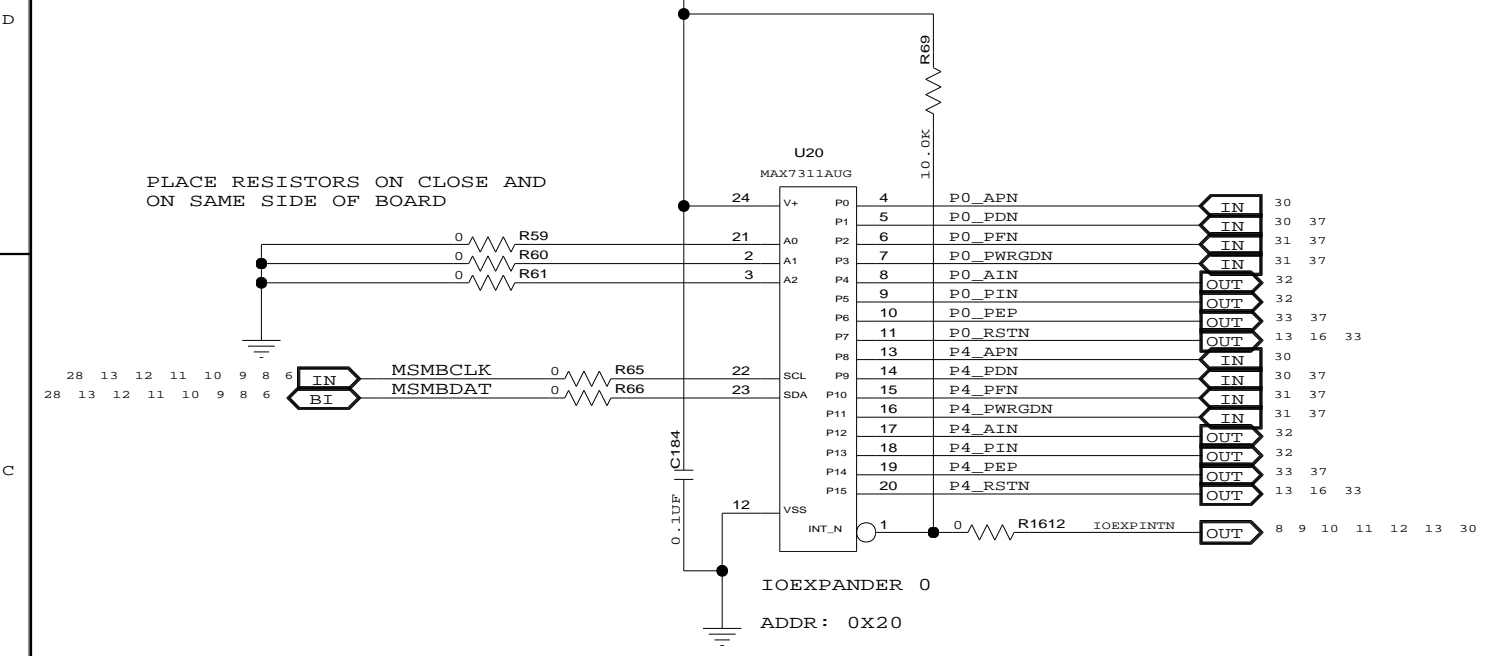



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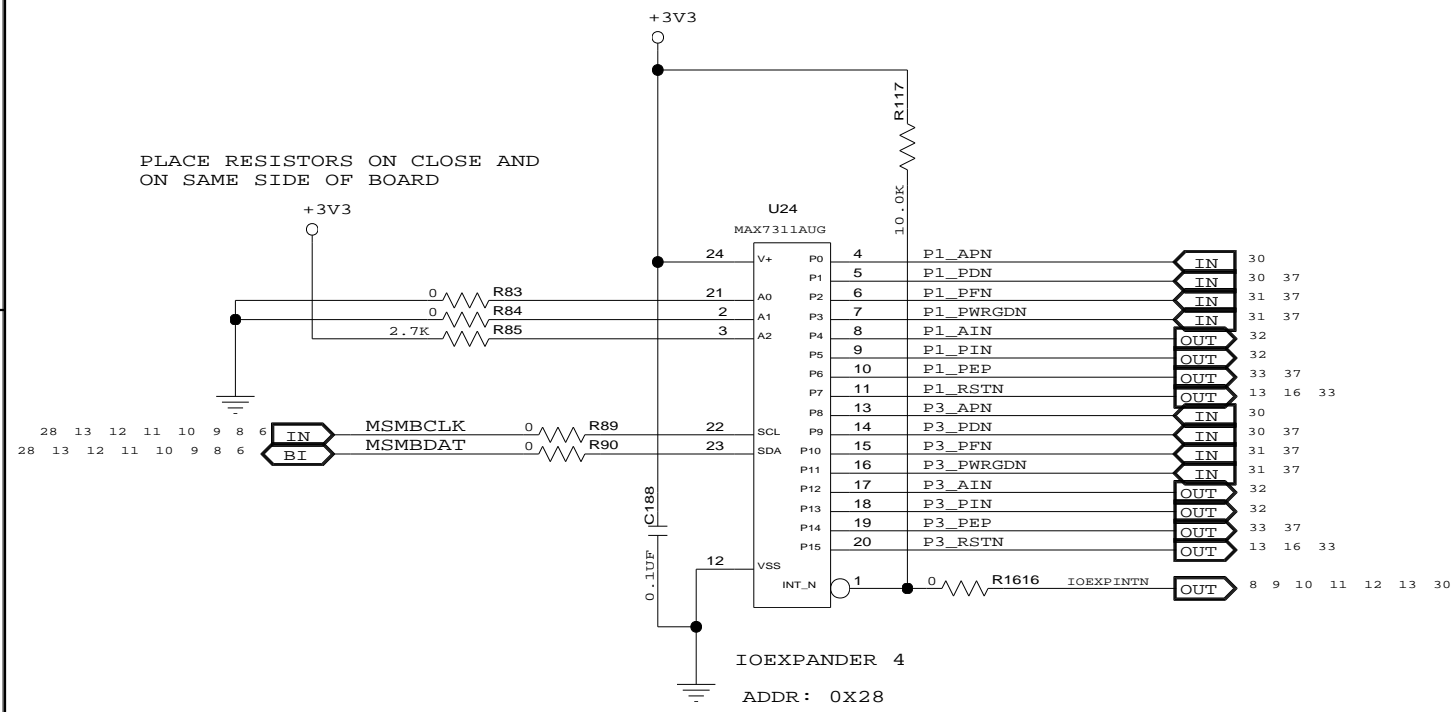
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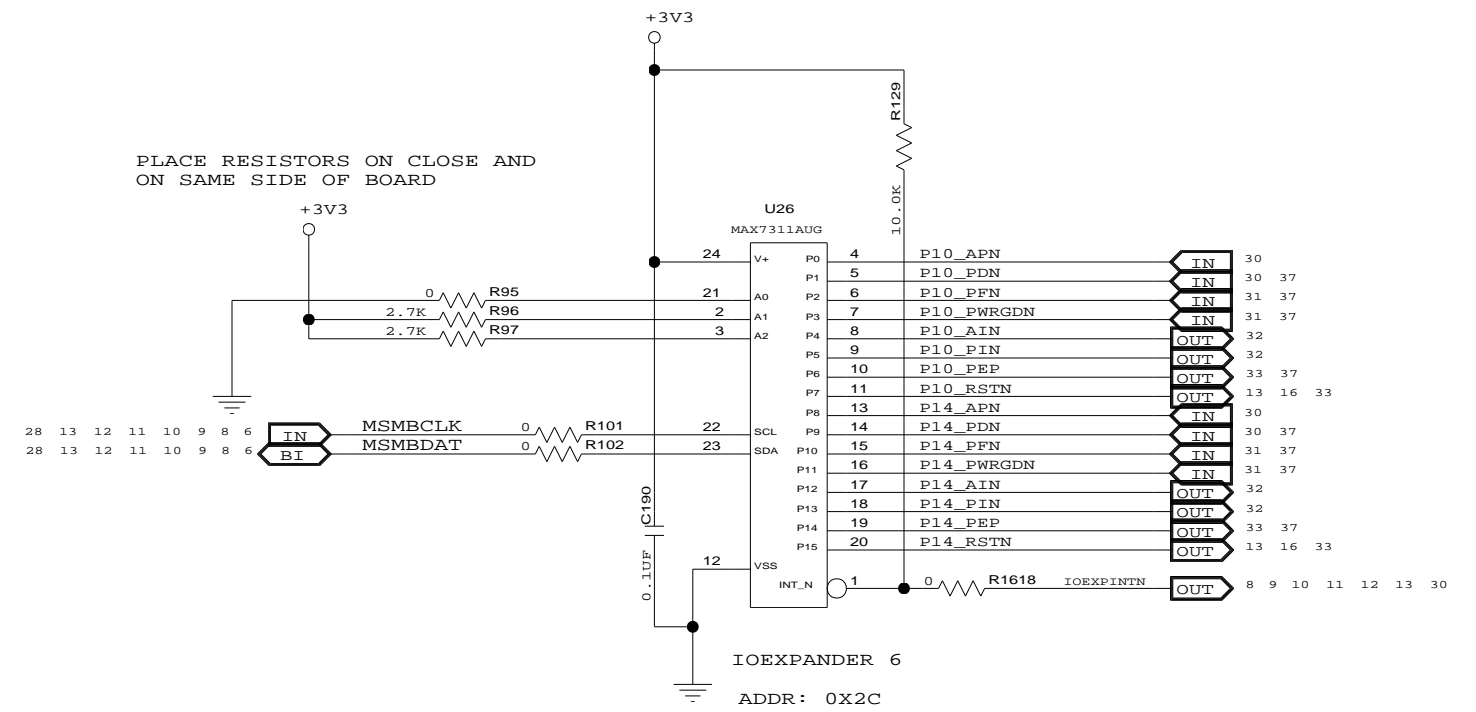
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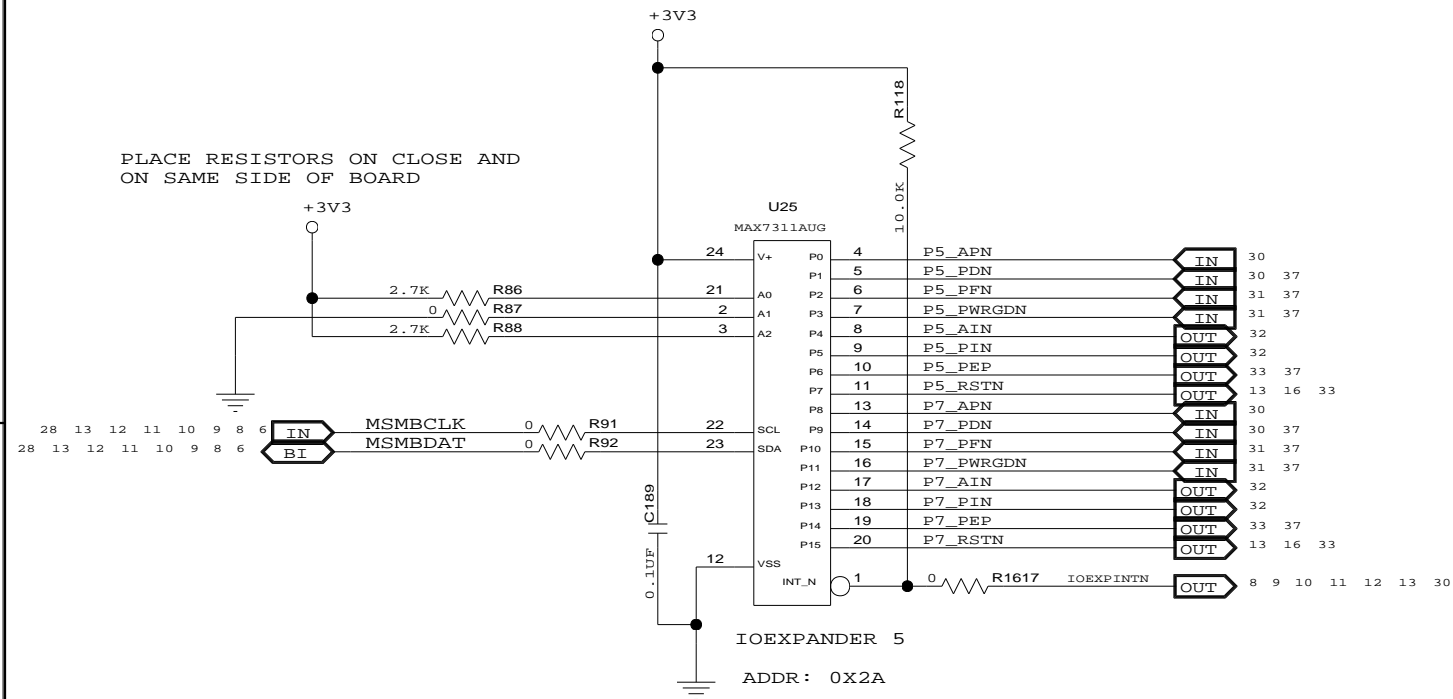
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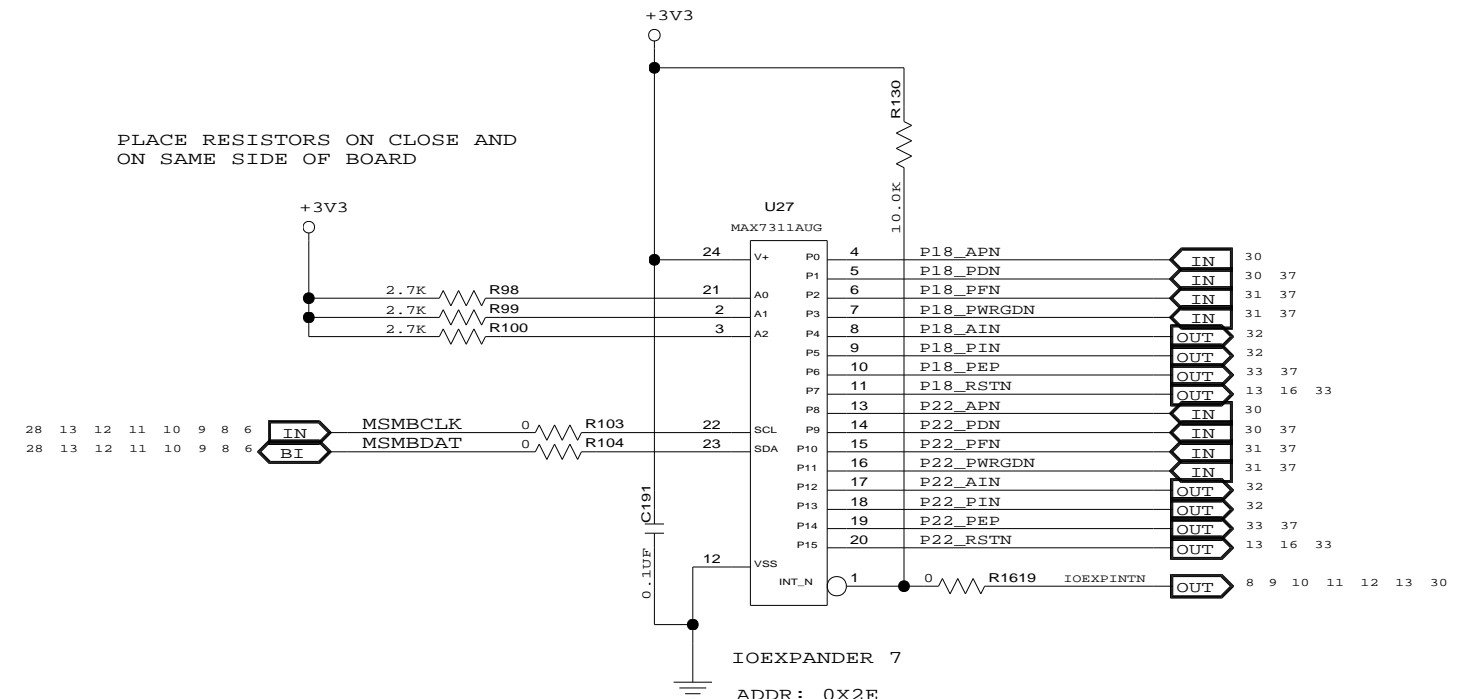
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PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD



PLACE RESISTORS ON CLOSE AND ON SAME SIDE OF BOARD

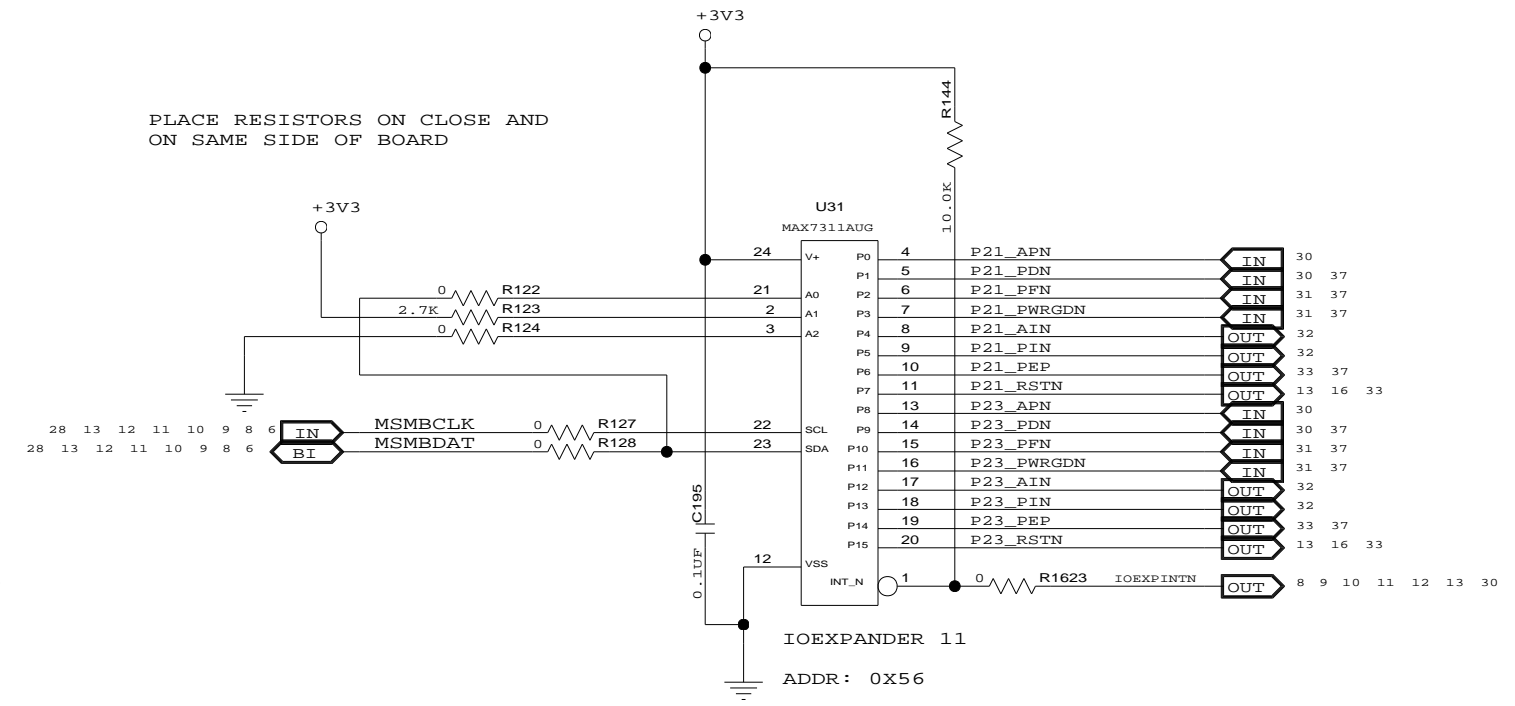
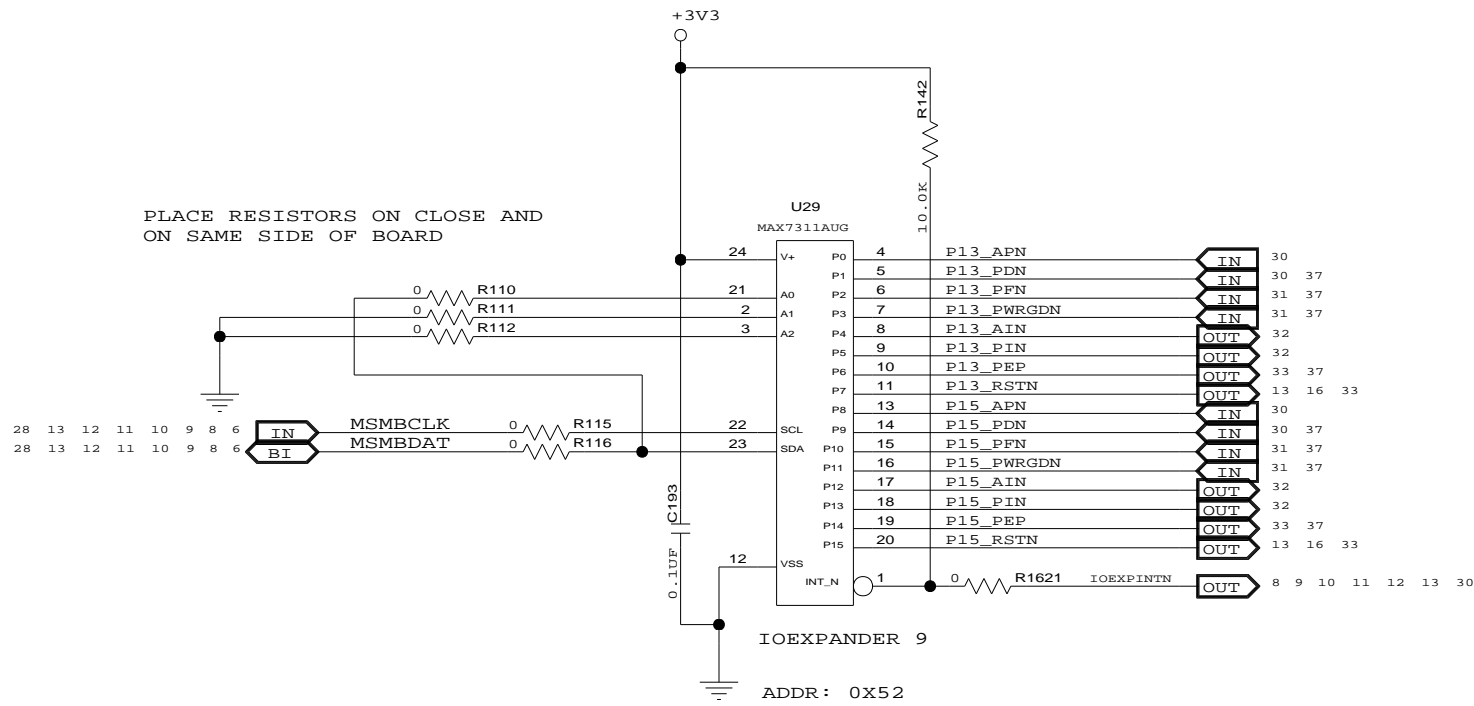
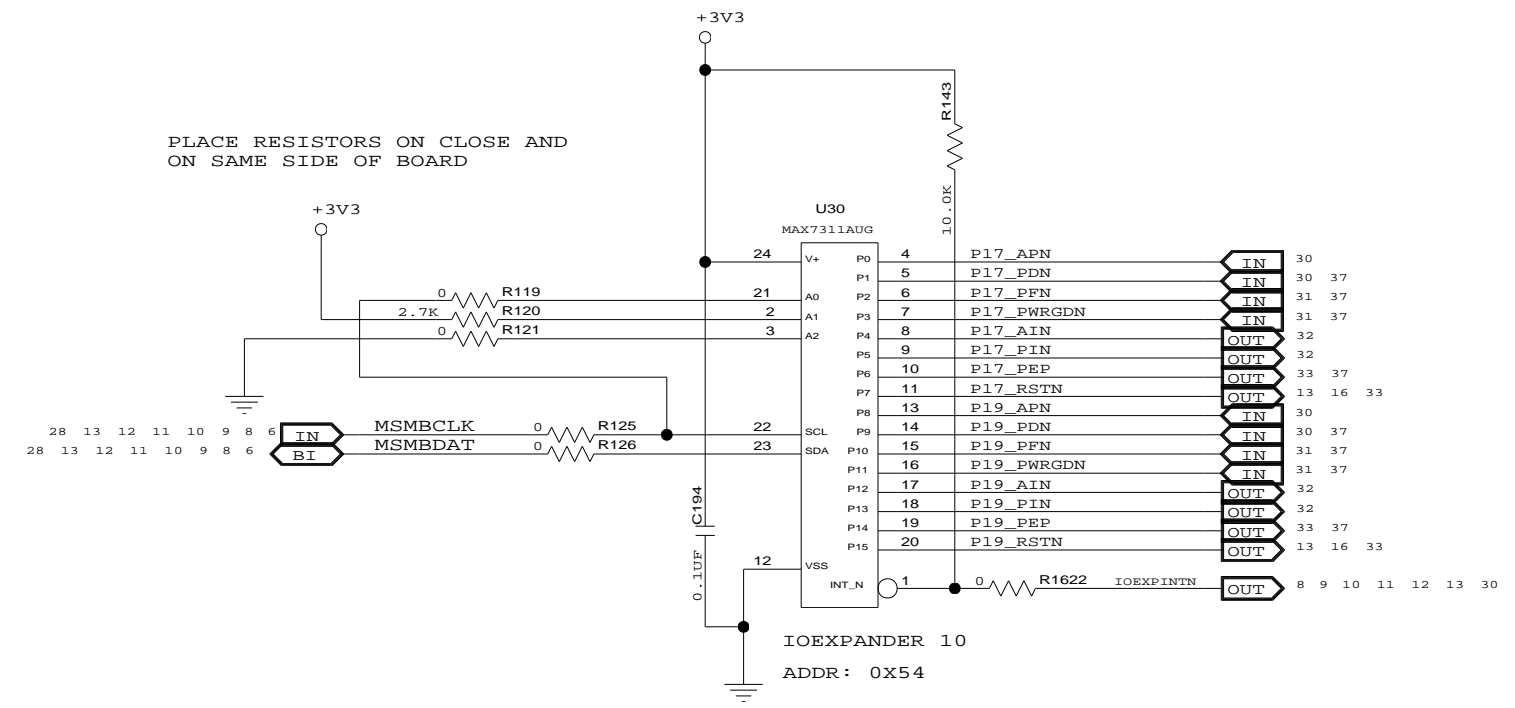
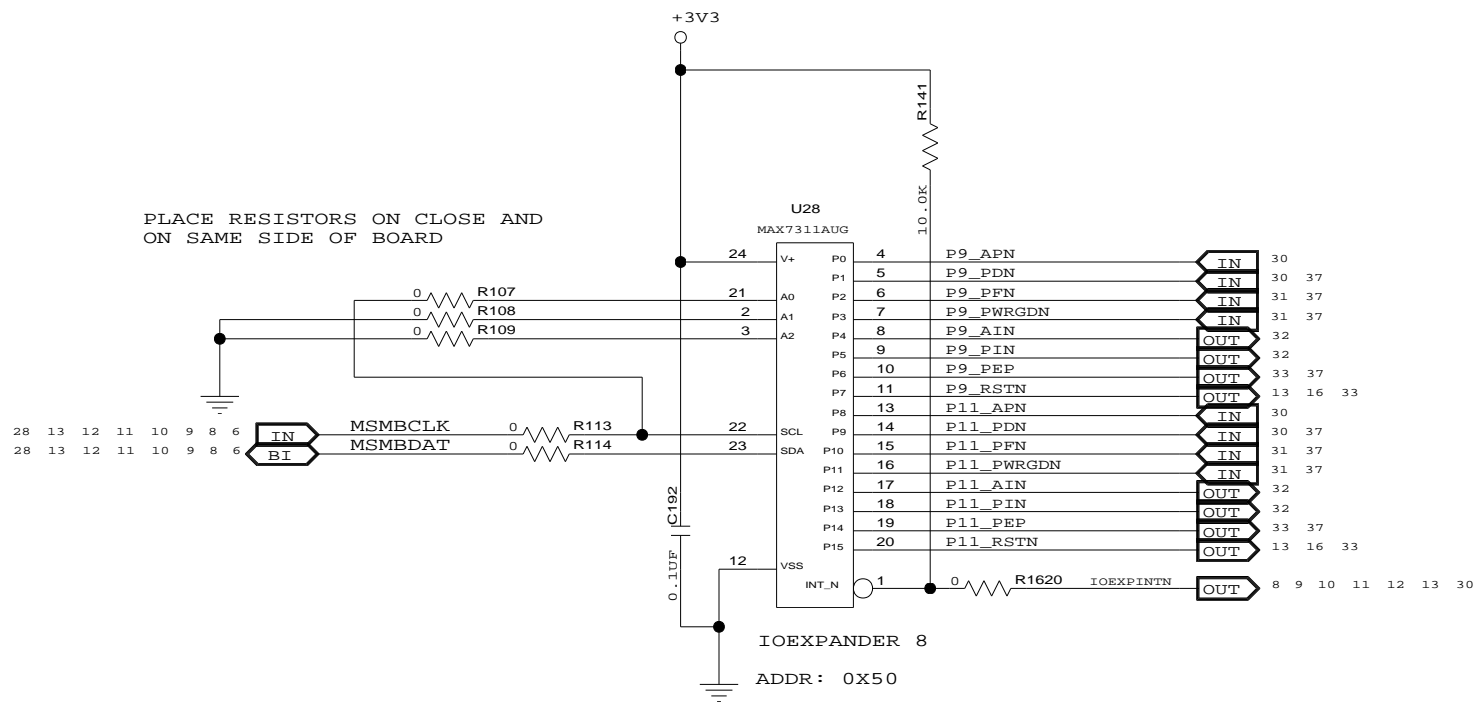


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IOEXPANDER 4-7

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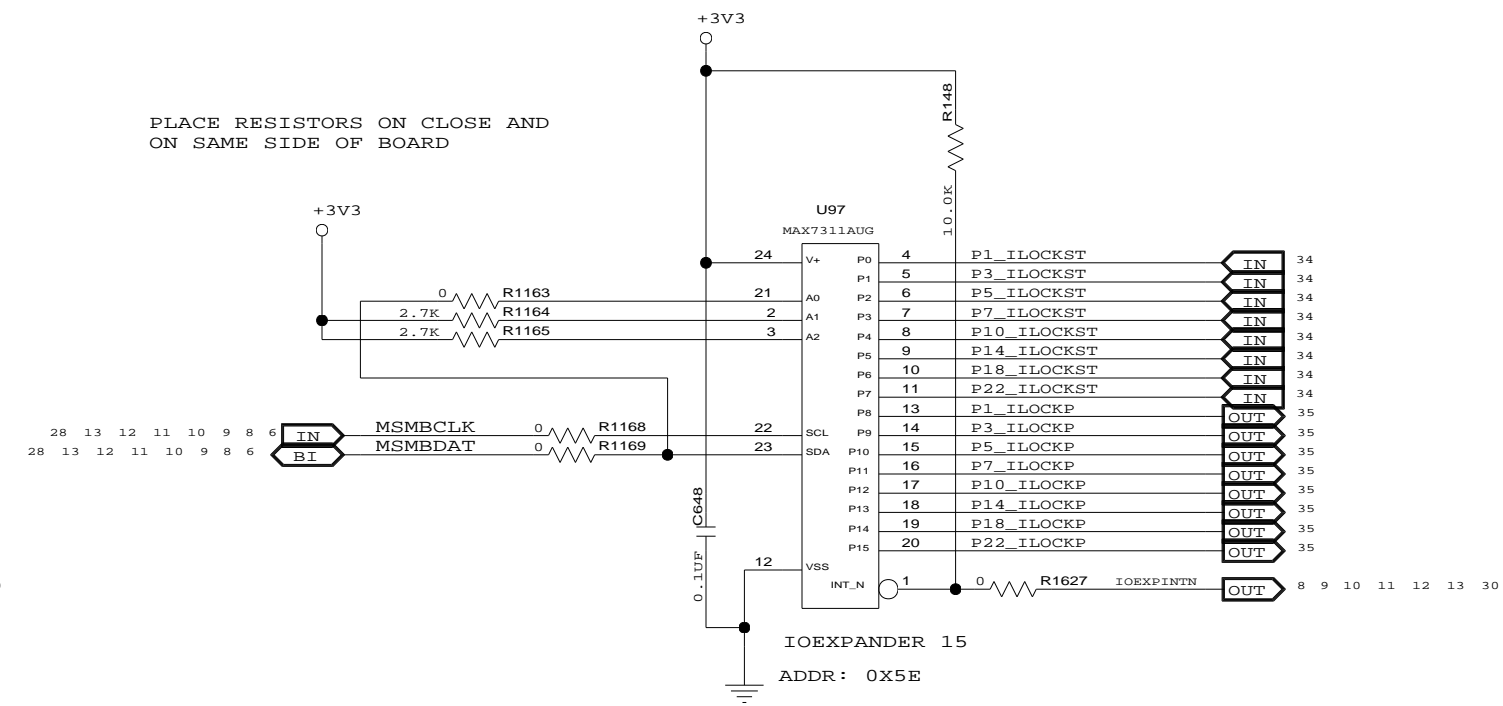
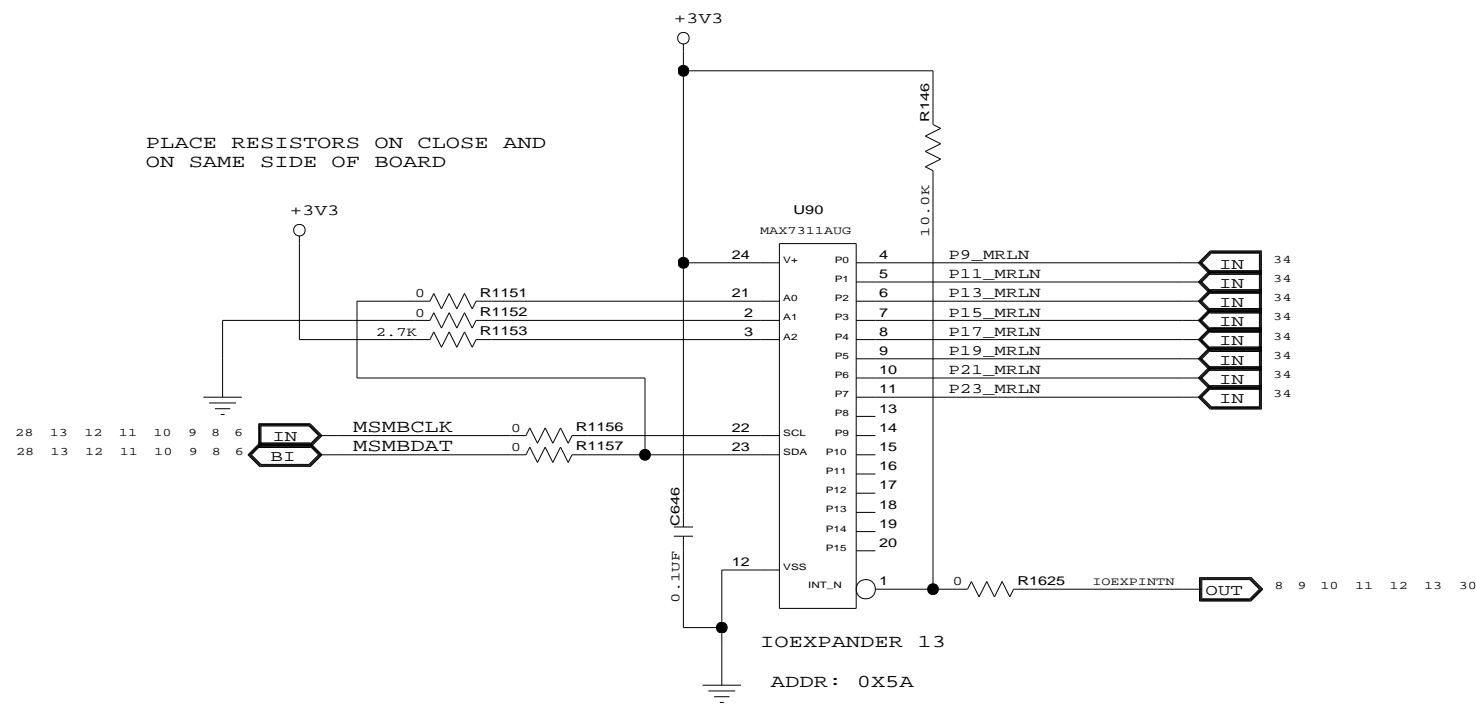
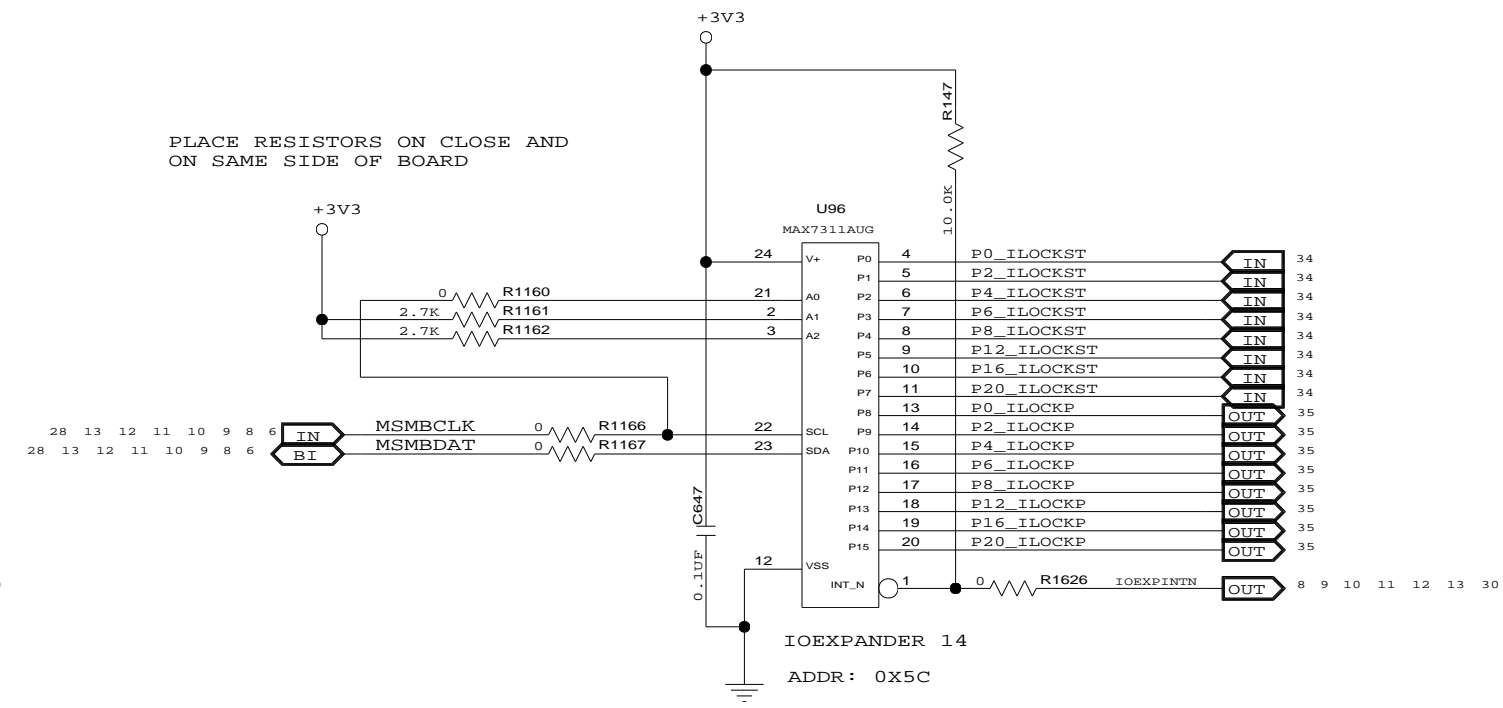
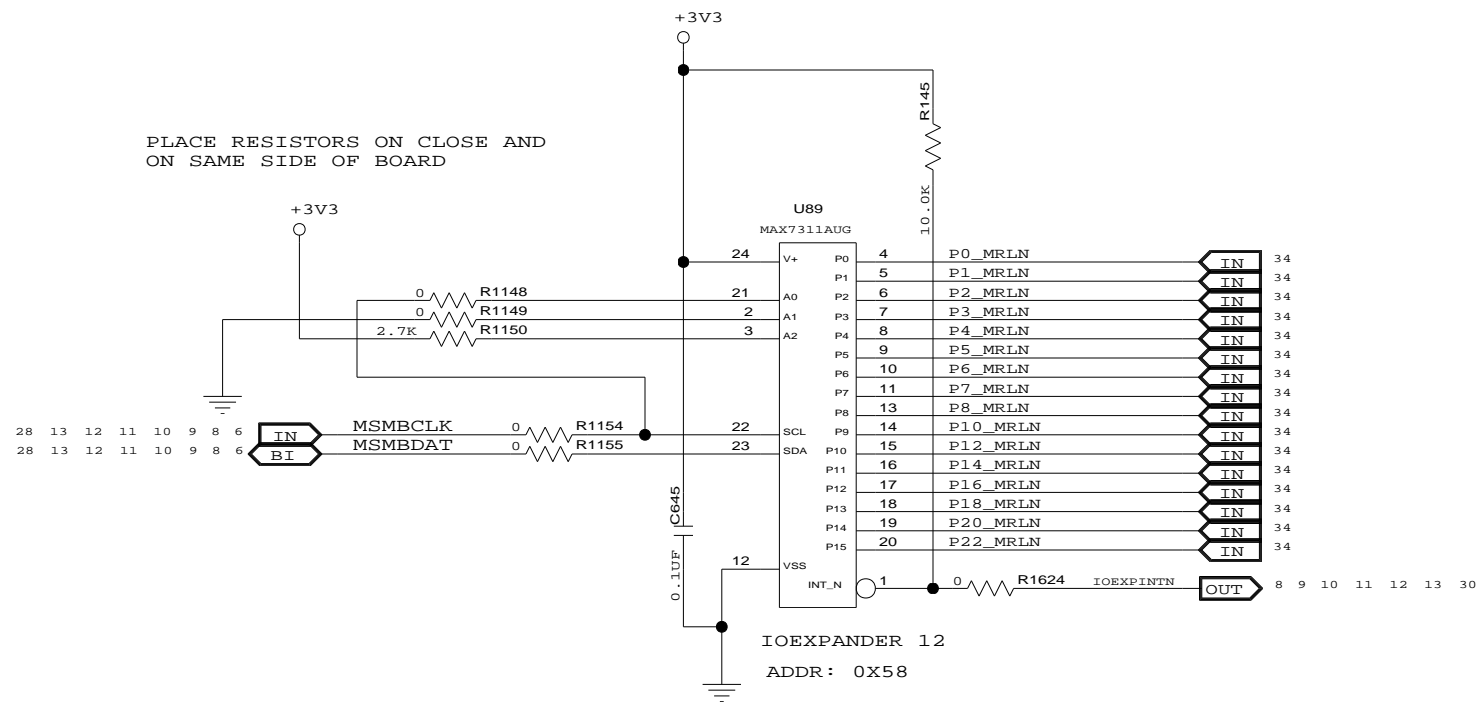


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TITLE EB-LOGAN-19

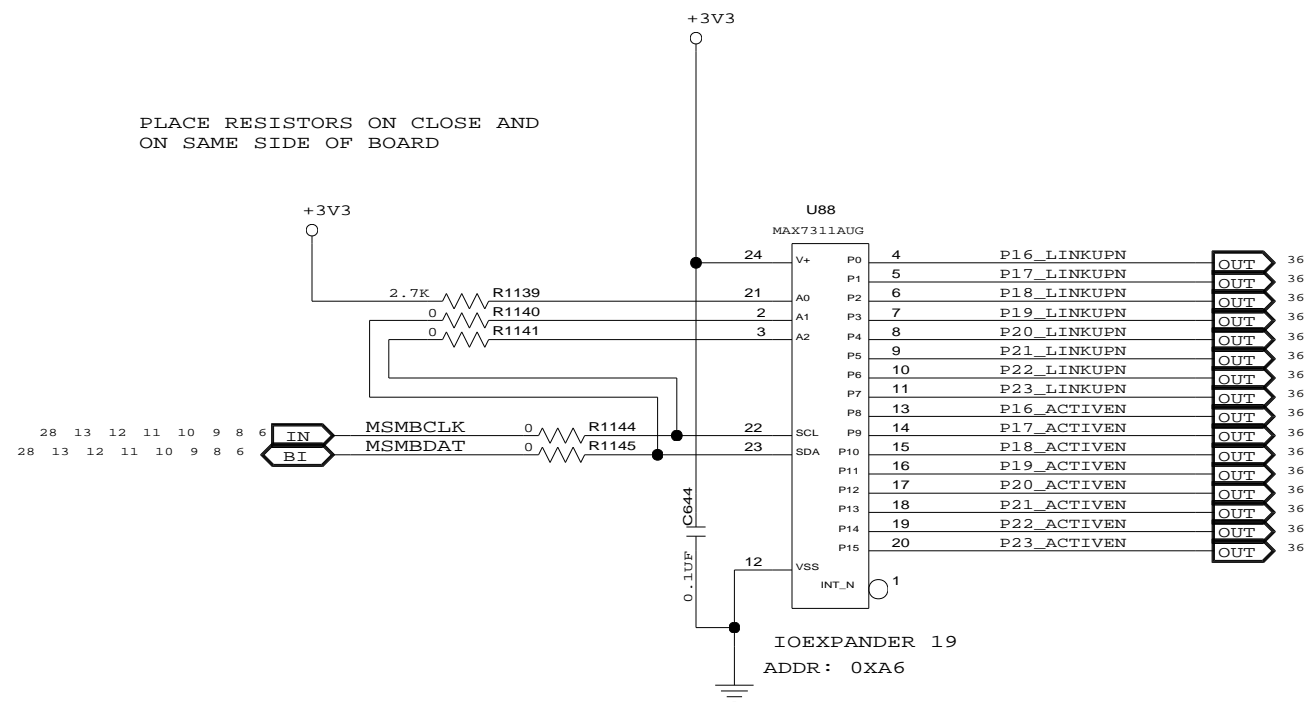
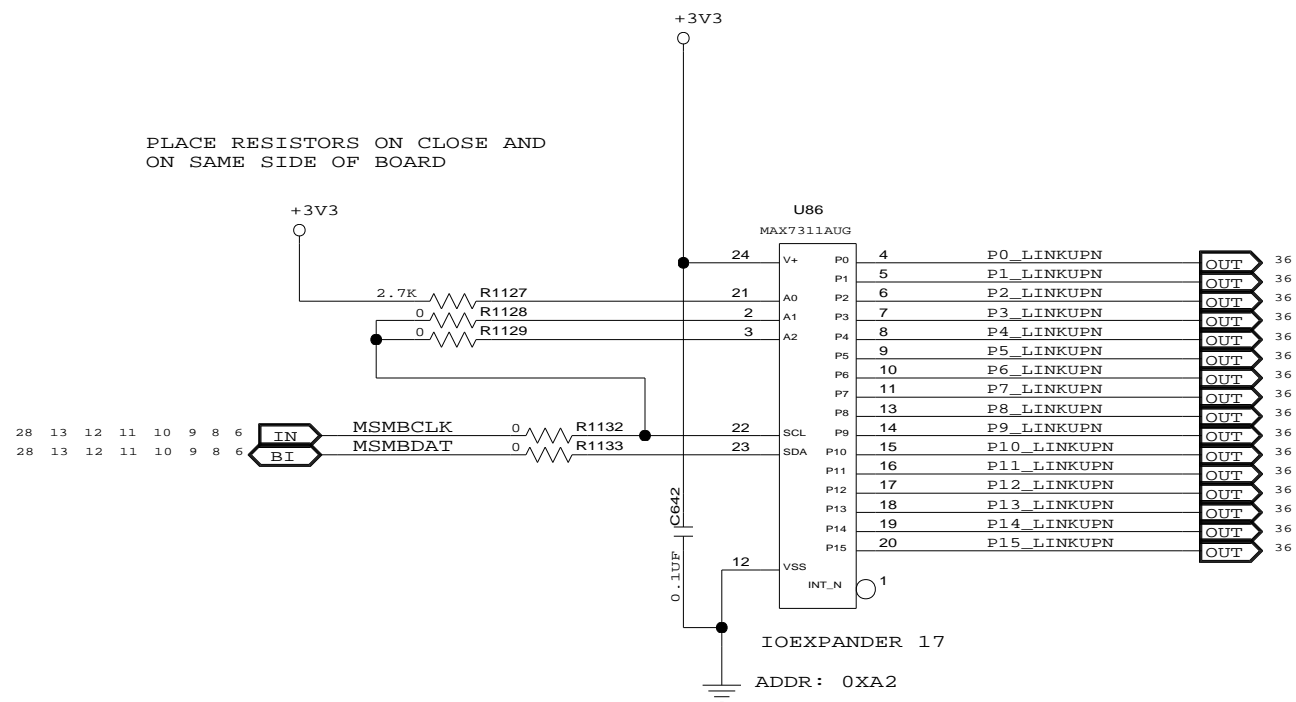
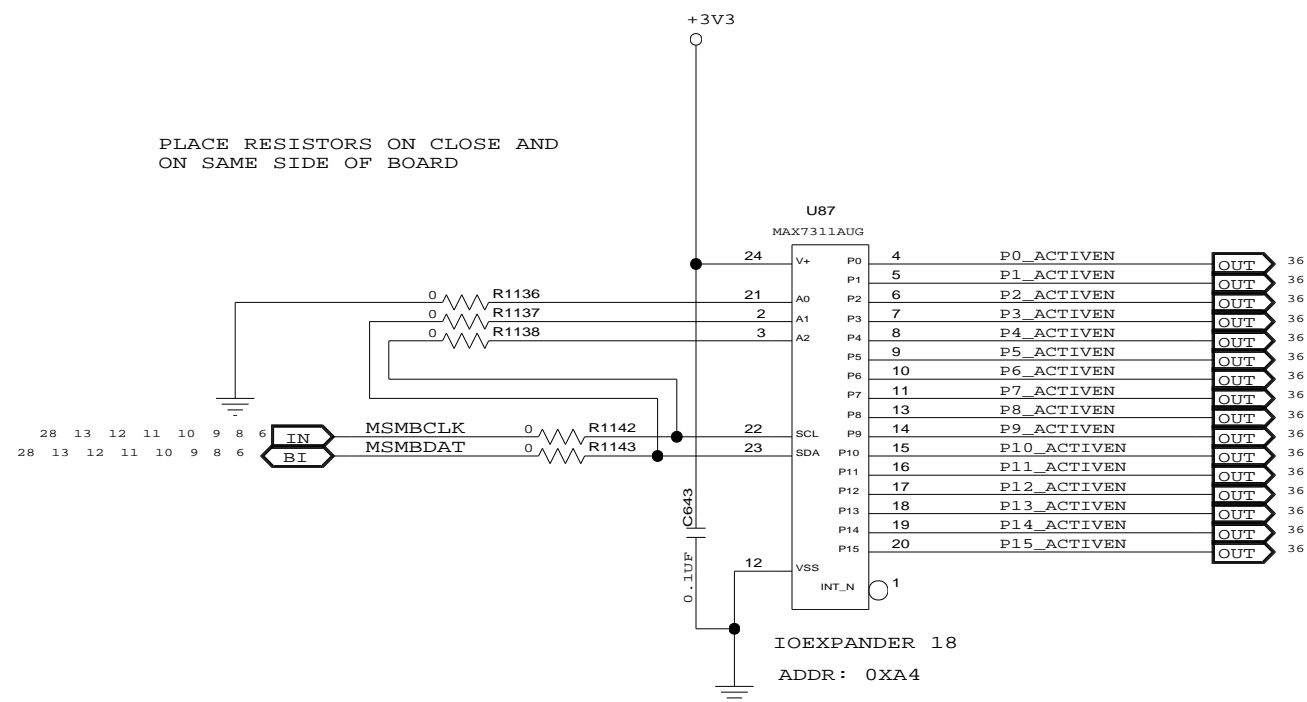
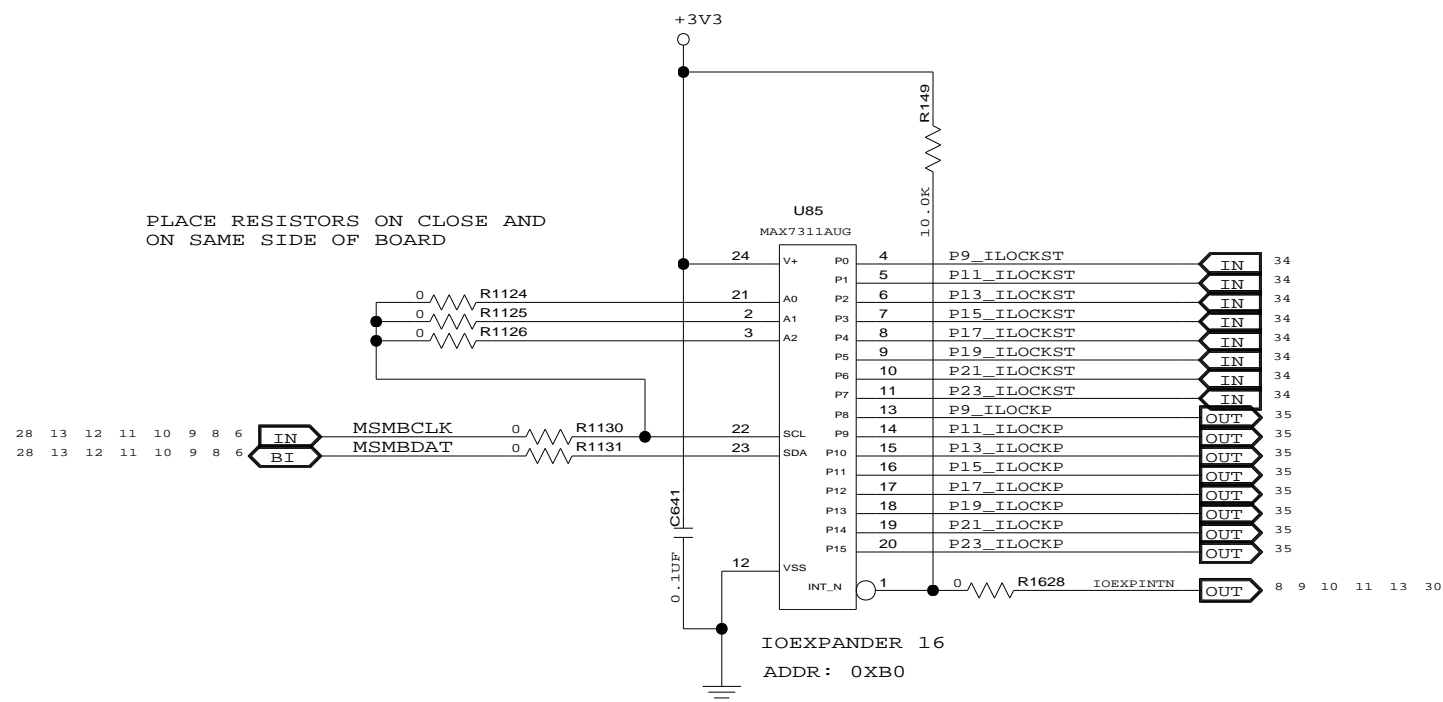
IOEXPANDER 8-11


SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:45 2010			SHEET 10 OF 41



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TITLE EB-LOGAN-19			
<b>IOEXPANDER 12-15</b>			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:45 2010			SHEET 11 OF 41



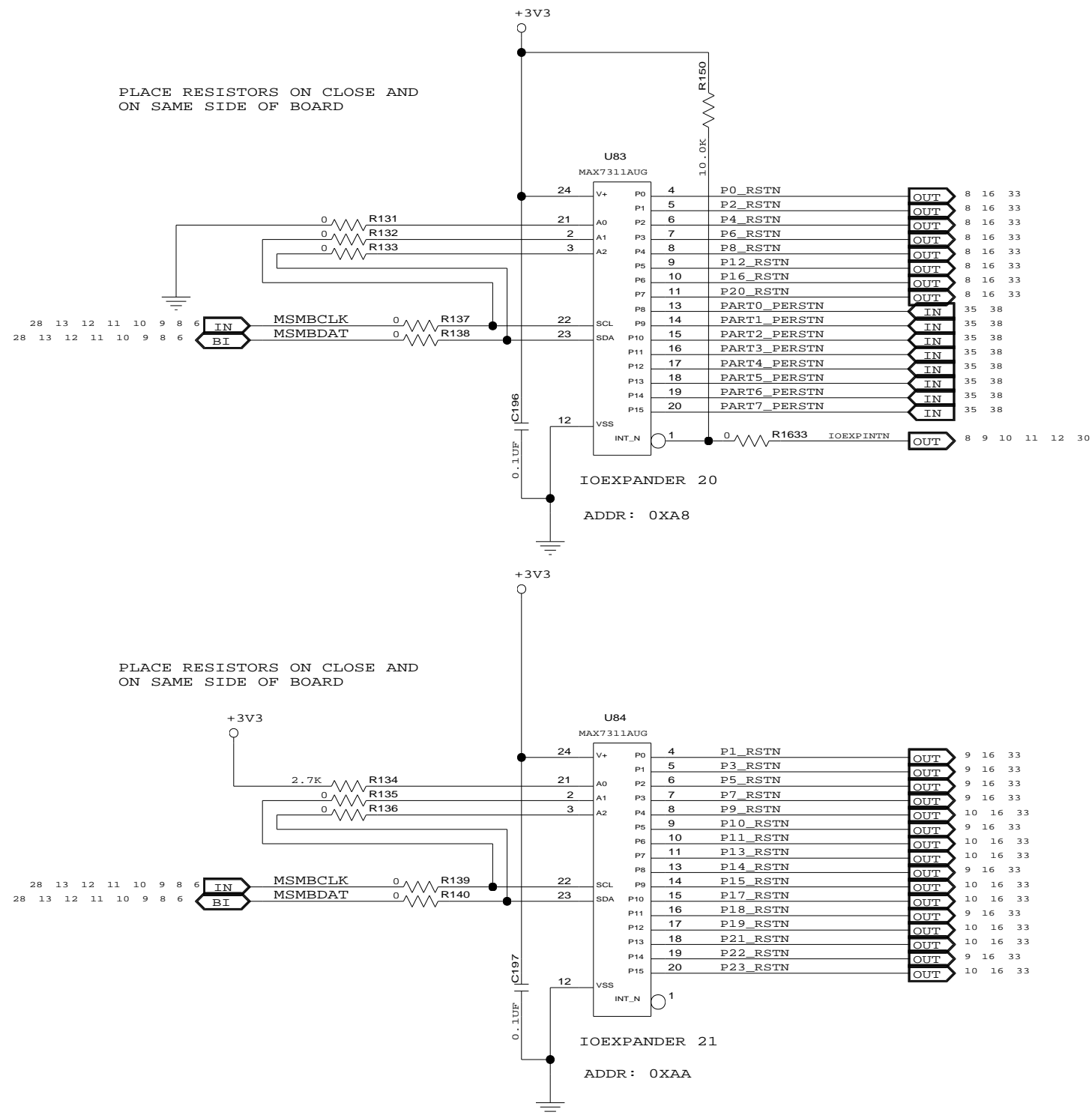


TITLE EB-LOGAN-19

## IOEXPANDER 16-19

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:46 2010			SHEET 12 OF 41

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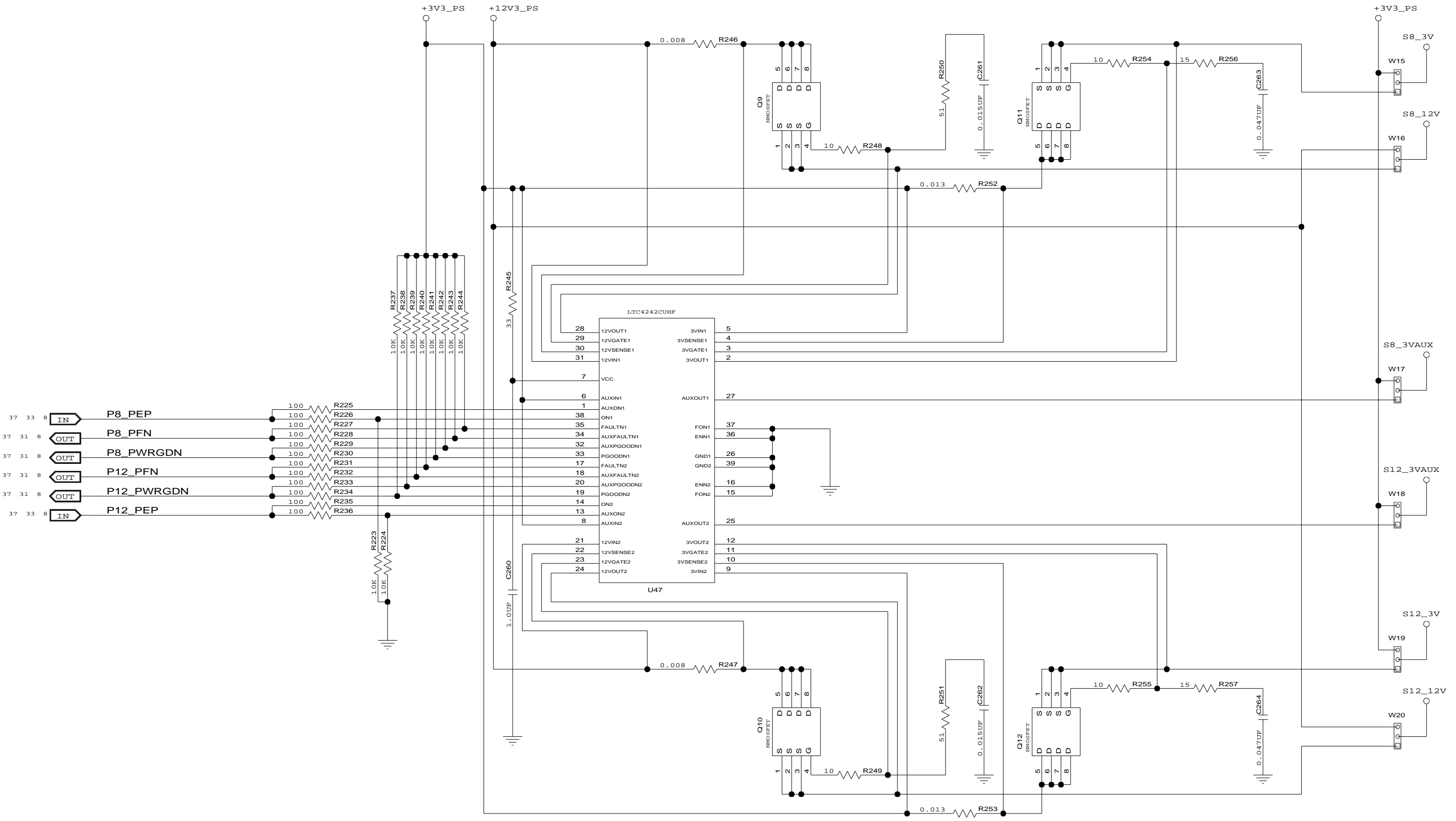


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TITLE EB-LOGAN-19

IOEXPANDER 20-21

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:46 2010			SHEET 13 OF 41



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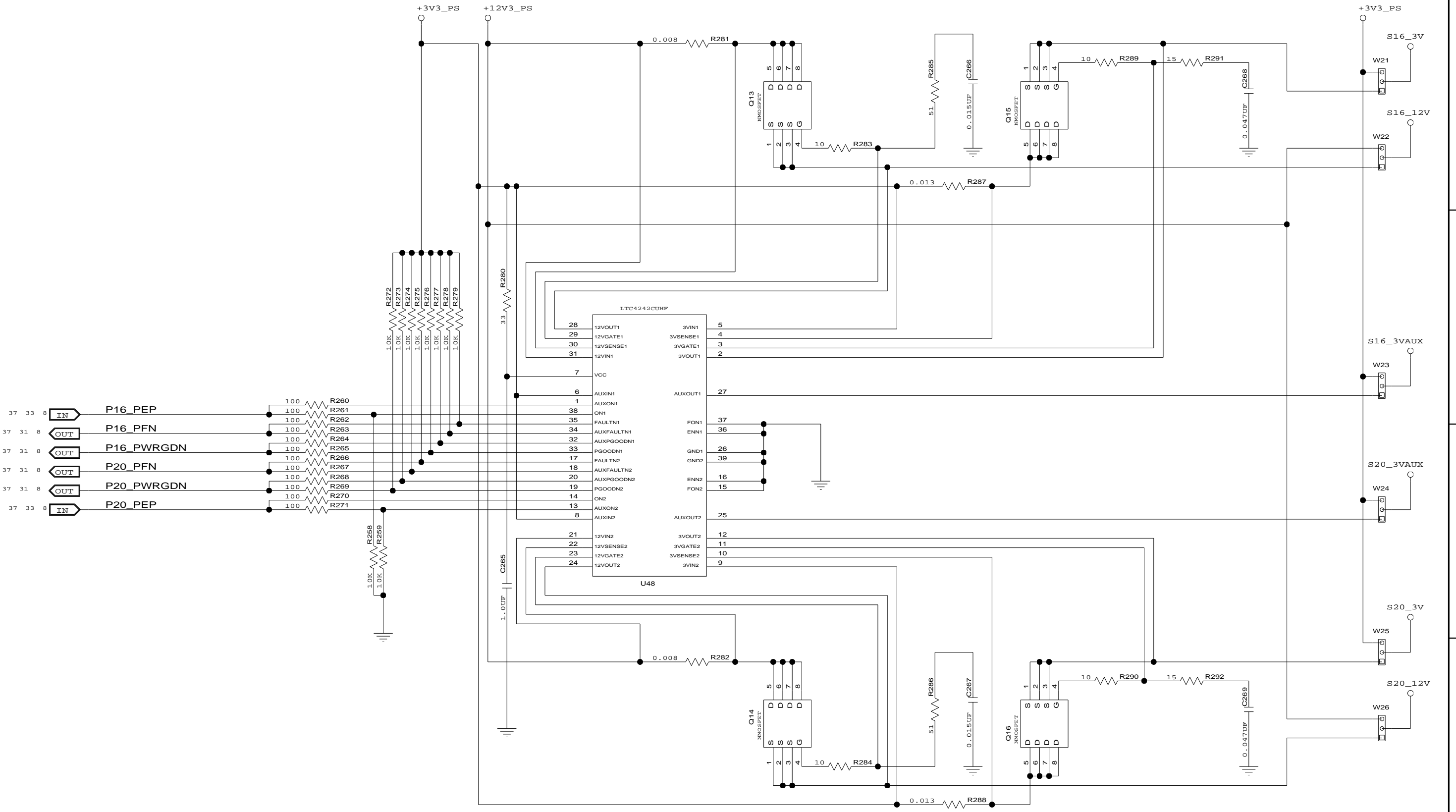

TITLE EB-LOGAN-19

HOT PLUG CONTROL PORTS 8-12

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

Thu Jun 10 11:24:46 2010 SHEET 14 OF 41

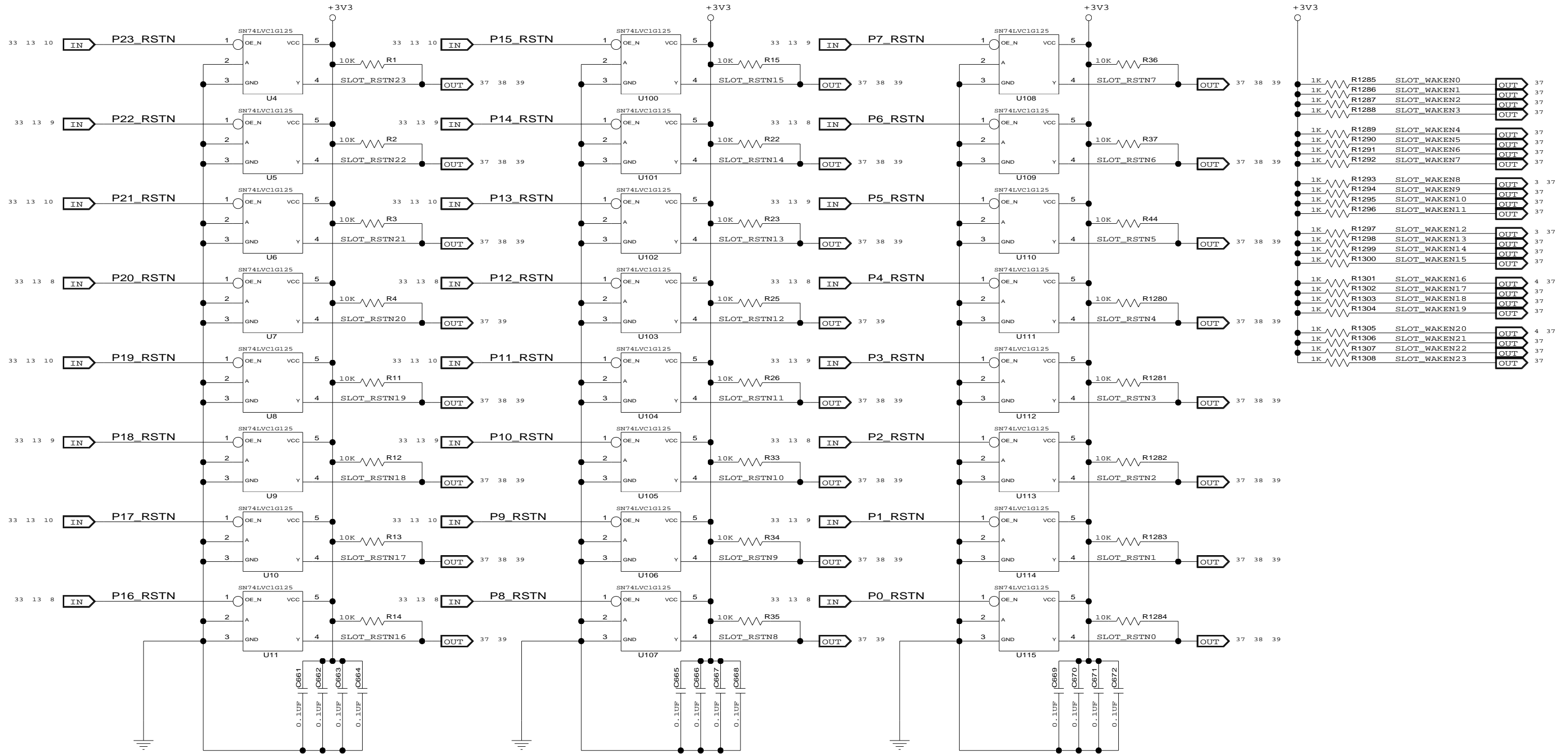




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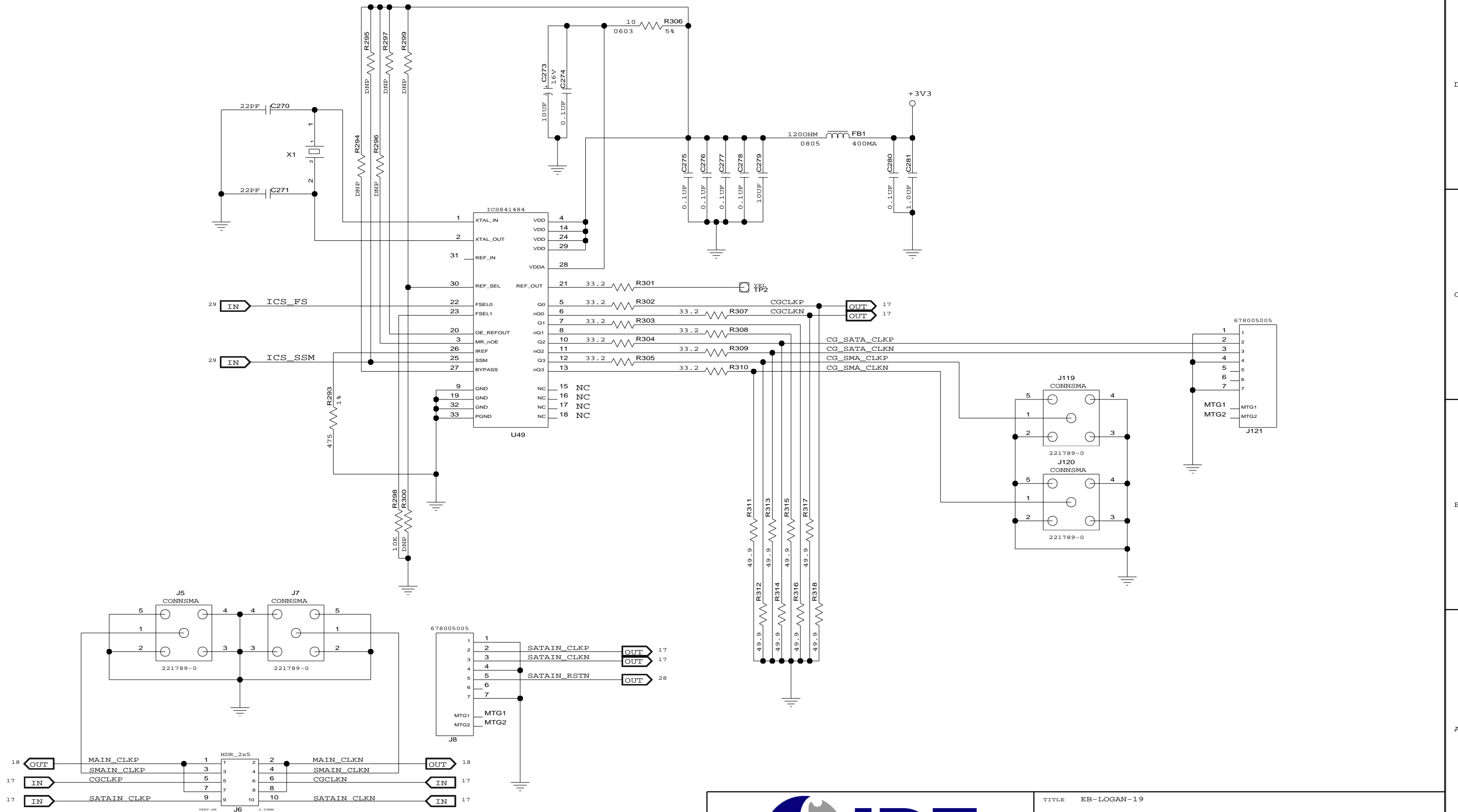
TITLE EB-LOGAN-19			
HOT PLUG CONTROL PORTS 16-20			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:47 2010			SHEET 15 OF 41


D  
C  
B  
A

D  
C  
B  
A



		TITLE EB-LOGAN-19	
		SLOT RESETS AND WAKE PULL-UPS	
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
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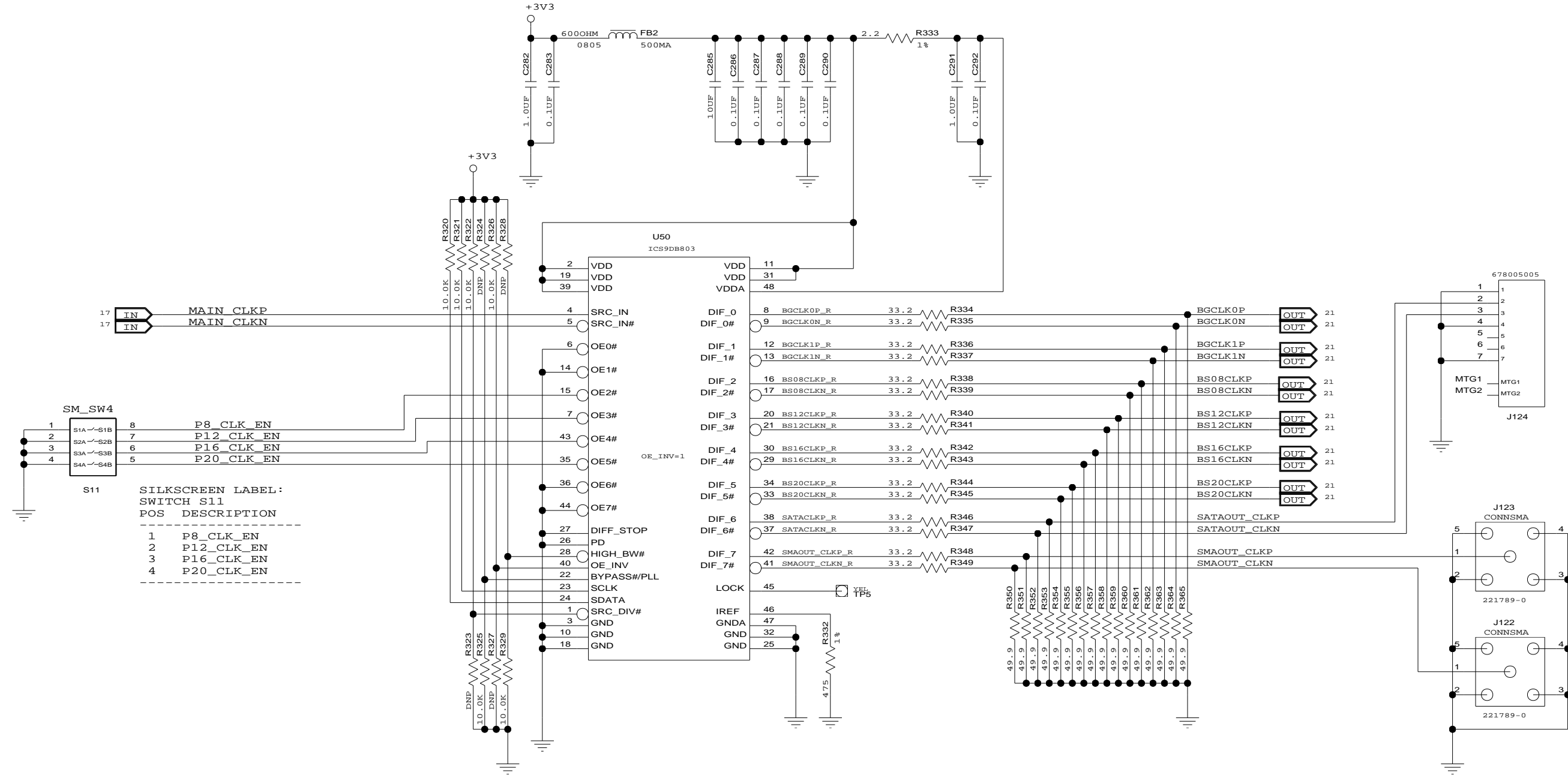


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TITLE EB-LOGAN-19

## CLOCK

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:48 2010			SHEET 17 OF 41



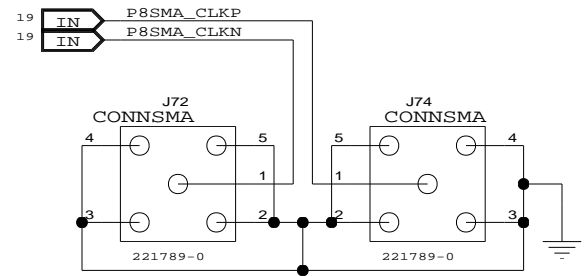
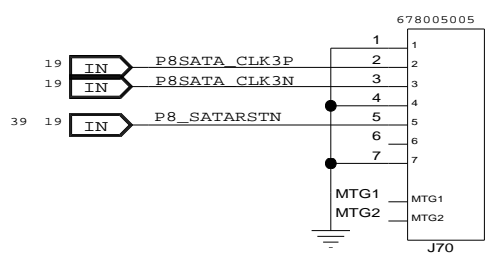
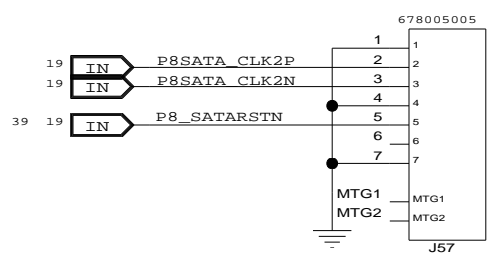
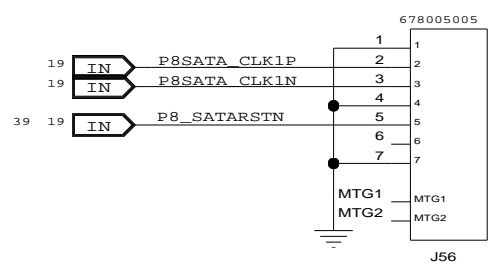
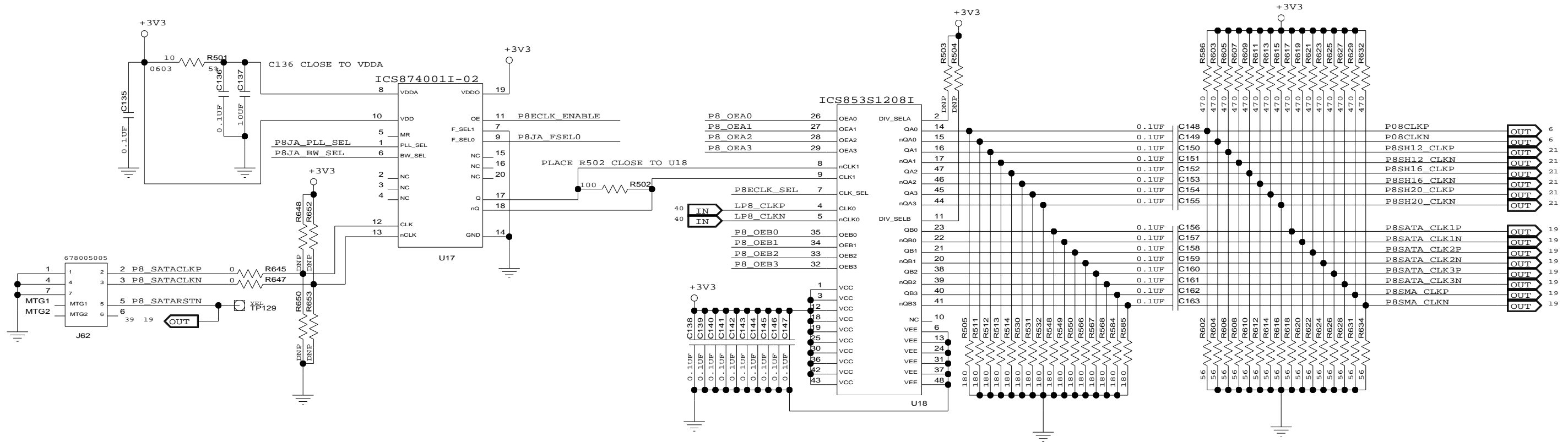
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TITLE EB-LOGAN-19

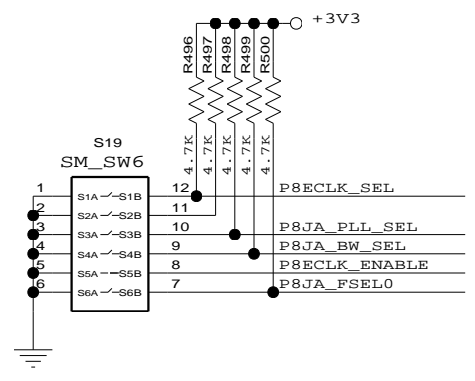
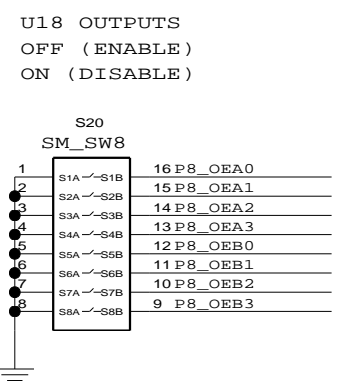
CLOCK BUFFER

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:48 2010			SHEET 18 OF 41

P8CLK - DUT PORT 8 CLK  
 LP8CLK - LOCAL CLOCK GEN. PORT 8 CLK  
 P8SHXCLK - TO SLOT CLK HEADERS



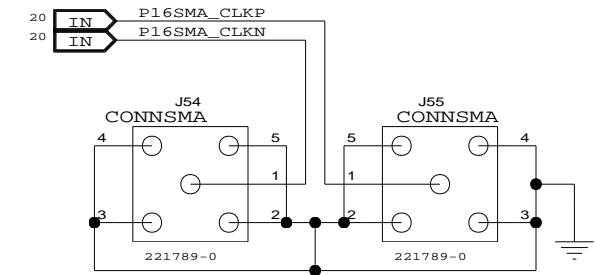
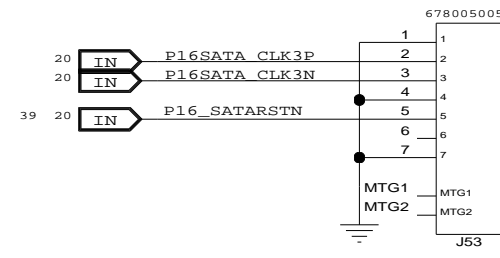
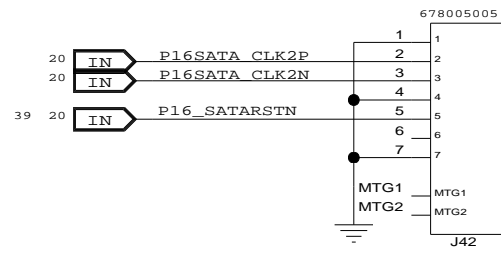
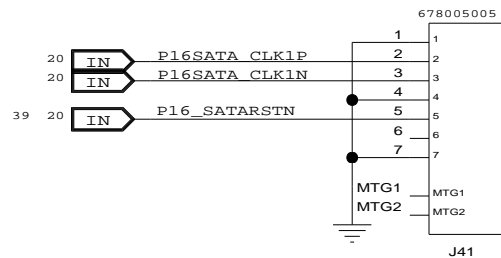
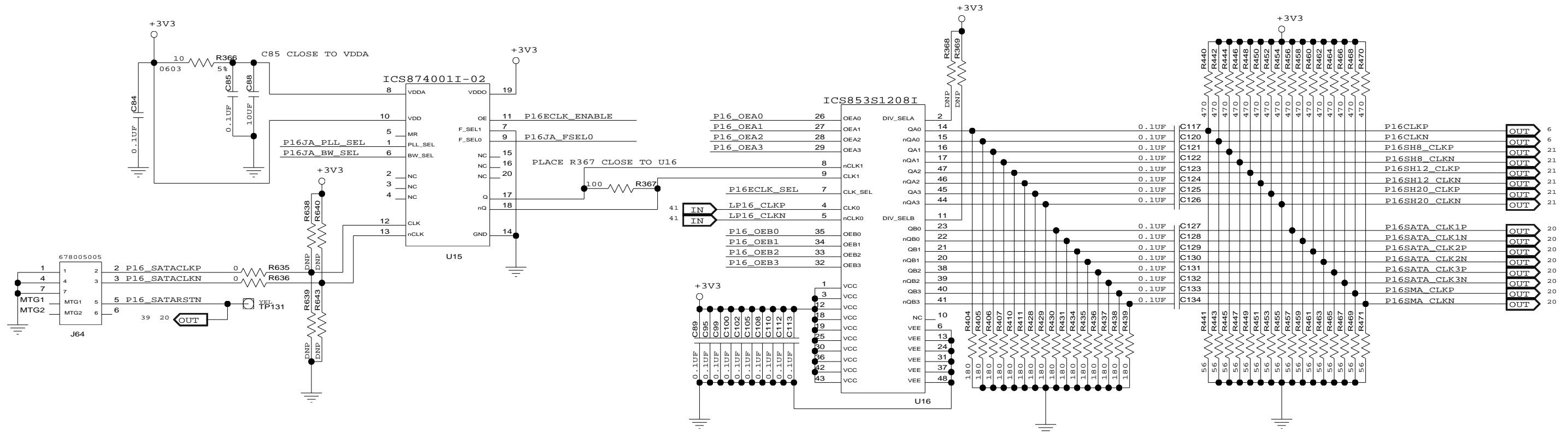
DEFAULT DIPSW SETTING  
 S19:1 OFF (SATACLK)  
 S19:3 OFF (PLL)  
 S19:4 OFF (2.2MHZ)  
 S19:5 OFF (U15 OUT ON)  
 S19:6 ON (100MHZ)



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TITLE EB-LOGAN-19			
CLOCK SELECTOR DUT PCLK 8			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:28:22 2010			SHEET 19 OF 41

P16CLK - DUT PORT 16 CLK  
 LP16CLK - LOCAL CLOCK GEN. PORT 16 CLK  
 P16SHXCLK - TO SLOT CLK HEADERS

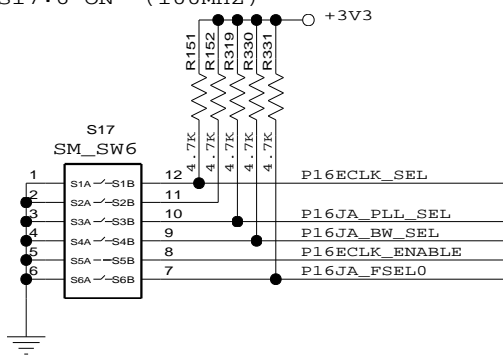


DEFAULT DIPSW SETTING

- S17:1 OFF (SATACLK)
- S17:3 OFF (PLL)
- S17:4 OFF (2.2MHZ)
- S17:5 OFF (U15 OUT ON)
- S17:6 ON (100MHZ)

U16 OUTPUTS  
 OFF (ENABLE)  
 ON (DISABLE)

S18 SM_SW8		
1	S1A-S1B	16 P16_OEA0
2	S2A-S2B	15 P16_OEA1
3	S3A-S3B	14 P16_OEA2
4	S4A-S4B	13 P16_OEA3
5	S5A-S5B	12 P16_OEB0
6	S6A-S6B	11 P16_OEB1
7	S7A-S7B	10 P16_OEB2
8	S8A-S8B	9 P16_OEB3



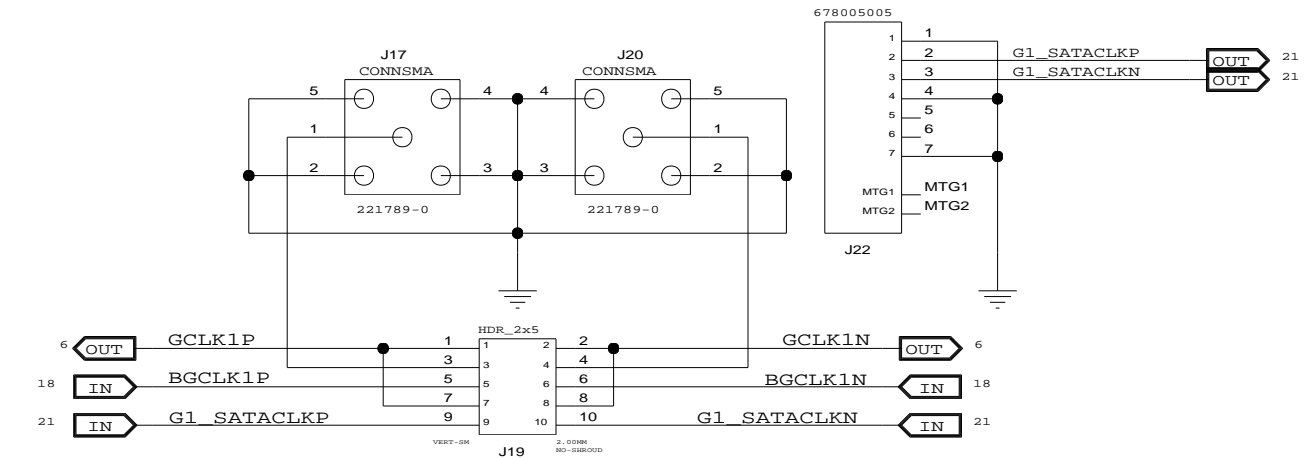
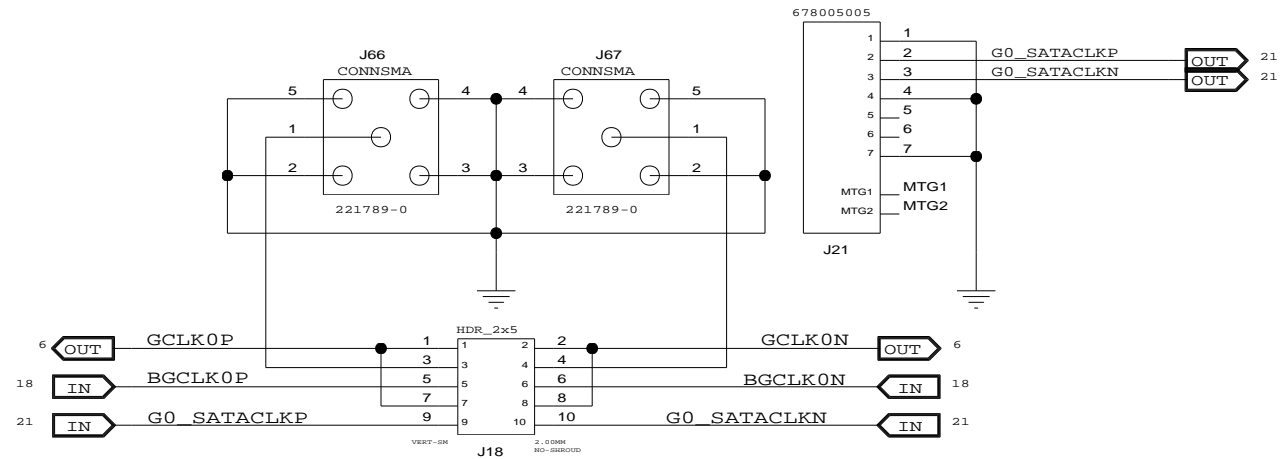
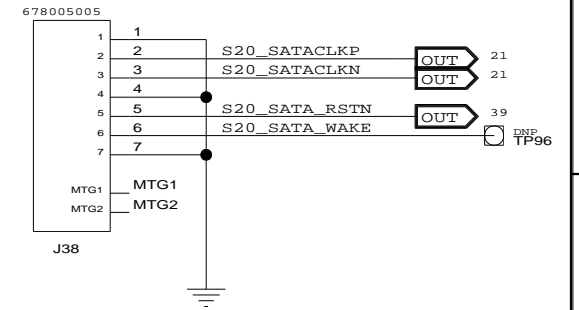
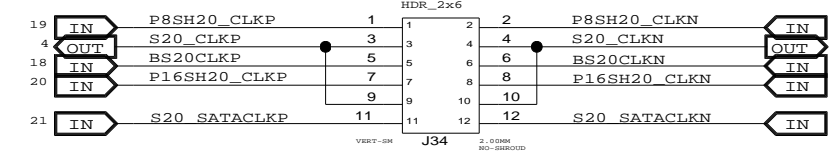
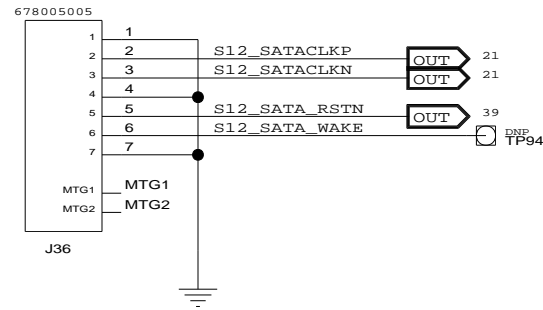
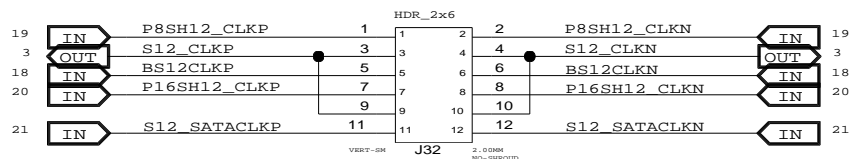
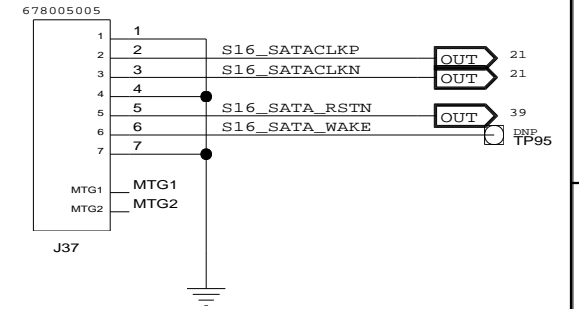
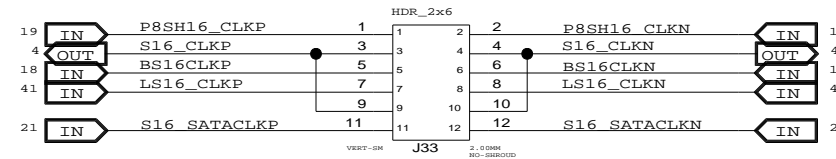
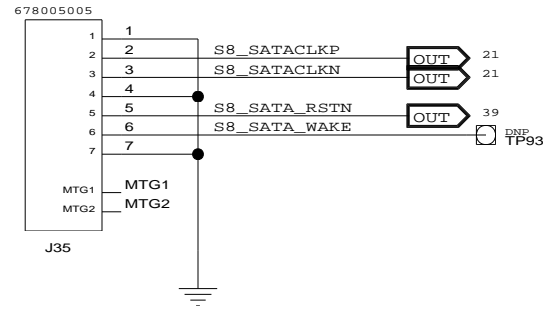
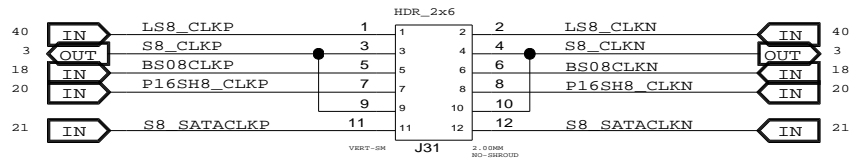
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TITLE EB-LOGAN-19

CLOCK SELECTOR DUT PCLK 16

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:28:19 2010			SHEET 20 OF 41

SXXCLK - SLOT CLK  
 BSXXCLK - BUFFER SLOT CLK  
 LSXXCLK - LOCAL CLOCK GEN. SLOT CLK  
 SHXXCLK - SLOT HDR.CLK



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TITLE EB-LOGAN-19

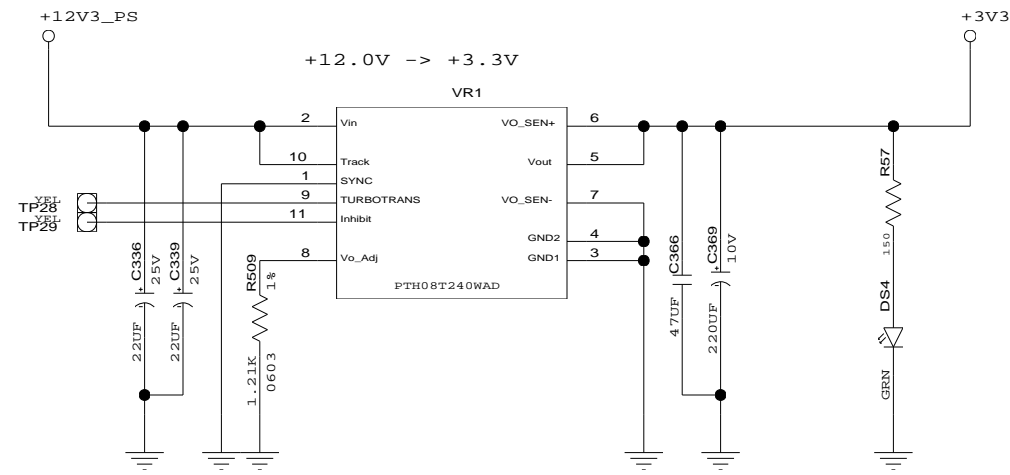
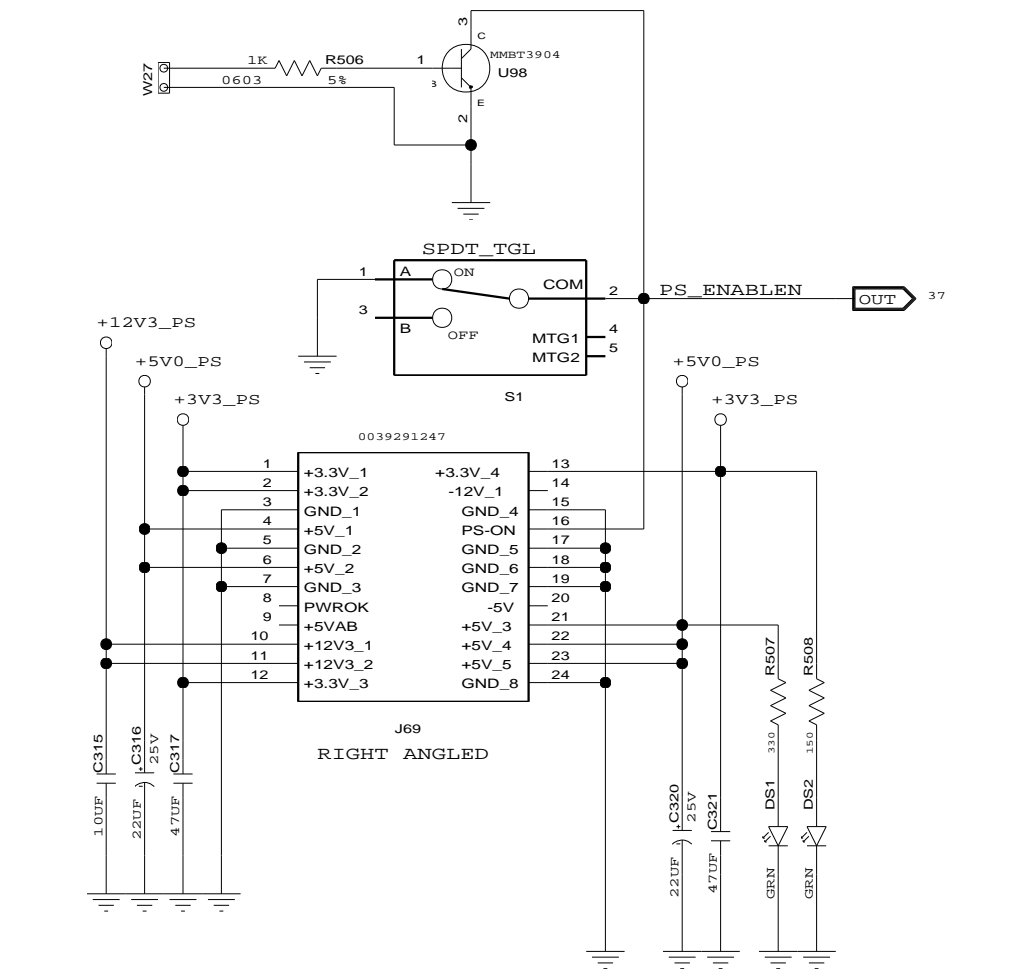
CLOCK SELECTOR SLOTS 8-20, GCLK

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	

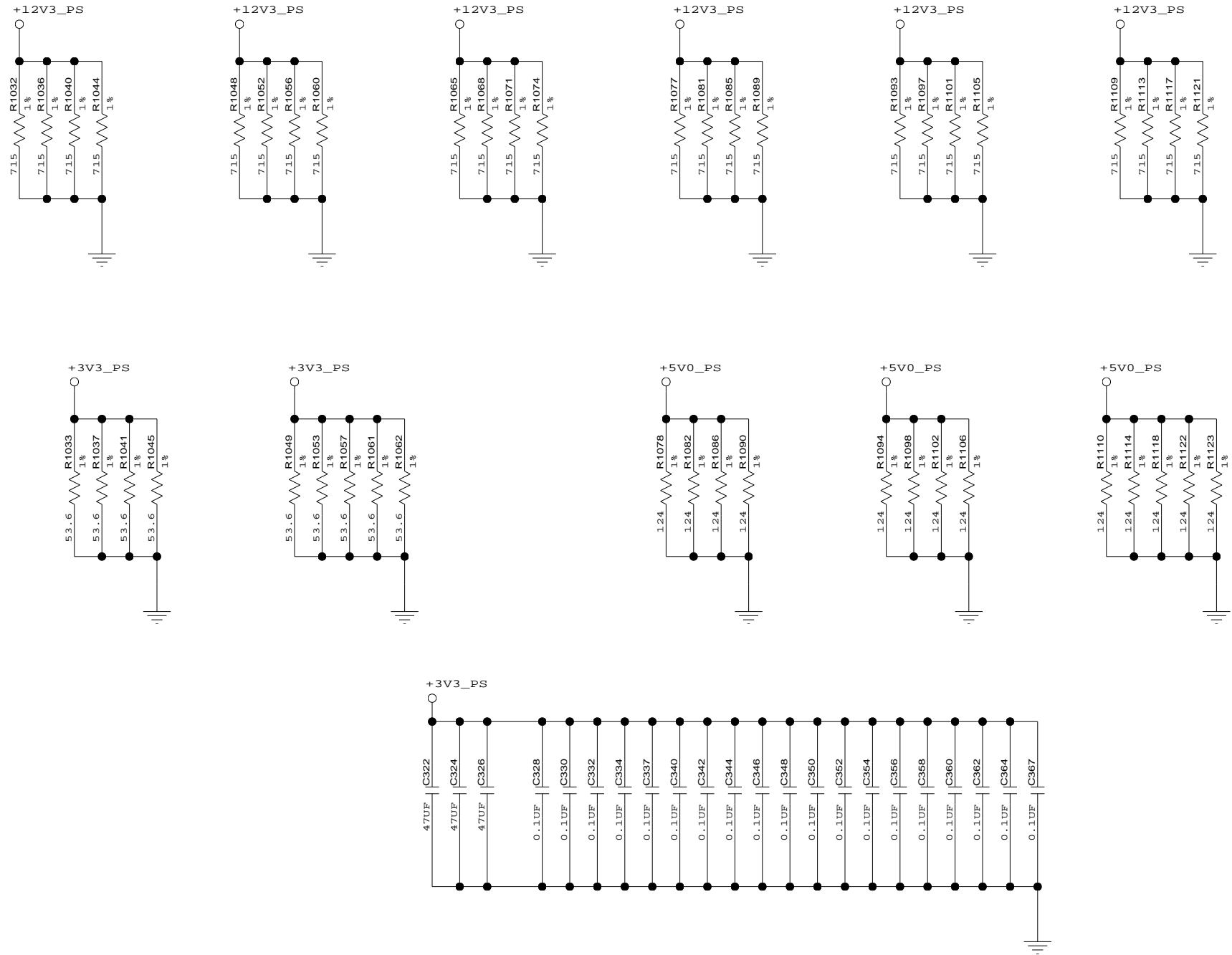
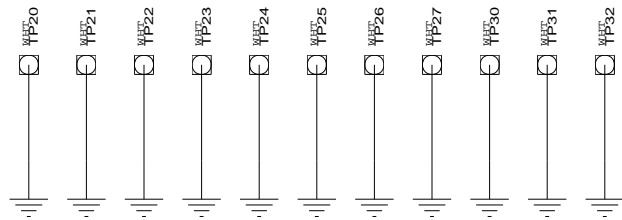
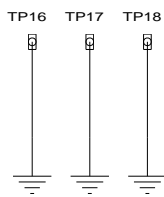
Thu Jun 10 11:24:49 2010

SHEET 21 OF 41

MINIMUM POWER SUPPLY LOADS



GND TEST POINTS  
SCATTER AROUND BOARD



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TITLE EB-LOGAN-19

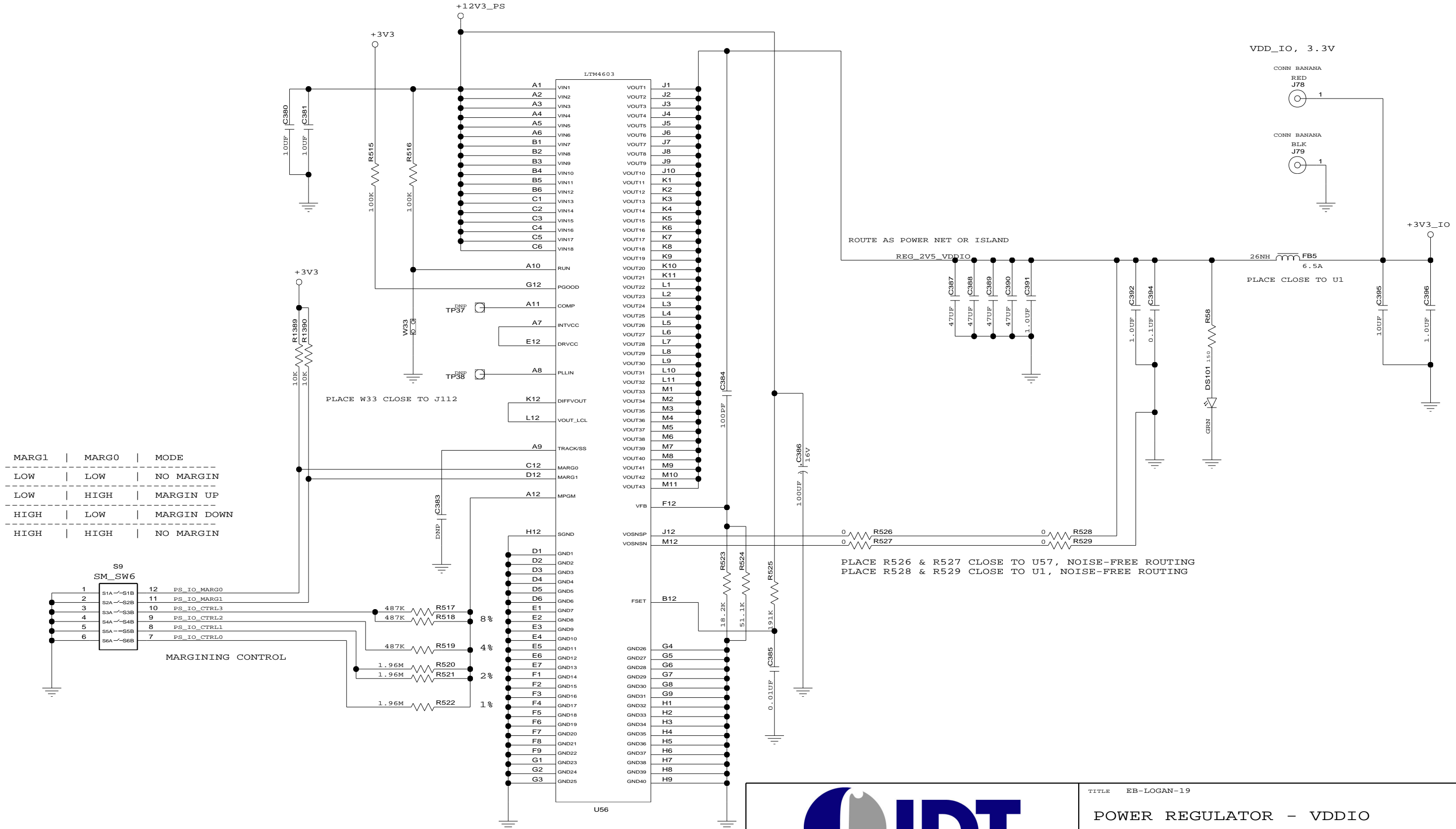
POWER CONNECTORS, MIN LOAD RESISTORS

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
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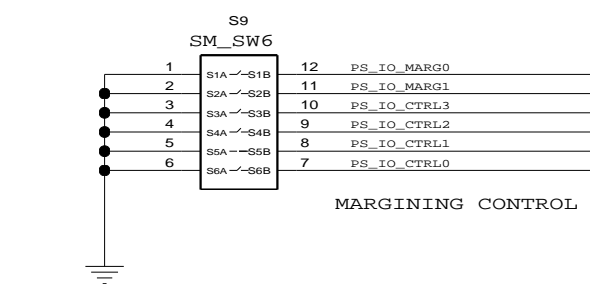
AUTHOR Tony Tran	CHECKED BY Derek Huang
---------------------	---------------------------

Thu Jun 10 11:24:50 2010

SHEET 22 OF 41



MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

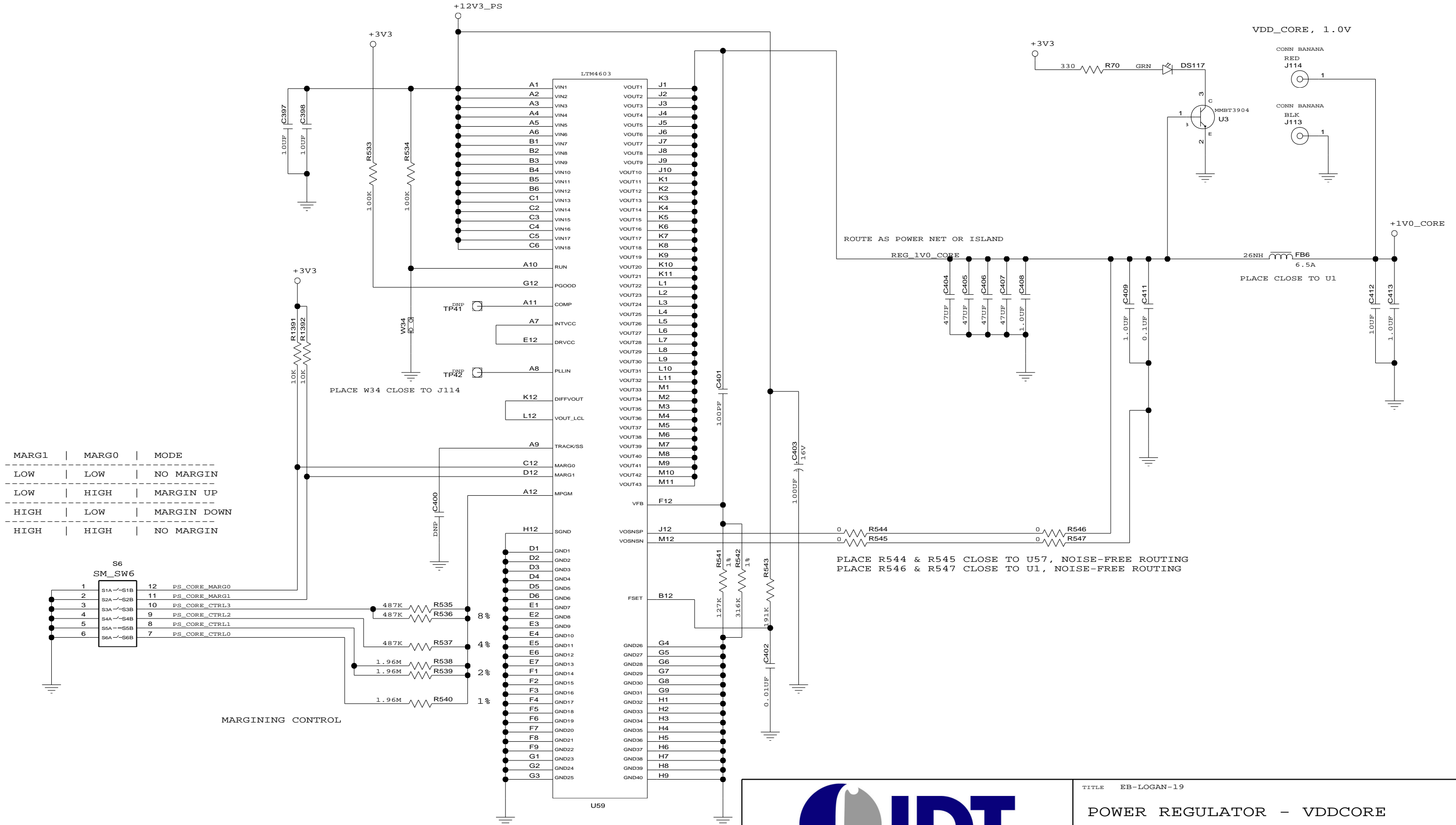


PLACE R526 & R527 CLOSE TO U57, NOISE-FREE ROUTING  
 PLACE R528 & R529 CLOSE TO U1, NOISE-FREE ROUTING

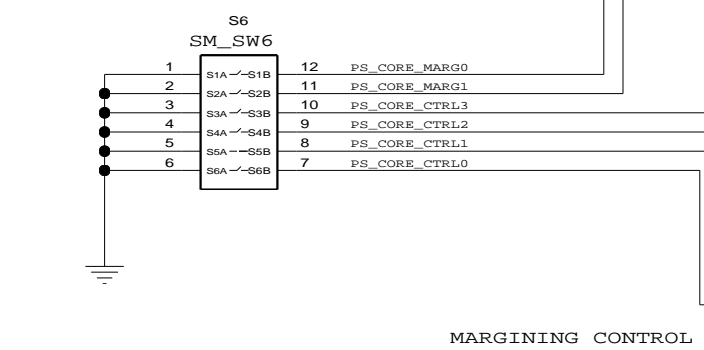


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TITLE EB-LOGAN-19			
POWER REGULATOR - VDDIO			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:50 2010			SHEET 23 OF 41



MARG1	MARG0	MODE
LOW	LOW	NO MARGIN
LOW	HIGH	MARGIN UP
HIGH	LOW	MARGIN DOWN
HIGH	HIGH	NO MARGIN

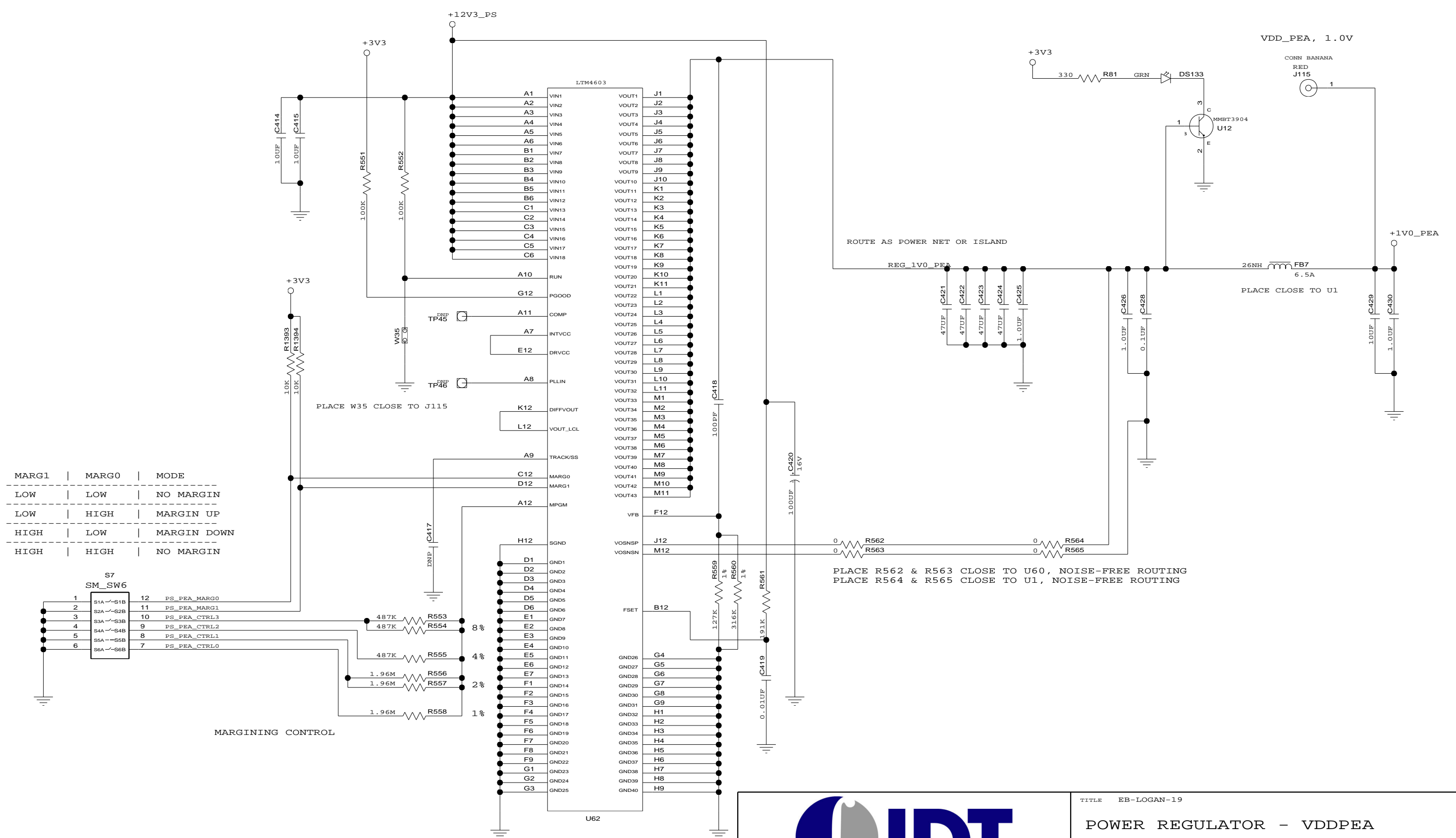


PLACE R544 & R545 CLOSE TO U57, NOISE-FREE ROUTING  
PLACE R546 & R547 CLOSE TO U1, NOISE-FREE ROUTING



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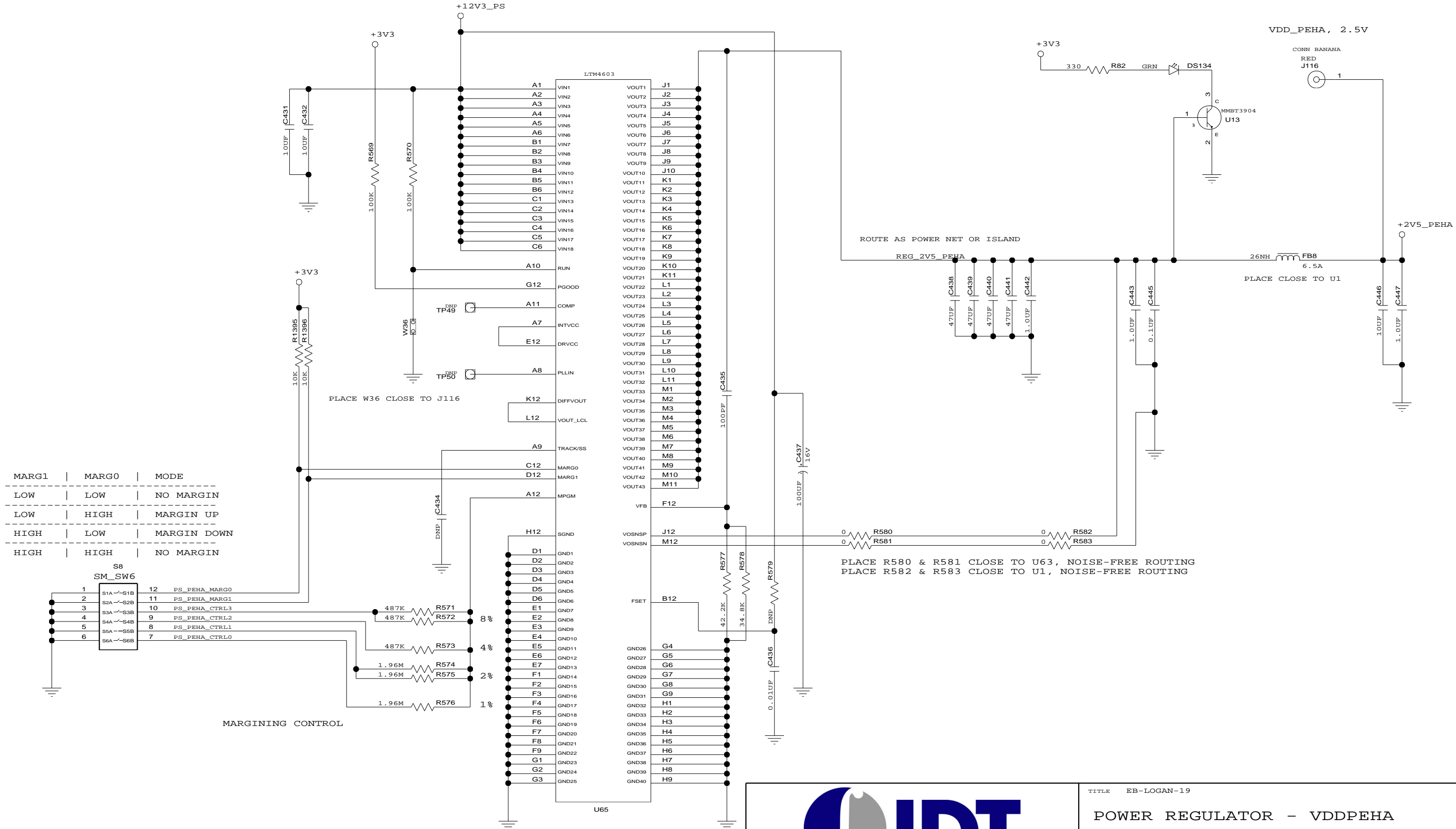
TITLE EB-LOGAN-19			
POWER REGULATOR - VDDCORE			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:51 2010			SHEET 24 OF 41



**IDT**<sup>TM</sup>

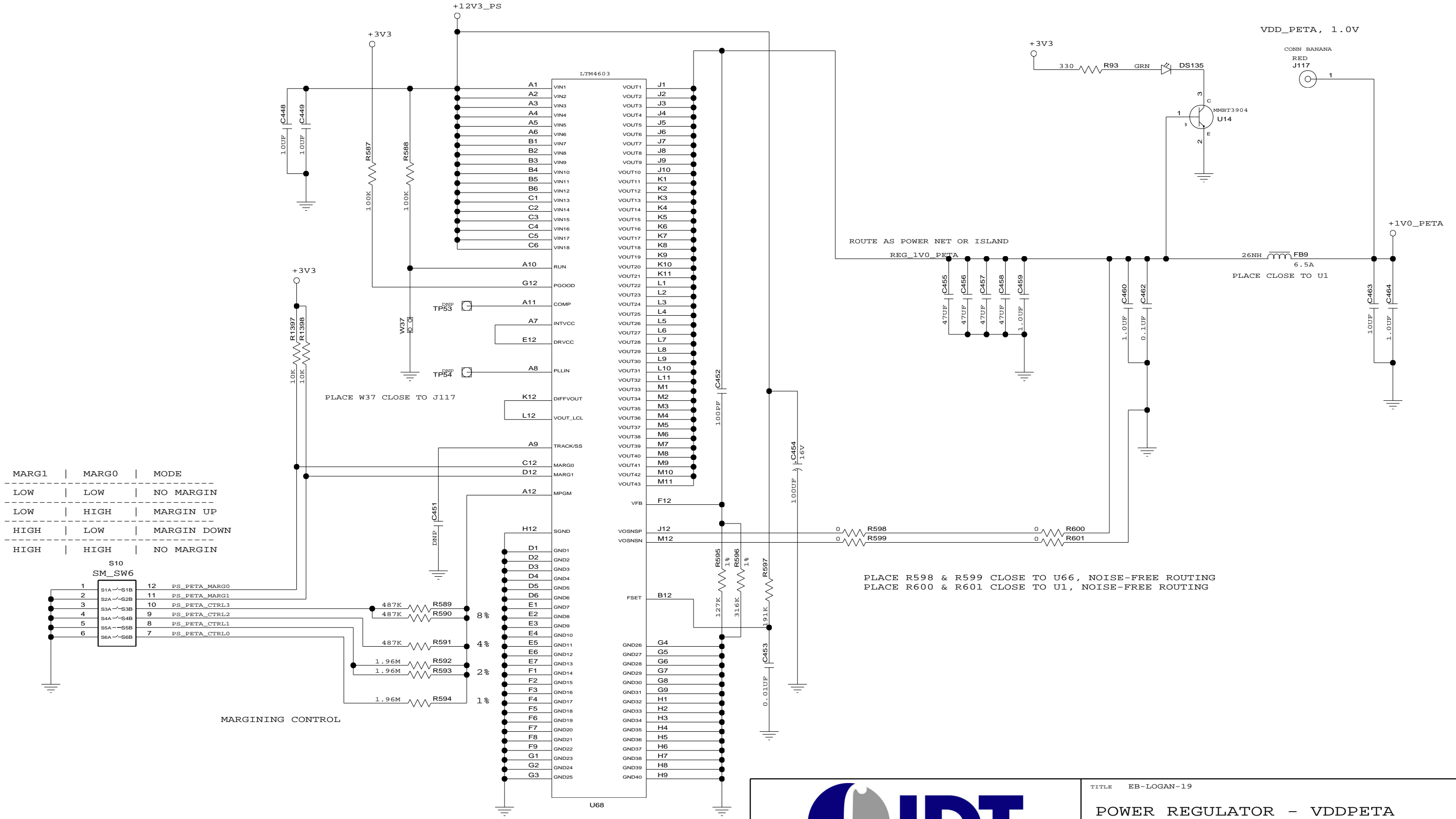
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TITLE EB-LOGAN-19			
<b>POWER REGULATOR - VDDPEA</b>			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:51 2010			SHEET 25 OF 41



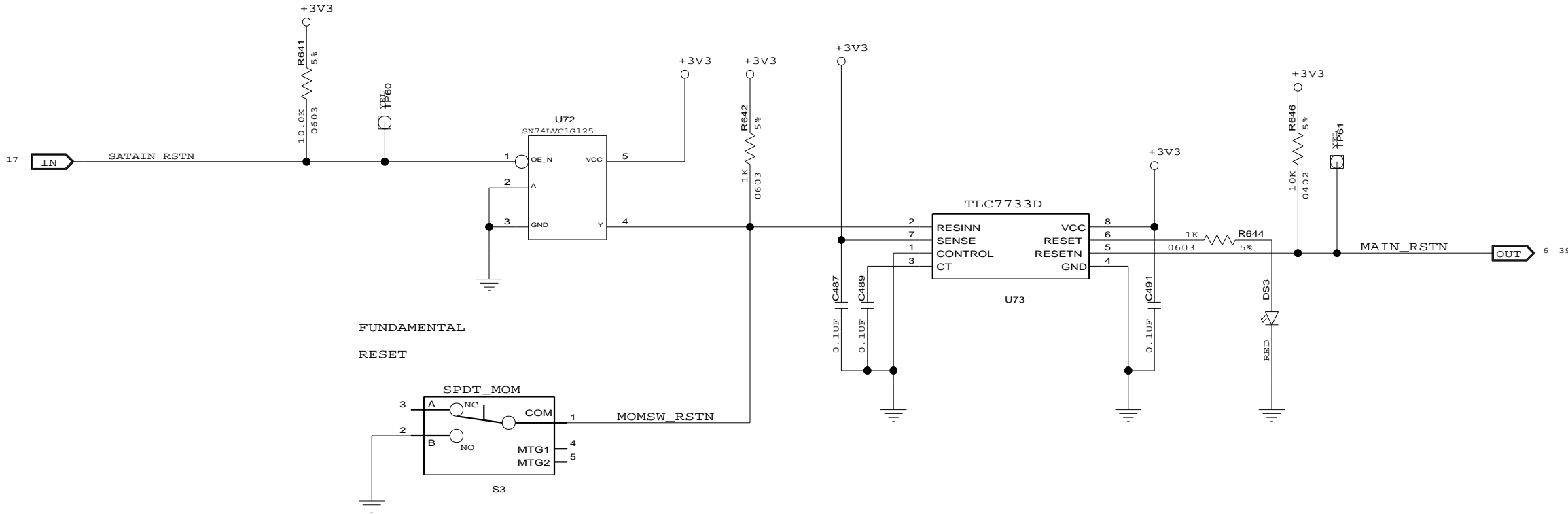
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TITLE EB-LOGAN-19			
POWER REGULATOR - VDDPEHA			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:51 2010			SHEET 26 OF 41

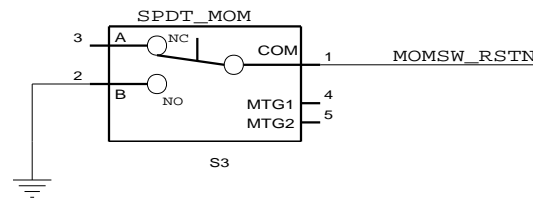


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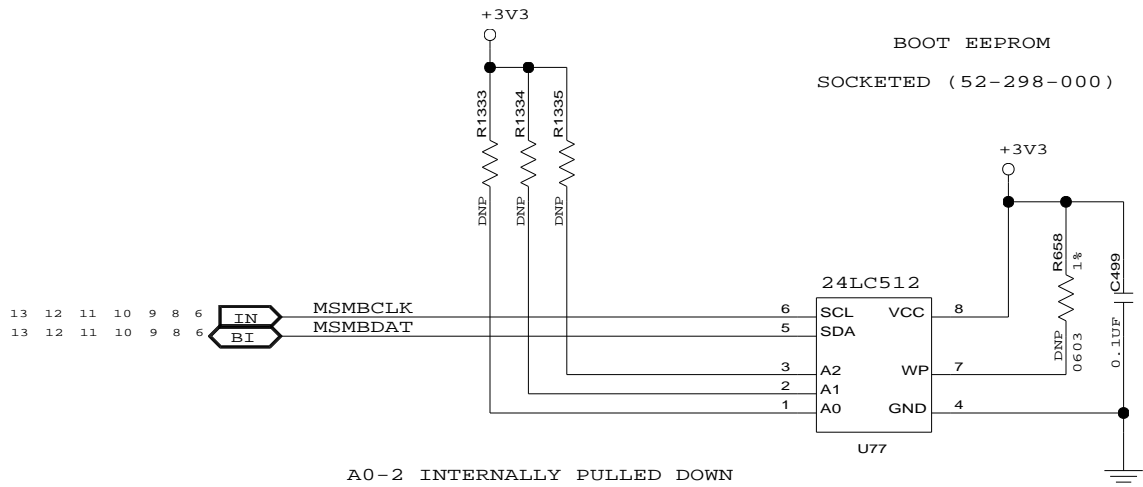
TITLE EB-LOGAN-19			
POWER REGULATOR - VDDPETA			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:52 2010			SHEET 27 OF 41



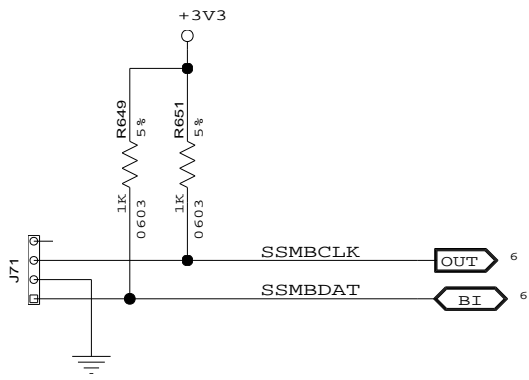
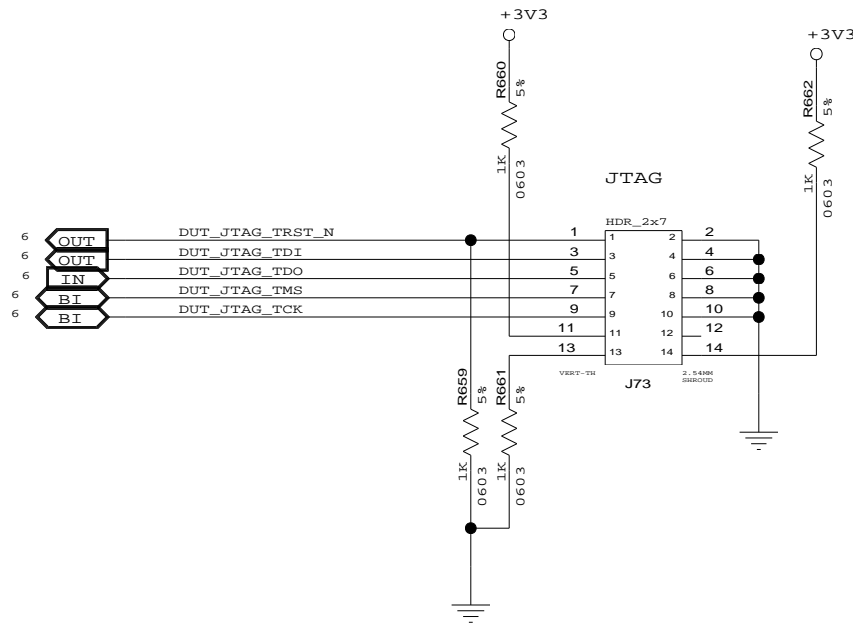
FUNDAMENTAL  
RESET



BOOT EEPROM  
SOCKETED (52-298-000)



A0-2 INTERNALLY PULLED DOWN



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TITLE EB-LOGAN-19

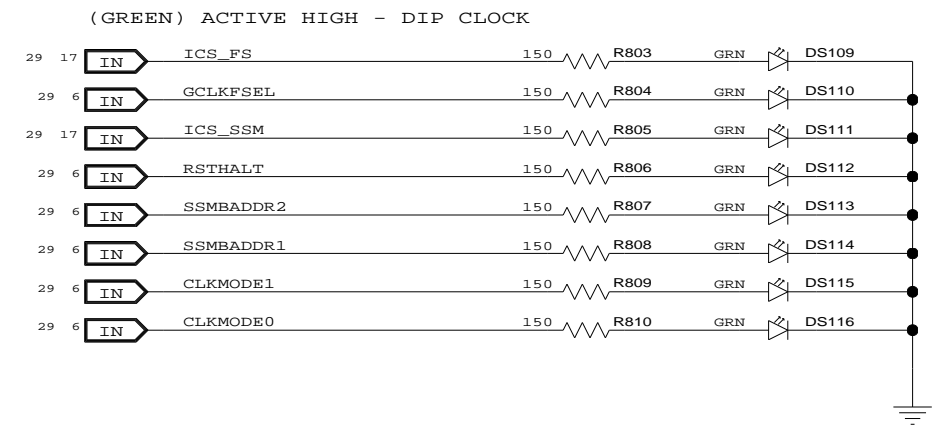
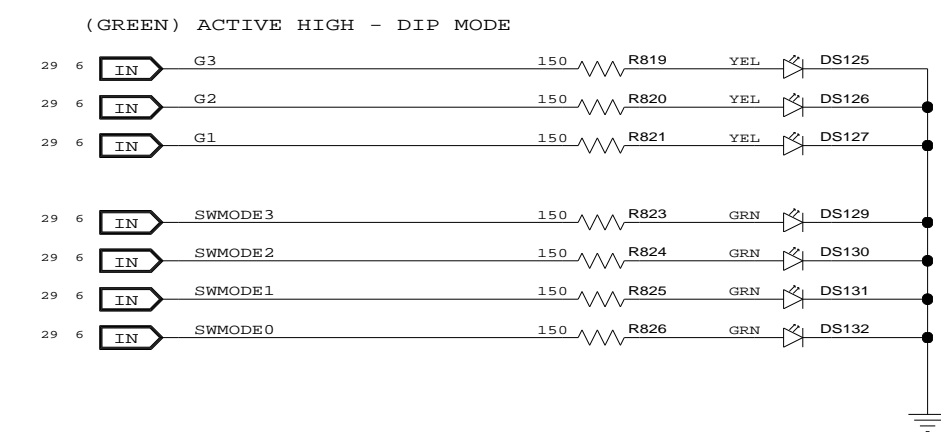
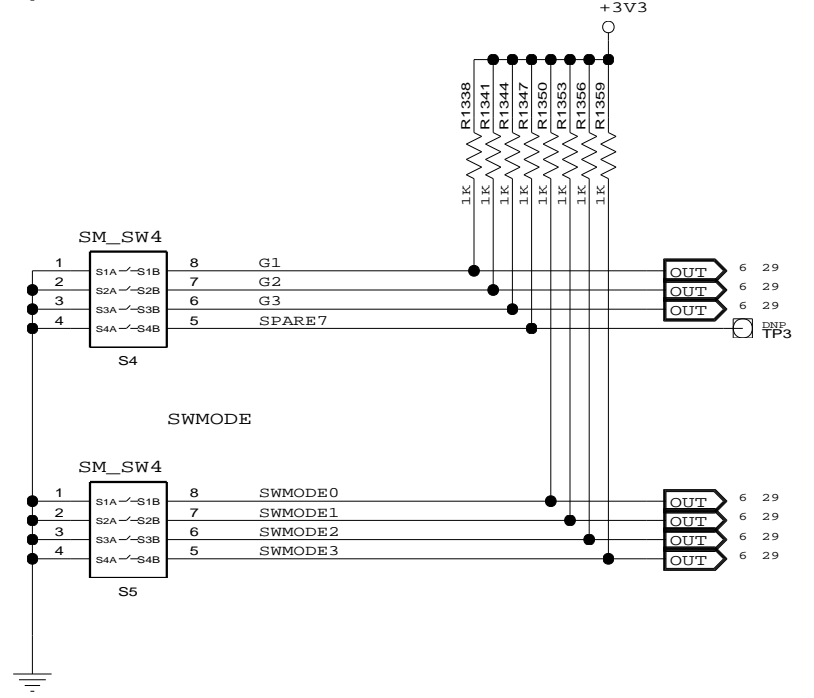
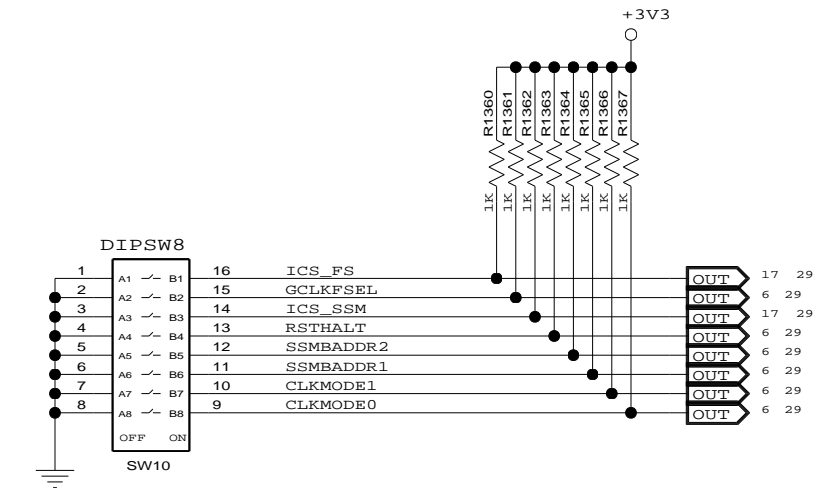
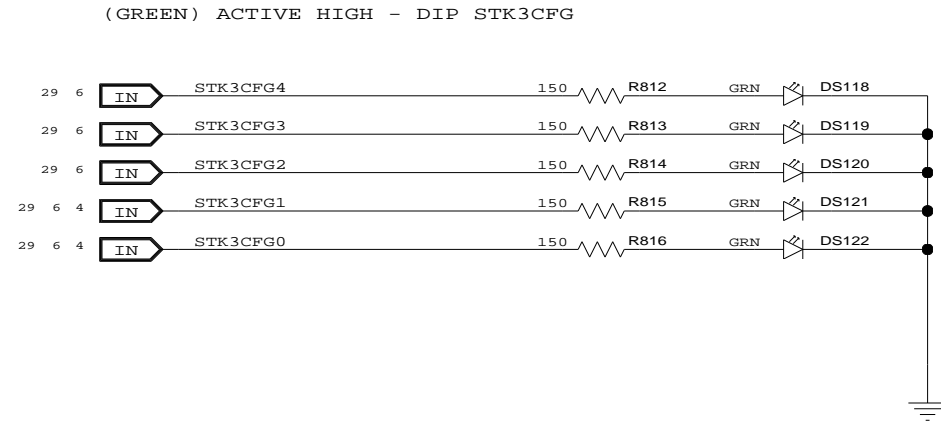
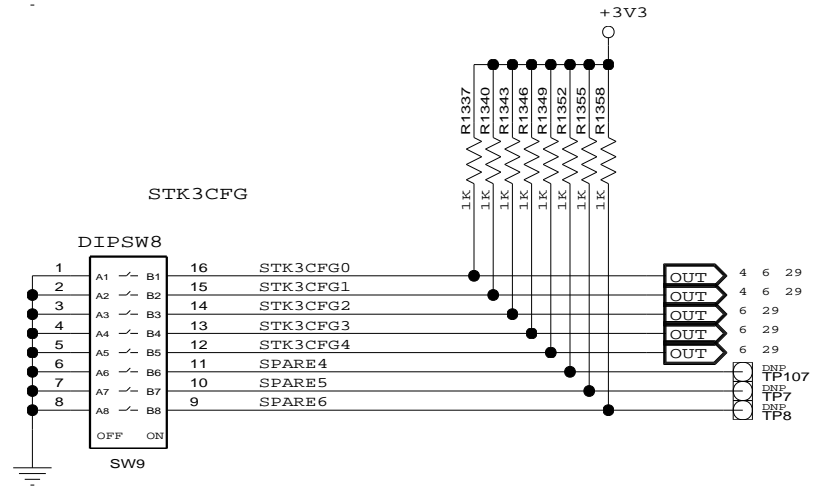
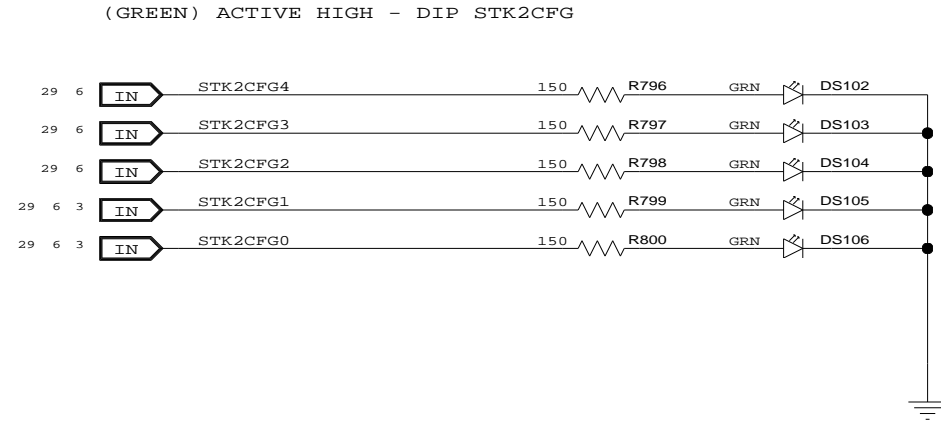
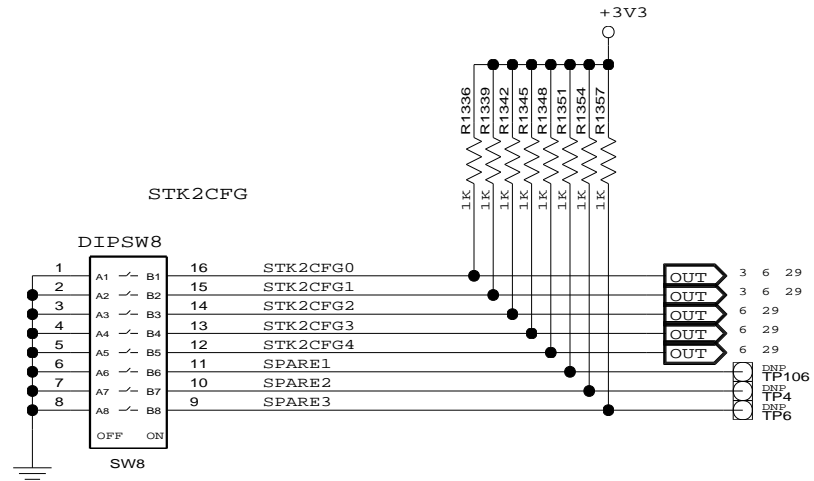
RESET, SMBUS, EEPROM, JTAG

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

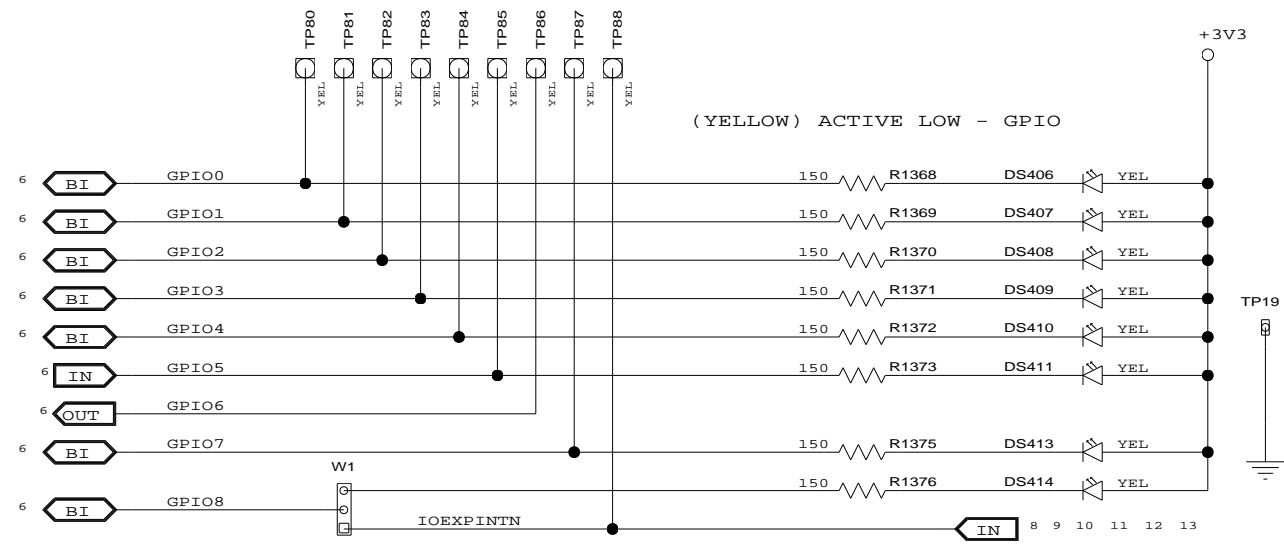
Thu Jun 10 11:24:52 2010

SHEET 28 OF 41

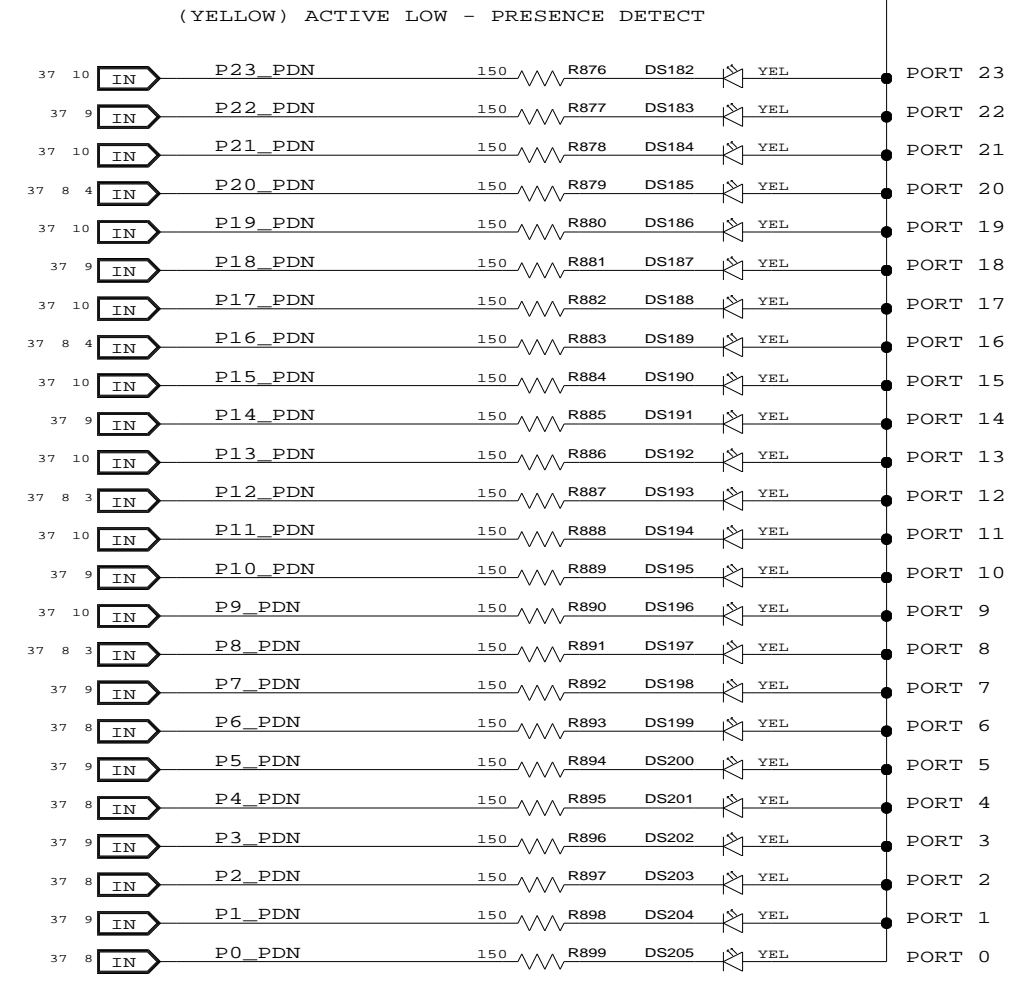
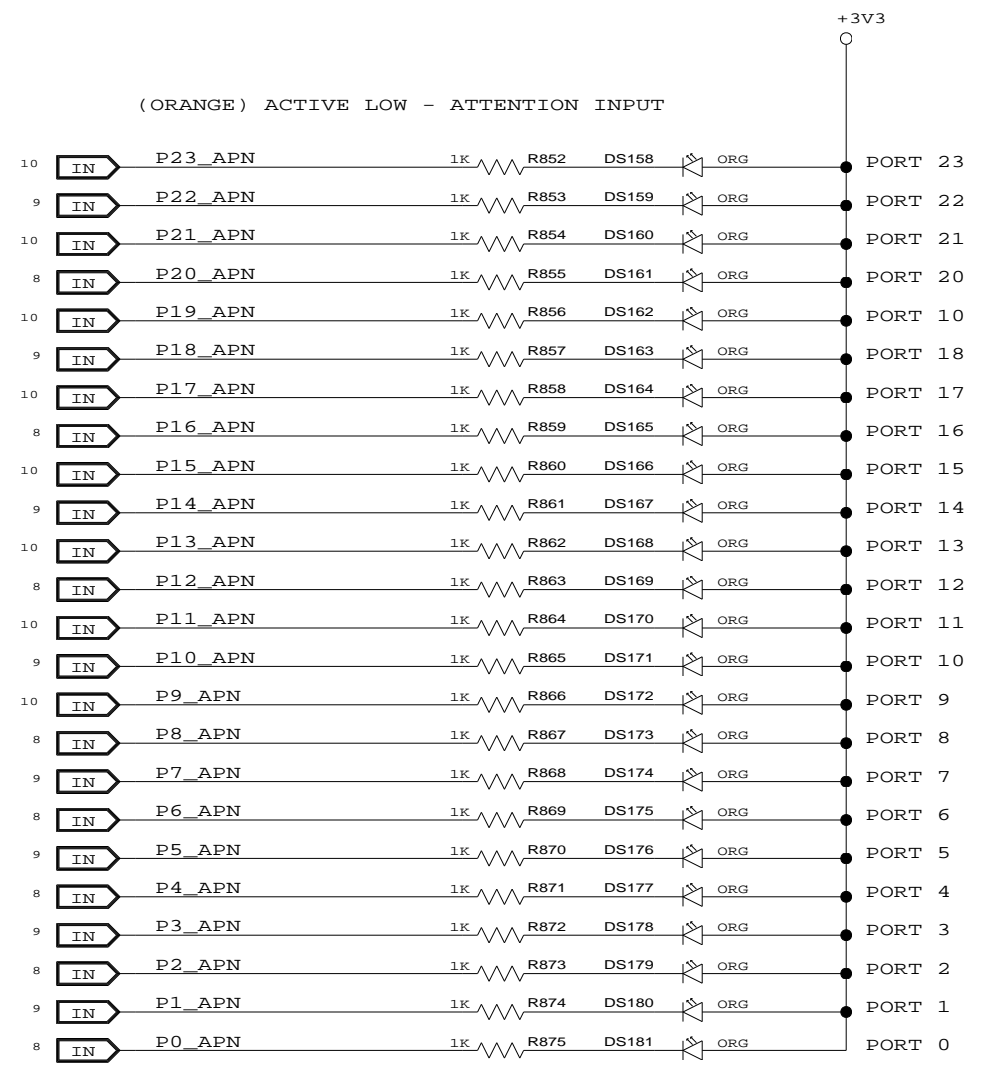


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TITLE EB-LOGAN-19			
DIP SWITCHES			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
Thu Jun 10 11:24:52 2010			SHEET 29 OF 41

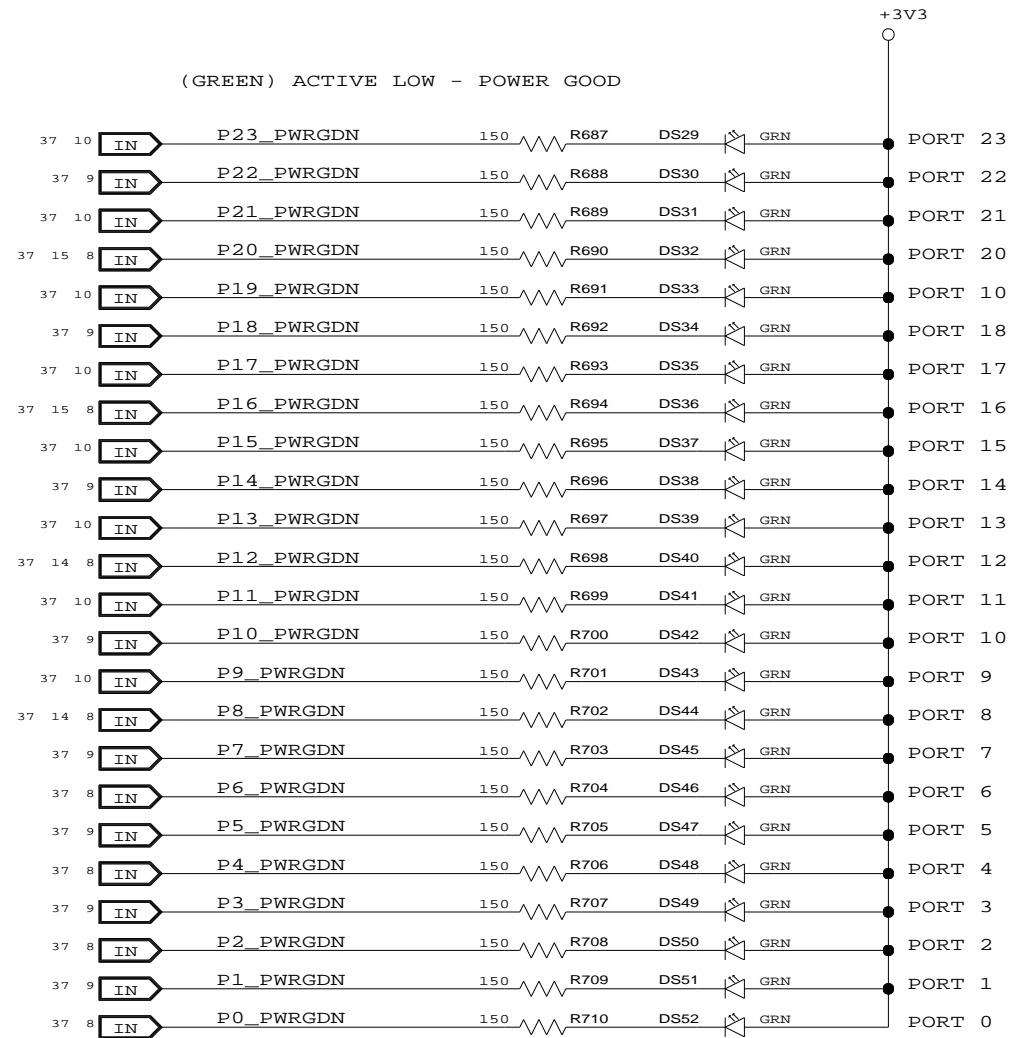
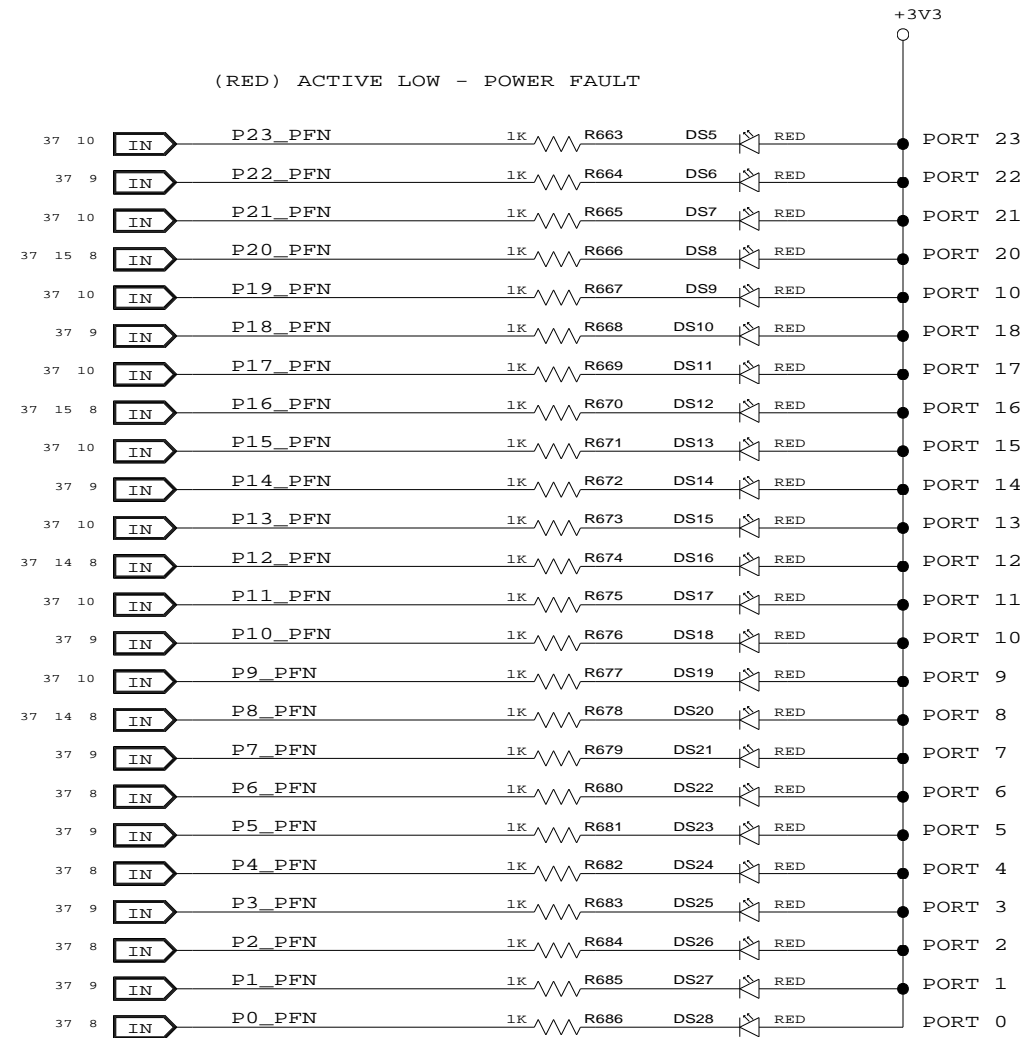


GPIO	ALT0	ALT1
0	PART0PERSTN	P16LINKUPN
1	PART1PERSTN	P16ACTIVEN
2	PART2PERSTN	P4LINKUPN
3	PART3PERSTN	P4ACTIVEN
4	FAILOVER0	P0LINKUPN
5	GPEN	P0ACTIVEN
6	FAILOVER1	FAILOVER3
7	FAILOVER2	P8LINKUPN
8	IOEXPINTN W1:1-2	P8ACTIVEN W1:2-3



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TITLE EB-LOGAN-19			
LED - PORT STATUS (1 OF 7)			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:53 2010			SHEET 30 OF 41



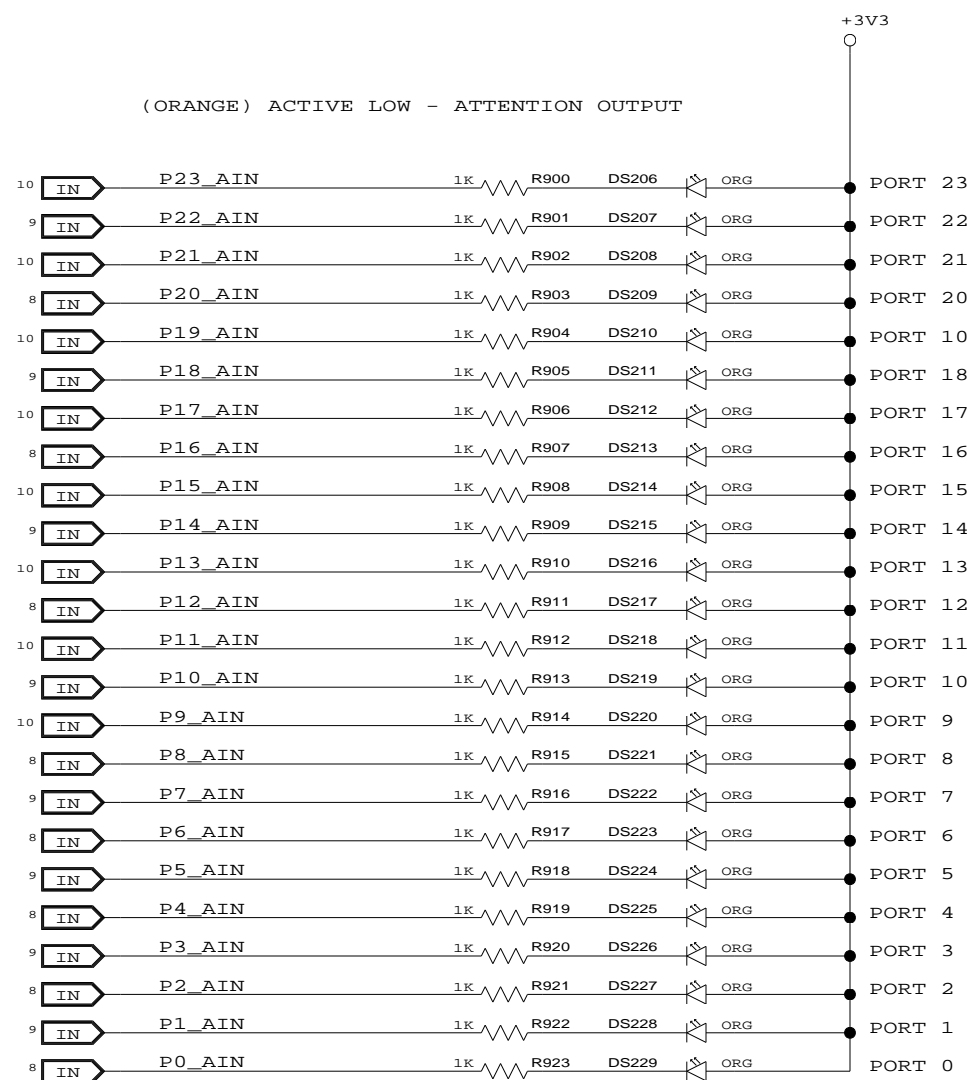
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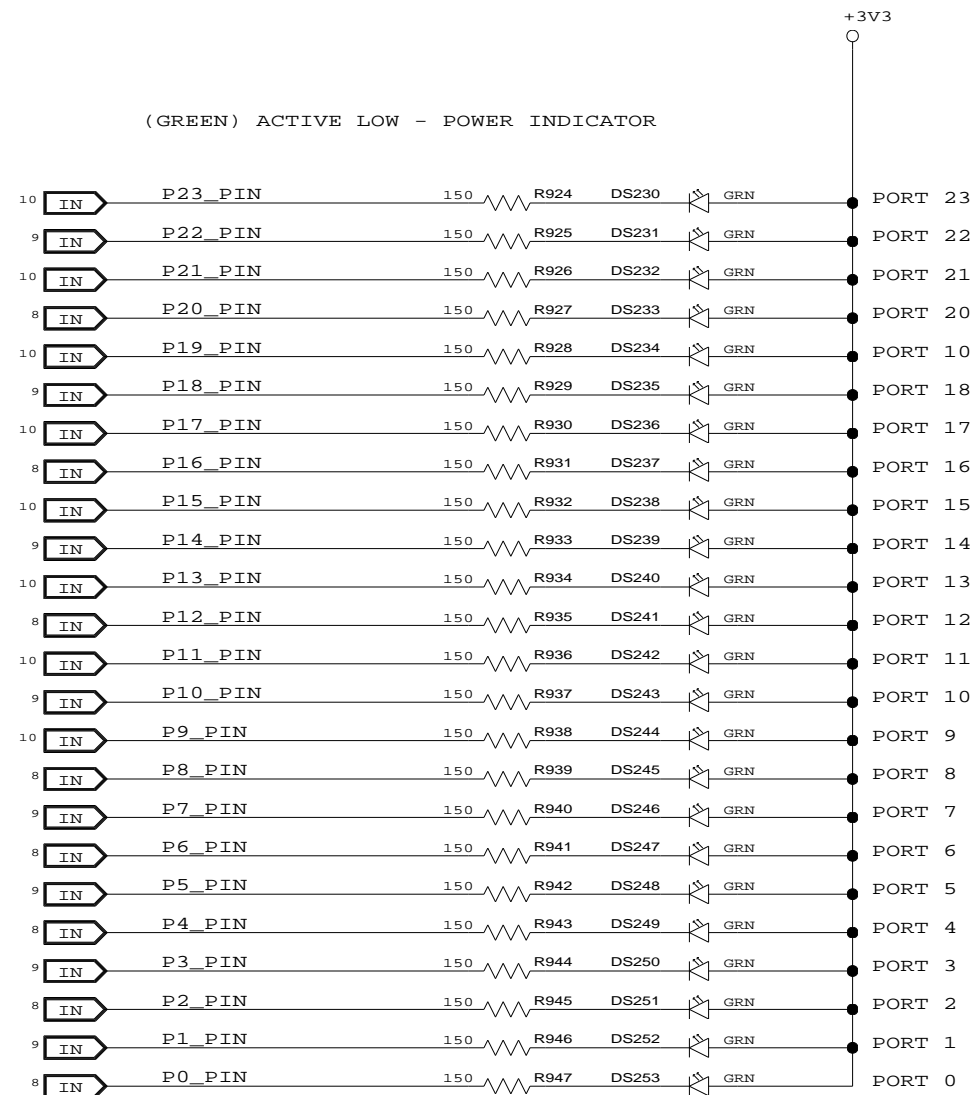
LED - PORT STATUS (2 OF 7)

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:53 2010			SHEET 31 OF 41

(ORANGE) ACTIVE LOW - ATTENTION OUTPUT



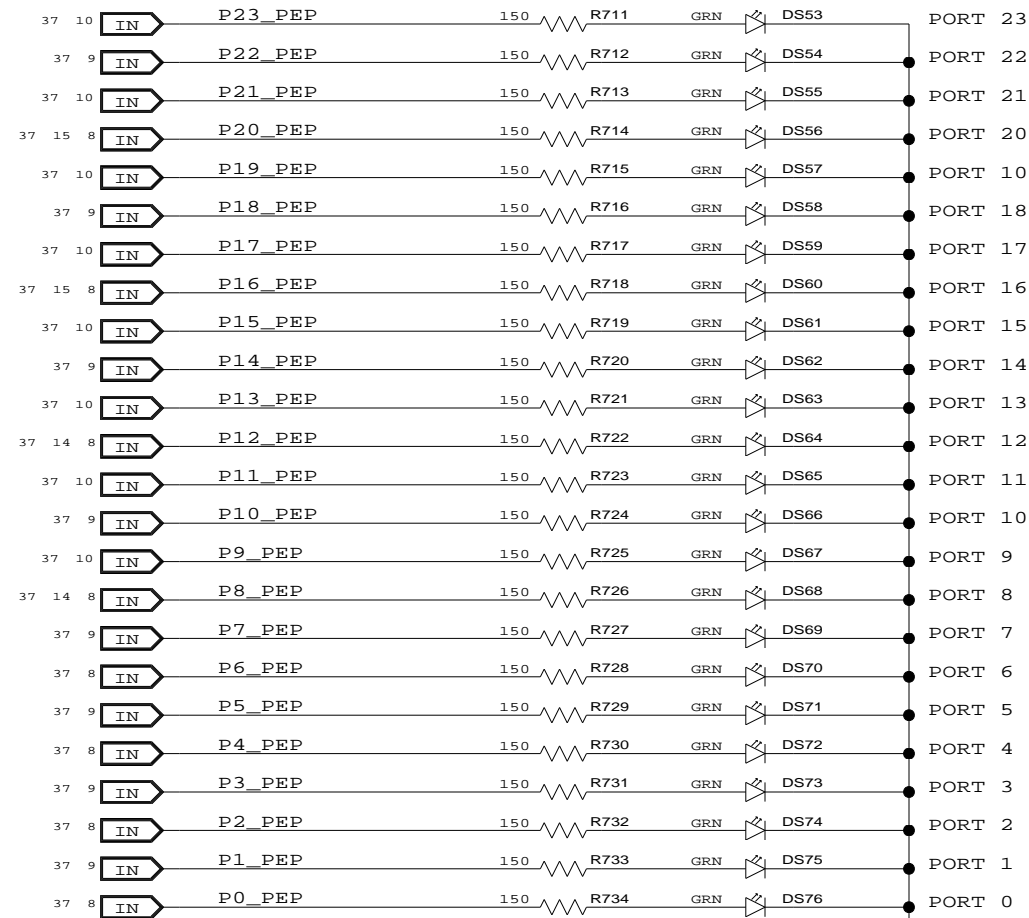
(GREEN) ACTIVE LOW - POWER INDICATOR



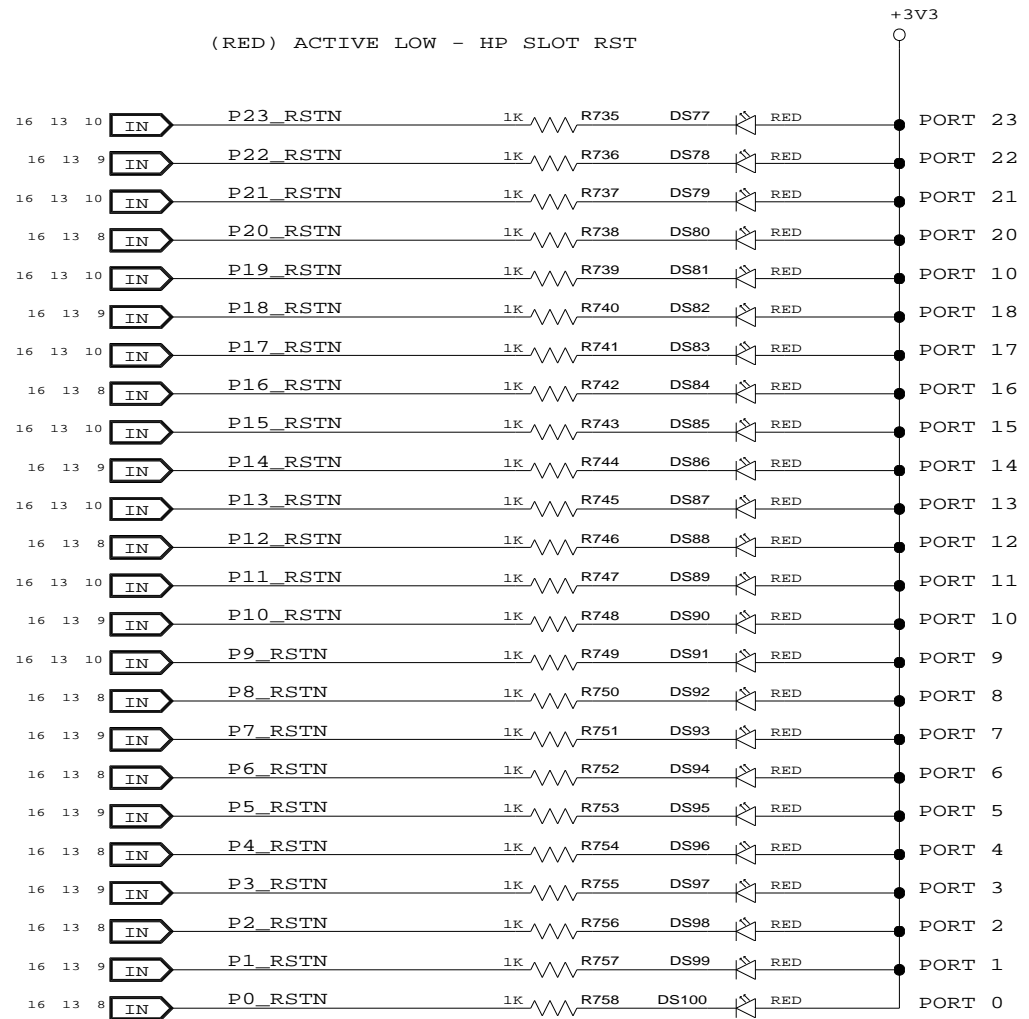
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TITLE EB-LOGAN-19			
LED - PORT STATUS (3 OF 7)			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
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(GREEN) ACTIVE HIGH - POWER ENABLE



(RED) ACTIVE LOW - HP SLOT RST



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LED - PORT STATUS (4 OF 7)

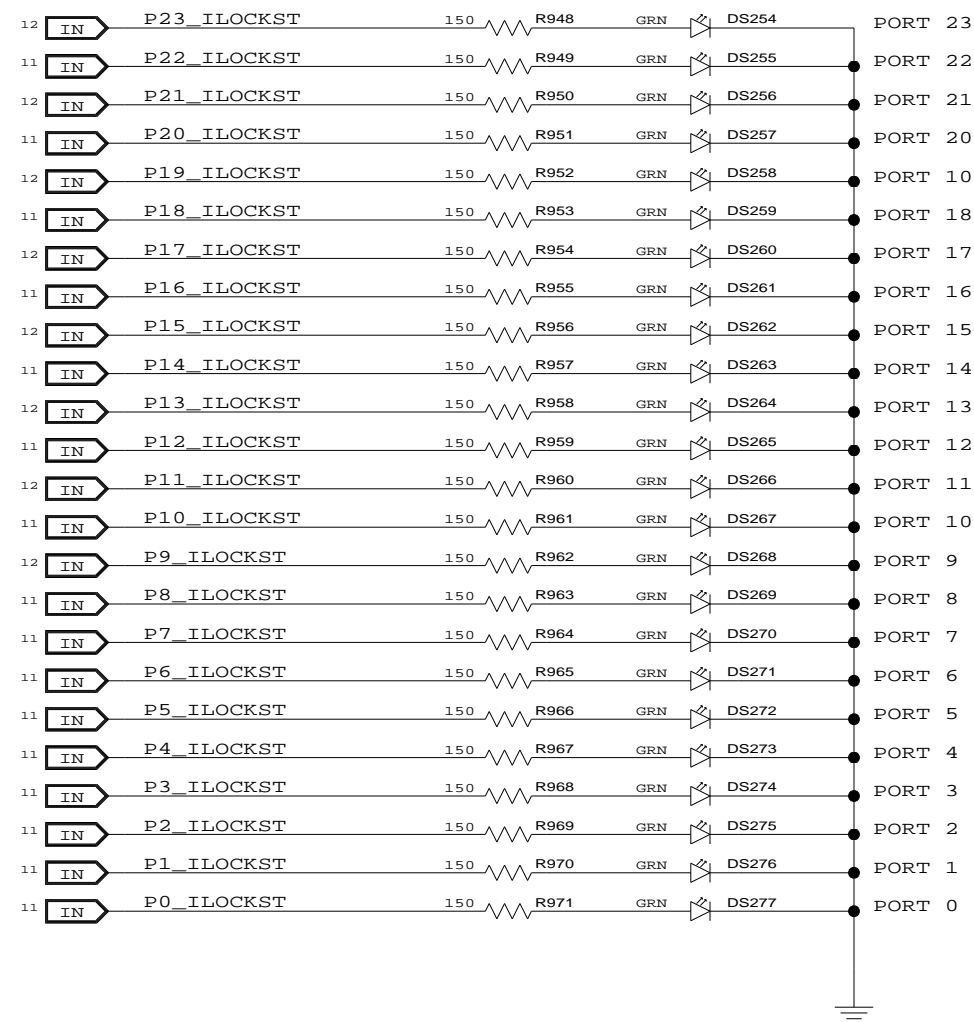
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
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AUTHOR Tony Tran	CHECKED BY Derek Huang
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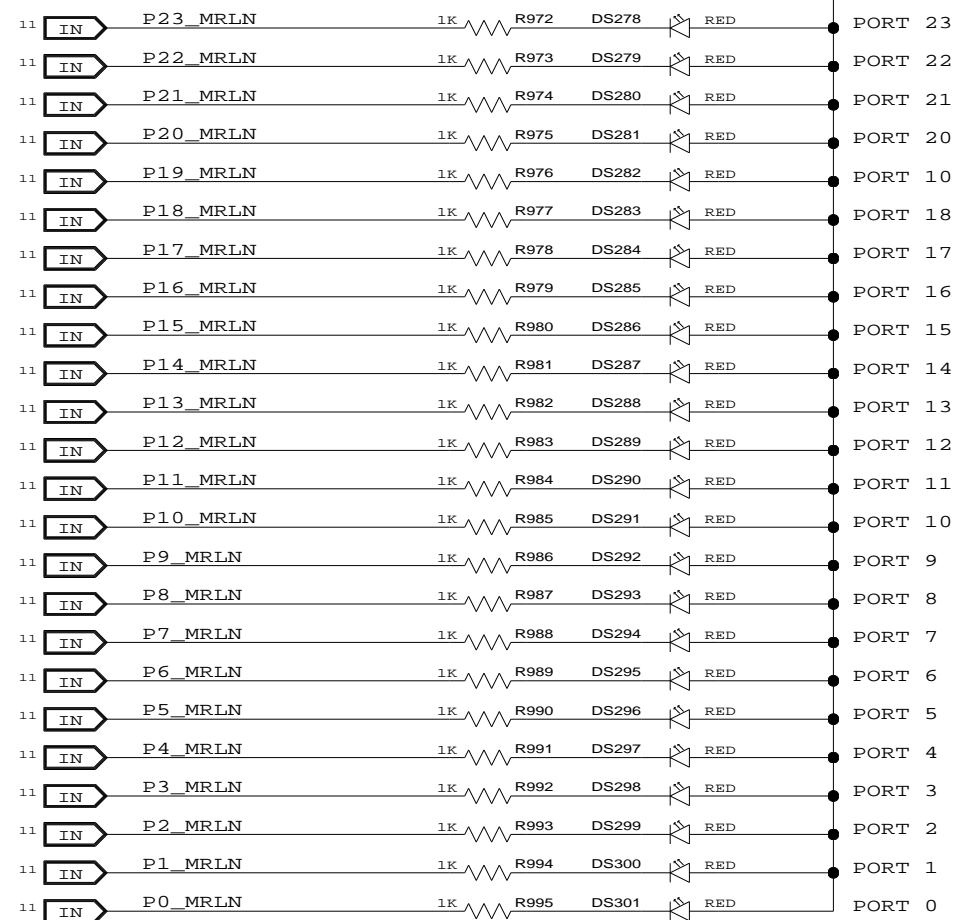
Thu Jun 10 11:24:54 2010

SHEET 33 OF 41

(GREEN) ACTIVE HIGH - INTERLOCK INPUT



(RED) ACTIVE LOW - MRL



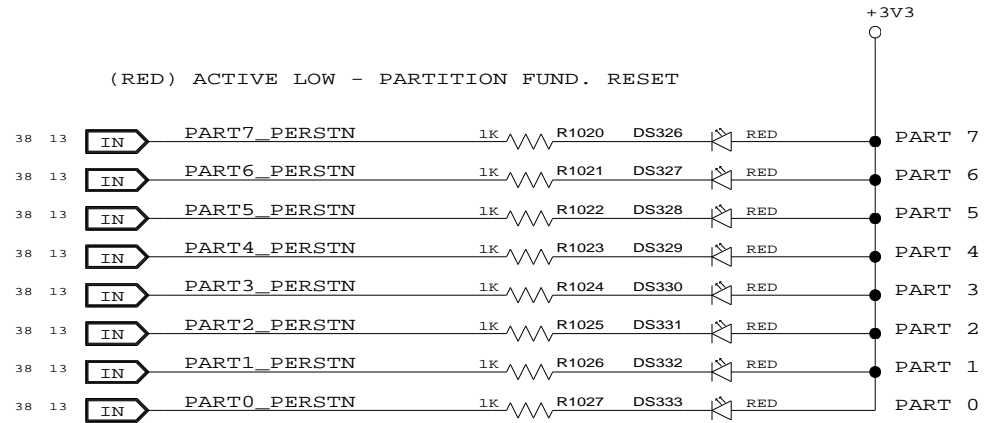
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TITLE EB-LOGAN-19

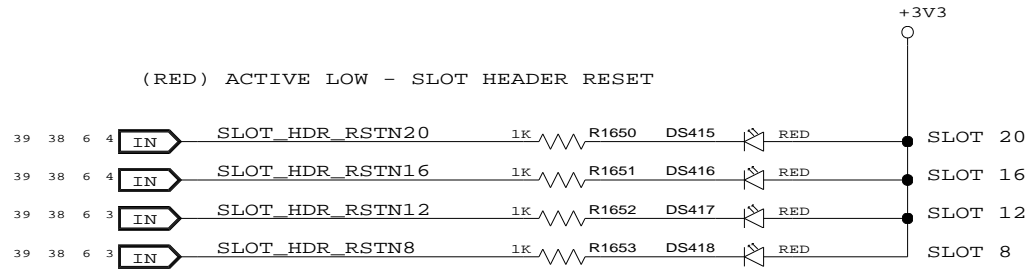
LED - PORT STATUS (5 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:54 2010			SHEET 34 OF 41

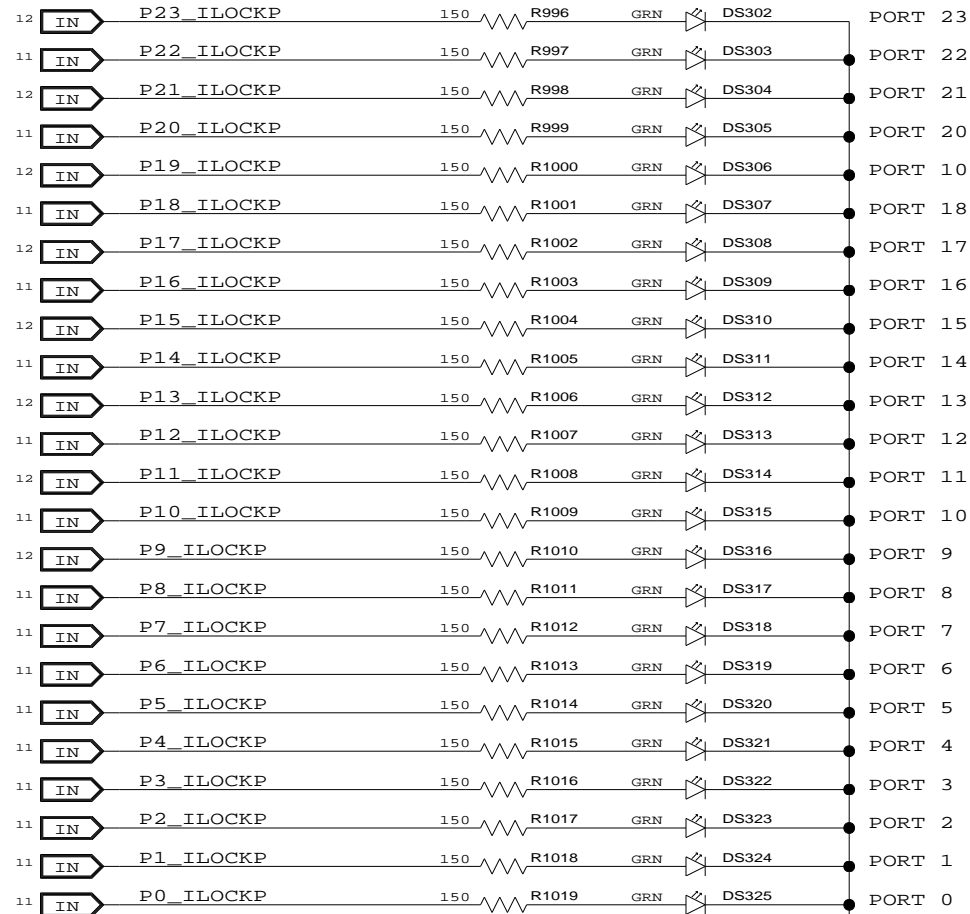
(RED) ACTIVE LOW - PARTITION FUND. RESET



(RED) ACTIVE LOW - SLOT HEADER RESET



(GREEN) ACTIVE HIGH - INTERLOCK OUTPUT



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TITLE EB-LOGAN-19

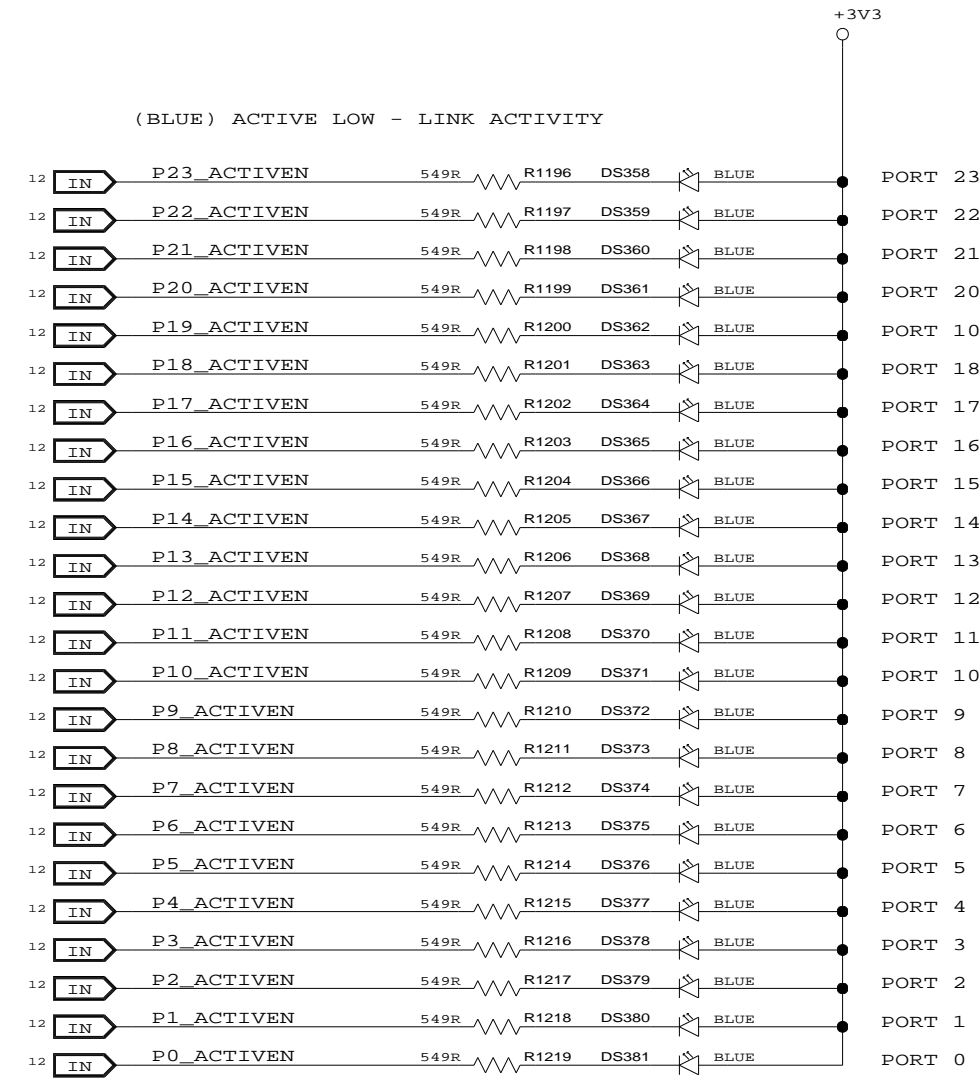
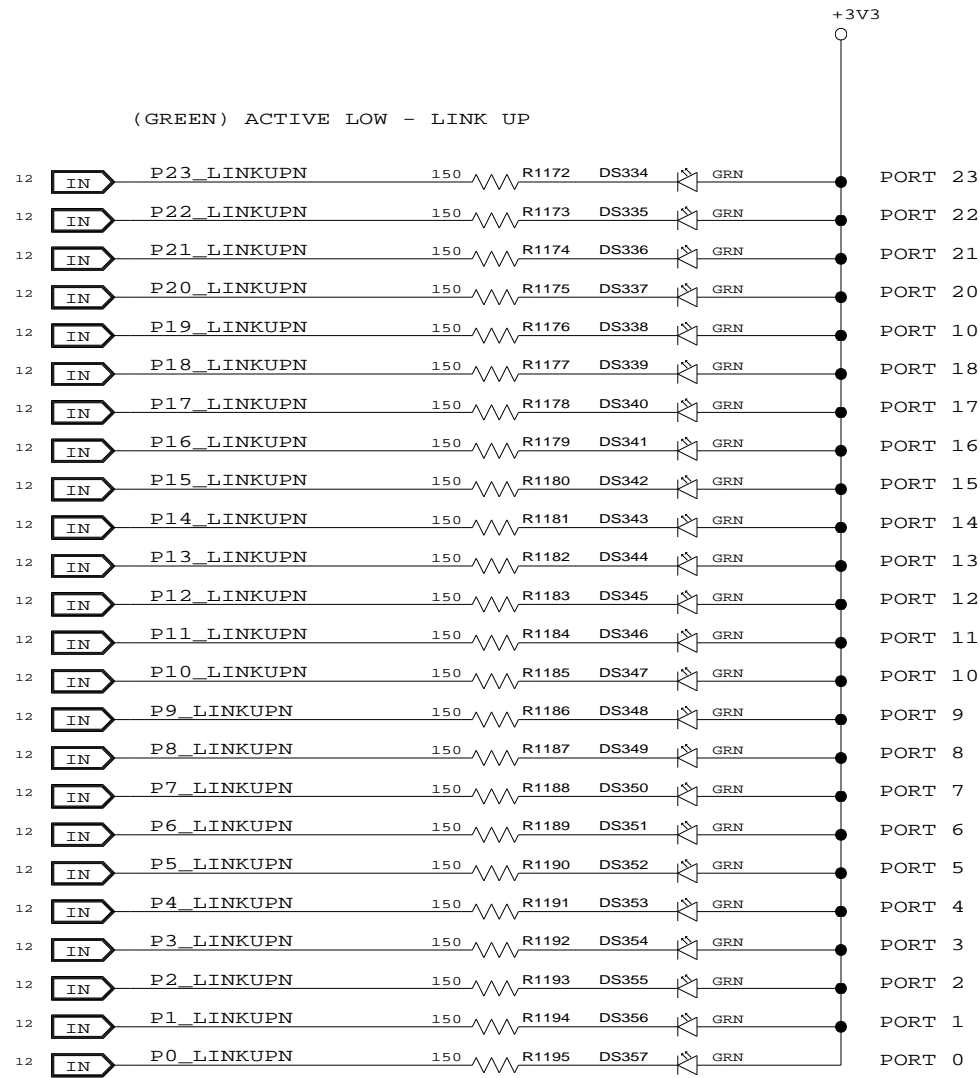
LED - PORT STATUS (6 OF 7)

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0

AUTHOR	CHECKED BY
Tony Tran	Derek Huang

Thu Jun 10 11:24:54 2010

SHEET 35 OF 41



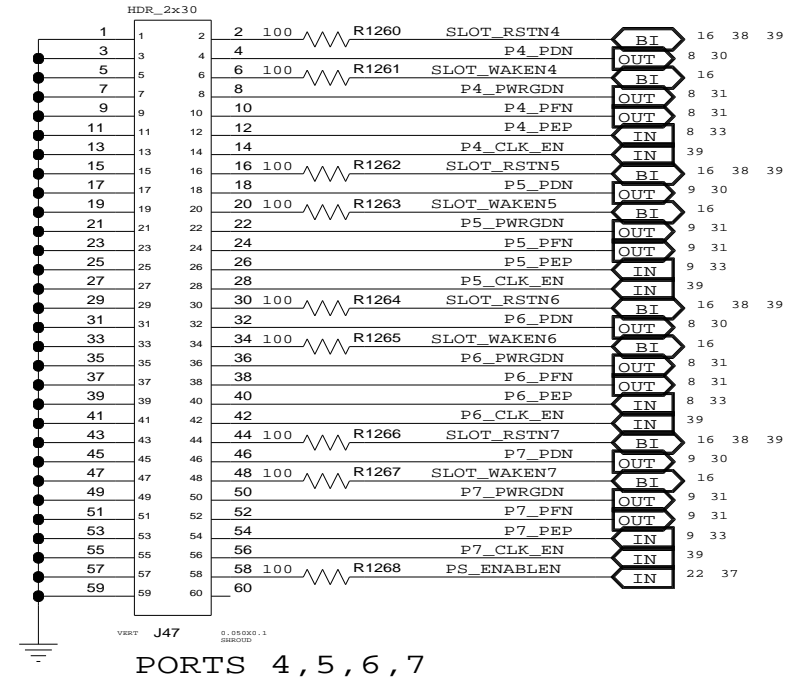
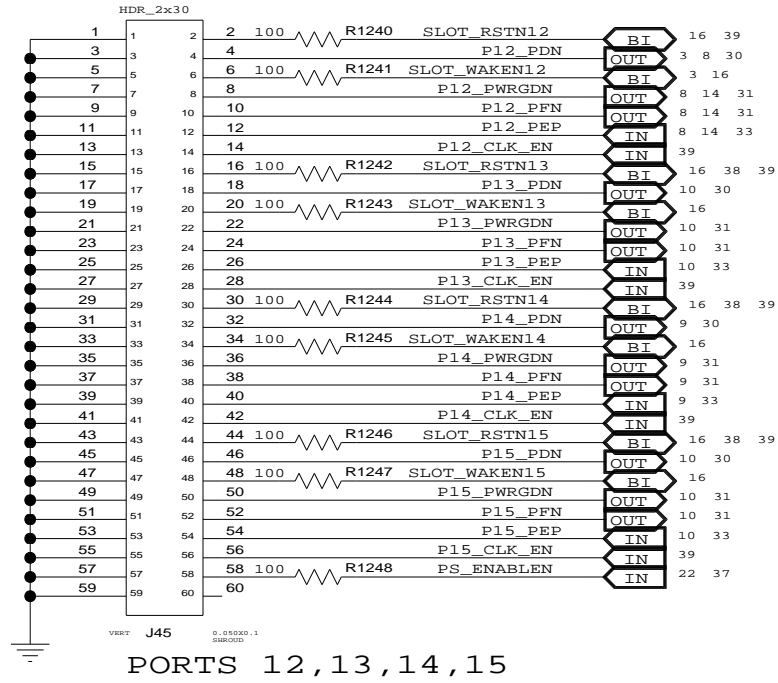
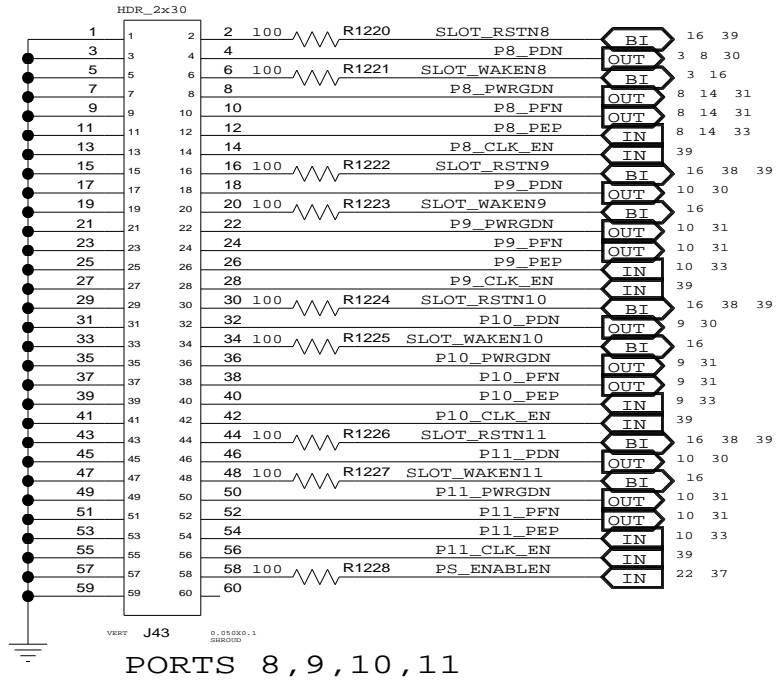
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TITLE EB-LOGAN-19

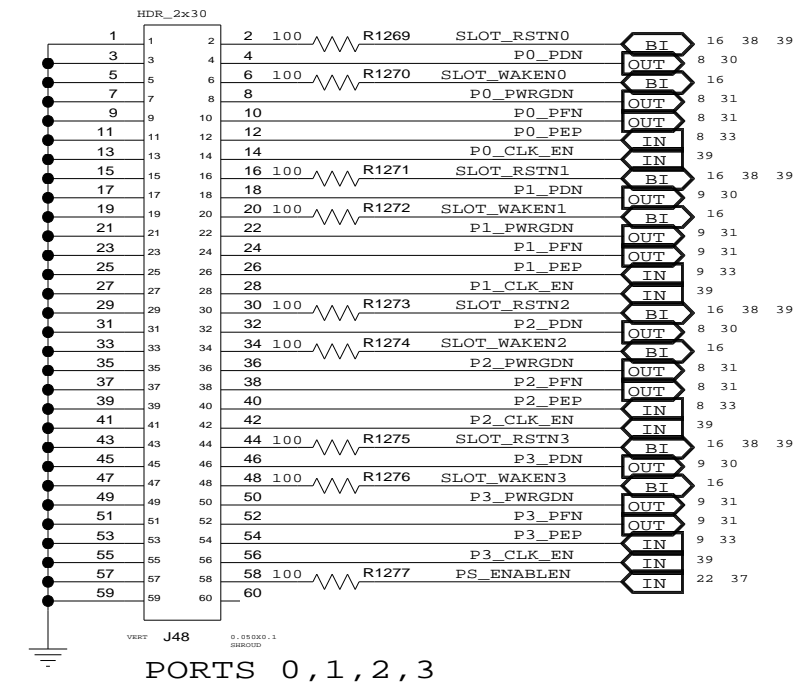
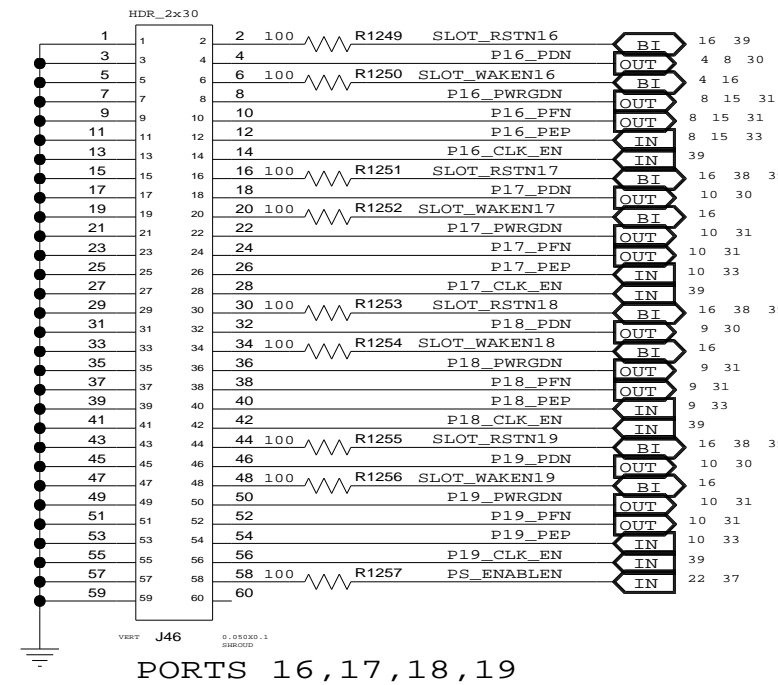
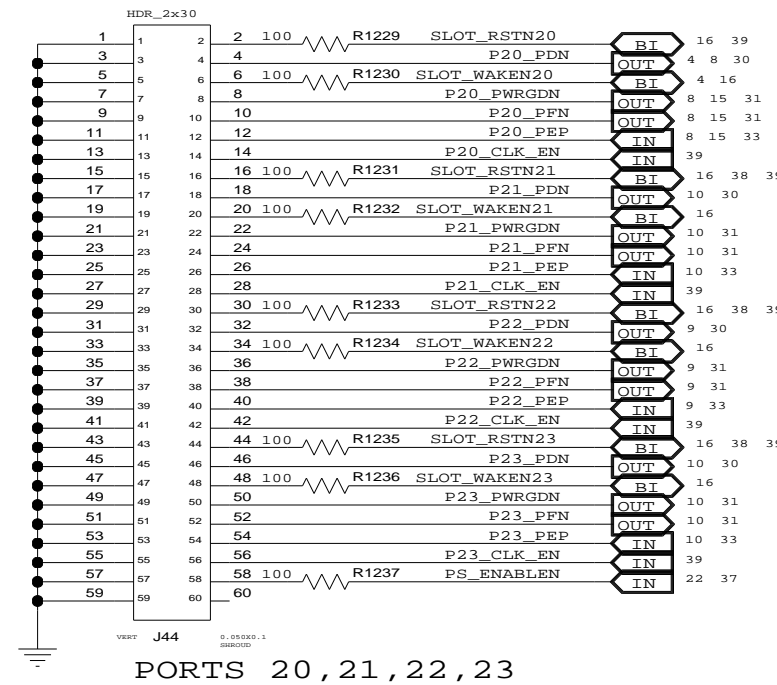
LED - PORT STATUS (7 OF 7)

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:55 2010			SHEET 36 OF 41

SLOT\_RESETN  
 CARD\_PRESENTN  
 WAKEN  
 POWERGOOD  
 PWR\_FLTN  
 PWR\_ENABLE  
 CLOCK\_ENABLEN  
 PS\_ENABLEN  
 CABLE SENSE



SLOT\_RESETN  
 CARD\_PRESENTN  
 WAKEN  
 POWERGOOD  
 PWR\_FLTN  
 PWR\_ENABLE  
 CLOCK\_ENABLEN  
 PS\_ENABLEN  
 CABLE SENSE

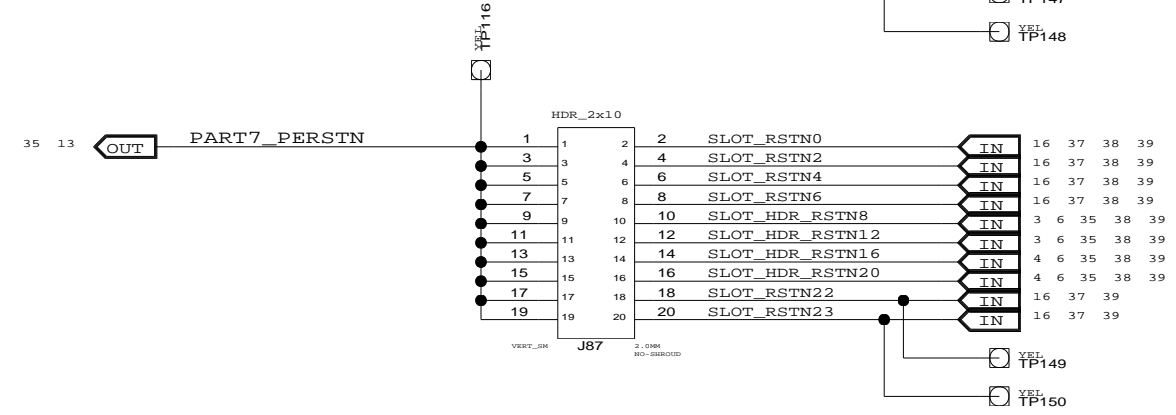
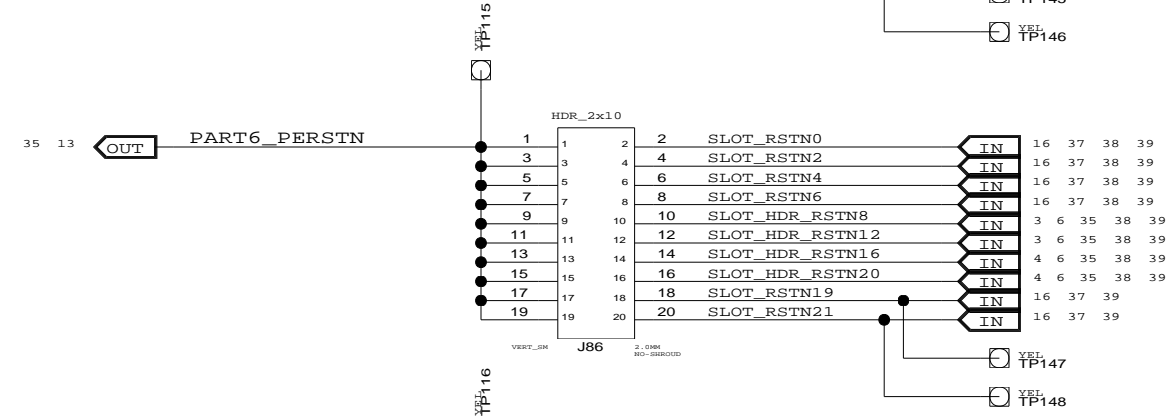
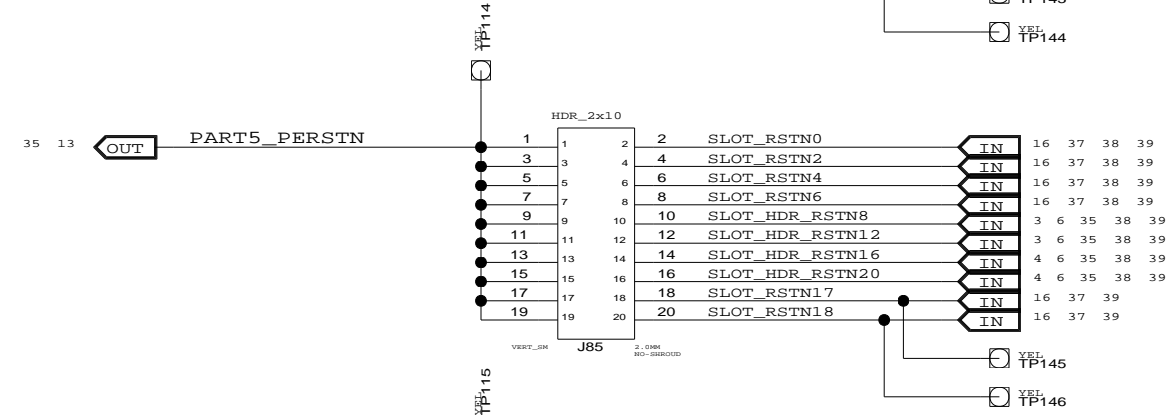
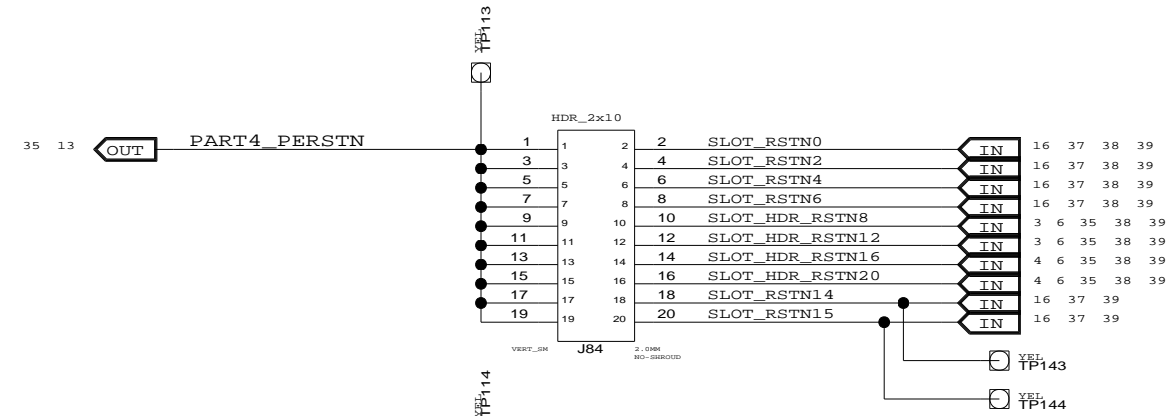
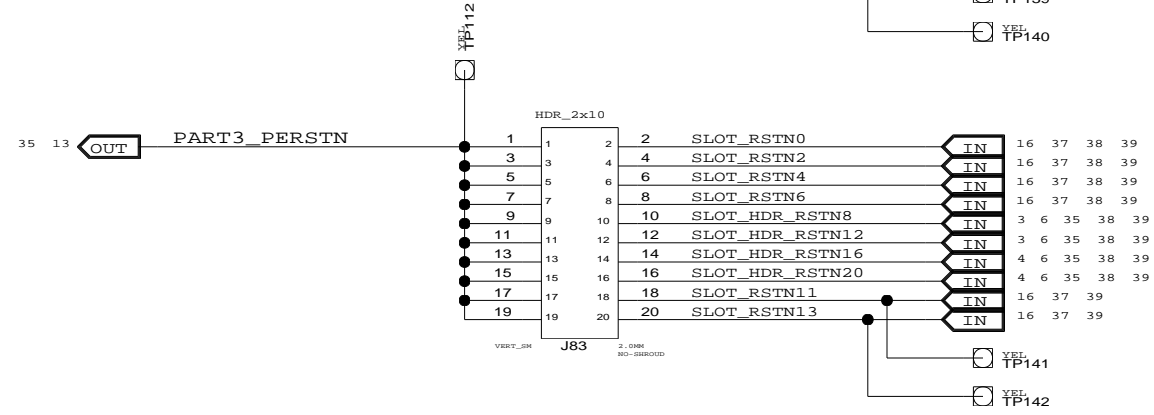
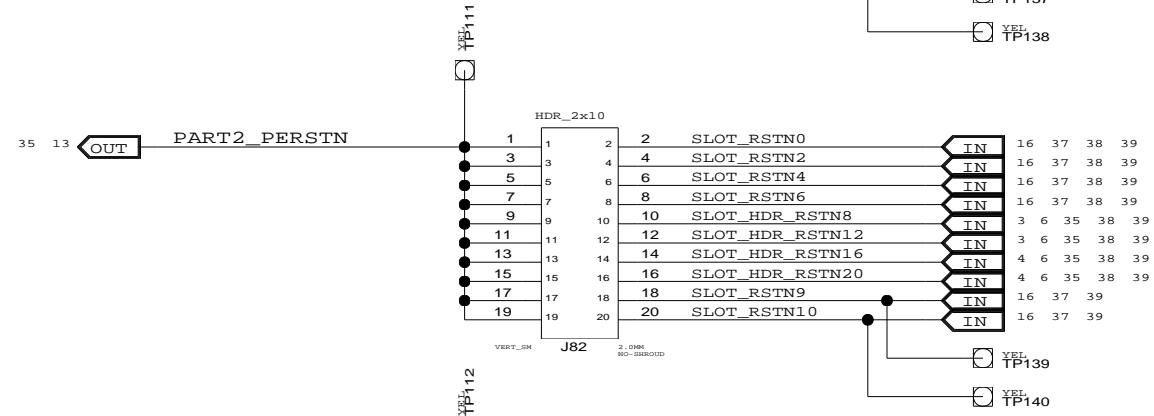
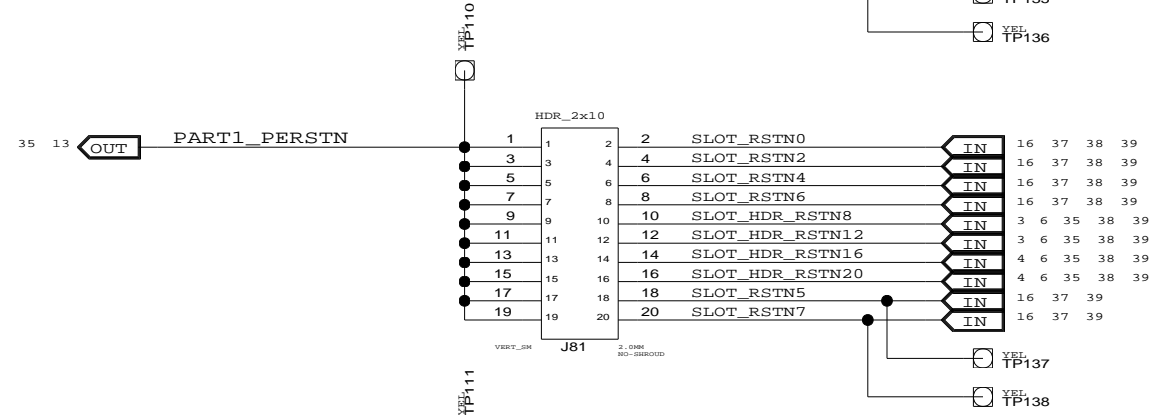
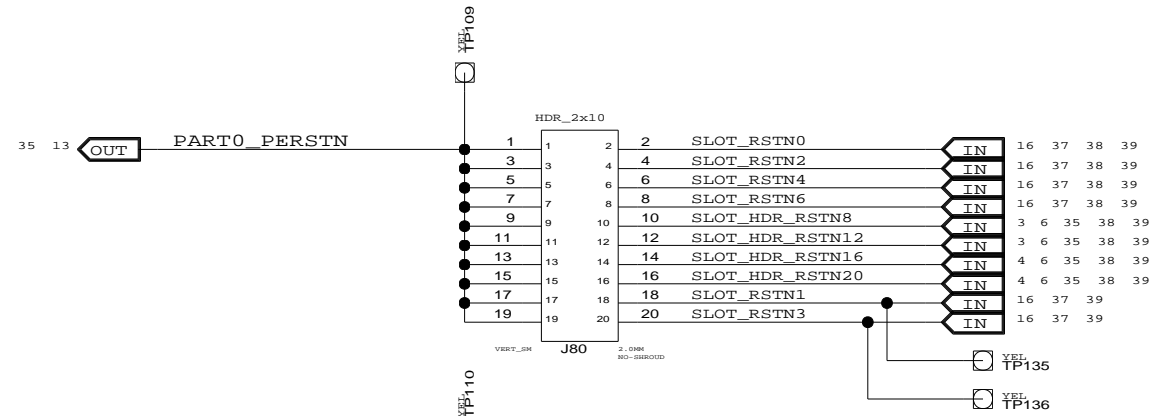


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TITLE EB-LOGAN-19

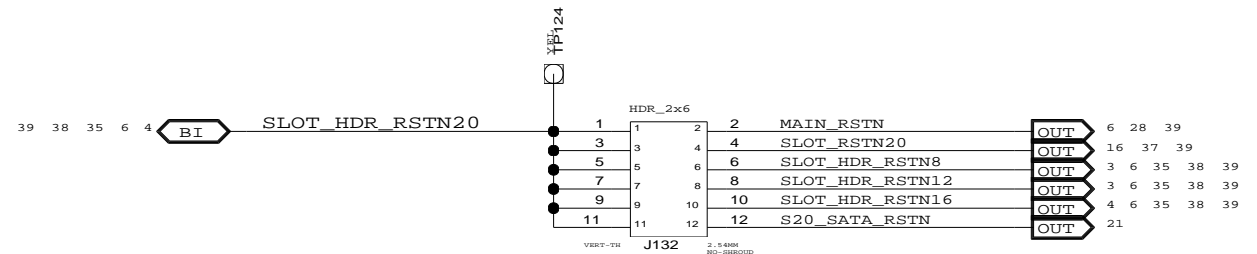
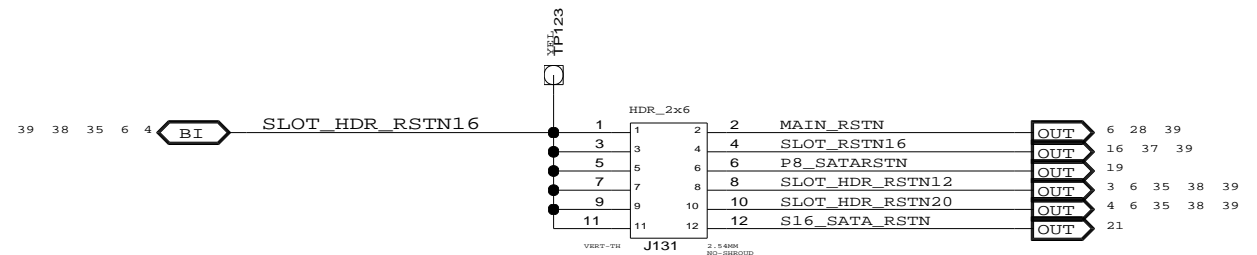
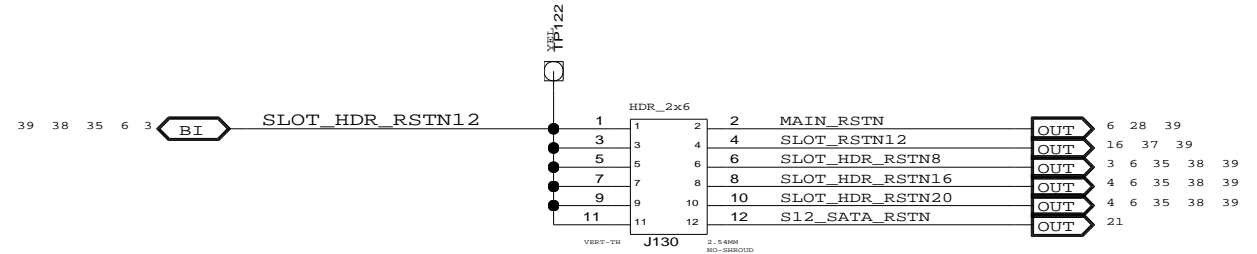
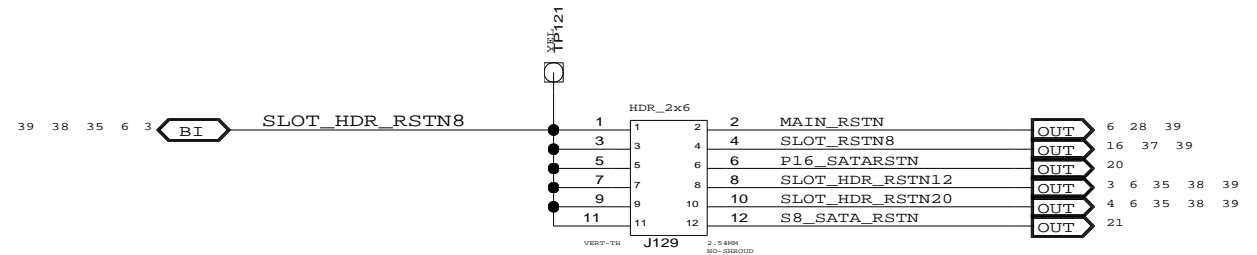
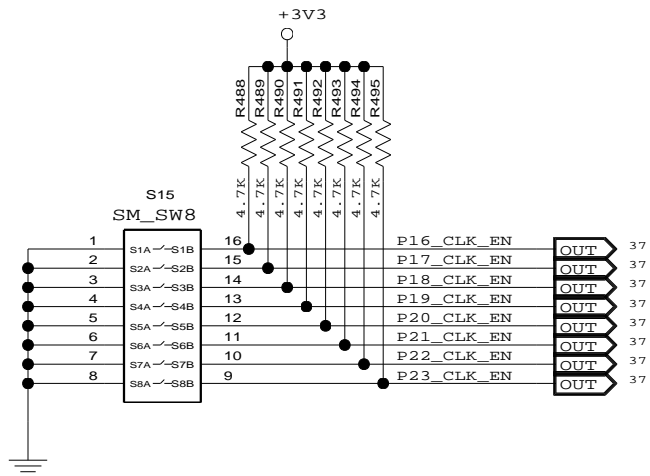
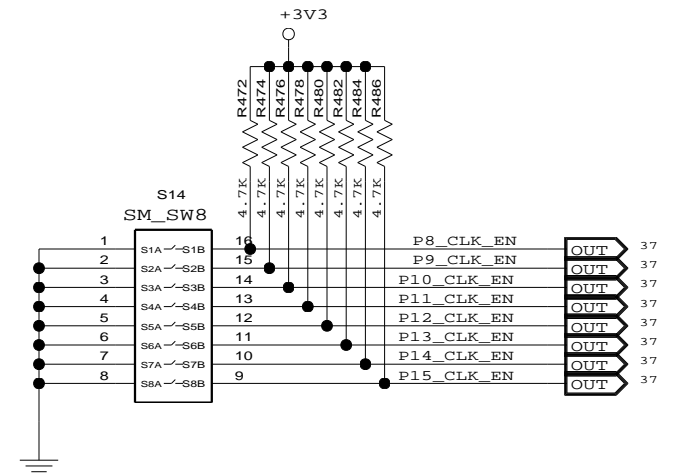
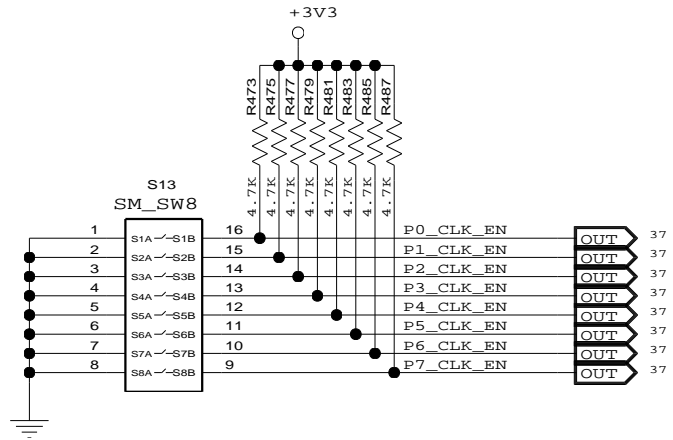
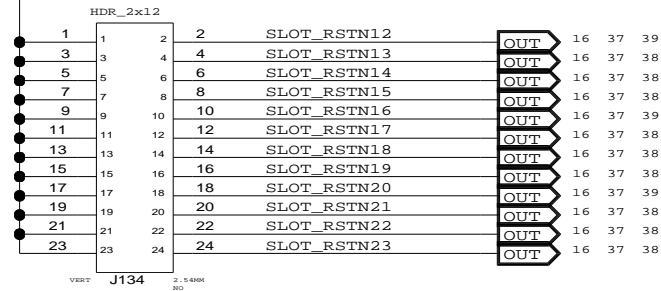
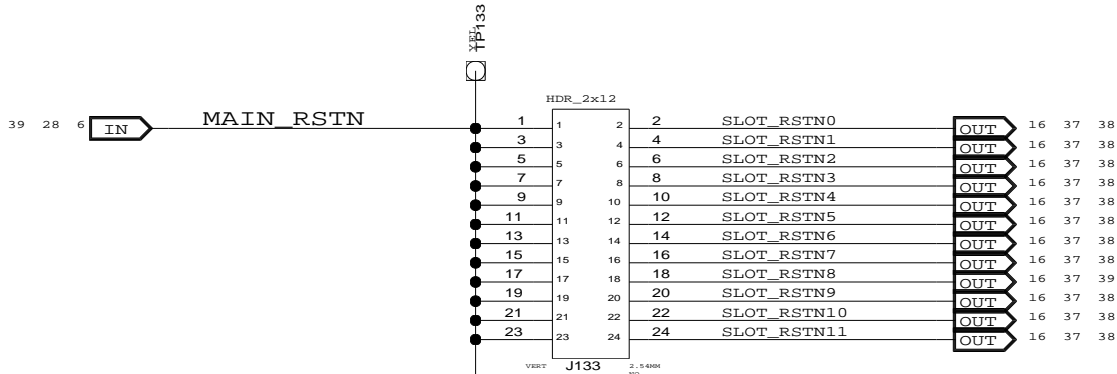
SIDEBAND CONNECTORS

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:55 2010		SHEET 37 OF 41	



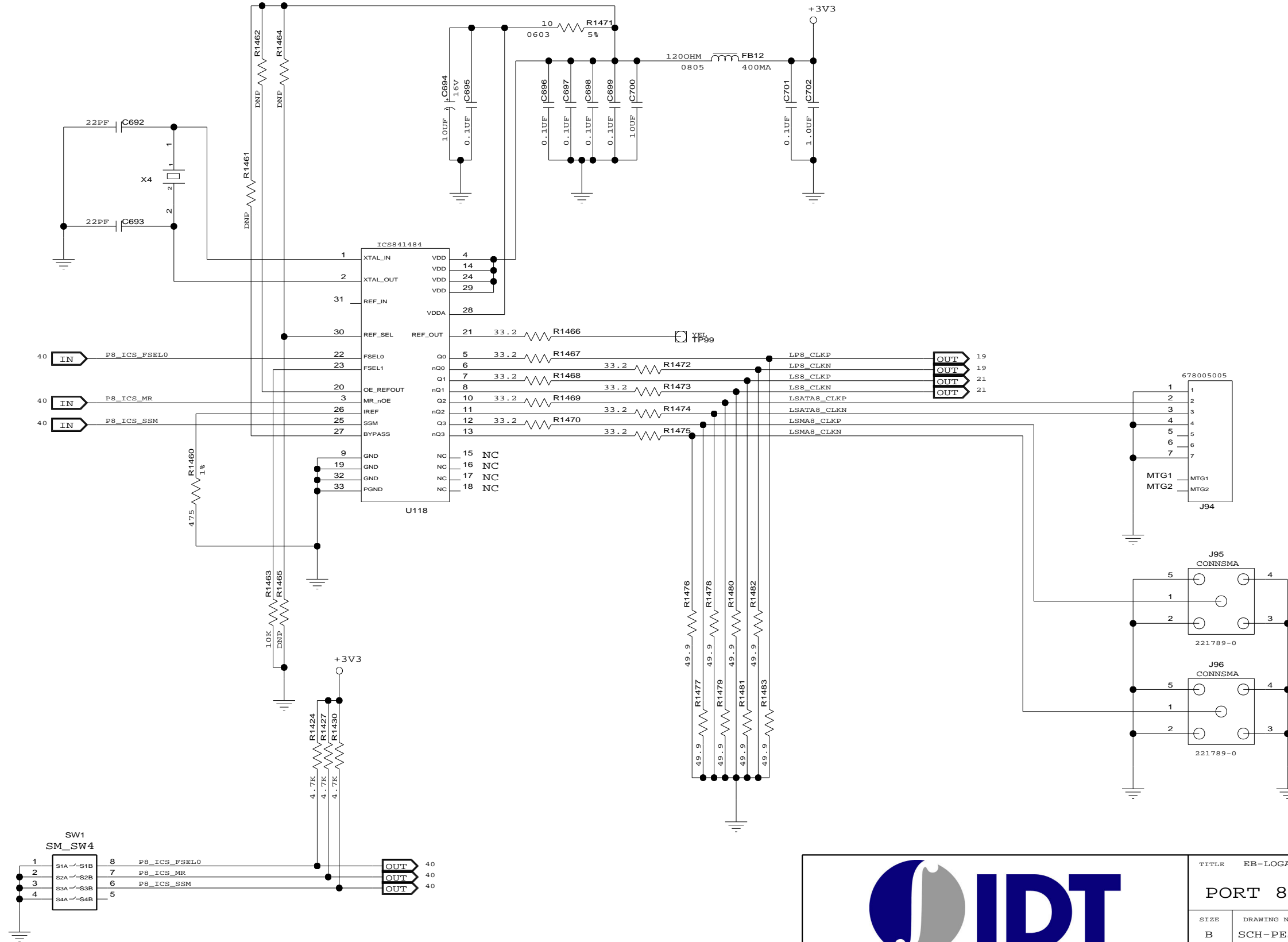
		TITLE EB-LOGAN-19	
		PARTITION RESET SELECT HEADERS	
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
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NOTE: DNP JUMPERS WHEN IOEXPANDER IS ENABLED



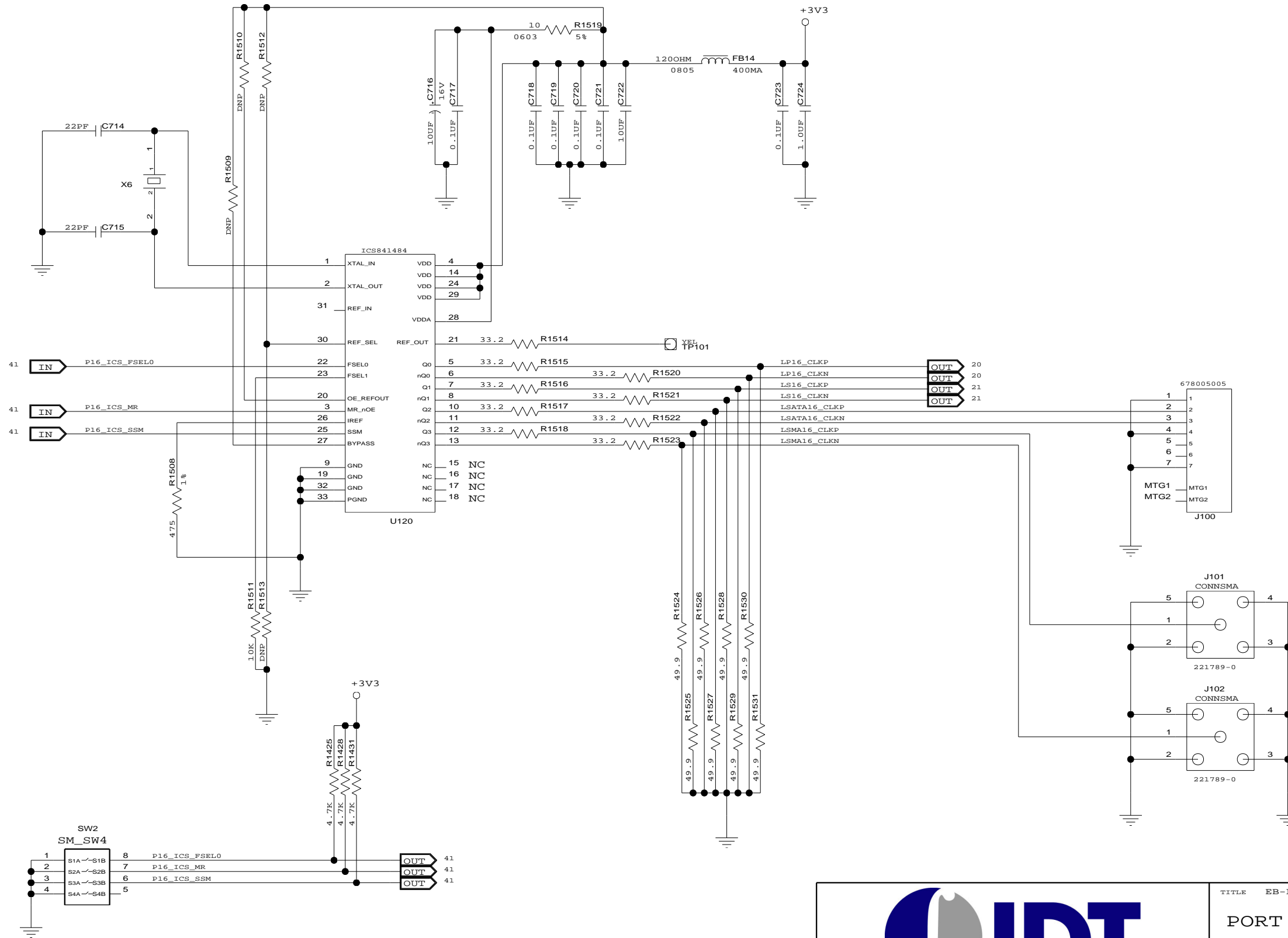
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TITLE EB-LOGAN-19			
SLOT RESET SELECT HEADERS			
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-PESEB-002	18-692-001	2.0
AUTHOR		CHECKED BY	
Tony Tran		Derek Huang	
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TITLE EB-LOGAN-19			
PORT 8 CLOCK GENERATOR			
SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
Thu Jun 10 11:24:56 2010			SHEET 40 OF 41



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TITLE EB-LOGAN-19

PORT 16 CLOCK GENERATOR

SIZE B	DRAWING NO. SCH-PESEB-002	FAB P/N 18-692-001	REV. 2.0
AUTHOR Tony Tran		CHECKED BY Derek Huang	
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