



**THE DATASHEET OF
TLK10021GWQ**



Product Bulletin

TLK10021—10 Gbps PHY Transceiver for LAN/MAN/SAN Applications

The Texas Instruments (TI) TLK10021 device is a single channel monolithic CMOS physical layer (PHY) transceiver designed for use in 10 Gbps applications. Its XFI-compliant serial interconnect supports interfacing with XFP modules at 10 Gigabit Ethernet or 10 Gigabit Fibre Channel data rates. Its flexible system side interconnect supports interfacing with MACs and ASICs using a XAUI interface.

The TLK10021 device makes use of CMOS technology to offer an advanced combination of high-performance (10 Gbps) and low-

power consumption (800 mW). Full PCS, PMA and XGXS sublayer functionality is provided through the consolidation of the receiver and transmitter PHY functions on a single chip, along with the integration of encode/decode/alignment logic, FIFOs, integrated clock drivers, multiple loopback features and PRBS generation, and verification for both the line side and the system side. This combination reduces the number of components and enables 10 Gbps Ethernet and Fibre Channel systems to dissipate much less power.

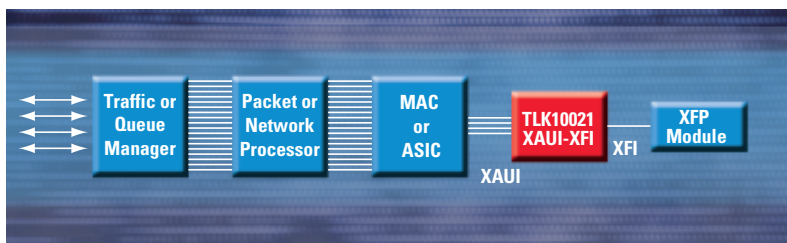


Figure 1: XFP-based Line Card

TLK 10021

Device	Line Side (Gbps)	System Side (Gbps)	Standard
10 Gigabit Ethernet	10.3125	4 x 3.125	IEEE802.3ae
10 Gigabit Fibre Channel	10.51875	4 x 3.1875	INCITS 10GFC

TLK10021

Key Features

- Minimal power consumption (800 mW)
- 1.2 V and 2.5 V power supplies
- On-chip clock generation and data recovery
- High-speed adaptive receive equalization
- Multiple external reference clock frequencies
- Optional 10 GHz / divide-by-64 output clock
- Fast lock time – 30 ns
- Programmable XAUI and XFI polarity
- Programmable XAUI lane ordering
- Adjustable XAUI transmit equalization
- Multiple loopback modes
- PRBS generator and checker
- MDIO and SDA/SCL management interfaces
- JTAG support
- 13 x 13 mm PBGA package with 1.0 mm ball pitch uses less board space
- 0.13 mm CMOS process

Benefits

- Enables increased port density
- Dissipates very low power
- Simplifies system clocking
- Supports XFI-compliance
- Supports different clocking rates
- Helps meet clocking requirements
- Handles bursty data
- Eases board layout
- Enhances data eye
- Enhances testability
- Uses standard control interface
- Supports standard testing access
- Lowers power consumption

Applications

The high-performance features of the TLK10021 device make it the optimal choice for 10 Gbps SerDes

PHY designs targeted at 10 Gigabit Ethernet LAN and MAN systems, 10 Gigabit Fibre Channel systems and all

other applications requiring a device to bridge an XFP module's 10 Gbps serial XFI link to a XAUI system side interface.

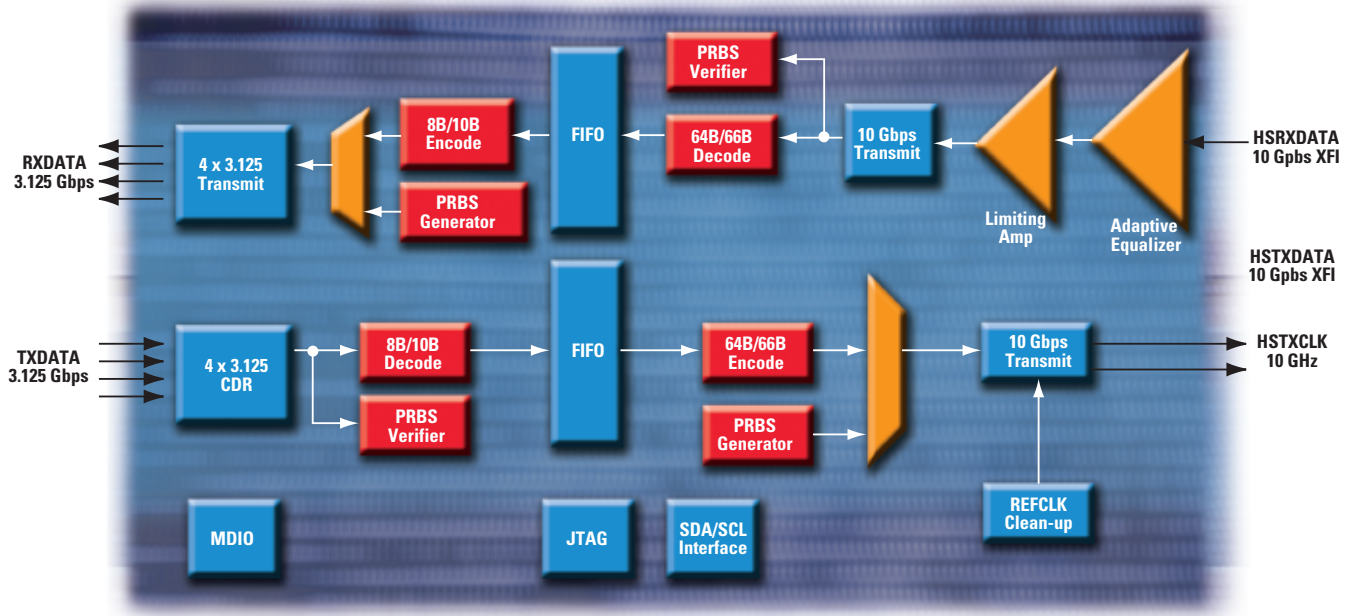


Figure 2: TLK10021 Block Diagram

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