WINSOURCE ELECTRONICS

THE DATASHEET OF

XRT82L24AIV-F

QUAD E1 LINE TRANSCEIVER WITH CLOCK RECOVERY AND JITTER ATTENUATOR

AUGUST 2004 *REV. 1.1.2*

GENERAL DESCRIPTION

The XRT82L24A is a fully integrated Quad (four channels) short-haul line interface unit for E1(2.048Mbps) 75Ω or 120Ω applications. Each channel consists of a receiver with equalizer for reliable data and clock recovery, and a transmitter which accepts either single or dual-rail digital inputs for signal transmission to the line using a low output impedance line driver. The device also includes a crystal-less jitter attenuator which, depending on system requirements, can be selected in the receive or transmit path through the Host or Hardware Mode control.

XRT82L24A is a low power CMOS device operating on a single 3.3V supply with 5V tolerant digital inputs.

FEATURES

- Fully integrated quad, short-haul PCM transceivers for E1 applications.
- On Chip Receive Equalizer and Transmit Pulse Shaper for CEPT 75Ω and 120Ω line terminations
- On chip clock recovery circuit
- Transformer or capacitor coupled receiver inputs
- Crystal-less jitter attenuator can be selected in the transmit or receive path
- High receiver interference immunity
- Per-channel transmit power shutdown
- Tri-state transmit output capability
- On chip per-channel driver failure monitoring circuit
- On chip HDB3/B8ZS/AMI encoder/decoder functions
- Supports Gapped Clock for Multiplexer Mapper Applications
- Transmit return loss meets or exceeds ETSI 300 166 standard
- Meets or exceeds specifications in ITU G.703, G.775, G.736 and G.823; ETSI 300-166
- Meets or exceeds G.783 and G.823 Jitter Specifications
- 3.3V or 5.0V Logic level inputs
- Single +3.3V Supply Operation
- New Patent# 6,313,671B1 Low Power IC I/O Buffer

APPLICATIONS

- Digital cross connects (DSX-1)
- Channel Banks
- High speed data transmission line cards
- E1 Multiplexer
- Public switching systems and PBX interfaces

FIGURE 1. BLOCK DIAGRAM OF THE XRT82L24A E1 LIU (HOST MODE)

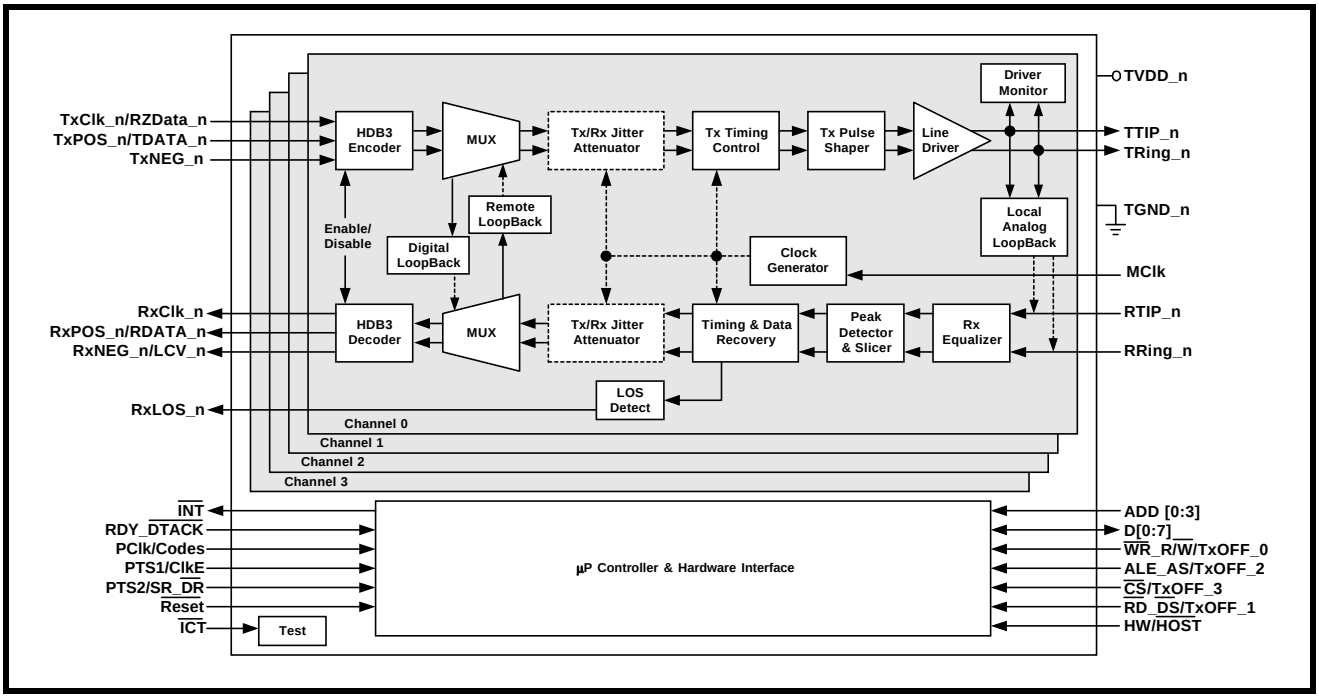
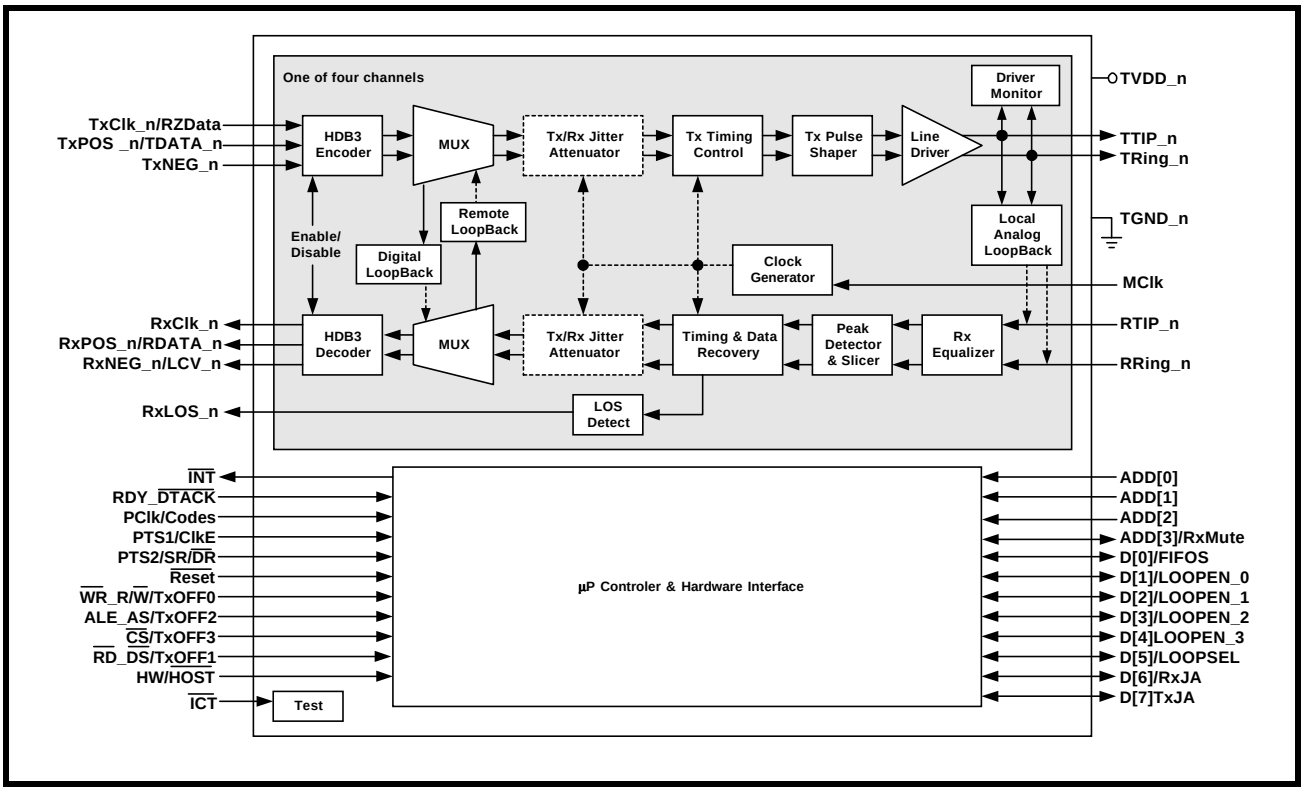


FIGURE 2. BLOCK DIAGRAM OF THE XRT82L24A T1/E1/J LIU (HARDWARE MODE)



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT82L24AIV	100 Lead TQFP (14 x 14 x 1.4mm)	-40°C to +85°C

FIGURE 3. PIN OUT OF THE XRT82L24A

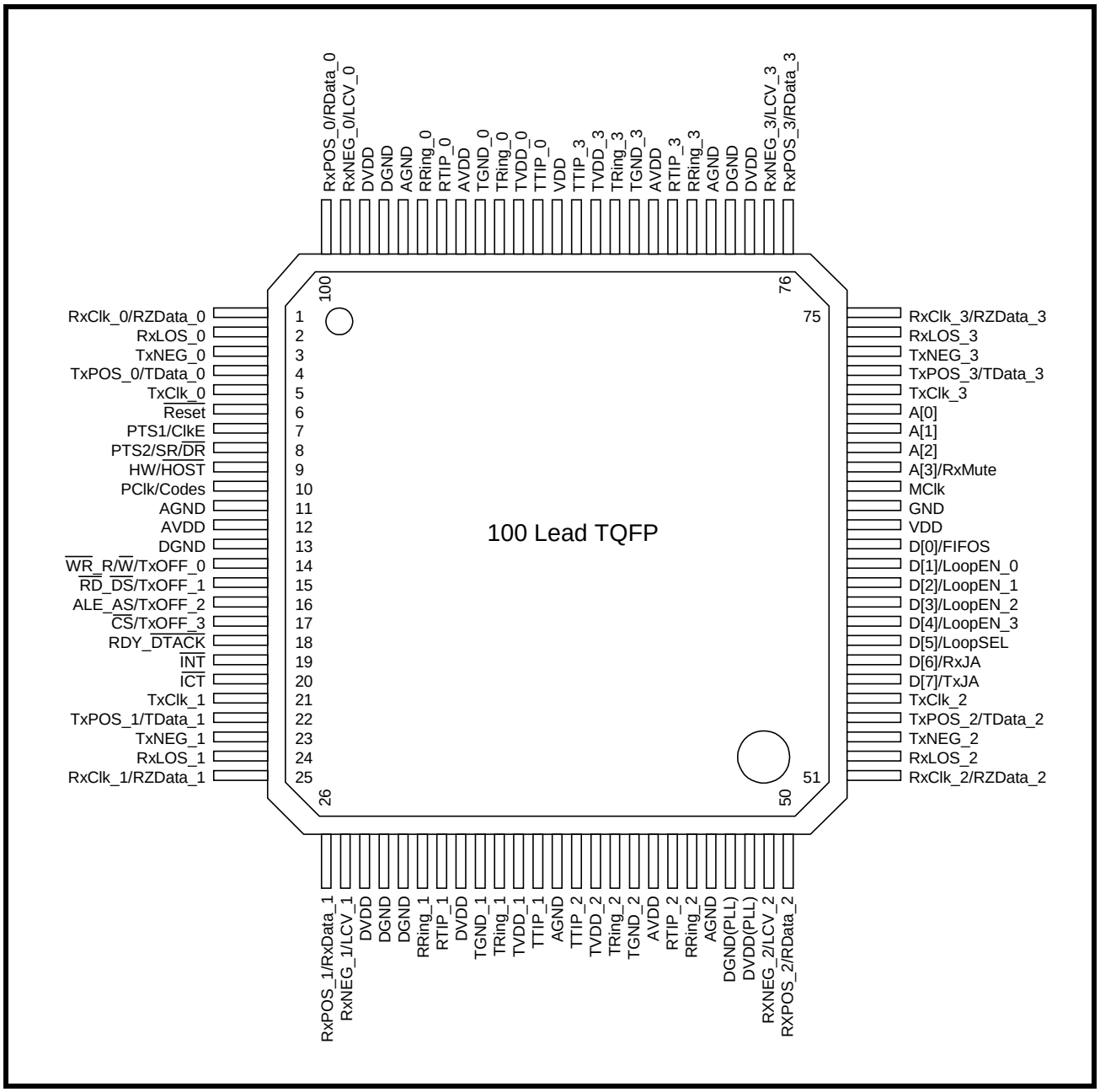


TABLE OF CONTENTS

PIN DESCRIPTION

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
RECEIVER SECTIONS			
1 25 51 75	**RxCLK_0/RZData_0** **RxCLK_1/RZData_1** **RxCLK_2/RZData_2** **RxCLK_3/RZData_3**	O	**Receiver_n Clock Output** **Rzdata Output:** In Data Slicer Mode, (register 0, bit 7 = 1) or in Hardware Mode when **MClk** is absent, this signal is OR-ed **RZdata** after the slicers.
2 24 52 74	**RxLOS_0** **RxLOS_1** **RxLOS_2** **RxLOS_3**	O	**Receiver_n Loss of Signal**. This signal is asserted "High" to indicate loss of signal at the receive input.
100 26 50 76	**RxPOS_0/RData_0** **RxPOS_1/RData_1** **RxPOS_2/RData_2** **RxPOS_3/RData_3**	O	**Receiver 1 Positive Data Output:** In dual-rail mode, this signal is the receive P-rail output data. **Receiver 1 NRZ Data Output:** In single-rail mode, this signal is the receive output data.
99 27 49 77	**RxNEG_0/LCV_0** **RxNEG_1/LCV_1** **RxNEG_2/LCV_2** **RxNEG_3/LCV_3**	O	**Receiver_n Negative Data Output:** In dual-rail mode, n-rail data are sent to the framer. **Line Code Violation Output - Channel_n:** In single-rail mode, this signal output "High" for one receive clock cycle to indicate a code violation is detected in the received data. If AMI coding is selected, every bipolar violation received will cause this pin to go "High".
95 31 45 81	**RRing_0** **RRing_1** **RRing_2** **RRing_3**	I	**Receiver_n Differential Negative Input.**
94 32 44 82	**RTIP_0** **RTIP_1** **RTIP_2** **RTIP_3**	I	**Receiver_n Differential Positive Input.**
67	**RXMUTE**	I	**Hardware Mode, Receive Muting**: Connect this pin "High" to mute RxPOS/RxNEG output to a low state upon receive LOS condition to prevent data chattering. Connect Low to disable muting function.
TRANSMITTER SECTIONS			
3 23 53 73	**TxNEG_0** **TxNEG_1** **TxNEG_2** **TxNEG_3**	I	**Transmitter_n Negative NRZ Data Input**. In dual-rail mode, this signal is the n-rail input data for transmitter 0. In single-rail mode, this pin can be left unconnected.
4 22 54 72	**TxPOS_0/TData_0** **TxPOS_1/TData_1** **TxPOS_2/TData_2** **TxPOS_3/TData_3**	I	**Transmitter_n Positive Data Input**. In dual-rail mode, this signal is the p-rail input data for transmitter 0. **Transmitter 0 Data Input**. In single-rail mode, this pin is used as the NRZ input data for transmitter 0.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
5 21 55 71	**TxClk_0** **TxClk_1** **TxClk_2** **TxClk_3**	I	**Transmitter_n Clock Input: E1 rate at 2.048MHz ± 50ppm.** During normal operation both in Host Mode and Hardware Mode, **TxClk** is used for sampling input data at **TxPOS/TData** and **TxNEG**, while **MCLK** is used as the timing reference for the transmit pulse shaping circuit. If **TxClk** is active while **MClk** is not present, **TxPOS** and **TxNEG** accepts NRZ data input and the transmit pulse width is determined by **TxClk** clock duty cycle. If **TxClk** is tied to "Low", **TxPOS** and **TxNEG** input accepts **RZ** data format and the pulse width is determined by the duty cycle of the input data. In **RZ** Mode, single-rail data format is not supported. **In Hardware Mode,** if TxClk is tied "High" for more than 10 µs, then TAOS (a continuous all one's AMI signal) will be transmitted to the line using **MCLK** as timing reference. If TxClk_0 is tied "Low" for more than 10 µs, the transmitter will be powered down and the output will be tri-stated.
14 15 16 17	**TxOFF_0** **TxOFF_1** **TxOFF_2** **TxOFF_3**	I	**Powered-down Transmitter_n:** In Hardware Mode, tie this pin "High" to power-down channel 0 transmitter and set TTIP_n and TRing_n to high impedance. ***NOTE:*** *Internally pulled -up with a 50kΩ resistor.*
91 35 41 85	**TRing_0** **TRing_1** **TRing_2** **TRing_3**	O	**Transmitter_n Ring Output:** Negative Differential data output to the line.
89 37 39 87	**TTIP_0** **TTIP_1** **TTIP_2** **TTIP_3**	O	**Transmitter_n Tip Output:** Positive Differential data output to the line.
MICROPROCESSOR INTERFACE			
6	**$\overline{\text{RESET}}$**	I	**Hardware Reset** (Active Low). When this pin is tied Low for more than 10µS, the device is put in the reset state. ***NOTE:*** *Internally pulled -up with a 50kΩ resistor.*
7	**PTS1**	I	**Processor Type Select bit 1:** **Host Mode** In Host Mode the appropriate bits are set in the command mode PTS1 / PTS2 / 0 0 8HC11,8081,80C188 (async.) / 1 0 Motorola 68K (async.) / 0 1 Intel x86 (sync.) / 1 1 Intel i906,Motorola 860 (sync.)
	ClkE	I	**Hardware Mode:** The state of the ClkE input controls the sampling edge of both TxClk and RxClk. A "1" selects the positive edge of TxClk and RxClk A "0" selects the negative edge of TxClk and RxClk.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
8	**PTS2** **SR/$\overline{DR}$**	I	**Host Mode:** **Processor Type Select Input bit 2:** See description for pin 7. **Hardware Mode** **Single rail/Dual Rail Control** Connect this pin “Low” to select transmit and receive data format in dual-rail mode. In this mode, HDB3 encoder and decoder are not available. Connect this pin "High" to select single-rail data format. ***NOTE:*** *Internally pulled -downwith a 50kΩ resistor.*
9	**HW/$\overline{HOST}$**	I	**Mode Control Input:** This pin is used to select the operating mode of the device, (Hardware Mode or Host Mode.) In **Hardware Mode**, the parallel Microprocessor interface is disabled and enables all hardware control pin functions. In **Host Mode**, the parallel microprocessor interface pins are used for control functions. **Pin 9** / **Operating Mode** “Low” / Host Mode “High” / Hardware Mode ***NOTE:*** *Internally pulled "High" with 50kΩ.*
10	**PCLK** **Codes**	I I	**Processor Clock Input**. Input clock for synchronous microprocessor operation. Maximum clock rate is 16 MHz. This pin is internally pulled-up for asynchronous microprocessor interface when no clock is present. **Coding/Decoding Select**. **In Hardware Mode**, if single-rail data format is selected (pin 8 =”1”), connect this pin "High" to select AMI encoding and decoding. Connect this pin Low to select HDB3.
14	**$\overline{WR}$_R/$\overline{W}$**	I	**Write Input (Read/Write)**. With Intel bus timing, a Low pulse on WR selects a write operation when $\overline{CS}$ pin is Low. When configured in Motorola bus timing, a "High" pulse on R/W selects a read operation and a Low pulse on R/$\overline{W}$ selects a write operation when $\overline{CS}$ is Low.
15	**$\overline{RD}$_$\overline{DS}$**	I	**Read Input (Data Strobe).** With Intel bus timing, a Low pulse on $\overline{RD}$ selects a read operation when CS pin is Low. When configured in Motorola bus timing, a Low pulse on DS indicates a read or write operation when $\overline{CS}$ pin is Low.
16	**ALE_AS**	I	**Address Latch Input (Address Strobe)**. With Intel bus timing, the address inputs are latched into the internal register on the falling edge of ALE. When configured in Motorola bus timing, the address inputs are latched into the internal register on the falling edge of AS.
17	**$\overline{CS}$**	I	**Chip Select Input**. This signal must be Low in order to access the parallel port.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
18	**RDY_$\overline{\text{DTACK}}$**	O	**Ready Output (Data Transfer Acknowledge Output)**. With Intel bus timing, RDY is asserted "High" to indicate the device has completed a read or write operation. When configured in Motorola bus timing, DTACK is asserted Low to indicate the device has completed a read or write cycle.
67 68 69 70	**A[3]** **A[2]** **A[1]** **A[0]**	I	**Host Mode, Microprocessor Interface Address Bus [3]** **Host Mode, Microprocessor Interface Address Bus [2]** **Host Mode, Microprocessor Interface Address Bus [1]** **Host Mode, Microprocessor Interface Address Bus [0].**
56 57 58 59 60 61 62 63	**D[7]** **D[6]** **D[5]** **D[4]** **D[3]** **D[2]** **D[1]** **D[0]**	I/O	**Data Bus[7:0]**. Microprocessor read/write data bus pins.
CLOCKS			
66	**MCLK**	I	**Master Clock Input**. This signal is an independent 2.048MHz clock with accuracy better than ±50ppm and duty cycle within 40% to 60%. The function of MCLK is to provide internal timing for the PLL clock recovery circuit, jitter attenuator block, reference clock during transmit all ones data and timing reference for the microprocessor in Host Mode operation. If **MClk** is absent, all receive channels perform as analog front-end (AFE). The OR-ed **RZ** data is also available at **RxClk** output in this mode, instead. The clock recovery function is disabled.
JITTER ATTENUATOR			
56	**TXJA**	I	**Transmit Jitter Attenuator Select**. In Hardware Mode, connect this pin “High” to select jitter attenuator in the transmit path and connect Low to disable jitter attenuator. Setting RXJA simultaneously "High" also disables jitter attenuator selection.
57	**RXJA**	I	**Receive Jitter Attenuator Select**. In Hardware Mode, connect this pin “High” to select jitter attenuator in the receive path and connect Low to disable jitter attenuator. Setting TXJA simultaneously "High" also disables jitter attenuator selection.
CONTROL			
8	**SR/$\overline{\text{DR}}$**	I	**Single rail/Dual Rail Control:** **Hardware Mode** Connect this pin “Low” to select transmit and receive data format in dual-rail mode. In this mode, HDB3 encoder and decoder are not available. Connect this pin "High" to select single-rail data format. ***NOTE:*** *Internally pulled -down with a 50kΩ resistor.*
10	**Codes**	I	**Coding/Decoding Select**. **In Hardware Mode**, if single-rail data format is selected (pin 8 =”1”), connect this pin "High" to select AMI encoding and decoding. Connect this pin Low to select HDB3.

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
19	**$\overline{\text{INT}}$**	O	**Interrupt Output**. This pin is asserted Low to indicate an alarm condition has occurred within the device. Interrupt generation can be globally disabled by setting the GIE bit to a "0" in the command control register. ***NOTE:*** *This pin is an open drain output and requires an external 10KΩ pull-up resistor.*
20	**$\overline{\text{ICT}}$**	I	**In-Circuit Testing (Active Low)**. When this pin is tied Low, all output pins are forced to high impedance state for in-circuit testing. ***NOTE:*** *Internally pulled -up with 50kΩ.*
58	**LOOPSEL**	I	**DLoop-back Mode Select**. In Hardware Mode, if LOOPEN_(0-3) is “High”, this pin is used for selecting loop-back mode. Connect this pin "High" to select local loop-back and Low to select remote loop-back. Digital Loop-back is not supported in Hardware Mode.
62 61 60 59	**LOOPEN_0** **LOOPEN_1** **LOOPEN_2** **LOOPEN_3**	I	**Loop-back Enable - Channel_n:** **In Hardware Mode**: Connect this pin “High” to enable channel_n loop-back operation. Remote or local loop-back is determined by pin 58 setting.
63	**FIFOS**	I	**FIFO Size Select.** In Hardware Mode, connect this pin "High" selects 64 bit FIFO depth and connect Low to select 32 bit FIFO depth.
POWER SUPPLIES AND GROUNDS			
12	**AVDD**	****	**Analog Positive Supply(3.3V± 5%)**
28	**DVDD**	****	**Digital Positive Supply(3.3V± 5%)**
33	**DVDD**	****	**Digital Positive Supply(3.3V± 5%)**
90 36 40 86	**TVDD_0** **TVDD_1** **TVDD_2** **TVDD_3**	****	**Transmitter_n Analog Positive Supply(3.3V± 5%).**
43	**AVDD**	****	**Analog Positive Supply(3.3V± 5%)**
48	**DVDD**	****	**Digital Positive Supply(3.3V± 5%)**
64	**DVDD**	****	**Digital Positive Supply(3.3V± 5%)**
78	**DVDD**	****	**Digital Positive Supply(3.3V± 5%)**
11	**AGND**	****	**Analog Ground**
13	**DGND**	****	**Digital Ground**
29	**DGND**	****	**Digital Ground**
30	**DGND**	****	**Digital Ground**
92 34 42 84	**TGND_0** **TGND_1** **TGND_2** **TGND_3**	****	**Transmitter_n Analog Ground.**

PIN DESCRIPTIONS

PIN #	NAME	TYPE	DESCRIPTION
38	**AGND**	****	**Analog Ground**
46	**AGND**	****	**Analog Ground**
47	**DGND**	****	**Digital Ground**
65	**DGND**	****	**Digital Ground**
79	**DGND**	****	**Digital Ground**
80	**AGND**	****	**Analog Ground**
83	**AVDD**	****	**Analog Positive Supply(3.3V± 5%)**
88	**AVDD**	****	**Analog Positive Supply(3.3V± 5%)**
93	**AVDD**	****	**Analog Positive Supply(3.3V± 5%)**
96	**AGND**	****	**Analog Ground**
97	**DGND**	****	**Digital Ground**
98	**DVDD**	****	**Digital Positive Supply(3.3V± 5%)**

SYSTEM-FUNCTIONAL DESCRIPTION

A simplified single channel block diagram of the XRT 82L24A is presented in Figure 1. The XRT 82L24A consists of four identical transmit and receive channels for E1(2.048 Mbps) PCM systems. The operational mode of each channel of the line interface can be configured by the microprocessor interface (Host Mode) or by Hardware control.

RECEIVER

At the receiver input, cable attenuated AMI signals can be coupled to the receiver using a capacitor or a 1:2 transformer. The receive signal first goes through the equalizer for signal conditioning before being applied to the data recovery circuit. The data recovery circuit includes a peak detector which is set typically at 50% for E1 of the equalizer output peak amplitude for data slicing. After the data slicers, the digital representation of the AMI signals goes to the clock recovery circuit for timing recovery and subsequently to the HDB3 decoder (if selected) before they are output via the RxPOS/RDATA and RxNEG/LCV pins. The digital data output can be in dual-rail or single-rail mode depending on the option selected. Clock and timing recovery is accomplished by means of a digital PLL scheme which can tolerate high input jitter and meets or exceeds the jitter tolerance requirements as specified in the ITU - G.823 standard.

JITTER ATTENUATOR

To reduce jitter in the transmit line signal or recovered clock and data signals, a crystal-less jitter attenuator with a 32x2 bit or 64x2 bit FIFO is provided for each channel. The jitter attenuator can be configured to operate in either the transmit or receive path, or it can be disabled through Host or Hardware Mode control. The jitter attenuator design is based on a digital scheme that uses the MCLK signal as a reference input. No other high frequency clock is necessary. With the jitter attenuator selected, the typical throughput delay is 16 bits for a 32 bit FIFO depth or 32 bit for a 64 bit FIFO depth. The design of the jitter attenuator is such that if the write and read pointers of the FIFO are within two bits of overflowing or underflowing, the bandwidth of the jitter attenuator is automatically widened in order to permit the “Jitter Attenuator” PLL to track the short term input jitter to avoid data corruption. When this situation occurs, the jitter attenuator will not attenuate input jitter until the read/write pointer's position is outside the two bit window. Under normal condition, the jitter transfer characteristic meets the narrow bandwidth requirement as specified in ITU- G.736 and ITU- I.431standards.

GAPPED CLOCK (JA MUST BE ENABLED IN THE TRANSMIT PATH)

The XRT82L24A LIU is ideal for multiplexer or mapper applications where the network data crosses multiple timing domains. As the higher data rates are de-multiplexed down to T1 or E1 data, stuffing bits are removed which can leave gaps in the incoming data stream. If the jitter attenuator is enabled in the transmit path, the 32-Bit or 64-Bit FIFO is used to smooth the gapped clock into a steady T1 or E1 output. The maximum gap width of the XRT82L24A is shown in Table 1.

TABLE 1: MAXIMUM GAP WIDTH FOR MULTIPLEXER/MAPPER APPLICATIONS

FIFO DEPTH	MAXIMUM GAP WIDTH
32-Bit	20 UI
64-Bit	50 UI

NOTE: *If the LIU is used in a loop timing system, the jitter attenuator should be enabled in the receive path.*

HDB3/AMI DECODER

The decoder function is only active if the chip has been configured to operate in the single-rail mode. When the single-rail mode is selected, the receive line signal will be decoded according to HDB3 rules for E1. Further, any bipolar violation of the HDB3 line coding scheme will be flagged as a Line Code Violation via the LCV output pin. The LCV output pin will be pulsed high for one RxClk cycle for each line code violation that is detected. Excessive number of zeros in the receive data stream are also flagged as a line code violation via the same output pin. If AMI decoding is selected in single-rail mode operation, every bipolar violation in the receive data stream is reported as error at the LCV pin.

RECEIVER LOSS OF SIGNAL (LOS)

The receiver loss of signal monitoring function is implemented using both analog and digital detection schemes compatible with ITU G.775 requirements. When the amplitude of the E1line signal at RTIP/RRING drops 16dB (typical) below the 0dB nominal level the digital circuit is activated to parse through and check for 32 consecutive zeros before LOS is asserted, to indicate loss of input signal. The number of

consecutive zeros before LOS is declared can be increased to 4096 bits. During extended LOS Mode, the LOS condition will be cleared when 4096 more valid data bits are present (when operating in the Host Mode). The LOS condition is cleared when the input signal rises above 16dB below 0dB nominal level and meets 12.5% density of 4 ones in a 32 bit window with no more than 16 consecutive zeros.

Clock signals generated when LOS is declared

The output signal at the RxClk output pin depends upon the type of LOS condition that is occurring.

Complete Loss of Signal (Zero Amplitude)

If the XRT 82L24A experiences a complete Loss of Signal (e.g., no signal amplitude), then the XRT 82L24A Clock Recovery PLL enters the Training Mode, and Differentially begins to lock onto the signal applied to the MCLK input pin. As a consequence, the Clock Recovery PLL will begin to drive a clock signal to the Terminal Equipment (via the RxClk output pin), which is derived from the MCLK input pin.

Degraded Type of Loss of Signal Event (Non-Zero Amplitude)

If the XRT 82L24A experiences a degraded type of LOS event (e.g., where there is still a small amount of discernible signal amplitude in the line signal, but small enough to qualify as an LOS event) then the Clock Recovery PLL could lock onto this degraded line signal and will subsequently drive the same frequency via the RxClk output pins.

CONDITIONS FOR DECLARING AND CLEARING LOS IN THE E1 MODE.

Each E1 channel of the XRT 82L24A has two criteria for LOS Detection, **Analog** and **Digital**. A channel will declare a LOS condition when both of these LOS Detectors detect an LOS condition.

Analog LOS Detector

The Analog LOS Detector will declare an LOS condition, if it determines that the amplitude of the incoming line signal has dropped to less than -15dB (below the nominal pulse amplitude of 3V for **twisted-pair**, or 2.37V for **coaxial-cable**) for at least 32 bit-periods.

The Analog LOS Detector will clear the LOS condition, if it determines that the incoming line signal is no more than 12.5dB below the nominal 3V pulse amplitude.

NOTE: *The difference in the signal level required to declare and clear LOS is 2.5dB. This 2.5dB hysteresis is designed into the Analog LOS Detector circuitry, in order to prevent chattering in the LOS output pin or bit-field.*

Digital LOS Detector

The Digital LOS Detector will declare an LOS condition, if it detects a string of at least 32 consecutive "0"s.

The Digital LOS Detector will clear the LOS condition, if it determines that the incoming E1 line signal has a pulse density of 12.5% or more without 16 consecutive “0’s” for at least 32 consecutive bit periods.

NOTE: *The pulse density requirement of 12.5% accounts for HDB3 coding.*

RECEIVE DATA MUTING

The XRT 82L24A permits the user to “MUTE” the recovered data output signals anytime the LOS condition is declared. If the user invokes this function, then the RPOS/RDAT and RNEG output pins will be pulled to GND for the duration that the LOS condition exists. This feature is useful in that it prevents the LIU from routing electrical noise (which has been “recovered” by the Clock Recovery PLL) to the Framer IC and preventing it from declaring an LOS condition. This feature is enabled by setting the RXMUTE bit to a “1” in the Host Mode (Register 1, Bit 2 Location) or by connecting pin 67 High in the Hardware Mode.

LOOP-BACK MODES

Each channel within the XRT 82L24A can be configured to operate in any of the following loop-back modes:

- Remote Loop-Back Mode
- Digital Local Loop-Back Mode
- Analog Local Loop-Back Mode

Each of these loop-back modes are described in some detail below.

REMOTE LOOP-BACK (RLOOP) MODE

With Remote Loop-Back activated, (Channel Control Register bit 2 = “1”) in Host Mode or in Hardware Mode with **LoopSEL** (pin 58) tied Low and **LoopEN** tied High received data after the jitter attenuator (if selected) is looped back to the transmit path using RxClk as transmit timing. In this mode the data/signals applied to the TxClk, TPOS/TDAT and TNEG input pins are ignored, while RxClk and received data will continue to be available at their respective output pins. Simultaneously setting RLOOP and ALOOP active is not allowed (see Loop-Back Mode in Figure 4 & Figure 5). Remote loop-back has priority over TAOS.

DIGITAL LOCAL LOOP-BACK (DLOOP) MODE

The Digital Local Loop-Back mode allows the transmit clock and data to be looped back to the corresponding receiver output pins through the encoder/decoder and the jitter attenuator. In this mode, the receive line signal is ignored, but the transmit data will

be sent to the line uninterrupted. This loop back feature allows users to configure the line interface as a pure jitter attenuator. (see Loop-Back Mode in Figure 6 & Figure 7).

NOTE: *Digital Local Loop-Back is not supported in Hardware Mode.*

ANALOG LOCAL LOOP-BACK (ALOOP) MODE

With Analog Local Loop-Back activated, the transmit data at TTIP and TRING are looped-back to the analog input of the receiver. External inputs at RTIP/RRING in this mode are ignored while valid transmit data continues to be sent to the line. Analog Loop-Back exercises most of the functional blocks of the line interface (see Loop-Back Mode in Figure 8 & Figure 9).

FIGURE 4. REMOTE LOOP-BACK WITH JITTER ATTENUATOR SELECTED IN RECEIVE PATH

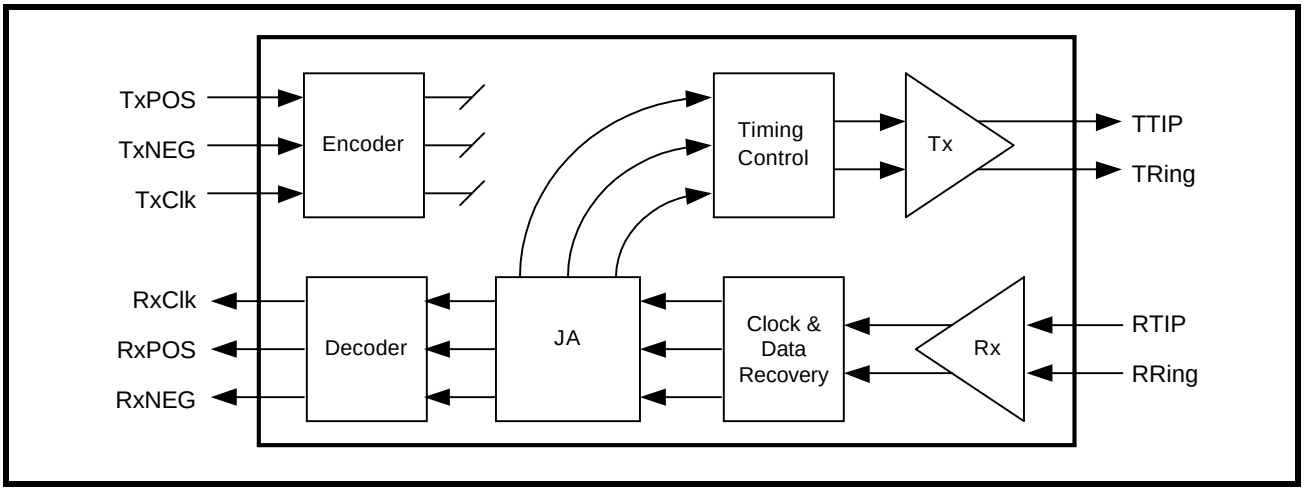


FIGURE 5. REMOTE LOOP-BACK WITH JITTER ATTENUATOR SELECTED IN TRANSMIT PATH

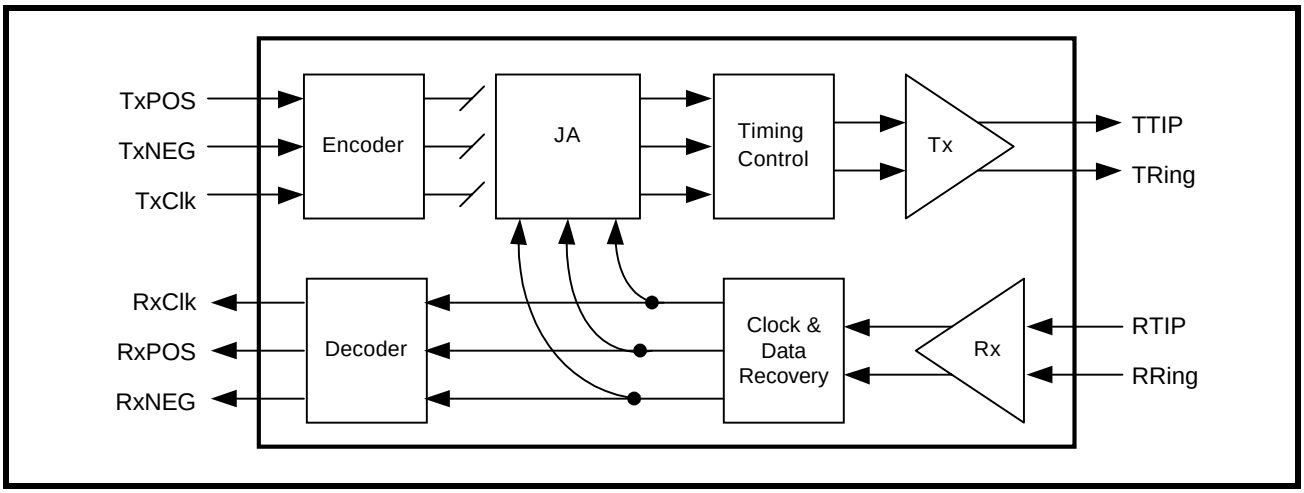


FIGURE 6. DIGITAL LOCAL LOOP-BACK WITH OPTION TO TRANSMIT ALL "ONES" TO THE LINE (JA SELECTED & IN RECEIVE PATH)

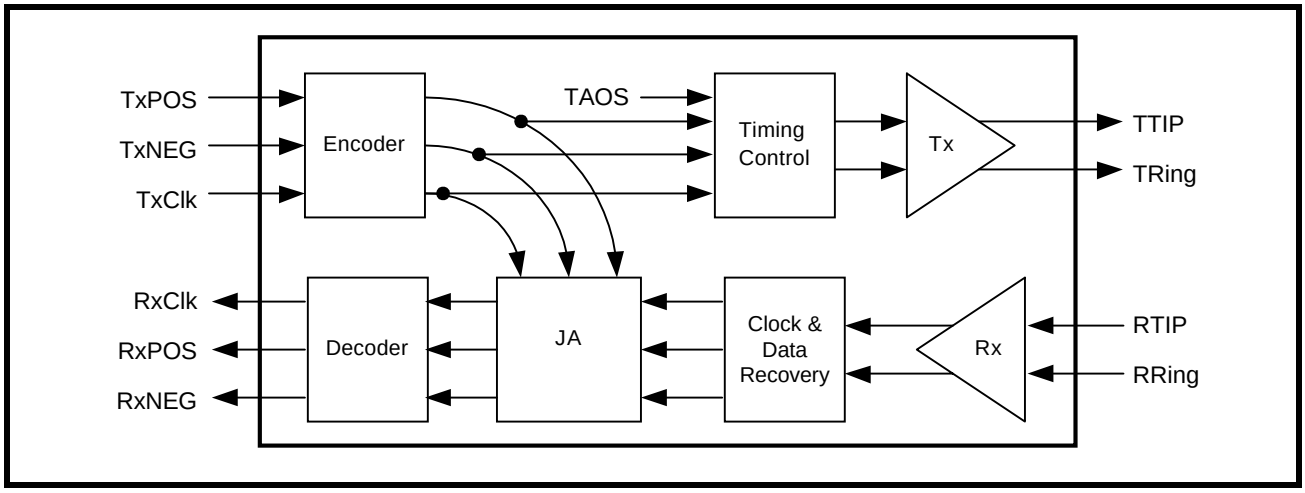


FIGURE 7. DIGITAL LOCAL LOOP-BACK WITH OPTION TO TRANSMIT ALL "ONES" TO THE LINE (JA SELECTED & IN TRANSMIT PATH)

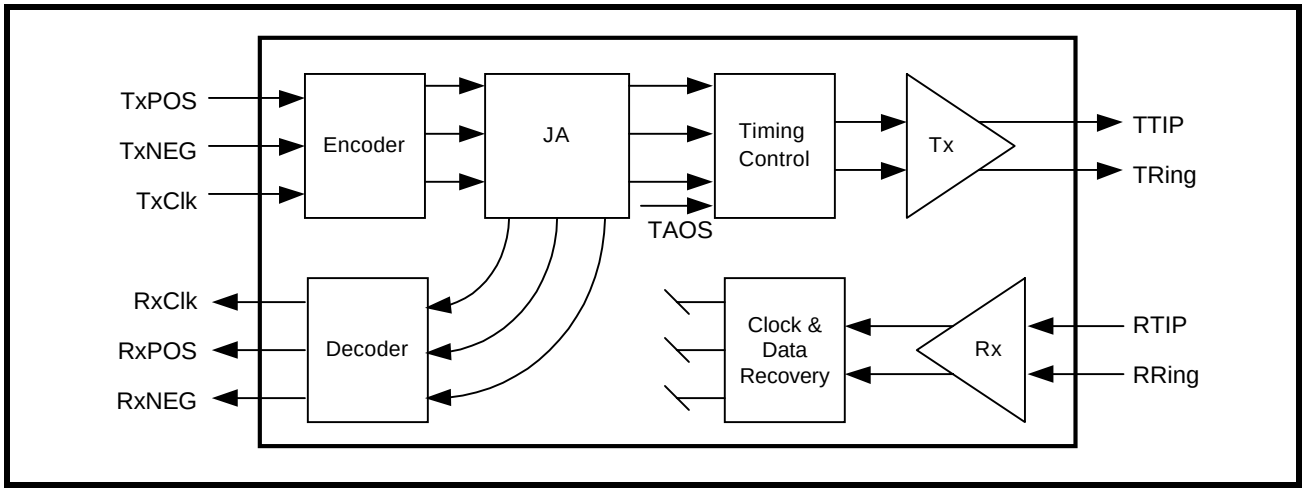


FIGURE 8. ANALOG LOCAL LOOP-BACK SIGNAL FLOW JITTER ATTENUATOR SELECTED & IN RECEIVE PATH

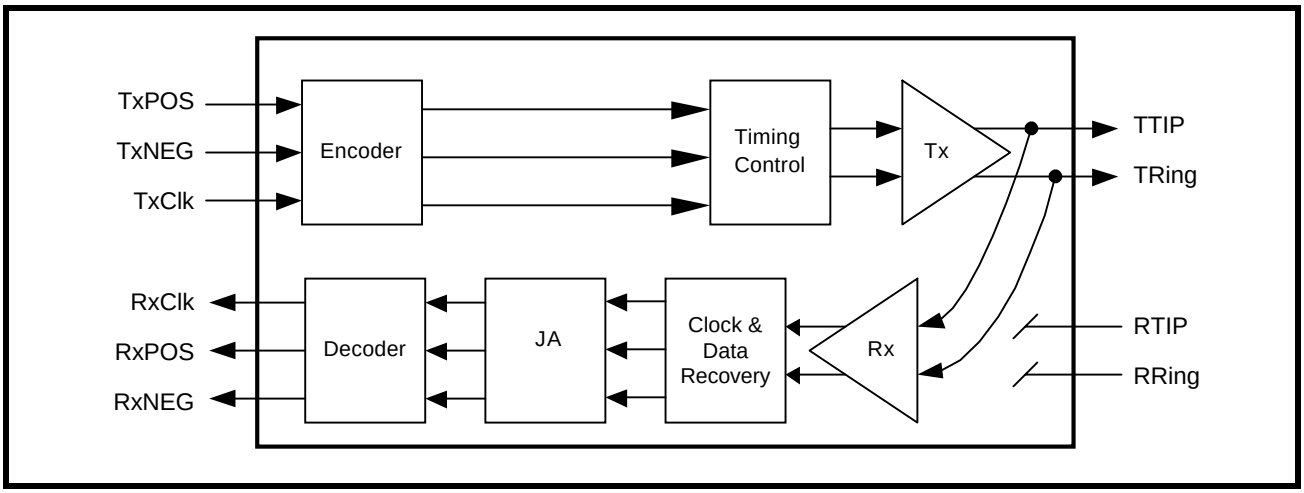
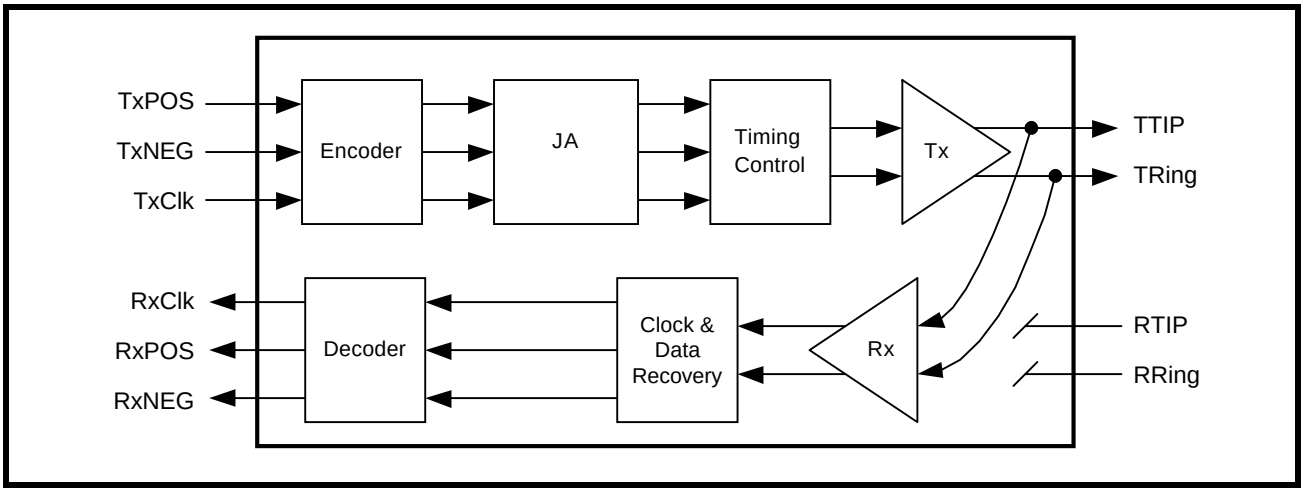


FIGURE 9. ANALOG LOCAL LOOP-BACK SIGNAL FLOW JITTER ATTENUATOR SELECTED & IN TRANSMIT PATH



RESET OPERATION

The XRT 82L24A provides both Hardware and Software resets. In Hardware reset, with pin 6 forced to "0" for more than 10µs, the entire state of the device including the microprocessor R/$\overline{W}$ registers are reset. In Software reset, only the state of the interface is reset (the microprocessor registers are not affected).

RECEIVER MODES OF OPERATION

Through the microprocessor interface or in Hardware Mode, XRT 82L24A offers several alternative receive modes of operation making it flexible for different applications as dictated by the system requirements.

RECEIVE DATA INVERT MODE

Receive output data by default is active high at RxPOS/RDATA and RxNEG/LCV pins. These signals can be changed to active Low by setting the DATAP bit in the interface register(Register 1, Bit 3 = “1”). In single rail mode DATAP = “1”, (Register 0, Bit 7 = “1”), LCV output also becomes active Low. Data invert Mode is only available in Host Mode.

FIGURE 10. DATA CHANGES ON RISING EDGE OF CLK AND DATA IS SAMPLED ON FALLING EDGE

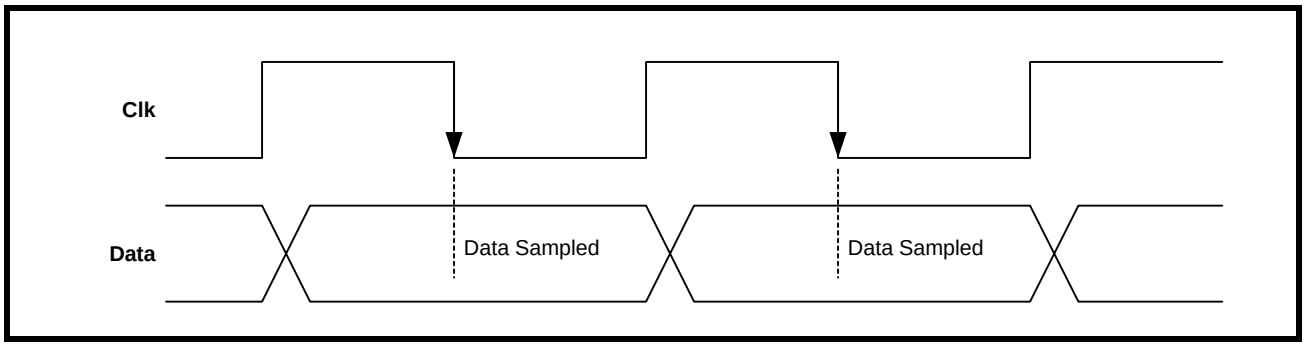
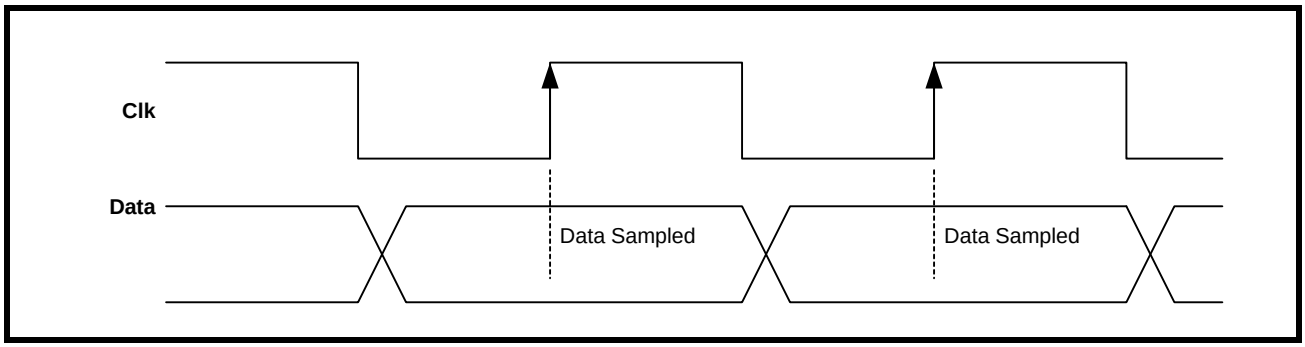


FIGURE 11. DATA CHANGES ON FALLING EDGE OF CLK AND IS SAMPLED ON RISING EDGE



RxClk Clock Sampling Edge

The sampling edge of the RxClk output can be changed through control bit RClkE within the interface register for receive output data re-timing. With RClkE="1", (Bit 5 = "1"), data is validated on the rising edge of RxClk and with RClkE="0", (Bit 5 = "0"),, receive data is validated on the falling edge of RxClk. In Hardware Mode, the state of pin 7 (ClkE) controls the rising or falling edge of RxClk for data re-timing.

TRANSMIT CLOCK SAMPLING EDGE

NRZ Transmit data at TxPOS/TDATA or TxNEG is clocked serially into the device using TxClk. With the interface register bit 4 (TClkE="1"), input data is sampled on the rising edge of TxClk. The sampling edge is inverted when TClkE= "0". In Hardware Mode, the state of pin 7 (ClkE) controls the sampling edge of both TxClk and RxClk.

SINGLE RAIL, DUAL RAIL

Transmit data format can be in dual-rail (SR/$\overline{DR}$=1) or single-rail modes (SR/$\overline{DR}$=0). In Hardware Mode, dual or single-rail format is determined by the state of pin 8. For single-rail mode operation, NRZ data can be applied to TxPOS/TDATA with TxClk, while TxNEG input is left unconnected. The transmitter converts NRZ input data into differential signal for transmission to the line using low impedance output drivers.

TRANSMIT ALL ONES (TAOS)

In the Host Mode, individual channels can be programmed to transmit an all "Ones" AMI signal by setting the per channel bit control TAOS=1. In this mode, input data at TxPOS/TDATA and TxNEG are ignored. In Host Mode, reference clock for TAOS is TxClk. If TxClk is not available, MCLK is used for transmission. In Hardware Mode, if TxClk is not present and High for more than 10µs, TAOS is transmitted using MCLK as a reference. Remote Loop-Back has priority over TAOS request.

HDB3/AMI ENCODER

The encoder is only available in single-rail mode (SR/$\overline{DR}$=1) in Host Mode, or pin 8 set High in Hardware Mode. In an E1 system, if interface register CODES=0, HDB3 encoding is selected. Input data applied to TxPOS/TDATA which contains more than four consecutive zeros will be removed and replaced by "000V" or "B00V", where "B" indicates a pulse conforming with bipolar rule and "V" represents a pulse violating the rule. With register CODES="1", AMI coding is selected. In Hardware Mode, HDB3 or AMI coding selection is determined by the state of pin 10.

The choice of these codes is made such that an odd number of “B” pulses is transmitted between consecutive bipolar violation “V” pulses

TRANSMIT PULSE SHAPER

The transmit pulse shaper uses high a speed clock derived from MCLK to synthesize the shape and width of the transmitted pulse applied to TTIP and TRING. The internal high speed timing generator eliminates the need for a tightly controlled transmit clock TxClk duty cycle.

The intrinsic jitter at the transmit output using a jitter-free input clock source and with the jitter attenuator disabled will generate no more than 0.03UIpp.

DRIVER MONITOR

The driver monitor circuit is used for detecting transmit driver failure by monitoring the activity at TTIP and TRING. Driver failure may be caused by a short-circuit in the primary of the transformer or system problems at the input.

In the Host Mode, when the driver monitor detects no transitions at TTIP and TRING for more than 128 clock cycles, the DMO bit (bit 7) in the interface register is set and results in an interrupt ($\overline{INT}$) to be generated. Driver monitor function is not supported in Hardware Mode.

TxPOS/TDATA and TxNEG Polarity

In HOST Mode, transmit data at TxPOS/TDATA and TxNEG can be configured for active Low or active High operation, by controlling the state of the DATAP bit in the interface register. Writing a "0" to this bit selects active High data and a "1" selects active Low data. This control bit also selects receive output data polarity (see Receive Data Invert Mode description). This feature is not supported in Hardware Mode.

TRANSMIT OFF CONTROL

Each transmit channel of the line interface can be shut down by writing a "1" to TxOFF in the channel control interface register. In the “Transmitter off” mode, the entire transmitter is disabled and the outputs at TTIP and TRING are placed in a high impedance state. In Hardware Mode, pins 14 through pin 17 are used for powering down each transmit channel independently.

INTERFACING THE XRT 82L24A TO THE LINE

The XRT 82L24A in E1 configuration can be transformer coupled to 75Ω coaxial or 120Ω twisted pair lines as shown in Figure 12 and Figure 13 below.

FIGURE 12. XRT 82L24A CHANNEL 1IN AN E1 UNBALANCED 75 Ω APPLICATION

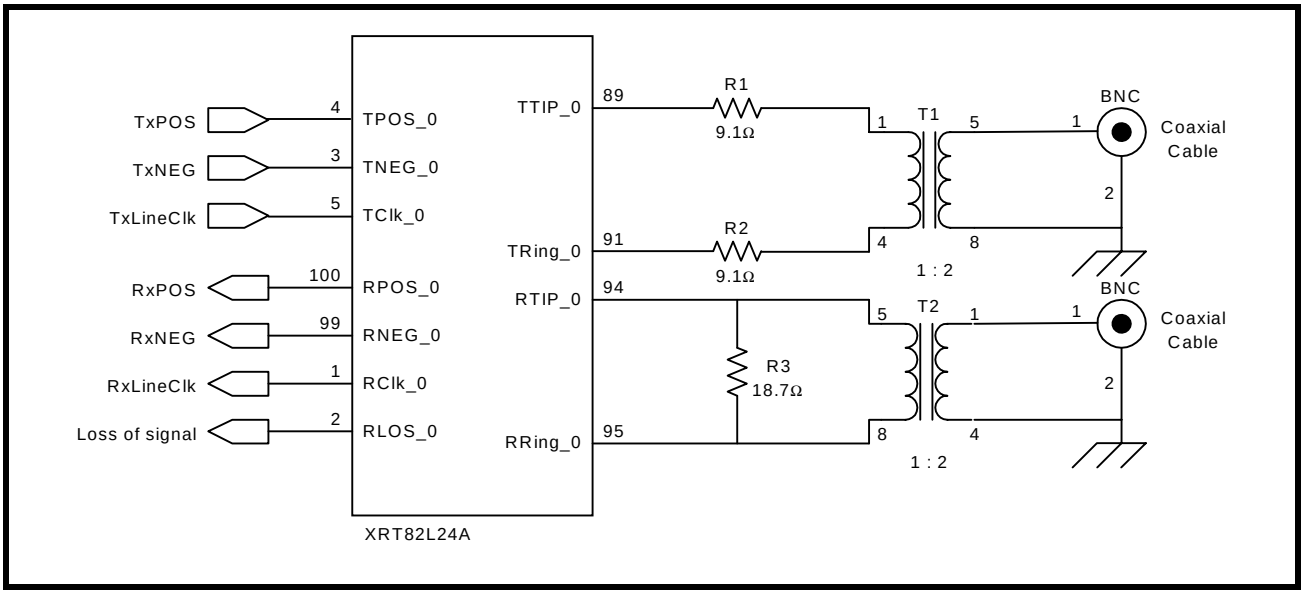


FIGURE 13. XRT 82L24A CHANNEL 1 - E1 120 Ω BALANCED APPLICATION

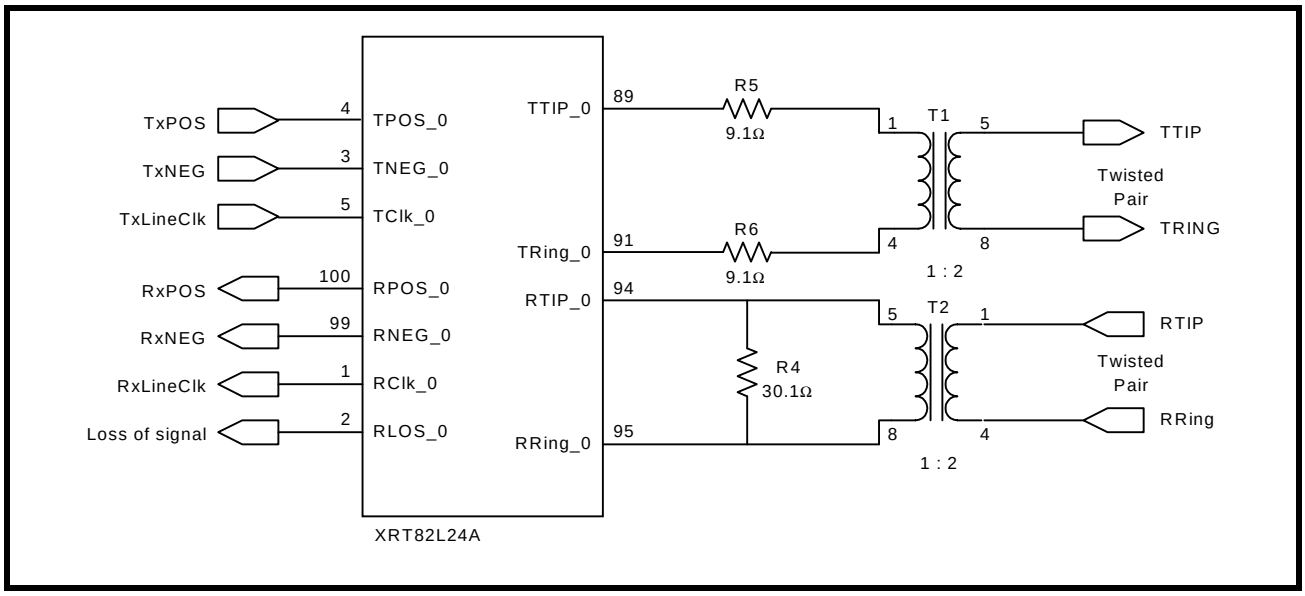


TABLE 2: E1 RECEIVER ELECTRICAL CHARACTERISTICS

(Vdd=3.3V±5%, Ta=-40°C to 85°C unless otherwise specified)

PARAMETER	MIN	TYP.	MAX	UNIT	TEST CONDITIONS
Receiver loss of signal:					
Number of consecutive zeros before LOS is set	-	32	-	bit	Cable attenuation @1024KHz ITU-G.775, ETS1 300 233
Input signal level at LOS	15	20	-	dB	
LOS De-asserted	12.5	-	-	% ones	
Receiver Sensitivity	11	13	-	dB	With nominal pulse amplitude of 3.0V for 120Ω and 2.37V for 75Ω application. With -18dB interference signal added.
Interference Margin	-18	-14	-	dB	With 6dB cable loss
Input Impedance	15		-	KΩ	
Jitter Tolerance: 20 Hz 700KHz 10KHz---100KHz	 10 5 0.3	 - -	 - -	 UIpp	ITU G.823
Recovered Clock Jitter Transfer Corner Frequency Peaking Amplitude	-	36	- 0.5	KHz dB	ITU G.736
Jitter Attenuator Corner Frequency(-3dB curve)	-	10	-	Hz	ITU G.736
Return Loss: 51KHz --- 102KHz 102KHz --- 2048KHz 2048KHz --- 3072KHz	 14 20 16	 - - -	 - - -	 dB dB dB	ITU G.703

TABLE 3: E1 TRANSMITTER ELECTRICAL CHARACTERISTICS

(Ta=-40°C to 85°C, Vdd=3.3V±5%, unless otherwise specified)

PARAMETER	MIN	TYP.	MAX	UNIT	TEST CONDITIONS
AMI Output Pulse Amplitude: 75Ω Application 120Ω Application	 2.13 2.70	 2.37 3.0	 2.60 3.30	 V V	Use transformer with 1:2 ratio and 9.1Ω resistor in series with each end of primary.
Output Pulse Width	224	244	264	ns	
Output Pulse Width Ratio	0.95	-	1.05	-	ITU-G.703
Output Pulse Amplitude Ratio	0.95	-	1.05	-	ITU-G.703
Jitter Added by the Transmitter Output	-	0.025	0.05	UIpp	Broad Band with jitter free TxClk applied to the input.
Return Loss: 51KHz --- 102KHz 102KHz --- 2048KHz 2048KHz --- 3072KHz	 8 14 10	 - - -	 - - -	 dB dB dB	ETSI 300 166

TABLE 4: TRANSMIT PULSE MASK SPECIFICATION

Test Load Impedance	75 Ω resistive (Coax)	120 Ω resistive (Twisted Pair)
Nominal peak voltage of a mark	2.37V	3.0V
Peak voltage of a space (no mark)	0 ± 0.237V	0± 0.3V
Nominal pulse width	244ns	244ns
Ratio of positive and negative pulses imbalance	0.95 to 1.05	0.95 to 1.05

FIGURE 14. ITU G.703 E1 PULSE TEMPLATE

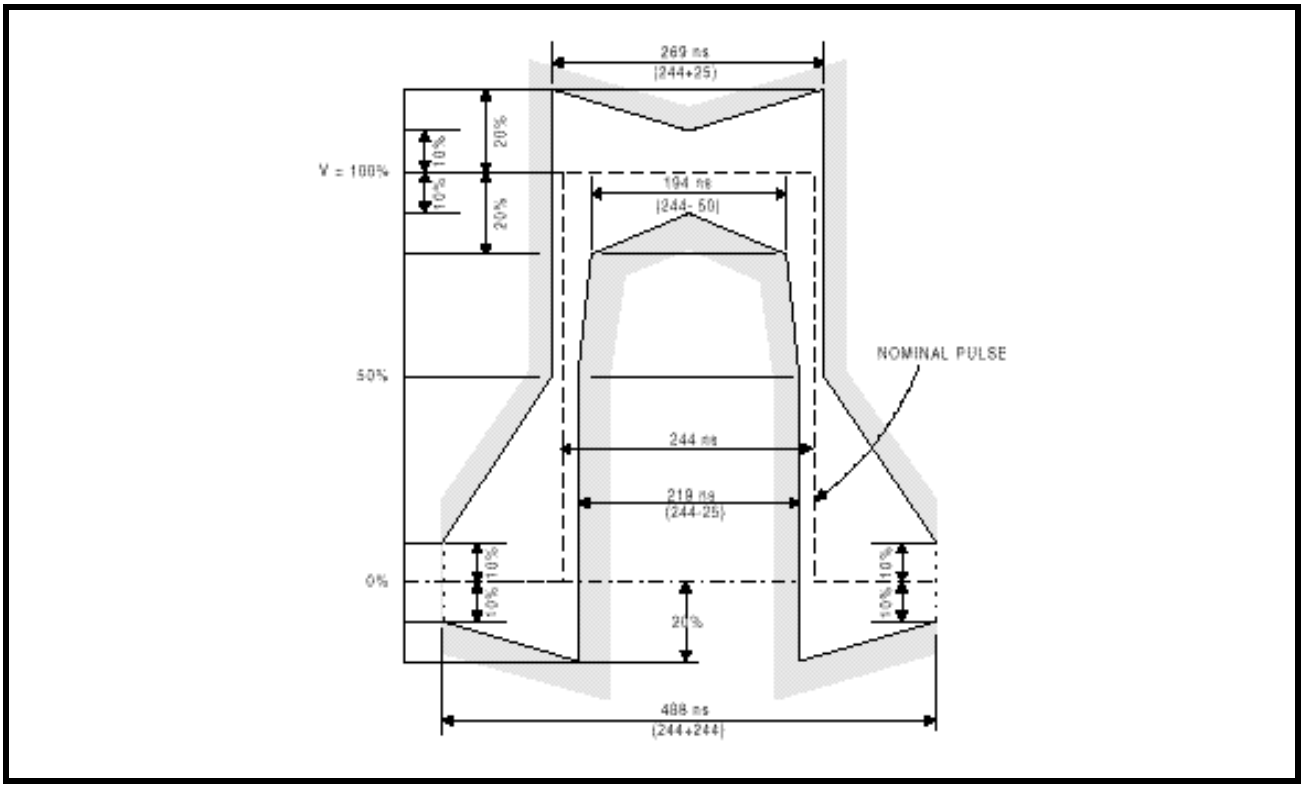


TABLE 5: DC ELECTRICAL CHARACTERISTICS

(Vdd=3.3V±5%, Ta=25°C unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP.	MAX	UNITS
Power Supply Voltage	Vdd	3.13	3.3	3.46	V
Input High Voltage	V_{IH}	2.0	-	5.0	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Output High Voltage @ IOH=-5mA	V_{OH}	2.4	-	-	V
Output Low Voltage @IOL=5mA	V_{OL}	-	-	0.4	V
Input Leakage Current (except Input pins with Pull-up resistor.)	I_L	-	-	± 10	µA
Input Capacitance	C_I	-	5.0	-	pF
Output Load Capacitance	C_L	-	-	25	pF

TABLE 6: POWER CONSUMPTION (TA=-40°C TO 85°C, VDD=3.3V ± 5%, UNLESS OTHERWISE SPECIFIED.)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Power Consumption	PC	-	450	650	mW	E1(75 Ohm) load. At 50% Mark Density
Power Consumption	PC	-	650	680	mW	E1(75 Ohm) load. At 100% Mark Density
Power Consumption	PC	-	400	500	mW	E1(120 Ohm) load. At 50% Mark Density
Power Consumption	PC	-	540	600	mW	E1(120 Ohm) load. At 100% Mark Density
Power Consumption	PC	-	80	100	mW	All Transmitters Powered-Down

ABSOLUTE MAXIMUM RATINGS

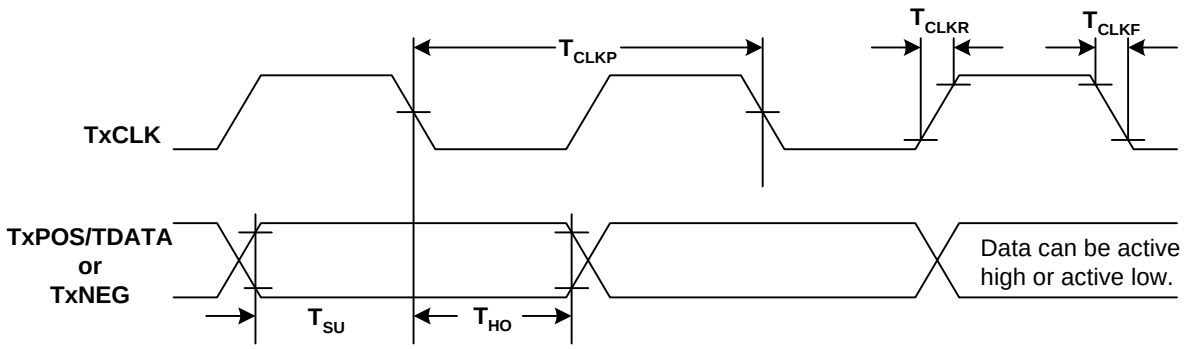
Storage Temperature	-65°C to + 150°C
Operating Temperature	-40°C to + 85°C
Supply Voltage	-0.5V to + 6.0V
Theta-JA	38° C/W
Theta-JC	6° C/W

TABLE 7: AC ELECTRICAL CHARACTERISTICS

(Vdd=3.3V±5%, Ta=25°C unless otherwise specified)

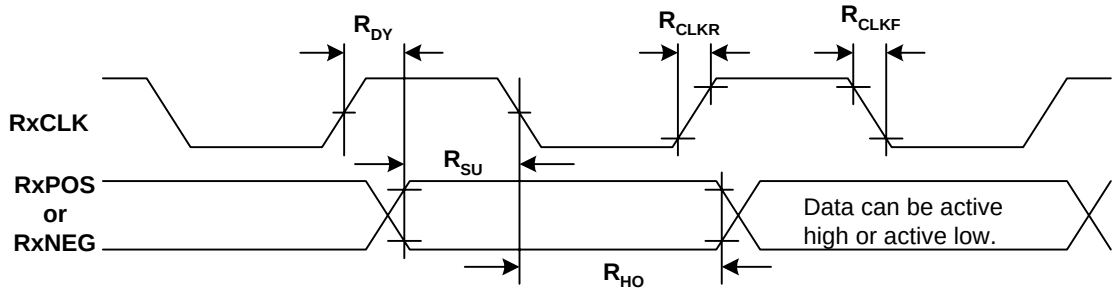
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
E1 MCLK Clock Frequency		-	2.048	-	MHz
MCLK Clock Duty Cycle		40	-	60	%
MCLK Clock Tolerance		-	±50	-	ppm
E1 TxClk Clock Period	T_{CLKP}	-	488	-	ns
TxClk Duty Cycle	T_{CDU}	30	50	70	%
Transmit Data Setup Time	T_{SU}	50	-	-	ns
Transmit Data Hold Time	T_{HO}	30	-	-	ns
TxClk Rise Time (10%/90%)	T_{CLKR}	-	-	40	ns
TxClk Fall Time (90%/10%)	T_{CLKF}	-	-	40	ns
RxClk Duty Cycle	R_{CDU}	45	50	55	%
Receive Data Setup Time	R_{SU}	150	-		-
Receive Data Hold Time	R_{HO}	150	-	-	ns
RxClk to Data Delay	R_{DY}	-	-	40	ns
RxClk Rise Time (10%/90%) with 25pF Loading.	R_{CLKR}	-	-	40	ns
RxClk Fall Time(90%/10%) with 25pF Loading	R_{CLKF}			40	ns
Data Pulse Width in Data Slice Mode	RZData	210	244	448	ns

FIGURE 15. TRANSMIT CLOCK AND INPUT DATA TIMING



Note: Set TCLKE bit-4 "High" in Command Control Register 0 to select **TxCLK** inversion.

FIGURE 16. RECEIVE CLOCK AND OUTPUT DATA TIMING.



Note: Set RCLKE bit=5 "High"in Command Control Register 0 to select **RxCLK** inversion.

MICROPROCESSOR INTERFACE

XRT 82L24A is equipped with a microprocessor interface for easy device configuration. The parallel port of the XRT 82L24A is compatible with both Intel and Motorola address and data buses.

The device has 4-bit address ADD[3:0] input and 8-bit bi-directional data bus ADD[7:0]. The signals required for a generic microprocessor to access the internal registers are described in Table 8.

TABLE 8: MICROPROCESSOR INTERFACE SIGNAL

<table>
<tr><td>D[7:0]</td><td>Data Input (Output): 8 bits bi-directional data bus for register access.</td></tr>
<tr><td>ADD[3:0]</td><td>Address Input: 4 bit address to select internal register location.</td></tr>
<tr><td>PTS1
PTS2</td><td>Processor Type Select:
<table>
<tr><th>PTS1</th><th>PTS2</th><th></th></tr>
<tr><td>0</td><td>0</td><td>8HC11,8081,80C188 (async.)</td></tr>
<tr><td>1</td><td>0</td><td>Motorola 68K (async.)</td></tr>
<tr><td>0</td><td>1</td><td>Intel x86 (sync.)</td></tr>
<tr><td>1</td><td>1</td><td>Intel i906,Motorola 860 (sync.)</td></tr>
</table></td></tr>
<tr><td>PCLK</td><td>Process Clock Input: Input clock for synchronous microprocessor operation. Maximum clock speed is 16MHz. This pin is internally pulled up for asynchronous microprocessor operation if no clock is present.</td></tr>
<tr><td>ALE_AS</td><td>Address Latch Input (Address Strobe): With Intel bus timing, the address inputs are latched into the internal register on the falling edge of ALE. When configured in Motorola bus timing, the address inputs are latched into the internal register on the falling edge of AS.</td></tr>
<tr><td>$\overline{CS}$</td><td>Chip Select Input: This signal must be low in order to access the parallel port.</td></tr>
<tr><td>$\overline{RD}$_$\overline{DS}$</td><td>Read Input (Data Strobe): With Intel bus timing, a low pulse on RD selects a read operation when $\overline{CS}$ pin is low. When configured in Motorola bus timing, a low pulse on DS indicates a read or write operation when $\overline{CS}$ pin is low.</td></tr>
<tr><td>$\overline{WR}$_R/$\overline{W}$</td><td>Write Input (Read/$\overline{Write}$): With Intel bus timing, a low pulse on $\overline{WR}$ selects a write operation when $\overline{CS}$ pin is low. When configured in Motorola bus timing, a high pulse on R/$\overline{W}$ selects a read operation and a low pulse on R/$\overline{W}$ selects a write operation when $\overline{CS}$ pin is low.</td></tr>
<tr><td>RDY_$\overline{DTACK}$</td><td>Ready Output (Data Transfer Acknowledge Output): With Intel bus timing, RDY is asserted high to indicate the device has completed a read or write operation. When configured in Motorola bus timing, $\overline{DTACK}$ is asserted low to indicate the device has completed a read or write operation.</td></tr>
<tr><td>$\overline{INT}$</td><td>Interrupt Output: This pin is asserted low to indicate an interrupt caused by an alarm condition in the device status registers. The activation of this pin can be blocked by the interrupt status register bit.</td></tr>
</table>

TABLE 9: MICROPROCESSOR REGISTER MAP

REGISTER NUMBER	ADDRESS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Command Control Registers (Read/$\overline{\text{Write}}$)									
0	0000	SR/$\overline{\text{DR}}$	RZData	RCLKE	TCLKE	DATAP	CODES	IMASK	SRESET
1	0001	Reserved (Set to 0)	Reserved (Set to 0)	FIFOS	RXJA	TXJA	RXMUTE	EXLOS	ICT
		reset=0	reset=0	reset=0	reset=0	reset=0	reset=0	reset=0	reset=0
Channel 0 Register									
2	0010	DMO0	LOS0	LCV0	TCLK0	DMO0IS	LOS0IS	LVC0IS	TCKL0IS
3	0011	Reserved	Reserved	Reserved	Reserved	MDMO0	MLOS0	MLCV0	MTCKL0
4	0100	Reserved	Reserved	Reserved	ALOOP0	DLOOP0	RLOOP0	TAOS0	TxOFF0
		reset=0	reset=0	reset=0	reset=0	reset=0	reset=0	reset=0	reset=0
Channel 1 Register									
5	0101	DMO1	LOS1	LCV1	TCLK1	DMO1IS	LLOSIS1	LCV1	TCKL1IS
6	0110	Reserved	Reserved	Reserved	Reserved	MDMO1	MLOS1	MLCV1	MTCKL1
7	0111	Reserved	Reserved	Reserved	ALOOP1	DLOOP1	RLOOP1	TAOS1	TxOFF1
		reset=0	reset=0	reset=0	reset=0	reset=0	reset=0	reset=0	reset=0
Channel 2 Register									
8	1000	DMO2	LOS2	LVC2	TCLK2	DMO2IS	LLOS2IS	LCV2	TCKL2IS
9	1001	Reserved	Reserved	Reserved	Reserved	MDMO2	MLOS2	MLCV2	MTCKL2
10	1010	Reserved	Reserved	Reserved	ALOOP2	DLOOP2	RLOOP2	TAOS2	TxOFF2
		reset=0	reset=0	reset=0	reset=0	reset=0	reset=0	reset=0	reset=0
Channel 3 Register									
11	1011	DMO3	LOS3	LCV3	TCLK3	DMO3IS	LLOS3IS	LCV3	TCKL3IS
12	1100	Reserved	Reserved	Reserved	Reserved	MDMO3	MLOS3	MLCV3	MTCKL3
13	1101	Reserved	Reserved	Reserved	ALOOP3	DLOOP3	RLOOP3	TAOS3	TxOFF3
		reset=0	reset=0	reset=0	reset=0	reset=0	reset=0	reset=0	reset=0

NOTE: *Address 1110 and 1111 R/W Registers (14 and 15) are Reserved for Exar Testing Purposes*

TABLE 10: COMMAND CONTROL REGISTER 0

COMMAND CONTROL REGISTER 0 PARALLEL PORT ADDRESS: 0000				
BIT NO.	**NAME**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
7	SR/$\overline{DR}$	**Single/Dual Rail:** Writing a "1" to this bit selects transmit and receive data format in single-rail mode. In this mode, HDB3/B8ZS/AMI encoder and decoder are available. Writing a "0" selects dual-rail mode.	R/W	0
6	RZData	**RZ Data:** Writing a “1” to this bit selects receive data to pass to the output after the slicers without re-timing. In this mode, PLL clock recovery, jitter attenuator, decoder and remote loop-back functions are disabled.	R/W	0
5	RCLKE	**RxClk Clock Edge:** Writing a "1" to this bit selects receive output data to be updated on positive edge of RxClk. Writing a "0" to this bit selects the negative edge of RxClk.	R/W	0
4	TCLKE	**TxClk Clock Edge:** Writing a "1" to this bit selects positive edge of TxClk to sample input data. Write "0" to select negative edge.	R/W	0
3	DATAP	**DATA Polarity:** Writing a "0" to this bit selects transmit input and receive output data to be active-high. Write "1" to select active-low.	R/W	0
2	CODES	**Coding/Decoding Select:** This bit is used in conjunction with SR/$\overline{DR}$ bit 1. If SR/$\overline{DR}$ is "1", writing a "0" to this bit selects HDB3 coding. Writing a "1" to this bit position selects AMI code.	R/W	0
1	GIE	**Global Interrupt Enable:** Writing a "0" to this bit globally disables interrupt generation caused by any alarm generated within the line interface. Write a "1" to enable interrupt generation.	R/W	0
0	SRESET	**Software Reset:** Writing a "1" to this bit longer than 10µs initiates a device reset through the microprocessor interface. All internal circuits are placed in the reset state with this bit set to a "1" except the microprocessor register bits.	R/W	0

NOTE: *Register Type Abrbreviation:*
R = Read Only, **R/W** = Read or Write, **RUR** = Reset Upon Read

TABLE 11: COMMAND CONTROL REGISTER 1

COMMAND CONTROL REGISTER 1 PARALLEL PORT ADDRESS: 0001				
BIT NO.	**NAME**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
7	--	**Reserved** Must be set to “0” for proper operation.	R/W	0
6	--	**Reserved** Must be set to “0” for proper operation.	R/W	0
5	FIFOS	**FIFO Size Select:** Writing a "1" to this bit selects 64 bit FIFO depth. Write "0" to select 32 bit FIFO depth.	R/W	0
4	RxJA	**Receive Jitter Attenuator:** Select: Writing a "1" to this bit selects jitter attenuator in the receive path. If bit 3(TxJA) is also set, jitter attenuator is disabled.	R/W	0
3	TxJA	**Transmit Jitter Attenuator Select:** Writing a "1" to this bit selects jitter attenuator in the transmit path. If bit 4(RxJA) is also set, jitter attenuator is disabled.	R/W	0
2	RXMUTE	**Receive Muting:** Writing a "1" to this bit mutes receive data output to a low state during LOS condition to prevent data chattering.	R/W	0
1	EXLOS	**Extended LOS:** Writing a "1" to this bit extends the number of zeros at the input to 4096 bits, (approximately 2mS), before LOS is declared.	R/W	0
0	ICT	**In-Circuit-Testing:** Writing a "1" to this bit causes all output pins to be in high impedance mode for in-circuit testing. The software ICT function is equivalent to connecting pin 20 to ground.	R/W	0

NOTE: *Register Type Abrbreviation:*
R = Read Only, **R/W** = Read or Write, **RUR** = Reset Upon Read

TABLE 12: CHANNEL STATUS REGISTER

CHANNEL STATUS REGISTER PARALLEL PORT ADDRESS CHANNEL 0: 0010 PARALLEL PORT ADDRESS CHANNEL 1: 0101 PARALLEL PORT ADDRESS CHANNEL 2: 1000 PARALLEL PORT ADDRESS CHANNEL 3: 1011				
BIT NO.	**SYMBOL**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
7	DMOn	**Driver Monitor Output:** This bit is set to a "1" to indicate current DMO is detected. Any change in the state of this bit causes an interrupt to be generated. Reading this register bit does not clear the DMO bit.	R	0
6	LOSn	**Loss of Signal:** This bit is set to a "1" to indicate current LOS condition is detected. Any change in the state of this bit causes an interrupt to be generated. Reading this register bit does not clear the LOS bit.	R	0
5	LCVn	**Line Code Violation:** This bit is set to a "1" to indicate current LCV condition is detected. Any change in the state of this bit causes an interrupt to be generated. Reading this register bit does not clear the LCV bit.	R	0
4	TCKLn	**Transmit Clock Loss:** This bit is set to a "1" to indicate current TxClk clock loss is detected. Any change in the state of this bit causes an interrupt to be generated. Reading this register bit does not clear the TCKL bit.	R	0
3	DMOnIS	**Driver Monitor Output:** This bit is set to a "1" every time the state of DMO status changes since last read. This bit is cleared by a read operation.	RUR	0
2	LOSnIS	**Latched- Loss of signal:** This bit is set to a "1" every time the state of LOS changes since last read. This bit is cleared by a read operation.	RUR	0
1	LCVnIS	**Latched- Line Code Violation:** This bit is set to a "1" every time the state of LCV changes since last read. This bit is cleared by a read operation.	RUR	0
0	TCLKnIS	**Latched-Transmit Clock Loss.** This bit is set to a "1" every time the state of TCKL changes since last read. This bit is cleared by a read operation.	RUR	0

NOTE: n = channel number 0 to 3.

NOTE: *Register Type Abrbreviation:*

R = Read Only, **R/W** = Read or Write, **RUR** = Reset Upon Read

TABLE 13: CHANNEL MASK REGISTER

CHANNEL MASK REGISTER PARALLEL PORT ADDRESS CHANNEL 0: 0011 PARALLEL PORT ADDRESS CHANNEL 1: 0110 PARALLEL PORT ADDRESS CHANNEL 2: 1001 PARALLEL PORT ADDRESS CHANNEL 3: 1100				
BIT NO.	**NAME**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
7	--	This bit is Reserved.	R/W	0
6	--	This bit is Reserved.	R/W	0
5	--	This bit is Reserved.	R/W	0
4	--	This bit is Reserved.	R/W	0
3	DMOnIS	**Driver Monitor Output Interrupt Status:** Writing a "1" to this bit enables DMO alarm interrupt generation.	R/W	0
2	LOSnIS	**Loss of Signal Interrupt Status:** Writing a "1" to this bit enables LOS alarm interrupt generation.	R/W	0
1	LCVnIS	**Line Code Violation Interrupt Status:** Writing a "1" to this bit enables LCV interrupt generation.	R/W	0
0	TCKLnIS	**Transmit Clock Loss Interrupt Status:** Writing a "1" to this bit enables TxClk clock loss interrupt generation.	R/W	0

NOTE: n = channel number 0 to 3.

NOTE: *Register Type Abrbreviation:*

R = Read Only, **R/W** = Read or Write, **RUR** = Reset Upon Read

TABLE 14: CHANNEL CONTROL REGISTER

CHANNEL CONTROL REGISTER Parallel Port Address Channel 0: 0100 Parallel Port Address Channel 1: 0111 Parallel Port Address Channel 2: 1010 Parallel Port Address Channel 3: 1101				
BIT NO.	**SYMBOL**	**FUNCTION**	**REGISTER TYPE**	**RESET VALUE**
7 6 5	****	These bits are Reserved.	R/W R/W R/W	0 0 0
4	LLOOPn	**Local Loop-Back:** Writing a "1" to this bit enables Analog Local Loop-Back. Simultaneously setting RLOOP High is not allowed.	R/W	0
3	DLOOPn	**Digital Loop-Back:** Writing a "1" to this bit enables Digital Loop-Back.	R/W	0
2	RLOOPn	**Remote Loop-Back:** Writing a "1" to this bit enables Remote Loop-back. Simultaneously setting LLOOP High is not allowed.	R/W	0
1	TAOSn	**Transmit All Ones:** Writing a "1" to this bit enables the All Ones AMI signal to be transmitted to the line.	R/W	0
0	TxOFFn	**Transmitter Off:** Writing a "1" to this bit powers down the transmitter and places the corresponding output driver in a high impedance mode.	R/W	0

NOTE: n = channel number 0 to 3.

NOTE: *Register Type Abrbreviation:*

R = Read Only, **R/W** = Read or Write, **RUR** = Reset Upon Read

Microprocessor Interface I/0 Timing

Intel Interface Timing

The signals used for the Intel microprocessor interface are: Address Latch Enable (ALE), Read Enable ($\overline{RD}$), Write Enable ($\overline{WR}$), Chip Select ($\overline{CS}$), Address and Data bits. The microprocessor interface uses minimum external glue logic and is compatible with the timings of the 8051 or 80C188 with an 8-16 MHz clock frequency, and with the timings of x86 or I960 family or microprocessors. The interface timing shown in Figure 17 and Figure 18 is described in Table 15.

FIGURE 17. INTEL INTERFACE TIMING (READ)

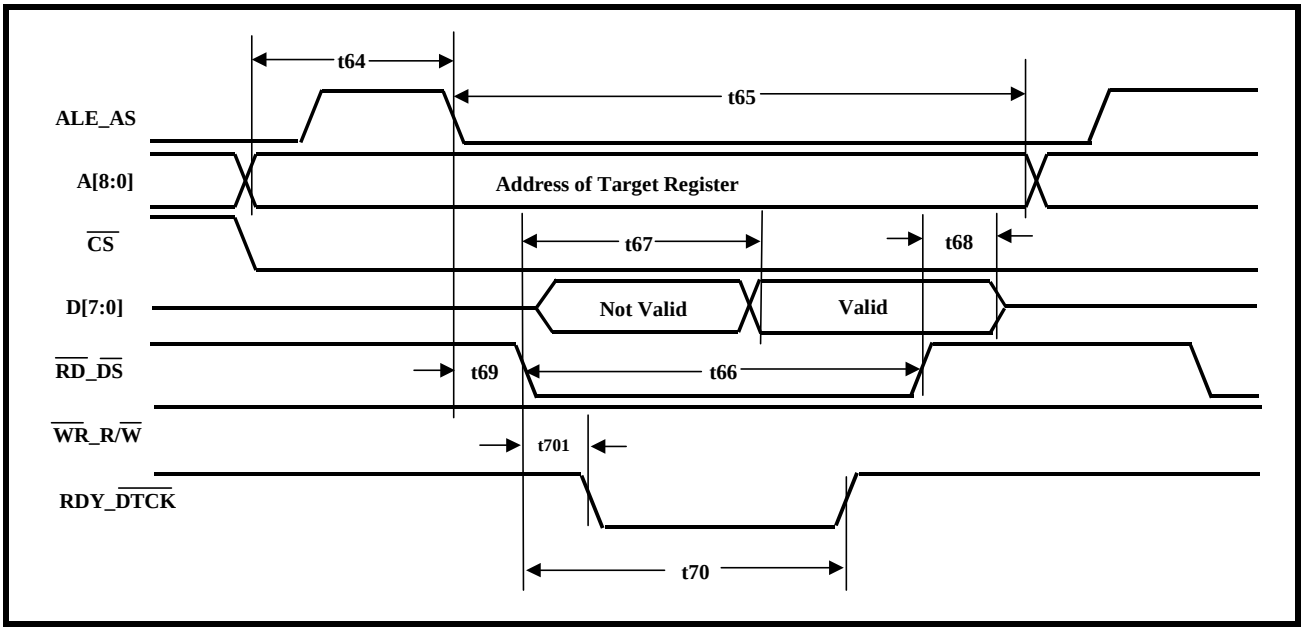


FIGURE 18. INTEL INTERFACE TIMING (WRITE)

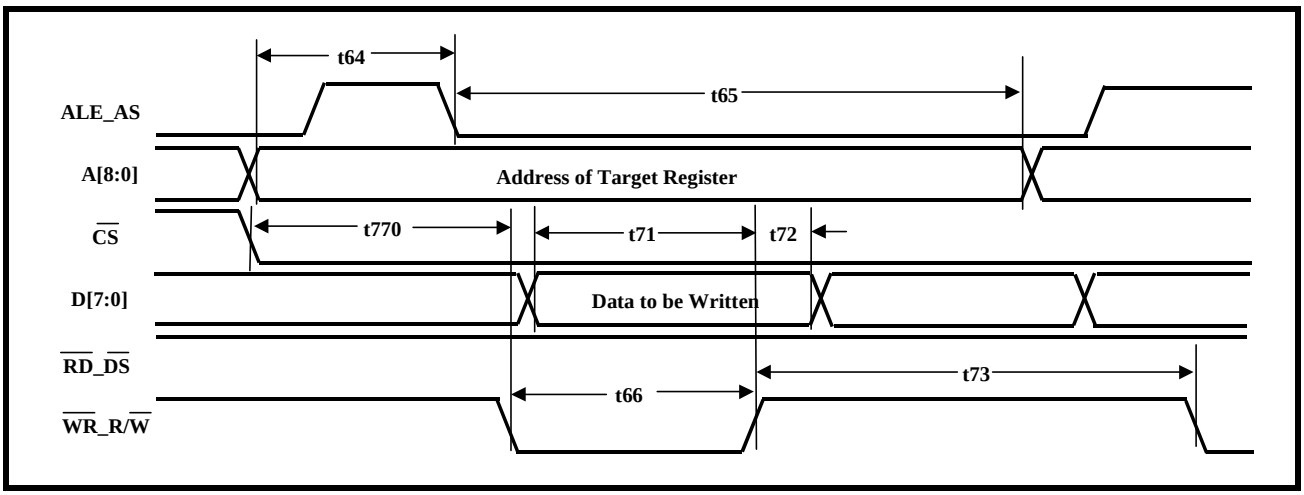


TABLE 15: INTEL INTERFACE TIMING SPECIFICATIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	CONDITION
t_{64}	A8 - A0 Setup Time to ALE_AS Low	4			ns
t_{65}	A8 - A0 Hold Time from ALE_AS Low.	2			ns
Intel Type Read Operation					
t_{66}	RDS_$\overline{DS}$ Pulse Width	260			ns
t_{67}	Data Valid from RDS_DS* Low.	240			ns
t_{68}	Data Bus Floating from RDS_DS* High	2			ns
t_{69}	ALE to $\overline{RD}$ Time	4			ns
t_{701}	$\overline{RD}$ Time to "NOT READY" (e.g., RDY_$\overline{DTCK}$ toggling "Low")			145	ns
t_{76}	Minimum Time between Read Burst Access (e.g., the rising edge of $\overline{RD}$ to falling edge of $\overline{RD}$)	60			ns
Intel Type Write Operations					
t_{71}	Data Setup Time to $\overline{WR}$_R/$\overline{W}$ High	160			ns
t_{72}	Data Hold Time from $\overline{WR}$_R/$\overline{W}$ High	0			ns
t_{73}	High Time between Reads and/ or Writes	60			ns
t_{74}	ALE to $\overline{WR}$ Time	4			ns
t_{77}	Min Time between Write Burst Access (e.g., the rising edge of $\overline{WR}$ to the falling edge of $\overline{WR}$)	60			ns
t_{770}	$\overline{CS}$ Assertion to falling edge of $\overline{WR}$_R/$\overline{W}$	20			ns

Motorola Interface Timing

The signals used in the Motorola microprocessor interface mode are: Address Strobe (AS), Data Strobe ($\overline{DS}$), Read/Write Enable (R/$\overline{W}$), Chip Select ($\overline{CS}$), Address and Data bits. The interface is compatible with the timing of a Motorola 68000 microprocessor family with up to 16.67 MHz clock frequency. The interface timing is shown in Figure 19, Figure 20 and Figure 21. The I/O specifications are shown in Table 16.

FIGURE 19. MICROPROCESSOR INTERFACE TIMING - MOTOROLA TYPE PROGRAMMED I/O READ OPERATION

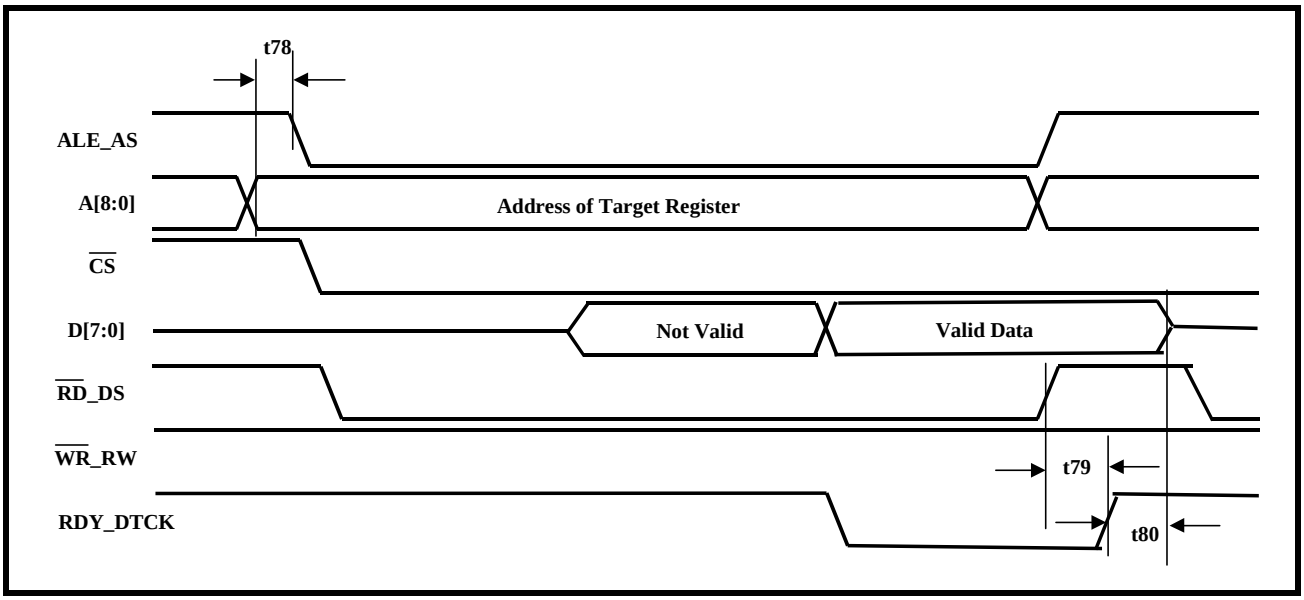


FIGURE 20. MICROPROCESSOR INTERFACE TIMING - MOTOROLA TYPE PROGRAMMED I/O WRITE OPERATION

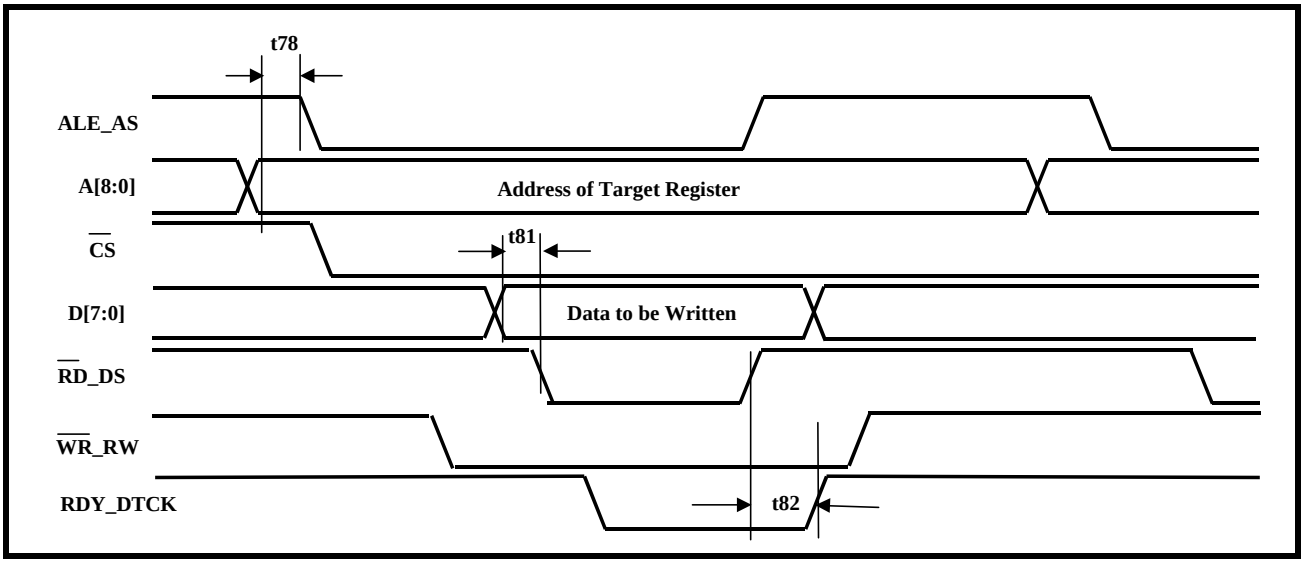


FIGURE 21. MICROPROCESSOR INTERFACE TIMING - $\overline{\text{RESET}}$ PULSE WIDTH

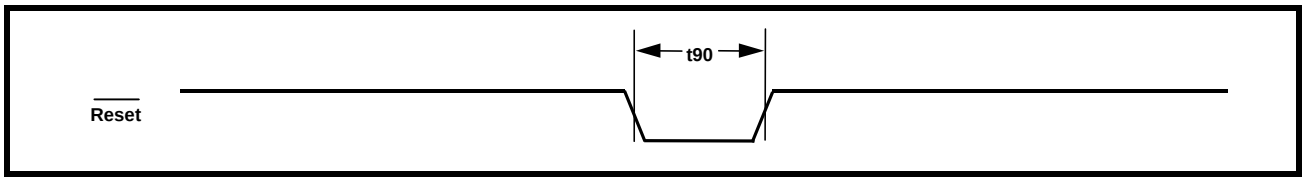


TABLE 16: MOTOROLA INTERFACE TIMING SPECIFICATION

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Microprocessor Interface - Motorola Read Operations (see Figure 19)					
t_{78}	A3 - A0 Setup Time to falling edge of ALE_AS	5			ns
t_{79}	Rising edge of $\overline{\text{RD}}$_DS to rising edge of RDY_DTCK delay	0			ns
t_{80}	Rising edge of RDY_$\overline{\text{DTCK}}$ to tri-state of D[7:0]	0			ns
Microprocessor Interface - Motorola Write Operations (see Figure 20)					
t_{78}	A3 - A0 Setup Time to falling edge of ALE_AS	5			ns
t_{81}	D[7:0] Setup Time to falling edge of $\overline{\text{RD}}$_DS	10			ns
t_{82}	Rising edge of $\overline{\text{RD}}$_DS to rising edge of RDY_DTCK delay	0			ns
Reset pulse width - both Motorola and Intel Operations (see Figure 21)					
t_{90}	$\overline{\text{Reset}}$ pulse width	30			ns

JITTER TOLERANCE

Input Jitter Tolerance Measurements are presented for the following two situations.

1. The Jitter Attenuator within the Channel-Under-Test is disabled.

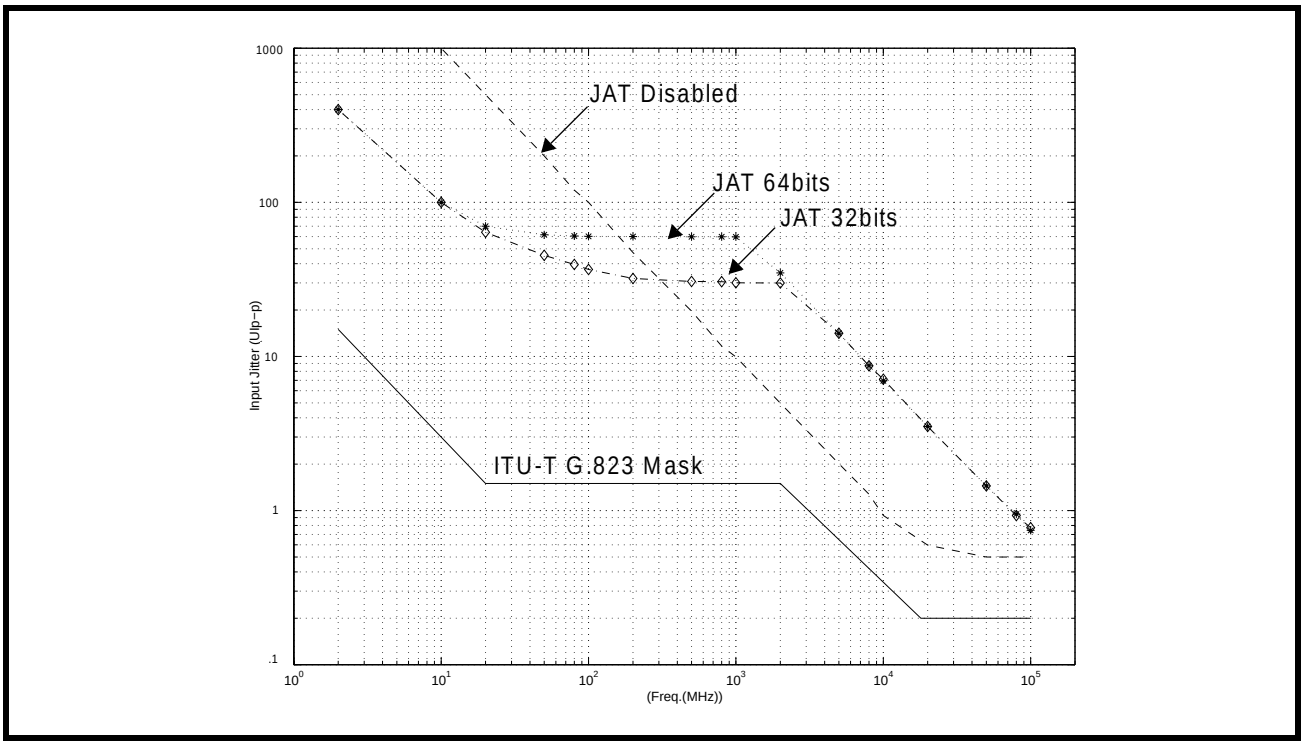
2. The Jitter Attenuator within the Channel-Under-Test is enabled and configured to operate in the Receive Path.

The results of the Input Jitter Tolerance Measurements are plotted in Figure 22.

Test Conditions

- Test Pattern $2^{\wedge 15}$-1
- (-6dB) Cable Loss

FIGURE 22. RECEIVE MAXIMUM JITTER TOLERANCE



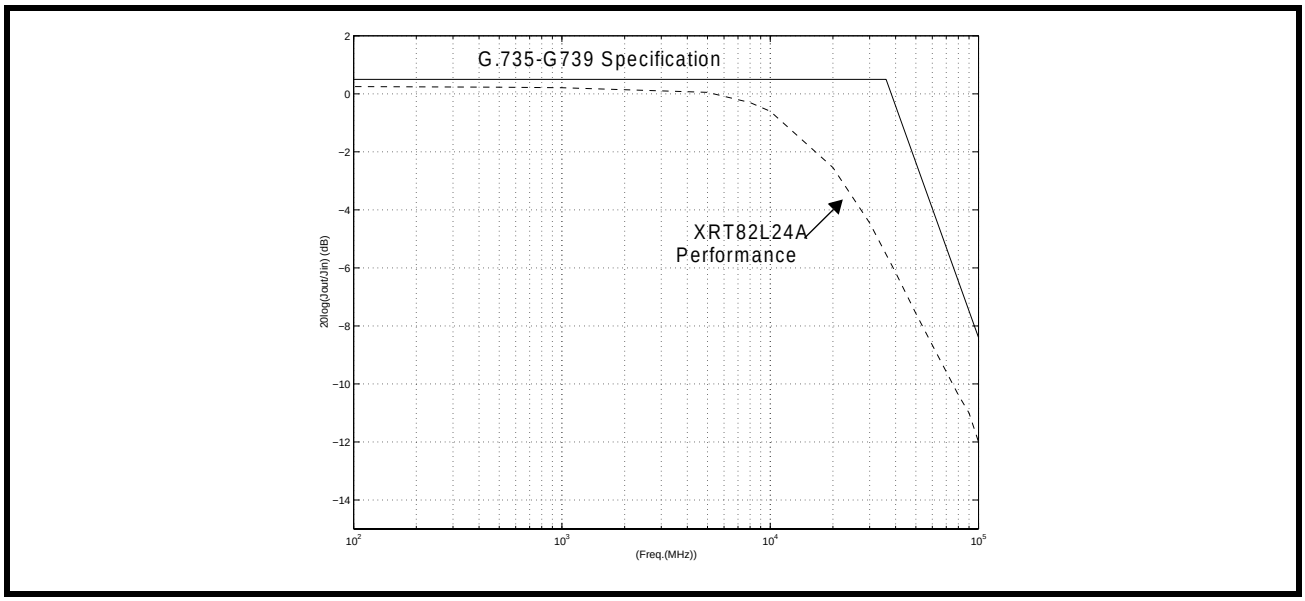
Receiver Jitter Transfer Function (Jitter Attenuator disabled)

Test Conditions:

- Test Pattern $2^{\wedge 15}$-1

- Input Jitter 0.5UIp-pThe results of the Input Jitter Tolerance Measurements with the Jitter Attenuator enabled and configured to operate in the receive path are plotted in Figure 23.

FIGURE 23. RECEIVER JITTER TRANSFER FUNCTION (JITTER ATTENUATOR DISABLED)

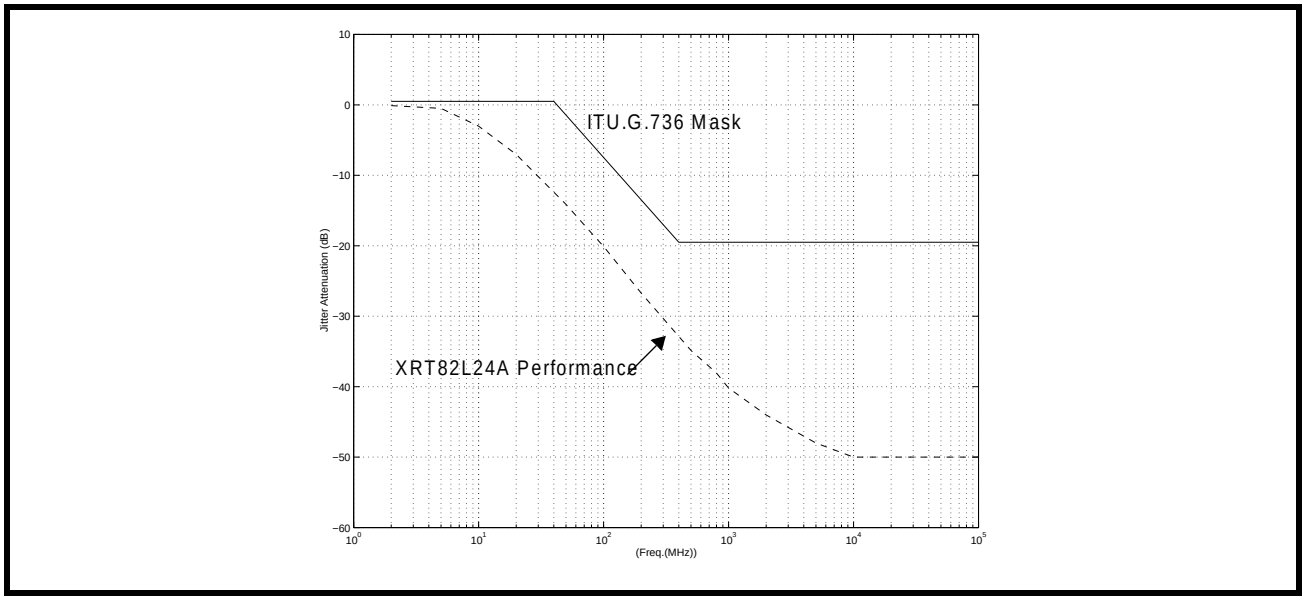


Receiver Jitter Transfer Function (Jitter Attenuator enabled)

Test Conditions:

- Test Pattern $2^{\wedge 15}$-1
- Input Jitter 75% of Maximum Jitter Tolerance

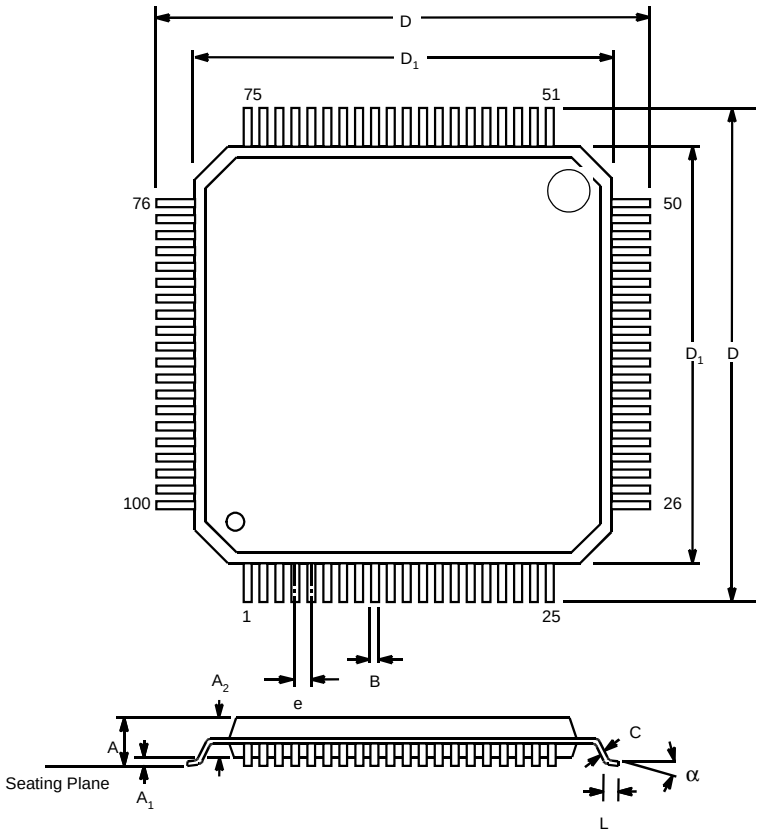
FIGURE 24. JITTER ATTENUATION FUNCTION



ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT82L24AIV	100 Lead TQFP (14 x 14 x 1.4mm)	-40°C to +85°C
PACKAGE DISSIPATION	Theta-JA 38° C/W	Theta-JC 6° C/W

PACKAGE DIMENSIONS 100 LEAD TQFP 14X14MM



NOTE: *The control dimension is the millimeter column*

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.055	0.063	1.40	1.60
A_1	0.002	0.006	0.05	0.15
A_2	0.053	0.057	1.35	1.45
B	0.007	0.011	0.17	0.27
C	0.004	0.008	0.09	0.20
D	0.622	0.638	15.80	16.20
D_1	0.547	0.555	13.90	14.10
e	0.020 BSC		0.50 BSC	
L	0.018	0.030	0.45	0.75
α	0°	7°	0°	7°

REVISION HISTORY

REVISION	DATE	DESCRIPTION
1.0.0	11/02	Initial issue
1.1.0	10/03	Table 8 corrected PCLK frequency from 33MHz to16MHz and changed pulled down to pulled up. Figures 12 & 13 transformer ratio on Receive side changed from 2:1 to 1:2.
1.1.1	06/04	Added the Manufacturing Mark on the Package Drawing.
1.1.2	07/04	Changed Max power consumption for 100% Mark Density to 680 and 600 mW respectively for 75 and 120 Ohm Loads.

NOTICE

EXAR Corporation reserves the right to make changes to the products contained in this publication in order to improve design, performance or reliability. EXAR Corporation assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Charts and schedules contained here in are only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked; no responsibility, however, is assumed for inaccuracies.

EXAR Corporation does not recommend the use of any of its products in life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness. Products are not authorized for use in such applications unless EXAR Corporation receives, in writing, assurances to its satisfaction that: (a) the risk of injury or damage has been minimized; (b) the user assumes all such risks; (c) potential liability of EXAR Corporation is adequately protected under the circumstances.

Copyright 2004 EXAR Corporation

Datasheet August 2004.

Reproduction, in part or whole, without the prior written consent of EXAR Corporation is prohibited.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View XRT82L24AIV-F on WIN SOURCE
- Exar Corporation Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management