THE DATASHEET OF

C8051F991-GMR

January 27, 2014

C8051F990/1/6/7, C8051F980/1/2/3/5/6/7/8/9 Rev. A/B Errata

Errata Status Summary

Errata #	Title	Status	
		Rev A Device	Rev B Device
1	Capacitive sense pin monitor	See Errata Details 1	Fixed
2	CS0MD1 bit mapping	See Errata Details 2	Fixed
3	No ADC Input on P1.4	See Errata Details 3	Fixed
4	SmaRTClock startup time	See Errata Details 4	Fixed
5	Non Sleep Mode Current	See Errata Details 5	Fixed
6	Writes to CRC0CN that initiate a CRC0 operation	See Errata Details 6	Fixed
7	Address 0x0000 of XRAM	Information See Errata Details 7	Information See Errata Details 7
8	POR Supply Monitor for supply voltages greater than 2.4 V	Information See Errata Details 8	Information See Errata Details 8
9	Writes to CRC0CN that initiate a CRC0 operation	See Errata Details 9	See Errata Details 9
10	Writes to ADC0H and ADC0L while burst mode is enabled	See Errata Details 10	See Errata Details 10

Rev B is recommended for production.

Errata Details

1. **Capacitive Sense Pin Monitor**

   Description: An issue has been identified with the capacitive sense pin monitor function when the device enters Suspend mode. If the pin monitor is enabled, under some circumstances, conversions may be continuously initiated.

   Impacts: The Capacitive sense conversion may not complete due to continuously being restarted.

   Workaround: Disable all pin monitor functionality (CS0PM = 0x00) before entering Suspend mode.

   Resolution: Fixed in Rev B and later.

2. **CS0MD1 Bit Mapping**

   Description: Bit 4 and Bit 5 of CS0MD1 have been incorrectly mapped to Bit 5 and Bit 6.

   Impacts: Both the CS0 Digital Polarity Select and the CS0 Double Reset Select function share the same bit (Bit 5) in the CS0MD1 register. This may cause a limitation in functionality if these functions are being used.

   Workaround: Since making a change to one of the functions will cause a change to the other function, care should be taken when setting up either function. If Bit 5 and Bit 6 are not written, then the device will follow the default behavior described in the data sheet.

   Resolution: Fixed in Rev B and later.

3. **No ADC Input on P1.4**

   Description: An issue has been identified that prevents P1.4 from being routed to the ADC.

   Impacts: On C8051F996/7/8/9 devices, P1.4 cannot be used as an analog input for the ADC. This behavior does not affect C8051F990/1/2/3/4/5 devices.

   Resolution: Fixed in Rev B and later.

4. **SmaRTClock Startup Time**

   Description: A modification was made to the SmaRTClock crystal driver circuit.

   Impacts: The startup time of the SmaRTClock crystal oscillator is longer than other devices in the ‘F9xx family. Instability may occur at voltages above 3.0 V. The “Oscillator Robustness Test” described in the data sheet is not a valid way to determine oscillator robustness for this silicon revision.

   Workaround: Disable automatic gain control or use bias doubling to increase the drive current if the crystal has high ESR (> 40 kΩ) or if the supply voltage is greater than 3.0 V.

   Resolution: Fixed in Rev B and later.

5. **Non Sleep Mode Current**

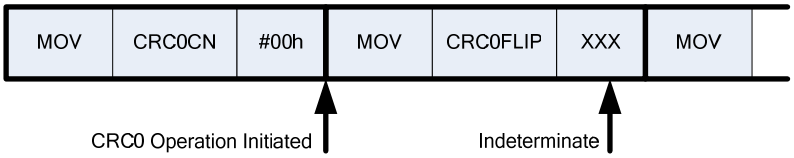
   Description: An internal pull-up transistor is enabled, drawing approximately 100 µA, when the precision oscillator is disabled.

   Impacts: In all power modes other than Sleep mode, device power consumption will be 100 µA higher than data sheet specifications if the precision oscillator is disabled.

   Resolution: Fixed in Rev B and later.

6. **Writes to CRC0CN that Initiate a CRC0 Operation**

Description: The third op-code byte fetched from program memory following a write to CRC0CN that initiates a CRC0 operation is indeterminate.



Impacts: If the indeterminate op-code byte is the first or second byte in an instruction, improper code execution may result.

Workaround: Writes to CRC0CN that initiate a CRC0 operation must be immediately followed by a benign 3-byte instruction whose third byte is a "don't care." An example of such an instruction is the write of a dummy value to the CRC0FLIP register using a 3-byte MOV instruction. The value written to CRC0FLIP will be indeterminate, but this should have no effect on the system. To ensure that both instructions are executed without interruption, global interrupts should be disabled.

Note: When programming in C, the dummy value written to CRC0FLIP should be a non-zero value. This prevents the compiler from generating the following instruction sequence:

```
CLR  A
MOV  CRC0FLIP,  A
```

When programming in C, the disassembly should be checked to ensure the compiler generated the following instruction sequence:

```
MOV  CRC0FLIP,  #AAh  where #AAh is the non-zero dummy value.
```

Resolution: Fixed in Rev B and later.

7. **Address 0x0000 of XRAM**

Description: On device reset, or upon waking up from Sleep mode, address 0x0000 of external memory may be overwritten by an indeterminate value. The indeterminate value is 0x00 in most situations.

Impacts: Application data stored at 0x0000 in external memory may be overwritten upon reset or waking up from sleep mode.

Workaround: A dummy variable should be placed at address 0x0000 in external memory to ensure that the application software does not store any data that needs to be retained during sleep or reset at this memory location. The compiler-independent example below shows how to locate a dummy variable at address 0x0000 in external memory.

```
LOCATED_VARIABLE_NO_INIT (reserved, U8, SEG_XDATA, 0x0000);
```

Compiler-independent code requires the use of the compiler_defs.h and c8051F990_defs.h header files supplied in the C:\Silabs\MCU\INC folder after installation of the Silicon Laboratories IDE.

Resolution: This information will be added to the device data sheet.

8. **POR Supply Monitor for supply voltages greater than 2.4 V**

   Description: The POR Supply Monitor should not be disabled if the supply voltage is greater than 2.4 V.

   Impacts: The lowest power sleep mode current, 10 nA typical, can only be achieved when the supply voltage is less than 2.4 V. The lowest power sleep mode for voltages above 2.4 V is 50 nA typical, with the POR Supply Monitor enabled.

   Resolution: This information will be added to the device data sheet.

9. **Writes to CRC0CN that Initiate a CRC0 Operation**

   Description: The flash read signal on Revision B devices will deactivate early if the write to the CRC0CN register that starts the automatic flash CRC operation is not followed by a single cycle instruction.

   Impacts: The automatic flash CRC operation may not complete successfully if the write to the CRC0CN register that starts the operation is not followed by a single cycle instruction.

   Workaround: Writes to CRC0CN that initiate a CRC0 operation must be immediately followed by a benign single-cycle instruction. An example of such an instruction is the write of a value of zero to the CRC0FLIP register in C. When programming in C, the disassembly should be checked to ensure the compiler generated the following instruction sequence:

```
CLR   A
MOV  CRC0FLIP,  A
```

   For assembly programs, clear the accumulator:

```
CLR  A
```

   Resolution: Will be fixed in Rev C and later.

10. **Writes to ADC0H and ADC0L while Burst Mode is Enabled**

    Description: The ADC0H and ADC0L registers can be corrupted if firmware writes to them while burst mode is enabled on Revision B devices.

    Impacts: Firmware that writes to the ADC0H and ADC0L registers while burst mode is enabled may be setting the accumulator to an incorrect value.

    Workaround: Firmware should first disable burst mode before writing to the ADC0H and ADC0L registers. Once the write completes, burst mode can be re-enabled.

    Resolution: Will be fixed in Rev C and later.

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