



**THE DATASHEET OF
CY7C199CN-12ZXC**



256K (32K x 8) Static RAM

Features

- Fast access time: 12 ns, 15 ns, 20 ns, and 25 ns
- Wide voltage range: 5.0V ± 10% (4.5V to 5.5V)
- CMOS for optimum speed and power
- TTL-compatible inputs and outputs
- 2.0V data retention
- Low CMOS standby power
- Automated power down when deselected
- Available in Pb-free 28-pin TSOP I, 28-pin Molded SOJ and 28-pin DIP packages

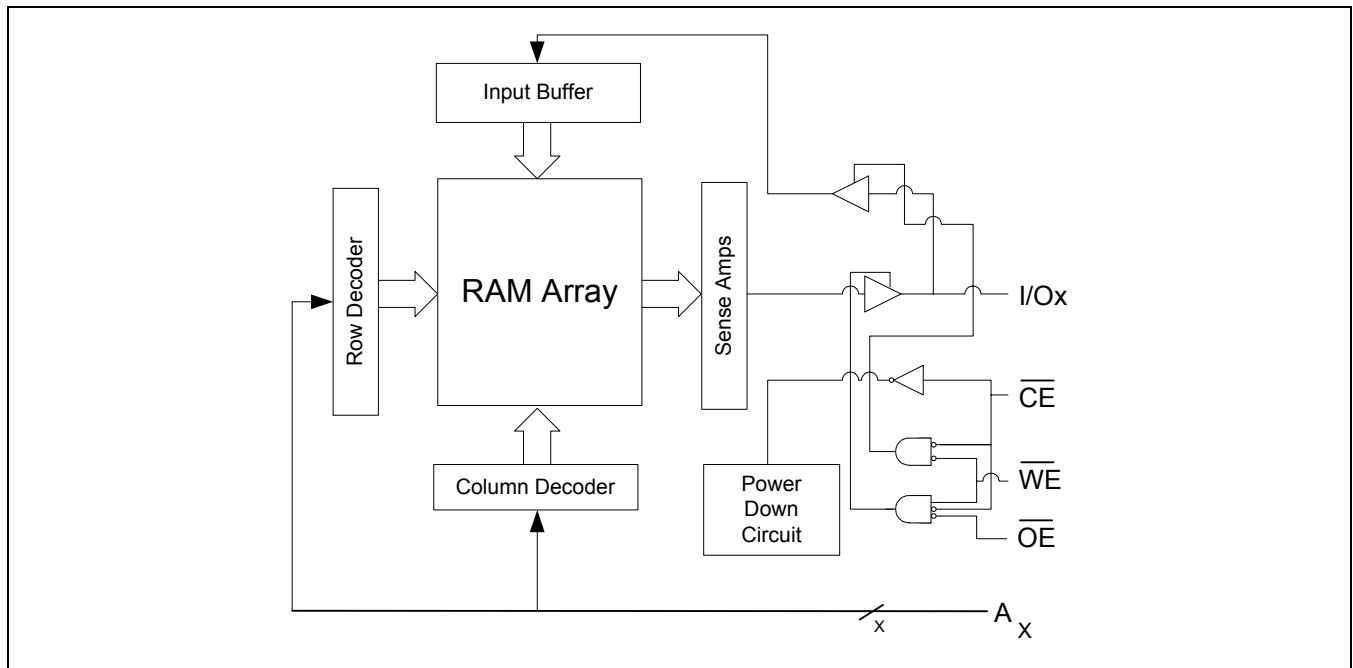
General Description ^[1]

The CY7C199CN is a high performance CMOS Asynchronous SRAM organized as 32K by 8 bits that supports an asynchronous memory interface. The device features an automatic power down feature that reduces power consumption when deselected.

See the "Truth Table" on page 3 in this data sheet for a complete description of read and write modes.

The CY7C199CN is available in Pb-free 28-pin TSOP I, 28-pin Molded SOJ and 28-pin DIP package(s).

Logic Block Diagram



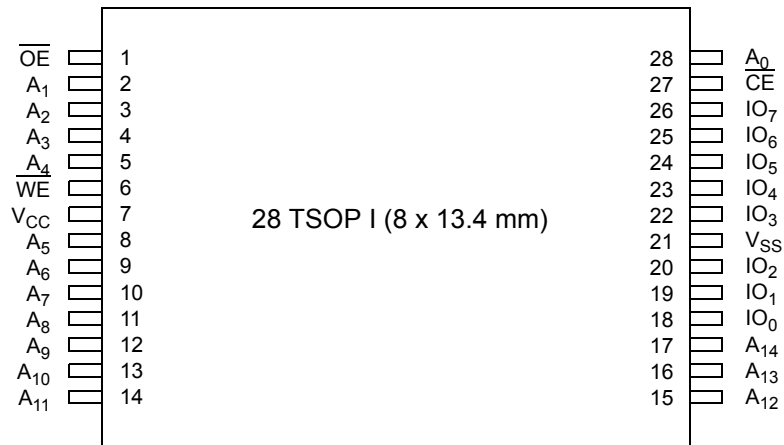
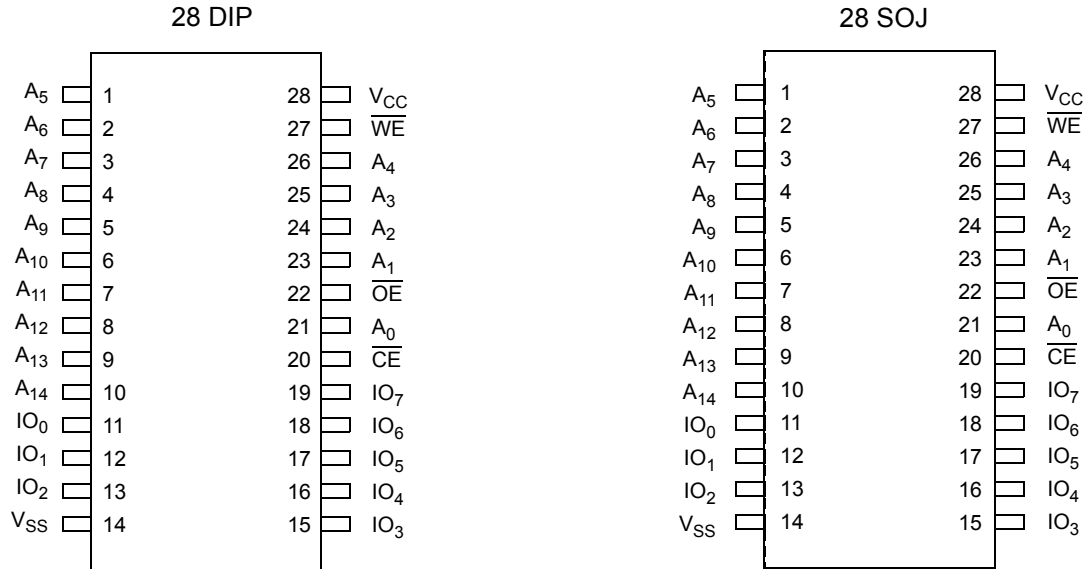
Product Portfolio

| | -12 | -15 | -20 | -25 | Unit |
|--|-----|-----|-----|-----|------|
| Maximum Access Time | 12 | 15 | 20 | 25 | ns |
| Maximum Operating Current | 85 | 80 | 75 | 75 | mA |
| Maximum CMOS Standby Current (low power) | 500 | 500 | 500 | 500 | μA |

Note

1. For best practices recommendations, refer to the Cypress application note *System Design Guidelines* on www.cypress.com.

Pin Layout and Specifications



Pin Description

| Pin | Type | Description | DIP | SOJ | TSOP I |
|------------------------|-----------------|--------------------|---|---|--|
| A _X | Input | Address Inputs | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26 | 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 21, 23, 24, 25, 26 | 2, 3, 4, 5, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 28 |
| $\overline{\text{CE}}$ | Control | Chip Enable | 20 | 20 | 27 |
| IO _X | Input or Output | Data Input Outputs | 11, 12, 13, 15, 16, 17, 18, 19 | 11, 12, 13, 15, 16, 17, 18, 19 | 18, 19, 20, 22, 23, 24, 25, 26 |
| $\overline{\text{OE}}$ | Control | Output Enable | 22 | 22 | 1 |
| V _{CC} | Supply | Power (5.0V) | 28 | 28 | 7 |
| V _{SS} | Supply | Ground | 14 | 14 | 21 |
| $\overline{\text{WE}}$ | Control | Write Enable | 27 | 27 | 6 |

Truth Table

| $\overline{\text{CE}}$ | $\overline{\text{OE}}$ | $\overline{\text{WE}}$ | IO _X | Mode | Power |
|------------------------|------------------------|------------------------|-----------------|----------------------------|-----------------------------|
| H | X | X | High-Z | Deselect/Power Down | Stand by (I _{SB}) |
| L | L | H | Data Out | Read | Active (I _{CC}) |
| L | X | L | Data In | Write | Active (I _{CC}) |
| L | H | H | High-Z | Selected, Outputs Disabled | Active (I _{CC}) |

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

| Parameter | Description | Value | Unit |
|------------------------------------|--|-------------------------------|------|
| T _{STG} | Storage Temperature | -65 to +150 | °C |
| T _{AMB} | Ambient Temperature with Power Applied (that is, case temperature) | -55 to +125 | °C |
| V _{CC} | Core Supply Voltage Relative to V _{SS} | -0.5 to +7.0 | V |
| V _{IN} , V _{OUT} | DC Voltage Applied to Any Pin Relative to V _{SS} | -0.5 to V _{CC} + 0.5 | V |
| I _{OUT} | Output Short-Circuit Current | 20 | mA |
| V _{ESD} | Static Discharge Voltage (in accordance with MIL-STD-883, Method 3015) | > 2001 | V |
| I _{LU} | Latch-up Current | > 200 | mA |

Operating Range

| Range | Ambient Temperature (T _A) | Voltage Range (V _{CC}) |
|--------------|---------------------------------------|----------------------------------|
| Commercial | 0°C to 70°C | 5.0V ± 10% |
| Industrial | -40°C to 85°C | 5.0V ± 10% |
| Automotive-A | | |

DC Electrical Characteristics

Over the Operating Range (–12, –15) [2]

| Parameter | Description | Condition | Power | –12 | | –15 | | Unit |
|------------------|--|---|-------|------|-----------------------|------|-----------------------|------|
| | | | | Min | Max | Min | Max | |
| V _{IH} | Input HIGH Voltage | | – | 2.2 | V _{CC} + 0.3 | 2.2 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW Voltage | | – | –0.5 | 0.8 | –0.5 | 0.8 | V |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min, I _{OH} = –4.0 mA | – | 2.4 | – | 2.4 | – | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min, I _{OL} = 8.0 mA | – | – | 0.4 | – | 0.4 | V |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max, I _{OUT} = 0 mA, f = F _{max} = 1/t _{RC} | – | – | 85 | – | 80 | mA |
| I _{SB1} | Automatic \overline{CE} Power Down Current TTL Inputs | Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = F _{max} | – | – | 30 | – | 30 | mA |
| | | | L | – | 10 | – | 10 | mA |
| I _{SB2} | Automatic \overline{CE} Power Down Current CMOS Inputs | Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} – 0.3V, or V _{IN} ≤ 0.3V, f = 0 | – | – | 10 | – | 10 | mA |
| | | | L | – | 500 | – | 500 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _I ≤ V _{CC} , Output Disabled | – | –5 | +5 | –5 | +5 | μA |
| I _{IX} | Input Leakage Current | GND ≤ V _I ≤ V _{CC} | – | –5 | +5 | –5 | +5 | μA |

DC Electrical Characteristics

Over the Operating Range (–20, –25) [2]

| Parameter | Description | Condition | Power | –20 | | –25 | | Unit |
|------------------|--|---|-------|------|-----------------------|------|-----------------------|------|
| | | | | Min | Max | Min | Max | |
| V _{IH} | Input HIGH Voltage | | – | 2.2 | V _{CC} + 0.3 | 2.2 | V _{CC} + 0.3 | V |
| V _{IL} | Input LOW Voltage | | – | –0.5 | 0.8 | –0.5 | 0.8 | V |
| V _{OH} | Output HIGH Voltage | V _{CC} = Min, I _{OH} = –4.0 mA | – | 2.4 | – | 2.4 | – | V |
| V _{OL} | Output LOW Voltage | V _{CC} = Min, I _{OL} = 8.0 mA | – | – | 0.4 | – | 0.4 | V |
| I _{CC} | V _{CC} Operating Supply Current | V _{CC} = Max, I _{OUT} = 0 mA, f = F _{max} = 1/t _{RC} | – | – | 75 | – | 75 | mA |
| I _{SB1} | Automatic \overline{CE} Power Down Current TTL Inputs | Max V _{CC} , $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = F _{max} | – | – | 30 | – | 30 | mA |
| | | | L | – | 10 | – | 10 | mA |
| I _{SB2} | Automatic \overline{CE} Power Down Current CMOS Inputs | Max V _{CC} , $\overline{CE} \geq V_{CC} - 0.3V$, V _{IN} ≥ V _{CC} – 0.3V, or V _{IN} ≤ 0.3V, f = 0 | – | – | 10 | – | 10 | mA |
| | | | L | – | 500 | – | 500 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _i ≤ V _{CC} , Output Disabled | – | –5 | +5 | –5 | +5 | μA |
| I _{IX} | Input Leakage Current | GND ≤ V _i ≤ V _{CC} | – | –5 | +5 | –5 | +5 | μA |

Note

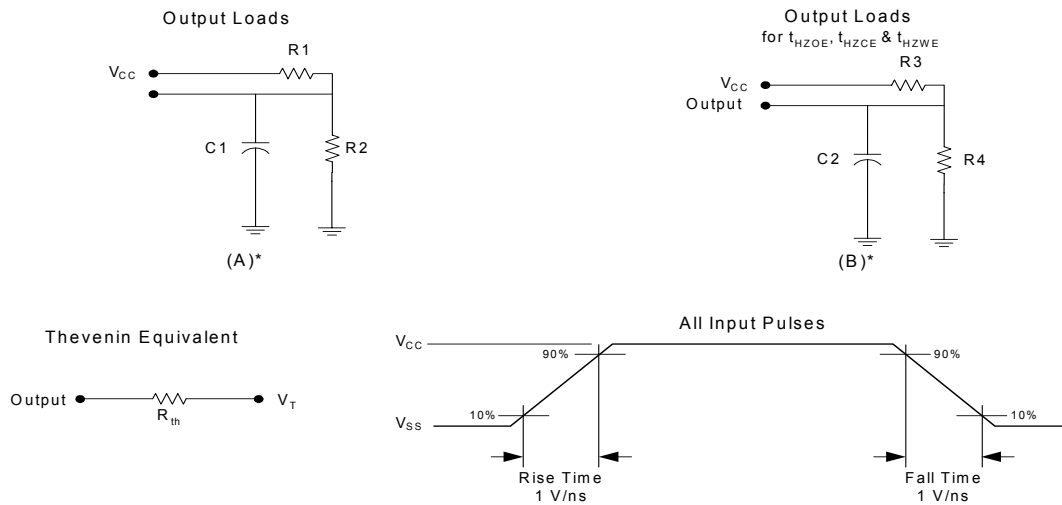
 2. V_{IL} (min) = –2.0V for pulse durations of less than 20 ns.

Capacitance ^[3]

| Parameter | Description | Conditions | Max | Unit |
|-----------|--------------------|--|-----|------|
| C_{IN} | Input Capacitance | $T_A = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{CC} = 5.0\text{V}$ | 8 | pF |
| C_{OUT} | Output Capacitance | | 8 | |

Thermal Resistance ^[3]

| Parameter | Description | Conditions | TSOP I | SOJ | DIP | Unit |
|---------------|--|--|--------|-------|-------|--------------------|
| Θ_{JA} | Thermal Resistance (junction to ambient) | Still air, soldered on a 3×4.5 square inch, two-layer printed circuit board | 88.6 | 79 | 69.33 | $^\circ\text{C/W}$ |
| Θ_{JC} | Thermal Resistance (junction to case) | | 21.94 | 41.42 | 31.62 | |

AC Test Loads


* including scope and jig capacitance

AC Test Conditions

| Parameter | Description | Nom | Unit |
|-----------|-------------------|------|----------|
| C1 | Capacitor 1 | 30 | pF |
| C2 | Capacitor 2 | 5 | |
| R1 | Resistor 1 | 480 | Ω |
| R2 | Resistor 2 | 255 | |
| R3 | Resistor 3 | 480 | |
| R4 | Resistor 4 | 255 | |
| R_{TH} | Resistor Thevenin | 167 | |
| V_{TH} | Voltage Thevenin | 1.73 | V |

Note

3. Tested initially and after any design or process change that may affect these parameters.

AC Electrical Characteristics ^[4]

| Parameter | Description | -12 | | -15 | | -20 | | -25 | | Unit | |
|-------------------|--|--------------|-----|-----|-----|-----|-----|-----|-----|------|----|
| | | Min | Max | Min | Max | Min | Max | Min | Max | | |
| t _{RC} | Read Cycle Time | 12 | – | 15 | – | 20 | – | 25 | – | ns | |
| t _{AA} | Address to Data Valid | – | 12 | – | 15 | – | 20 | – | 25 | ns | |
| t _{OHA} | Data Hold from Address Change | 3 | – | 3 | – | 3 | – | 3 | – | ns | |
| t _{ACE} | $\overline{\text{CE}}$ to Data Valid | – | 12 | – | 15 | – | 20 | – | 25 | ns | |
| t _{DOE} | $\overline{\text{OE}}$ to Data Valid | Ind'l/Com'l | – | 5 | – | 7 | – | 9 | – | 9 | ns |
| | | Automotive-A | – | 6 | – | – | – | – | – | – | |
| t _{LZOE} | $\overline{\text{OE}}$ to Low-Z ^[5] | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| t _{HZOE} | $\overline{\text{OE}}$ to High-Z ^[5, 6] | – | 5 | – | 7 | – | 9 | – | 9 | ns | |
| t _{LZCE} | $\overline{\text{CE}}$ to Low-Z ^[5] | 3 | – | 3 | – | 3 | – | 3 | – | ns | |
| t _{HZCE} | $\overline{\text{CE}}$ to High-Z ^[5, 6] | – | 5 | – | 7 | – | 9 | – | 9 | ns | |
| t _{PU} | $\overline{\text{CE}}$ to Power Up | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| t _{PD} | $\overline{\text{CE}}$ to Power Down | – | 12 | – | 15 | – | 20 | – | 20 | ns | |
| t _{WC} | Write Cycle Time ^[7] | 12 | – | 15 | – | 20 | – | 25 | – | ns | |
| t _{SCE} | $\overline{\text{CE}}$ to Write End | 9 | – | 10 | – | 15 | – | 15 | – | ns | |
| t _{AW} | Address Setup to Write End | 9 | – | 10 | – | 15 | – | 15 | – | ns | |
| t _{HA} | Address Hold from Write End | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| t _{SA} | Address Setup to Write Start | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| t _{PWE} | $\overline{\text{WE}}$ Pulse Width | 8 | – | 9 | – | 15 | – | 15 | – | ns | |
| t _{SD} | Data Setup to Write End | 8 | – | 9 | – | 10 | – | 10 | – | ns | |
| t _{HD} | Data Hold from Write End | 0 | – | 0 | – | 0 | – | 0 | – | ns | |
| t _{HZWE} | $\overline{\text{WE}}$ LOW to High-Z ^[5, 6] | – | 7 | – | 7 | – | 10 | – | 10 | ns | |
| t _{LZWE} | $\overline{\text{WE}}$ HIGH to Low-Z ^[5] | 3 | – | 3 | – | 3 | – | 3 | – | ns | |

Data Retention Characteristics ^[8]

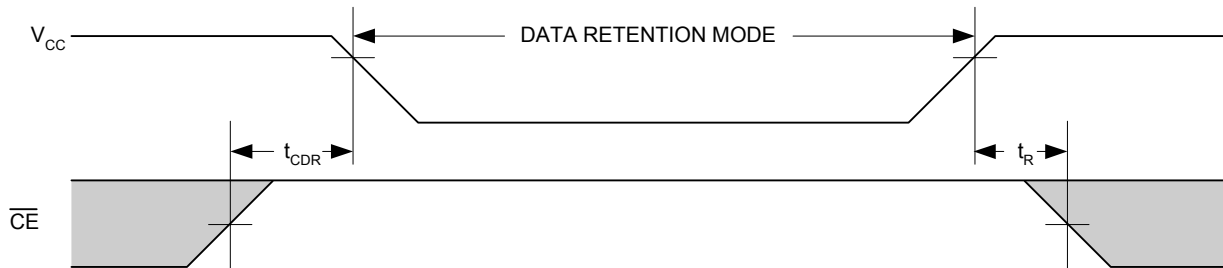
| Parameter | Description | Condition | Min | Max | Unit |
|-------------------|--------------------------------------|---|-----|-----|------|
| V _{DR} | V _{CC} for Data Retention | | 2.0 | – | V |
| I _{CCDR} | Data Retention Current | V _{CC} = V _{DR} = 2.0V, $\overline{\text{CE}} \geq V_{\text{CC}} - 0.3\text{V}$, V _{IN} ≥ V _{CC} – 0.3V or V _{IN} ≤ 0.3V | – | 150 | μA |
| t _{CDR} | Chip Deselect to Data Retention Time | | 0 | – | ns |
| t _R | Operation Recovery Time | | 200 | – | μs |

Notes

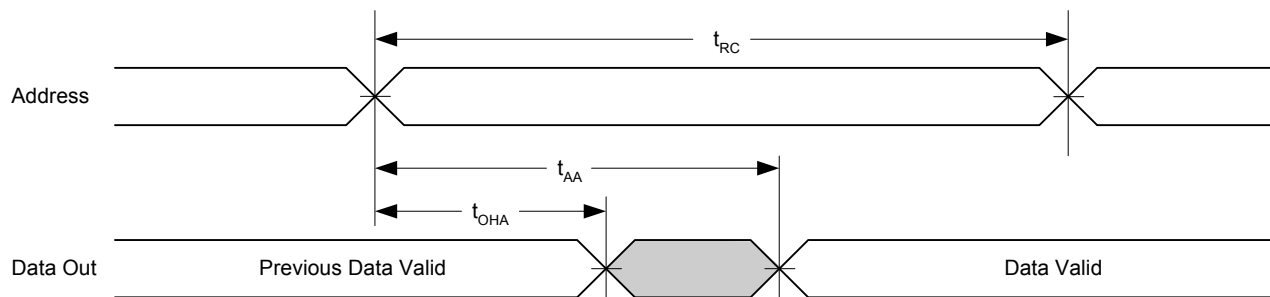
- Test Conditions are based on a transition time of 3 ns or less and timing reference levels of 1.5V, and input pulse levels of 0 to 3.0V.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE}, t_{HZCE}, t_{HZWE} are specified as in part (b) of the "" on page 1. Transitions are measured ± 200 mV from steady state voltage.
- The internal memory write time is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. $\overline{\text{CE}}$ and $\overline{\text{WE}}$ must be LOW to initiate a write, and the transition of any of these signals can terminate the write. The input data setup and hold timing must be referenced to the leading edge of the signal that terminates the write.
- L-version only.

Timing Waveforms

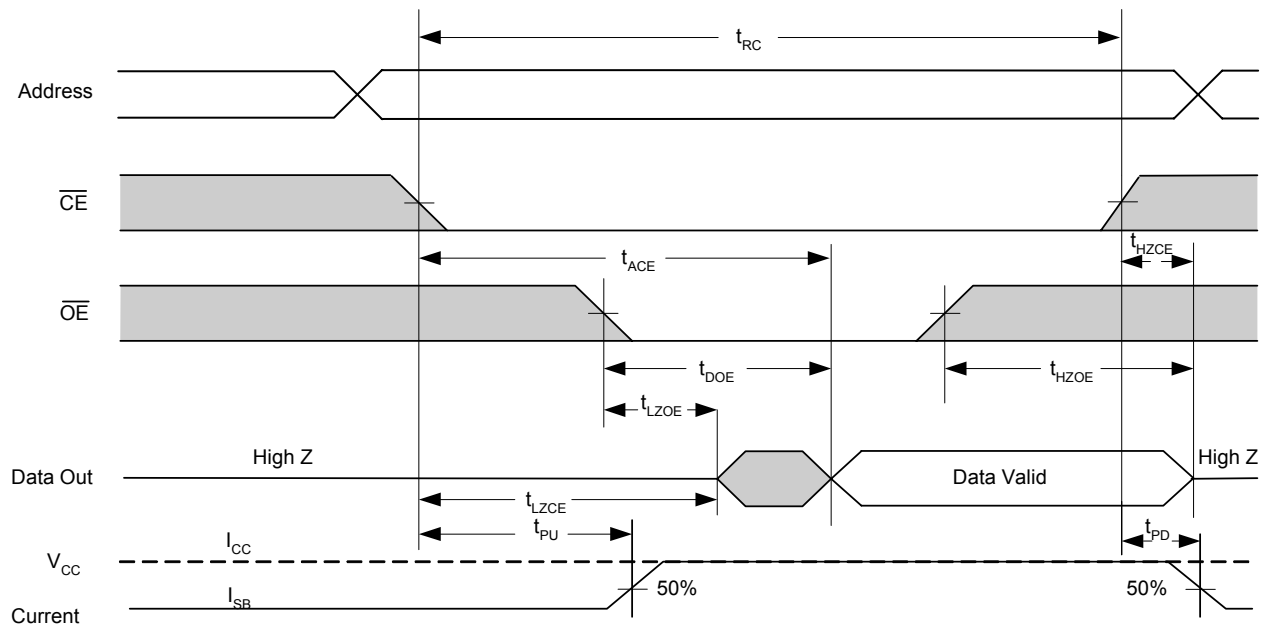
Data Retention Waveform



Read Cycle 1 [9, 10]



Read Cycle 2 [11, 12]

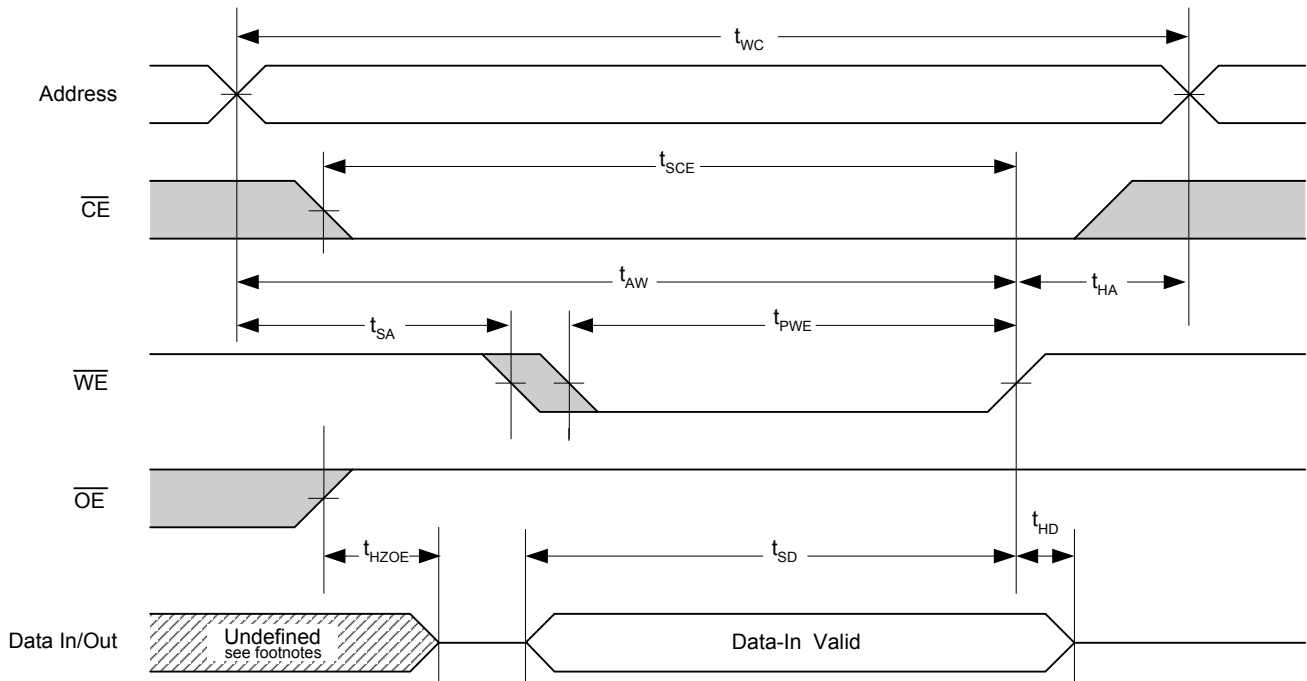


Notes

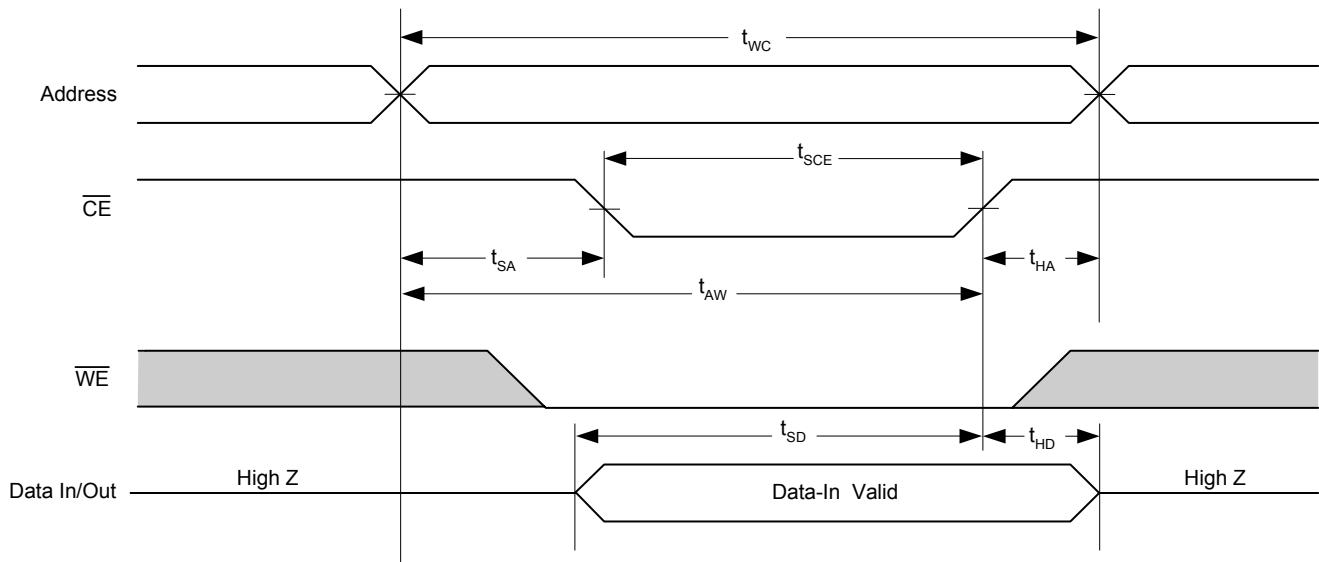
9. Device is continuously selected. $\overline{OE} = V_{IL} = \overline{CE}$.
10. \overline{WE} is HIGH for read cycle.
11. This cycle is \overline{OE} controlled and \overline{WE} is HIGH read cycle.
12. Address valid before or similar with \overline{CE} transition LOW.

Timing Waveforms (continued)

Write Cycle 1 (\overline{WE} controlled) [13, 14, 15]



Write Cycle 2 (\overline{CE} controlled) [14, 16, 17]

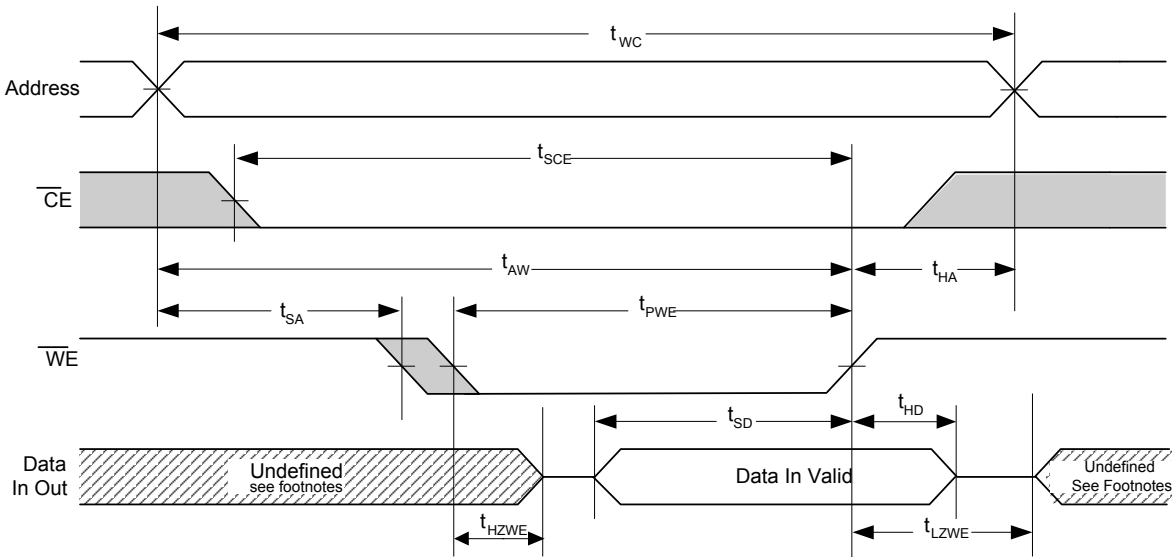


Notes

13. This cycle is \overline{WE} controlled, \overline{OE} is HIGH during write.
14. Data in and/or out is high impedance if $\overline{OE} = V_{IH}$.
15. During this period the IOs are in output state and input signals must not be applied.
16. This cycle is \overline{CE} controlled.
17. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high impedance state.

Timing Waveforms (continued)

Write Cycle 3 (\overline{WE} controlled, \overline{OE} low) [18]



Note

18. The cycle is \overline{WE} controlled, \overline{OE} LOW. The minimum write cycle time is the sum of t_{HZWE} and t_{SD} .

Ordering Information

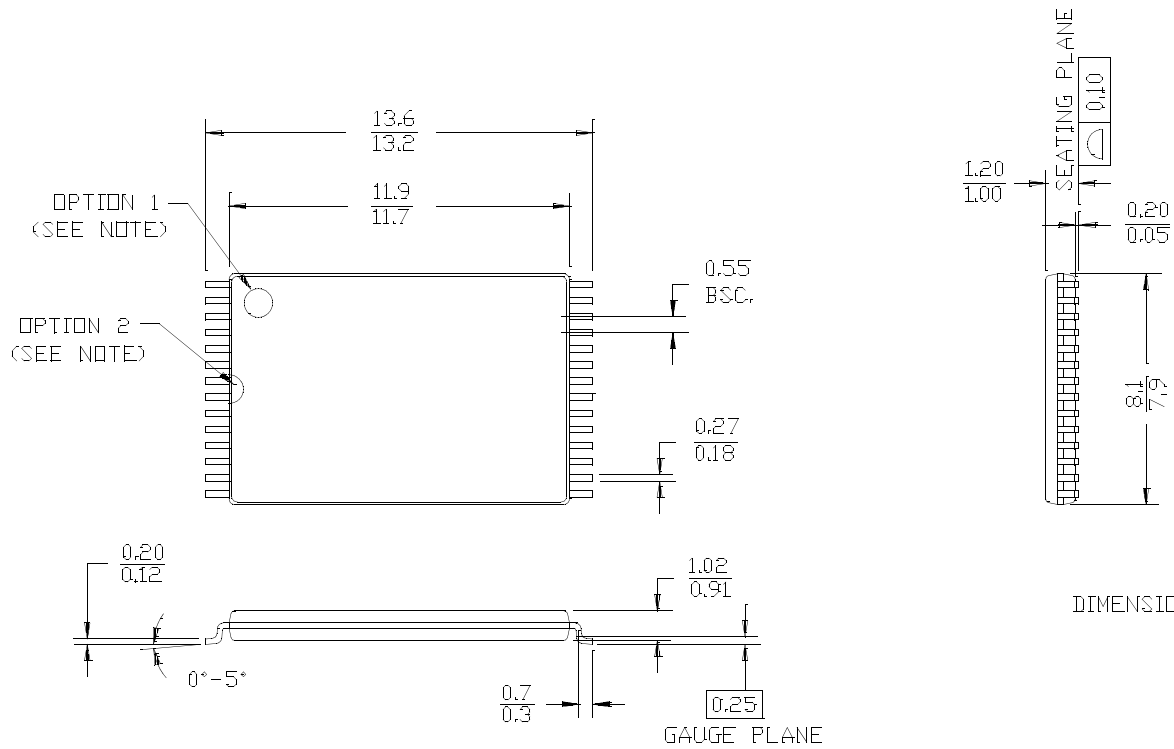
Contact local sales representative regarding availability of these parts.

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Power Option | Operating Range |
|------------|------------------|-----------------|---------------------------------------|--------------|-----------------|
| 12 | CY7C199CN-12VC | 51-85031 | 28-Lead (300-Mil) Molded SOJ | Standard | Commercial |
| | CY7C199CN-12ZC | 51-85071 | 28 TSOP I (8 x 13.4 mm) | Standard | Commercial |
| | CY7C199CN-12ZXC | 51-85071 | 28 TSOP I (8 x 13.4 mm), Pb-free | Standard | Commercial |
| | CY7C199CN-12VI | 51-85031 | 28-Lead (300-Mil) Molded SOJ | Standard | Industrial |
| | CY7C199CN-12VXI | 51-85031 | 28-Lead (300-Mil) Molded SOJ, Pb-free | Standard | Industrial |
| | CY7C199CN-12VXA | 51-85031 | 28-Lead (300-Mil) Molded SOJ, Pb-free | Standard | Automotive-A |
| 15 | CY7C199CN-15PC | 51-85014 | 28 DIP (6.9 x 35.6 x 3.5 mm) | Standard | Commercial |
| | CY7C199CN-15PXC | 51-85014 | 28 DIP (6.9 x 35.6 x 3.5 mm), Pb-free | Standard | Commercial |
| | CY7C199CN-15VC | 51-85031 | 28-Lead (300-Mil) Molded SOJ | Standard | Commercial |
| | CY7C199CN-15VXC | 51-85031 | 28-Lead (300-Mil) Molded SOJ, Pb-free | Standard | Commercial |
| | CY7C199CN-15ZC | 51-85071 | 28 TSOP I (8 x 13.4 mm), Pb-free | Standard | Commercial |
| | CY7C199CN-15ZXC | 51-85071 | 28 TSOP I (8 x 13.4 mm), Pb-free | Standard | Commercial |
| | CY7C199CN-15VI | 51-85031 | 28-Lead (300-Mil) Molded SOJ | Standard | Industrial |
| | CY7C199CNL-15VC | 51-85031 | 28-Lead (300-Mil) Molded SOJ | Low Power | Commercial |
| | CY7C199CNL-15VXC | 51-85031 | 28-Lead (300-Mil) Molded SOJ, Pb-free | Low Power | Commercial |
| | CY7C199CNL-15ZXC | 51-85071 | 28 TSOP I (8 x 13.4 mm), Pb-free | Low Power | Commercial |
| | CY7C199CNL-15VXI | 51-85031 | 28-Lead (300-Mil) Molded SOJ, Pb-free | Low Power | Industrial |
| 20 | CY7C199CN-20VC | 51-85031 | 28-Lead (300-Mil) Molded SOJ | Standard | Commercial |
| | CY7C199CN-20ZI | 51-85071 | 28 TSOP I (8 x 13.4 mm) | Standard | Industrial |
| | CY7C199CN-20ZXI | 51-85071 | 28 TSOP I (8 x 13.4 mm), Pb-free | Standard | Industrial |
| 25 | CY7C199CN-25PC | 51-85014 | 28 DIP (6.9 x 35.6 x 3.5 mm) | Standard | Commercial |
| | CY7C199CN-25PXC | 51-85014 | 28 DIP (6.9 x 35.6 x 3.5 mm), Pb-free | Standard | Commercial |

Package Diagrams

Figure 1. 28-pin TSOP I (8 x 13.4 mm), 51-85071

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

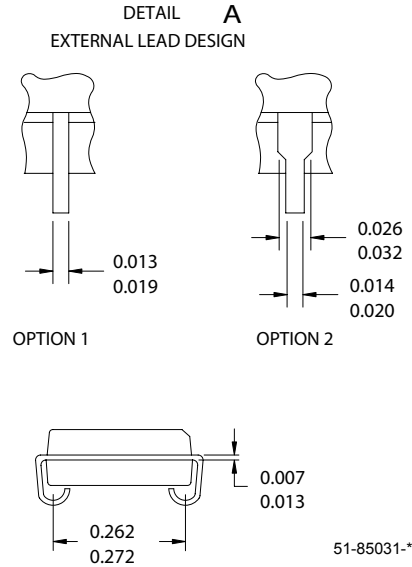
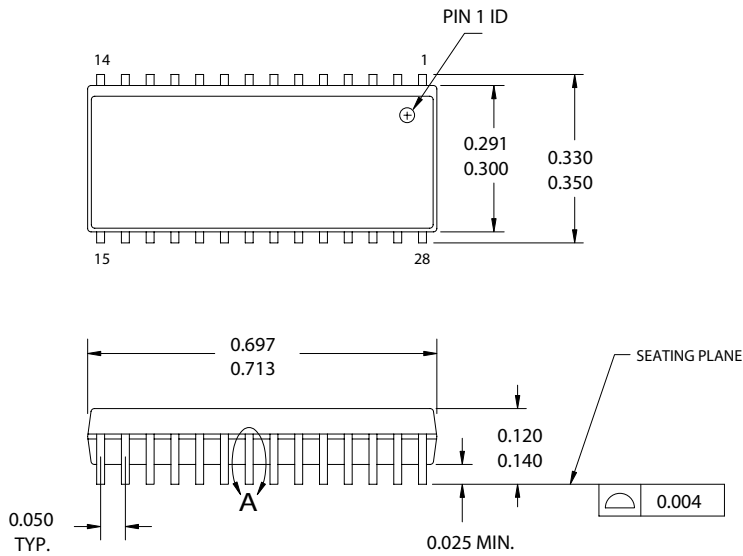


Package Diagrams (continued)

Figure 2. 28-pin (300 Mil) Molded SOJ, 51-85031

NOTE :

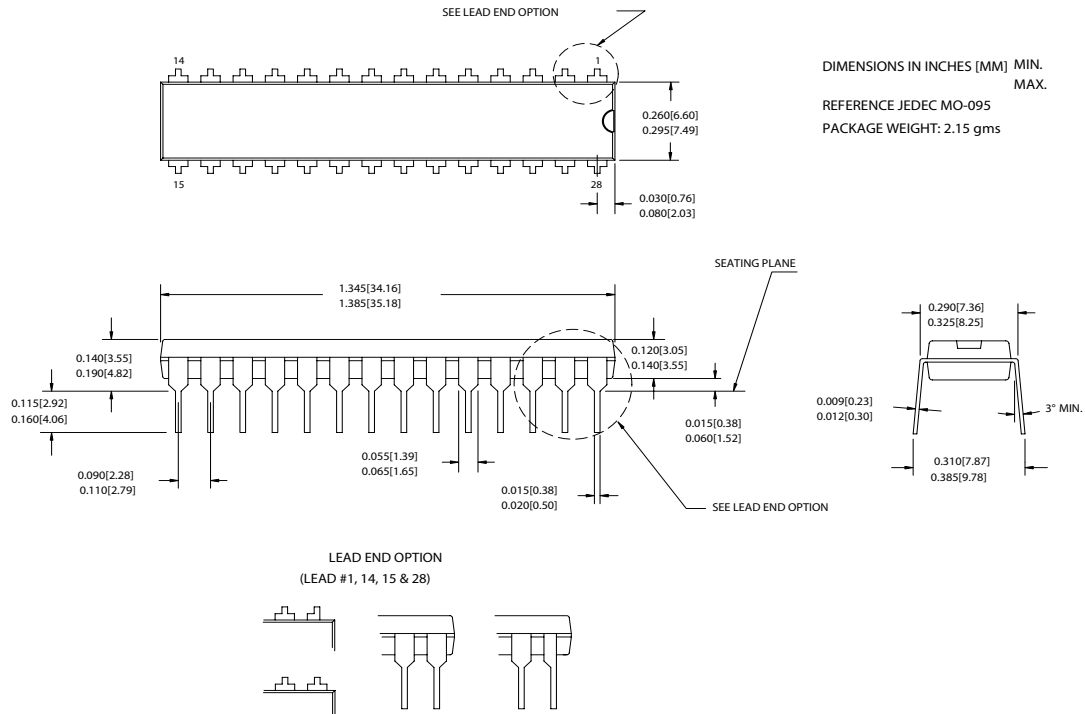
1. JEDEC STD REF MO088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES



51-85031-°C

Package Diagrams (continued)

Figure 3. 28-pin (300 Mil) PDIP, 51-85014



51-85014-*D

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Document History Page

| Document Title: CY7C199CN, 256K (32K x 8) Static RAM Document Number: 001-06435 | | | | |
|--|---------|------------|-----------------|---|
| REV. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 430363 | See ECN | NXR | New Data Sheet |
| *A | 684342 | See ECN | VKN | Added Automotive-A Information Updated Ordering Information Table |
| *B | 839904 | See ECN | VKN | Added t_{DOE} spec for Automotive-A part in AC Electrical characteristics table |

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