



**THE DATASHEET OF**  
**5V41064NLG8**



# 1 OUTPUT PCIE GEN1/2 SYNTHESIZER

IDT5V41064

## Recommended Applications

One output synthesizer for PCIe Gen1/2

## General Description

The IDT5V41064 is a PCIe Gen2 compliant spread spectrum capable clock generator. The device has 1 differential HCSL output and can be used in communication or embedded systems to substantially reduce electro-magnetic interference (EMI). Spread spectrum can be enabled via a select pin.

## Output Features

- 1 - 0.7V current mode differential HCSL output pairs

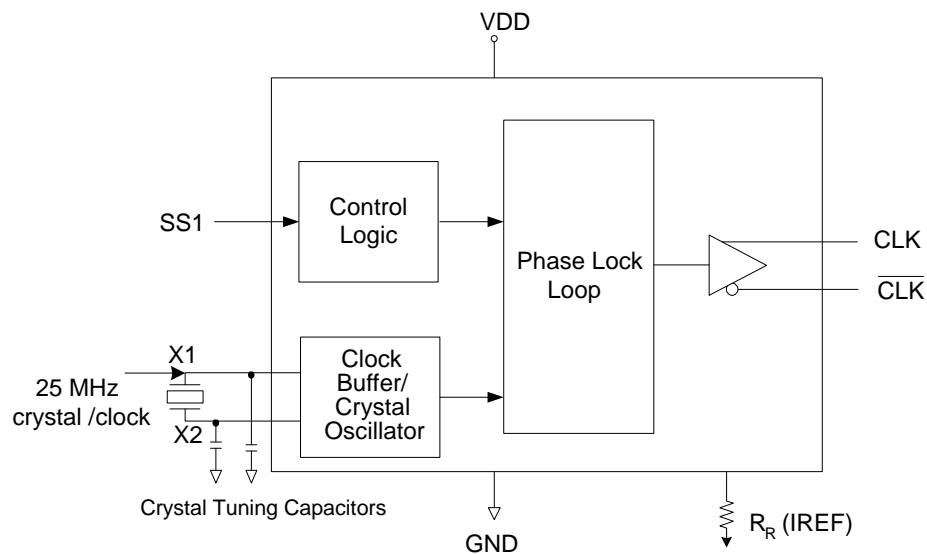
## Features/Benefits

- 16-pin QFN package; very small board footprint
- Spread-spectrum capable; reduces EMI
- Outputs can be terminated to LVDS; can drive a wider variety of devices
- Spread enable via pin selection; no software required to configure device
- Industrial temperature range available; supports demanding embedded applications
- **For PCIe Gen3 applications, see the 5V41234**

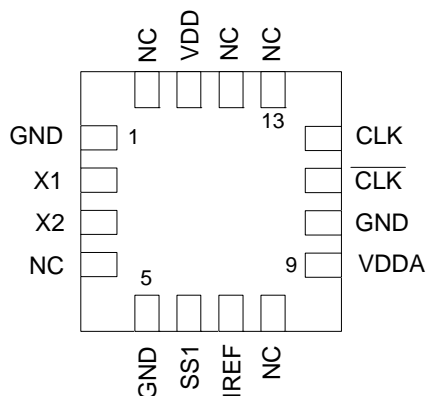
## Key Specifications

- Cycle-to-cycle jitter < 100 ps
- PCIe Gen2 phase jitter < 3.0ps RMS

## Block Diagram



## Pin Assignment



16-pin QFN

## Spread Spectrum Select Table

| SS1 | Spread%    |
|-----|------------|
| 0   | -0.5% down |
| 1   | No spread  |

## Pin Descriptions

| Pin Number | Pin Name | Pin Type | Pin Description   |
|------------|----------|----------|---|
| 1          | GND      | Power    | Connect to ground.  |
| 2          | X1       | XI       | Crystal or clock input. Connect to 25 MHz crystal or single-ended clock.                                    |
| 3          | X2       | XO       | Crystal connection. Connect to parallel mode crystal. Leave floating if X1 is driven by single-ended clock. |
| 4          | NC       | –        | No connect.   |
| 5          | GND      | Power    | Connect to ground.  |
| 6          | SS1      | Input    | Spread Select 1. See table above. Internal pull-up resistor.  |
| 7          | IREF     | Output   | 475Ω precision resistor must be attached to this pin, which is connected to internal current source.        |
| 8          | NC       | –        | No connect.   |
| 9          | VDDA     | Power    | Connect to 3.3V and filter as analog supply.  |
| 10         | GND      | Power    | Connect to ground.  |
| 11         | CLK      | Output   | HCSL complementary output clock.  |
| 12         | CLK      | Output   | HCSL true output clock.   |
| 13         | NC       | –        | No connect.   |
| 14         | NC       | –        | No connect.   |
| 15         | VDD      | Power    | Connect to 3.3 V for OSC and digital circuits.  |
| 16         | NC       | –        | No connect.   |

## Applications Information

### External Components

A minimum number of external components are required for proper operation.

### Decoupling Capacitors

Decoupling capacitors of 0.01  $\mu\text{F}$  should be connected between VDD and the ground plane (pin 4) as close to the VDD pin as possible. Do not share ground vias between components. Route power from power source through the capacitor pad and then into IDT pin.

### Crystal

A 25 MHz fundamental mode parallel resonant crystal with  $C_L = 16$  pF should be used. This crystal must have less than 300 ppm of error across temperature in order for the IDT5V41064 to meet PCI Express specifications.

### Crystal Capacitors

Crystal capacitors are connected from pins X1 to ground and X2 to ground to optimize the accuracy of the output frequency.

$C_L$  = Crystal's load capacitance in pF

Crystal Capacitors (pF) =  $(C_L - 8) * 2$

For example, for a crystal with a 16 pF load cap, each external crystal cap would be 16 pF.  $(16-8)*2=16$ .

Current Source (Iref) Reference Resistor -  $R_R$

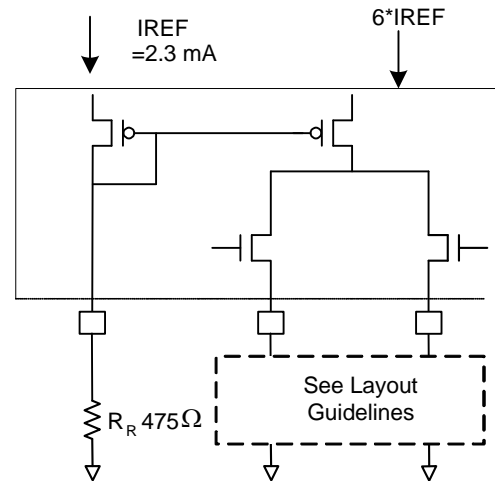
If board target trace impedance (Z) is 50 $\Omega$ , then  $R_R = 475\Omega$  (1%), providing IREF of 2.32 mA. The output current ( $I_{OH}$ ) is equal to 6\*IREF.

### Output Termination

The PCI-Express differential clock outputs of the IDT5V41064 are open source drivers and require an external series resistor and a resistor to ground. These resistor values and their allowable locations are shown in detail in the **PCI-Express Layout Guidelines** section.

The IDT5V41064 can also be terminated to LVDS compatible voltage levels. See Layout Guidelines section.

## Output Structures



### General PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

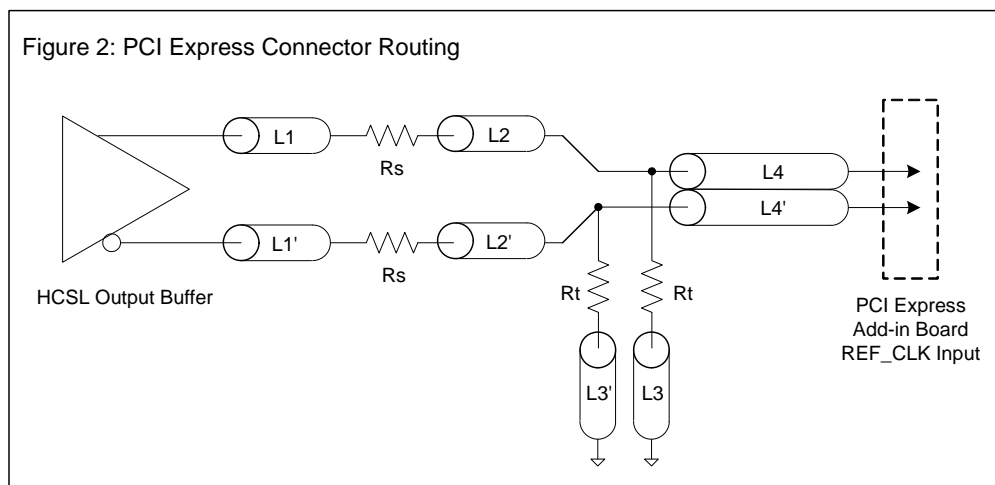
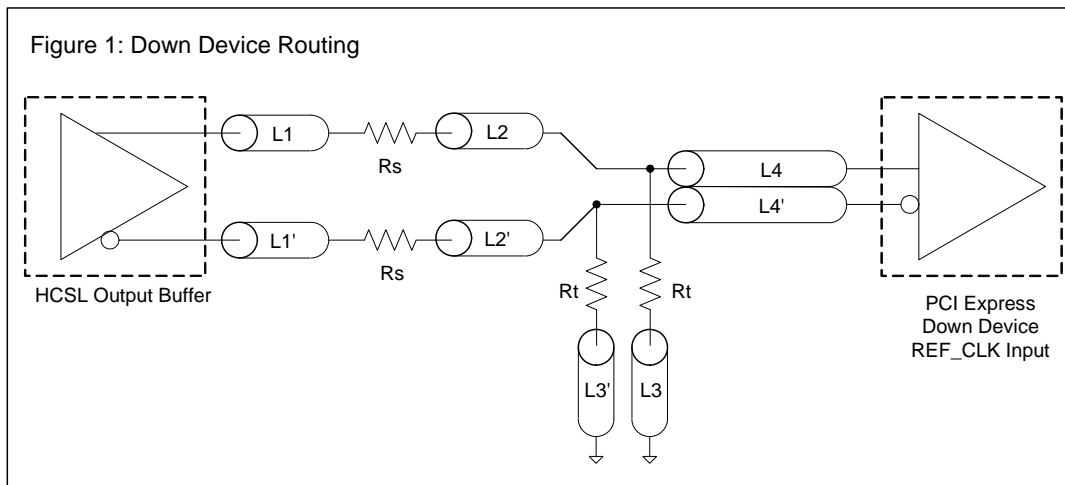
1. Each 0.01 $\mu\text{F}$  decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible.
2. No vias should be used between decoupling capacitor and VDD pin.
3. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via. Distance of the ferrite bead and bulk decoupling from the device is less critical.
4. An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers (any ferrite beads and bulk decoupling capacitors can be mounted on the back). Other signal traces should be routed away from the IDT5V41064. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

## Layout Guidelines for PCI Express

| PCIe Reference Clock                            |                    |      |        |
|---|--------------------|------|--------|
| Common Recommendations for Differential Routing | Dimension or Value | Unit | Figure |
| L1 length, route as non-coupled 50ohm trace     | 0.5 max            | inch | 1      |
| L2 length, route as non-coupled 50ohm trace     | 0.2 max            | inch | 1      |
| L3 length, route as non-coupled 50ohm trace     | 0.2 max            | inch | 1      |
| Rs  | 33                 | ohm  | 1      |
| Rt  | 49.9               | ohm  | 1      |

| Down Device Differential Routing                                 |                     |      |   |
|--|---------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 2 min to 16 max     | inch | 1 |
| L4 length, route as coupled stripline 100ohm differential trace  | 1.8 min to 14.4 max | inch | 1 |

| Differential Routing to PCI Express Connector                    |                       |      |   |
|--|-----------------------|------|---|
| L4 length, route as coupled microstrip 100ohm differential trace | 0.25 to 14 max        | inch | 2 |
| L4 length, route as coupled stripline 100ohm differential trace  | 0.225 min to 12.6 max | inch | 2 |



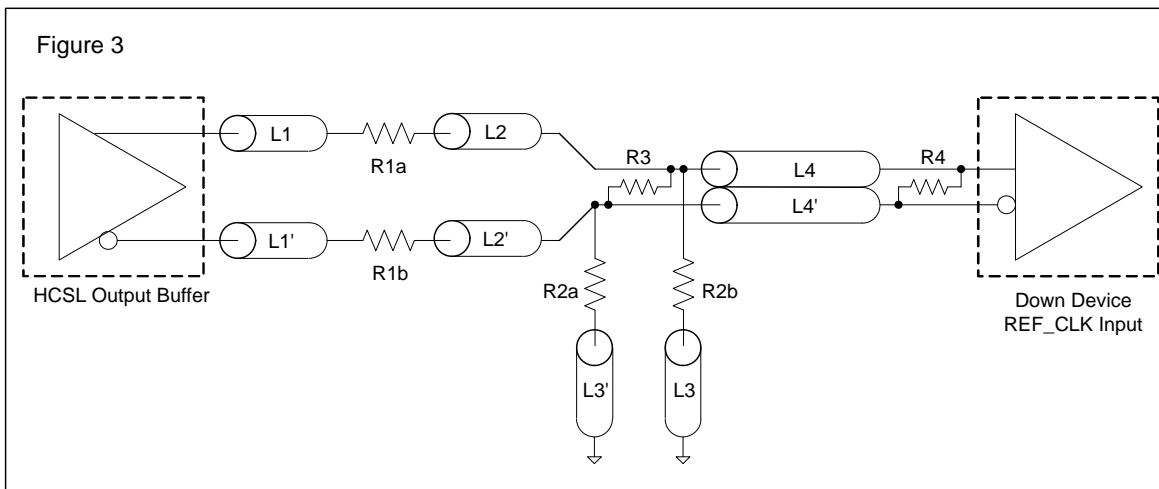
### Layout Guidelines for LVDS and Other Applications

**Alternative Termination for LVDS and other Common Differential Signals (figure 3)**

| Vdiff | Vp-p  | Vcm  | R1 | R2   | R3   | R4  | Note                           |
|-------|-------|------|----|------|------|-----|--------------------------------|
| 0.45v | 0.22v | 1.08 | 33 | 150  | 100  | 100 |                                |
| 0.58  | 0.28  | 0.6  | 33 | 78.7 | 137  | 100 |                                |
| 0.80  | 0.40  | 0.6  | 33 | 78.7 | none | 100 | ICS874003i-02 input compatible |
| 0.60  | 0.3   | 1.2  | 33 | 174  | 140  | 100 | Standard LVDS                  |

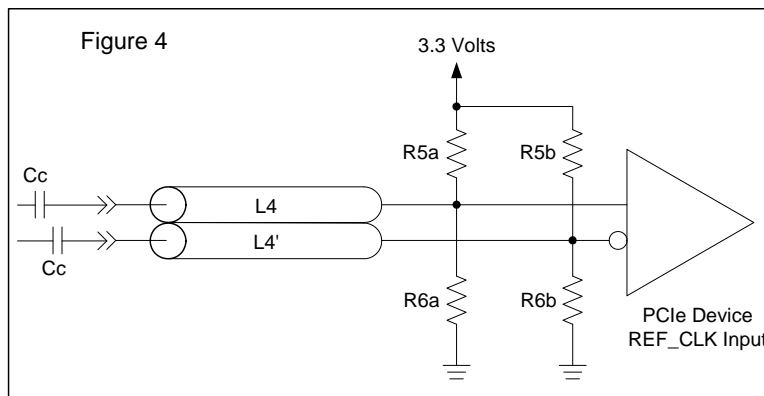
R1a = R1b = R1

R2a = R2b = R2

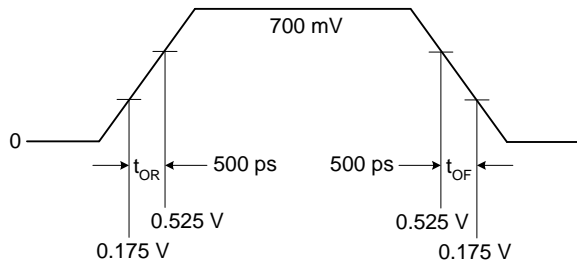


**Cable Connected AC Coupled Application (figure 4)**

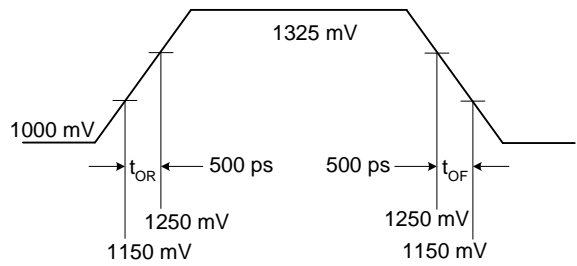
| Component | Value       | Note |
|-----------|-------------|------|
| R5a, R5b  | 8.2K 5%     |      |
| R6a, R6b  | 1K 5%       |      |
| Cc        | 0.1 $\mu$ F |      |
| Vcm       | 0.350 volts |      |



### Typical PCI-Express (HCSL) Waveform



### Typical LVDS Waveform



## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the IDT5V41064. These ratings are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item                                       | Rating              |
|--|---------------------|
| Supply Voltage, VDD, VDDA                  | 5.5 V               |
| All Inputs and Outputs                     | -0.5 V to VDD+0.5 V |
| Ambient Operating Temperature (commercial) | 0 to +70°C          |
| Ambient Operating Temperature (industrial) | -40 to +85°C        |
| Storage Temperature                        | -65 to +150°C       |
| Junction Temperature                       | 125°C               |
| Soldering Temperature                      | 260°C               |
| ESD Protection (Input)                     | 2000 V min. (HBM)   |

## DC Electrical Characteristics

Unless stated otherwise, VDD = 3.3 V  $\pm$ 5%, Ambient Temperature -40 to +85°C

| Parameter                          | Symbol           | Conditions                | Min.    | Typ. | Max.     | Units      |
|------------------------------------|------------------|---------------------------|---------|------|----------|------------|
| Supply Voltage                     | V                |                           | 3.135   |      | 3.465    |            |
| Input High Voltage <sup>1</sup>    | V <sub>IH</sub>  |                           | 2.2     |      | VDD +0.3 | V          |
| Input Low Voltage <sup>1</sup>     | V <sub>IL</sub>  |                           | VSS-0.3 |      | 0.8      | V          |
| Input Leakage Current <sup>2</sup> | I <sub>IL</sub>  | 0 < V <sub>in</sub> < VDD | -5      |      | 5        | $\mu$ A    |
| Operating Supply Current           | I <sub>DD</sub>  | 2 pF load                 |         |      | 70       | mA         |
| Input Capacitance                  | C <sub>IN</sub>  | Input pin capacitance     |         |      | 7        | pF         |
| Output Capacitance                 | C <sub>OUT</sub> | Output pin capacitance    |         |      | 6        | pF         |
| Pin Inductance                     | L <sub>PIN</sub> |                           |         |      | 5        | nH         |
| Output Resistance                  | R <sub>out</sub> | CLK outputs               | 3.0     |      |          | k $\Omega$ |
| Pull-up Resistor                   | R <sub>PUP</sub> | SS1                       |         | 100  |          | k $\Omega$ |

1 Single edge is monotonic when transitioning through region.

2 Inputs with pull-ups/-downs are not included.

## AC Electrical Characteristics - CLK/CLK

Unless stated otherwise, VDD=3.3 V ±5%, Ambient Temperature -40 to +85°C

| Parameter                               | Symbol              | Conditions                          | Min. | Typ. | Max. | Units |
|---|---------------------|-------------------------------------|------|------|------|-------|
| Input Frequency                         |                     |                                     |      | 25   |      | MHz   |
| Output Frequency                        |                     |                                     |      | 100  |      | MHz   |
| Output High Voltage <sup>1,2</sup>      | V <sub>OH</sub>     |                                     | 660  | 700  | 850  | mV    |
| Output Low Voltage <sup>1,2</sup>       | V <sub>OL</sub>     |                                     | -150 | 27   | 150  | mV    |
| Crossing Point Voltage <sup>1,2</sup>   |                     | Absolute                            | 250  | 350  | 550  | mV    |
| Crossing Point Voltage <sup>1,2,4</sup> |                     | Variation over all edges            |      | 40   | 140  | mV    |
| Jitter, Cycle-to-Cycle <sup>1,3</sup>   |                     |                                     |      | 25   | 100  | ps    |
| Rise Time <sup>1,2</sup>                | t <sub>OR</sub>     | From 0.175 V to 0.525 V             | 175  | 332  | 700  | ps    |
| Fall Time <sup>1,2</sup>                | t <sub>OF</sub>     | From 0.525 V to 0.175 V             | 175  | 344  | 700  | ps    |
| Rise/Fall Time Variation <sup>1,2</sup> |                     |                                     |      | 75   | 125  | ps    |
| Duty Cycle <sup>1,3</sup>               |                     |                                     | 45   | 51   | 55   | %     |
| Stabilization Time                      | t <sub>STABLE</sub> | From power-up VDD=3.3 V             |      | 1.2  | 3.0  | ms    |
| Spread Change Time                      | t <sub>SPREAD</sub> | Settling period after spread change |      | 3.0  |      | ms    |

<sup>1</sup> Test setup is R<sub>S</sub>=33 ohms R<sub>P</sub>=50 ohms with 2 pF, R<sub>R</sub> = 475Ω (1%).

<sup>2</sup> Measurement taken from a single-ended waveform.

<sup>3</sup> Measurement taken from a differential waveform.

<sup>4</sup> Measured at the crossing point where instantaneous voltages of both CLK and  $\overline{\text{CLK}}$  are equal.

## Electrical Characteristics - Differential Phase Jitter

| Parameter     | Symbol                  | Conditions                                | Min | Typ | Max | Units    | Notes |
|---------------|-------------------------|---|-----|-----|-----|----------|-------|
| Jitter, Phase | t <sub>jphasePLL</sub>  | PCIe Gen1                                 |     | 30  | 86  | ps (p-p) | 1,2,3 |
|               | t <sub>jphaseLO</sub>   | PCIe Gen2, 10 kHz < f < 1.5 MHz           |     | 1.2 | 3   | ps (RMS) | 1,2,3 |
|               | t <sub>jphaseHIGH</sub> | PCIe Gen2, 1.5 MHz < f < Nyquist (50 MHz) |     | 1.9 | 3.1 | ps (RMS) | 1,2,3 |

Note 1. Guaranteed by design and characterization, not 100% tested in production.

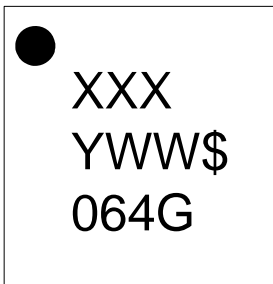
Note 2. See <http://www.pcisig.com> for complete specs.

Note 3: Applies to 100MHz, spread off and 0.5% down spread only.

## Thermal Characteristics

| Parameter                              | Symbol          | Conditions     | Min. | Typ. | Max. | Units |
|--|-----------------|----------------|------|------|------|-------|
| Thermal Resistance Junction to Ambient | θ <sub>JA</sub> | Still air      |      | 63.2 |      | °C/W  |
|  | θ <sub>JA</sub> | 1 m/s air flow |      | 55.9 |      | °C/W  |
|  | θ <sub>JA</sub> | 2 m/s air flow |      | 53.1 |      | °C/W  |
|  | θ <sub>JA</sub> | 3 m/s air flow |      | 51.4 |      | °C/W  |
| Thermal Resistance Junction to Case    | θ <sub>JC</sub> |                |      | 65.8 |      | °C/W  |

## Marking Diagrams

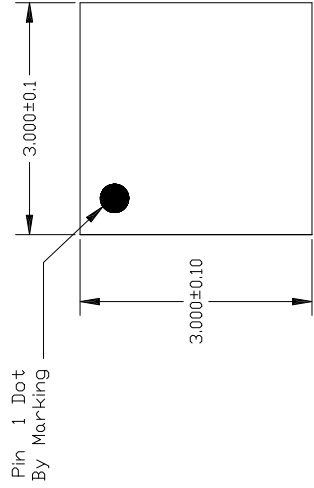


### Notes:

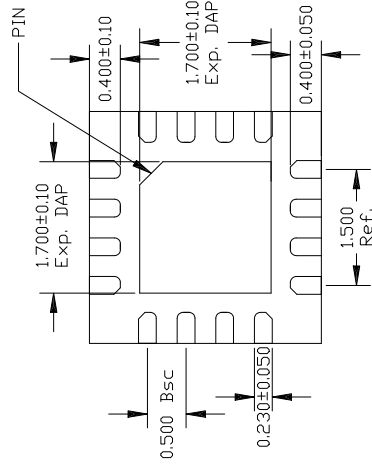
1. Line 1: 'XXX' is the lot traceability (last numeric character of the assembly lot number).
2. Line 2: 'YYW' – Date code; '\$' – Assembly location.
3. Line 3: truncated IDT part number.
4. "G" designates RoHS compliant package.
5. "I" within the part number indicates industrial temperature range.

| REVISIONS |                           |
|-----------|---------------------------|
| REV       | DESCRIPTION               |
| 00        | INITIAL RELEASE           |
| 01        | COMBINE P0D & LAND PATTIE |

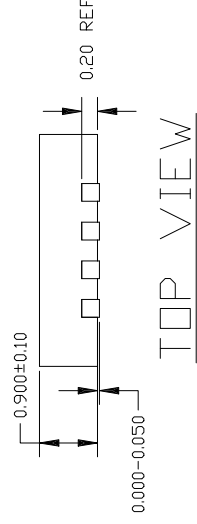
PIN #1 IDENTIFICATION



TOP VIEW



BOTTOM VIEW



TOP VIEW

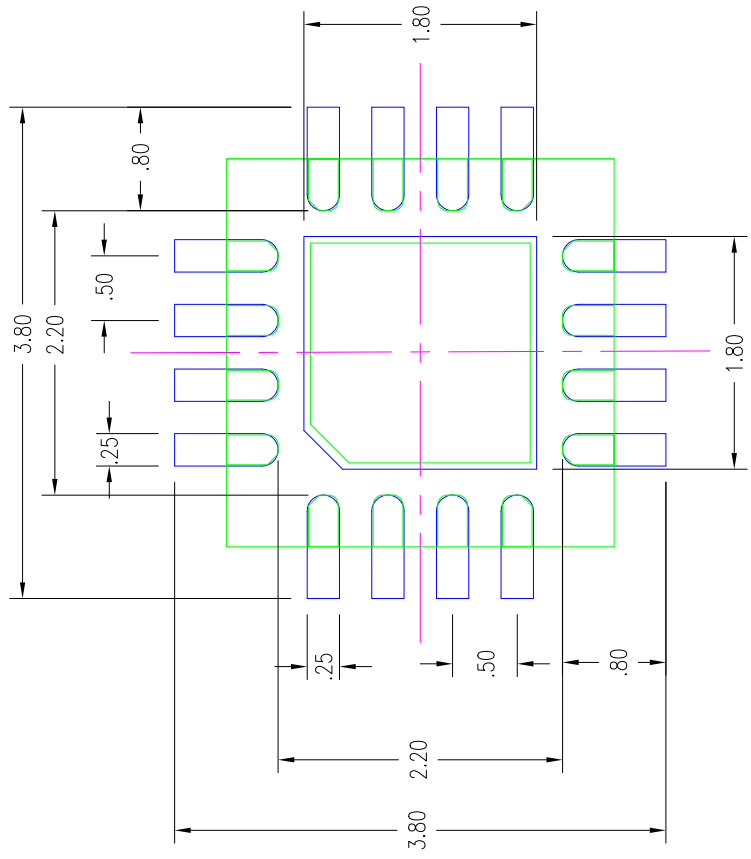
16LD QFN 3X3 (0.5MM PITCH)

|                             |         |                      |
|-----------------------------|---------|----------------------|
| TOLERANCES UNLESS SPECIFIED | DECIMAL | ±                    |
|                             | ANGULAR | ±                    |
| APPROVALS                   | DATE    | TITLE                |
| DRAWN /24C/12/15/08         |         | NI/NIG/1             |
| CHECKED                     |         | 3.0 x 3.0            |
|                             |         | 0.5 mm               |
|                             |         | SIZE                 |
|                             |         | C                    |
|                             |         | DRAWING No.          |
|                             |         | P                    |
|                             |         | DO NOT SCALE DRAWING |



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| REVISIONS |                            |
|-----------|----------------------------|
| REV       | DESCRIPTION                |
| 00        | INITIAL RELEASE            |
| 01        | COMBINE POD & LAND PATTERN |



NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW: AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

|   |           |          |                   |
|---|-----------|----------|-------------------|
| TOLERANCES UNLESS SPECIFIED IN DECIMAL PLACES | APPROVALS | DATE     | TITLE             |
|   | XXXX      | 10/15/08 | NU/NG16           |
| XXXX  | CHECKED   |          | 3.0 x 3.0         |
| XXXX  |           |          | 0.5 mm P          |
|   |           |          | SIZE              |
|   |           |          | DRAWING No.       |
|   |           |          | C                 |
|   |           |          | P                 |
|   |           |          | DO NOT SCALE DRAW |

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## Ordering Information

| Part / Order Number | Marking    | Shipping Packaging | Package    | Temperature   |
|---------------------|------------|--------------------|------------|---------------|
| 5V41064NLG          | See Page 9 | Trays              | 16-pin QFN | 0 to +70° C   |
| 5V41064NLG8         |            | Tape and Reel      | 16-pin QFN | 0 to +70° C   |
| 5V41064NLGI         |            | Trays              | 16-pin QFN | -40 to +85° C |
| 5V41064NLGI8        |            | Tape and Reel      | 16-pin QFN | -40 to +85° C |

“G” after the two-letter package code are the Pb-Free configuration and are RoHS compliant.

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## Revision History

| Rev. | Originator | Date     | Description of Change   |
|------|------------|----------|---|
| A    |            | 04/01/08 | Initial release - preliminary.  |
| B    | RW         | 03/02/10 | 1. Updated Title and Features bullets<br>2. Added Differential Phase Jitter table<br>3. Updated Cycle-to-cycle Jitter spec from 80ps to 125ps   |
| C    | RDW        | 06/18/10 | 1. Updated package and pinout to 16QFN.<br>2. Added Spread Spectrum.  |
| D    | RDW        | 07/19/10 | 1. Updated title and general description<br>2. Updated cycle-to-cycle jitter spec from 125 to 100 ps  |
| E    | RDW        | 12/21/10 | 1. Minor corrections<br>2. Updated with Typical data<br>3. Released to final  |
| F    | RDW        | 10/28/11 | Updated Thermal char data   |
| G    | RDW        | 11/21/11 | 1. Changed title to “1 Output PCIe GEN1/2 Synthesizer”<br>2. Added note to Features section: “For PCIe Gen3 applications, see 5V41234”<br>3. Updated Differential Phase Jitter table. |
| H    | RDW        | 10/07/13 | Updated VOH min and VOL max values in AC Char table.  |
| J    | C.P.       | 04/17/17 | Replaced package outline drawings with latest NLG16 drawings.   |

IDT5V41064

1 OUTPUT PCIE GEN1/2 SYNTHESIZER

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