



**THE DATASHEET OF  
STB80NE03L-06T4**





## STB80NE03L-06

N-channel 30V - 0.005 $\Omega$  - 85A - D<sup>2</sup>PAK  
STripFET™ Power MOSFET

### General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STB80NE03L-06	30V	<0.006 $\Omega$	80A

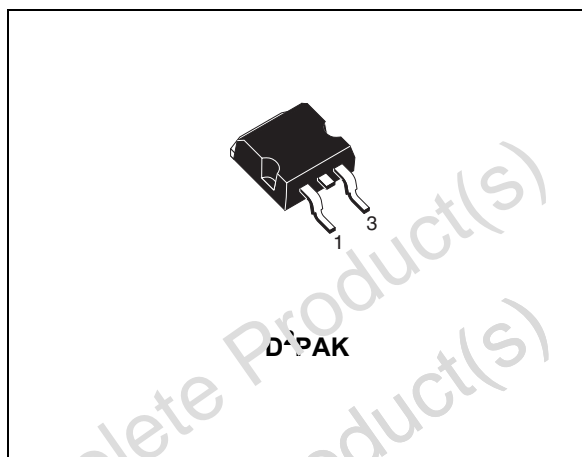
- Exceptional dv/dt capability
- Low gate charge 100°C
- 100% Avalanche tested

### Description

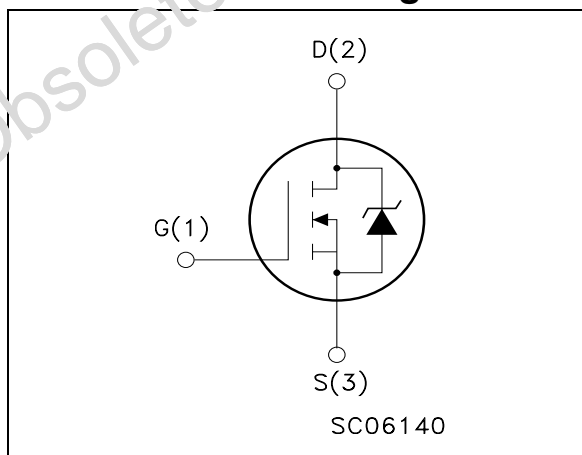
This Power MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### Applications

- Switching application



### Internal schematic diagram



### Order codes

Part number	Marking	Package	Packaging
STB80NE03L-06	B80NE03L	D <sup>2</sup> PAK	Tape & reel

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{DGR}$	Drain-gate voltage ( $R_{GS} = 20\text{ k}\Omega$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	80	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	60	A
$I_{DM}^{(1)}$	Drain current (pulsed)	320	A
	Derating factor	1	
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	150	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	7	V/ns
$T_J$	Operating junction temperature	-55 to 175	$^\circ\text{C}$
$T_{stg}$	Storage temperature		

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 20\text{A}$ ,  $di/dt \leq 100\text{A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 2. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thJC}$	Thermal resistance junction-case Max	1	$^\circ\text{C}/\text{W}$
$R_{thJA}$	Thermal resistance junction-ambient Max	62.5	$^\circ\text{C}/\text{W}$
	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 3. Avalanche characteristics**

Symbol	Parameter	Max Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_J$ max)	80	A
$E_{AS}$	Single pulse avalanche energy (starting $T_J=25^\circ\text{C}$ , $I_d=I_{AR}$ , $V_{dd}=50\text{V}$ )	600	mJ

## 2 Electrical characteristics

(T<sub>CASE</sub> = 25°C unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 250µA, V <sub>GS</sub> = 0	30			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max rating, V <sub>DS</sub> = Max rating @ 125°C			1 10	µA µA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>DS</sub> = ± 20V			± 1.00	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250µA	1	1.7	2.5	V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 40A V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 40A		0.005	0.006 0.008	Ω Ω

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 40A	30	50		S
C <sub>iss</sub>	Input capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		6500		pF
C <sub>oss</sub>	Output capacitance			1500		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			500		pF
Q <sub>g</sub>	Total gate charge	V <sub>DD</sub> = 24 V, I <sub>D</sub> = 80A, V <sub>GS</sub> = 5V		95	130	nC
Q <sub>gs</sub>	Gate-source charge			30		nC
Q <sub>gd</sub>	Gate-drain charge			44		nC

<sup>(1)</sup> Pulsed: pulse duration = 300µs, duty cycle 1.5%

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t <sub>d(on)</sub>	Turn-on delay time	V <sub>DD</sub> = 15 V, I <sub>D</sub> = 40 A R <sub>G</sub> = 4.7Ω V <sub>GS</sub> = 4.5 V <i>Figure 12.</i>		40	55	ns
t <sub>r</sub>	Rise time			260	350	ns
t <sub>r(Voff)</sub>	Off-voltage rise time	V <sub>DD</sub> = 24 V, I <sub>D</sub> = 80 A, R <sub>G</sub> = 4.7Ω V <sub>GS</sub> = 5V <i>Figure 12.</i>		70	95	ns
t <sub>f</sub>	Fall time			165	220	ns
t <sub>c</sub>	Cross over time			250	340	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				80	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				320	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 80A, V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 80 A,$ $di/dt = 100A/\mu s, V_{DD} = 15$ $V, T_J = 150^\circ C$ <i>Figure 15.</i>		75		ns
$Q_{rr}$	Reverse recovery charge			0.14		nC
$I_{RRM}$	Reverse recovery current			4		A

1. Pulse with limited by safe operating area
2. Pulsed: pulse duration = 300 $\mu$ s, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

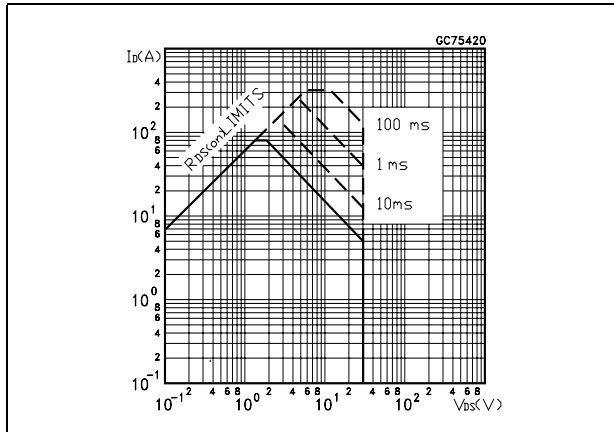


Figure 2. Thermal impedance

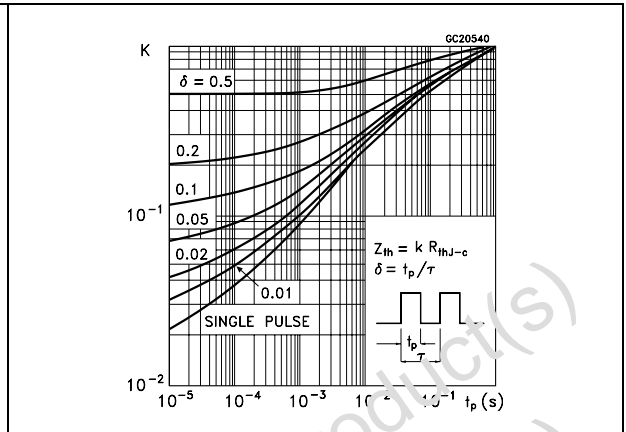


Figure 3. Output characteristics

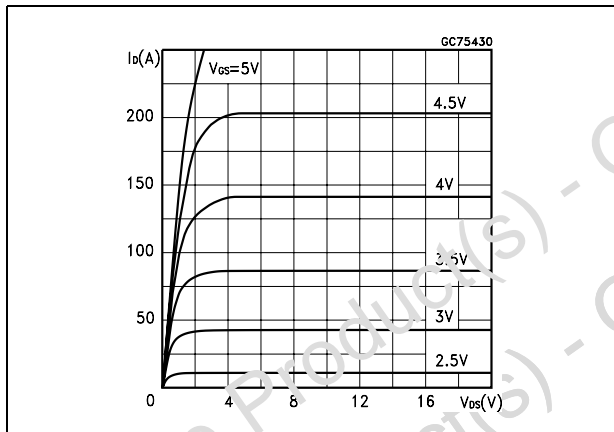


Figure 4. Transfer characteristics

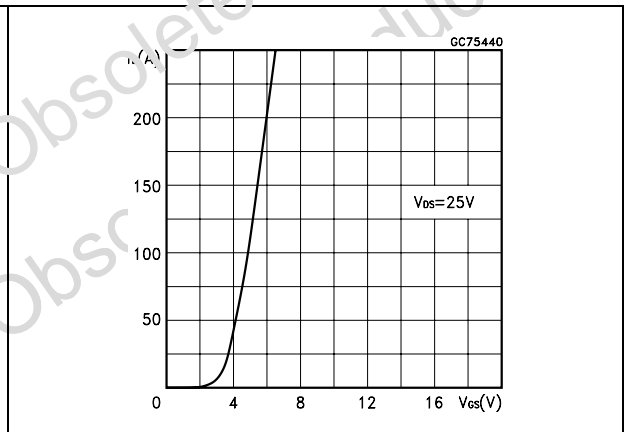


Figure 5. Transconductance

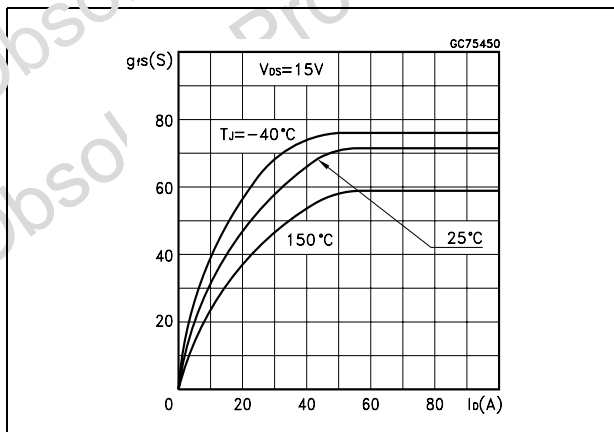


Figure 6. Static drain-source on resistance

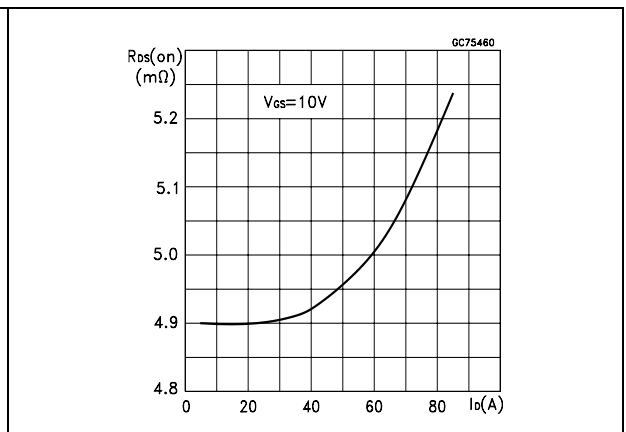


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

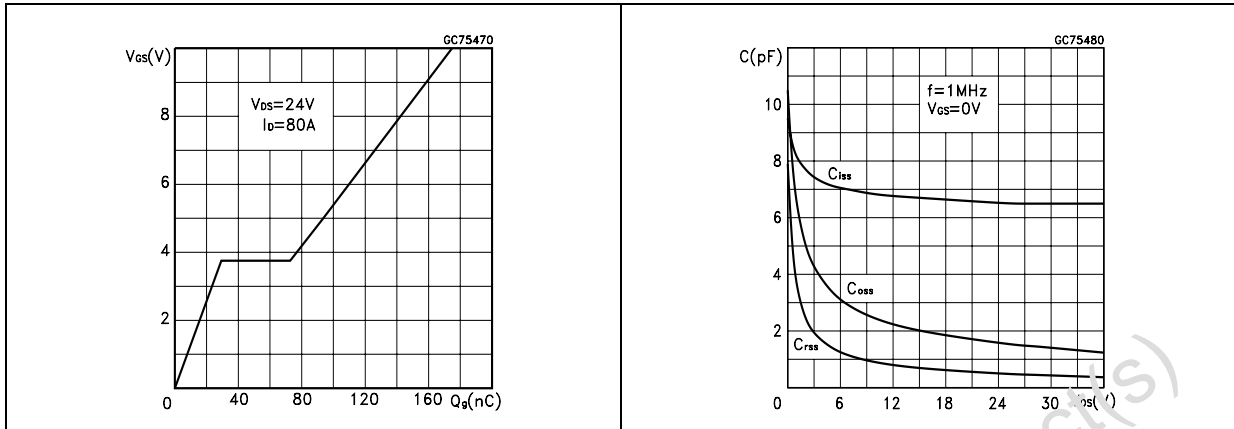


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

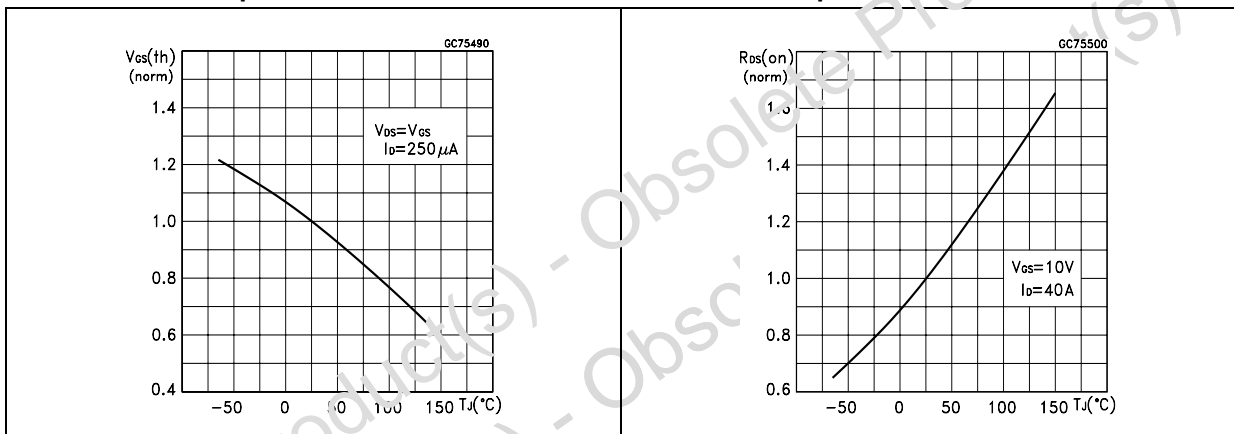
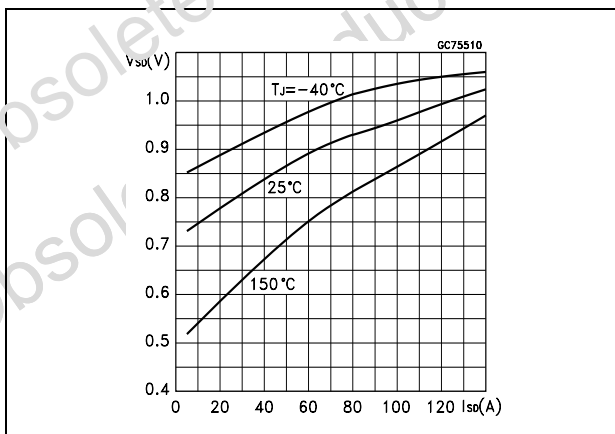


Figure 11. Source-drain diode forward characteristics



### 3 Test circuit

Figure 12. Switching times test circuit for resistive load

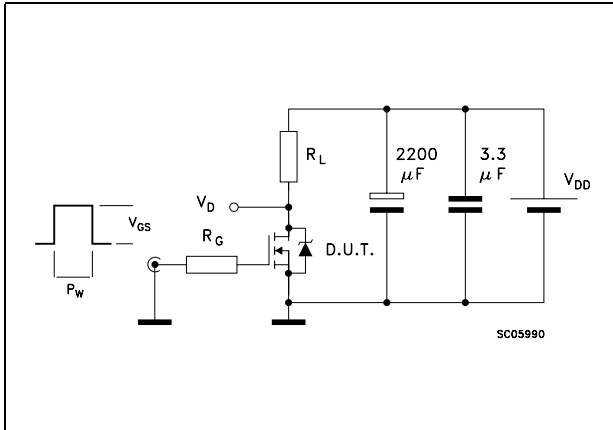


Figure 13. Gate charge test circuit

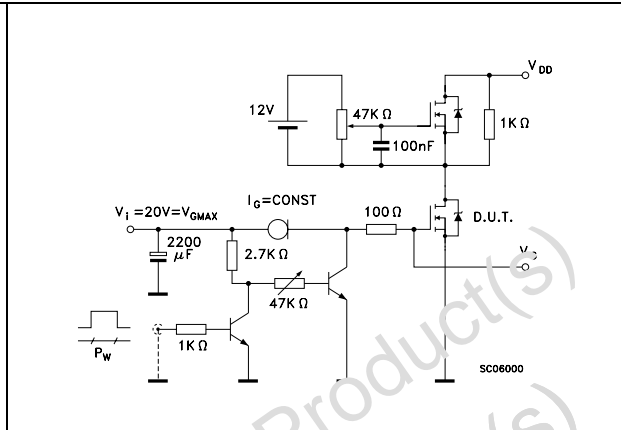


Figure 14. Test circuit for inductive load switching and diode recovery times

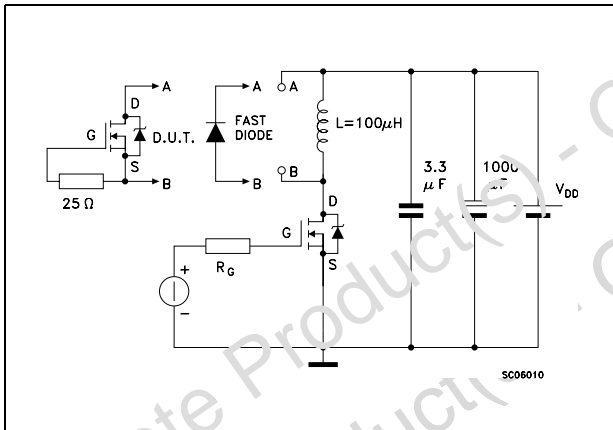


Figure 15. Unclamped inductive load test circuit

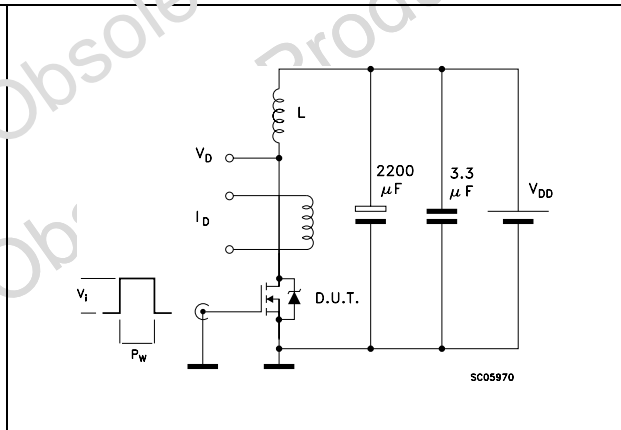
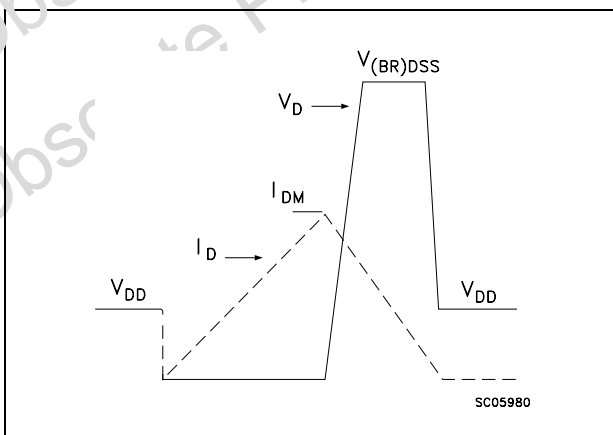


Figure 16. Unclamped inductive waveform



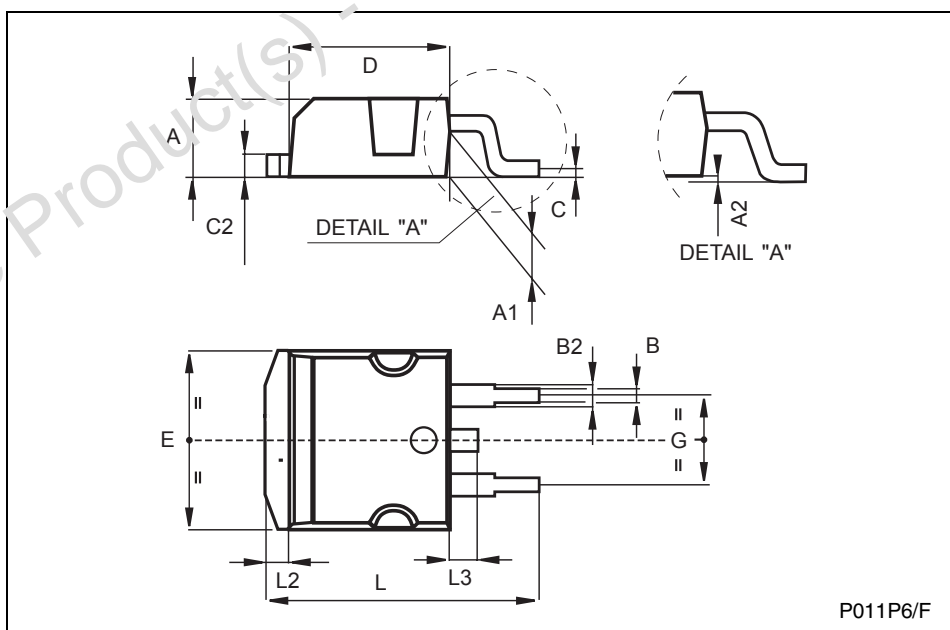
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

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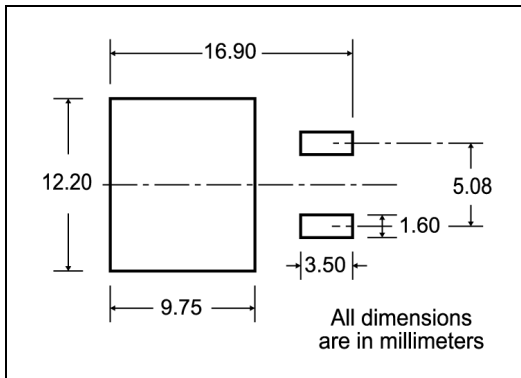
**TO-263 (D<sup>2</sup>PAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.87	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



## 5 Packaging mechanical data

### D<sup>2</sup>PAK FOOTPRINT



### TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

25 mm min. width

Tape slot in core for tape start

Full radius

#### REEL MECHANICAL DATA

C.M.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	24.4	26.4	0.960	1.039
N	100		3.937	
T		30.4		1.197

BASE QTY	BULK QTY
1000	1000

#### TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	10.5	10.7	0.413	0.421
B0	15.7	15.9	0.618	0.626
D	1.5	1.6	0.059	0.063
D1	1.59	1.61	0.062	0.063
E	1.65	1.85	0.065	0.073
F	11.4	11.6	0.449	0.456
K0	4.8	5.0	0.189	0.197
P0	3.9	4.1	0.153	0.161
P1	11.9	12.1	0.468	0.476
P2	1.9	2.1	0.075	0.082
R	50		1.574	
T	0.25	0.35	0.0098	0.0137
W	23.7	24.3	0.933	0.956

10 pitches cumulative tolerance on tape +/- 0.2 mm

Center line of cavity

User Direction of Feed

FEED DIRECTION

Bending radius R min.

\* on sales type

## 6 Revision history

**Table 8. Revision history**

Date	Revision	Changes
21-Jun-2004	5	Preliminary version
25-Jul-2006	6	New template, SOA updated

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