



**THE DATASHEET OF  
LM48823TLX/NOPB**



**LM48823****Boomer<sup>®</sup>** Audio Power Amplifier Series**Mono, Bridge-Tied Load, Ceramic Speaker Driver with I<sup>2</sup>C Volume Control and Reset**Check for Samples: [LM48823](#), [LM48823TLEVAL](#)**FEATURES**

- Integrated Charge Pump
- Bridge-Tied Load Output
- High PSRR
- I<sup>2</sup>C Volume and Mode Control
- Reset Input
- Advanced Click-and-Pop Suppression
- Low Supply Current
- Minimum External Components
- Micro-Power Shutdown
- Available in Space-Saving 16-Bump DSBGA Package

**APPLICATIONS**

- Cell Phones
- Smart Phones
- Portable Media Devices
- Notebook PCs

**KEY SPECIFICATIONS**

- Output Voltage at  $V_{DD} = 4.2V$ ,  $R_L = 2.2\mu F + 15\Omega$   
THD+N  $\leq 1\%$ : 5.4V<sub>RMS</sub> (typ)
- Quiescent Power Supply Current at 4.2V:  
3.3mA (typ)
- PSRR at 217Hz: 93dB (typ)
- Shutdown Current: 0.01 $\mu$ A (typ)

**DESCRIPTION**

The LM48823 is a single supply, mono, ceramic speaker driver with an integrated charge-pump, designed for portable devices, such as cell phones, where board space is at a premium. The LM48823 charge pump allows the device to deliver 5.4V<sub>RMS</sub> from a single 4.2V supply.

The LM48823 features high power supply rejection ratio (PSRR), 93dB at 217Hz, allowing the device to operate in noisy environments without additional power supply conditioning. Flexible power supply requirements allow operation from 2.0V to 4.5V. The LM48823 features an active low reset input that reverts the device to its default state. Additionally, the LM48823 features a 32-step I<sup>2</sup>C volume control. The low power Shutdown mode reduces supply current consumption to 0.01 $\mu$ A.

The LM48823's superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48823 is available in an ultra-small 16-bump DSBGA package (2mmx2mm).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

Typical Application

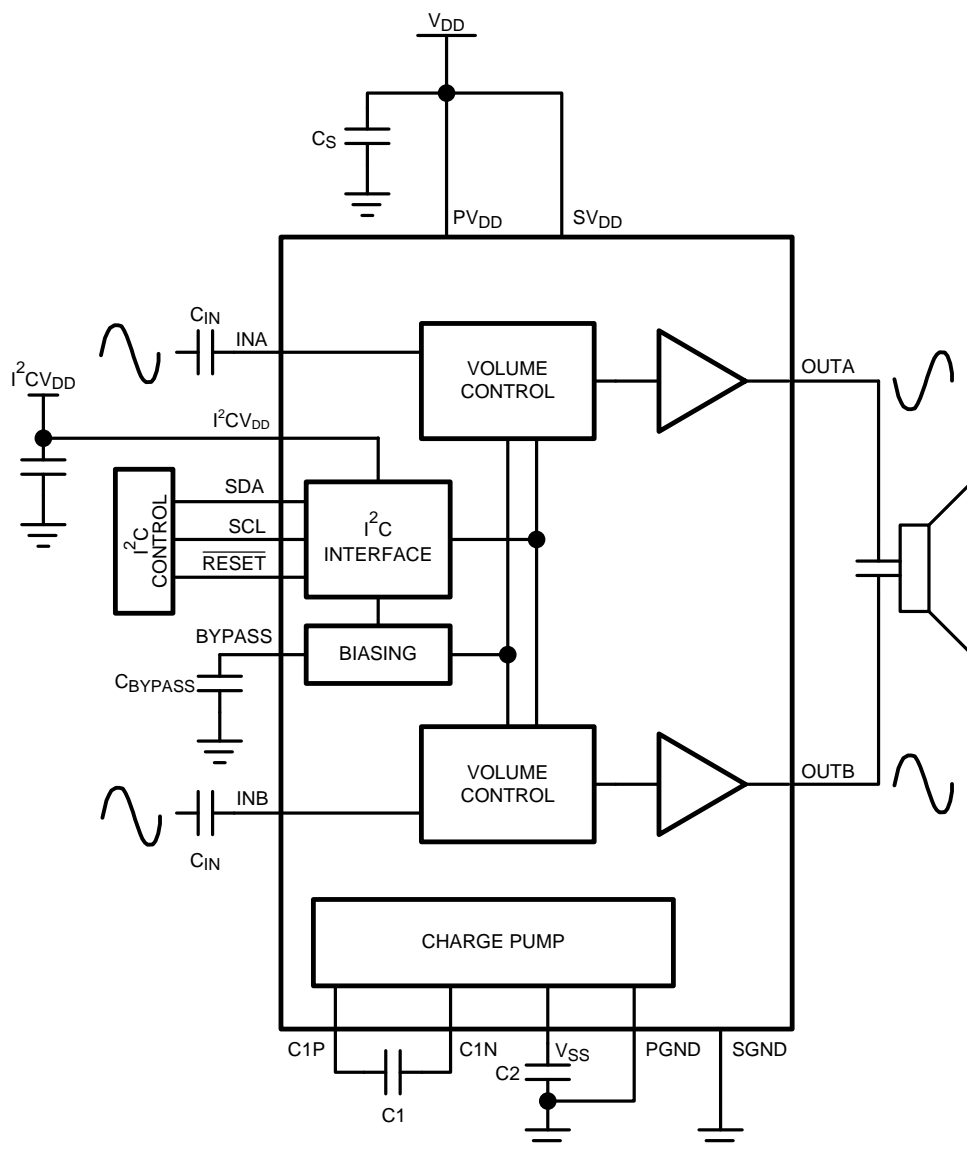


Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

YZR Package  
2mm x 2mm x 0.8mm

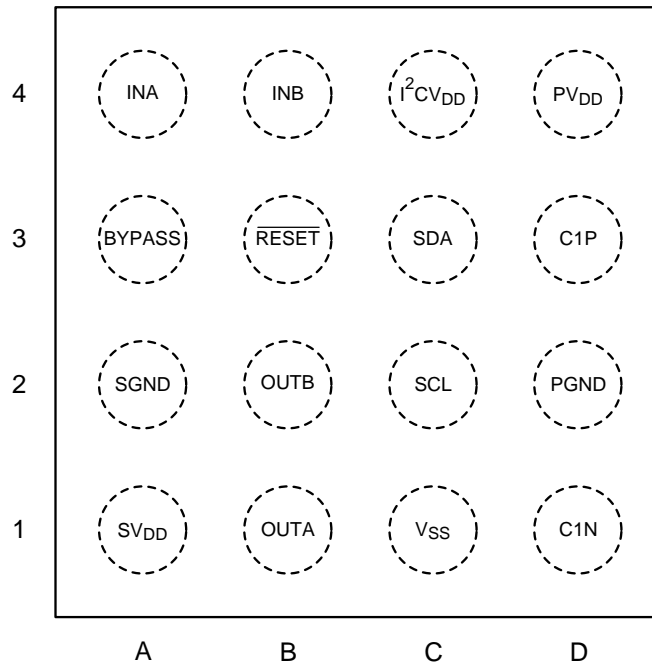


Figure 2. Top View  
See Package Number YZR 16

Bump Descriptions

Pin Designator	Pin Name	Pin Function
A1	SV <sub>DD</sub>	Signal Power Supply
A2	SGND	Signal Ground
A3	BYPASS	Amplifier Reference Bypass
A4	INA	Amplifier Inverting input A
B1	OUTA	Amplifier Inverting output A
B2	OUTB	Amplifier Non-Inverting Output B
B3	$\overline{\text{RESET}}$	Active Low Reset Input. Connect to V <sub>DD</sub> for normal operation. Toggle between V <sub>DD</sub> and GND to reset the device.
B4	INB	Amplifier Non-Inverting Input B
C1	V <sub>SS</sub>	Charge Pump Output
C2	SCL	I <sup>2</sup> C Serial Clock Input
C3	SDA	I <sup>2</sup> C Serial Data Input
C4	I <sup>2</sup> CV <sub>DD</sub>	I <sup>2</sup> C Supply Voltage
D1	C1N	Charge Pump Flying Capacitor Negative Terminal
D2	PGND	Power Ground
D3	C1P	Charge Pump Flying Capacitor Positive Terminal
D4	PV <sub>DD</sub>	Power Supply



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ABSOLUTE MAXIMUM RATINGS <sup>(1) (2)</sup>

Supply Voltage <sup>(1)</sup>	5.25V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to $V_{DD} + 0.3V$
Power Dissipation <sup>(3)</sup>	Internally Limited
ESD Rating <sup>(4)</sup>	8kV
ESD Rating <sup>(5)</sup>	250V
Junction Temperature	150°C
Thermal Resistance	
$\theta_{JA}$ (typ) - (TLA1611A)	63.2°C/W

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The [Electrical Characteristics](#) tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation is  $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$  or the number given in *Absolute Maximum Ratings*, whichever is lower.
- (4) Human body model, applicable std. JESD22-A114C.
- (5) Machine model, applicable std. JESD22-A115-A.

## OPERATING RATINGS

Temperature Range	
$T_{MIN} \leq T_A \leq T_{MAX}$	$-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
Supply Voltage	
$PV_{DD}$ and $SV_{DD}$	$2.0V \leq V_{DD} \leq 4.5V$
$I^2CV_{DD}$	$1.8V \leq I^2CV_{DD} \leq 4.5V$

**AUDIO AMPLIFIER ELECTRICAL CHARACTERISTICS  $V_{DD} = 4.2V$  <sup>(1)</sup> <sup>(2)</sup>**

The following specifications apply for  $A_V = 6dB$ ,  $R_L = 2.2\mu F + 15\Omega$ ,  $C_1 = C_2 = 2.2\mu F$ ,  $f = 1kHz$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	LM48823		Units (Limits)	
			Typical <sup>(3)</sup>	Limits <sup>(4)</sup>		
$I_{DD}$	Quiescent Power Supply Current	$V_{IN} = 0V$ , $R_L = \infty$	3.3	4.3	mA (max)	
$I_{SD}$	Shutdown Current	Shutdown Enabled	0.01	1	$\mu A$ (max)	
$V_{OS}$	Differential Output Offset Voltage	$V_{IN} = 0V$	0.5	3	mV (max)	
$V_{IH}$	Logic High Input Threshold	$\overline{RESET}$		1.4	V (min)	
$V_{IL}$		$\overline{RESET}$		0.4	V (max)	
$A_V$	Gain	Minimum Gain Setting	-70		dB	
		Maximum Gain Setting	24		dB	
$R_{IN}$	Input Resistance	Maximum Gain Setting	9	7	k $\Omega$ (min)	
			9	11	k $\Omega$ (max)	
		Minimum Gain Setting	80	64	k $\Omega$ (min)	
			80	96	k $\Omega$ (max)	
$V_O$	Output Voltage	$R_L = 2.2\mu F + 15\Omega$ , THD+N = 1%	$f = 1kHz$		$V_{RMS}$	
			$f = 5kHz$	3.1		$V_{RMS}$
THD+N	Total Harmonic Distortion + Noise	$V_O = 4V_{RMS}$	0.015		%	
PSRR	Power Supply Rejection Ratio	$V_{RIPPLE} = 200mV_{P-P}$ Sine, Inputs AC GND, $C_{IN} = 1\mu F$ , input referred	$f = 217Hz$	93	82	dB (min)
			$f = 1kHz$	93		dB
SNR	Signal-to-Noise-Ratio	$P_{OUT} = 40mW$ , $R_L = 16\Omega$ $f = 1kHz$	119		dB	
$\epsilon_{OS}$	Output Noise	$A_V = 4dB$ , Input Referred, A-weighted Filter	5.5		$\mu V$	
$T_{WU}$	Wake-Up Time		200		$\mu s$	

- (1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The [Electrical Characteristics](#) tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at  $T_A = +25^\circ C$ , and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
- (4) Datasheet min/max specification limits are specified by test or statistical analysis.

## I<sup>2</sup>C INTERFACE CHARACTERISTICS $V_{DD} = 3.0V$ <sup>(1)</sup> <sup>(2)</sup>

The following specifications apply for  $A_V = 6dB$ ,  $R_L = 2.2\mu F + 15\Omega$ ,  $C_1 = C_2 = 2.2\mu F$ ,  $f = 1kHz$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	LM48823		Units (Limits)
			Typical <sup>(3)</sup>	Limits <sup>(4)</sup>	
$t_1$	SCL period			2.5	$\mu s$ (min)
$t_2$	SDA Setup Time			100	ns (min)
$t_3$	SDA Stable Time			0	ns (min)
$t_4$	Start Condition Time			100	ns (min)
$t_5$	Stop Condition Time			100	ns (min)
$V_{IH}$	Logic High Input Threshold			$0.7 \times I^2CV_{DD}$	V (min)
$V_{IL}$	Logic Low Input Threshold			$0.3 \times I^2CV_{DD}$	V (max)

- (1) “*Absolute Maximum Ratings*” indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
- (2) The [Electrical Characteristics](#) tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
- (3) Typical values represent most likely parametric norms at  $T_A = +25^\circ C$ , and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
- (4) Datasheet min/max specification limits are specified by test or statistical analysis.

TYPICAL PERFORMANCE CHARACTERISTICS

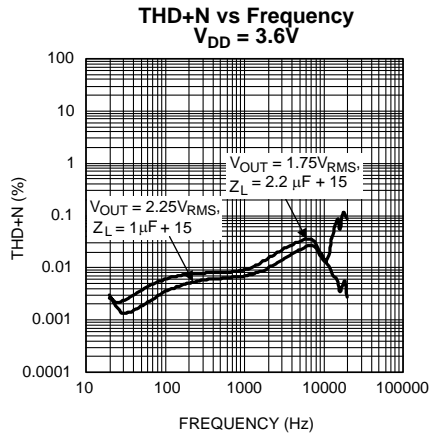


Figure 3.

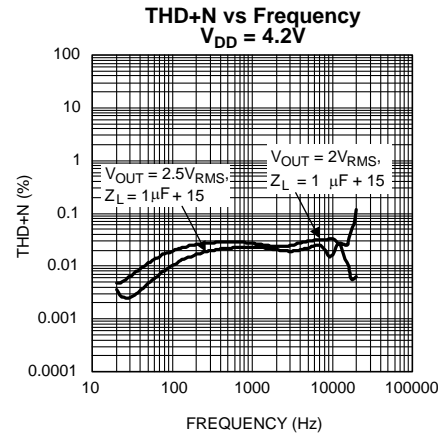


Figure 4.

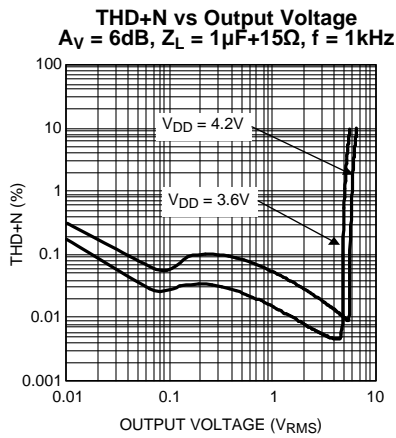


Figure 5.

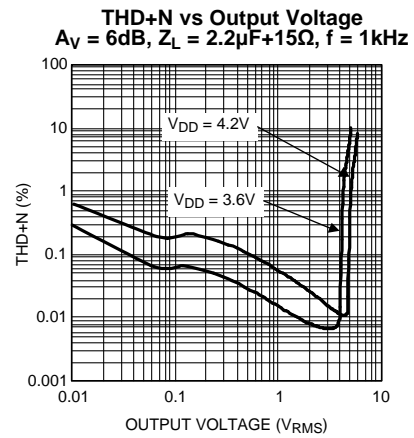


Figure 6.

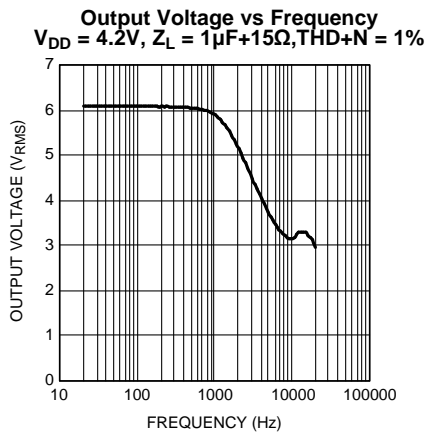


Figure 7.

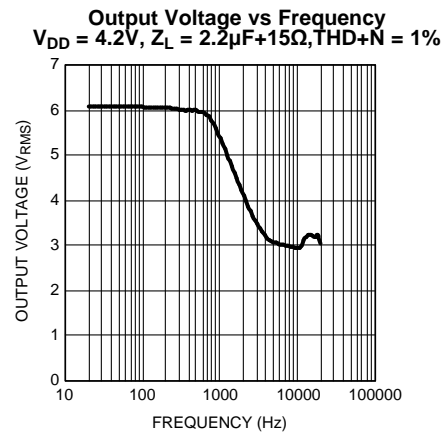
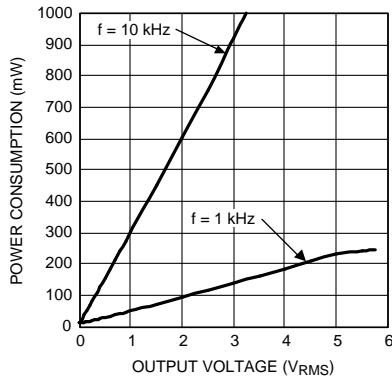


Figure 8.

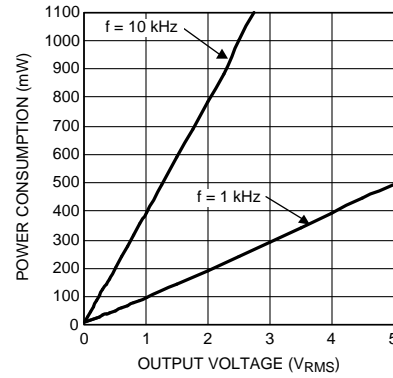
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**

**Power Consumption vs Output Voltage**  
 $V_{DD} = 3.6V, Z_L = 1\mu F + 15\Omega$



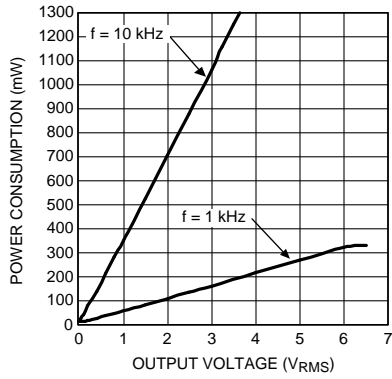
**Figure 9.**

**Power Consumption vs Output Voltage**  
 $V_{DD} = 3.6V, Z_L = 2.2\mu F + 15\Omega$



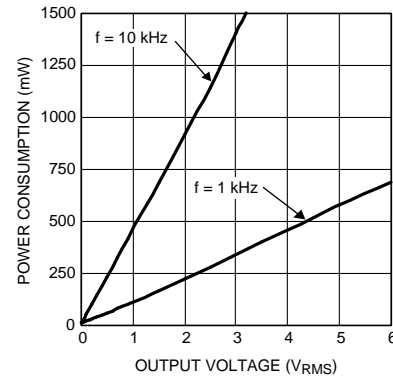
**Figure 10.**

**Power Consumption vs Output Voltage**  
 $V_{DD} = 4.2V, Z_L = 1\mu F + 15\Omega$



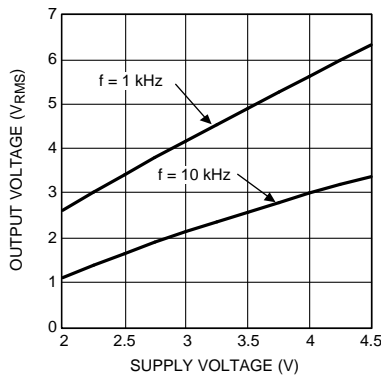
**Figure 11.**

**Power Consumption vs Output Voltage**  
 $V_{DD} = 4.2V, Z_L = 2.2\mu F + 15\Omega$



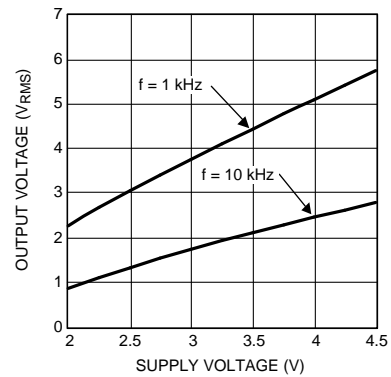
**Figure 12.**

**Output Voltage vs Supply Voltage**  
 $Z_L = 1\mu F + 15\Omega, THD+N = 1\%$



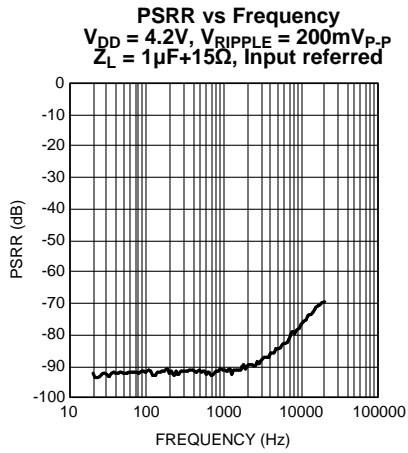
**Figure 13.**

**Output Voltage vs Supply Voltage**  
 $Z_L = 2.2\mu F + 15\Omega, THD+N = 1\%$

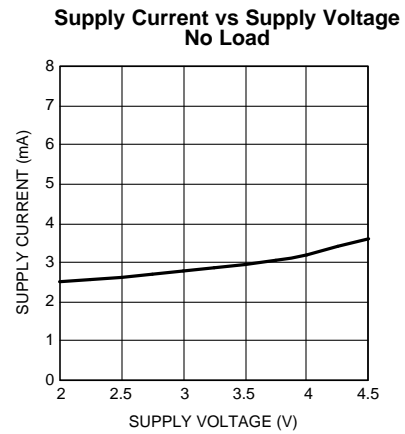


**Figure 14.**

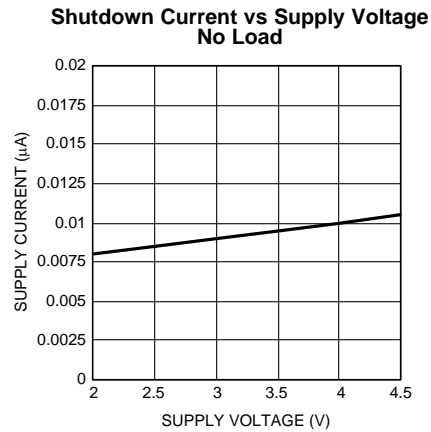
**TYPICAL PERFORMANCE CHARACTERISTICS (continued)**



**Figure 15.**



**Figure 16.**



**Figure 17.**

## APPLICATION INFORMATION

### I<sup>2</sup>C COMPATIBLE INTERFACE

The LM48823 is controlled through an I<sup>2</sup>C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48823 and the master can communicate at clock rates up to 400kHz. Figure 18 shows the I<sup>2</sup>C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48823 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 19). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 20). The LM48823 device address is 1110110.

### I<sup>2</sup>C BUS FORMAT

The I<sup>2</sup>C bus format is shown in Figure 20. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the  $\overline{R/W}$  bit.  $\overline{R/W} = 0$  indicates the master is writing to the slave device,  $\overline{R/W} = 1$  indicates the master wants to read data from the slave device. Set  $\overline{R/W} = 0$ ; the LM48823 is a WRITE-ONLY device and will not respond to the  $\overline{R/W} = 1$ . The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48823 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM48823 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.

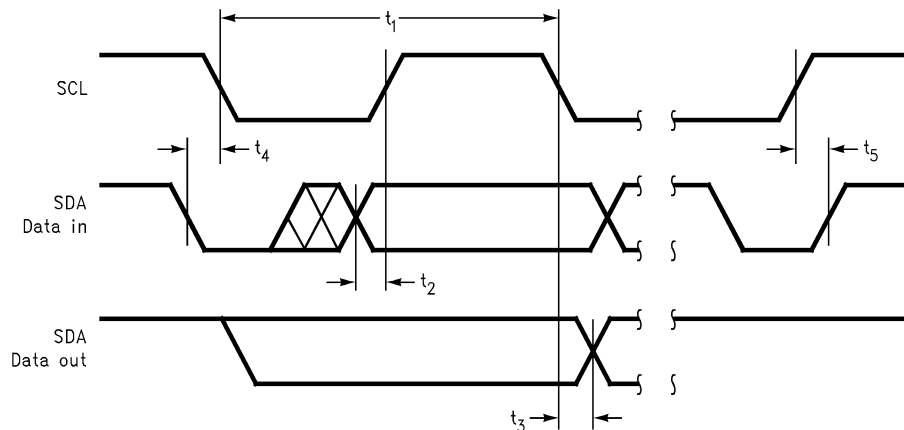


Figure 18. I<sup>2</sup>C Timing Diagram

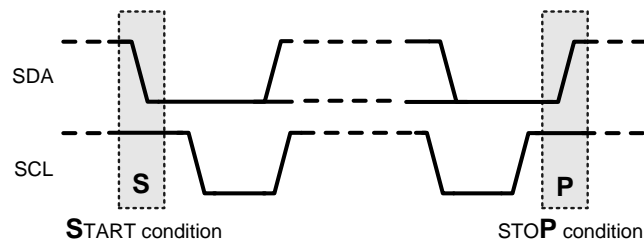


Figure 19. Start and Stop Diagram

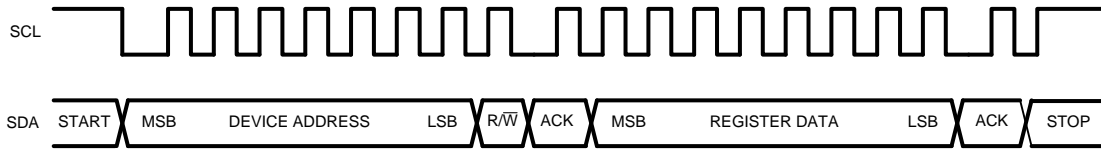


Figure 20. Example Write Sequence

Table 1. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 R/W
Chip Address	1	1	1	0	1	1	0	0

Table 2. Mode Control Registers

Register Name	B7	B6	B5	B4	B3	B2	B1	B0
Mode Control	VOL4	VOL3	VOL2	VOL1	VOL0	0	ENABLE_A	ENABLE_B

### GENERAL AMPLIFIER FUNCTION

The LM48823 is a ceramic speaker driver that utilizes TI's inverting charge pump technology to deliver over 15V<sub>P-P</sub> to a 2.2μF ceramic speaker while operating from a single 4.2V supply. The LM48823 features a unique input stage that converts two single-ended audio signals into a mono BTL output. This stereo to mono conversion is useful in applications where a stereo audio source is driving a single ceramic speaker, such as a ringer on a cellular phone. Connect INA and INB as shown in Figure 21 for the stereo-to-mono conversion. When the LM48823 is used with a single-ended mono audio source, connect both INA and INB to the audio source as shown in Figure 22.

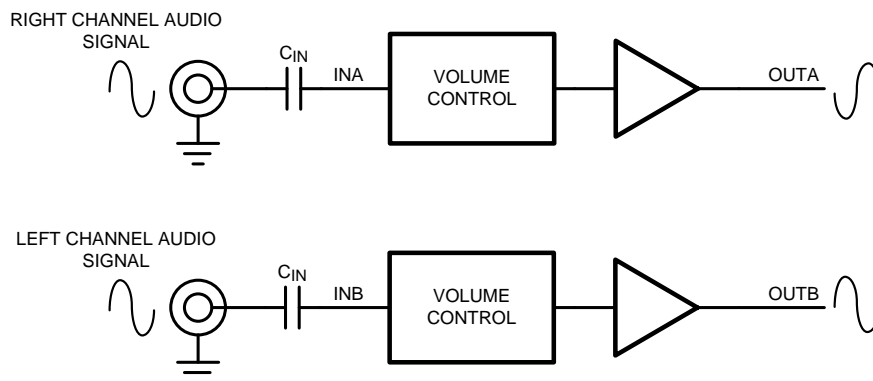


Figure 21. Stereo to Mono Conversion Connection Example

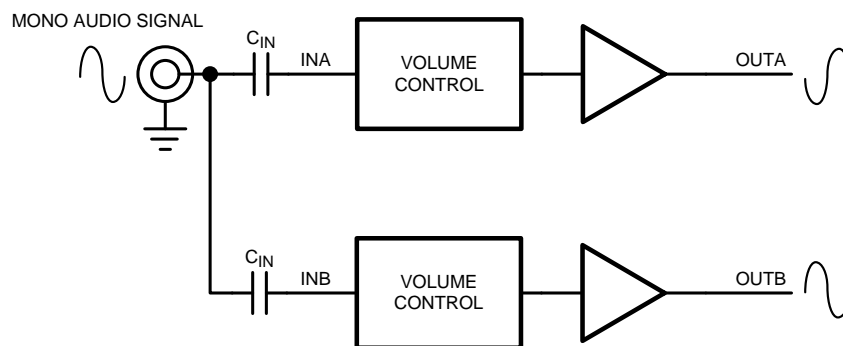


Figure 22. Mono Audio Source Connection Example

## VOLUME CONTROL

Table 3. Volume Control

Volume Step	VOL4	VOL3	VOL2	VOL1	VOL0	Gain (dB)
1	0	0	0	0	0	-70
2	0	0	0	0	1	-56
3	0	0	0	1	0	-46
4	0	0	0	1	1	-38
5	0	0	1	0	0	-32
6	0	0	1	0	1	-28
7	0	0	1	1	0	-24
8	0	0	1	1	1	-21
9	0	1	0	0	0	-18
10	0	1	0	0	1	-15
11	0	1	0	1	0	-12
12	0	1	0	1	1	-10
13	0	1	1	0	0	-8
14	0	1	1	0	1	-6
15	0	1	1	1	0	-4
16	0	1	1	1	1	-2
17	1	0	0	0	0	0
18	1	0	0	0	1	2
19	1	0	0	1	0	4
20	1	0	0	1	1	6
21	1	0	1	0	0	8
22	1	0	1	0	1	10
23	1	0	1	1	0	12
24	1	0	1	1	1	14
25	1	1	0	0	0	16
26	1	1	0	0	1	18
27	1	1	0	1	0	19
28	1	1	0	1	1	20
29	1	1	1	0	0	21
30	1	1	1	0	1	22
31	1	1	1	1	0	23
32	1	1	1	1	1	24

## SHUTDOWN FUNCTION

The LM48823 features a low-power shutdown mode that disables the device, lowering the quiescent current to 0.01 $\mu$ A. Set bits B1 (ENABLE\_A) and B2 (ENABLE\_B) to 0 to disable the amplifiers and charge pump. Set both ENABLE\_A and ENABLE\_B to 1 for normal operation. Shutdown mode does not clear the I<sup>2</sup>C register. When re-enabled, the device returns to its previous volume setting. To clear the I<sup>2</sup>C register, either remove power from the device, or toggle RESET (see [RESET](#) section).

## RESET

The LM48823 features an active low reset input. Driving  $\overline{\text{RESET}}$  low clears the I<sup>2</sup>C register. Volume control is set to 00000 (-70dB) and both ENABLE\_A and ENABLE\_B are set to 0, disabling the device. While  $\overline{\text{RESET}}$  is low, the LM48823 ignores any I<sup>2</sup>C data. After the device is reset, and RESET is driven high, the LM48823 remains in shutdown mode with the volume set to -70dB. Re-enable the device by writing to the I<sup>2</sup>C register.

## PROPER SELECTION OF EXTERNAL COMPONENTS

### Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1µF ceramic capacitor from V<sub>DD</sub> to GND. Additional bulk capacitance may be added as required.

### Bypass Capacitor Selection

The BYPASS capacitor, C<sub>BYPASS</sub>, improves PSRR, noise rejection and output offset. For best results, use a capacitor of identical value to the input coupling capacitors

### Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

### Charge Pump Flying Capacitor (C1)

The flying capacitor (C1) affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the R<sub>DS(ON)</sub> of the charge pump switches and the ESR of C1 and C2 dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

### Charge Pump Hold Capacitor (C2)

The value and ESR of the hold capacitor (C2) directly affects the ripple on CPV<sub>SS</sub>. Increasing the value of C2 reduces output ripple. Decreasing the ESR of C2 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

### Input Capacitor Selection

Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48823. The input capacitors create a high-pass filter with the input resistors R<sub>IN</sub>. The -3dB point of the high pass filter is found using [Equation 1](#).

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (\text{Hz})$$

where

- the value of R<sub>IN</sub> is given in the [Electrical Characteristics](#) table. (1)

High pass filtering the audio signal helps protect the speakers. When the LM48823 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

## PCB LAYOUT GUIDELINES

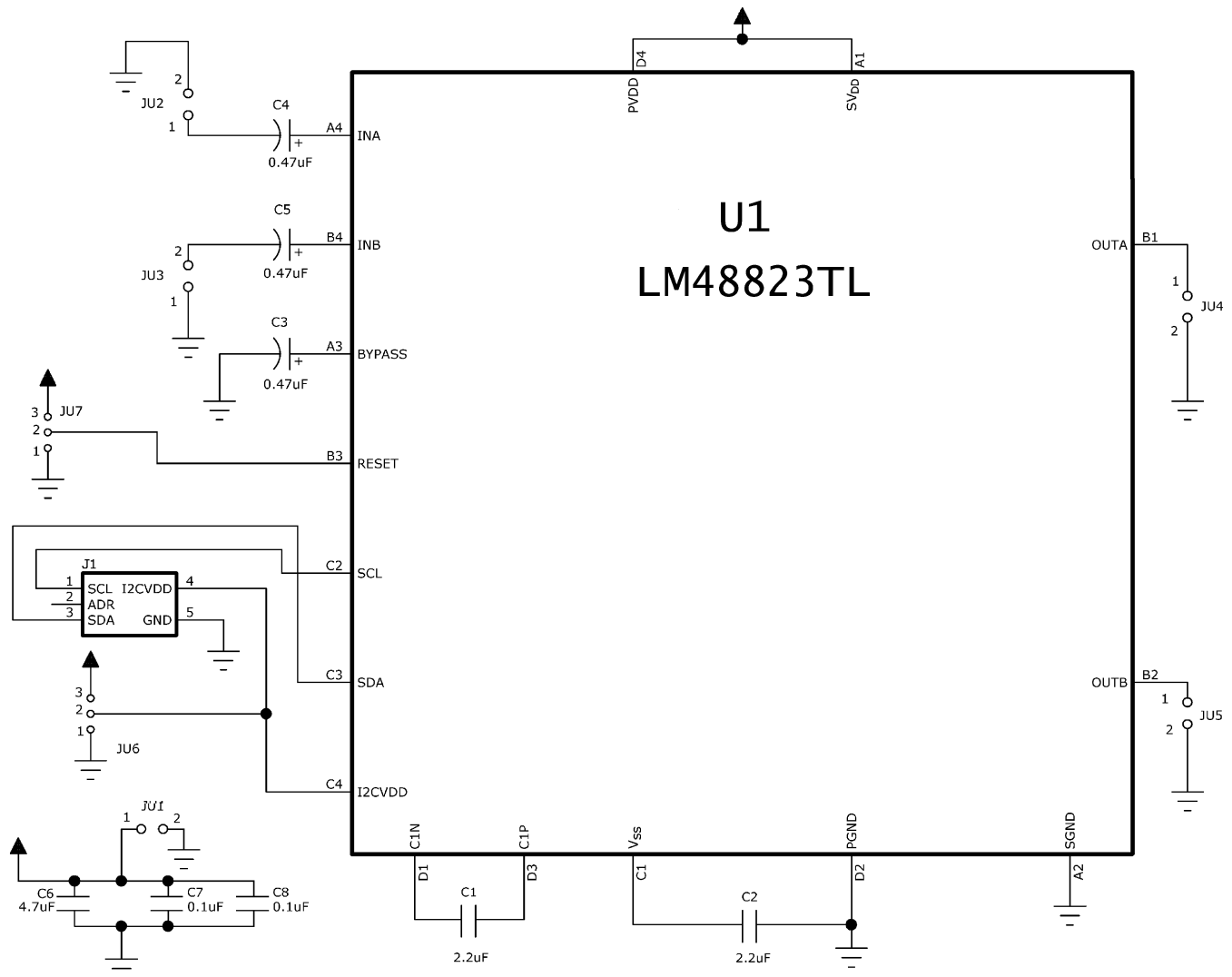
Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48823 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

**LM48823TL DEMOBOARD BILL OF MATERIALS**

Designator	Quantity	Description
C1, C2	2	2.2µF ±10% 10V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB1A225K Murata GRM033R60J104KE19D
C3 – C5	3	1µF ±10% 10V Tantalum Capacitor (402) AVX TACK105M010QTA
C6	1	4.7µF ±10% 6.3V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB0J475K Murata GRM188R60J475KE19D
C7, C8	2	0.1µF ±10% 6.3V X5R Ceramic Capacitor (201) Panasonic ECJ-ZEB0J104K Murata GRM188R61A225KE34D
JU1 – JU5	5	2 Pin Header
JU6, JU7	3	2 Pin Header
J1	1	5-Pin I <sup>2</sup> C Header
LM48823TL	1	LM48823TL (16-Bump DSBGA)

**DEMO BOARD SCHEMATIC**



**Figure 23. LM48823 Demo Board Schematic**

PC BOARD LAYOUT

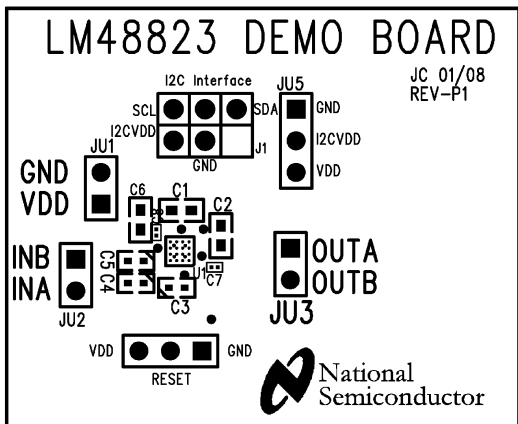


Figure 24. Top Silkscreen Layer

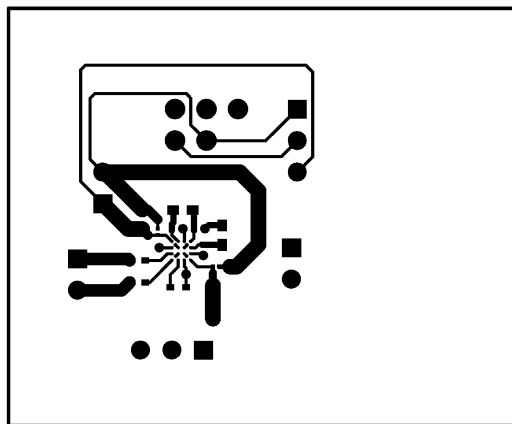


Figure 25. Top Layer

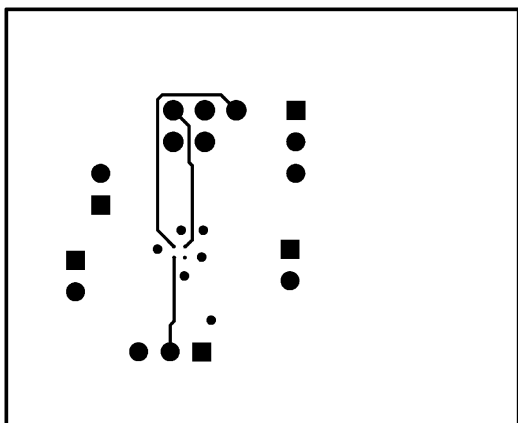


Figure 26. Layer 2

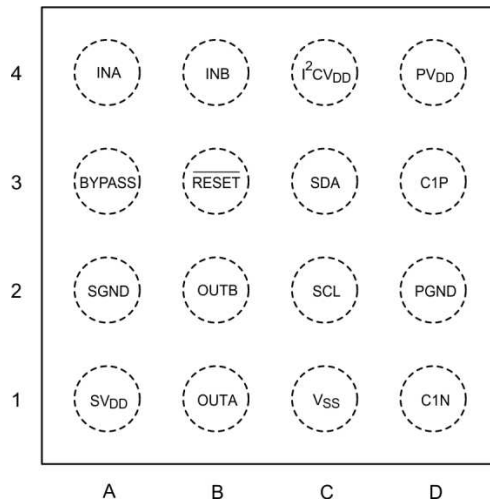


Figure 27. Layer 3

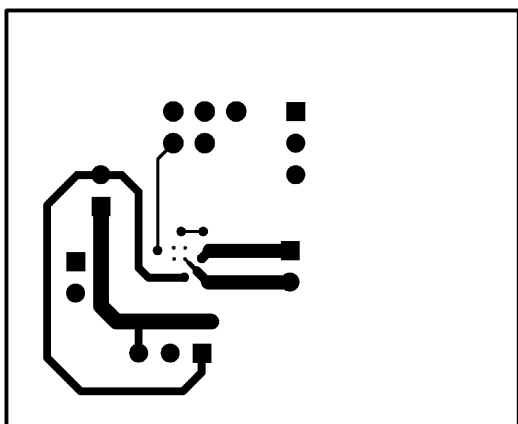


Figure 28. Bottom Layer

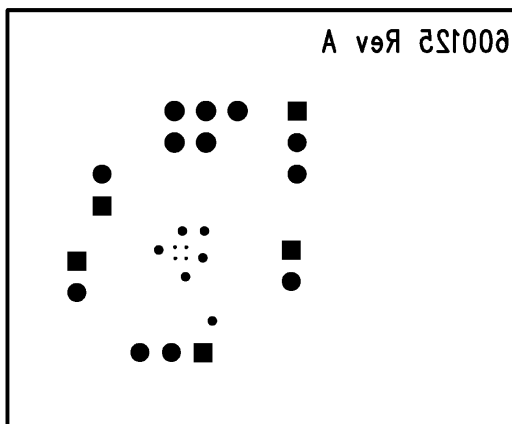


Figure 29. Bottom Silkscreen

### REVISION HISTORY

Rev	Date	Description
1.0	06/27/08	Initial release.
1.01	07/15/08	Edited the Ordering Information table.
1.02	10/08/10	Updated some Limits (under Gain) in the Volume Control table.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM48823TL/NOPB	ACTIVE	DSBGA	YZR	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		GK6	<b>Samples</b>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

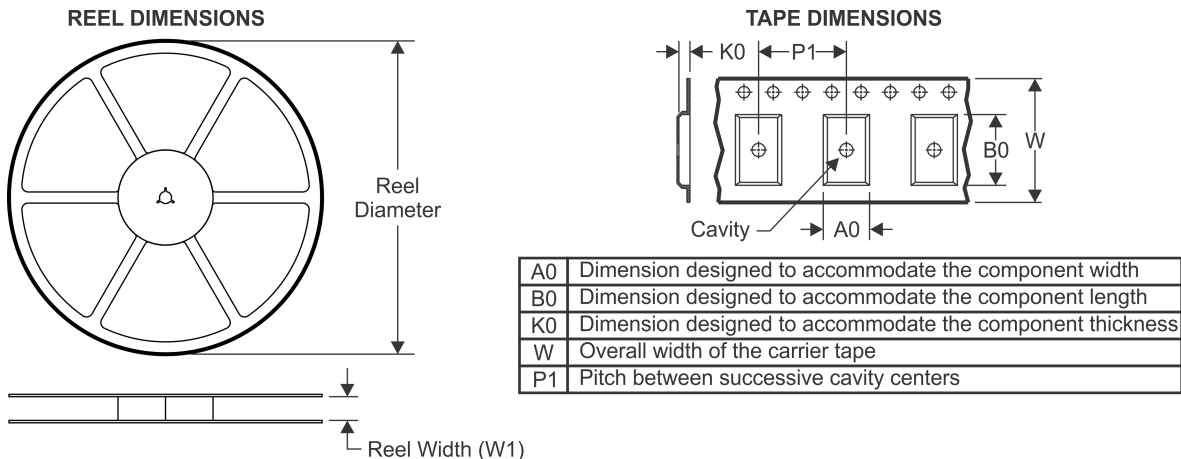
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

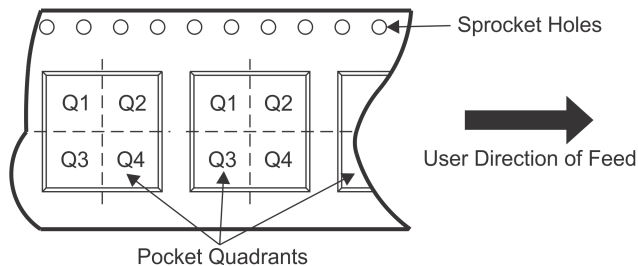
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48823TL/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

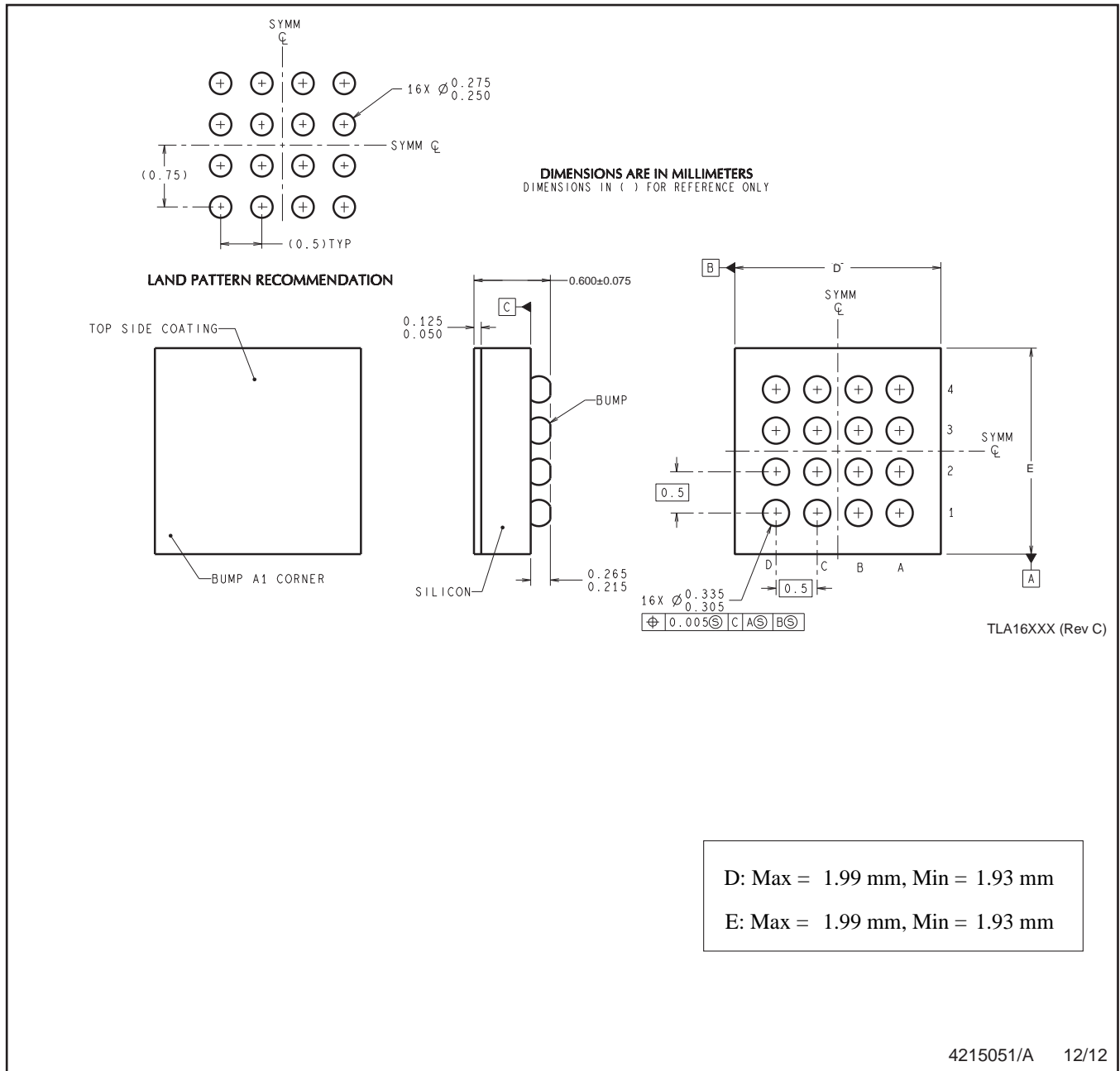
**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48823TL/NOPB	DSBGA	YZR	16	250	210.0	185.0	35.0

YZR0016



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.  
 B. This drawing is subject to change without notice.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View LM48823TLX/NOPB on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management