THE DATASHEET OF

LM5068MMX-2

LM5068 Negative Voltage Hot Swap Controller

Check for Samples: LM5068

FEATURES

- **Safe Module Insertion and Removal from Live Backplanes**
- **In-Rush Current Limiting for Safe Board Insertion into Live Backplanes**
- **Fast Response to Over-Current Fault Conditions with Active Current Limiting**
- **-10V to -90V Input Range**
- **Programmable Under-Voltage/Over-Voltage Shutdown Protection with Adjustable Hysteresis**
- **Programmable Multi-Function Timer for Board Insertion De-Bounce Delay**
- **Fault Timer Avoids Nuisance Trips Caused by Short Duration Load Transients**
- **Active Gate Clamping During Initial Power Application**
- **Available in both Latched Fault and Automatic Re-Try Versions**
- **Available with either Active HIGH or Active LOW Power Good Flag**

APPLICATIONS

- **- 48V Power Modules**
- **Central Office Switching**
- **Distributed Power Systems**
- **Electronic Circuit Breaker**
- **PBX Systems**
- **Negative Power Supply Control**

DESCRIPTION

The LM5068 hot-swap controller provides intelligent control of power supply connections during the insertion and removal of circuit cards powered by live system backplanes.

The LM5068 provides both in-rush current control and short-circuit protection functions, and limits power supply transients in the backplane caused by the insertion of additional circuit cards. The LM5068 controls the external N-Channel MOSFET to provide programmable load current limiting and circuit breaker functions using a single external current sense resistor. The LM5068 issues a power good (PWRGD) signal at the conclusion of a successful power-on sequence. Input over-voltage or under -voltage fault conditions will cancel the PWRGD indication.

The LM5068-1 and -2 indicate power-good as an open-drain active HIGH PWRGD state. The LM5068-3 and -4 indicate power-good as an open-drain active LOW PWRGD state. The LM5068-1 and -3 latch off after a fault condition is detected while the LM5068-2 and -4 continuously re-try at intervals set by a programmable timer.

The LM5068 is available in a VSSOP-8 package.

Typical Application

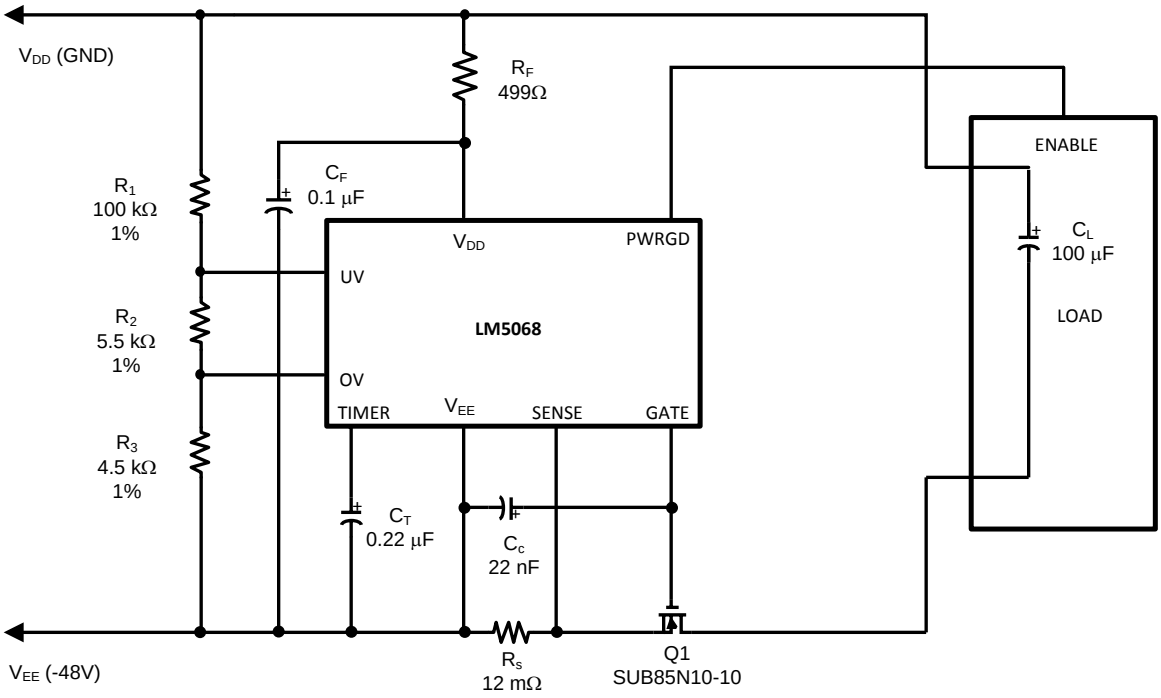
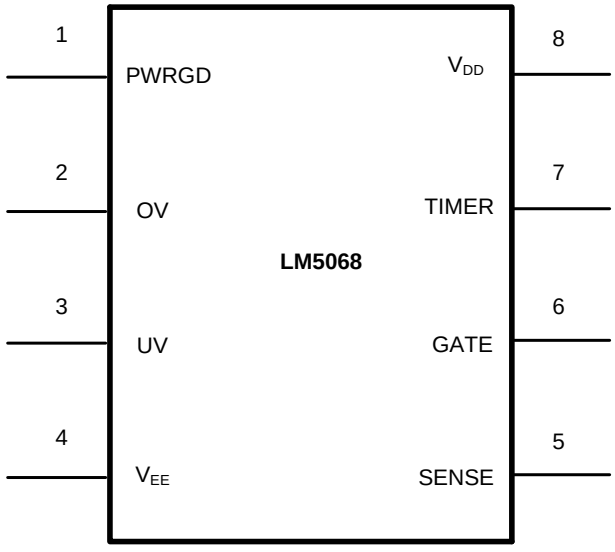


Figure 1. Negative Power Supply Control

Connection Diagram



PIN DESCRIPTION

PIN	NAME	DESCRIPTION	APPLICATION INFORMATION
1	PWRGD	Open Drain Power Good indicator	Following a successful power-up sequence the PWRGD signal will be active. The LM5068-1 and -2 are configured for an active power-good state as HIGH, while the LM5068-3 and –4 are configured for an active power-good state as LOW.
2	OV	Line Over-Voltage Shutdown	An external resistor divider from the power source sets the over-voltage shutdown level. Hysteresis is generated by an internal current source which sources 20 µA into the external divider when the OV pin exceeds 2.5V.
3	UV	Line Under-Voltage Shutdown	An external resistor divider from the power source sets the under-voltage shutdown level. Hysteresis is set by an internal current source which sinks 20 µA from the external divider when the UV pin falls below 2.5V.
4	V_{EE}	Negative Supply Voltage Input	
5	SENSE	Current Sense Input	Load current is monitored via an external current sense resistor (R_S). If the voltage across R_S exceeds 50mV the fault timer is initiated. Load current is actively limited to 100mV/R_S. If the sense voltage exceeds 200mV due to a catastrophic fault, the fast gate pull down circuit will reduce the MOSFET gate voltage and initiate active current limiting.
6	GATE	N-Channel MOSFET Gate Drive Output	This output is pulled high by a 60 µA current source to turn on the MOSFET.
7	TIMER	Timer Input	An external capacitor connected to this pin sets the initial start-up delay and the delay to shutdown in the event of an over-current condition. This pin is also used for the automatic re-try timing sequence, following fault shutdown (-2 and –4 versions).
8	V_{DD}	Positive Supply Voltage Input	

Configuration Table

Part Number	Latch Off /Successive Re-try	Power Good Polarity	Package
LM5068MM-1/MMX-1	Latch Off	Active HIGH	VSSOP- 8
LM5068MM-2/MMX-2	Auto Re-try	Active HIGH	
LM5068MM-3/MMX-3	Latch Off	Active LOW	
LM5068MM-4/MMX-4	Auto Re-try	Active LOW	

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

V_{DD} (V_{DD} to V_{EE})	100V
PWRGD (PWRGD to V_{EE})	100V
SENSE (SENSE to V_{EE})	8V
UV/OV (Clamped) (UV/OV to V_{EE})	8V
All Other Inputs to V_{EE}	16V
Junction Temperature (T_J)	+150°C
Storage Temperature (T_S)	-55°C to +150°C
Soldering Information	
ESD Rating (3)	2kV

(1) Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is intended to be functional. For specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The ESD rating of Pin 7 is 1.5kV. It is recommended that proper ESD precautions are taken to avoid performance degradation or loss of functionality.

Operating Ratings

Supply Voltage Range (V_{DD})	10V to 90V
Junction Temp. Range	−40°C to +105°C

Electrical Characteristics

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise noted V_{DD} − V_{EE} = 48V.

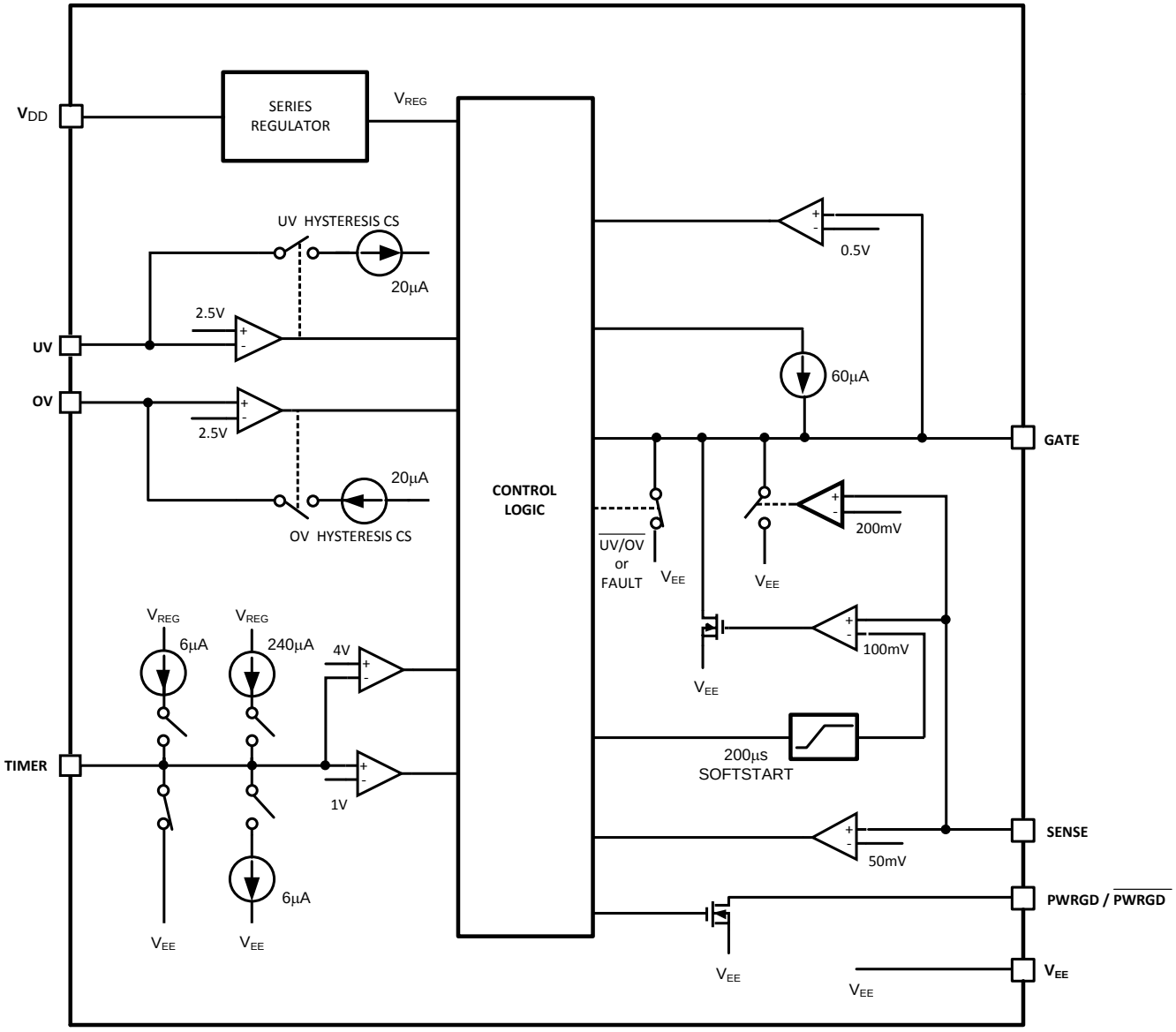
Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD} Supply						
I_{IN}	Supply Current			0.82	**1.3**	mA
I_{SD}	Shutdown Current	UV/OV = 0V		580	**1000**	µA
V_{DD} − V_{EE}	Operating Supply Range		**10**		**90**	V
UV/OV Shutdown						
V_{UVS}	V_{DD} Under-voltage Shutdown			8.5		V
V_{UVSH}	V_{DD} Under-voltage Shutdown Hysteresis			0.6		V
V_{UV}	Under-voltage Comparator Threshold		**2.45**	2.5	**2.55**	V
I_{UVHCS}	Under-voltage Hysteresis Current Source		**18**	20	**22**	µA
V_{OV}	Over-voltage Comparator Threshold		**2.45**	2.5	**2.55**	V
I_{OVHCS}	Over-voltage Hysteresis Current Sink		**18**	20	**22**	µA
t_{UVCD}	UV Comparator Delay	UV Low to Gate Low		1100		ns
t_{OVCD}	OV Comparator Delay	OV High to Gate Low		500		ns
Current Limit Voltage						
V_{CB}	Circuit Breaker Current Limit Voltage		**40**	50	**60**	mV
V_{AC}	Analog Current Limit Voltage		**80**	100	**120**	mV
V_{FDC}	Fast Discharge Current Limit Voltage (Fast Gate Pull Down Threshold)		**150**	200	**250**	mV
Sense Input						
I_{SENSE}	Sense Input Current	V_{SENSE} = 50mV	**-30**	-15		µA

Electrical Characteristics (continued)

Specifications in standard typeface are for T_J = +25°C, and those in **boldface type** apply over the full operating junction temperature range. Unless otherwise noted $V_{DD} - V_{EE}$ = 48V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Timer						
V_{THVT}	Timer High Voltage Threshold			4		V
V_{TLVT}	Timer Low Voltage Threshold			**1**		V
I_{TIMER}	Timer On (Initial Cycle, Sourcing)	V_{TIMER} = 2V	**4**	6	**8**	µA
	Timer Off (Initial Cycle, Sinking)	V_{TIMER} = 2V		27		mA
	Timer On (Circuit Breaker, Sourcing)	V_{TIMER} = 2V	**200**	240	**280**	µA
	Timer Off (Cooling Cycle, Sinking)	V_{TIMER} = 2V	**4**	6	**8**	µA
Gate Drive						
V_G	Saturation Gate Drive Voltage	V_{DD}- V_{EE} = 48V	**9**	10.6	**12**	V
		V_{DD}- V_{EE} = 10V		7.8		V
V_{GLT}	Gate Low Threshold	Before Gate ramp-up		0.5		V
I_{GATE}	Gate Pin Current (Sourcing)	V_{SENSE} = 0V	**40**	60	**80**	µA
	Gate Pin Current (Sinking)	V_{SENSE} = 150mV V_{GATE} = 3V		2.7		mA
	Gate Pin Current (Sinking)	V_{SENSE} = 300mV V_{GATE} = 1V		300		mA
PWRGD						
V_{PGLV}	PWRGD Low Voltage	I_{SINK} = 1mA		0.2	**0.6**	V
I_{PGLC}	PWRGD High Leakage Current	V_{PWRGD} = 90V		1		µA
V_{PGV}	GATE Voltage at onset of PWRGD			8		V

Block Diagram



Typical Performance Characteristics

I_{IN} vs Temperature

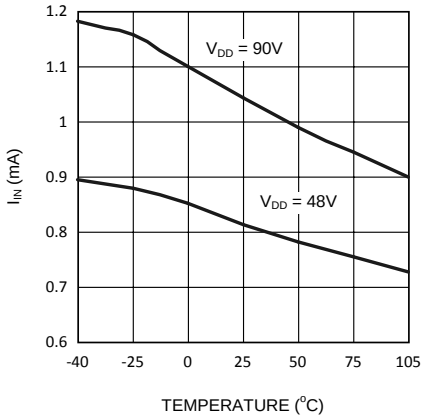


Figure 2.

I_{IN} vs V_{DD}

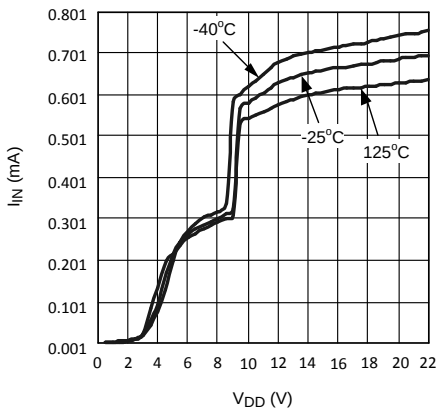


Figure 3.

V_{DD} Under-Voltage Shutdown (V_{UVS}) vs Temperature

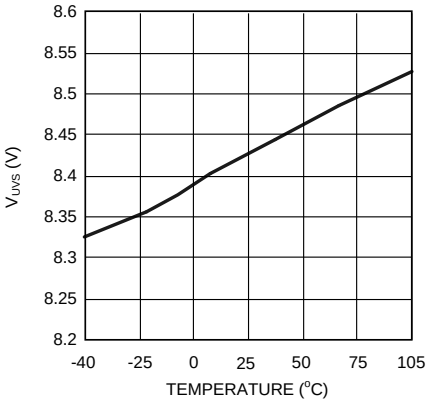


Figure 4.

V_{DD} Under-Voltage Shutdown Hysteresis (V_{UVSH}) vs Temperature

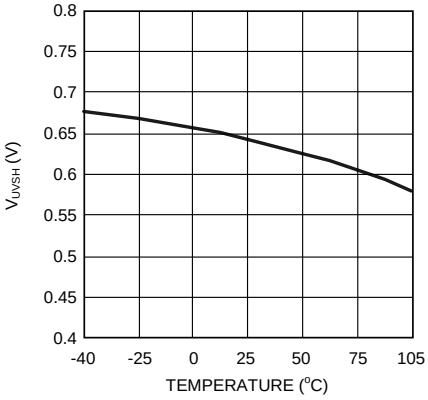


Figure 5.

Under-Voltage Comparator Threshold (V_{UV}) and Over-Voltage Comparator Threshold (V_{OV}) vs Temperature

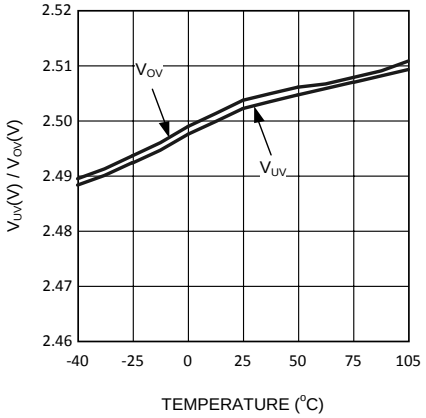


Figure 6.

Under-Voltage Comparator Threshold Hysteresis Current Source (I_{UVHCS}) vs Temperature

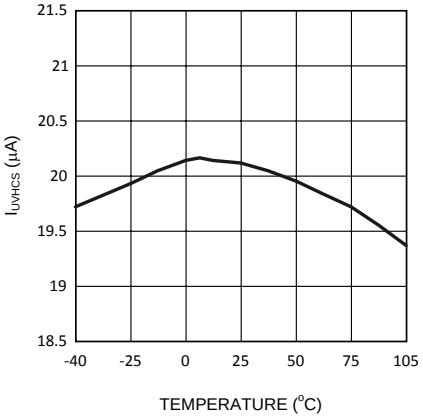


Figure 7.

Typical Performance Characteristics (continued)

Over-Voltage Comparator Threshold Hysteresis Current Sink (I_{OVHCS}) vs Temperature

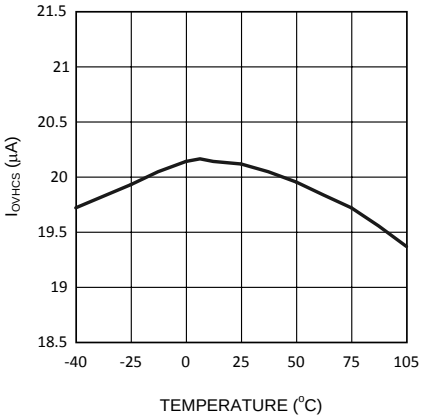


Figure 8.

UV Comparator Delay (t_{UVCD}) and OV Comparator Delay (t_{OVCD}) vs Temperature

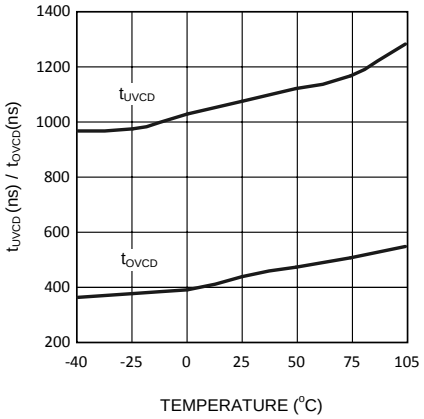


Figure 9.

Circuit Breaker Current Limit Voltage (V_{CB}) vs Temperature

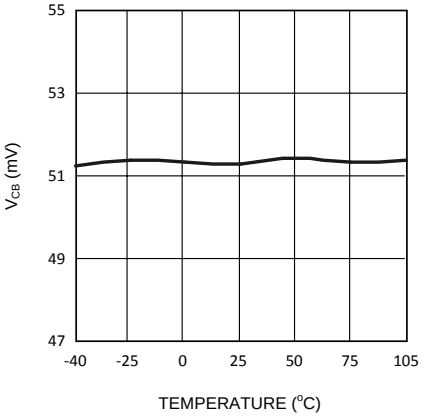


Figure 10.

Analog Current Limit Voltage (V_{AC}) vs Temperature

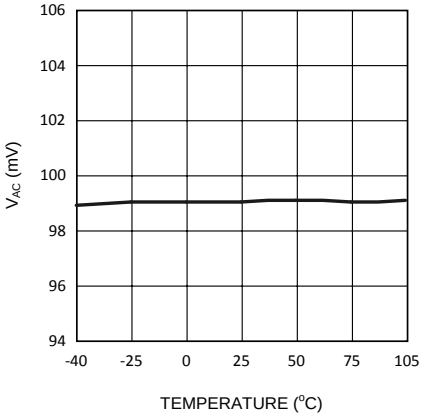


Figure 11.

Fast Discharge Current Limit Voltage (V_{FDC}) vs Temperature

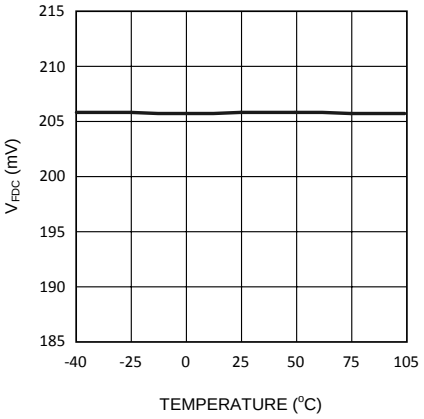


Figure 12.

Timer High Voltage Threshold (V_{THVT}) vs Temperature

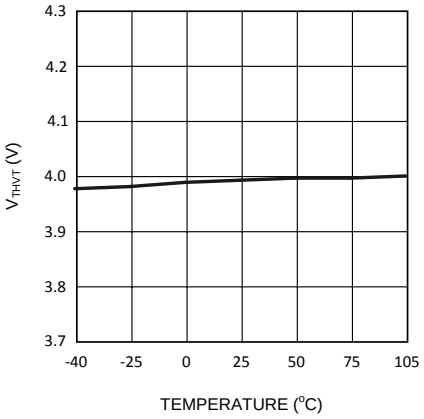


Figure 13.

Typical Performance Characteristics (continued)

Timer Low Voltage Threshold (V_{TLVT}) vs Temperature

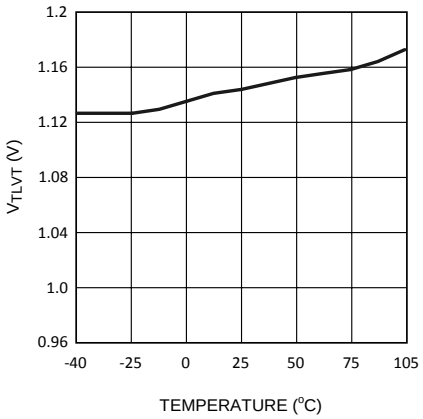


Figure 14.

Timer On (Initial Cycle, Sourcing) vs Temperature

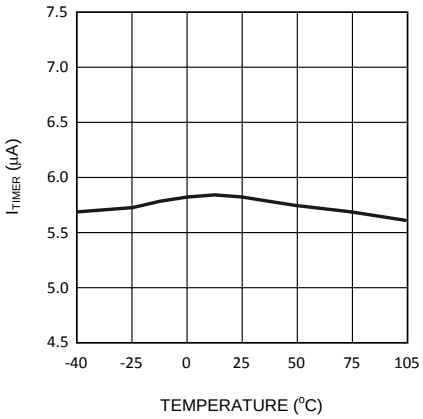


Figure 15.

Timer On (Circuit Breaker, Sourcing) vs Temperature

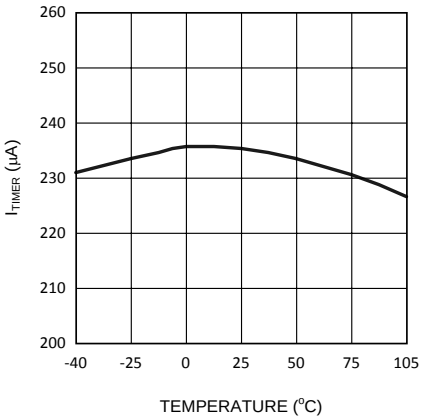


Figure 16.

Timer Off (Cooling Cycle, Sinking) vs Temperature

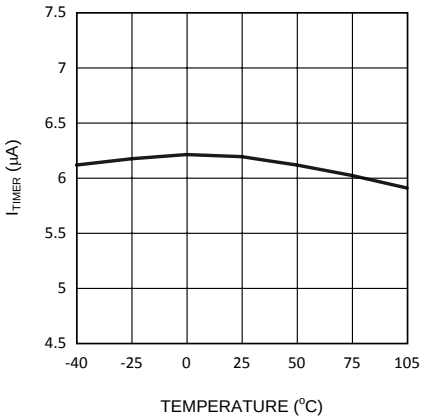


Figure 17.

Saturation Gate Drive Voltage (V_G) vs Temperature (48V)

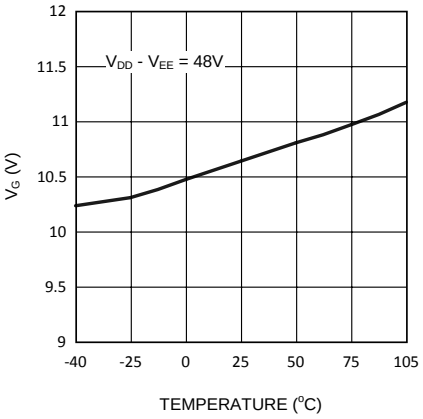


Figure 18.

Saturation Gate Drive Voltage (V_G) vs Temperature

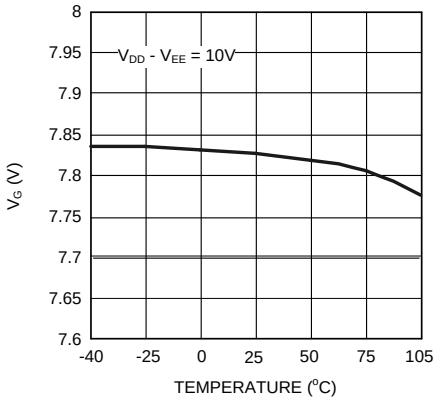


Figure 19.

Typical Performance Characteristics (continued)

Gate Pin Current (Sourcing) (I_{GATE}) vs Temperature

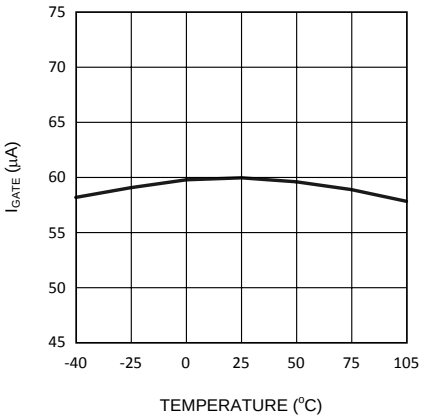


Figure 20.

PWRGD Low Voltage (V_{PGLV}) vs Temperature

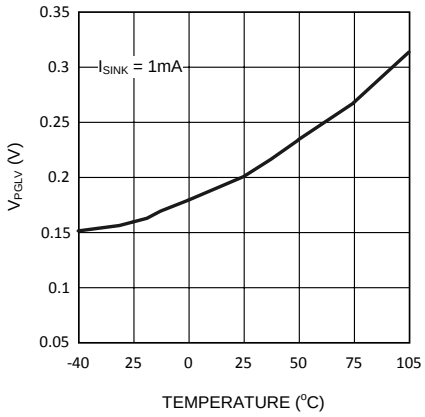


Figure 21.

Gate Voltage at onset of PWRGD (V_{PGV}) vs Temperature

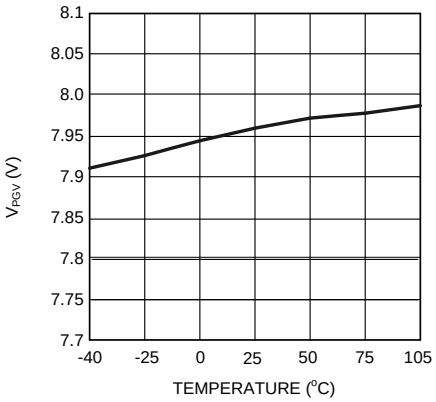


Figure 22.

FUNCTION DESCRIPTION

The LM5068 is designed to facilitate the insertion and removal of circuit cards into live backplanes in a controlled manner. Because the supply bypass capacitors on the circuit card can draw large transient currents, it is critical to control the supply current during insertion to limit system power glitches and connector damage. Controlling in-rush current prevents other boards in the system from resetting during board insertion. Load short-circuit protection is accomplished by active current limiting of the load current. The topology of the LM5068 is illustrated in the simplified application circuit shown in Figure 23.

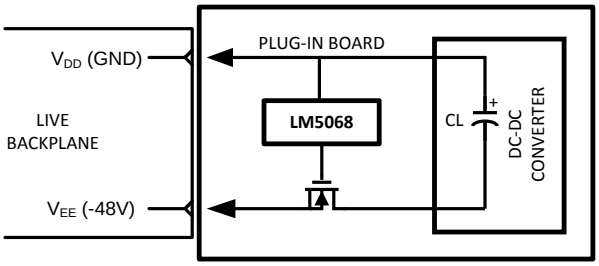


Figure 23. LM5068 Topology

Start-Up Operation

The LM5068 resides on a removable circuit card. Power is applied to the load or power conversion circuitry through an external N-Channel MOSFET switch and current sense resistor.

When power is initially applied to the card, the gate of the external MOSFET is held low. When certain interlock conditions are met, a turn-on sequence begins and an internal 60 µA current source charges the gate of the MOSFET. To initiate the start-up sequence, all of the following interlock conditions must be satisfied:

- The input voltage V_{DD} - V_{EE} exceeds 9V(V_{UVS})
- The voltage at UV is above 2.5V (V_{UV})
- The voltage at OV falls below 2.5V (V_{OV})
- The voltage on the Timer capacitor (C_T) is less than 1V (V_{TLVT})
- The GATE pin is below 0.5V (V_{GLT})

When all of the interlock conditions are met, a 6 µA TIMER current source is enabled to charge the timer capacitor C_T. During this initial timer sequence the GATE output is held low. When the C_T capacitor successfully charges up to 4V, the TIMER circuit resets the timer capacitor to 1V and activates a 60 µA current source (I_{GATE}) into the MOSFET gate.

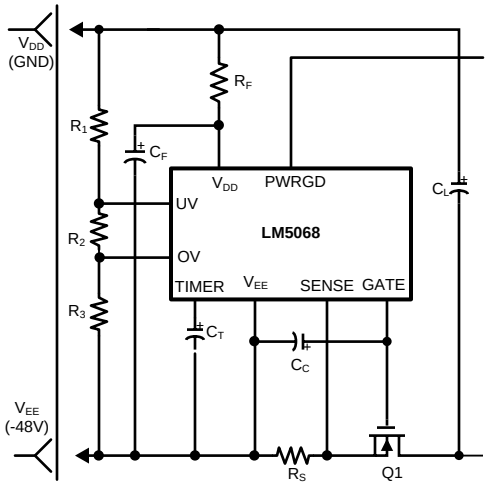


Figure 24. Hot Swap Controller

Over and Under-Voltage Lockout

The line Under-voltage lockout (UVLO) circuitry of the LM5068 monitors V_{DD} for under-voltage conditions, where V_{UVS} is the negative going threshold and the hysteresis is V_{UVSH} (see Electrical Characteristics). A V_{DD} - V_{EE} voltage less than 8.5V (V_{UVS}) keeps the controller in a disabled mode. Raising the V_{DD} voltage above 9.1V (V_{UVS} + V_{UVSH}) releases the V_{DD} UVLO and enables the controller.

In addition to the internal UVLO circuit, the UV and OV comparators monitor the input line voltage through an external resistor divider. Programmable UV and OV comparator hysteresis is implemented with switched 20µA current sources that raise or lower the OV and UV pins when the comparators reach their threshold. Either UV or OV fault conditions will switch the GATE pin low and disconnect the power to the load. To restart the GATE pin, the supply voltage must return to a level which is greater than the UV fault and less than the OV fault threshold and all of the interlock conditions (with the exception of the TIMER) must be met.

Removal of the circuit card from the backplane initiates an under-voltage condition. The series MOSFET is then disabled to disconnect the source of power to the load. The under-voltage threshold and hysteresis are programmed by the external resistor divider connected to the UV pin.

Timer

The value of the C_T capacitor sets the duration of the LM5068's timer delay and filter functions. There are four charging and discharging modes:

1. 6µA slow charge for initial timing delay and post-fault re-try timer (LM5068-2 and -4)
2. 240µA fast charge for circuit breaker delay.
3. 6µA slow discharge for circuit breaker "cool-off".
4. Low impedance switch to reset capacitor after initial timing delay, input under-voltage lockout, and during over-voltage and under-voltage initial timing.

Current Control

The LM5068 has three current sense thresholds which protect the backplane supply and circuit card from overload conditions. The voltage drop across the sense resistor (R_S) is monitored at the SENSE pin. The over-current protection functions are determined through the following three distinct thresholds at the SENSE pin:

1. Circuit Breaker (CB) threshold (typically 50mV)
2. Analog Current Limit (ACL) loop threshold (typically 100mV)
3. Fast Discharge Current (FDC) threshold (typically 200mV)

When the voltage drop across R_S exceeds 50mV the Circuit Breaker comparator indicates an over-load condition. The TIMER sources 240µA into C_T when SENSE exceeds 50mV and sinks 6µA from C_T when SENSE falls below 50mV. If the C_T capacitor ramps to a 4V threshold, a fault condition is declared and the gate of the MOSFET is forced low, disconnecting the power to the load.

Active Current Limiting (ACL) is activated when the voltage across sense resistor R_S reaches 100mV. The LM5068 controls the gate of the MOSFET and maintains a constant output load current equal to 100mV/ R_S. In the ACL mode the SENSE pin is greater than 50mV and the TIMER charges C_T with 240µA. A fault will be declared if the LM5068 remains in the ACL mode longer than the circuit breaker timer period.

Fast Discharge Current (FDC) responds to fast rising over-loads such as short circuit faults. During a short circuit event the fast rising current may overshoot past the ACL threshold due to the finite response time of the ACL loop. If the SENSE voltage reaches 200mV a fast discharge comparator quickly pulls GATE pin low. The rapid response of the FDC circuit assures a fast and safe transition to the ACL mode.

The LM5068 circuit breaker action filters low duty cycle over-load conditions to avoid declaring a fault during short duration load transients. The timer charges capacitor C_T with 240µA when the SENSE voltage is greater than 50mV. When the SENSE pin voltage falls below 50mV, a 6µA current discharges the TIMER capacitor. Repetitive over-current faults with duty cycle greater than 2.5% will eventually charge C_T and trip the fault timer. This feature protects the pass MOSFET which has a fast heating and slow cooling characteristic.

Latch-Off and Auto-Retry

If the fault conditions persist long enough for TIMER to charge C_T to 4V, the LM5068 latches off (LM5068-1, -3) or switches off and initiates the re-try timer (LM5068-2, -4).

At the fault condition, after reaching the 4V, the TIMER pin will continue to ramp-up with 6µA current source until it reaches the internal regulated voltage, which is equivalent to the saturation GATE drive voltage. The LM5068-1 and LM5068-3 remains off until the controller is reset by either temporarily pulling the UV pin low, pulling the TIMER pin below 1 volt, or decreasing the input voltage below the internal V_{DD} under-voltage lockout (UVLO) threshold.

The LM5068-2 and LM5068-4 respond to a fault condition by pulling the GATE and TIMER pins low and then initiating a timer sequence for automatic re-try. The re-try timer sequence begins with C_T capacitor being charged slowly to 4V with a 6µA current source and then discharged quickly to 1V with a 30mA discharge current. After 8 charge/discharge cycles the GATE pin is released and charged with a 60µA current source. If the fault condition persists, the LM5068 will again turn off the MOSFET and another 8-cycle fault timer sequence will begin.

Power Good Flag

The power good flag (PWRGD) is activated when the MOSFET GATE is fully enhanced (>8V) and the voltage input UV and OV comparators are satisfied. The power good output is a 90V capable open drain N-Channel MOSFET. The LM5068-1 and LM5068-2 provide an active HIGH power-good state, while the LM5068-3 and LM5068–4 are configured for an active LOW power-good state. The UV comparator, OV comparator, V_{DD} UVLO, or a circuit breaker time-out will reset the power good flag.

Internal Soft-Start

An internal soft-start feature ramps the (positive) input of the analog current limit amplifier during initial start-up. The ramp duration is approximately 200µs. This feature reduces the load current slew rate (di/dt) at start-up.

Design Information

The LM5068 contains an internal regulator enabling the V_{DD} pin to be connected directly to the line voltage from 10 to 90V. A local RC filter (0.1µF ceramic capacitor and 499Ω resistor) connected between V_{DD} and V_{EE} is recommended to filter supply transients that exceed the 100V Absolute Maximum Rating.

UV and OV Thresholds and Voltage Divider Selection for R1, R2, and R3

Two comparators detect under-voltage and over-voltage conditions at the UV and OV pins. The threshold voltages (V_{UV} , V_{OV}) of the UV and OV comparators are nominally 2.5V. Hysteresis is accomplished by 20µA current sources (I_{UVHCS}), into the external resistor divider connected to the UV and OV pins as shown in Figure 25

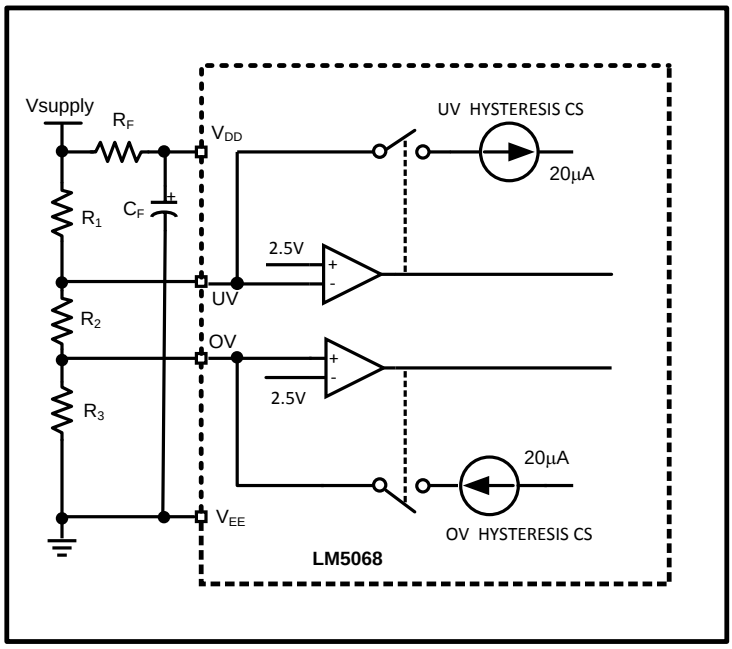


Figure 25. UV/OV Setting

Hysteresis is necessary to prevent a possible “chattering” condition when the controller enables or disables the external MOSFET. The change in line current interacts with the line impedance. This interaction can cause several rapid on/off cycles on the MOSFET. A hysteresis window larger than the line impedance voltage drop prevents this condition.

The impedance seen looking into the resistor divider from the UV and OV pin determines the hysteresis level. UV/OV ON and OFF thresholds are calculated as follow:

$$\text{UV turn-on} = \left(\frac{R_1}{R_2 + R_3} V_{UV}\right) + V_{UV} + I_{UVHCS} R_1 \quad (1)$$

$$\text{UV turn-off} = \frac{R_1 + R_2 + R_3}{R_2 + R_3} V_{UV} \quad (2)$$

$$\text{OV turn-off} = \frac{R_1 + R_2 + R_3}{R_3} V_{OV} \quad (3)$$

$$\text{OV turn-on} = \left[\left(\frac{V_{OV}}{R_3} - I_{UVHCS}\right)(R_1 + R_2)\right] + V_{OV} \quad (4)$$

The independent UV and OV pins provide complete flexibility for the user to select the operational voltage range of the system. However, due to the UV Abs Max rating, the UV and OV thresholds can't be simultaneously set to extremes in one resistor string. For the wide ranges of input voltages (i.e. UV threshold to12V and OV threshold to 90V) it is recommended to use two separate voltage dividers to set the UV and OV thresholds independently.

The typical operating ranges of under-voltage and over-voltage thresholds are calculated from the above equations with known resistors. For example, for resistor values: R1=130KΩ, R2=5.5KΩ, and R3=4.5KΩ, the computed thresholds are:

- UV turn-on = **37.60V**
- UV turn-off = **35.0V**
- OV turn-off = **77.78V**
- OV turn-on = **75.07V**

To maintain the threshold's accuracy, a resistor tolerance of 1% or better is recommended.

Calculation of Normal, Circuit Breaker, and Retry Timing

The C_T capacitor at the TIMER pin controls the timing functions of the LM5068. When the interlock conditions are met the timer capacitor is charged to 4V in a slow initial delay time period t_{IDT} calculated from:

$$t_{IDT} = \frac{4V \times C_T}{6\ \mu A} \tag{5}$$

If the SENSE pin detects more than 50mV across R_S, the TIMER pin charges C_T with 240µA. The Circuit Breaker timeout period t_{CBT} is calculated from:

$$t_{CBT} = \frac{4V \times C_T}{240\mu A} \tag{6}$$

When the LM5068-2 or LM5068-4 is latched, it pulls down the GATE pin and initiates eight, 6µA charging cycles between 1V and 4V on C_T. The total re-try time period t_{RT} is given by:

$$t_{RT} = \frac{8 \times 3V \times C_T}{6\mu A} \tag{7}$$

Sense Resistor (R_S), Timer Capacitor (C_T) and N-Channel Mosfet (Q1) Selection

To select the proper MOSFET, the following safe operating area (SOA) parameters are needed: maximum input voltage, maximum current and the maximum current conduction time.

First, R_S is calculated for the maximum operating load current ($I_{L(MAX)}$) and the minimum circuit breaker trip point ($V_{CB(MIN)}$):

$$R_S = \frac{V_{CB(MIN)}}{I_{L(MAX)}} = \frac{40mV}{I_{L(MAX)}} \quad (8)$$

During the initial charging process, the LM5068 may operate the MOSFET in current limit, forcing $V_{AC(MIN)}$ (80mV) to $V_{AC(MAX)}$ (120mV) across R_S.

The minimum in-rush current and maximum short-circuit limit are calculated from:

$$I_{INRUSH(MIN)} = \frac{80mV}{R_S} \quad (9)$$

$$I_{SHORT\text{-}CIRCUIT(MAX)} = \frac{120mV}{R_S} \quad (10)$$

The value of TIMER capacitor (C_T) is calculated in order to prevent C_T from timing out before the load capacitor is fully charged using the slowest expected charging rate of the load capacitor. Assuming there is no initial resistive loading, the time necessary to charge the load capacitor C_L is calculated from:

$$t_{CL\ CHARGE} = \frac{C_L \times V_{IN(MAX)}}{I_{INRUSH(MIN)}} \quad (11)$$

Applying Equation 9 and Equation 11 to Equation 6 gives the TIMER capacitor value of:

$$C_T = \frac{C_L \times V_{IN(MAX)} \times R_S \times 240\mu A}{4V \times 80mV} \quad (12)$$

Finally, the SOA curves of a prospective MOSFET are checked using $V_{IN\ (MAX)}$, and $I_{SHORT\text{-}CIRCUIT\ (MAX)}$ calculated from equation Equation 10 and time of the current flow from Equation 6.

Example: For: I_L=1A, V_{DD} = 48V, $V_{DD\ (MAX)}$ = 100V and C_L=100µF,

$$R_S = \frac{40mV}{1A} = 40m\Omega \quad (13)$$

$$C_T = \frac{100\mu F \times 100V \times 40m\Omega \times 240\mu A}{4V \times 80mV} = 300nF \quad (14)$$

To account for tolerances of R_S, C_L, TIMER current and TIMER threshold voltage, the computed C_T value should be increased, for this example 50% was selected, therefore:

C_T = 300nF • 1.5 = 450nF

The maximum active current limiting value and duration are:

$$I_{SHORT\text{-}CIRCUIT(MAX)} = \frac{120mV}{40m\Omega} = 3A \quad (15)$$

$$t_{CBT} = \frac{4V \times C_T}{240\mu A} = \frac{4V \times 450nF}{240\mu A} = 7.5ms \quad (16)$$

The N-channel MOSFET selection for use with the LM5068 controller in this example must be capable of sustaining V_{DD}=100V and $I_{(MAX)}$=3A for 7.5ms in the worst case fault condition. A device that meets the established criteria is the Vishay - 5UB85N10-10.

External Sense Resistor

Precise current measurement depends on the accuracy of the sense resistor (R_S). For the optimal results, Kelvin connection and close location of R_S to the LM5068 should be considered. Figure 26 demonstrates PCB layout for the Kelvin sensing.

The R_S power rating should be greater than $I^2_L{}^*R$, where I_L is the normal maximum operating load.

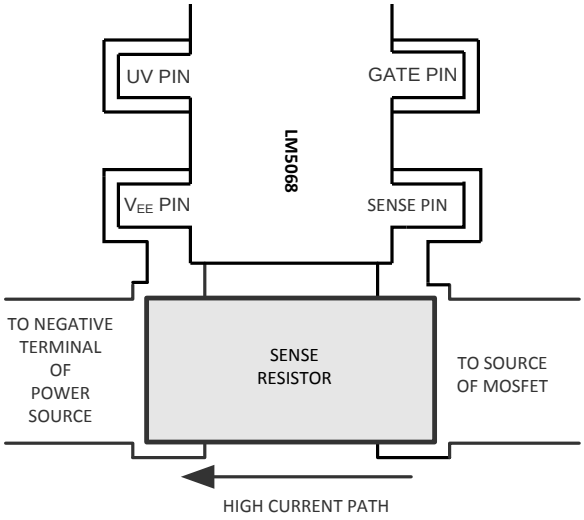


Figure 26. Sense Resistor Connections

Timing Diagrams

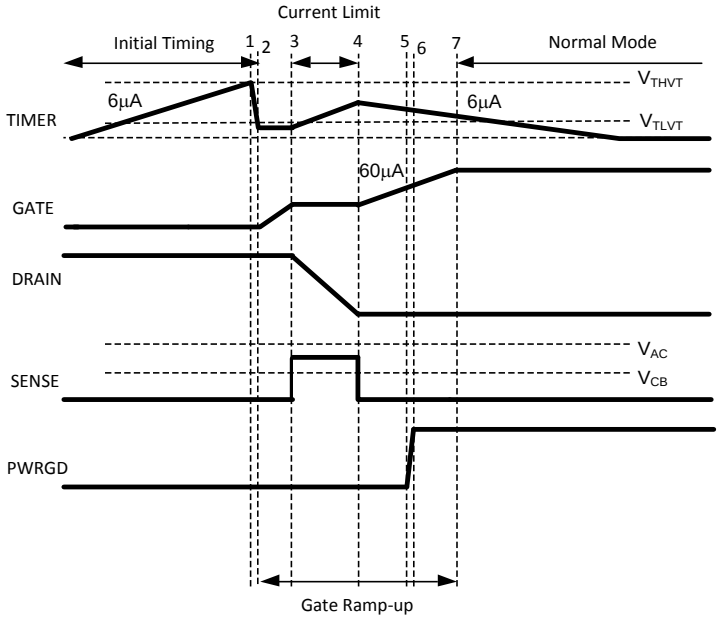


Figure 27. System Power-Up Timing Behavior

Assuming all of the initial conditions are met, the power-up sequence starts with Timer capacitor (C_T) getting charged. C_T is charged with 6µA current source up to V_{THVT} (4V) then quickly discharge to V_{TLVT} (1V). At time point (2) the 60µA GATE current source is enabled. The GATE voltage increases until the MOSFET starts conducting causing the SENSE voltage to increase until Active Current Limiting is activated (3). During the current limiting period (3-4), C_T is charged again, but there is not enough time to reach the 4V threshold before the load capacitor is fully charged and the SENSE voltage falls below V_{CB}. The GATE continues to fully enhance the MOSFET and activating the PWRGD when the GATE voltage exceeds 8V (see Figure 27).

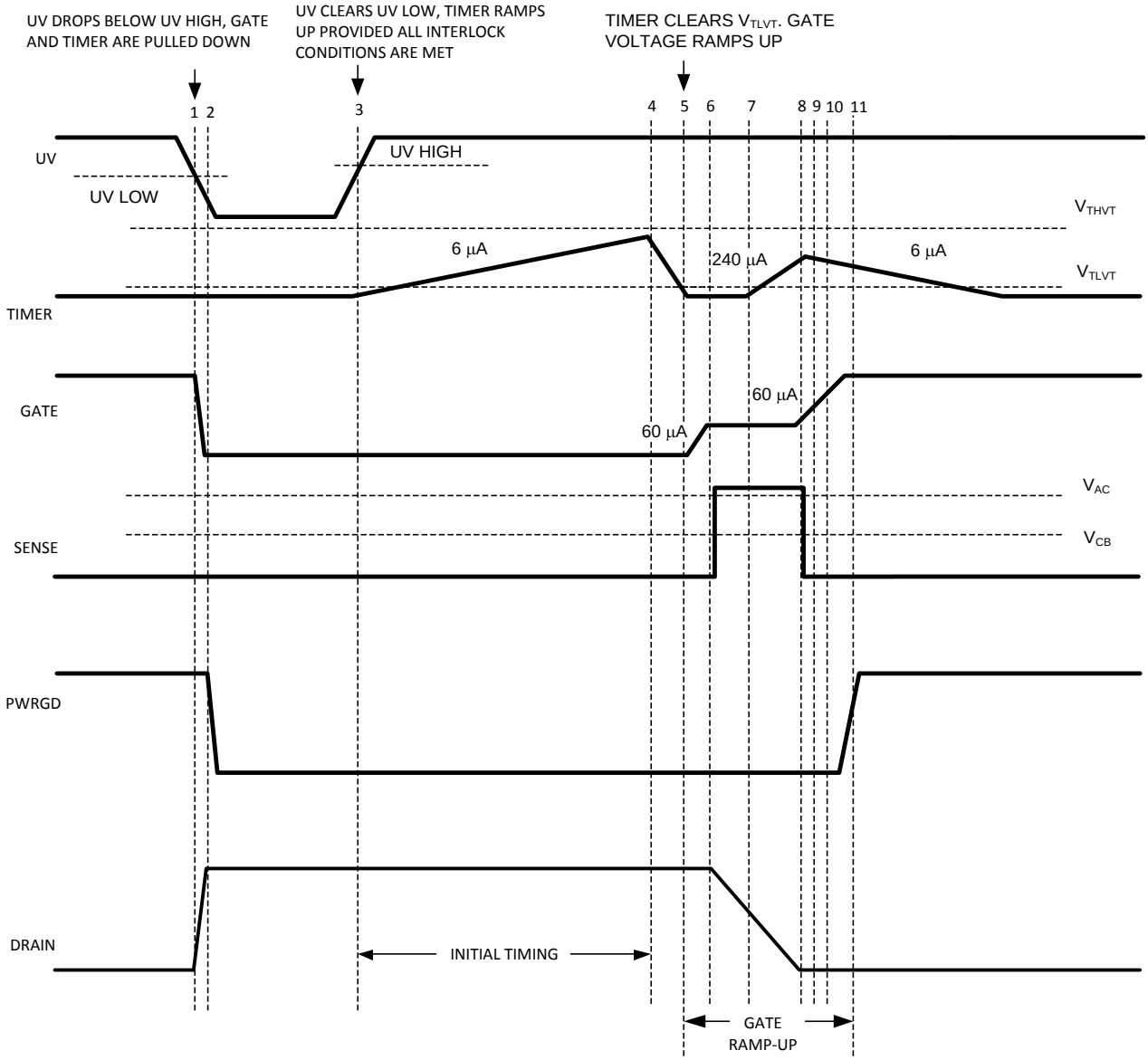


Figure 28. Under-Voltage Timing Behavior

UV drops below UV HIGH (time point 1) puts the controller into a disabled mode. Later, UV increases over the UV LOW threshold (time point 3), which initiates a system power-up sequence.

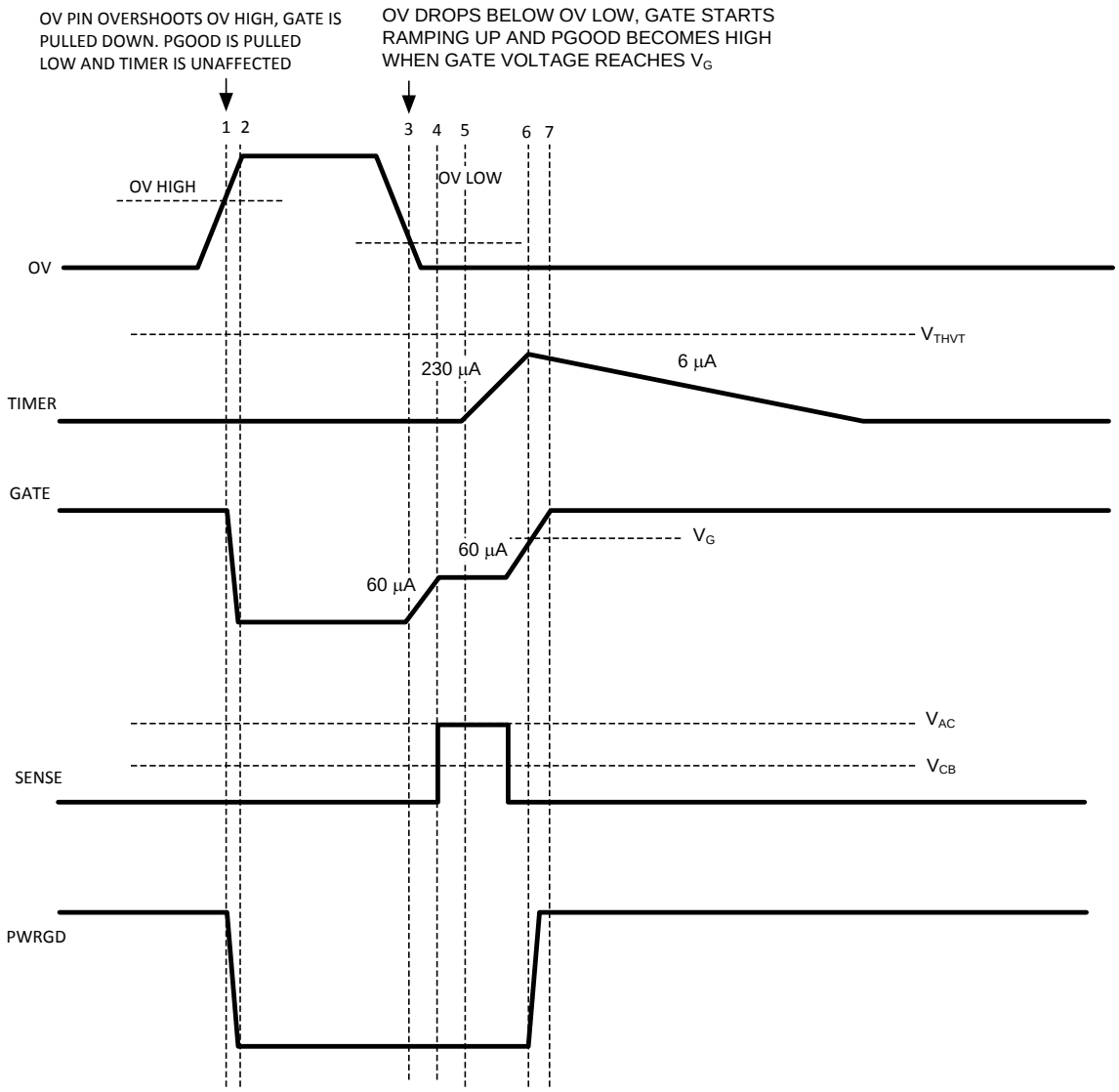


Figure 29. Over-Voltage Timing Behavior

During normal operation, if the OV pin exceeds OV HIGH, as shown at time point 1 in the above diagram, the TIMER status is unaffected. The GATE and PWRGD (for LM5068-1 & -2) pins are pulled low and the load is disconnected. At time point 2, OV recovers and drops below the OV LOW threshold, the GATE start-up cycle begins. If the load capacitor is completely depleted during OV conditions, a full start-up cycle is initiated.

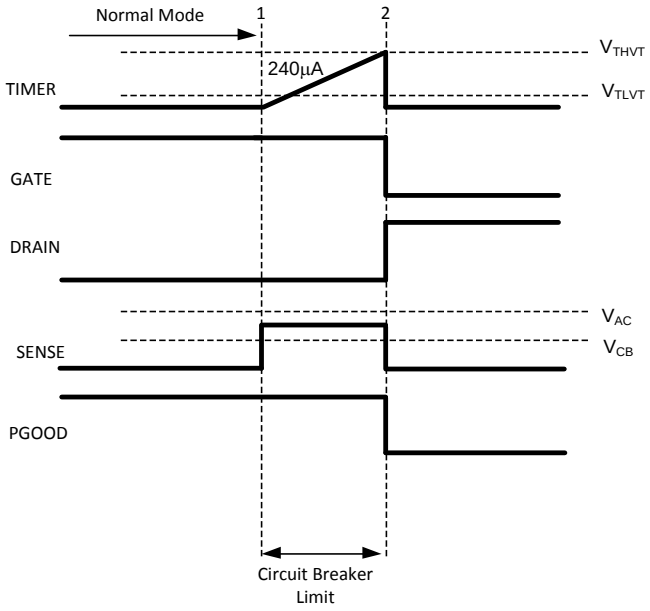


Figure 30. Circuit Breaker Current Limit Fault

The above timing waveform shows the circuit breaker current limit fault behavior. The timer capacitor is charged with 240µA when the SENSE pin exceeds V_{CB}. If the SENSE pin drops below V_{CB} before the TIMER reaches V_{THVT}, the timer capacitor will be discharged with 6µA. In the above figure when TIMER exceeds V_{THVT}, GATE is pulled low immediately to disconnect power to the load.

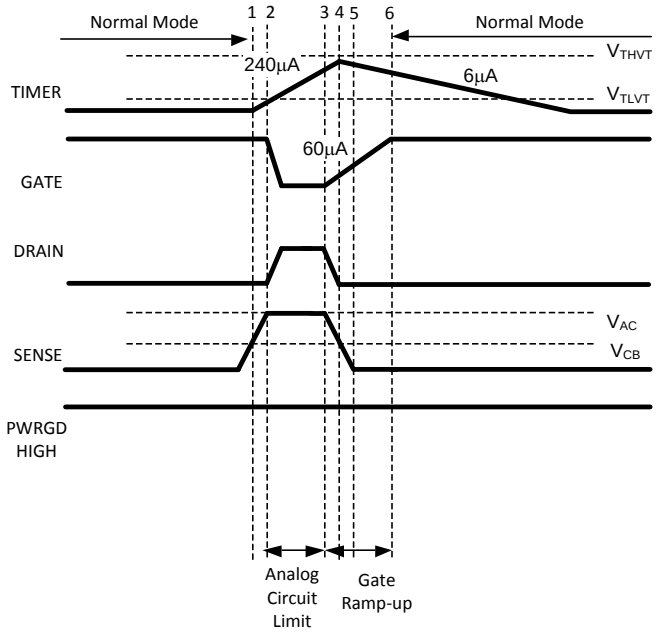


Figure 31. Analog Current Limit Fault

Figure 31 shows analog current limit behavior when the SENSE pin voltage exceeds V_{AC} for a period of time, which activates the Analog Current Limit but never reaches the fault timer threshold. At that time the GATE is regulated by the analog current limit amplifier loop. When the SENSE voltage falls below V_{AC}, GATE is allowed to charge with a 60µA current source. A compensation circuit consisting of a resistor and a capacitor in series, connected between GATE and V_{EE} stabilizes the current limit loop.

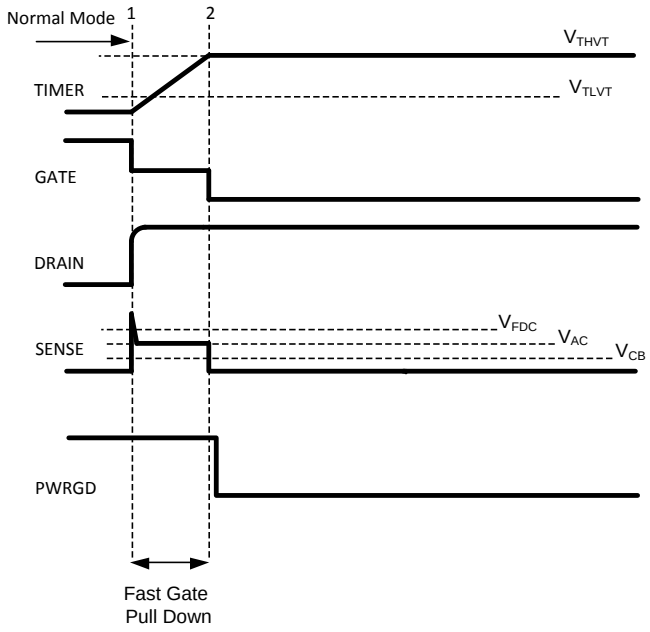


Figure 32. Fast Current Limit Fault

In case of a severe fault (for example sudden short-circuit of the output load) the SENSE pin exceeds the V_{FDC} threshold and GATE immediately pulls down until the Active Current Limit loop establishes control of the current in the MOSFET. Careful selection of TIMER capacitor and MOSFET with adequate current and voltage ratings will prevent damage to MOSFET low impedance faults.

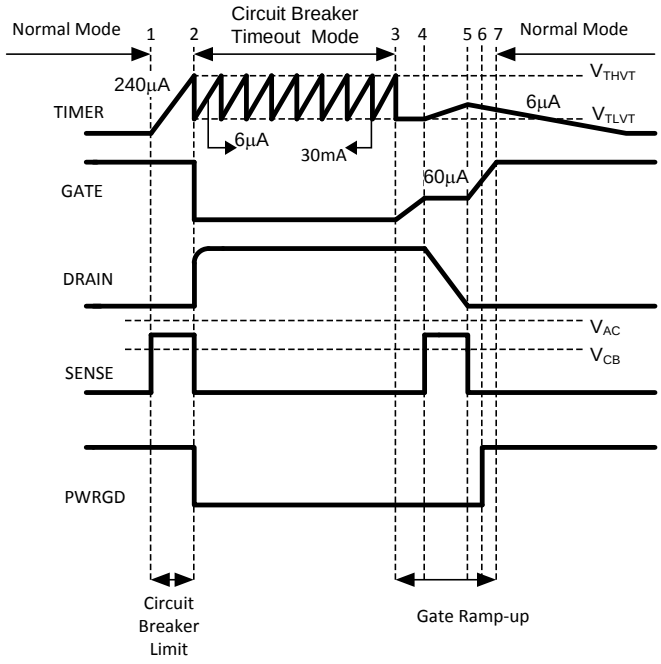
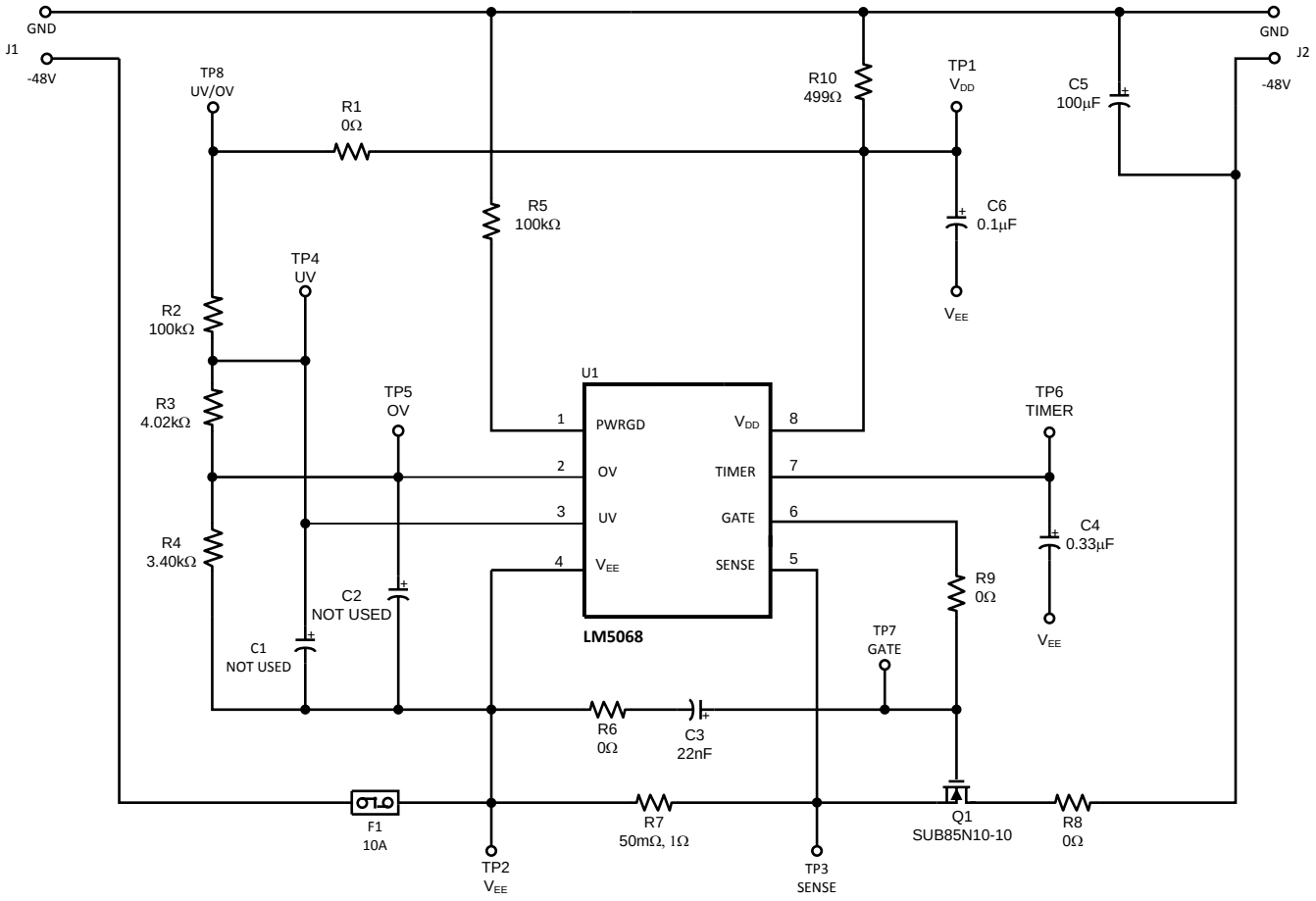


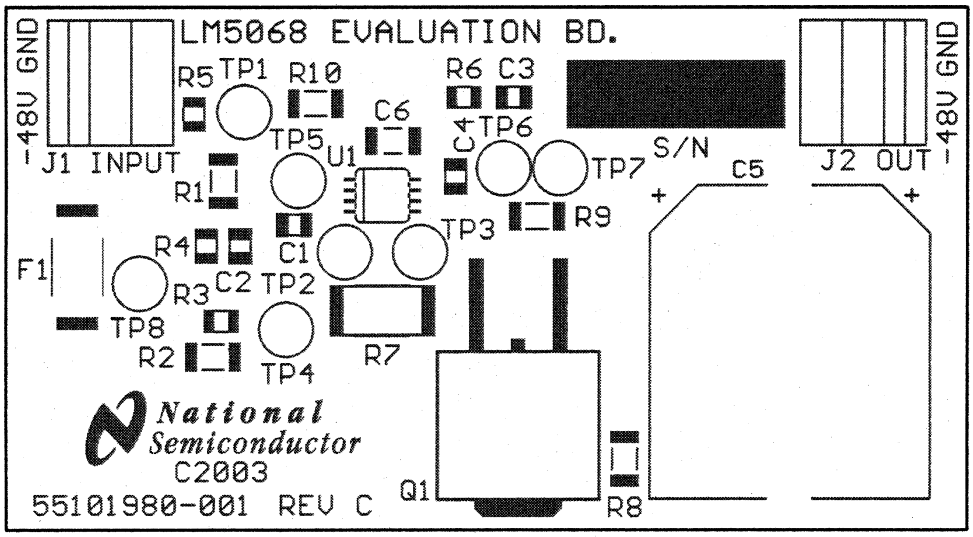
Figure 33. Shutdown Cooling Timing Behavior

Figure 33 shows the timer behavior for LM5068-2, -4 during fault re-try time. During normal operation, whenever the SENSE pin exceeds the 50mV, circuit breaker fault limit, the timer capacitor begins to charge. If the TIMER pin voltage exceeds 4V, the GATE is pulled down immediately, and LM5068-2, -4 disconnects power to the load. The TIMER starts the fault re-try cycle by discharging C_T with 30mA to the V_{TLVT} threshold. The TIMER then charges C_T with 6µA to the V_{THVT} threshold. After eight charging phases and nine discharging phases, LM5068-2, -4 initiates an automatic retry start-up cycle.

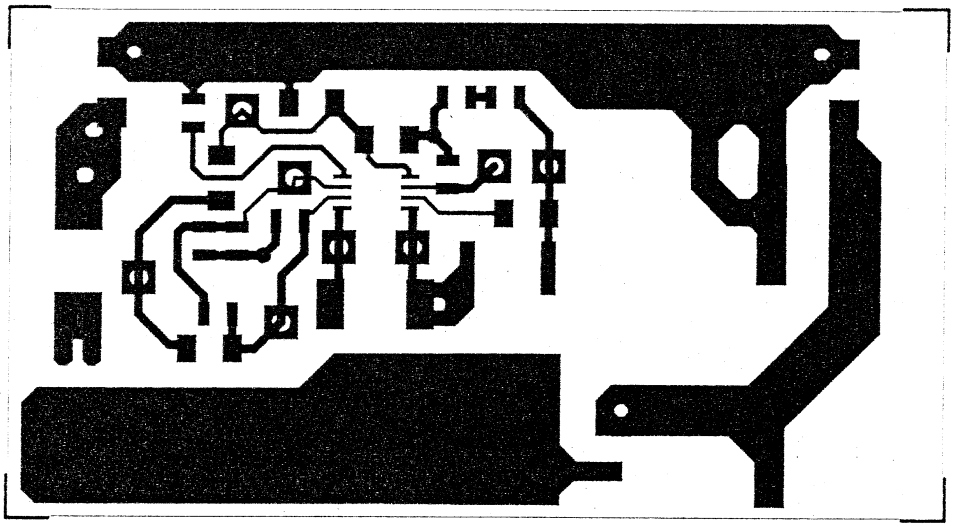
Evaluation Board Schematic



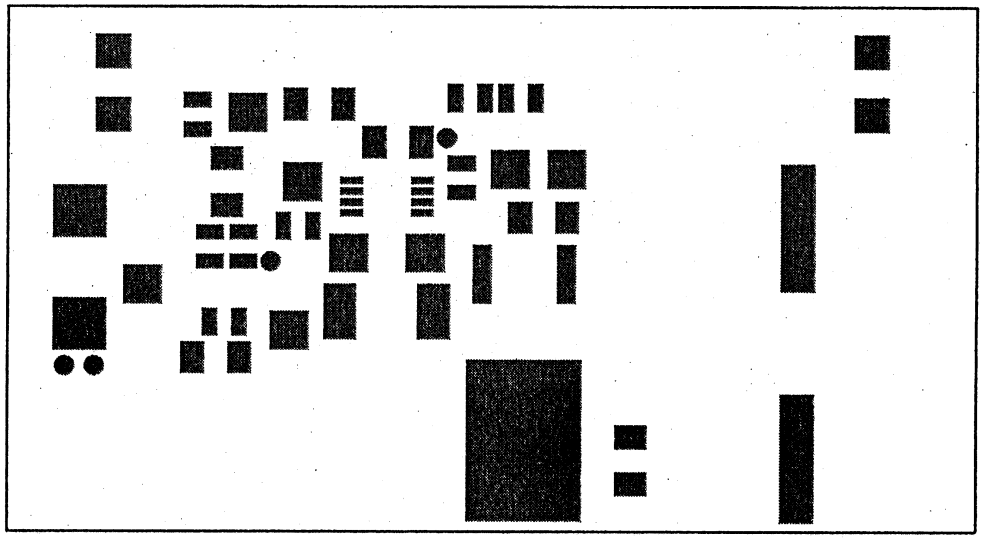
PART	VALUE	PACKAGE	DESCRIPTION	PART NUMBER
C1	NOT USED			
C2	NOT USED			
C3	0.022uF/ 50V	C0805	CAPACITOR, CERAMIC,KEMET	C0805C223K5RAC
C4	0.33uF / 50V	C0805	CAPACITOR,CERAMIC,KEMET	C0805C334K5RAC
C5	100uF / 100V		CAPACITOR, ALUMINIUM ELECTROLYTIC, SURFACE MOUNT,PANASONIC	EEV-FK2A101M
C6	0.1uF / 100V	C1206	CAPACITOR, CERAMIC, TDK	C3216X7R2A104KT
F1	10A FUSE	SMD_FUSE	COOPER BUSSMAN FAST ACTING FUSE TRON	TR/SFT-10 (Digikey # 283-2439-2-ND)
J1	PCB terminal Blocks/ 10A		MOUSER TERMINAL BLOCKS	651-1727010
J2	PCB terminal Blocks/ 10A		MOUSER TERMINAL BLOCKS	651-1727010
Q1	100V / 60A	N-Channel Power MOSFET,TO263	VISHAY	SUB85N10-10
R1	0	R1206	SMD RESISTOR, 1% TOL	CRCW12060000F
R2	100K	R1206	SMD RESISTOR, 1% TOL	CRCW12061003F
R3	4.02K	R0805	SMD RESISTOR, 1% TOL	CRCW08053401F
R4	3.04K	R0805	SMD RESISTOR, 1% TOL	CRCW08053040F
R5	100K	R0805	SMD RESISTOR, 1% TOL	CRCW08051003F
R6	0	R0805	SMD RESISTOR, 1% TOL	CRCW08050000F
R7	50m	R2512	SMD RESISTOR, 1% TOL	WSL-2512 .050F
R8	0	R1206	SMD RESISTOR, 1% TOL	CRCW12060000F
R9	0	R1206	SMD RESISTOR, 1% TOL	CRCW12060000F
R10	499	R1206	SMD RESISTOR, 1% TOL	CRCW1206499RF
U1	LM5068	VSSOP-8	Texas Instruments	LM5068



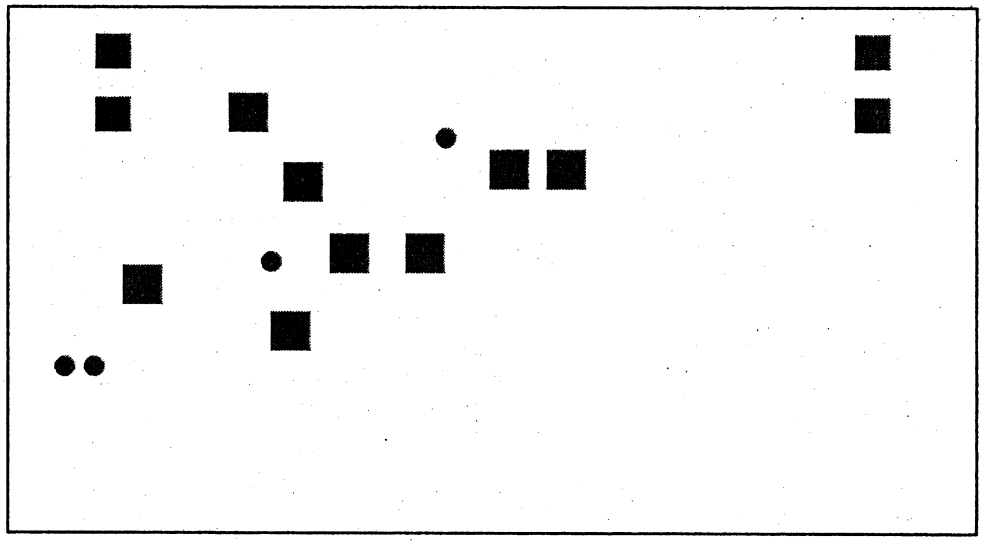
SILKSCREEN (PLACE) LAYER AS VIEWED FROM TOP



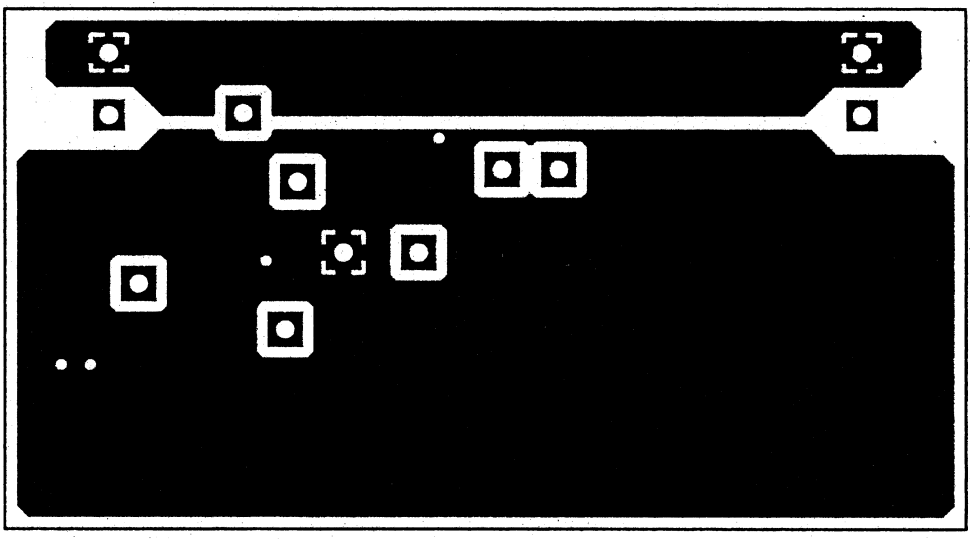
TOP (COMPONENT) LAYER AS VIEWED FROM TOP



TOP SIDE SOLDERMASK AS VIEWED FROM TOP



BOTTOM SIDE SOLDERMASK AS VIEWED FROM TOP



BOTTOM (SOLDER) LAYER AS VIEWED FROM TOP

REVISION HISTORY

Changes from Revision B (March 2013) to Revision C	Page
• Changed layout of National Data Sheet to TI format	26

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM5068MM-2/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	S67B	Samples
LM5068MM-4/NOPB	ACTIVE	VSSOP	DGK	8	1000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	S69B	Samples
LM5068MMX-2/NOPB	ACTIVE	VSSOP	DGK	8	3500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 105	S67B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

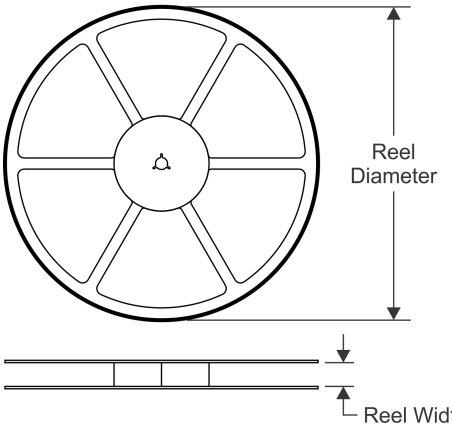
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

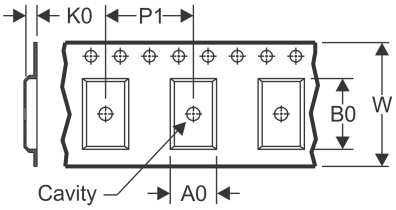
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

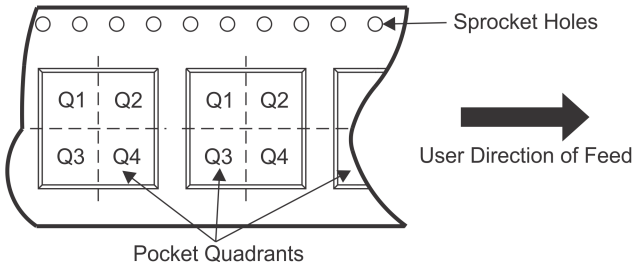


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

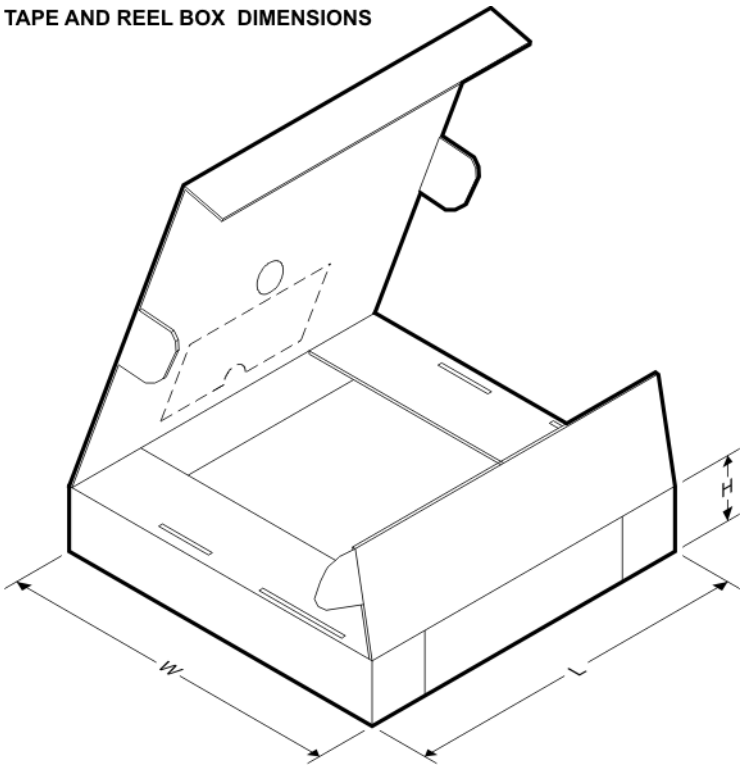
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM5068MM-2/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5068MM-4/NOPB	VSSOP	DGK	8	1000	178.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
LM5068MMX-2/NOPB	VSSOP	DGK	8	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

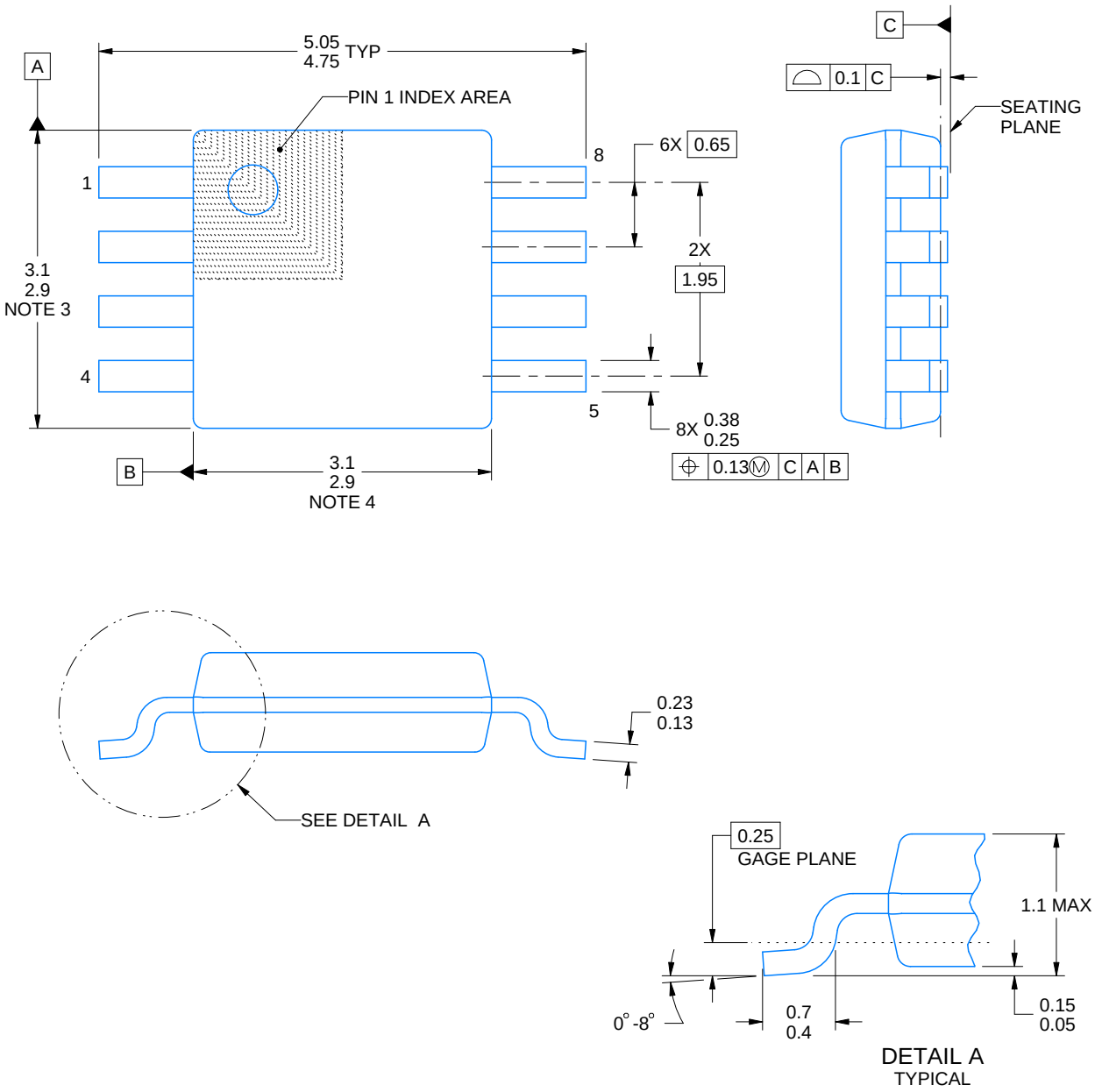
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM5068MM-2/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM5068MM-4/NOPB	VSSOP	DGK	8	1000	208.0	191.0	35.0
LM5068MMX-2/NOPB	VSSOP	DGK	8	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGK0008A

VSSOP - 1.1 mm max height

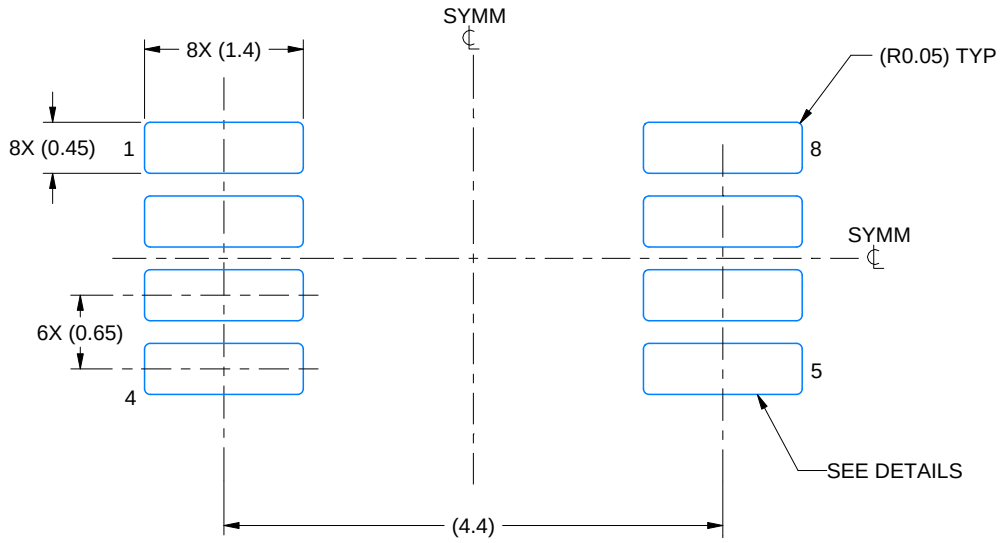
SMALL OUTLINE PACKAGE



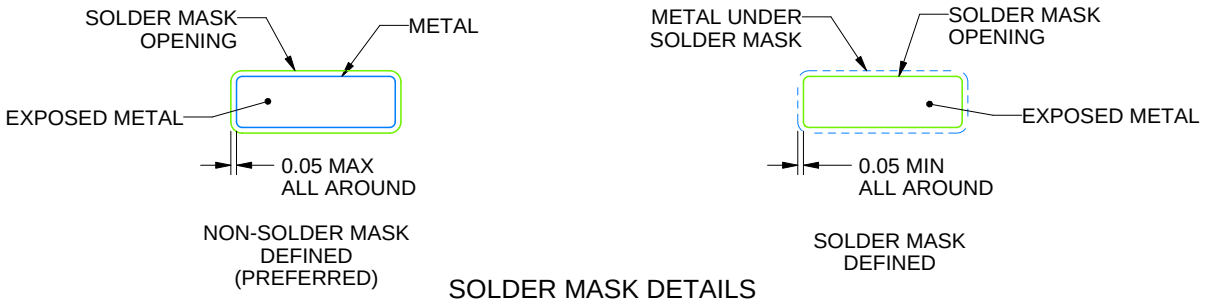
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

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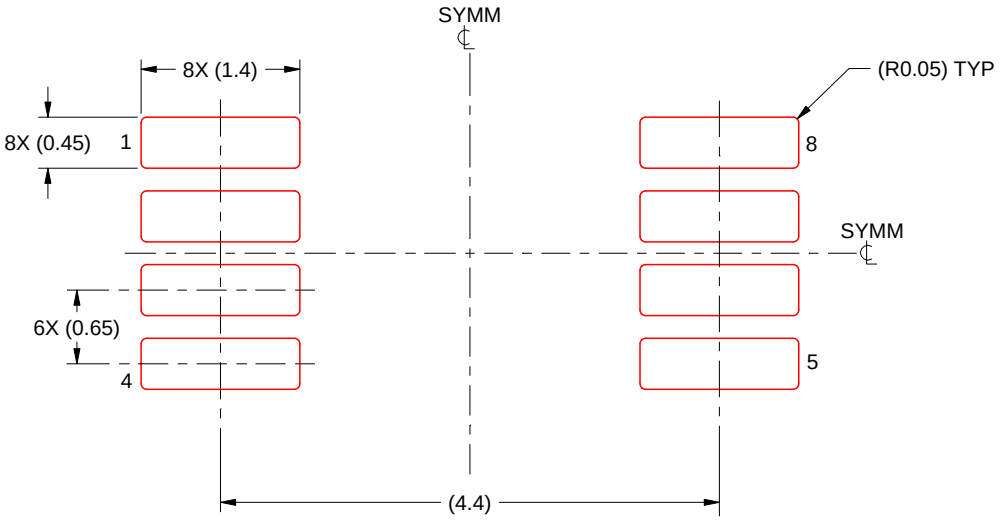
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
SCALE: 15X

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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