THE DATASHEET OF

CLC1010IST5

Data Sheet

COMLINEAR® CLC1010, CLC2010

70µA, Low Cost, 2.5 to 5.5V, 7.3MHz Rail-to-Rail Amplifiers

FEATURES

- 70µA supply current
- 7.3MHz bandwidth
- Input voltage range with 5V supply: -0.3V to 3.8V
- Output voltage range with 5V supply: 0.04V to 4.96V
- 9V/µs slew rate
- 29nV/√Hz input voltage noise
- 4mA linear output current
- Fully specified at 2.7V and 5V supplies
- Competes with low power CMOS amps

APPLICATIONS

- Portable/battery-powered applications
- Mobile communications, cell phones, pagers
- ADC buffer
- Active filters
- Portable test instruments
- Signal conditioning
- Medical Equipment
- Portable medical instrumentation

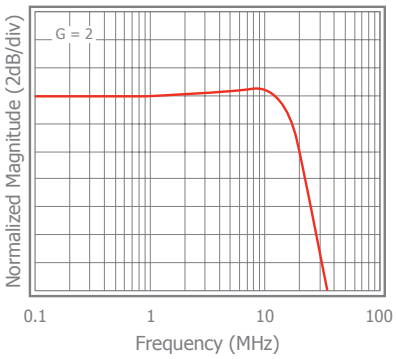
General Description

The COMLINEAR CLC1010 (single) and CLC2010 (dual) are ultra-low power, low cost, voltage feedback amplifiers. These amplifiers use only 70µA of supply current and are designed to operate from a supply range of 2.5V to 5.5V (±1.25 to ±2.75). The input voltage range extends 300mV below the negative rail and 1.2V below the positive rail.

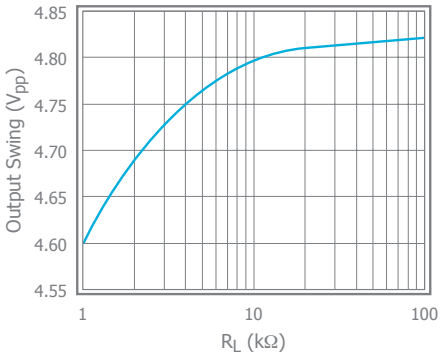
The CLC1010 and CLC2010 offer high bipolar performance at a low CMOS price. They offer superior dynamic performance with a 7.3MHz small signal bandwidth and 9V/µs slew rate. The combination of low power, high bandwidth, and rail-to-rail performance make the CLC1010 and CLC2010 well suited for battery-powered communication/computing systems.

Typical Performance Examples

Frequency Response



Output Swing vs. R_L



Ordering Information

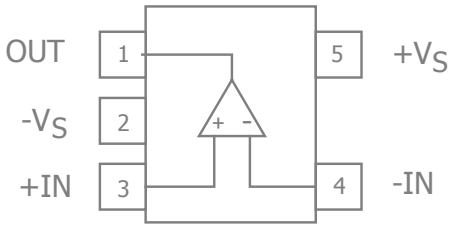
Part Number	Package	Pb-Free	RoHS Compliant	Operating Temperature Range	Packaging Method
CLC1010IST5X	SOT23-5	Yes	Yes	-40°C to +85°C	Reel
CLC1010ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel
CLC2010ISO8X	SOIC-8	Yes	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

Exar Corporation
48720 Kato Road, Fremont CA 94538, USA

www.exar.com
Tel. +1 510 668-7000 - Fax. +1 510 668-7001

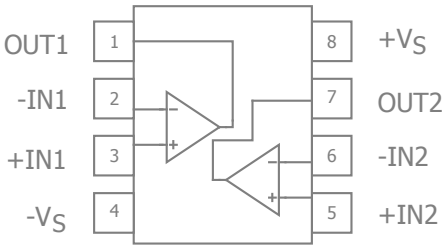
CLC1010 Pin Configuration



CLC1010 Pin Assignments

Pin No.	Pin Name	Description
1	OUT	Output
2	$-V_S$	Negative supply
3	+IN	Positive input
4	-IN	Negative input
5	$+V_S$	Positive supply

CLC2010 Pin Configuration



CLC2010 Pin Configuration

Pin No.	Pin Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative input, channel 1
3	+IN1	Positive input, channel 1
4	$-V_S$	Negative supply
5	+IN2	Positive input, channel 2
6	-IN2	Negative input, channel 2
7	OUT2	Output, channel 2
8	$+V_S$	Positive supply

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Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the "Absolute Maximum Ratings". The device should not be operated at these "absolute" limits. Adhere to the "Recommended Operating Conditions" for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

Parameter	Min	Max	Unit
Supply Voltage	0	6	V
Input Voltage Range	$-V_S$ -0.5V	$+V_S$ +0.5V	V
Continuous Output Current	-30	30	mA

Reliability Information

Parameter	Min	Typ	Max	Unit
Junction Temperature			175	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			260	°C
Package Thermal Resistance				
5-Lead SOT23		221		°C/W
8-Lead SOIC		100		°C/W

Notes:
Package thermal resistance (θ_{JA}), JDEC standard, multi-layer test boards, still air.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2.5		5.5	V

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Electrical Characteristics at +2.7V

T_A = 25°C, V_S = +2.7V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
$UGBW_{SS}$	Unity Gain -3dB Bandwidth	G = +1, V_{OUT} = 0.05V_{pp} , R_f = 0		6.5		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} < 0.2V_{pp}		3		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		2		MHz
GBWP	Gain Bandwdith Product	G = +11, V_{OUT} = 0.2V_{pp}		3.5		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step; (10% to 90%)		55		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		700		ns
OS	Overshoot	V_{OUT} = 1V step		7		%
SR	Slew Rate	2V step, G = -1		7		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 1V_{pp}, 100kHz		-68		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 1V_{pp}, 100kHz		-65		dBc
THD	Total Harmonic Distortion	V_{OUT} = 1V_{pp}, 100kHz		63		dB
e_n	Input Voltage Noise	> 10kHz		30		nV/√Hz
X_{TALK}	Crosstalk	V_{OUT} = 0.2V_{pp}, 10kHz		89		dB
DC Performance						
V_{IO}	Input Offset Voltage (1)		-5	1	5	mV
dV_{IO}	Average Drift			3		µV/°C
I_b	Input Bias Current (1)		-250	90	250	nA
dI_b	Average Drift			100		pA/°C
I_{OS}	Input Offset Current (1)			2.1	100	nA
PSRR	Power Supply Rejection Ratio (1)	DC	58	63		dB
A_{OL}	Open-Loop Gain	V_{OUT} = V_S / 2	65	82		dB
I_S	Supply Current (1)	per channel		62	95	µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		>10		MΩ
C_{IN}	Input Capacitance			1.4		pF
CMIR	Common Mode Input Range			-0.3 to 1.5		V
CMRR	Common Mode Rejection Ratio	DC, V_{CM} = 0V to V_S - 1.5	68	95		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 2kΩ to V_S / 2		0.07 to 2.6		V
		R_L = 10kΩ to V_S / 2 (1)	0.15 to 2.55	0.035 to 2.665		V
I_{OUT}	Output Current			±4		mA
I_{SC}	Short Circuit Output Current			±9		mA

Notes:

1. 100% tested at 25°C

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Electrical Characteristics at +5V

T_A = 25°C, V_S = +5V, R_f = R_g =10kΩ, R_L = 10kΩ to V_S/2, G = 2; unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Frequency Domain Response						
$UGBW_{SS}$	Unity Gain -3dB Bandwidth	G = +1, V_{OUT} = 0.05V_{pp} , R_f = 0		7.3		MHz
BW_{SS}	-3dB Bandwidth	G = +2, V_{OUT} < 0.2V_{pp}		3.4		MHz
BW_{LS}	Large Signal Bandwidth	G = +2, V_{OUT} = 2V_{pp}		2.5		MHz
GBWP	Gain Bandwdith Product	G = +11, V_{OUT} = 0.2V_{pp}		4		MHz
Time Domain Response						
t_R, t_F	Rise and Fall Time	V_{OUT} = 0.2V step; (10% to 90%)		50		ns
t_S	Settling Time to 0.1%	V_{OUT} = 1V step		600		ns
OS	Overshoot	V_{OUT} = 1V step		4		%
SR	Slew Rate	2V step, G = -1		9		V/µs
Distortion/Noise Response						
HD2	2nd Harmonic Distortion	V_{OUT} = 2V_{pp}, 100kHz		-67		dBc
HD3	3rd Harmonic Distortion	V_{OUT} = 2V_{pp}, 100kHz		-60		dBc
THD	Total Harmonic Distortion	V_{OUT} = 2V_{pp}, 100kHz		59		dB
e_n	Input Voltage Noise	> 10kHz		29		nV/√Hz
X_{TALK}	Crosstalk	V_{OUT} = 0.2V_{pp}, 10kHz		89		dB
DC Performance						
V_{IO}	Input Offset Voltage			1		mV
dV_{IO}	Average Drift			8		µV/°C
I_b	Input Bias Current			90		nA
dI_b	Average Drift			100		pA/°C
I_{OS}	Input Offset Current			1.3		nA
PSRR	Power Supply Rejection Ratio (1)	DC	58	63		dB
A_{OL}	Open-Loop Gain	V_{OUT} = V_S / 2		76		dB
I_S	Supply Current	per channel		70		µA
Input Characteristics						
R_{IN}	Input Resistance	Non-inverting		>10		MΩ
C_{IN}	Input Capacitance			1.25		pF
CMIR	Common Mode Input Range			-0.3 to 3.8		V
CMRR	Common Mode Rejection Ratio (1)	DC, V_{CM} = 0V to V_S - 1.5		97		dB
Output Characteristics						
V_{OUT}	Output Voltage Swing	R_L = 2kΩ to V_S / 2		0.09 to 4.9		V
		R_L = 10kΩ to V_S / 2		0.04 to 4.96		V
I_{OUT}	Output Current			±4		mA
I_{SC}	Short Circuit Output Current			±9		mA

Notes:

1. 100% tested at 25°C

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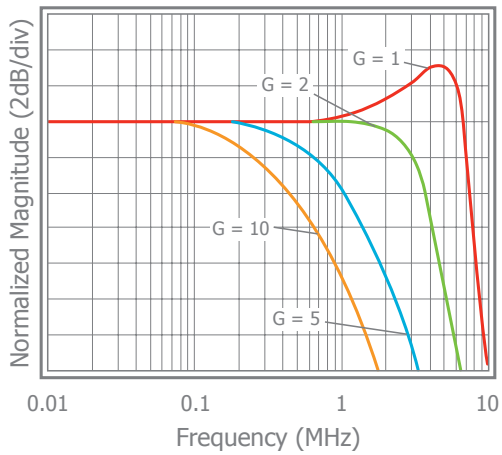
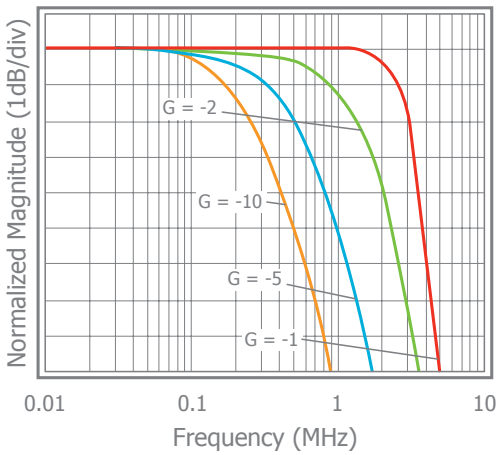
Typical Performance Characteristics

T_A = 25°C, V_S = +5V, R_f = R_g =2.5kΩ, R_L = 2kΩ to V_S/2, G = 2; unless otherwise noted.

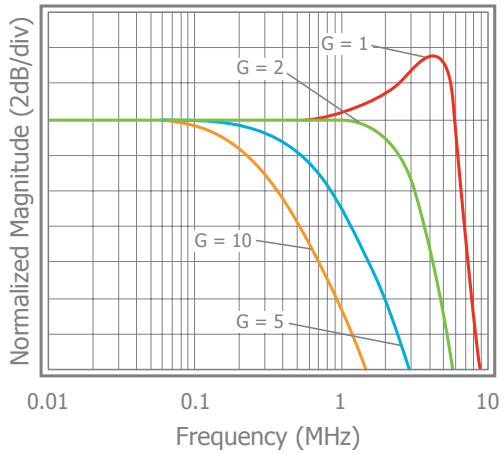
Non-Inverting Frequency Response



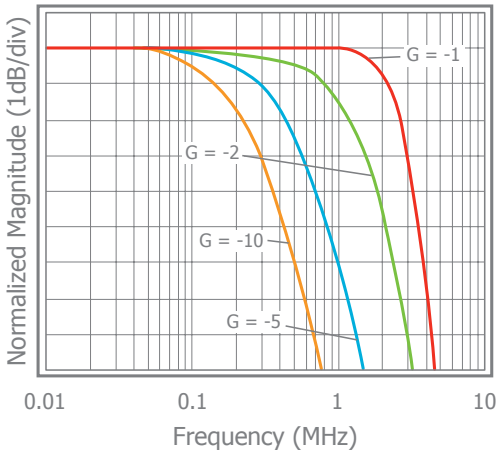
Inverting Frequency Response



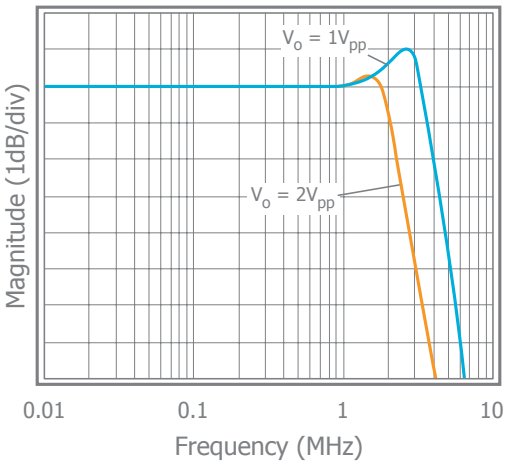
Non-Inverting Frequency Response at V_S = 2.7V



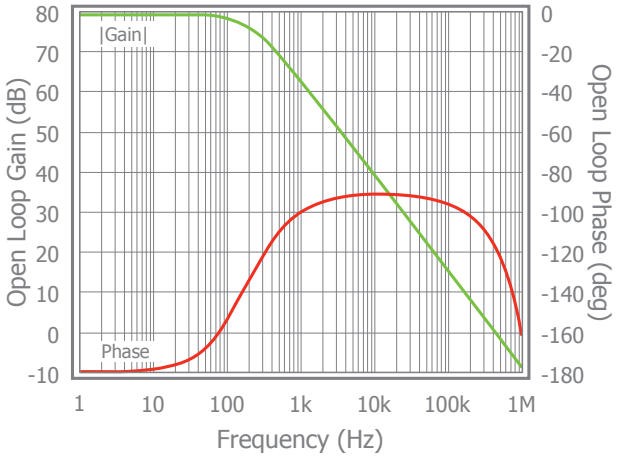
Inverting Frequency Response at V_S = 2.7V



Frequency Response vs. V_{OUT}



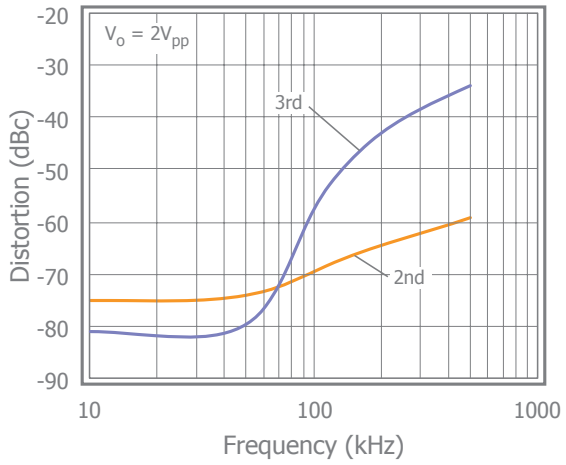
Open Loop Gain & Phase vs. Frequency



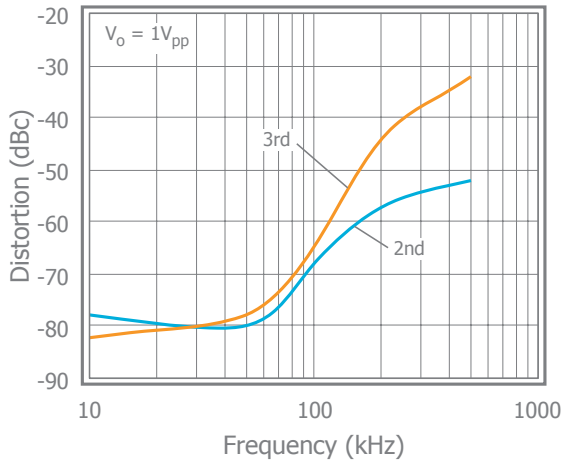
Typical Performance Characteristics

T_A = 25°C, V_S = +5V, R_f = R_g =2.5kΩ, R_L = 2kΩ to V_S/2, G = 2; unless otherwise noted.

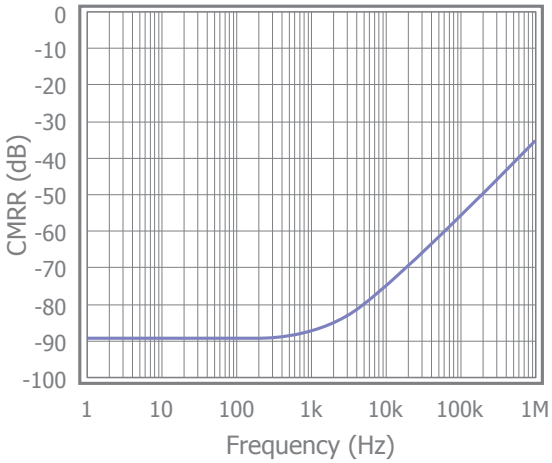
2nd & 3rd Harmonic Distortion



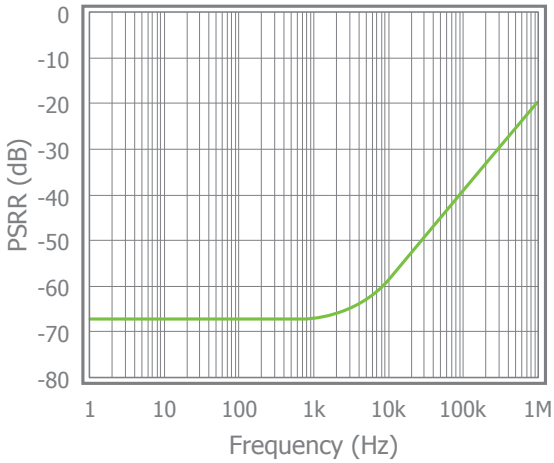
2nd & 3rd Harmonic Distortion at V_S = 2.7V



CMRR

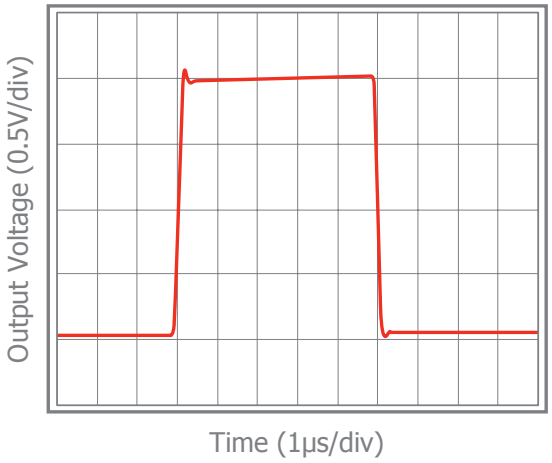


PSRR



Crosstalk vs Frequency

Large Signal Pulse Response



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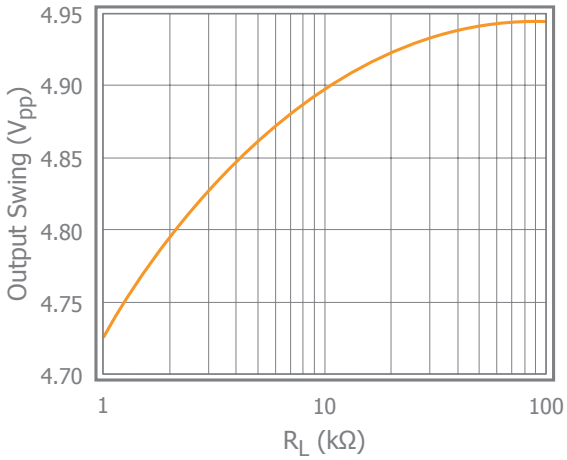
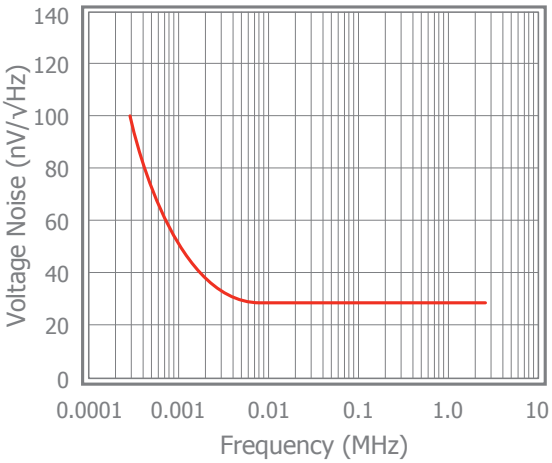
Typical Performance Characteristics - Continued

T_A = 25°C, V_s = +5V, R_f = R_g =2.5kΩ, R_L = 2kΩ to V_S/2, G = 2; unless otherwise noted.

Output Swing vs. R_L



Input Voltage Noise



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Application Information

General Description

The CLC1010 family are a single supply, general purpose, voltage-feedback amplifiers fabricated on a complementary bipolar process. The CLC1010 offers 7.3MHz unity gain bandwidth, 9V/µs slew rate, and only 70µA supply current. It features a rail-to-rail output stage and is unity gain stable.

The design utilizes a patent pending topology that provides increased slew rate performance. The common mode input range extends to 300mV below ground and to 1.2V below Vs. Exceeding these values will not cause phase reversal. However, if the input voltage exceeds the rails by more than 0.5V, the input ESD devices will begin to conduct. The output will stay at the rail during this overdrive condition.

The design uses a Darlington output stage. The output stage is short circuit protected and offers "soft" saturation protection that improves recovery time.

Figures 1, 2, and 3 illustrate typical circuit configurations for non-inverting, inverting, and unity gain topologies for dual supply applications. They show the recommended bypass capacitor values and overall closed loop gain equations. Figure 4 shows the typical non-inverting gain circuit for single supply applicaitons.

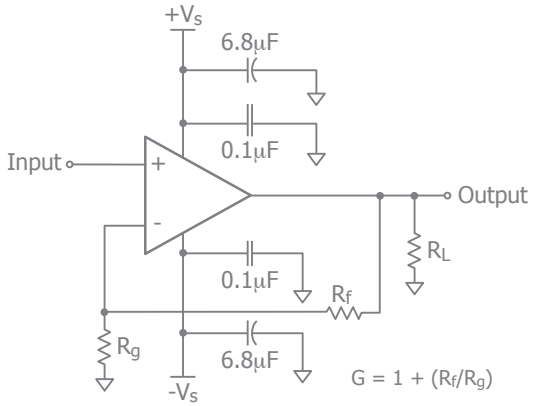

Figure 1. Typical Non-Inverting Gain Circuit

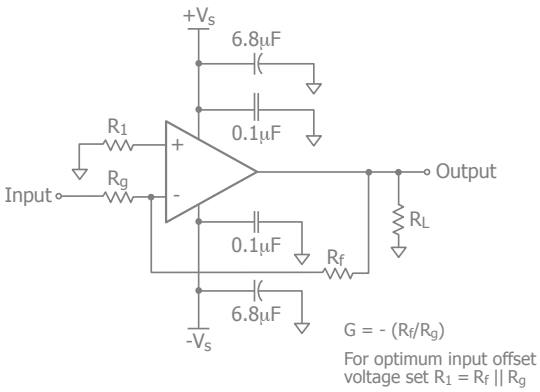

Figure 2. Typical Inverting Gain Circuit

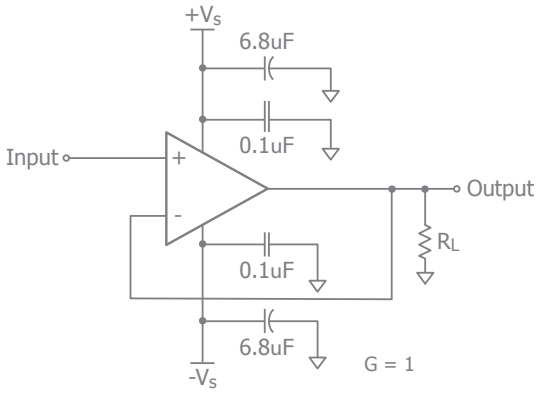

Figure 3. Unity Gain Circuit

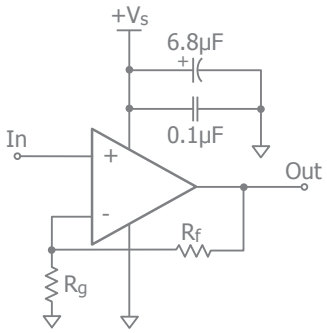

Figure 4. Single Supply Non-Inverting Gain Circuit

Power Dissipation

Power dissipation should not be a factor when operating under the stated 2kΩ load condition. However, applications with low impedance, DC coupled loads should be analyzed to ensure that maximum allowed junction temperature is not exceeded. Guidelines listed below can be used to verify that the particular application will not cause the device to operate beyond it's intended operating range.

Maximum power levels are set by the absolute maximum junction rating of 150°C. To calculate the junction temperature, the package thermal resistance value $Theta_{JA}$ (Θ_{JA}) is used along with the total die power dissipation.

$$T_{Junction} = T_{Ambient} + (\Theta_{JA} \times P_D)$$

Where $T_{Ambient}$ is the temperature of the working environment.

In order to determine P_D, the power dissipated in the load needs to be subtracted from the total power delivered by the supplies.

$$P_D = P_{supply} - P_{load}$$

Supply power is calculated by the standard power equation.

$$P_{supply} = V_{supply} \times I_{RMS\ supply}$$

$$V_{supply} = V_{S+} - V_{S-}$$

Power delivered to a purely resistive load is:

$$P_{load} = ((V_{LOAD})_{RMS}^2)/Rload_{eff}$$

The effective load resistor ($Rload_{eff}$) will need to include the effect of the feedback network. For instance,

$Rload_{eff}$ in Figure 3 would be calculated as:

$$R_L \,||\, (R_f + R_g)$$

These measurements are basic and are relatively easy to perform with standard lab equipment. For design purposes however, prior knowledge of actual signal levels and load impedance is needed to determine the dissipated power. Here, P_D can be found from

$$P_D = P_{Quiescent} + P_{Dynamic} - P_{Load}$$

Quiescent power can be derived from the specified I_S values along with known supply voltage, V_{Supply}. Load power can be calculated as above with the desired signal amplitudes using:

$$(V_{LOAD})_{RMS} = V_{PEAK} / \sqrt{2}$$

$$(I_{LOAD})_{RMS} = (V_{LOAD})_{RMS} / Rload_{eff}$$

The dynamic power is focused primarily within the output stage driving the load. This value can be calculated as:

$$P_{DYNAMIC} = (V_{S+} - V_{LOAD})_{RMS} \times (I_{LOAD})_{RMS}$$

Assuming the load is referenced in the middle of the power rails or $V_{supply}/2$.

The CLC1010 is short circuit protected. However, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. Figure 5 shows the maximum safe power dissipation in the package vs. the ambient temperature for the packages available.

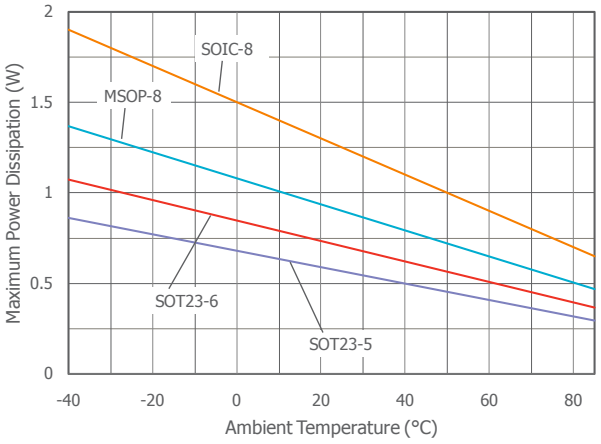

Figure 5. Maximum Power Derating

Driving Capacitive Loads

Increased phase delay at the output due to capacitive loading can cause ringing, peaking in the frequency response, and possible unstable behavior. Use a series resistance, R_S, between the amplifier and the load to help improve stability and settling performance. Refer to Figure 6.

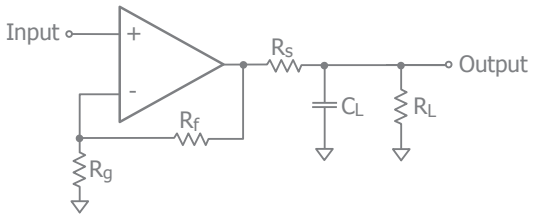

Figure 6. Addition of R_S for Driving Capacitive Loads

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Overdrive Recovery

An overdrive condition is defined as the point when either one of the inputs or the output exceed their specified voltage range. Overdrive recovery is the time needed for the amplifier to return to its normal or linear operating point. The recovery time varies, based on whether the input or output is overdriven and by how much the range is exceeded. The CLC1010 and CLC2010 will typically recover in less than 60ns from an overdrive condition.

Layout Considerations

General layout and supply bypassing play major roles in high frequency performance. CADEKA has evaluation boards to use as a guide for high frequency layout and as an aid in device testing and characterization. Follow the steps below as a basis for high frequency layout:

- Include 6.8µF and 0.1µF ceramic capacitors for power supply decoupling
- Place the 6.8µF capacitor within 0.75 inches of the power pin
- Place the 0.1µF capacitor within 0.1 inches of the power pin
- Remove the ground plane under and around the part, especially near the input and output pins to reduce parasitic capacitance
- Minimize all trace lengths to reduce series inductances

Refer to the evaluation board layouts below for more information.

Evaluation Board Information

The following evaluation boards are available to aid in the testing and layout of these devices:

Evaluation Board	Products
CEB002	CLC1010 in SOT23
CEB003	CLC1010 in SOIC
CEB006	CLC2010 in SOIC

Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 8-14. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short -Vs to ground.
2. Use C3 and C4, if the $-V_S$ pin of the amplifier is not directly connected to the ground plane.

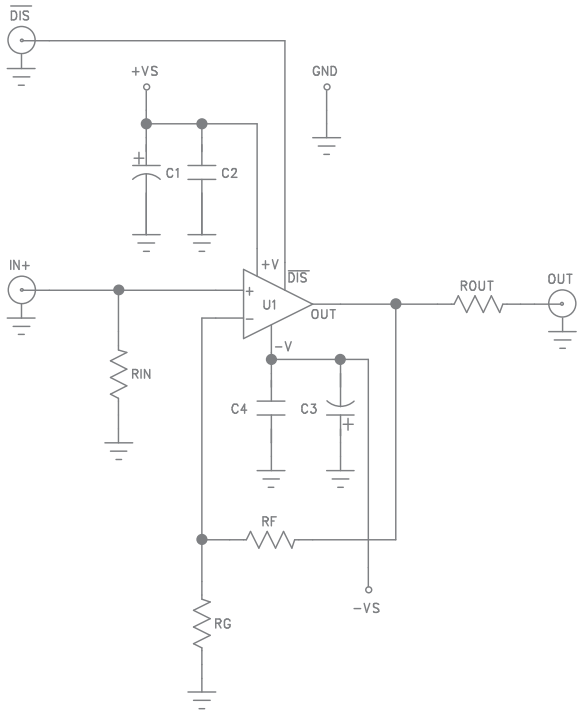


Figure 8. CEB002 & CEB003 Schematic

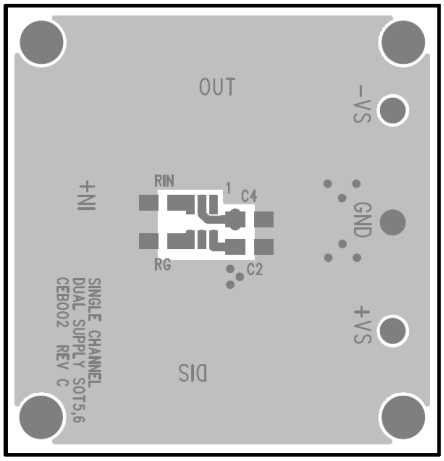


Figure 9. CEB002 Top View

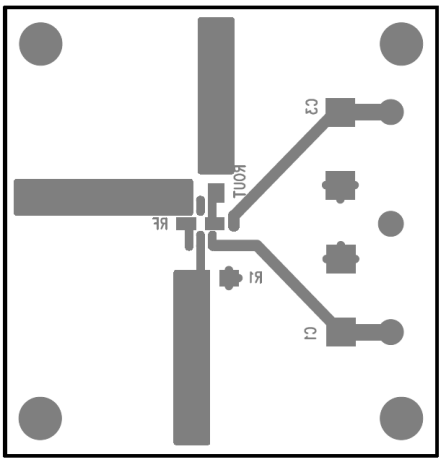


Figure 10. CEB002 Bottom View

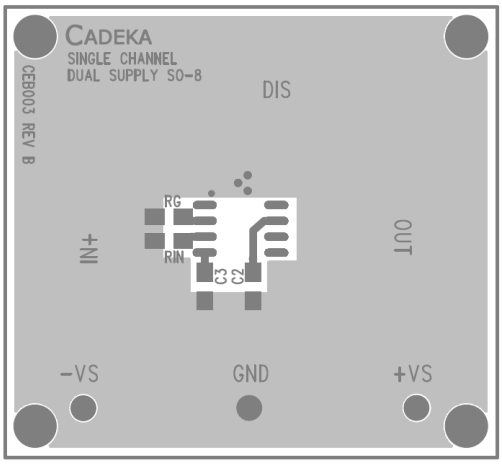


Figure 11. CEB003 Top View

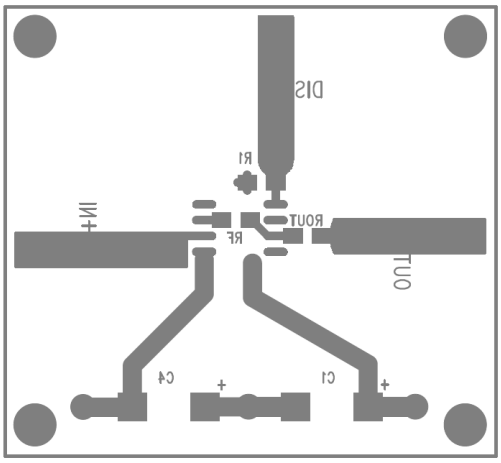


Figure 12. CEB003 Bottom View

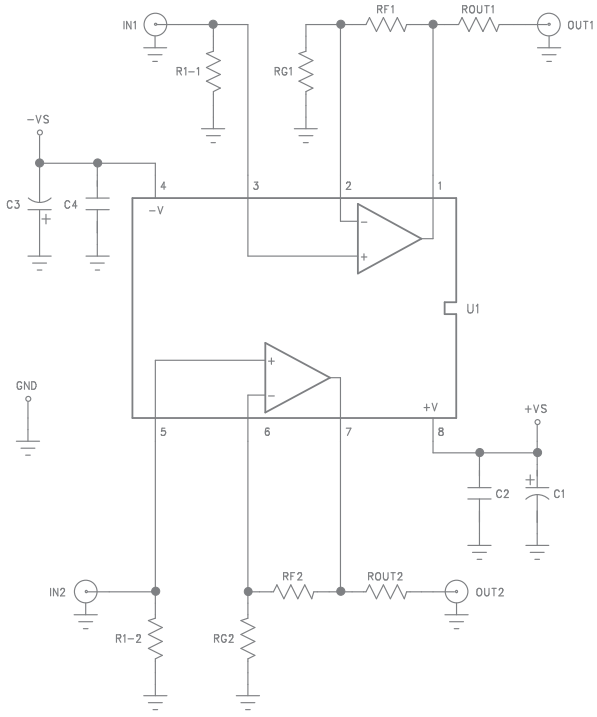


Figure 11. CEB006 Schematic

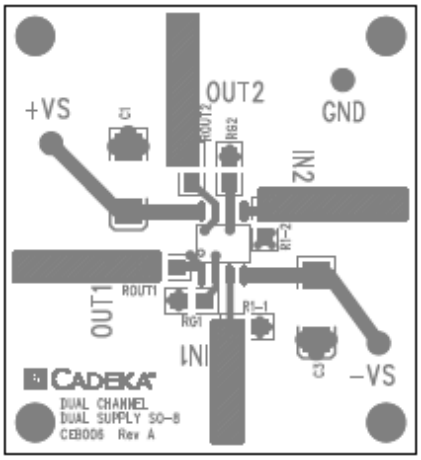


Figure 12. CEB006 Top View

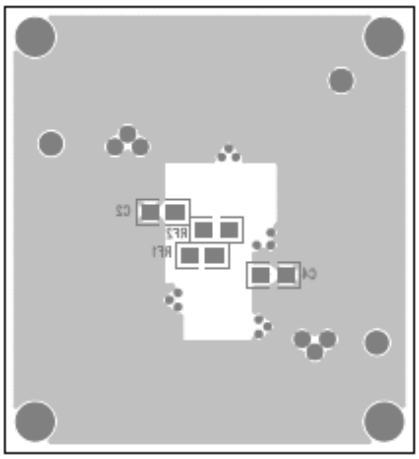
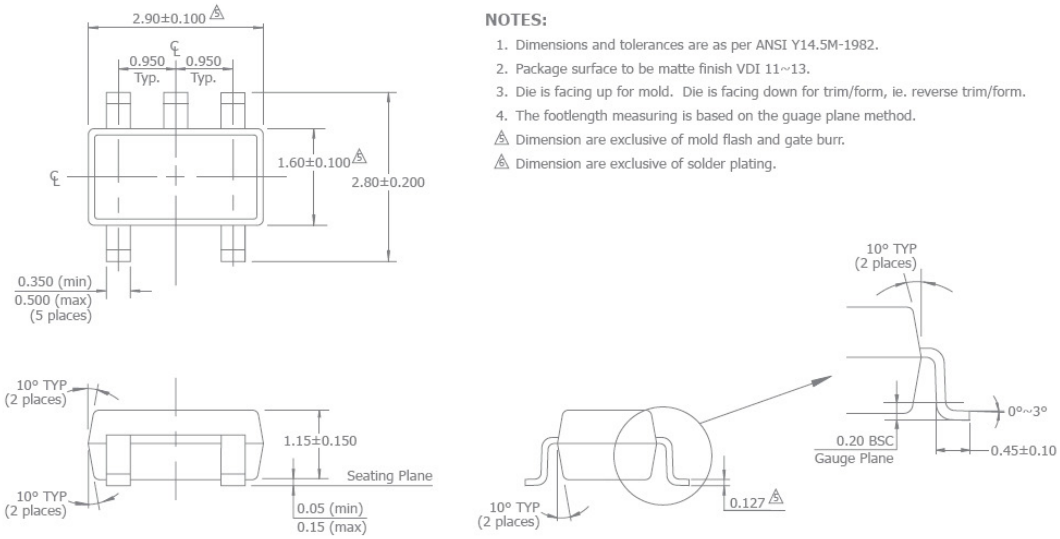


Figure 13. CEB006 Bottom View

Mechanical Dimensions

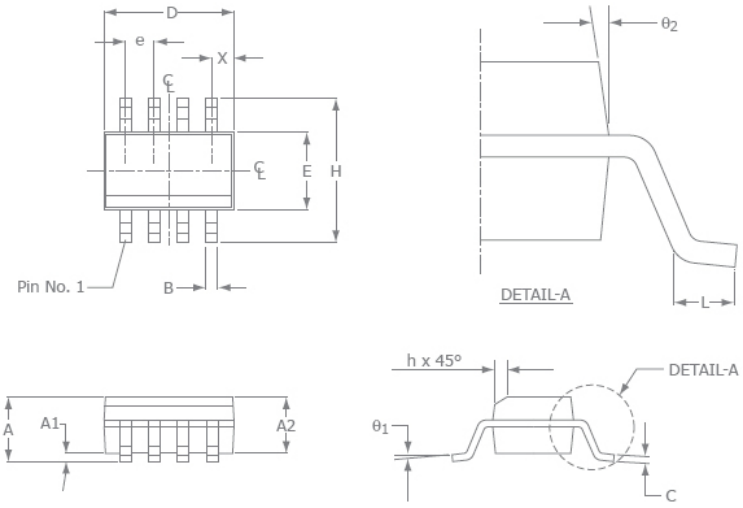
SOT23-5 Package



NOTES:

1. Dimensions and tolerances are as per ANSI Y14.5M-1982.
2. Package surface to be matte finish VDI 11~13.
3. Die is facing up for mold. Die is facing down for trim/form, ie. reverse trim/form.
4. The footlength measuring is based on the guage plane method.
5. Dimension are exclusive of mold flash and gate burr.
6. Dimension are exclusive of solder plating.

SOIC-8



SOIC-8		
SYMBOL	MIN	MAX
A1	0.10	0.25
B	0.36	0.48
C	0.19	0.25
D	4.80	4.98
E	3.81	3.99
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.5
L	0.41	1.27
A	1.37	1.73
θ_1	0°	8°
X	0.55 ref	
θ_2	7° BSC	

NOTE:

1. All dimensions are in millimeters.
2. Lead coplanarity should be 0 to 0.1mm (0.004") max.
3. Package surface finishing: VDI 24~27
4. All dimension excluding mold flashes.
5. The lead width, B to be determined at 0.1905mm from the lead tip.

For Further Assistance:

Exar Corporation Headquarters and Sales Offices
48720 Kato Road
Fremont, CA 94538 - USA

Tel.: +1 (510) 668-7000
Fax: +1 (510) 668-7001
www.exar.com

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