



**THE DATASHEET OF
ADUM1311BRWZ-RL**



FEATURES

Low power operation

5 V operation

- 1.7 mA per channel maximum at 0 Mbps to 2 Mbps
- 4.0 mA per channel maximum at 2 Mbps to 10 Mbps

3 V operation

- 1.0 mA per channel maximum at 0 Mbps to 2 Mbps
- 2.1 mA per channel maximum at 2 Mbps to 10 Mbps

Bidirectional communication

3 V/5 V level translation

Schmitt trigger inputs

High temperature operation: 105°C

Up to 10 Mbps data rate (NRZ)

Programmable default output state

High common-mode transient immunity: >25 kV/μs

16-lead, RoHS-compliant, SOIC wide body package

8.1 mm external creepage

Safety and regulatory approvals

UL recognition: 3750 V rms for 1 minute per UL 1577

CSA Component Acceptance Notice 5A

VDE certificate of conformity

DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12

$V_{IORM} = 560$ V peak working voltage

APPLICATIONS

General-purpose multichannel isolation

SPI interface/data converter isolation

RS-232/RS-422/RS-485 transceiver

Industrial field bus isolation

GENERAL DESCRIPTION

The ADuM1310/ADuM1311¹ are 3-channel digital isolators based on Analog Devices, Inc., *iCoupler*® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *iCoupler* devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, maximum operating temperature, and lifetime effects are eliminated with the simple *iCoupler* digital interfaces and stable performance characteristics. The need for external drivers and other discrete components is eliminated with these *iCoupler* products. Furthermore, *iCoupler* devices consume one-tenth to one-sixth the power of optocouplers at

¹ Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; and 7,075,329. Other patents pending.

Rev. K

Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

FUNCTIONAL BLOCK DIAGRAMS

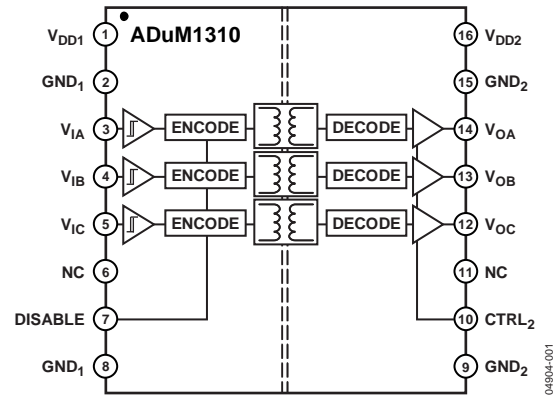


Figure 1. ADuM1310

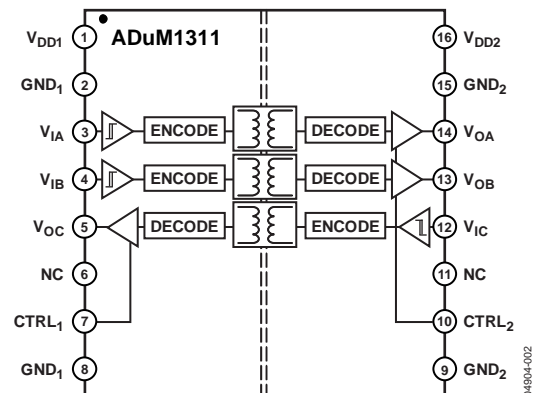


Figure 2. ADuM1311

comparable signal data rates. The *iCoupler* also offers higher channel densities and more options for channel directionality.

The ADuM1310/ADuM1311 isolators provide three independent isolation channels in a variety of channel configurations and data rates up to 10 Mbps (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling voltage translation functionality across the isolation barrier. All products allow the user to predetermine the default output state in the absence of input V_{DD1} power with a simple control pin. Unlike other optocoupler alternatives, the ADuM1310/ADuM1311 isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/ power-down conditions.

TABLE OF CONTENTS

| | | | |
|---|----|--|----|
| Features | 1 | Recommended Operating Conditions | 11 |
| Applications..... | 1 | Absolute Maximum Ratings | 12 |
| Functional Block Diagrams..... | 1 | ESD Caution..... | 12 |
| General Description | 1 | Pin Configurations and Function Descriptions | 13 |
| Revision History | 2 | Typical Performance Characteristics | 16 |
| Specifications..... | 3 | Applications Information | 18 |
| Electrical Characteristics—5 V Operation..... | 3 | PC Board Layout | 18 |
| Electrical Characteristics—3 V Operation..... | 5 | Propagation Delay-Related Parameters..... | 18 |
| Electrical Characteristics—Mixed 5 V/3 V or 3 V/5 V Operation..... | 7 | DC Correctness and Magnetic Field Immunity..... | 18 |
| Package Characteristics | 10 | Power Consumption | 19 |
| Regulatory Information..... | 10 | Insulation Lifetime | 20 |
| Insulation and Safety-Related Specifications..... | 10 | Outline Dimensions | 21 |
| DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 | | Ordering Guide | 21 |
| Insulation Characteristics..... | 11 | | |

REVISION HISTORY

6/15—Rev. J to Rev. K

| | |
|-------------------------------------|----|
| Changes to Table 5 and Table 6..... | 10 |
|-------------------------------------|----|

9/14—Rev. I to Rev. J

| | |
|-------------------------------------|----|
| Changes to Features Section..... | 1 |
| Changes to Table 5 and Table 6..... | 10 |

4/14—Rev. H to Rev. I

| | |
|-------------------------|----|
| Change to Table 5 | 10 |
|-------------------------|----|

3/12—Rev. G to Rev. H

| | |
|---|----|
| Created Hyperlink for Safety and Regulatory Approvals Entry in Features Section..... | 1 |
| Change to PC Board Layout Section..... | 18 |
| Updated Outline Dimensions | 21 |

6/07—Rev. F to Rev. G

| | |
|---|----|
| Updated VDE Certification Throughout | 1 |
| Changes to Features and Applications..... | 1 |
| Changes to DC Specifications in Table 1..... | 3 |
| Changes to DC Specifications in Table 2..... | 5 |
| Changes to DC Specifications in Table 3..... | 7 |
| Changes to Regulatory Information Section | 10 |
| Added Table 10 | 12 |
| Added Insulation Lifetime Section | 19 |

1/07—Rev. E to Rev. F

| | |
|--|-----------|
| Added ADuM1311 | Universal |
| Changes to Typical Performance Characteristics Section | 16 |
| Changes to Ordering Guide | 20 |

10/06—Rev. D to Rev. E

| | |
|--|-----------|
| Removed ADuM1410 | Universal |
| Updated Format..... | Universal |
| Change to Figure 3 | 10 |
| Changes to Table 10 | 10 |
| Changes to Application Information Section | 12 |
| Updated Outline Dimensions..... | 18 |
| Changes to Ordering Guide | 18 |

3/06—Rev. C to Rev. D

| | |
|--|----|
| Added Note 1; Changes to Figure 2 | 1 |
| Changes to Absolute Maximum Ratings..... | 11 |

11/05—Revision C: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION

$4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 5\text{ V}$. All voltages are relative to their respective grounds.

Table 1.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|--|------------|------------|----------------------|--|
| DC SPECIFICATIONS | | | | | | |
| ADuM1310, Total Supply Current, Three Channels ¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | 2.4 | 3.2 | mA | DC to 1 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | 1.2 | 1.6 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | 6.6 | 9.0 | mA | 5 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | 2.1 | 3.0 | mA | 5 MHz logic signal frequency |
| ADuM1311, Total Supply Current, Three Channels ¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | 2.2 | 2.8 | mA | DC to 1 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | 1.8 | 2.4 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | 4.5 | 5.7 | mA | 5 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | 3.5 | 4.3 | mA | 5 MHz logic signal frequency |
| For All Models | | | | | | |
| Input Currents | $I_{IA}, I_{IB}, I_{IC}, I_{CTRL1}, I_{CTRL2}, I_{DISABLE}$ | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{IA}, V_{IB}, V_{IC} \leq V_{DD1}$ or V_{DD2} , $0\text{ V} \leq V_{CTRL1}, V_{CTRL2} \leq V_{DD1}$ or V_{DD2} , $0\text{ V} \leq V_{DISABLE} \leq V_{DD1}$ |
| Logic High Input Threshold | V_{IH} | 2.0 | | | V | |
| Logic Low Input Threshold | V_{IL} | | | 0.8 | V | |
| Logic High Output Voltages | $V_{OAH}, V_{OBH}, V_{OCH}$ | $(V_{DD1}$ or $V_{DD2}) - 0.1$ $(V_{DD1}$ or $V_{DD2}) - 0.4$ | 5.0 4.8 | | V | $I_{Ox} = -20\ \mu\text{A}, V_{Ix} = V_{IxH}$ $I_{Ox} = -4\ \text{mA}, V_{Ix} = V_{IxH}$ |
| Logic Low Output Voltages | $V_{OAL}, V_{OBL}, V_{OCL}$ | | 0.0 0.2 | 0.1 0.4 | V | $I_{Ox} = 20\ \mu\text{A}, V_{Ix} = V_{IxL}$ $I_{Ox} = 4\ \text{mA}, V_{Ix} = V_{IxL}$ |
| SWITCHING SPECIFICATIONS | | | | | | |
| ADuM131xARWZ | | | | | | |
| Minimum Pulse Width ² | PW | | | 1000 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | 1 | | | Mbps | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 20 | | 100 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴ | PWD | | | 40 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 50 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Channel-to-Channel Matching ⁶ | $t_{PSKCD/OD}$ | | | 50 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| ADuM131xBRWZ | | | | | | |
| Minimum Pulse Width ² | PW | | | 100 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | 10 | | | Mbps | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 20 | 30 | 50 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} $ ⁴ | PWD | | | 5 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/ $^\circ\text{C}$ | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 30 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---------------|-----|------|------|-------------|--|
| Channel-to-Channel Matching, Codirectional Channels ⁶ | t_{PSKCD} | | | 5 | ns | $C_L = 15$ pF, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels ⁶ | t_{PSKOD} | | | 6 | ns | $C_L = 15$ pF, CMOS signal levels |
| For All Models | | | | | | |
| Output Rise/Fall Time (10% to 90%) | t_R/t_F | | 2.5 | | ns | $C_L = 15$ pF, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output ⁷ | $ CM_H $ | 25 | 35 | | kV/ μ s | $V_{IX} = V_{DD1}$ or V_{DD2} , $V_{CM} = 1000$ V, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output ⁷ | $ CM_L $ | 25 | 35 | | kV/ μ s | $V_{IX} = 0$ V, $V_{CM} = 1000$ V, transient magnitude = 800 V |
| Refresh Rate | f_r | | 1.2 | | Mbps | |
| Input Enable Time ⁸ | t_{ENABLE} | | | 2.0 | μ s | $V_{IA}, V_{IB}, V_{IC} = 0$ V or V_{DD1} |
| Input Disable Time ⁸ | $t_{DISABLE}$ | | | 5.0 | μ s | $V_{IA}, V_{IB}, V_{IC} = 0$ V or V_{DD1} |
| Input Supply Current per Channel, Quiescent ⁹ | $I_{DDI(Q)}$ | | 0.50 | 0.73 | mA | |
| Output Supply Current per Channel, Quiescent ⁹ | $I_{DDO(Q)}$ | | 0.38 | 0.53 | mA | |
| Input Dynamic Supply Current per Channel ¹⁰ | $I_{DDI(D)}$ | | 0.12 | | mA/ Mbps | |
| Output Dynamic Supply Current per Channel ¹⁰ | $I_{DDO(D)}$ | | 0.04 | | mA/ Mbps | |

¹ The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1310/ADuM1311 channel configurations.

² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁸ Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration, as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the CTRL₂ logic state (see Table 13).

⁹ $I_{DDX(Q)}$ is the quiescent current drawn from the corresponding supply by a single channel. To calculate the total quiescent current, an additional inaccessible channel in the same orientation as Channel A must be included to account for the total current consumed.

¹⁰ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—3 V OPERATION

$2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = V_{DD2} = 3.0\text{ V}$. All voltages are relative to their respective ground.

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|--------------------------------|-------|------|----------------------|--|
| DC SPECIFICATIONS | | | | | | |
| ADuM1310, Total Supply Current, Three Channels¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | 1.2 | 1.6 | mA | DC to 1 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | 0.8 | 1.0 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | 3.4 | 4.9 | mA | 5 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | 1.1 | 1.3 | mA | 5 MHz logic signal frequency |
| ADuM1311, Total Supply Current, Three Channels¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | 1.0 | 1.6 | mA | DC to 1 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | 0.9 | 1.4 | | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | 2.5 | 3.5 | mA | 5 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | 1.9 | 2.6 | | 5 MHz logic signal frequency |
| For All Models | | | | | | |
| Input Currents | $I_{IA}, I_{IB}, I_{IC}, I_{CTRL1}, I_{CTRL2}, I_{DISABLE}$ | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{IA}, V_{IB}, V_{IC} \leq V_{DD1}$ or V_{DD2} , $0\text{ V} \leq V_{CTRL1}, V_{CTRL2} \leq V_{DD1}$ or V_{DD2} , $0\text{ V} \leq V_{DISABLE} \leq V_{DD1}$ |
| Logic High Input Threshold | V_{IH} | 1.6 | | | V | |
| Logic Low Input Threshold | V_{IL} | | | 0.4 | V | |
| Logic High Output Voltages | $V_{OAH}, V_{OBH}, V_{OCH}$ | $(V_{DD1}$ or $V_{DD2}) - 0.1$ | 3.0 | | V | $I_{Ox} = -20\ \mu\text{A}, V_{Ix} = V_{IxH}$ |
| | | $(V_{DD1}$ or $V_{DD2}) - 0.4$ | 2.8 | | V | $I_{Ox} = -4\ \text{mA}, V_{Ix} = V_{IxH}$ |
| Logic Low Output Voltages | $V_{OAL}, V_{OBL}, V_{OCL}$ | | 0.0 | 0.1 | V | $I_{Ox} = 20\ \mu\text{A}, V_{Ix} = V_{IxL}$ |
| | | | 0.2 | 0.4 | V | $I_{Ox} = 4\ \text{mA}, V_{Ix} = V_{IxL}$ |
| SWITCHING SPECIFICATIONS | | | | | | |
| ADuM131xARWZ | | | | | | |
| Minimum Pulse Width ² | PW | | | 1000 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | 1 | | | Mbps | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 20 | | 100 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^4$ | PWD | | | 40 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 50 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Channel-to-Channel Matching ⁶ | $t_{PSKCD/OD}$ | | | 50 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| ADuM131xBRWZ | | | | | | |
| Minimum Pulse Width ² | PW | | | 100 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | 10 | | | Mbps | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 20 | 30 | 50 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^4$ | PWD | | | 5 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/ $^\circ\text{C}$ | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 30 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels ⁶ | t_{PSKCD} | | | 5 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels ⁶ | t_{PSKOD} | | | 6 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|---------------|-----|------|------|-------------------|---|
| For All Models | | | | | | |
| Output Rise/Fall Time (10% to 90%) | t_R/t_F | | 2.5 | | ns | $C_L = 15 \text{ pF}$, CMOS signal levels |
| Common-Mode Transient Immunity at Logic High Output ⁷ | $ CM_H $ | 25 | 35 | | kV/ μs | $V_{IX} = V_{DD1}$ or V_{DD2} , $V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output ⁷ | $ CM_L $ | 25 | 35 | | kV/ μs | $V_{IX} = 0 \text{ V}$, $V_{CM} = 1000 \text{ V}$, transient magnitude = 800 V |
| Refresh Rate | f_r | | 1.1 | | Mbps | |
| Input Enable Time ⁸ | t_{ENABLE} | | 2.0 | | μs | $V_{IA}, V_{IB}, V_{IC} = 0 \text{ V}$ or V_{DD1} |
| Input Disable Time ⁸ | $t_{DISABLE}$ | | 5.0 | | μs | $V_{IA}, V_{IB}, V_{IC} = 0 \text{ V}$ or V_{DD1} |
| Input Supply Current per Channel, Quiescent ⁹ | $I_{DDI(Q)}$ | | 0.25 | 0.38 | mA | |
| Output Supply Current per Channel, Quiescent ⁹ | $I_{DDO(Q)}$ | | 0.19 | 0.33 | mA | |
| Input Dynamic Supply Current per Channel ¹⁰ | $I_{DDI(D)}$ | | 0.07 | | mA/ Mbps | |
| Output Dynamic Supply Current per Channel ¹⁰ | $I_{DDO(D)}$ | | 0.02 | | mA/ Mbps | |

¹ The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1310/ADuM1311 channel configurations.

² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{IX} signal to the 50% level of the falling edge of the V_{OX} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{IX} signal to the 50% level of the rising edge of the V_{OX} signal.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8 \text{ V}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁸ Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration, as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the CTRL₂ logic state (see Table 13).

⁹ $I_{DDX(Q)}$ is the quiescent current drawn from the corresponding supply by a single channel. To calculate the total quiescent current, an additional inaccessible channel in the same orientation as Channel A must be included to account for the total current consumed.

¹⁰ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION

5 V/3 V operation: $4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$; 3 V/5 V operation: $2.7\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$, $4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$; all minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at $T_A = 25^\circ\text{C}$; $V_{DD1} = 3.0\text{ V}$, $V_{DD2} = 5\text{ V}$ or $V_{DD1} = 5\text{ V}$, $V_{DD2} = 3.0\text{ V}$. All voltages are relative to their respective ground.

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|---|-----|-------|-----|---------------|--|
| DC SPECIFICATIONS | | | | | | |
| ADuM1310, Total Supply Current, Three Channels¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | | | | |
| 5 V/3 V Operation | | | 2.4 | 3.2 | mA | DC to 1 MHz logic signal frequency |
| 3 V/5 V Operation | | | 1.2 | 1.6 | mA | DC to 1 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | | | | |
| 5 V/3 V Operation | | | 0.8 | 1.0 | mA | DC to 1 MHz logic signal frequency |
| 3 V/5 V Operation | | | 1.2 | 1.6 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | | | | |
| 5 V/3 V Operation | | | 6.5 | 8.2 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 3.4 | 4.9 | mA | 5 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | | | | |
| 5 V/3 V Operation | | | 1.1 | 1.3 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 1.9 | 2.2 | mA | 5 MHz logic signal frequency |
| ADuM1311, Total Supply Current, Three Channels¹ | | | | | | |
| DC to 2 Mbps | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(Q)}$ | | | | | |
| 5 V/3 V Operation | | | 2.2 | 2.8 | mA | DC to 1 MHz logic signal frequency |
| 3 V/5 V Operation | | | 1.0 | 1.6 | mA | DC to 1 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(Q)}$ | | | | | |
| 5 V/3 V Operation | | | 0.9 | 1.4 | mA | DC to 1 MHz logic signal frequency |
| 3 V/5 V Operation | | | 1.8 | 2.4 | mA | DC to 1 MHz logic signal frequency |
| 10 Mbps (BRWZ Grade Only) | | | | | | |
| V_{DD1} Supply Current | $I_{DD1(10)}$ | | | | | |
| 5 V/3 V Operation | | | 4.5 | 5.7 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 2.5 | 3.5 | mA | 5 MHz logic signal frequency |
| V_{DD2} Supply Current | $I_{DD2(10)}$ | | | | | |
| 5 V/3 V Operation | | | 1.9 | 2.6 | mA | 5 MHz logic signal frequency |
| 3 V/5 V Operation | | | 3.5 | 4.3 | mA | 5 MHz logic signal frequency |
| For All Models | | | | | | |
| Input Currents | $I_{IA}, I_{IB}, I_{IC}, I_{CTRL1}, I_{CTRL2}, I_{DISABLE}$ | -10 | +0.01 | +10 | μA | $0\text{ V} \leq V_{IA}, V_{IB}, V_{IC} \leq V_{DD1}$ or V_{DD2} , $0\text{ V} \leq V_{CTRL1}, V_{CTRL2} \leq V_{DD1}$ or V_{DD2} , $0\text{ V} \leq V_{DISABLE} \leq V_{DD1}$ |
| Logic High Input Threshold | V_{IH} | | | | | |
| $V_{DDX} = 5\text{ V}$ Operation | | 2.0 | | | V | |
| $V_{DDX} = 3\text{ V}$ Operation | | 1.6 | | | V | |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----------------------------|-------------------------------------|-------------------------------------|------|-------------------|---|
| Logic Low Input Threshold | V_{IL} | | | 0.8 | V | |
| $V_{DDX} = 5\text{ V}$ Operation | | | | 0.4 | V | |
| $V_{DDX} = 3\text{ V}$ Operation | | | | | | |
| Logic High Output Voltages | $V_{OAH}, V_{OBH}, V_{OCH}$ | $(V_{DD1}\text{ or }V_{DD2}) - 0.1$ | $(V_{DD1}\text{ or }V_{DD2})$ | | V | $I_{OX} = -20\ \mu\text{A}, V_{IX} = V_{IXH}$ |
| | | $(V_{DD1}\text{ or }V_{DD2}) - 0.4$ | $(V_{DD1}\text{ or }V_{DD2}) - 0.2$ | | V | $I_{OX} = -4\ \text{mA}, V_{IX} = V_{IXH}$ |
| Logic Low Output Voltages | $V_{OAL}, V_{OBL}, V_{OCL}$ | | 0.0 | 0.1 | V | $I_{OX} = 20\ \mu\text{A}, V_{IX} = V_{IXL}$ |
| | | | 0.2 | 0.4 | V | $I_{OX} = 4\ \text{mA}, V_{IX} = V_{IXL}$ |
| SWITCHING SPECIFICATIONS | | | | | | |
| ADuM131xARWZ | | | | | | |
| Minimum Pulse Width ² | PW | | | 1000 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | 1 | | | Mbps | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 25 | | 100 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Pulse Width Distortion $ t_{PLH} - t_{PHL} ^4$ | PWD | | | 40 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 50 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Channel-to-Channel Matching ⁶ | $t_{PSKCD/OD}$ | | | 50 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| ADuM131xBRWZ | | | | | | |
| Minimum Pulse Width ² | PW | | | 100 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Maximum Data Rate ³ | | 10 | | | Mbps | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay ⁴ | t_{PHL}, t_{PLH} | 20 | | 60 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Pulse Width Distortion, $ t_{PLH} - t_{PHL} ^4$ | PWD | | | 5 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Change vs. Temperature | | | 5 | | ps/°C | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Propagation Delay Skew ⁵ | t_{PSK} | | | 30 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Channel-to-Channel Matching, Codirectional Channels ⁶ | t_{PSKCD} | | | 5 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| Channel-to-Channel Matching, Opposing-Directional Channels ⁶ | t_{PSKOD} | | | 6 | ns | $C_L = 15\ \text{pF}$, CMOS signal levels |
| For All Models | | | | | | |
| Output Rise/Fall Time (10% to 90%) | t_R/t_F | | | | | $C_L = 15\ \text{pF}$, CMOS signal levels |
| $5\text{ V}/3\text{ V}$ Operation | | | 2.5 | | ns | |
| $3\text{ V}/5\text{ V}$ Operation | | | 2.5 | | ns | |
| Common-Mode Transient Immunity at Logic High Output ⁷ | $ CM_H $ | 25 | 35 | | kV/ μs | $V_{IX} = V_{DD1}\text{ or }V_{DD2}, V_{CM} = 1000\ \text{V}$, transient magnitude = 800 V |
| Common-Mode Transient Immunity at Logic Low Output ⁷ | $ CM_L $ | 25 | 35 | | kV/ μs | $V_{IX} = 0\ \text{V}, V_{CM} = 1000\ \text{V}$, transient magnitude = 800 V |
| Refresh Rate | f_r | | | | | |
| $5\text{ V}/3\text{ V}$ Operation | | | 1.2 | | Mbps | |
| $3\text{ V}/5\text{ V}$ Operation | | | 1.1 | | Mbps | |
| Input Enable Time ⁸ | t_{ENABLE} | | | 2.0 | μs | $V_{IA}, V_{IB}, V_{IC}, V_{ID} = 0\ \text{V}$ or V_{DD1} |
| Input Disable Time ⁸ | $t_{DISABLE}$ | | | 5.0 | μs | $V_{IA}, V_{IB}, V_{IC}, V_{ID} = 0\ \text{V}$ or V_{DD1} |
| Input Supply Current per Channel, Quiescent ⁹ | | | | | | |
| $V_{DDX} = 5\text{ V}$ Operation | $I_{DDI(Q)}$ | | 0.50 | 0.73 | mA | |
| $V_{DDX} = 3\text{ V}$ Operation | $I_{DDI(Q)}$ | | 0.25 | 0.38 | mA | |
| Output Supply Current per Channel, Quiescent ⁹ | | | | | | |
| $V_{DDX} = 5\text{ V}$ Operation | $I_{DDO(Q)}$ | | 0.38 | 0.53 | mA | |
| $V_{DDX} = 3\text{ V}$ Operation | $I_{DDO(Q)}$ | | 0.19 | 0.33 | mA | |
| Input Dynamic Supply Current per Channel ¹⁰ | $I_{DDI(D)}$ | | | | | |
| $V_{DDX} = 5\text{ V}$ Operation | | | 0.12 | | mA/ Mbps | |
| $V_{DDX} = 3\text{ V}$ Operation | | | 0.07 | | mA/ Mbps | |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|--------------|-----|------|-----|-------------|--------------------------|
| Output Dynamic Supply Current per Channel ¹⁰ | $I_{DDI(D)}$ | | | | | |
| $V_{DDX} = 5\text{ V Operation}$ | | | 0.04 | | mA/ Mbps | |
| $V_{DDX} = 3\text{ V Operation}$ | | | 0.02 | | mA/ Mbps | |

¹ The supply current values for all four channels are combined when running at identical data rates. Output supply current values are specified with no output load present. The supply current associated with an individual channel operating at a given data rate can be calculated as described in the Power Consumption section. See Figure 6 through Figure 8 for information on per-channel supply current as a function of data rate for unloaded and loaded conditions. See Figure 9 through Figure 12 for total V_{DD1} and V_{DD2} supply currents as a function of data rate for ADuM1310/ADuM1311 channel configurations.

² The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed.

³ The maximum data rate is the fastest data rate at which the specified pulse width distortion is guaranteed.

⁴ t_{PHL} propagation delay is measured from the 50% level of the falling edge of the V_{ix} signal to the 50% level of the falling edge of the V_{ox} signal. t_{PLH} propagation delay is measured from the 50% level of the rising edge of the V_{ix} signal to the 50% level of the rising edge of the V_{ox} signal.

⁵ t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

⁶ Codirectional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier. Opposing-directional channel-to-channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposing sides of the isolation barrier.

⁷ CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8 V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8\text{ V}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges. The transient magnitude is the range over which the common mode is slewed.

⁸ Input enable time is the duration from when $V_{DISABLE}$ is set low until the output states are guaranteed to match the input states in the absence of any input data logic transitions. If an input data logic transition within a given channel does occur within this time interval, the output of that channel reaches the correct state within the much shorter duration, as determined by the propagation delay specifications within this data sheet. Input disable time is the duration from when $V_{DISABLE}$ is set high until the output states are guaranteed to reach their programmed output levels, as determined by the CTRL₂ logic state (see Table 13).

⁹ $I_{DDX(Q)}$ is the quiescent current drawn from the corresponding supply by a single channel. To calculate the total quiescent current, an additional inaccessible channel in the same orientation as Channel A must be included to account for the total current consumed.

¹⁰ Dynamic supply current is the incremental amount of supply current required for a 1 Mbps increase in signal data rate. See Figure 6 through Figure 8 for information on per-channel supply current for unloaded and loaded conditions. See the Power Consumption section for guidance on calculating the per-channel supply current for a given data rate.

PACKAGE CHARACTERISTICS

Table 4.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------------------|-----|------------------|-----|------|---|
| Resistance (Input-to-Output) ¹ | R _{I-O} | | 10 ¹² | | Ω | |
| Capacitance (Input-to-Output) ¹ | C _{I-O} | | 2.2 | | pF | f = 1 MHz |
| Input Capacitance ² | C _i | | 4.0 | | pF | |
| IC Junction-to-Case Thermal Resistance | | | | | | |
| Side 1 | θ _{JCI} | | 33 | | °C/W | Thermocouple located at center of package underside |
| Side 2 | θ _{JCO} | | 28 | | °C/W | |

¹ The device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

² Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM1310/ADuM1311 have been approved by the organizations listed in Table 5. See Table 10 and the Insulation Lifetime section for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 5.

| UL | CSA | CQC | VDE |
|--|--|---|--|
| Recognized Under 1577 Component Recognition Program ¹ | Approved under CSA Component Acceptance Notice 5A | Approved under CQC11-471543-2012 | Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 ² |
| Single Protection, 3750 V rms Isolation Voltage | Basic insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage | Basic insulation per GB4943.1-2011 Basic insulation, 415 V rms (588 V peak) maximum working voltage, tropical climate, altitude ≤ 5000 m | Reinforced insulation, 560 V peak |
| File E214100 | File 205078 | File: CQC14001114897 | File 2471900-4880-0001 |

¹ In accordance with UL 1577, each ADuM1310/ADuM1311 is proof-tested by applying an insulation test voltage ≥4500 V rms for 1 sec (current leakage detection limit = 8.1 μA).

² In accordance with DIN V VDE V 0884-10, each ADuM1310/ADuM1311 is proof-tested by applying an insulation test voltage ≥1050 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marked on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 6.

| Parameter | Symbol | Value | Unit | Test Conditions/Comments |
|--|--------|-----------|-------|--|
| Rated Dielectric Insulation Voltage | | 3750 | V rms | 1-minute duration |
| Minimum External Air Gap (Clearance) | L(I01) | 7.7 min | mm | Measured from input terminals to output terminals, shortest distance through air |
| Minimum External Tracking (Creepage) | L(I02) | 8.1 min | mm | Measured from input terminals to output terminals, shortest distance path along body |
| Minimum Internal Gap (Internal Clearance) | | 0.017 min | mm | Insulation distance through insulation |
| Tracking Resistance (Comparative Tracking Index) | CTI | >400 | V | DIN IEC 112/VDE 0303 Part 1 |
| Isolation Group | | II | | Material Group (DIN VDE 0110, 1/89, Table 1) |

DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 INSULATION CHARACTERISTICS

The ADuM1310/ADuM1311 isolators are suitable for reinforced electrical isolation within the safety limit data only. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marked on packages denotes DIN V VDE V 0884-10 approval for 560 V peak working voltage.

Table 7.

| Description | Test Conditions/Comments | Symbol | Characteristic | Unit |
|---|--|------------|--------------------------------|--------|
| Installation Classification per DIN VDE 0110 For Rated Mains Voltage ≤ 150 V rms For Rated Mains Voltage ≤ 300 V rms For Rated Mains Voltage ≤ 400 V rms | | | I to IV I to III I to II | |
| Climatic Classification | | | 40/105/21 | |
| Pollution Degree per DIN VDE 0110, Table 1 | | | 2 | |
| Maximum Working Insulation Voltage | | V_{IORM} | 560 | V peak |
| Input-to-Output Test Voltage, Method B1 | $V_{IORM} \times 1.875 = V_{PR}$, 100% production test, $t_m = 1$ sec, partial discharge < 5 pC | V_{PR} | 1050 | V peak |
| Input-to-Output Test Voltage, Method A | $V_{IORM} \times 1.6 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC | V_{PR} | 896 | V peak |
| After Environmental Tests Subgroup 1 | | | 672 | V peak |
| After Input and/or Safety Test Subgroup 2 and Subgroup 3 | $V_{IORM} \times 1.2 = V_{PR}$, $t_m = 60$ sec, partial discharge < 5 pC | | | |
| Highest Allowable Overvoltage | Transient overvoltage, $t_{TR} = 10$ sec | V_{TR} | 4000 | V peak |
| Safety-Limiting Values | Maximum value allowed in the event of a failure; see Figure 3 | | | |
| Case Temperature | | T_S | 150 | °C |
| Side 1 Current | | I_{S1} | 265 | mA |
| Side 2 Current | | I_{S2} | 335 | mA |
| Insulation Resistance at T_S | $V_{IO} = 500$ V | R_S | >10 ⁹ | Ω |

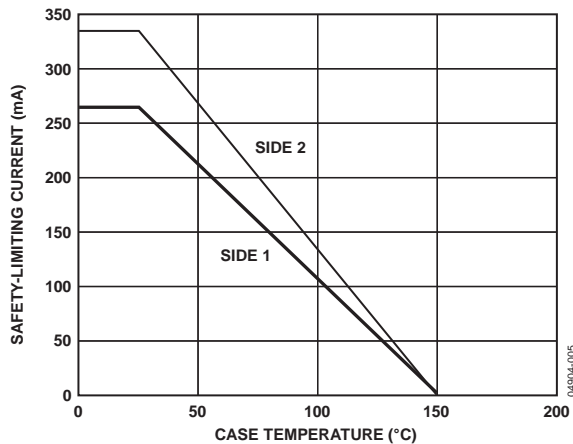


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 8.

| Parameter | Symbol | Min | Max | Unit |
|----------------------------------|--------------------|-----|------|------|
| Operating Temperature | T_A | -40 | +105 | °C |
| Supply Voltages ¹ | V_{DD1}, V_{DD2} | 2.7 | 5.5 | V |
| Input Signal Rise and Fall Times | | | 1.0 | ms |

¹ All voltages are relative to their respective ground. See the DC Correctness and Magnetic Field Immunity section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 9.

| Parameter | Rating |
|--|--|
| Storage Temperature (T_{ST}) Range | -65°C to $+150^\circ\text{C}$ |
| Ambient Operating Temperature (T_A) Range | -40°C to $+105^\circ\text{C}$ |
| Supply Voltages (V_{DD1} , V_{DD2}) ¹ | -0.5 V to $+7.0\text{ V}$ |
| Input Voltage (V_{IA} , V_{IB} , V_{IC} , $V_{DISABLE}$, V_{CTRL1} , V_{CTRL2}) ^{1,2} | -0.5 V to $V_{DD1} + 0.5\text{ V}$ |
| Output Voltage (V_{OA} , V_{OB} , V_{OC}) ^{1,2} | -0.5 V to $V_{DDO} + 0.5\text{ V}$ |
| Average Output Current per Pin ³ | |
| Side 1 (I_{O1}) | -18 mA to $+18\text{ mA}$ |
| Side 2 (I_{O2}) | -22 mA to $+22\text{ mA}$ |
| Common-Mode Transients ⁴ | $-100\text{ kV}/\mu\text{s}$ to $+100\text{ kV}/\mu\text{s}$ |

¹ All voltages are relative to their respective ground.

² V_{DD1} and V_{DDO} refer to the supply voltages on the input and output sides of a given channel, respectively. See the PC Board Layout section.

³ See Figure 3 for maximum rated current values for various temperatures.

⁴ Refers to common-mode transients across the insulation barrier.

Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

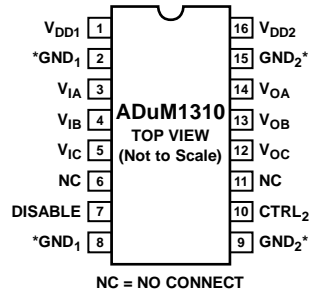
Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 10. Maximum Continuous Working Voltage¹

| Parameter | Max | Unit | Constraint |
|-------------------------------|------|--------|--|
| AC Voltage, Bipolar Waveform | 565 | V peak | 50-year minimum lifetime |
| AC Voltage, Unipolar Waveform | | | |
| Basic Insulation | 1131 | V peak | Maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 560 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |
| DC Voltage | | | |
| Basic Insulation | 1131 | V peak | Maximum approved working voltage per IEC 60950-1 |
| Reinforced Insulation | 560 | V peak | Maximum approved working voltage per IEC 60950-1 and VDE V 0884-10 |

¹ Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NC = NO CONNECT

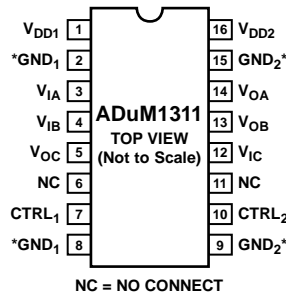
*PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND₁ IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND₂ IS RECOMMENDED.

04904-003

Figure 4. ADuM1310 Pin Configuration

Table 11. ADuM1310 Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-------------------|--|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V. |
| 2 | GND ₁ | Ground 1. Ground reference for Isolator Side 1. |
| 3 | V _{IA} | Logic Input A. |
| 4 | V _{IB} | Logic Input B. |
| 5 | V _{IC} | Logic Input C. |
| 6 | NC | No Connection. |
| 7 | DISABLE | Input Disable. Disables the isolator inputs and halts the dc refresh circuits. Outputs take on the logic state determined by CTRL ₂ . |
| 8 | GND ₁ | Ground 1. Ground reference for Isolator Side 1. |
| 9 | GND ₂ | Ground 2. Ground reference for Isolator Side 2. |
| 10 | CTRL ₂ | Default Output Control. Controls the logic state the outputs take on when the input power is off. V _{OA} , V _{OB} , and V _{OC} outputs are high when CTRL ₂ is high or disconnected and V _{DD1} is off. V _{OA} , V _{OB} , and V _{OC} outputs are low when CTRL ₂ is low and V _{DD1} is off. When V _{DD1} power is on, this pin has no effect. |
| 11 | NC | No Connection. |
| 12 | V _{OC} | Logic Output C. |
| 13 | V _{OB} | Logic Output B. |
| 14 | V _{OA} | Logic Output A. |
| 15 | GND ₂ | Ground 2. Ground reference for Isolator Side 2. |
| 16 | V _{DD2} | Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V. |



NC = NO CONNECT
 *PIN 2 AND PIN 8 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND₁ IS RECOMMENDED. PIN 9 AND PIN 15 ARE INTERNALLY CONNECTED. CONNECTING BOTH TO GND₂ IS RECOMMENDED.

04804-004

Figure 5. ADuM1311 Pin Configuration

Table 12. ADuM1311 Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-------------------|--|
| 1 | V _{DD1} | Supply Voltage for Isolator Side 1, 2.7 V to 5.5 V. |
| 2 | GND ₁ | Ground 1. Ground reference for Isolator Side 1. |
| 3 | V _{IA} | Logic Input A. |
| 4 | V _{IB} | Logic Input B. |
| 5 | V _{OC} | Logic Output C. |
| 6 | NC | No Connection. |
| 7 | CTRL ₁ | Default Output Control. Controls the logic state the outputs take on when the input power is off. V _{OC} output is high when CTRL ₁ is high or disconnected and V _{DD2} is off. V _{OC} output is low when CTRL ₁ is low and V _{DD2} is off. When V _{DD2} power is on, this pin has no effect. |
| 8 | GND ₁ | Ground 1. Ground reference for Isolator Side 1. |
| 9 | GND ₂ | Ground 2. Ground reference for Isolator Side 2. |
| 10 | CTRL ₂ | Default Output Control. Controls the logic state the outputs take on when the input power is off. V _{OA} and V _{OB} outputs are high when CTRL ₂ is high or disconnected and V _{DD1} is off. V _{OA} and V _{OB} outputs are low when CTRL ₂ is low and V _{DD1} is off. When V _{DD1} power is on, this pin has no effect. |
| 11 | NC | No Connection. |
| 12 | V _{IC} | Logic Input C. |
| 13 | V _{OB} | Logic Output B. |
| 14 | V _{OA} | Logic Output A. |
| 15 | GND ₂ | Ground 2. Ground reference for Isolator Side 2. |
| 16 | V _{DD2} | Supply Voltage for Isolator Side 2, 2.7 V to 5.5 V. |

Table 13. Truth Table (Positive Logic)

| V _{Ix} Input ¹ | CTRL _x Input ² | V _{DISABLE} State ³ | V _{DDI} State ⁴ | V _{DDO} State ⁵ | V _{Ox} Output | Description |
|---------------------------------------|---|--|--|--|---------------------------|--|
| H | X | L or NC | Powered | Powered | H | Normal operation, data is high. |
| L | X | L or NC | Powered | Powered | L | Normal operation, data is low. |
| X | H or NC | H | X | Powered | H | Inputs disabled. Outputs are in the default state determined by CTRL _x . |
| X | L | H | X | Powered | L | Inputs disabled. Outputs are in the default state determined by CTRL _x . |
| X | H or NC | X | Unpowered | Powered | H | Input unpowered. Outputs are in the default state determined by CTRL _x . Outputs return to input state within 1 μs of V _{DDI} power restoration. See the pin function descriptions (Table 11 and Table 12) for more details. |
| X | L | X | Unpowered | Powered | L | Input unpowered. Outputs are in the default state determined by CTRL _x . Outputs return to input state within 1 μs of V _{DDI} power restoration. See the pin function descriptions (Table 11 and Table 12) for more details. |
| X | X | X | Powered | Unpowered | Z | Output unpowered. Output pins are in high impedance state. Outputs return to input state within 1 μs of V _{DDO} power restoration. See the pin function descriptions (Table 11 and Table 12) for more details. |

¹ V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, or C).

² CTRL_x refers to the default output control signal on the input side of a given channel (A, B, or C).

³ Available only on the [ADuM1310](#).

⁴ V_{DDI} refers to the power supply on the input side of a given channel (A, B, or C).

⁵ V_{DDO} refers to the power supply on the output side of a given channel (A, B, or C).

TYPICAL PERFORMANCE CHARACTERISTICS

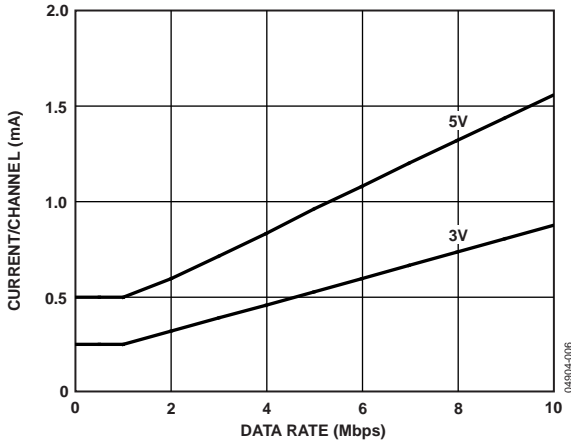


Figure 6. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3 V Operation

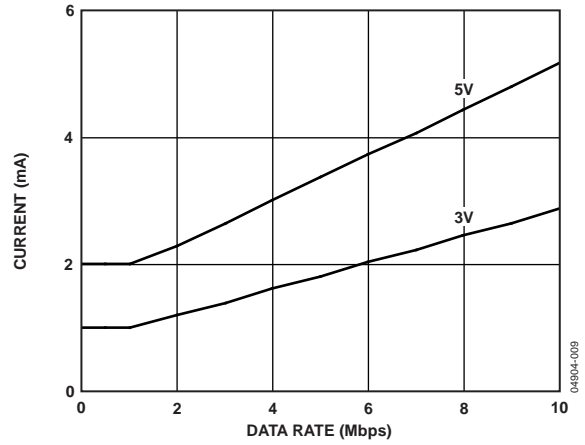


Figure 9. Typical ADuM1310 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation

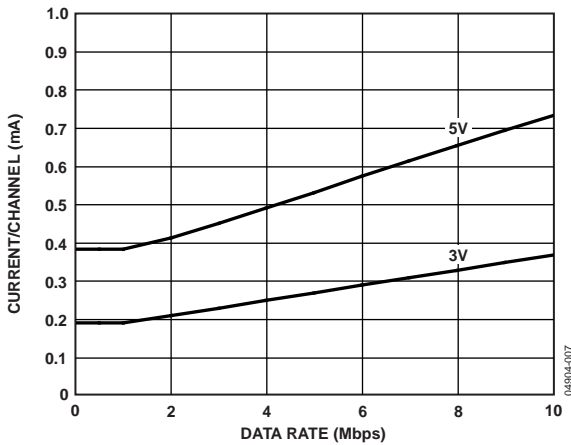


Figure 7. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (No Output Load)

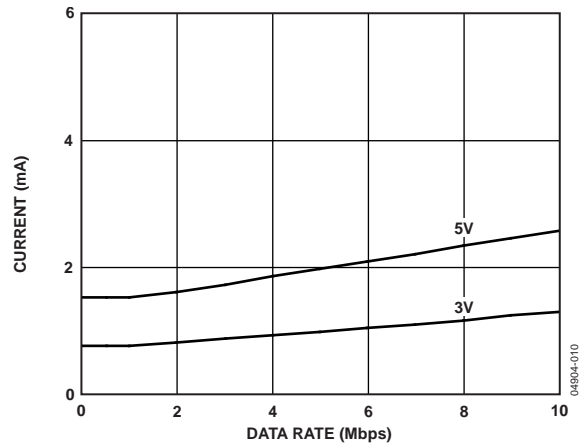


Figure 10. Typical ADuM1310 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation (No Output Load)

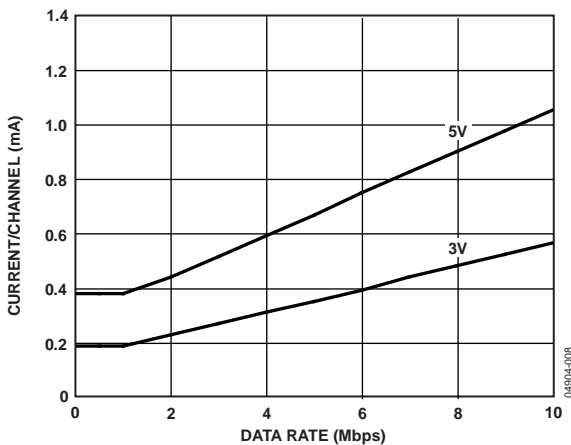


Figure 8. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3 V Operation (15 pF Output Load)

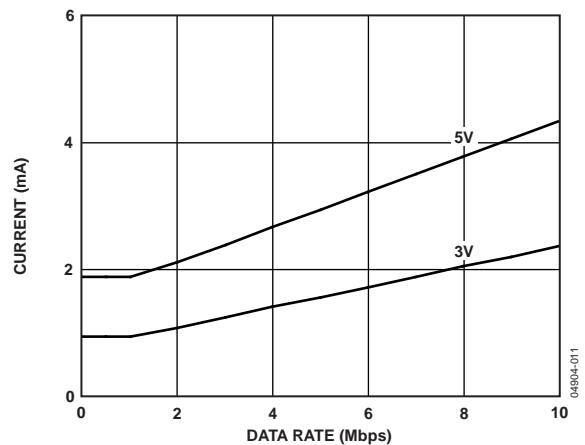


Figure 11. Typical ADuM1311 V_{DD1} Supply Current vs. Data Rate for 5 V and 3 V Operation (No Output Load)

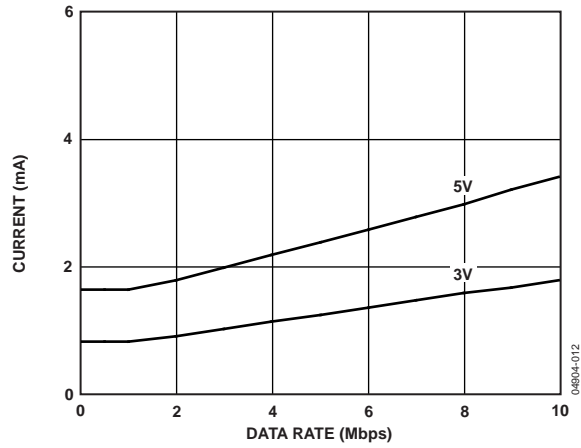


Figure 12. Typical ADuM1311 V_{DD2} Supply Current vs. Data Rate for 5 V and 3 V Operation (No Output Load)

APPLICATIONS INFORMATION

PC BOARD LAYOUT

The ADuM1310/ADuM1311 digital isolator requires no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 13). Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for V_{DD1} and between Pin 15 and Pin 16 for V_{DD2} . The capacitor value should be between 0.01 μF and 0.1 μF . The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm. Bypassing between Pin 1 and Pin 8 and between Pin 9 and Pin 16 should be considered, unless both ground pins on each package are connected together close to the package.

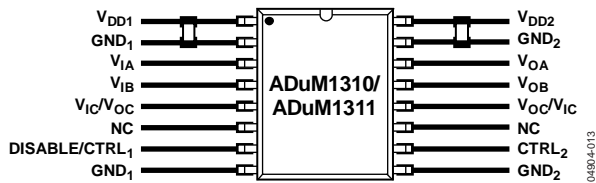


Figure 13. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, care should be taken to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the device's absolute maximum ratings, thereby leading to latch-up or permanent damage.

See the [AN-1109 Application Note](#) for board layout guidelines.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time of a low-to-high transition.

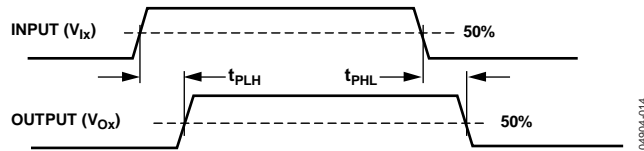


Figure 14. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the input signal's timing is preserved.

Channel-to-channel matching refers to the maximum amount the propagation delay differs between channels within a single ADuM1310/ADuM1311 component.

Propagation delay skew refers to the maximum amount the propagation delay differs between multiple ADuM1310/ADuM1311 components operating under the same conditions.

DC CORRECTNESS AND MAGNETIC FIELD IMMUNITY

Positive and negative logic transitions at the isolator input cause narrow (~ 1 ns) pulses to be sent to the decoder via the transformer. The decoder is bistable and is therefore either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~ 1 μs , a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than about 5 μs , the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default state (see Table 13) by the watchdog timer circuit.

The magnetic field immunity of the ADuM1310/ADuM1311 is determined by the changing magnetic field, which induces a voltage in the transformer's receiving coil large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM1310/ADuM1311 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2; n = 1, 2, \dots, N$$

where:

β is magnetic flux density (gauss).

r_n is the radius of the nth turn in the receiving coil (cm).

N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM1310/ADuM1311 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field at a given frequency can be calculated. The result is shown in Figure 15.

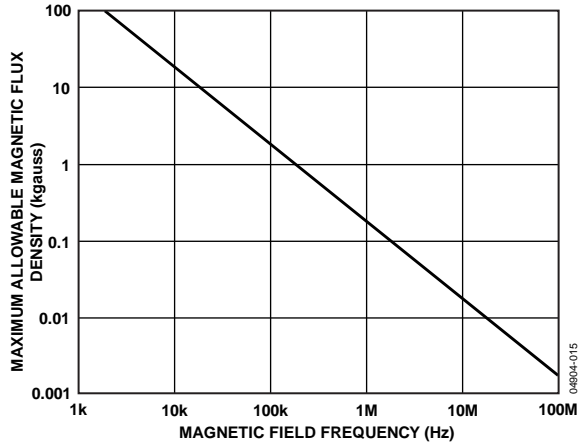


Figure 15. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurred during a transmitted pulse (and had the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM1310/ADuM1311 transformers. Figure 16 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM1310/ADuM1311 is extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted, a 0.5 kA current would have to be placed 5 mm away from the ADuM1310/ADuM1311 to affect the component's operation.

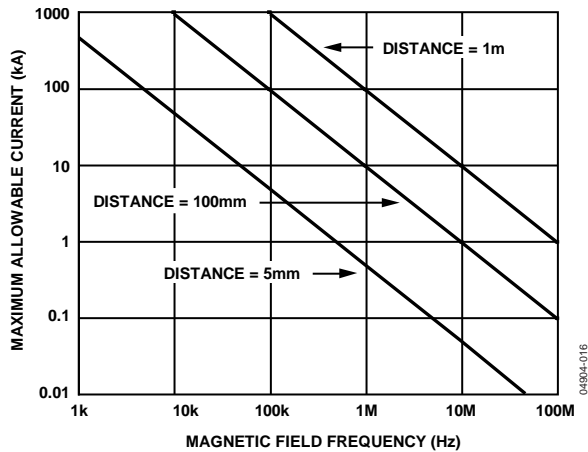


Figure 16. Maximum Allowable Current for Various Current-to-ADuM1310/ADuM1311 Spacings

Note that, at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce error voltages sufficient to trigger succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM1310/ADuM1311 isolator is a function of the supply voltage, the channel data rate, and the channel output load.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI(Q)} \quad f \leq 0.5 f_r$$

$$I_{DDI} = I_{DDI(D)} \times (2f - f_r) + I_{DDI(Q)} \quad f > 0.5 f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO(Q)} \quad f \leq 0.5 f_r$$

$$I_{DDO} = (I_{DDO(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO(Q)} \quad f > 0.5 f_r$$

where:

$I_{DDI(D)}$, $I_{DDO(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).

C_L is the output load capacitance (pF).

V_{DDO} is the output supply voltage (V).

f is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.

f_r is the input stage refresh rate (Mbps).

$I_{DDI(Q)}$, $I_{DDO(Q)}$ are the specified input and output quiescent supply currents (mA).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. The ADuM1310/ADuM1311 contains an internal data channel that is not available to the user. This channel is in the same orientation as Channel A and consumes quiescent current. The contribution of this channel must be included in the total quiescent current calculation for each supply. Figure 6 and Figure 7 show per-channel supply currents as a function of data rate for an unloaded output condition. Figure 8 shows per-channel supply current as a function of data rate for a 15 pF output condition. Figure 9 through Figure 12 show total V_{DD1} and V_{DD2} supply current as a function of data rate for ADuM1310/ADuM1311 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the [ADuM1310/ADuM1311](#).

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 10 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA/VDE approved working voltages. In many cases, the approved working voltage is higher than 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the [ADuM1310/ADuM1311](#) depends on the voltage waveform type imposed across the isolation barrier. The *iCoupler* insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 17, Figure 18, and Figure 19 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 10 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage case. Any cross-insulation voltage waveform that does not conform to Figure 18 or Figure 19 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 10.

Note that the voltage presented in Figure 18 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

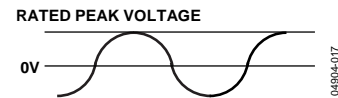


Figure 17. Bipolar AC Waveform

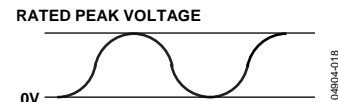


Figure 18. Unipolar AC Waveform

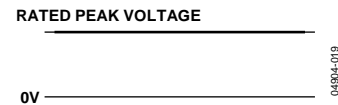
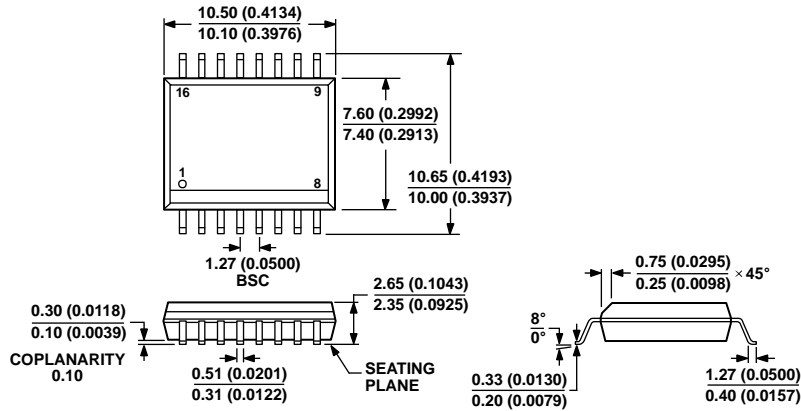


Figure 19. DC Waveform

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 20. 16-Lead Standard Small Outline Package [SOIC_W]
 Wide Body (RW-16)
 Dimensions shown in millimeters and (inches)

ORDERING GUIDE

| Model ¹ | Number of Inputs, V _{DD1} Side | Number of Inputs, V _{DD2} Side | Maximum Data Rate (Mbps) | Maximum Propagation Delay, 5 V (ns) | Maximum Pulse Width Distortion (ns) | Temperature Range | Package Description | Package Option |
|--------------------|---|---|--------------------------|-------------------------------------|-------------------------------------|-------------------|-----------------------------------|----------------|
| ADuM1310ARWZ | 3 | 0 | 1 | 100 | 40 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM1310ARWZ-RL | 3 | 0 | 1 | 100 | 40 | -40°C to +105°C | 16-Lead SOIC_W, 13" Tape and Reel | RW-16 |
| ADuM1310BRWZ | 3 | 0 | 10 | 50 | 5 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM1310BRWZ-RL | 3 | 0 | 10 | 50 | 5 | -40°C to +105°C | 16-Lead SOIC_W, 13" Tape and Reel | RW-16 |
| ADuM1311ARWZ | 2 | 1 | 1 | 100 | 40 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM1311ARWZ-RL | 2 | 1 | 1 | 100 | 40 | -40°C to +105°C | 16-Lead SOIC_W, 13" Tape and Reel | RW-16 |
| ADuM1311BRWZ | 2 | 1 | 10 | 50 | 5 | -40°C to +105°C | 16-Lead SOIC_W | RW-16 |
| ADuM1311BRWZ-RL | 2 | 1 | 10 | 50 | 5 | -40°C to +105°C | 16-Lead SOIC_W, 13" Tape and Reel | RW-16 |

¹ Z = RoHS Compliant Part.



NOTES

NOTES

NOTES

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View ADUM1311BRWZ-RL on WIN SOURCE](#)
-  [Analog Devices Inc. Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management